

Next-gen Power Systems with CoolSiC™ 1200 V SiC MOSFETs

IPCEI Microelectronics and Communication Technologies

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restricted

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Introduction

History

Early SiC development

Commercial SiC devices are 24 years old

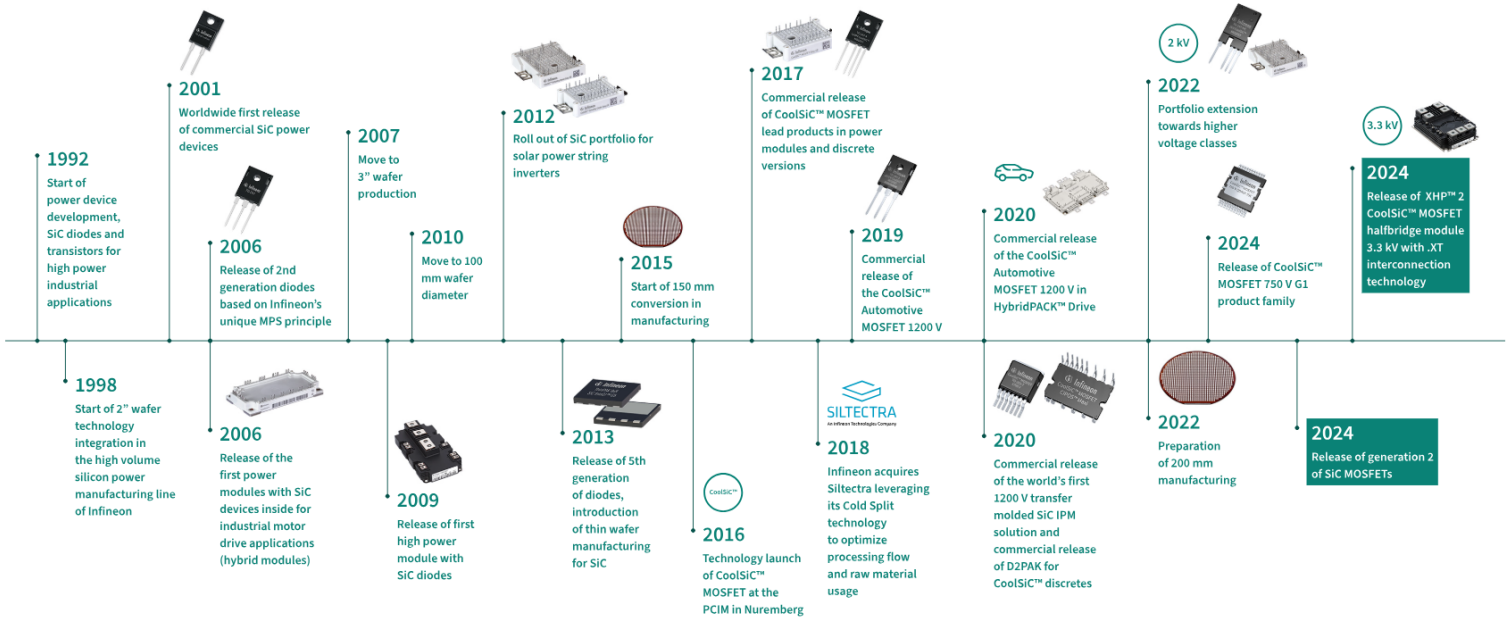
(Different cost, quality and availability as today

First commercial SiC Schotty diodes:

- 2001 – Infineon
- 2002 – Cree (today Wolspeed)

First commercial SiC MOSFETs

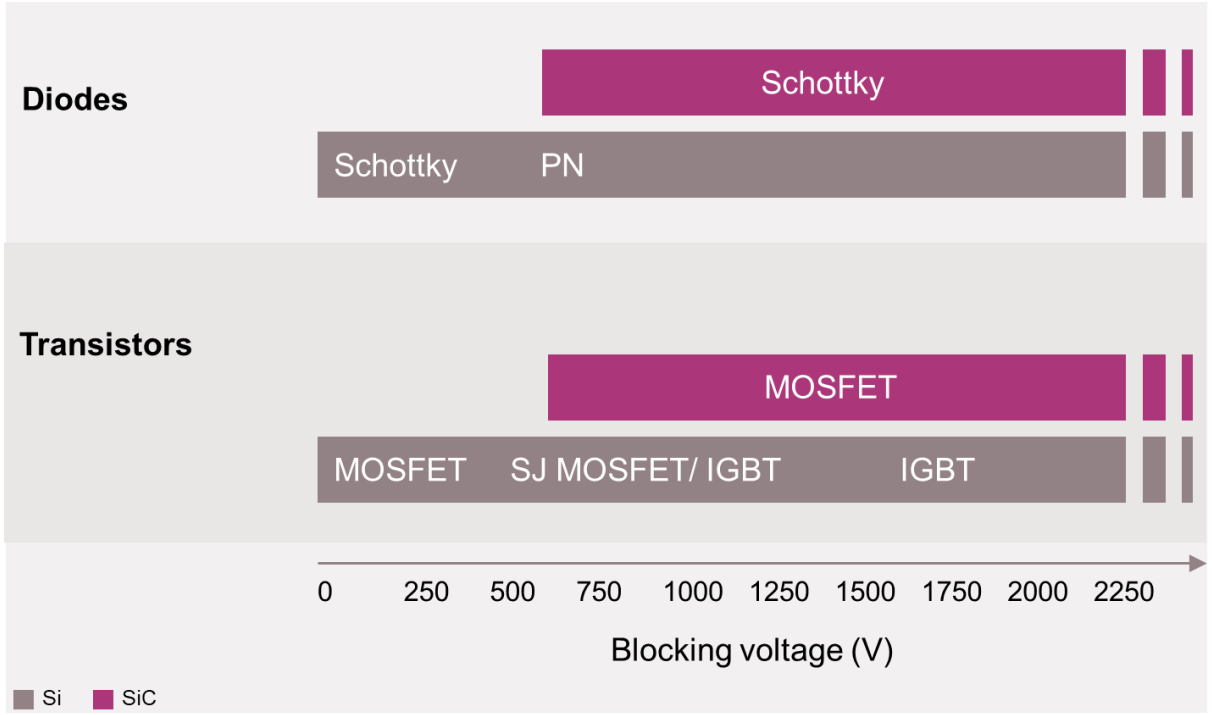
- 2011 – Cree (today Wolfspeed)
- 2017 – Infineon



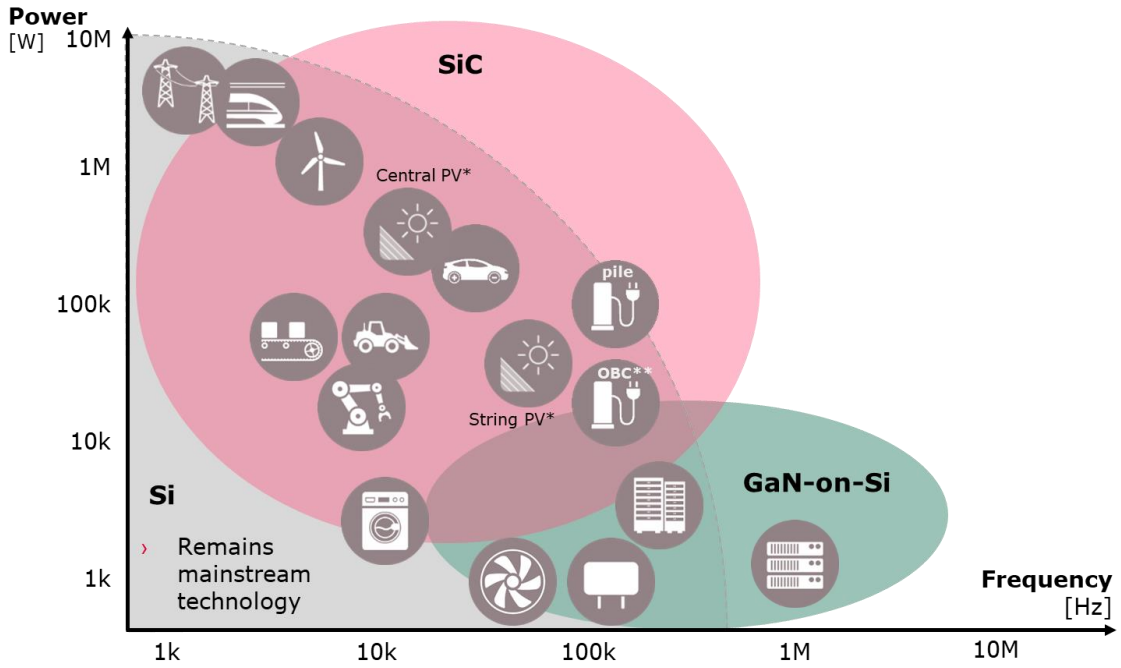
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Silicon carbide material MOSFETs target applications

- **Silicon Carbide Materials expand MOSFET Voltage Rating**



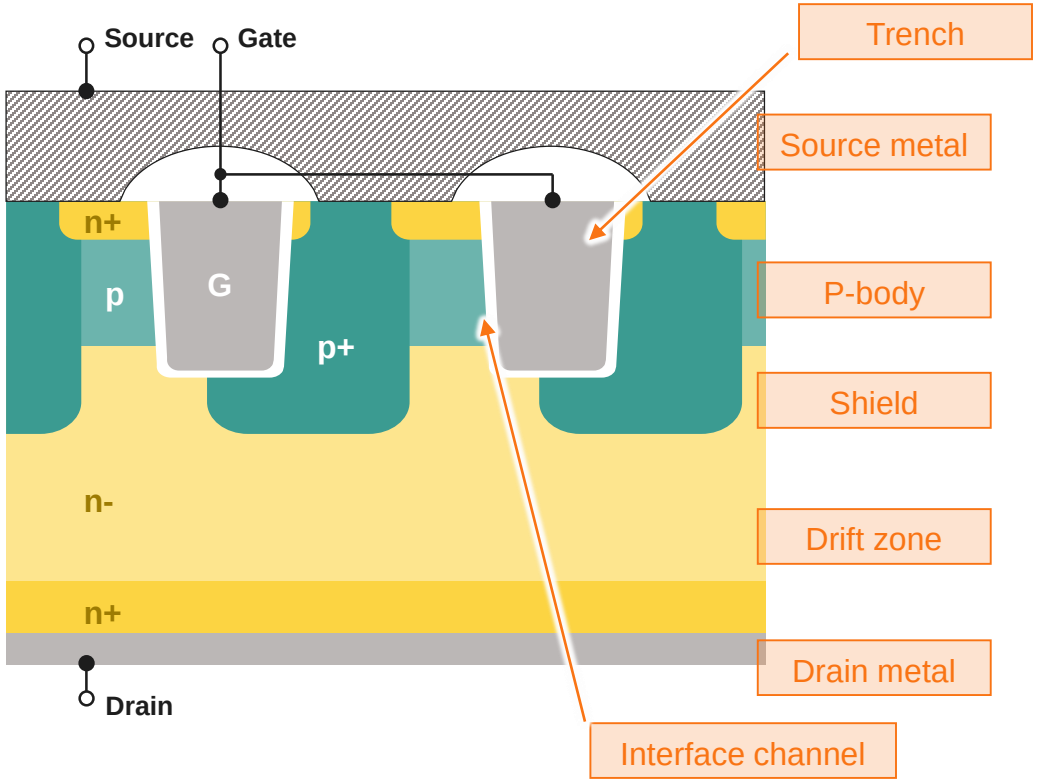
- **Target application range for SiC MOSFETs**



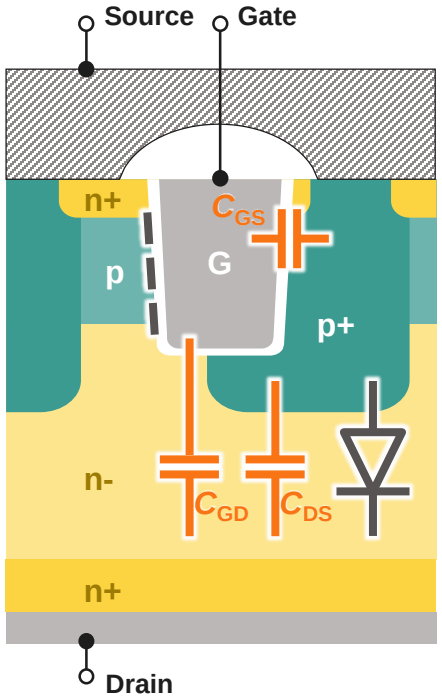
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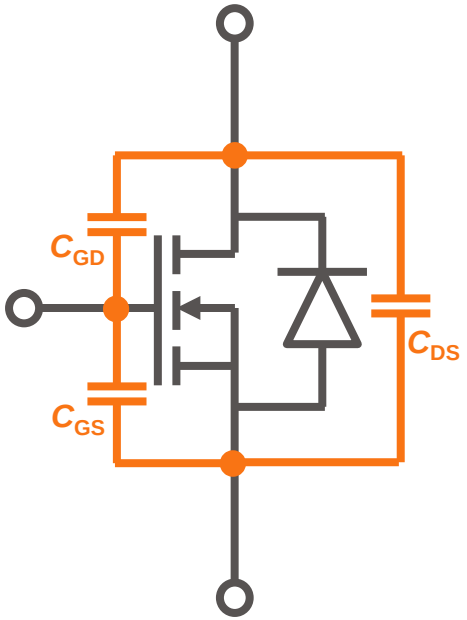
Construction & basic behavior

Construction



What does that mean for an electrical engineer?





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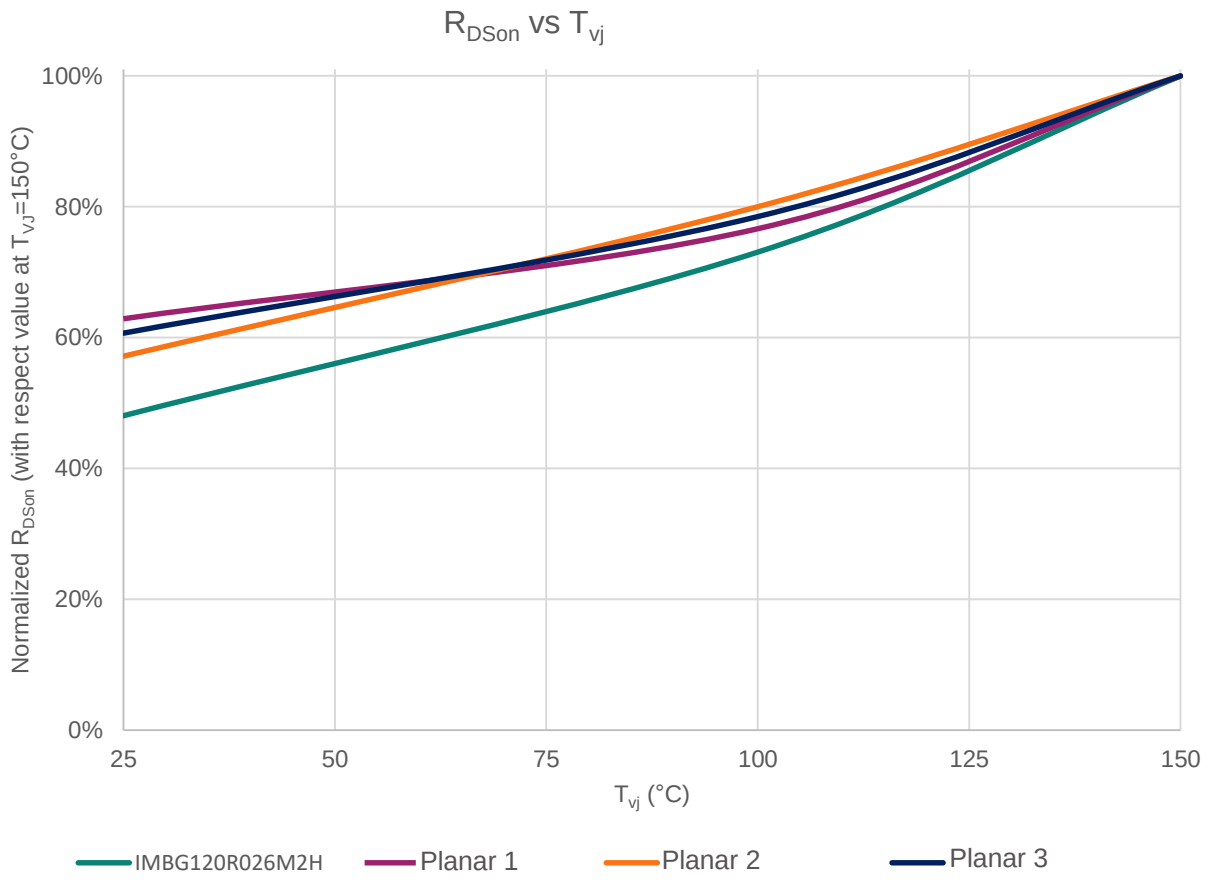
SiC MOSFET R_{DSon} versus temperature

- SiC MOSFET on-resistance has a positive temperature coefficient
- CoolSiC™ Trench curve is more steep than planar competitor devices

Advantage?

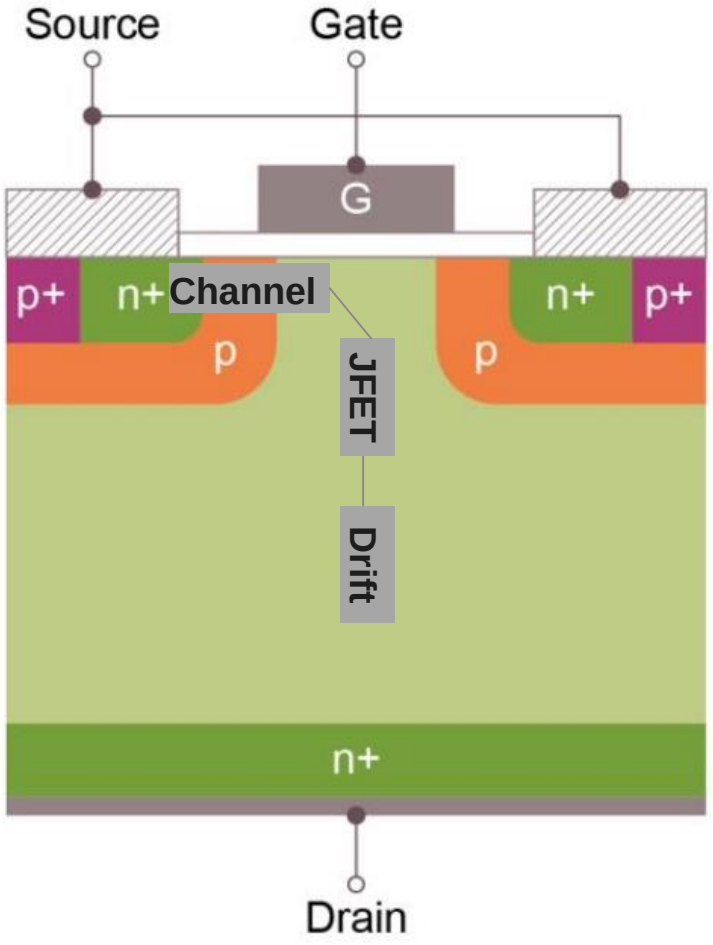
or

Disadvantage?

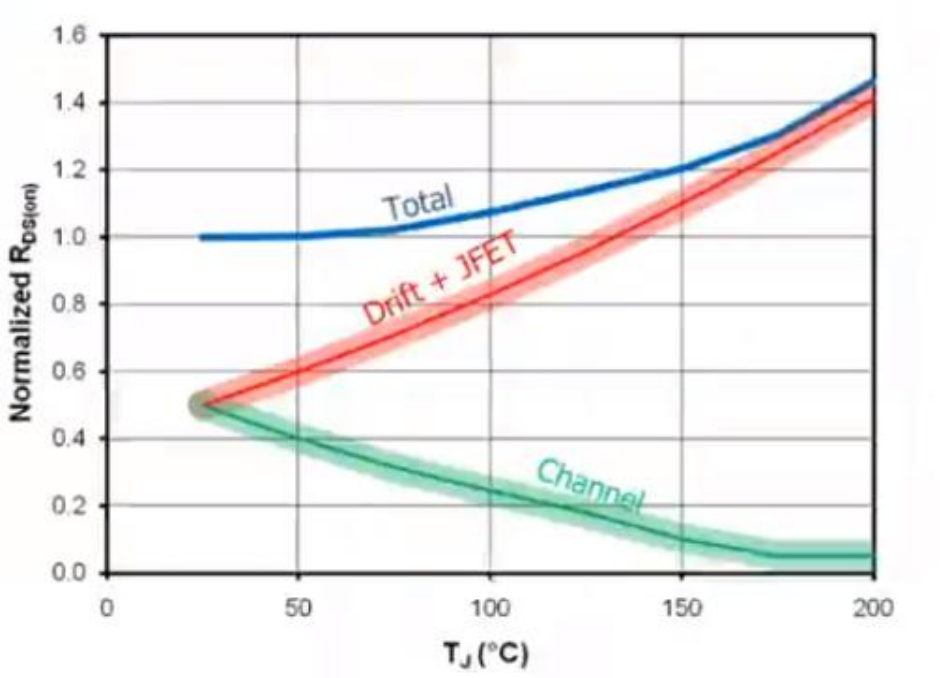


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Temperature dependence of on-resistance of SiC MOSFETs



$R_{DSon} = R_{channel} + R_{Drift} + R_{JFET}$



- $R_{channel}$ → negative temperature coefficient
- $R_{Drift+JFET}$ → positive temperature coefficient
- R_{DSon} temperature coefficient depends on the share between the three components

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CoolSiC™ MOSFET 1200 V G2 technology: faster, cooler and more robust device





CoolSiC™ Generation 2





Enhanced switching performance and FOM factors	25% lower switching losses, 10% total power loss reduction with 0.1% higher efficiency
Improved .XT interconnection technology	>15% better thermal resistance, $R_{th,j-c}$ 11% lower MOSFET temperature
Best-in-class $R_{DS(on)}$ and broad portfolio	4 mOhm in QDPAK and 8 mOhm in D2PAK package
Overload operation up to T_{vj} = 200°C	Ruggedness against overcurrent events
Parasitic turn-on robustness	Enhances reliability against Miller effect allowing unipolar drive (0 V Gate voltage)
Short-circuit max. rating of 2µs exclusively guaranteed by Infineon	Increases system reliability to withstand transient overloads
Tight $V_{GS(th)}$ and transfer characteristics distribution, and a lower negative temp. Coeff.	Enhanced reliability and performance in paralleling operation
Maximum $R_{DS(on)}$ at high temperature specified in datasheet	Simplifies and optimizes system design

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Application Driven Selection and System Impact

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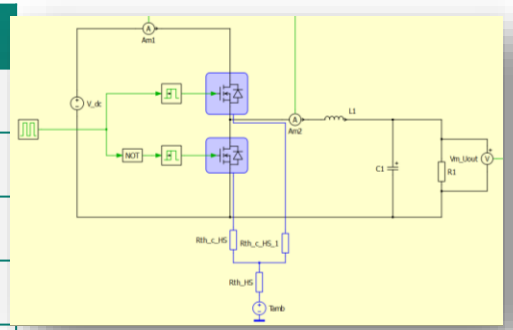
Renewable Energy Conversion

Solar MPPT and Inverter

Performance Comparison of CoolSiC™ G2 vs. G1 in Buck (synchronous)

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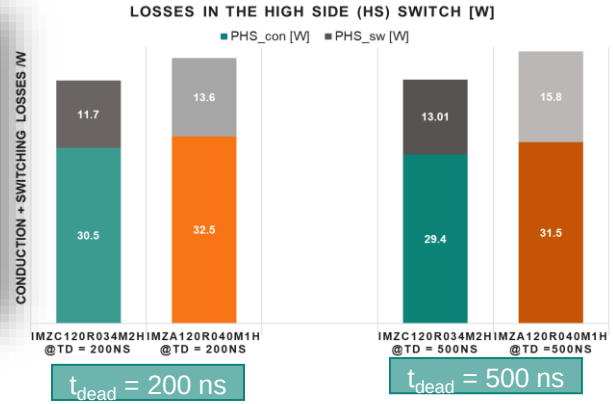
Parameters	Values
V_{in}	890 V_{DC}
V_{out}	500 V_{DC}
f_{sw}	30 kHz
I_{avg} / ripple	30 A / 20 %
R_{GON}/R_{GON}	2.5 ohm
$R_{th_c_hs}$	0.5 K/W
R_{th_HS} /per device	1 K/W
$T_{ambient}$	50 °C
V_{GS}	0/18V



40 mΩ G1

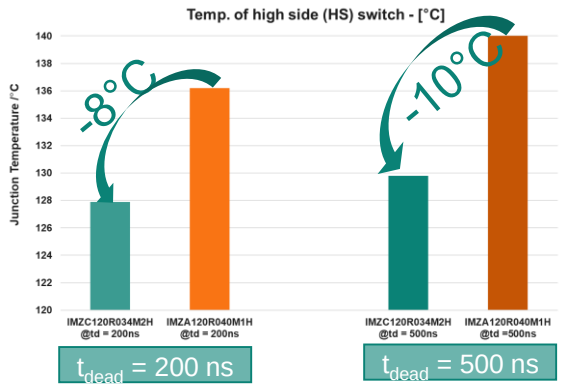
With improved system performance

34 mΩ G2



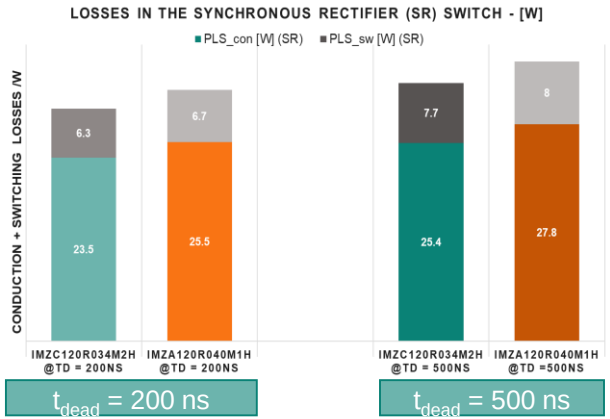
t_{dead} = 200 ns

t_{dead} = 500 ns



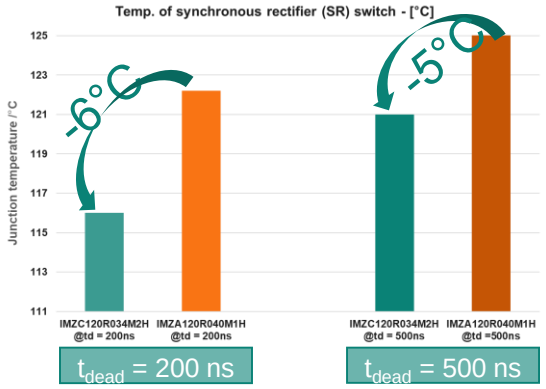
t_{dead} = 200 ns

t_{dead} = 500 ns



t_{dead} = 200 ns

t_{dead} = 500 ns



t_{dead} = 200 ns

t_{dead} = 500 ns

➢ Results and Take away:

1. For these system specifications, replacing a 40 mΩ G1 with a 34 mΩ G2 improves performance, resulting in lower total losses and reduced device temperature!
2. (**!!!**) The performance improves with shorter dead time:
   - ➔ **Deatime = 200 ns** ➔ high side (HS) G2 is 8°C cooler than G1 and the low side (SR) switch G2 is 10°C cooler than G1
   - ➔ **Deatime = 500 ns** ➔ HS G2 is 6°C cooler than G1 and the SR switch G2 is 5°C cooler than G1

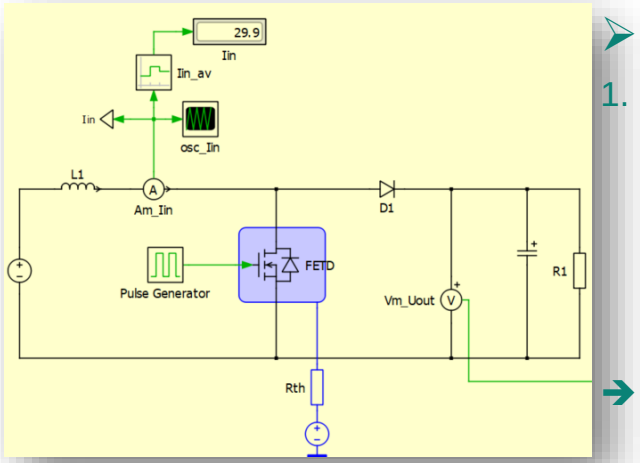
➔ Increasing the dead time from 200 ns to 500 ns increases the total device losses (in G2) by 5% and raises the SR switch temperature by 5°C.

➔ Increasing dead time reduces the conduction time of the HS switch and slightly reduces conduction loss.

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Performance Comparison of CoolSiC™ G2 vs. G1 in Boost

Parameters	Values
V_{in}	500 VDC
V_{out}	890 VDC
f_{sw}	45 kHz
I_{avg} / ripple	30 A / 20 %
R_{GON}/R_{GON}	2.5 ohm
$R_{th_c_hs}$	0.5 K/W



Results and Take away:

1. for the system specification (defining the worst case for a boost MPPT stage), replacing 30 mΩ G1 by 26 mΩ G2 improves the performance, resulting in:
   - ➔ lower total losses and reduced device temperature!
   - ➔ (!!!) Depending on the thermal assembly and heatsink condition, the percentage improvement varies!!

➔ Senario 1 depicts a (realistic) condition where heatsink temperature changes based on the total power losses from the heat source (devices)

➔ Senario 2 depicts that the heatsink is maintained to a fixed temperature regardless of the losses from the heat source ➔ providing a higher offset for a lower loss scenario and an optimal case for higher total losses

30 mΩ G1 → With improved system performance → 26 mΩ G2

cases	Device	P_{con} [W]	P_{sw} [W]	P_{tot} [W]	T_{HS} [°C]	T_j [°C]
Senario 1: R_{th_hs} = 1 K/W & $T_{ambient}$ = 50 °C	IMZC120R026M2H	16.6	17.3	33.9	83.8	114.8
	IMZA120R030M1H	18	18.6	36.6	86	120.4
Senario 2: fixed heatsink temperature T_{HS} = 85 °C	IMZC120R026M2H	16.8	17.3	34.1	85	116.2
	IMZA120R030M1H	17.8	18.5	36.3	85	118.7

~8 % lower total losses ➔ improved the device temperature by 6°C

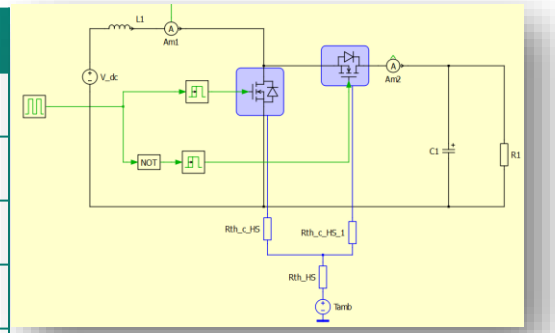
~6 % lower total losses ➔ improved the device temperature by 2°C

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Performance Comparison of CoolSiC™ G2 vs. G1 in Boost (synchronous)

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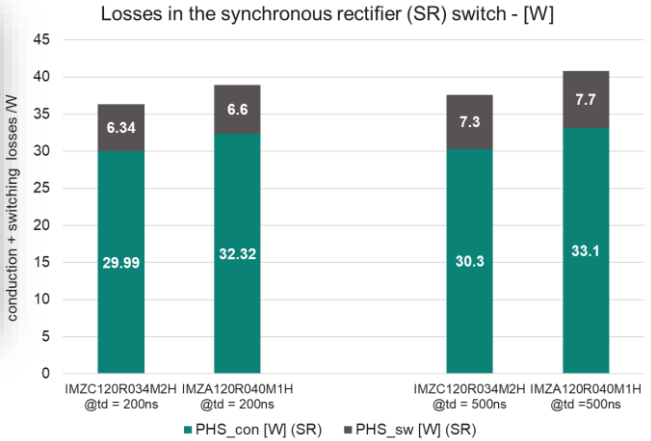
Parameters	Values
V_{in}	500 V_{DC}
V_{out}	890 V_{DC}
f_{sw}	30 kHz
I_{avg} / ripple	30 A / 20 %
R_{GON}/R_{GON}	2.5 ohm
$R_{th_c_hs}$	0.5 K/W
R_{th_HS} /per device	1 K/W
$T_{ambient}$	50 °C
V_{GS}	0/18V

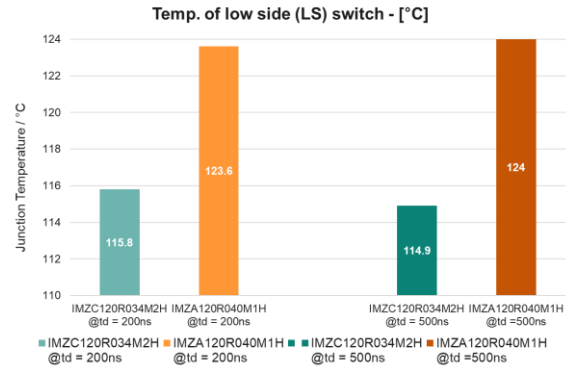


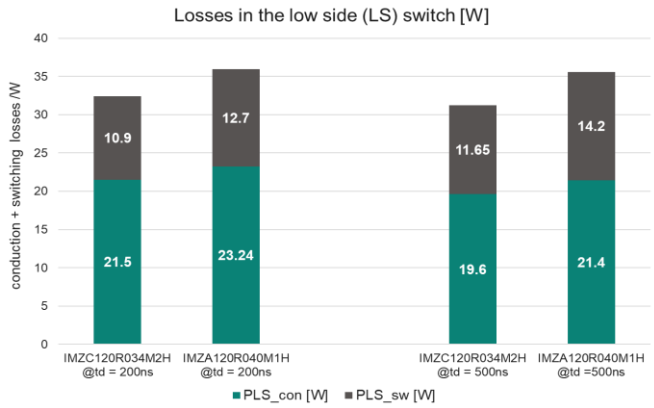
40 mΩ G1

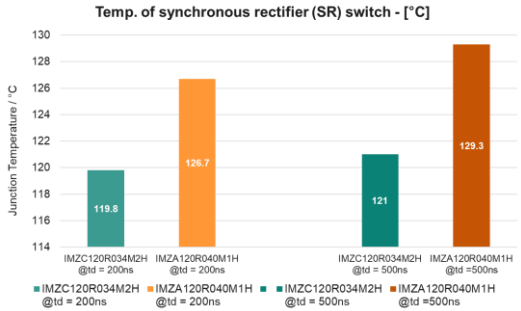
With improved system performance

34 mΩ G2









➢ Results and Take away:

1. For these system specifications, replacing a 40 mΩ G1 with a 34 mΩ G2 improves performance, resulting in lower total losses and reduced device temperature!
2. (**!!!**) The performance improves with shorter dead time:
   - ➔ **Deatime = 200 ns** ➔ Low side (LS) G2 is 8°C cooler than G1 and the high side (SR) switch G2 is 7°C cooler than G1
   - ➔ **Deatime = 500 ns** ➔ LS G2 is 9°C cooler than G1 and the SR switch G2 is 8°C cooler than G1

➔ Increasing dead time reduces the conduction time of the LS switch and slightly reduces conduction loss.

➔ Replacing G1 by G2 **allows an increase in switching frequency by 10 kHz** in the same thermal assembly condition

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CoolSiC™ Optimized $R_{DS(ON)}$ Selection for MPPT stages

Parameters	Values
V_{in}	450 V_{DC}
V_{out}	850 V_{DC}
f_{sw}	45 kHz
I_{avg} / ripple	20 A / 25 %
R_{GON}/R_{GOFF}	3.6/ 4.7 Ω
$R_{th_c_hs}$ /$T_{heastink}$	0.5 K/W / 85 °C

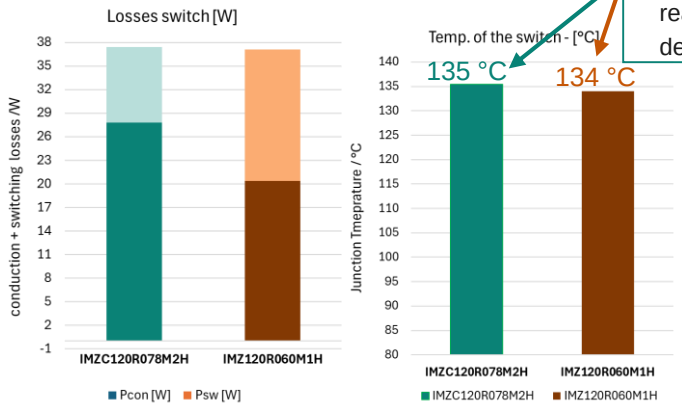
Parameters	Values
V_{in}	500 V_{DC}
V_{out}	880 V_{DC}
f_{sw}	45 kHz
I_{avg} / ripple	36 A / 25 %
R_{GON}/R_{GOFF}	3.0/ 3.0 Ω
$R_{th_c_hs}$ /$T_{heastink}$	0.5 K/W / 85 °C

Parameters	Values
V_{in}	500 V_{DC}
V_{out}	890 V_{DC}
f_{sw}	45 kHz
I_{avg} / ripple	42 A / 25 %
R_{GON}/R_{GOFF}	3.0/ 3.0 Ω
$R_{th_c_hs}$ /$T_{heastink}$	0.5 K/W / 85 °C

Design Boundary Condition: T_j < 145°C **Note**: The maximum allowed T_{vj} for continuous operation is 175°C and 200 °C for overload condition (100 h)

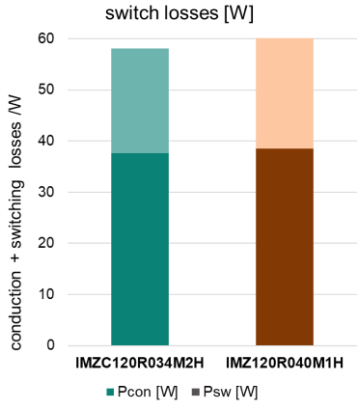
60 mΩ G1 with standard soft solder → 78 mΩ G2 .XT

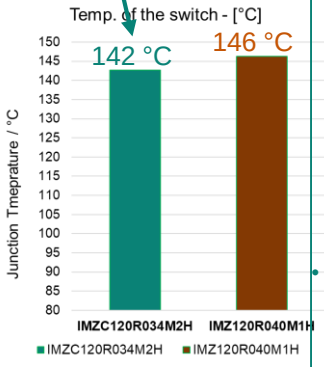
- more room to extend the output power range before reaching the defined T_{jmax}



40 mΩ G1 → 34 mΩ G2

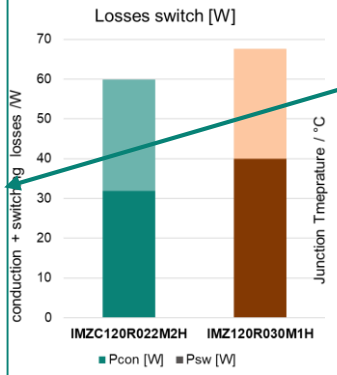
- 34 mΩ G2 fits well for these specs.

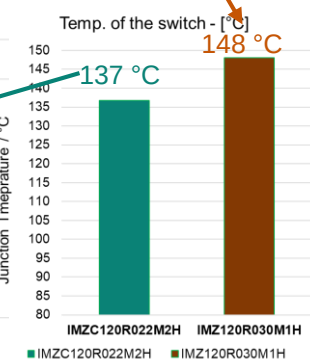




- G2 is capable of switching very fast hence, it's highly recommended to exploit the device fast switching capability. If lower Rgs are used then **26 mΩ G2** also fits quite well for these system specifications
- **22 mΩ G2** with more room to extend output power range

- 30 mΩ G1 ➔ can be used with lower Rg to improve the thermal, however, if that's not possible due to system limitation then the next possible $R_{DS(on)}$ class is 20 mΩ G1 for the given system spec.

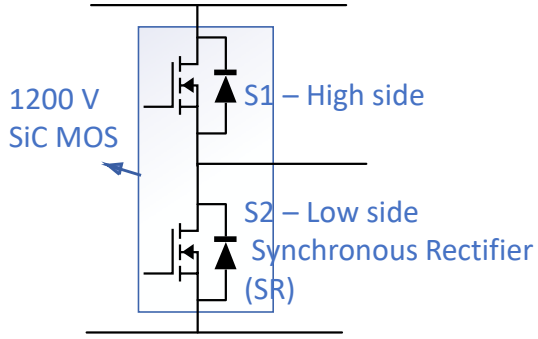




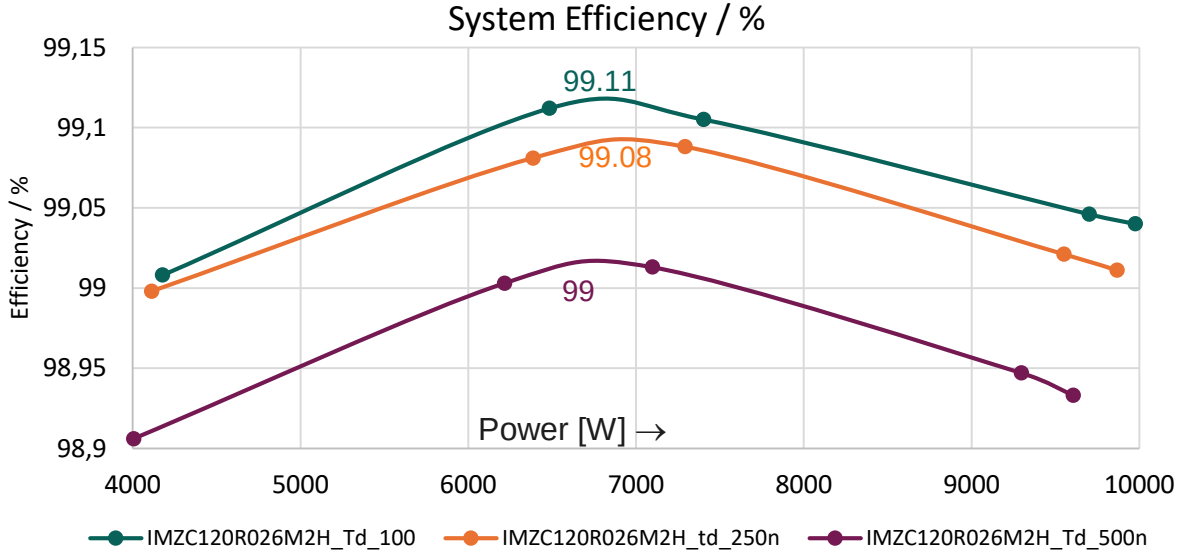
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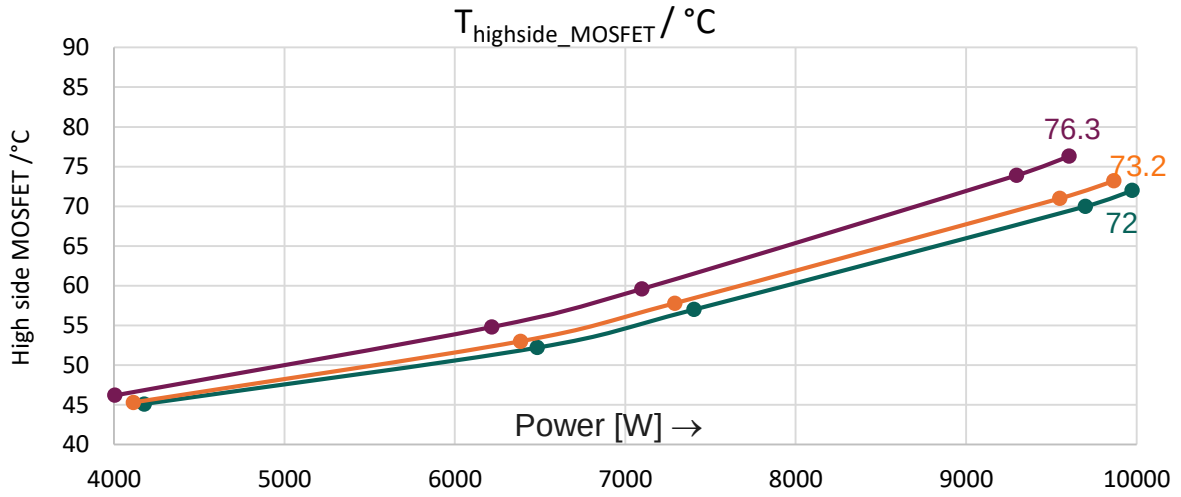
Application performance measurements – impact of dead time
Half bridge (solar inverter), CoolSiC™ G2 performance

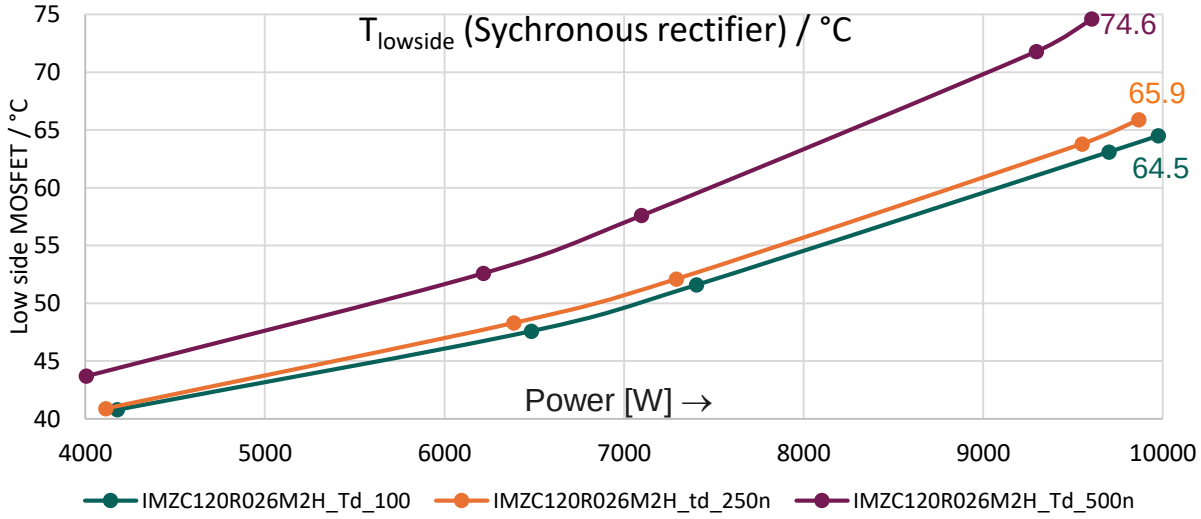
- **Test Conditions (Buck mode)**
  - f_{sw} = 60 kHz
  - R_G = 2.3 Ω, V_{GS} = -3 /18V
  - V_{DC} = 780 V
  - Duty = 60 %
  - I_{DCmax} = 21.7 A
  - Fan cooling, T_{amb} = 25°C
  - Dead time = 100ns, 250ns and 500ns



- shorter dead time lead to improved system performance (500n ➔ 100nsec)
  - 0.1% higher efficiency
  - Switching device 4 °C cooler and SR 10 °C cooler







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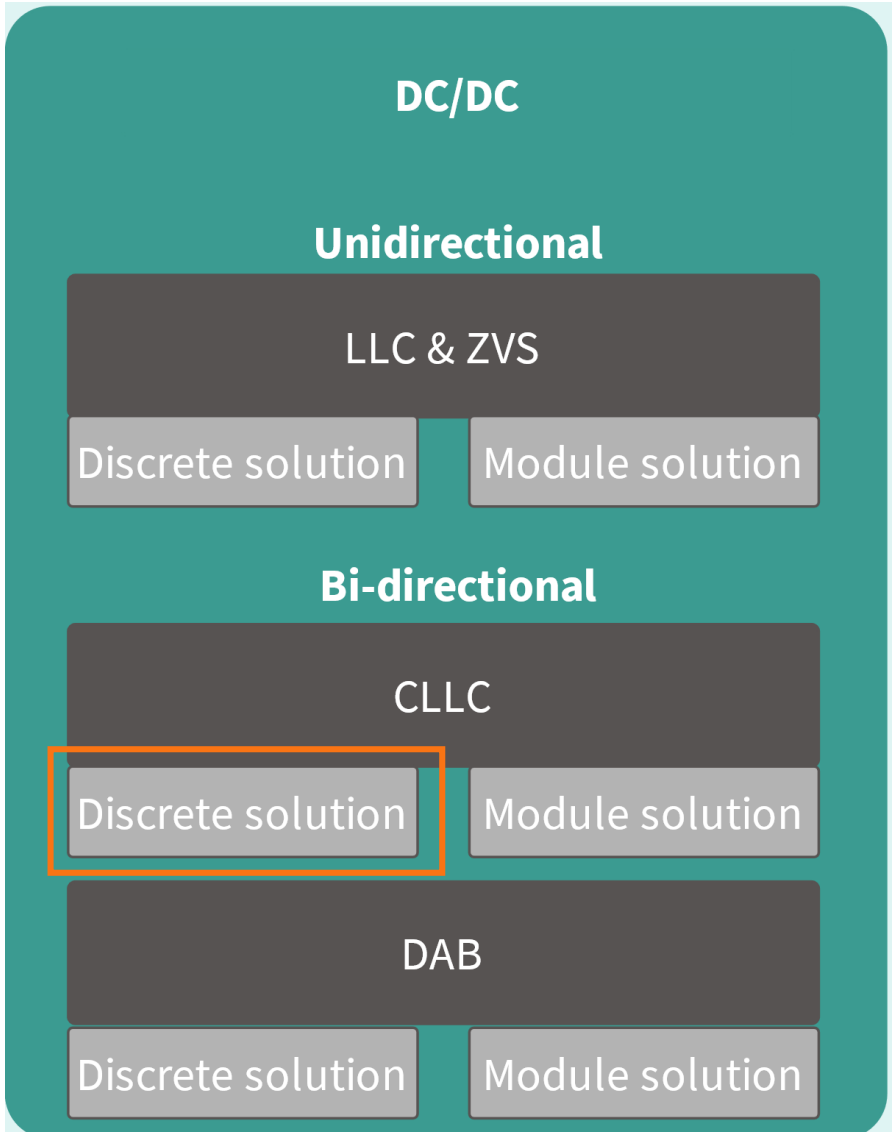
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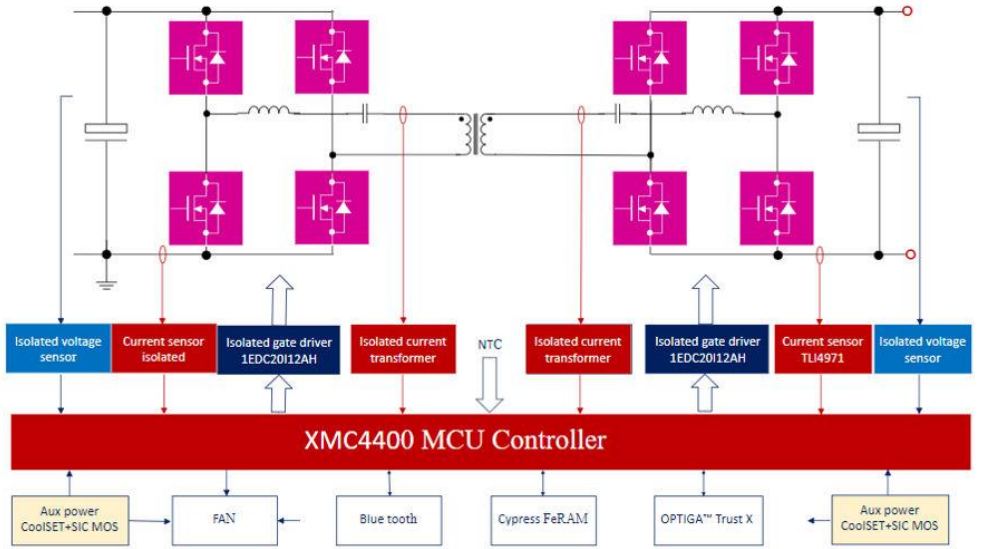
EV Charging

Bi-directional DC-DC CLLC Converter

11 kW SiC bi-directional DC/DC converter board for EV Charging and ESS applications

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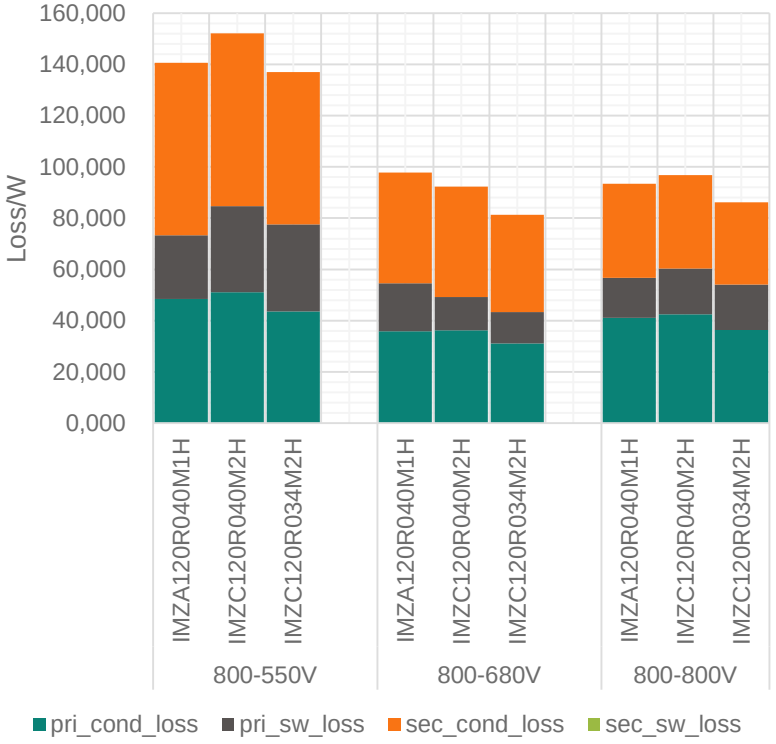


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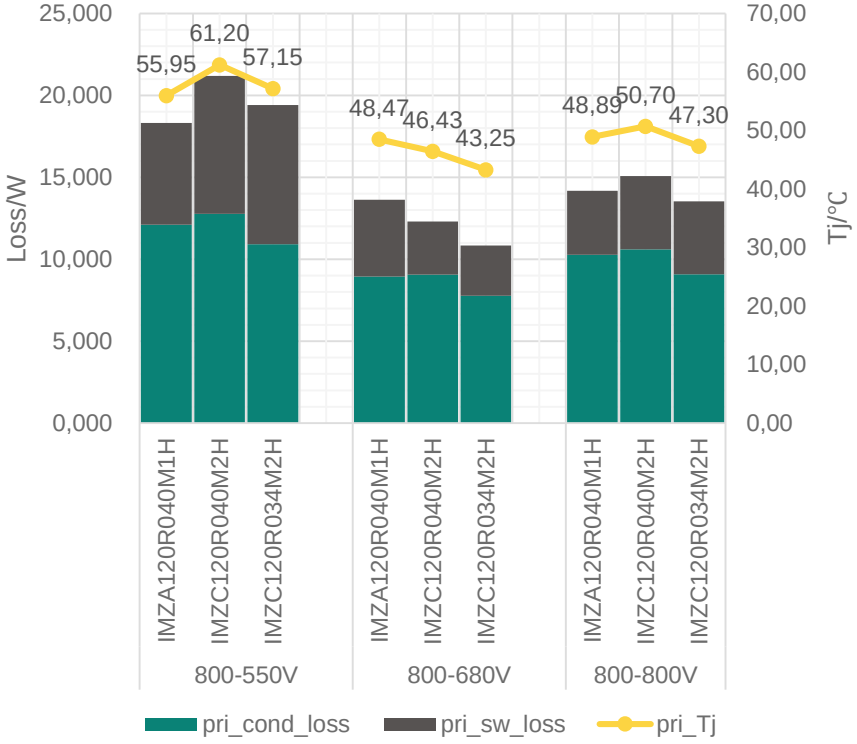
PLECS simulation G1 vs. G2 – full load (11kW), Forward mode, IMZA120R040M1H, IMZC120R040M2H, IMZC120R034M2H

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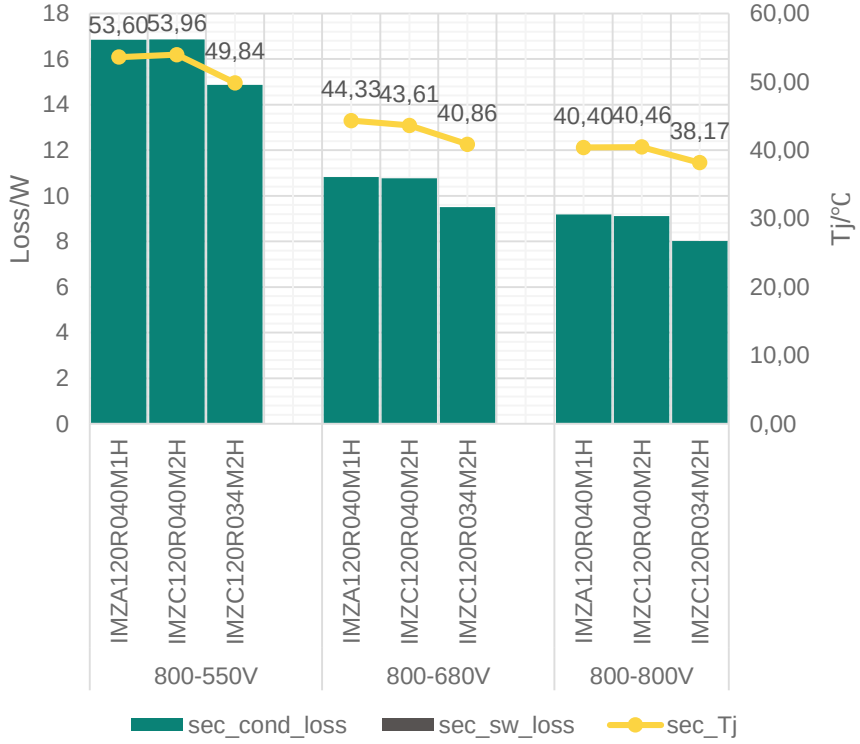
Total Loss



Primary Loss & Tj of a single device

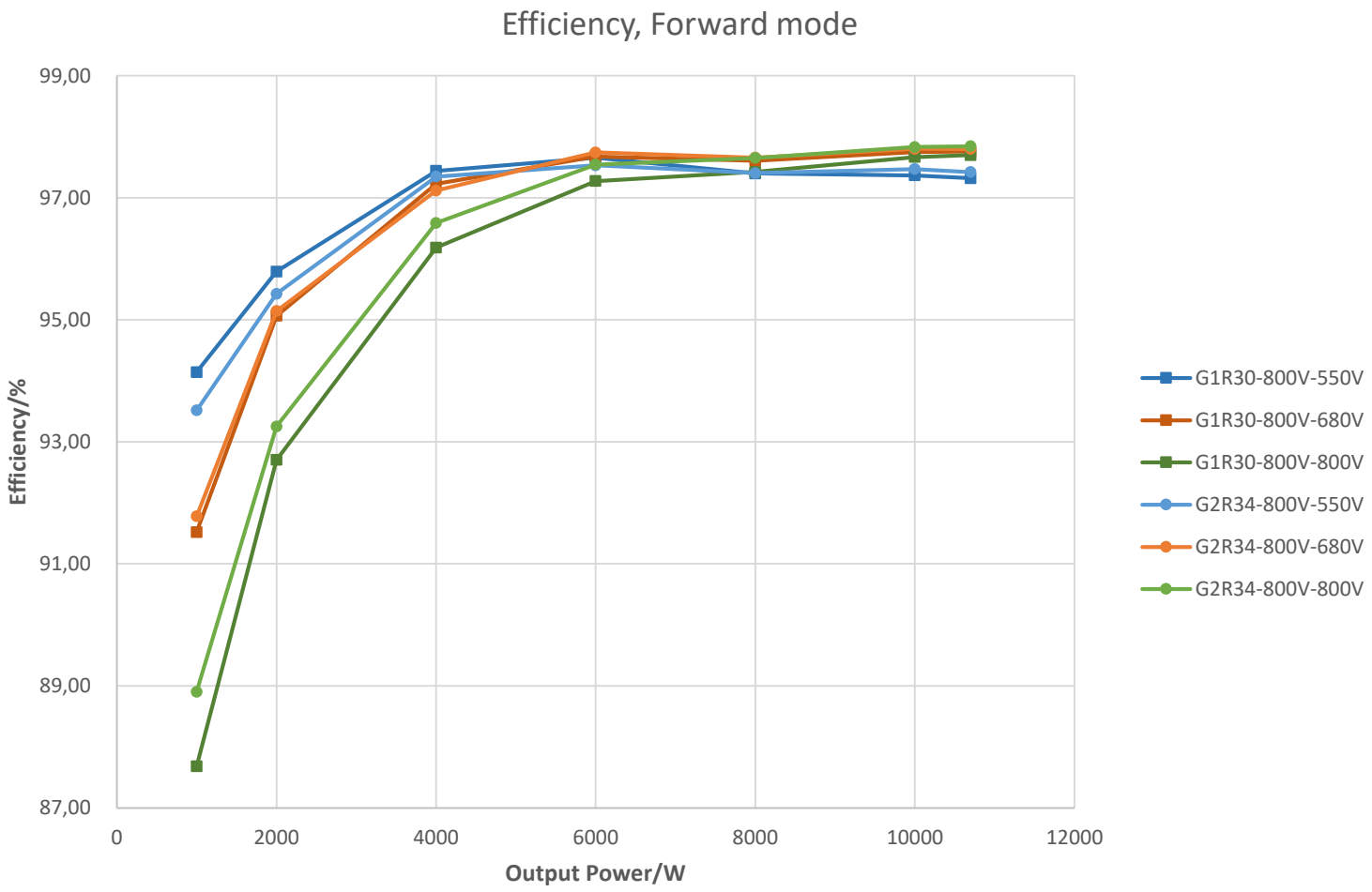


Secondary Loss & Tj of a single device

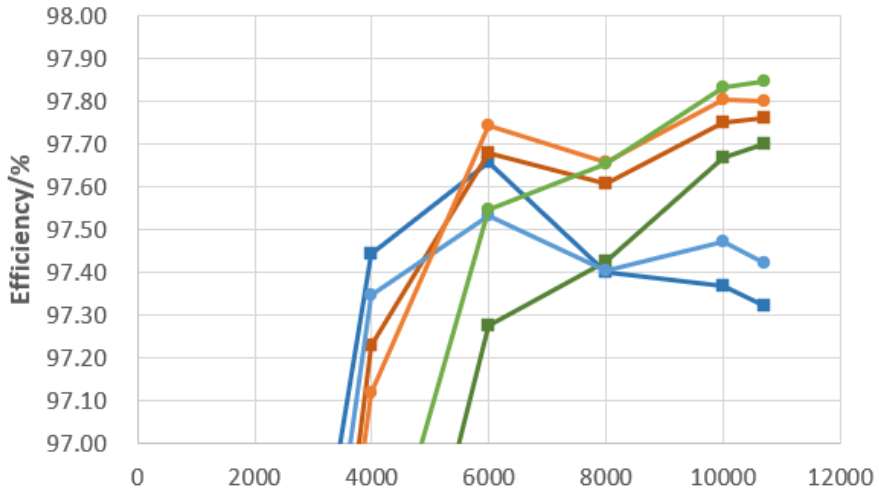


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Efficiency test – IMZC120R034M2H (G2) vs IMZ120R030M1H (G1)

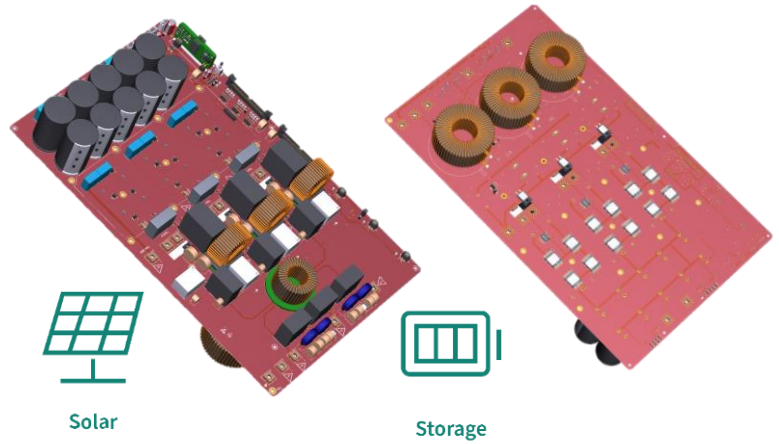


- 800V-550V (over-resonance) has the lowest efficiency at full load.
- At full load, 034M2H has slightly higher efficiency (~0.1%) than 030M1H.



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Assembly examples of the QDPAK variants in different systems and form factors

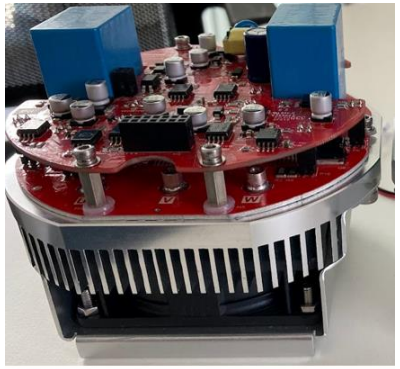


REF-10KW3LNPC2Q

- Power conversion design blueprint for fast prototyping of compact and highly efficient bi-directional 3-level NPC2 inverters with up to 10 kW
- Detailed PCB design files and modular hardware for the mainpower board with separate gate driver and aux power supply cards
- Optional: corresponding control card and executable software

Standard cooling assembly

Stack: FR4 + IMS + 



TSC cooling assembly

Stack: FR4 + 

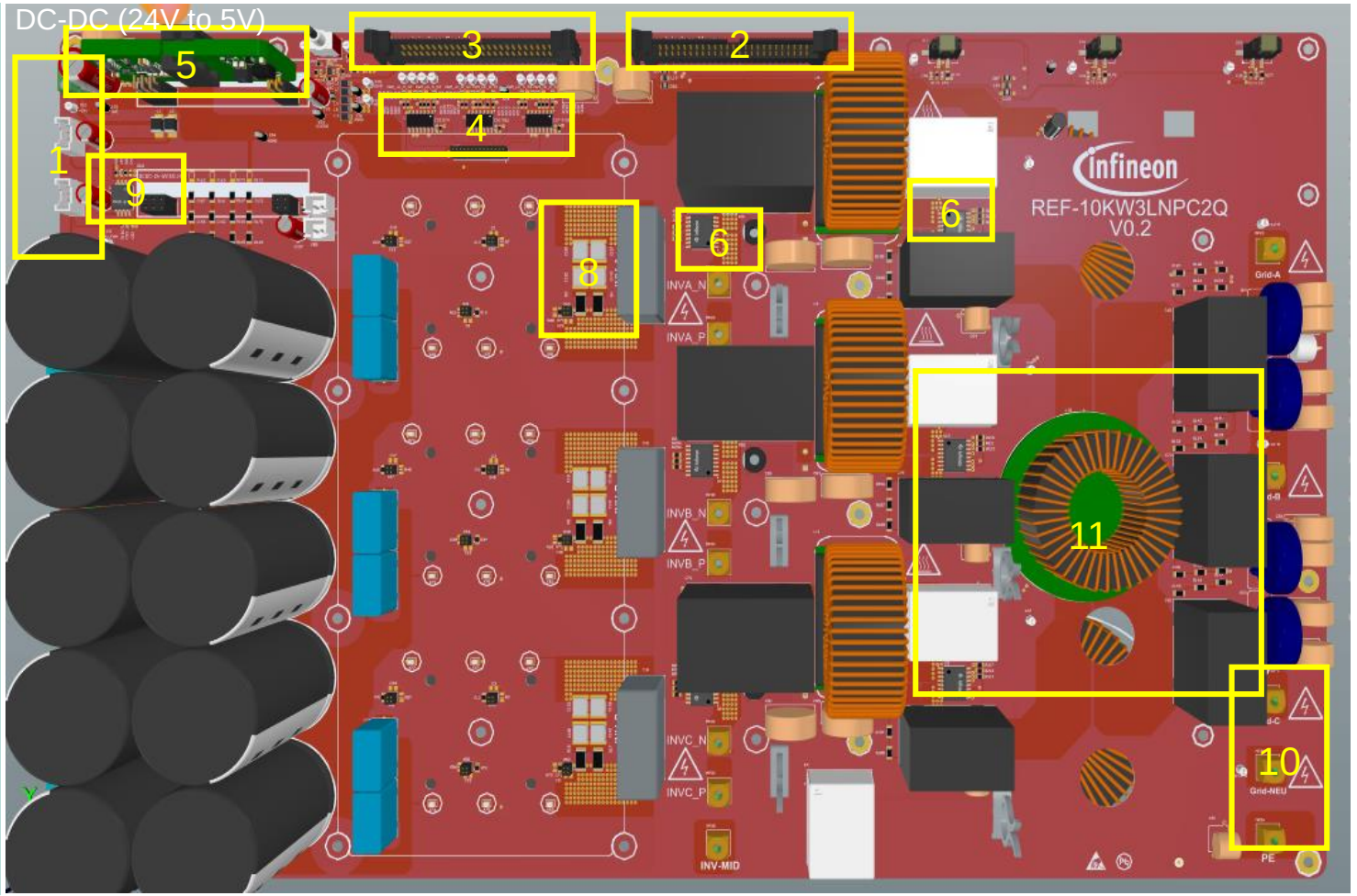


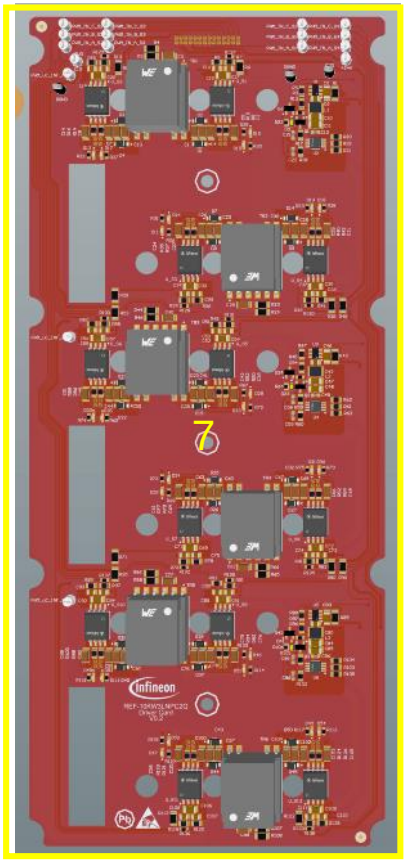
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REF-10KW3LNPC2Q Circuit Block Diagram

REF-10KW3LNPC2Q overview

1. Fan Header
2. Measurement Interface
3. Control Interface
4. Control signals protection
5. Aux-supply
6. Current sensor
7. Gate Drivers
8. Snubber for DC bus
9. Fan control
10. Output voltage connectors
11. EMI Filter





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Solid State Power Distribution

CoolSiC™ JFET 1200 V G1 in Q-DPAK top-side cooled package

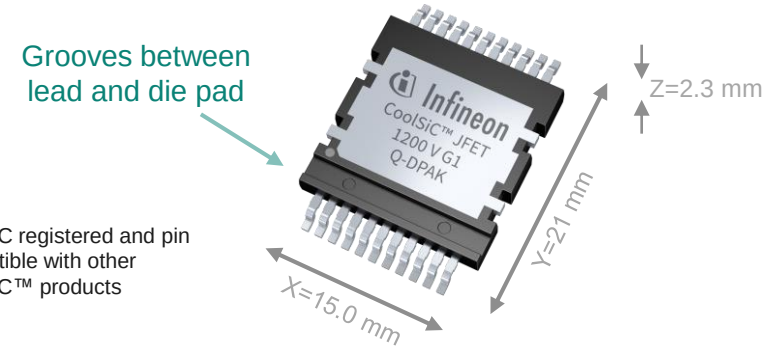
IPCEI Microelectronics and Communication Technologies

Key features

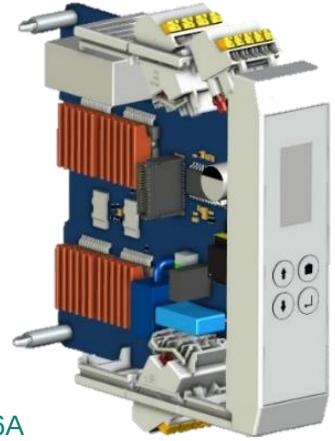
New CoolSiC™ JFET technology achieving industry-leading low Rdson x Area FoM
Conduction loss optimized technology for high robustness and reliability
Best-in-class $R_{DS(on)}$ ~ 2.3 mΩ in Q-DPAK top side cooled package
High inductive clamping capability
Avalanche rugged
High overload / overcurrent, high i^2t capability
Thermal stability in linear mode
Power / temperature cycling robustness
Reflow capability enables lower $R_{th,c-h}$ resulting in higher current output

Package design

*PG-HDSOP-22-3**



*JEDEC registered and pin compatible with other CoolSiC™ products



SSCB 16A
Reference Design

Target applications



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