

CoolSiC™ Automotive MOSFET 750 V G2



Blaž Rohseano

UNIVERSITY OF LJUBLJANA
FE Faculty of Electrical Engineering
Infineon
IPCEI Microelectronics and Communication Technologies

restricted

Table of contents

1 Role of Power Electronics in EV Car 3

2 Key Trends and Topologies 5

3 Infineon Technology Improvements 12

4 Infineon Packaging Innovation 22

Copyright © Infineon Technologies AG 2025. All rights reserved.

Table of contents

1 **Role of Power Electronics in EV Car** **3**

2 Key Trends and Topologies 5

3 Infineon Technology Improvements 12

4 Infineon Packaging Innovation 22

Copyright © Infineon Technologies AG 2025. All rights reserved.

Role of power electronics in a classic electric drive train

Power electronics in EV

On board charger

Converts the AC voltage from the Grid and motor to DC voltage for charging the battery, typically using an AC-DC converter.

Main Inverter

Converts the DC voltage from the battery and control the speed and torque of the motor, using techniques such as pulse-width modulation (PWM) and field-oriented control (FOC).

Auxiliary Inverter

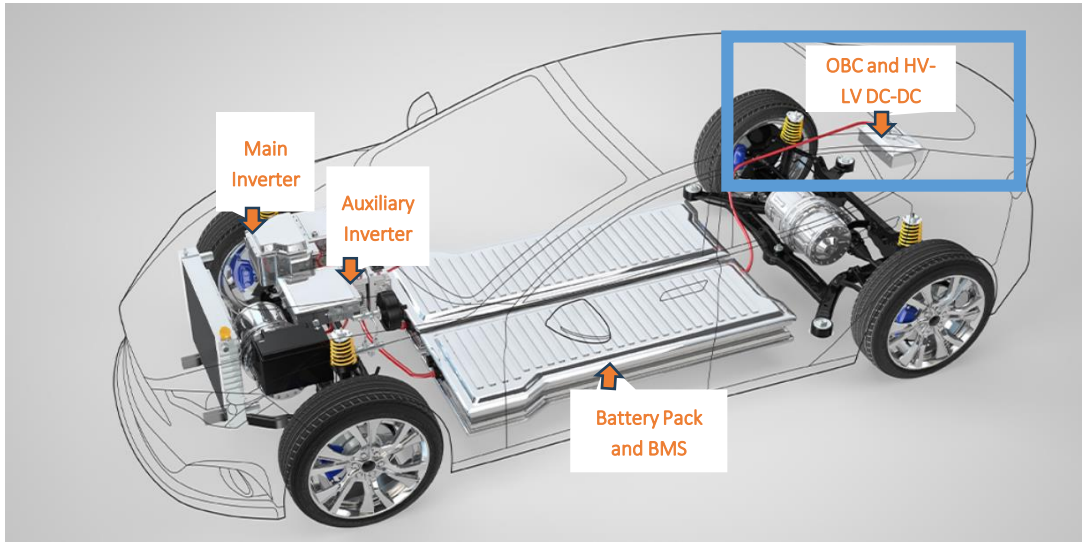
Converts the DC power from the traction battery into AC power to operate various auxiliary systems, such as the electric power steering, air conditioning compressor, water pumps, and other low-power motor drives

DC-DC converter

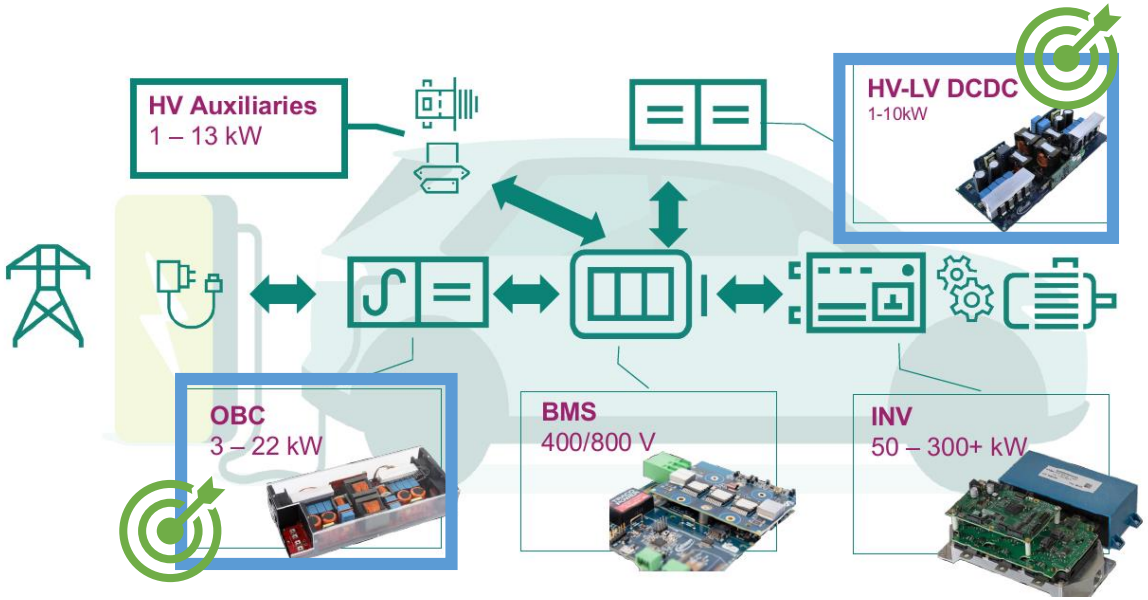
Converts the DC voltage from the battery to the required voltage for Auxiliary battery and load (12V)

BMS

Monitor and control the battery's state of charge, voltage, and temperature, ensuring safe and efficient operation.



750V SiC Focused applications



Copyright © Infineon Technologies AG 2025. All rights reserved.

Table of contents

1 Role of Power Electronics in EV Car 3

2 **Key Trends and Topologies** **5**

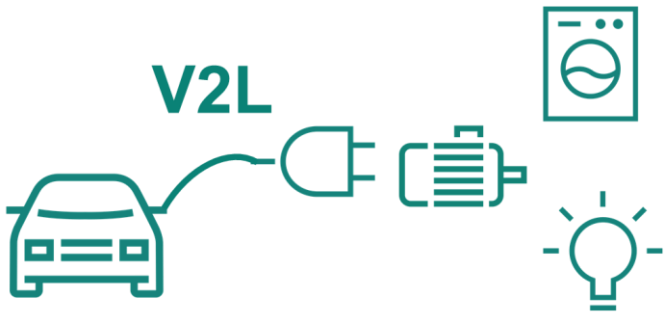
3 Infineon Technology Improvements 12

4 Infineon Packaging Innovation 22

Copyright © Infineon Technologies AG 2025. All rights reserved.

Key Trends in On Board Chargers (OBC)

1. Faster Charging
   – Higher Power
2. Longer travel range
   – Lighter, Power Density
3. System cost reduction
   – Less devices, less copper



Energy Storage Extension

AUTOMOTIVE 2-IN-1 CONVERTERS FOR EV – SYSTEMS COMPARISON

Source: Automotive Teardown Tracks, Yole SystemPlus, December 2024



	PCS2 Power Converter System	Combined Charging Unit (CCU)	DC/DC+OBC (D+C)
OBC output peak power	11kW	11kW	6.6kW
HV battery range	800V	400V	800V
LV battery range	48V	12V	12V
Power density (W/kg)	1.15W/cm³	1.13W/cm³	1.23W/cm³
Specific power (W/kg)	1.56kW/kg	1.27kW/kg	1.28kW/kg

Some comments:
- Tesla achieved a higher specific power ratio in its PCS2, about 0.29W/kg more than the others.
- This comes with a unique system form factor: the PCS2 is twice as long as its competitors but definitely the thinnest. Unlike the others, it is integrated into the battery pack.
- A different electrical design (topology) and specific electronic components form part of this innovation.

YOLE SystemPlus

www.yolegroup.com | ©Yole SystemPlus 2024

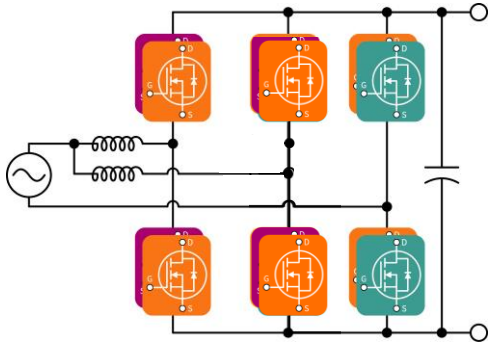
Copyright © Infineon Technologies AG 2025. All rights reserved.

Technology is the key for power conversion , WBG, especially SIC will dominate most of designs today

Si SiC GaN

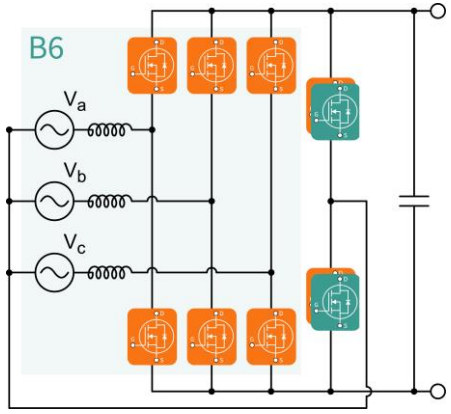
PFC

Totem-Pole for 1Φ (interleaved for 3Φ)



- Ease-of-use at high performance
- High modularity
- Efficiency up to 99%
- 1-phase for 3.6 kW and 7.2 kW
- 3-phase for 11 kW to 22 kW
- **IGBT, Si + SiC** offer cost down option for similar performance

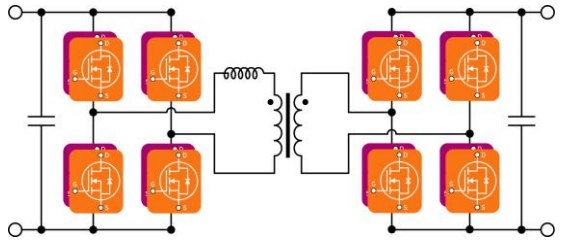
B6 / B8 (3Φ)



- Lower BOM due to low component count
- Easy control and widely known
- B6 for unidirectional power
- B8 for bidirectional power
- **IGBT + SiC** offer ~10% cost down

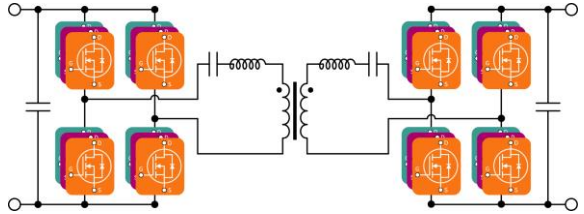
HV DC/DC

Dual Active Bridge (DAB)



- **Wide output voltage** supports different battery chemistry
- **Modular approach** matching Totem-Pole for multi-phase input
- GaN enables higher power density

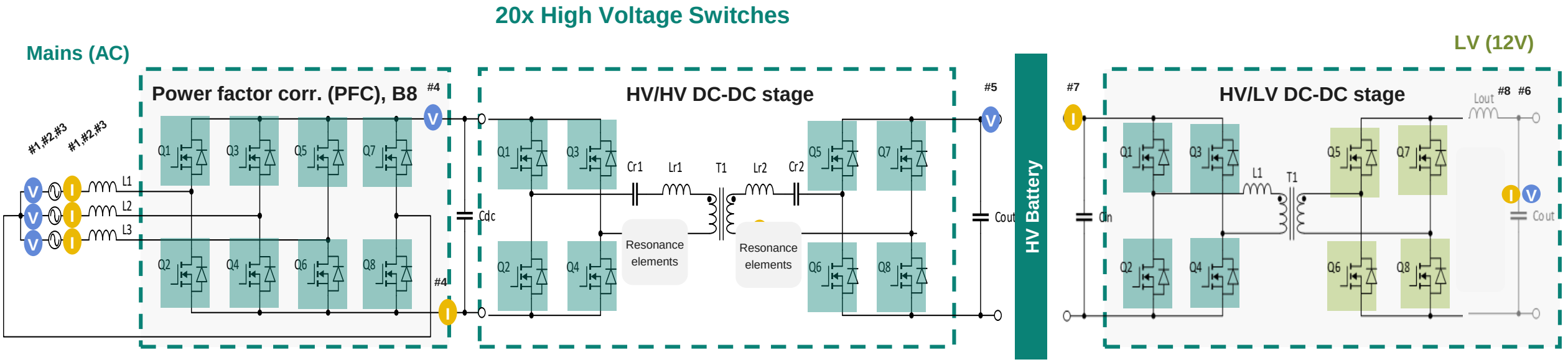
CLLC



- Peak efficiency > 96%
- High power density
- Compatible with all power technologies
- Bi-directional
- **Si MOS** offers best cost option

Copyright © Infineon Technologies AG 2025. All rights reserved.

State of the Art Topology/Systems



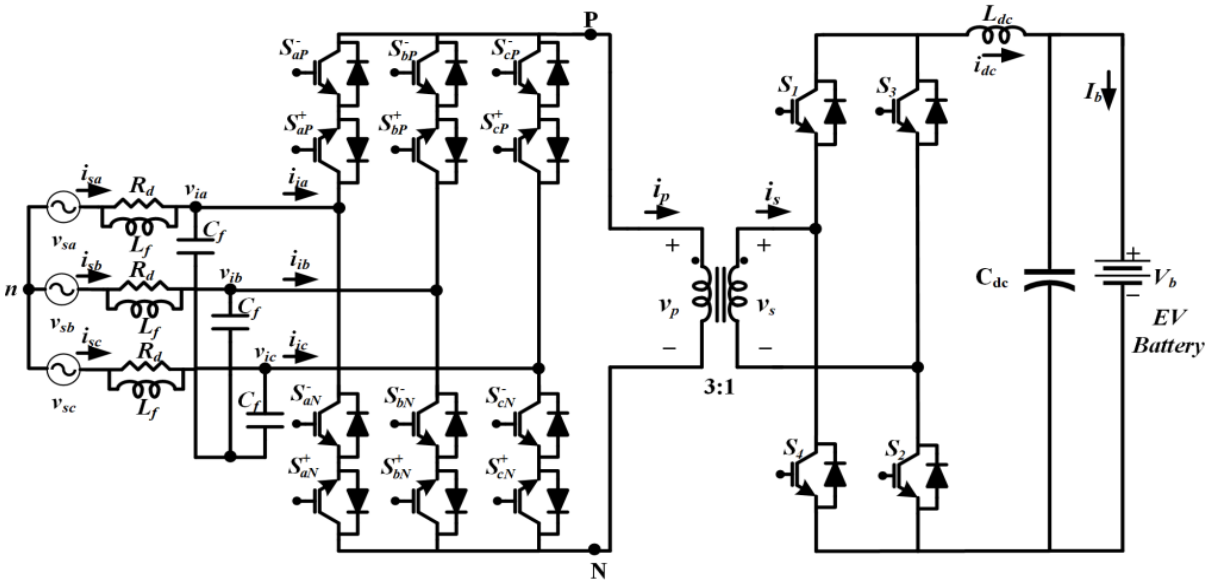


Copyright © Infineon Technologies AG 2025. All rights reserved.

New topologies, Modern Approach – Cycloconverters



3-phase Matrix Converter







Benefit:

- No bulky electrolytic capacitors needed
- Higher Power Density

Drawback:

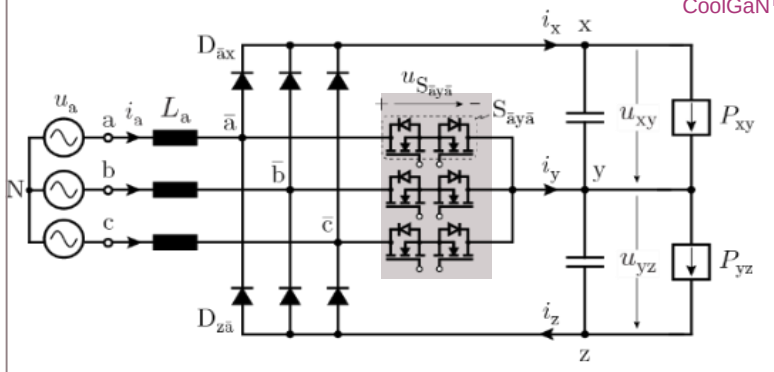
- More complex control

Copyright © Infineon Technologies AG 2025. All rights reserved.

Infineon offers comprehensive technologies addressing to various bi-directional topologies

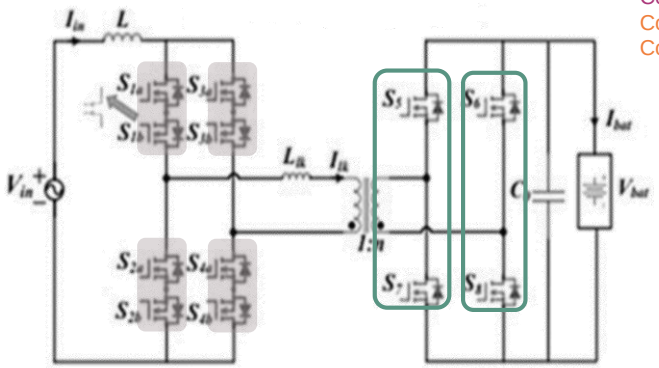
Vienna Rectifier

CoolSiC™ MOSFET 750 V BDS
CoolGaN™ MOSFET 650V BDS



1 phase Matrix Converter

CoolGaN™ MOSFET 650V BDS
CoolSiC™ MOSFET 750 V BDS
CoolSiC™ MOSFET 750 V HB

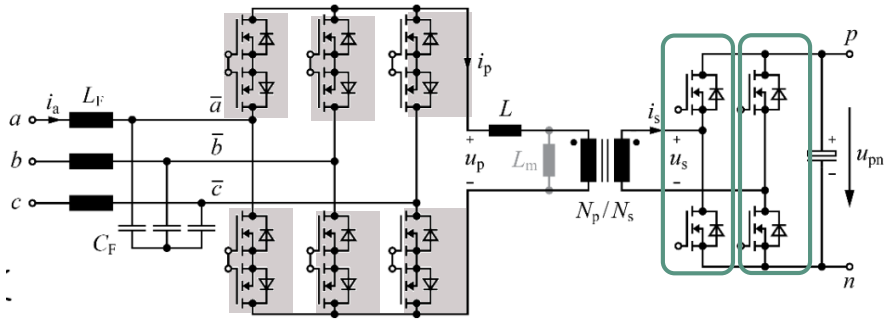


Bi-directional Switch
CoolSiC™ HexaDPAK
CoolGaN™ QDPAK

Half-bridge
CoolSiC™
HexaDPAK

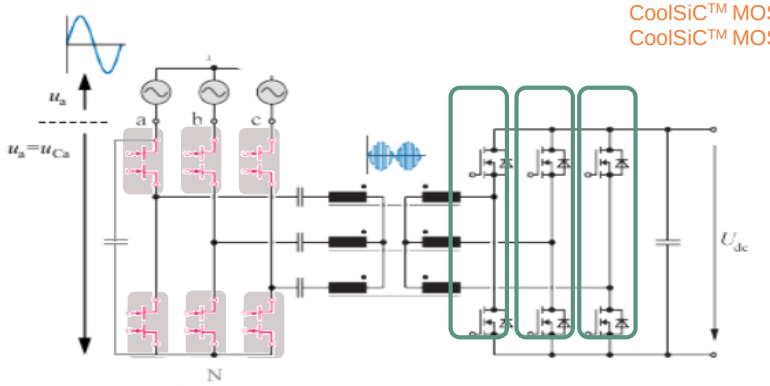
3-phase Matrix Converter

CoolSiC™ MOSFET 1200 V BDS
CoolSiC™ MOSFET 1200 V HB
CoolGaN™ MOSFET 850V BDS



3 phase isolated Y-converter

CoolGaN™ MOSFET 650V BDS
CoolSiC™ MOSFET 750 V BDS
CoolSiC™ MOSFET 750 V HB



Copyright © Infineon Technologies AG 2025. All rights reserved.

Table of contents

1 Role of Power Electronics in EV Car 3

2 Key Trends and Topologies 5

3 **Infineon Technology Improvements** **12**

4 Infineon Packaging Innovation 22

Copyright © Infineon Technologies AG 2025. All rights reserved.

Infineon enables electric drive train applications with system competence powered by CoolSiC™ MOSFETs

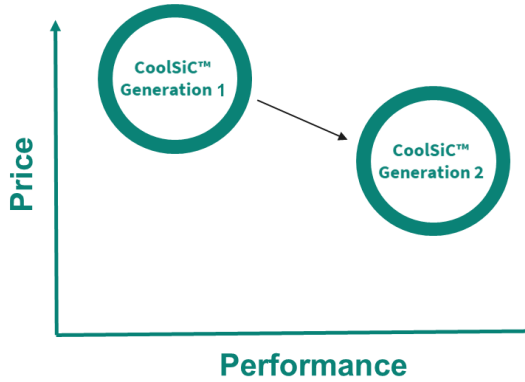
Power conversion trends

- **Increased power**
- **Higher power density**
- **Higher efficiency**
- **Bi-directionality – OBC**
  V2L, V2G, V2X

Power electronics

CoolSiC™ SiC

High performance



- **Excellent switching performance**
- **Optimal thermal conductivity**
- **.XT technology – die attach**
  Improved thermal performance

High reliability

- **Chip reliability**
  trench technology, Gate-oxide reliability
- **Package reliability**
  performance under mechanical &thermal stress
- **Infineon quality**
  More stringent approach beyond standards

Ease-of-use

- **Mature technology**
  Reduced design complexity

Copyright © Infineon Technologies AG 2025. All rights reserved.

CoolSiC™ Automotive MOSFET 750 V G2 vs G1

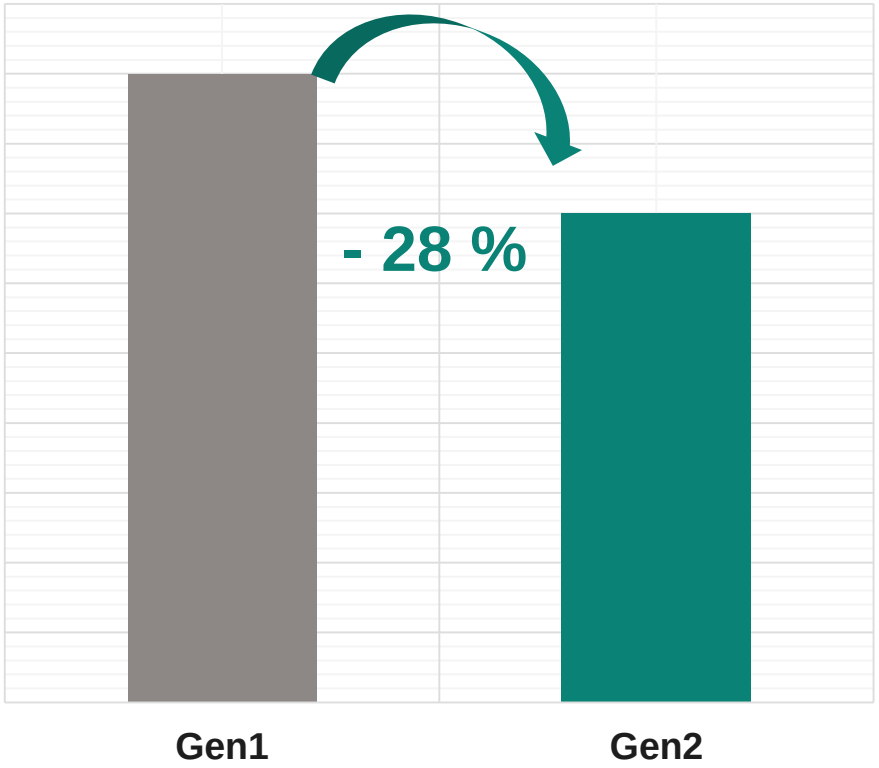
Cost vs performance optimization

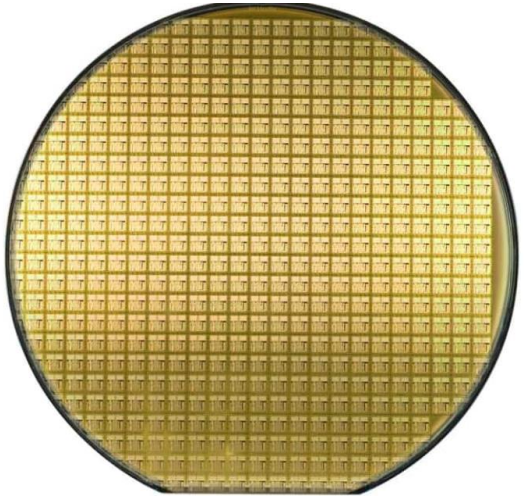
How ?



basic Idea

A_{Act} x $R_{on,typ}$





G1 = *x* devices/wafer
(e.g. 1000chips)

G1 = 1.28 *x* devices/wafer
(e.g. 1280 chips)

Pros.

- Lower parasitic capacitors (C_{oss} , C_{iss} , C_{rss})
- Lower gate charge
- Faster switching
- Lower Qrr
- Lower switching loss

Cons

- Lower Avalanche capabilities
- Higher R_{TH} *

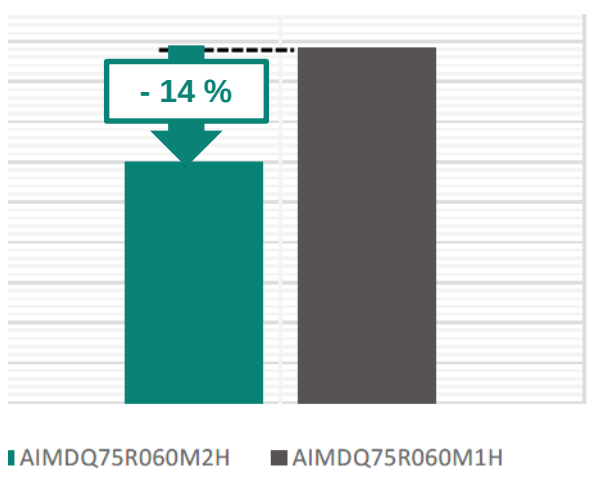
* Optimization on Max/typ margins from 750V SiC G1 to G2 , the R_{TH} max values in 750 G2 are close or almost same as G1

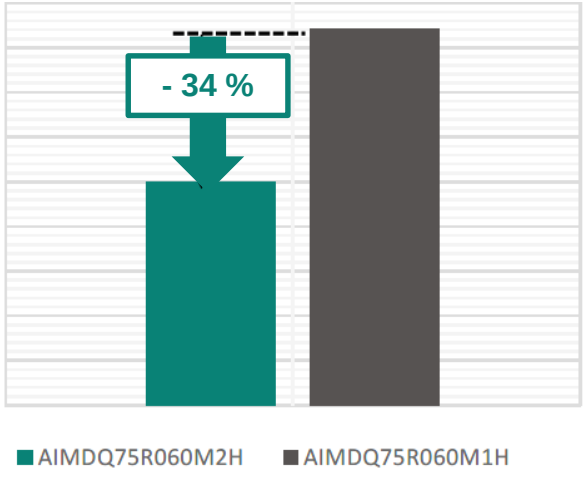
Copyright © Infineon Technologies AG 2025. All rights reserved.

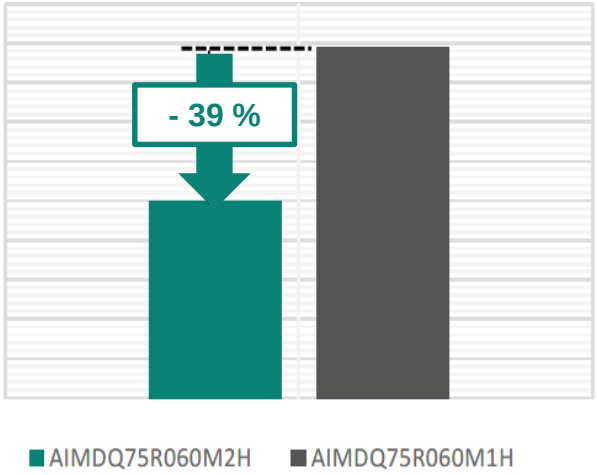
Unveiling a new performance with CoolSiC™ G2
FoM at 125°C

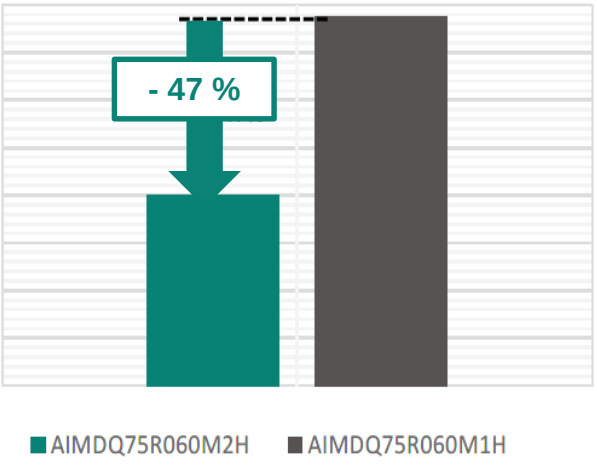
Figures-of-merit (FOM) comparison: lower is better for energy efficiency optimization

The classical MOSFET FOM (from low-voltage silicon world)			
$R_{DSON,typ}$ x Q_G (mΩ*nC) at 125°C	$R_{DSON,typ}$ x Q_{OSS} (mΩ*nC) at 125°C	$R_{DSON,typ}$ x E_{OSS}(mΩ*µJ) at 125°C	$R_{DSON,typ}$ x Q_{fr} (mΩ*nC) at 125°C
Lower means lower gate driving power loss	Lower is better in soft-switching topologies	Lower is better for light-load efficiency	lower is better for hard-switching half-bridge top.









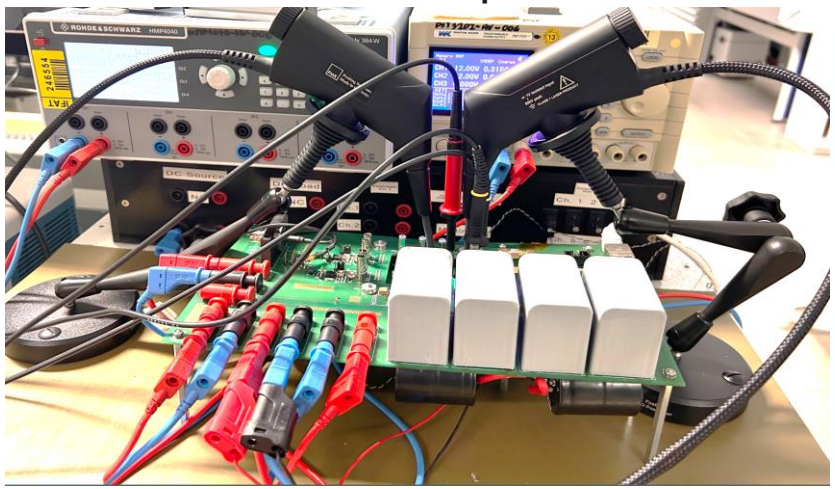
Infineon products: AIMDQ75R060M1H, AIMDQ75R060M2H
Q_G = total charge at given conditions, Q_{oss}= total charge associated to C_{OSS} at given conditions. E_{OSS} = total energy associated to C_{OSS} at given conditions
Source: Application Note- AN125027 CoolSiC™ 750 V G2 automotive MOSFET

Copyright © Infineon Technologies AG 2025. All rights reserved.

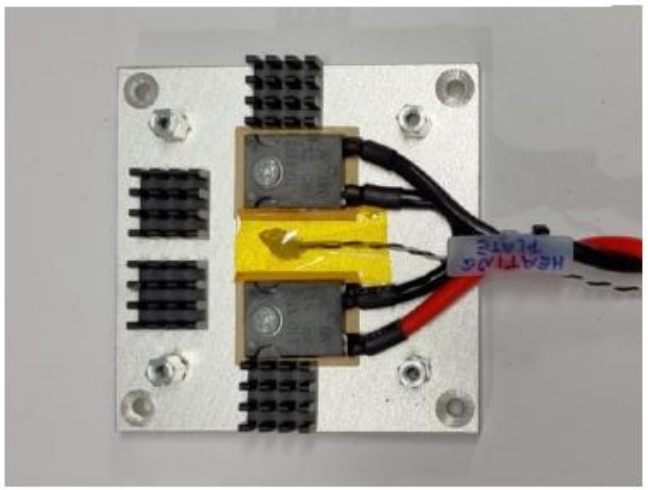
Experimental Verifications

Half bridge board for double pulse test

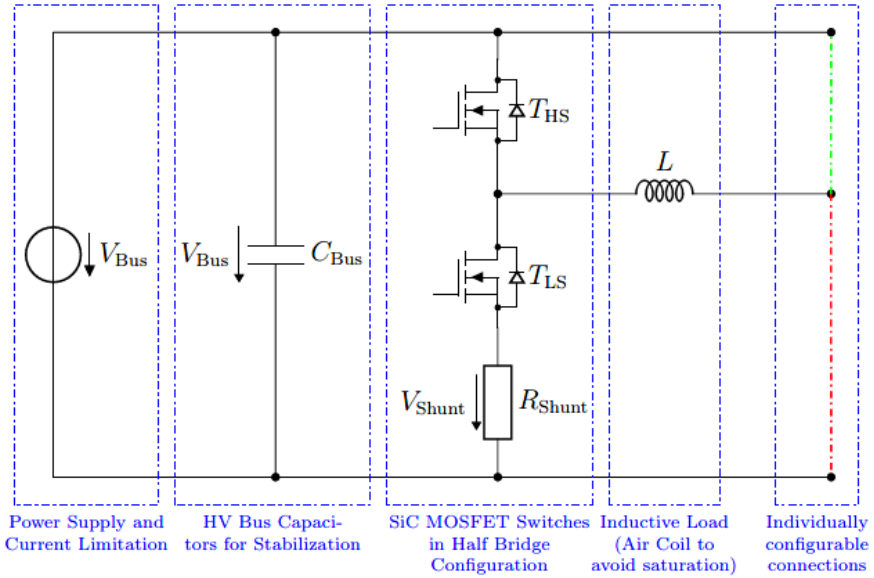
Test Setup



Heating Plate with 1 Ω 100 W Power resistors



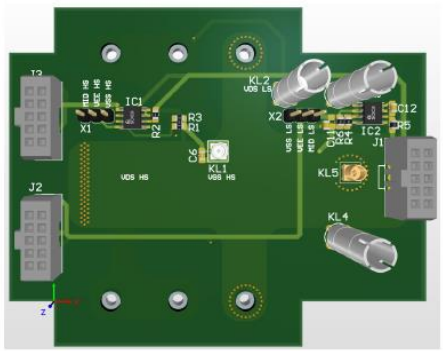
Concept Schematic -Double Pulse Test



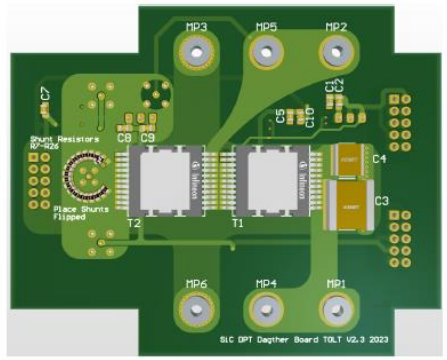
Equipment's Used :

- Programmable DC power Source chroma 62024P-600-8.
- Tektronix oscilloscope MSO56B, Probe PMK PHV 1000 & 3 Passive Probes
- Rhode & Schwarz HMP4040 for Power Resistors (Heating Plate).
- PID controller for heating the Resistors (100 W)

Daughter boards



(a) Top view



(b) Bottom view

Test Conditions

- V_{DD} = 400 V (Will be updated to 500 V)
- I_D = 5 A to 30 A
- R_g On/Off (Ext) = 2.7 Ω
- Shunts = 4.0 Ω (20 No's)
- V_{gs} = 18 V/-5 V

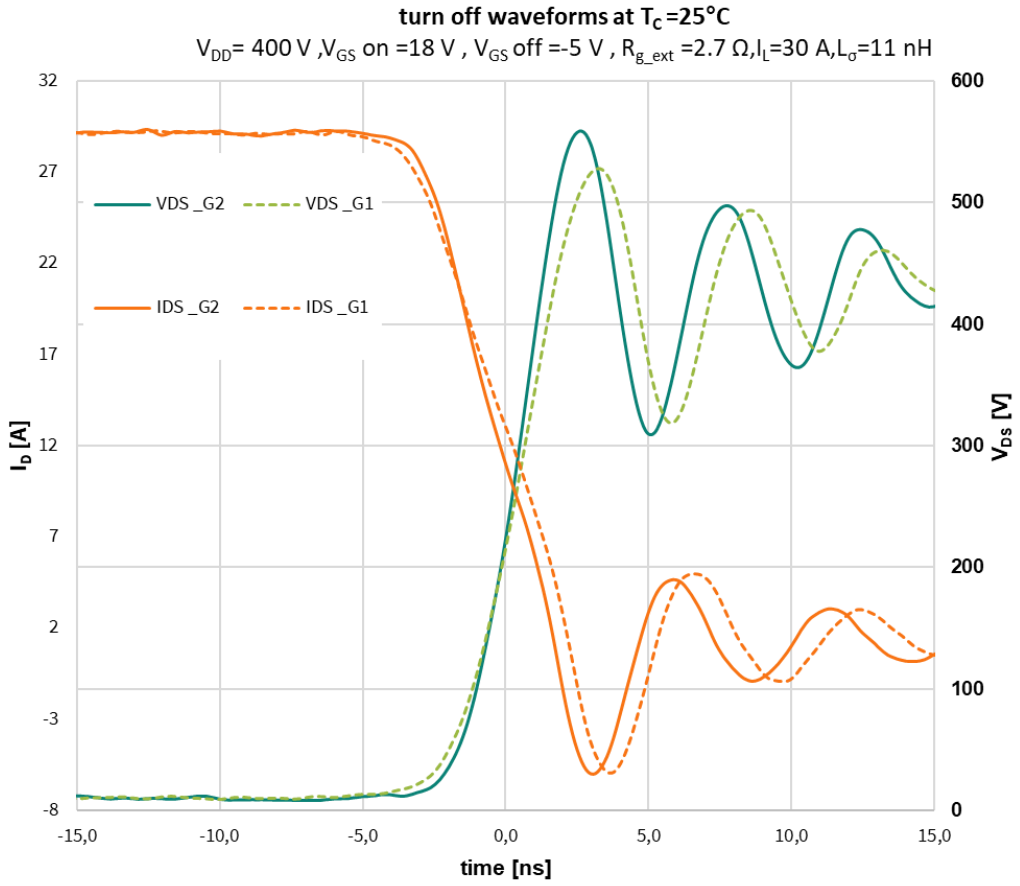
Parameters to be measured

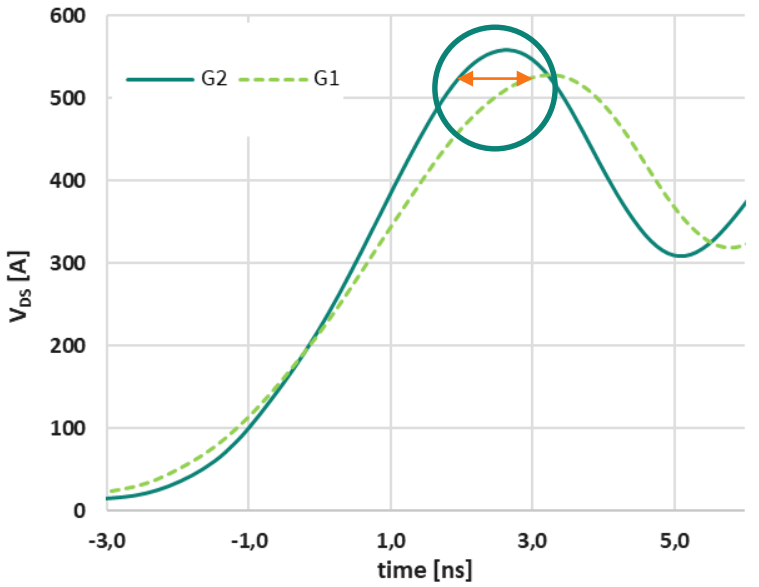
- E_{on} and E_{off}
  - 25°C
  - 150°C
- Q_{rr} at Typical I_D
  - 25°C
  - 150°C

Copyright © Infineon Technologies AG 2025. All rights reserved.

Switching Behavior –**Turn-off**

G2 is 25% faster then G1





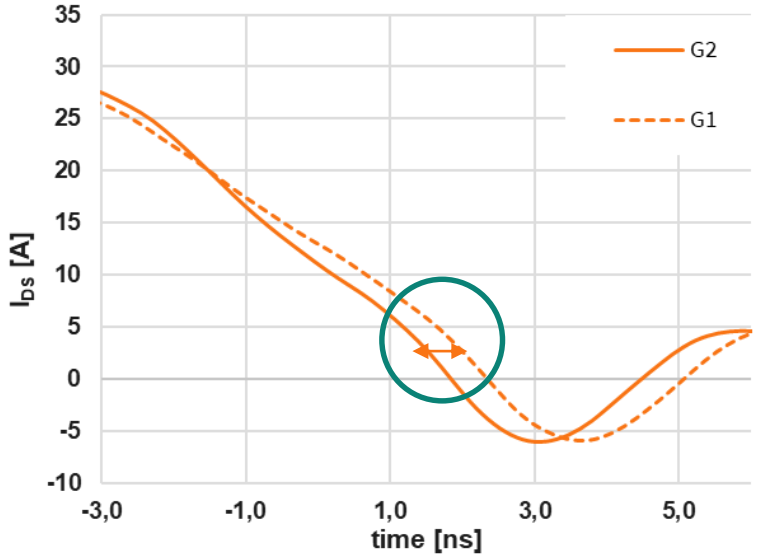
Gen 2

Gen 1

Voltage (V_{DS}) switching speed during turn OFF

$$\frac{dv}{dt} = 130V/ns$$

$$\frac{dv}{dt} = 103V/ns$$



Gen 2

Gen 1

Current (I_{DS}) switching speed during turn OFF

$$\frac{dI}{dt} = 5.6A/ns$$

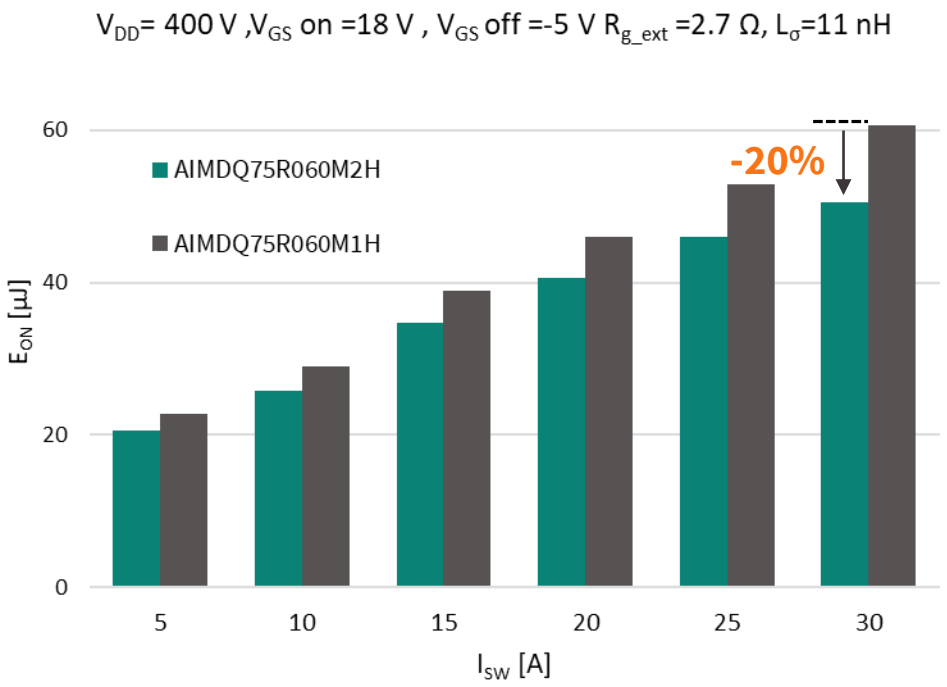
$$\frac{dI}{dt} = 4.5A/ns$$

Source: Application Note- AN125027 CoolSiC™ 750 V G2 automotive MOSFET

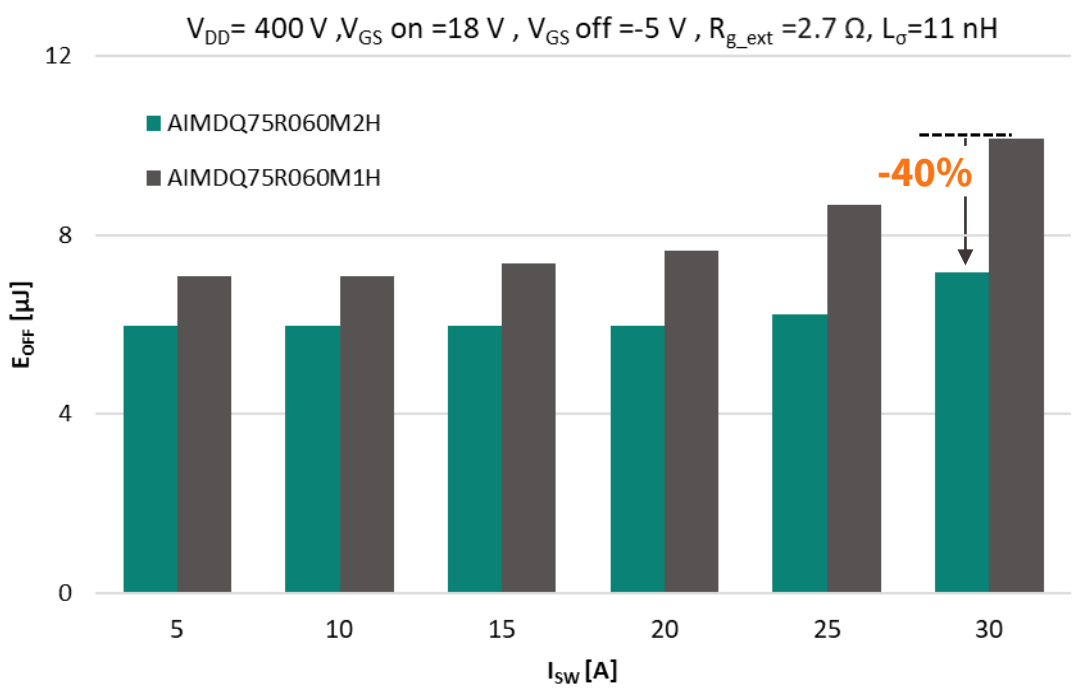
Copyright © Infineon Technologies AG 2025. All rights reserved.

Switching energies G1 vs G2

Turn-on losses



Turn-off losses



CoolSiC™ MOSFET 750 V G2 **device switches faster by 25%, lower turn on/OFF losses by 20-40% than G1**

Note: turn off energy includes the E_{OSS}, turn on energy does not include the E_{OSS}

Source: Application Note- AN125027 CoolSiC™ 750 V G2 automotive MOSFET

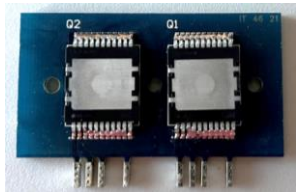
Copyright © Infineon Technologies AG 2025. All rights reserved.

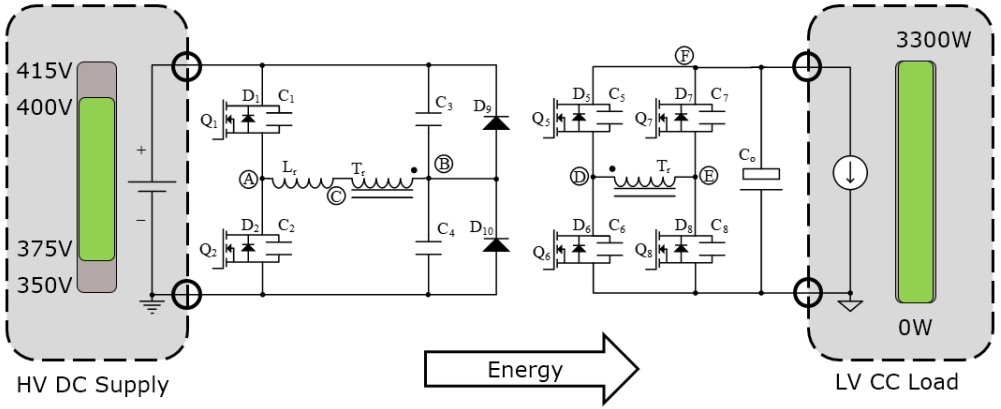
3.3 kW LLC Converter

3.3 kW LLC Converter Board



Daughter Board





Board Description

- DC/DC converter
  - 400 V nominal input voltage (350 V-415 V)
  - 8.25 A nominal input current
- 43.5 V – 59.5 V output voltage
  - 51.5 V nominal output voltage
  - 65 A nominal output current
- up to 3300 W output power
- Efficiency tested with dotnet Efficiency
- Frequency range 75 kHz – 107 kHz
- Unipolar driving 0 V/18 V

DUTs:

- G1 AIMDQ75R060M1H
- G2 AIMDQ75R060M2H*

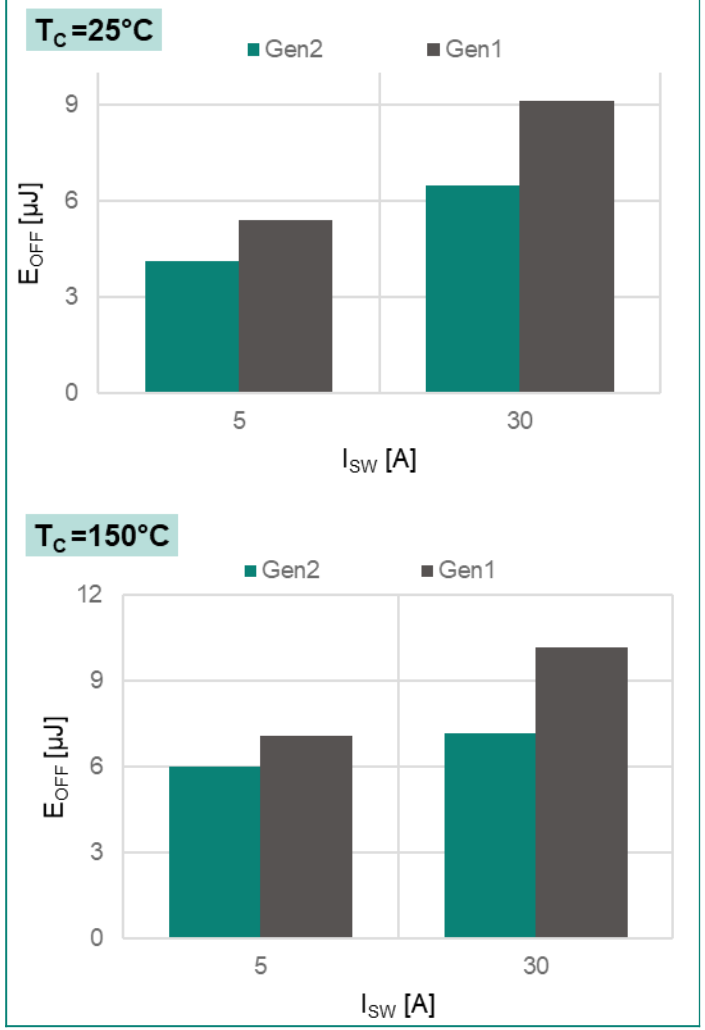
**EES used for this test are not based on final process.*

- A detailed description of this board is available in this Application Note.
- The turn ratio of the pulse transformer TR-2 has been modified (13:16:16 ➔ 13:20:20) to generate the 18 V driving voltage.

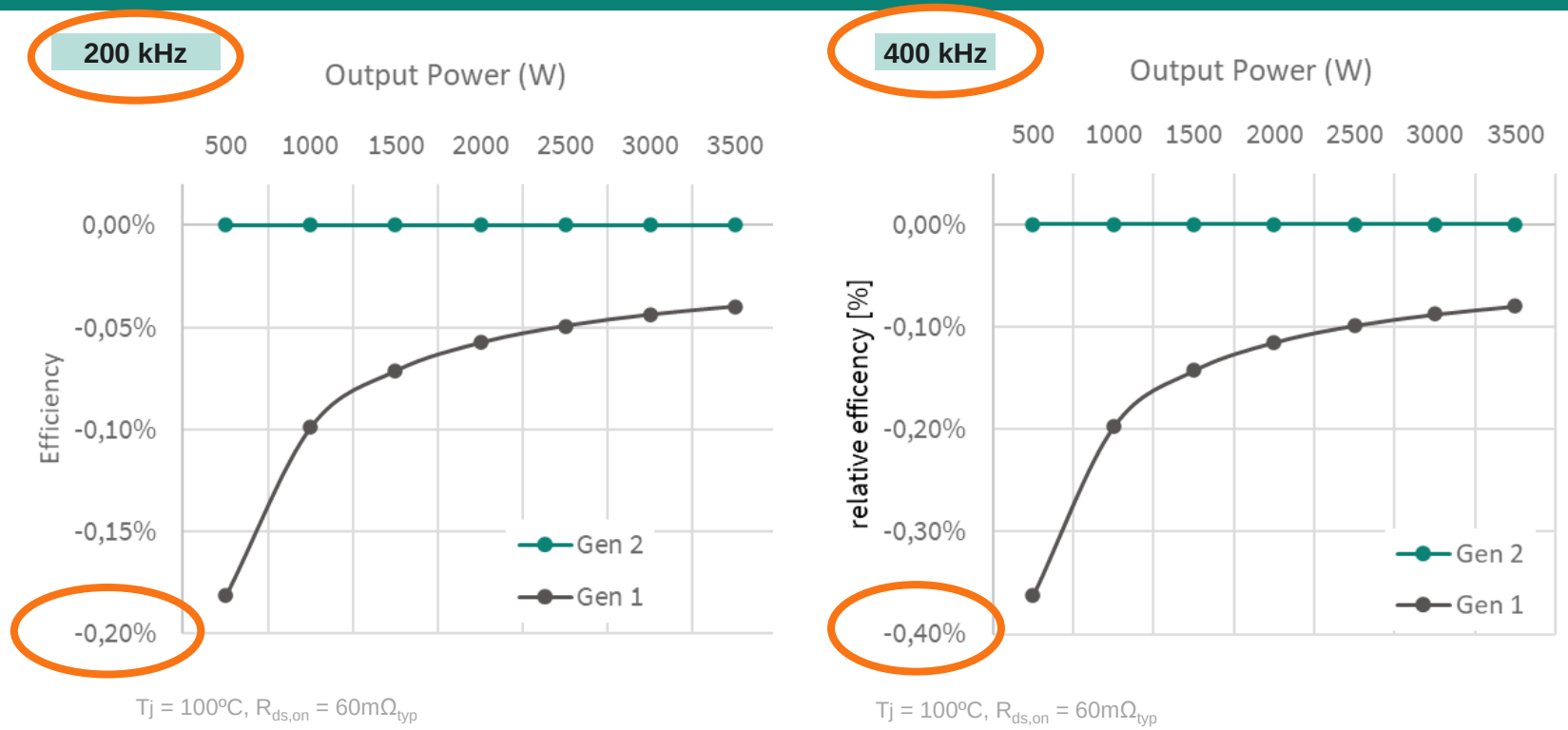
Copyright © Infineon Technologies AG 2025. All rights reserved.

Soft-switching LLC (impact of turn off losses)

Turn-off losses (soft sw.)



Application results



Infineon CoolSiC™ G2 demonstrates a **substantial improvement in soft-switching topologies**, addressing the lower efficiency than G1

Source: Application Note- AN125027 CoolSiC™ 750 V G2 automotive MOSFET

Copyright © Infineon Technologies AG 2025. All rights reserved.

Table of contents

1 Role of Power Electronics in EV Car 3

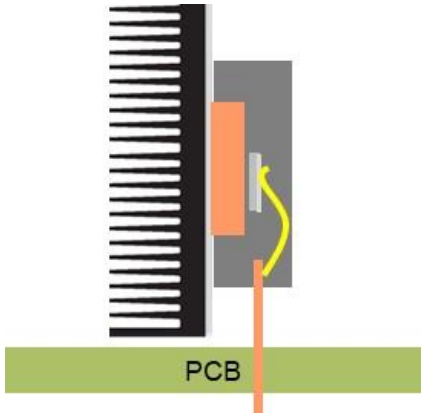
2 Key Trends and Topologies 5

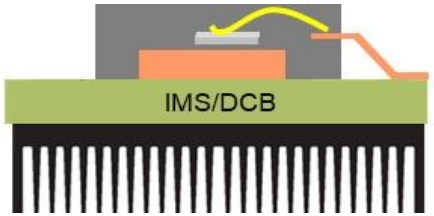
3 Infineon Technology Improvements 12

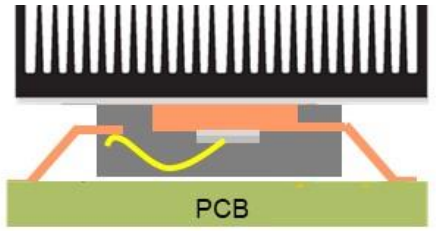
4 **Infineon Packaging Innovation** **22**

Copyright © Infineon Technologies AG 2025. All rights reserved.

Package evolution which enables high volume assembly and PCB design improvement at expensive assembly location





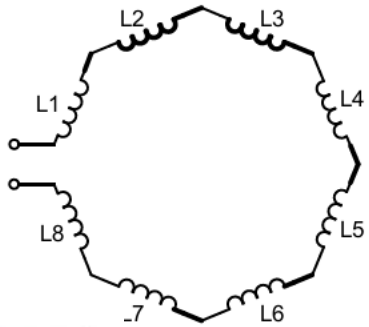


THD – Through Hole Device	SMD Bottom-side cooling	SMD top-side cooling
– Robust thermal performance – **Manual handling** – **Low pin count,** improved with 4-pin variant	– **Medium** thermal performance – Fully automatic handling – High pin count	– **Optimal** thermal performance – **Fully automatic** handling – **High** pin count

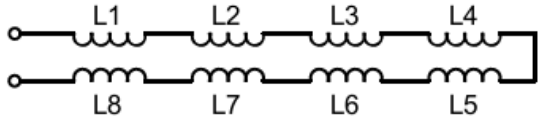
Copyright © Infineon Technologies AG 2025. All rights reserved.

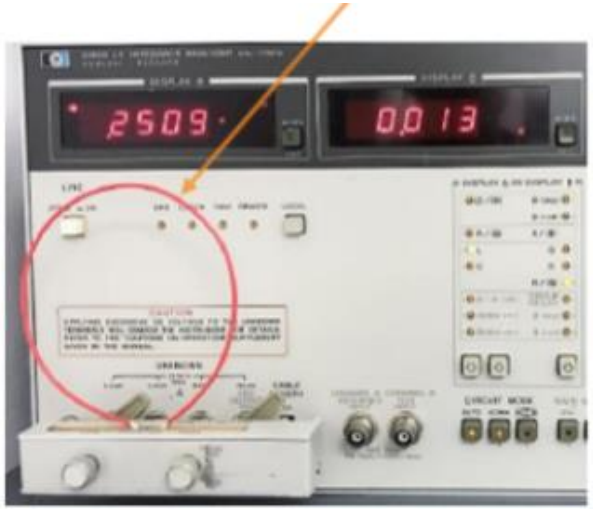
The Relationship between loop geometry and inductance

$$L_{Loop} \approx \sum_{n=1}^{n=8} L_n$$



$$L_{Loop} \approx \left(\sum_{n=1}^{n=8} L_n\right) - M_{L1-L8} - M_{L2-L7} - M_{L3-L6} - M_{L4-L5}$$





250nH

75nH



The same wire formed into stripe has a 3.5x reduction

Loop of a wire with 100mm diameter

Same wire lenght!

Loop formed into 150mm side-by-side stripline

Very little mutual inductance between these elements in the large loop, so the total inductance is essentially the sum of individual elements

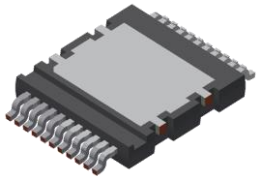
The stripline has small area but **high mutual inductance substracts** from sum of individual elements (negative sign because the direction of current is opposite)

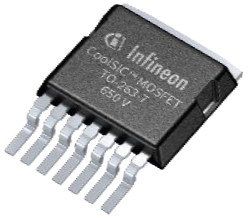
Both Measurement at 1MHz

Source: Eric Persson, APEC 2022 Professional Education Seminar

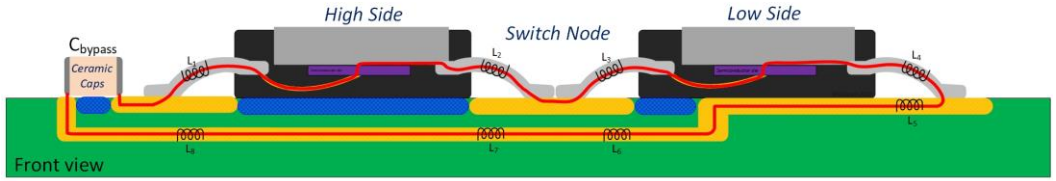
Copyright © Infineon Technologies AG 2025. All rights reserved.

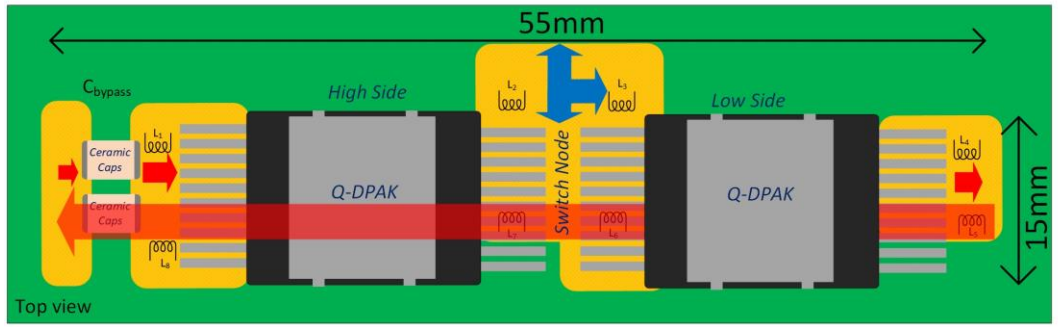
Power Loop Design



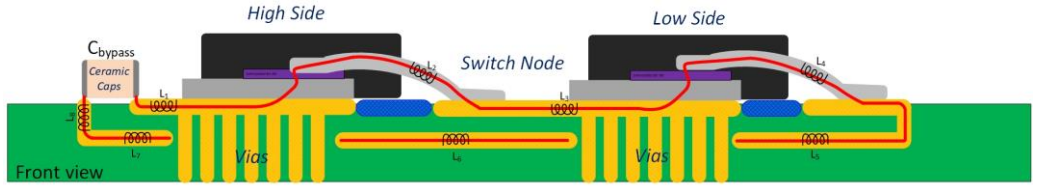


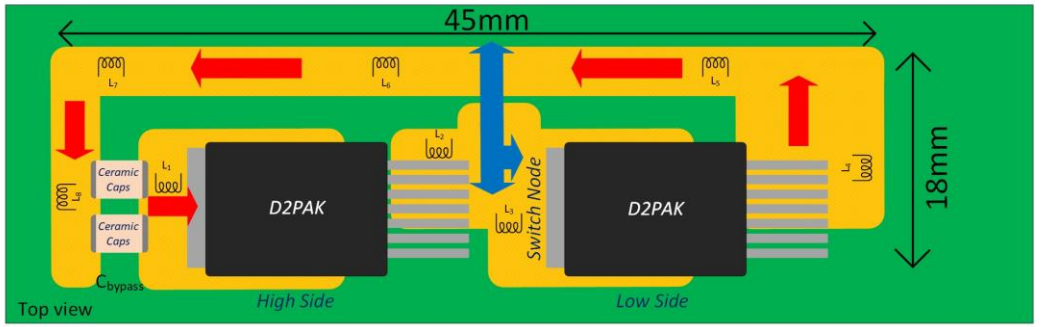
Top-side cooling device Q-DPAK

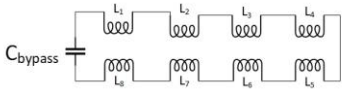




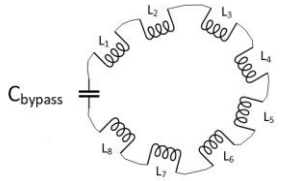
Bottom-side cooling device D2PAK







$$L_{Loop} = (\sum_{i=0}^{n} L_i) - M_{L_1-L_8} - M_{L_2-L_7} - M_{L_3-L_6} - M_{L_4-L_5}$$



$$L_{Loop} = \left(\sum_{i=0}^{n} L_i\right)$$

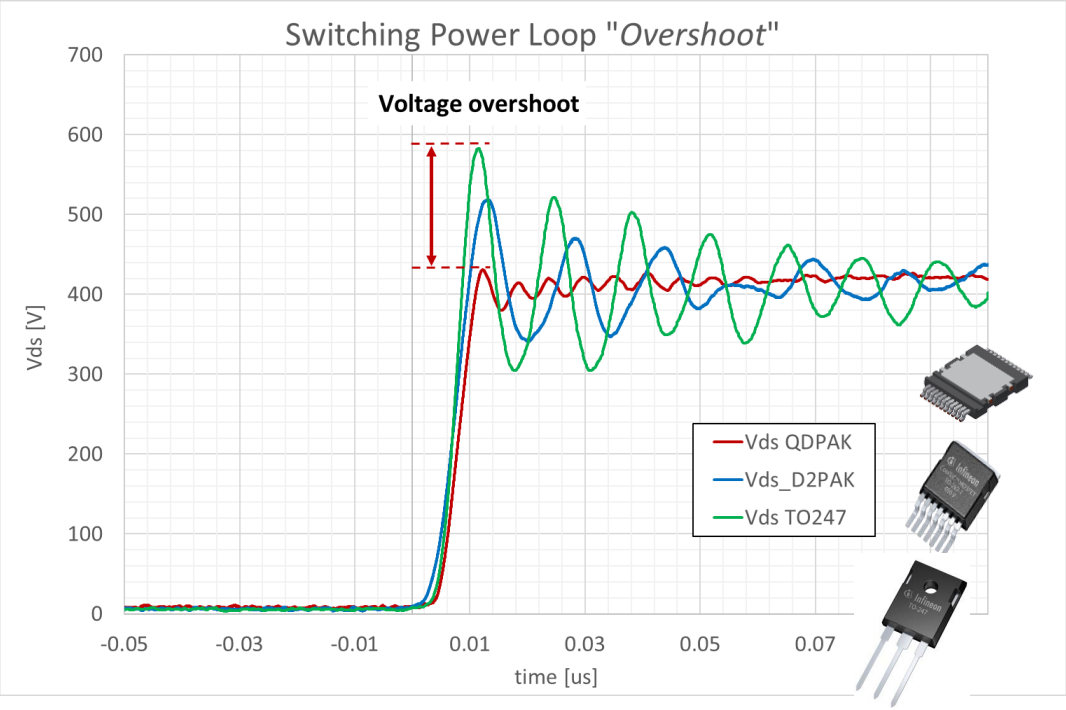
Power Loop Parasitic Inductance

Sum of parasitic inductances (power devices, bond wires and package) & conductive tracks, components

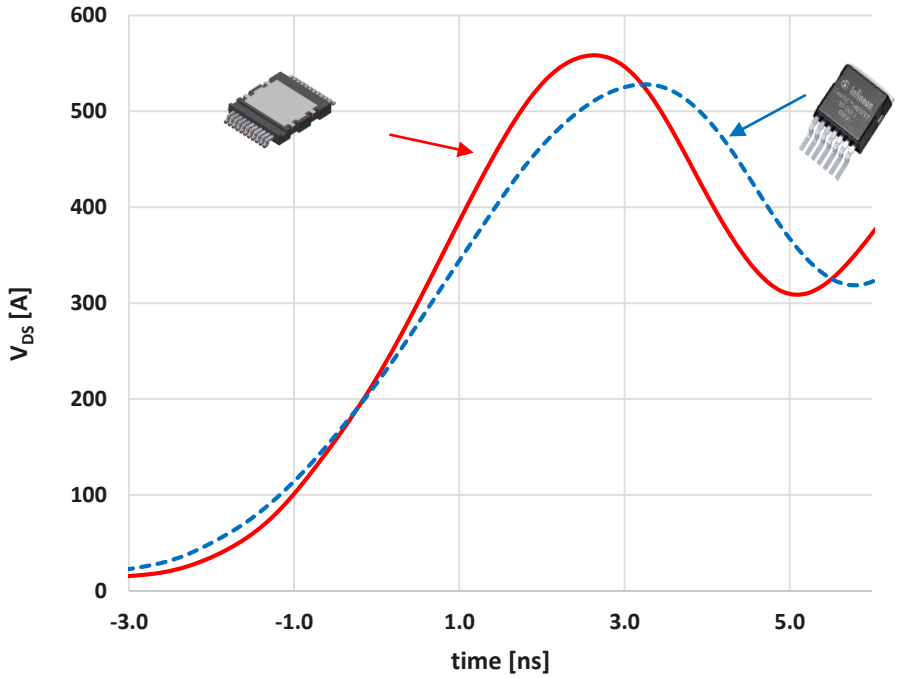
Use from mutual inductance for reduce the total commutation inductance loop (return path)

Copyright © Infineon Technologies AG 2025. All rights reserved.

Impact of parasitic power loop inductance for Power Semiconductors



48mΩ$_{typ}$ SiC MOSFET, 23A turn-off current, Rg,off = 1Ω



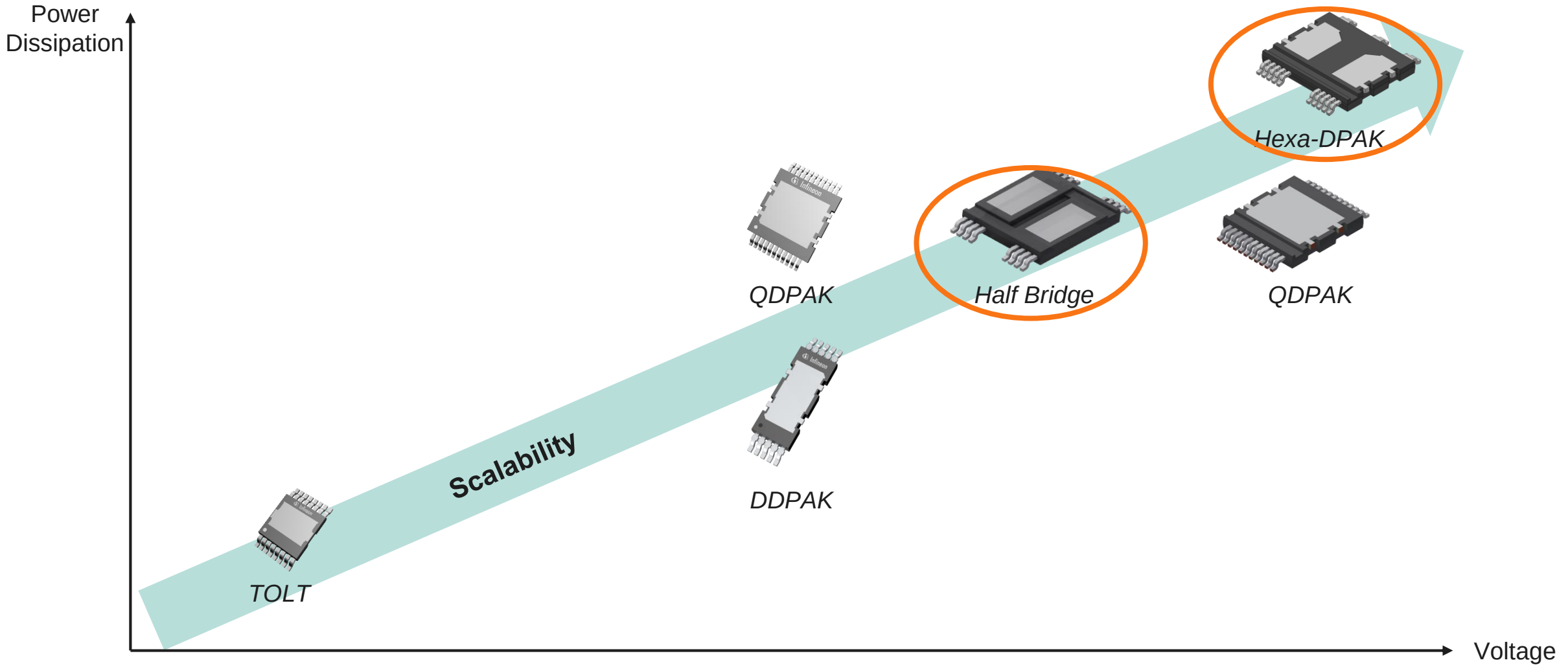
48mΩ$_{typ}$ SiC MOSFET, 23A turn-off current

Impact of parasitic power loop inductance for a turn off by power package
Different power packages with design has include thermal interface

Slow down the switching speed (dv/dt) by increasing the **gate resistor**
Cost of **increasing the switching losses, lower system efficiency**

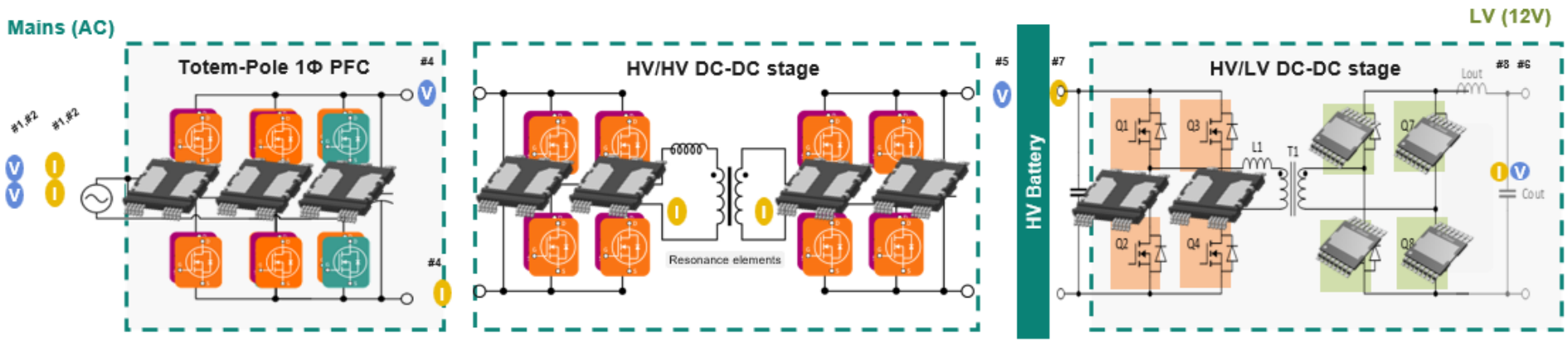
Copyright © Infineon Technologies AG 2025. All rights reserved.

The QDPAK package is part of a scalable, future proof package concept to address various applications and customer needs

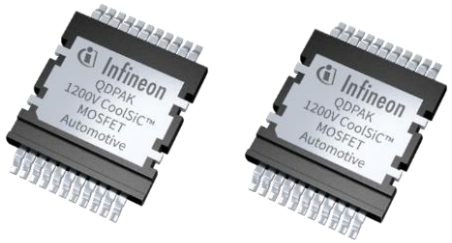


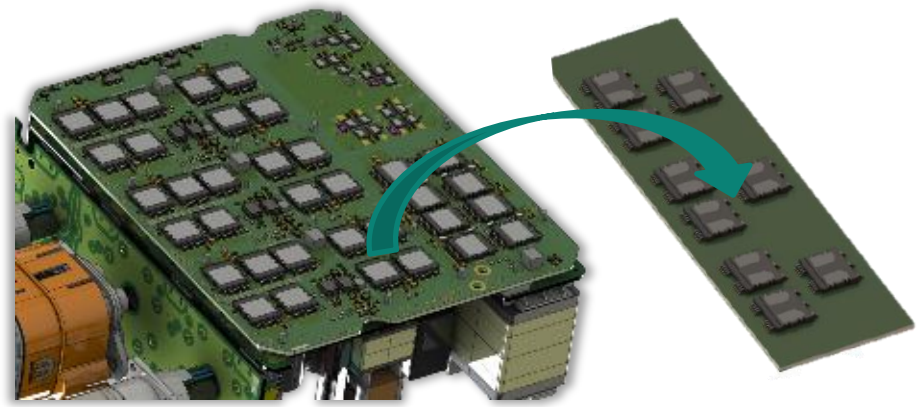
Copyright © Infineon Technologies AG 2025. All rights reserved.

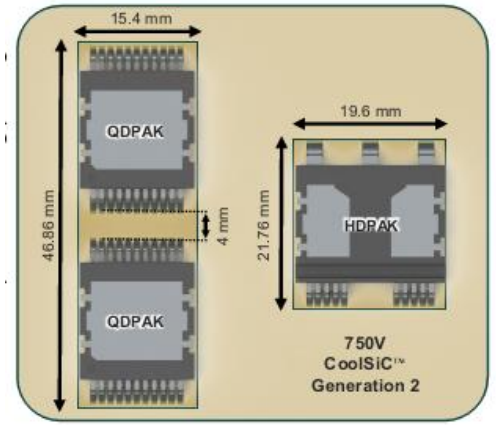
CoolSiC™ H-DPAK HB next step of integration

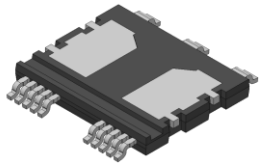


18x HV Devices









9x Devices

High Power Density

- Highly compact package
- smaller footprint

+

Low System Cost

- Smaller PCB area
- Reduced assembly effort
- Reduced TIM cost

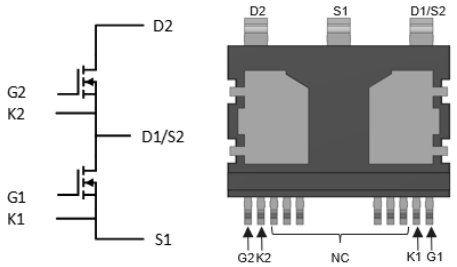
=

- High power density
- Lower system cost

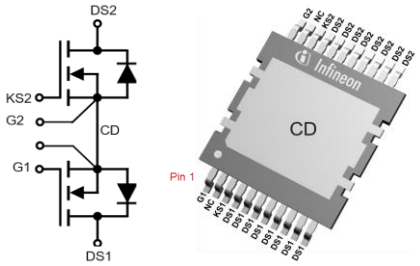
Copyright © Infineon Technologies AG 2025. All rights reserved.

More integrations

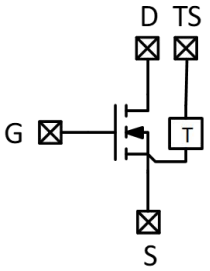
Half-Bridge

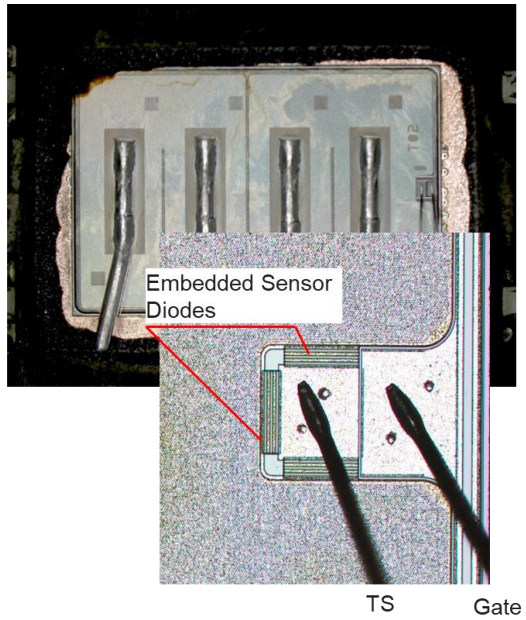


Bi directional - Matrix

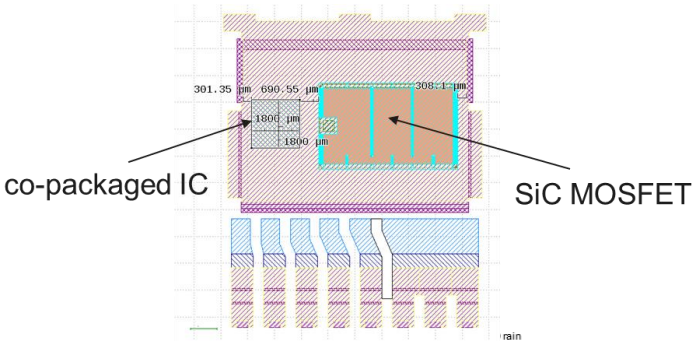


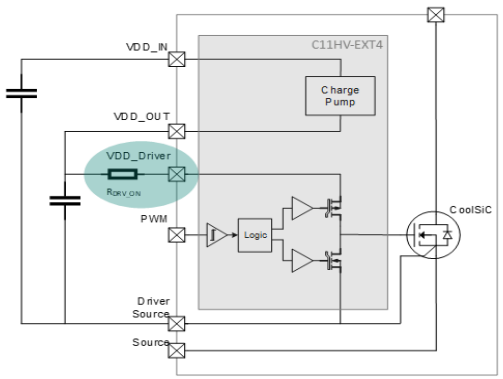
Current Sensor by embedded Diode



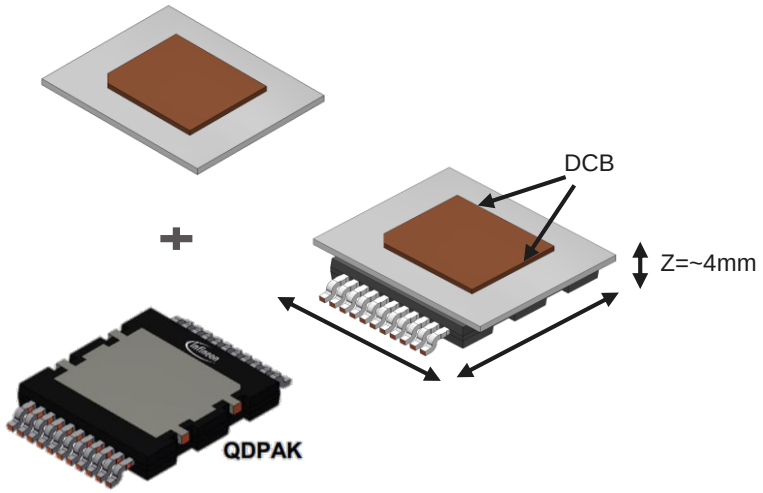


IC/Gate Driver Integration

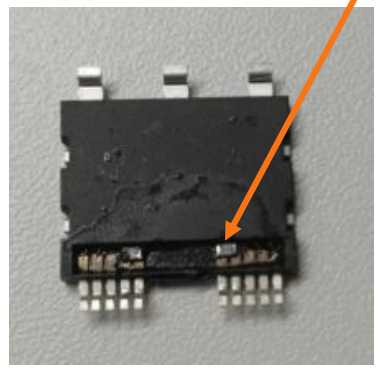




Isolated package



Current Sensor by shunt resistor



Copyright © Infineon Technologies AG 2025. All rights reserved.

Latest available Appnote and Article related to SiC Gen2

restricted
AN125027

CoolSiC™ 750 V G2 automotive MOSFET

The latest generation of Silicon Carbide (SiC) MOSFET

About this document

Scope and purpose

This application note introduces the new generation trench based CoolSiC™ 750 V G2 MOSFET and describes the differences between the earlier generation of CoolSiC™ 750 V MOSFETs and the latest CoolSiC™ 750 V G2 Silicon Carbide (SiC) MOSFET from Infineon. This application note includes technology parameters, figure of merits, target applications, and topologies and describes the latest and most important additional benefits fc designers.

The purpose of this document is to explain the features of this new family of products. Important application topics are covered to help in designing systems with maximum performance and reliability

Intended audience

This application note is intended for design engineers, technicians, and developers of electronic systems.

pc

Comprehensive electric and thermal evaluation of SiC high-power discrete packages for next generation power supplies

Josef Wildauer[1], Jon Azurza Anderson[1]

[1] Infineon Technologies Austria AG, Villach, Austria

Corresponding author: Josef Wildauer, josef.wildauer@infineon.com

Abstract

In modern power supplies, the use of SiC MOSFETs offers numerous advantages, including faster switching speeds and higher operating temperatures. However, to extract the largest benefit from discrete SiC MOSFETs, power electronics designers require a new understanding of the operating characteristics and their impact on power converter design. This article performs a quantitative and comprehensive electric and thermal evaluation of some of the most popular SiC MOSFET discrete packages, yielding that top-side-cooled devices offer a three-times lower parasitic loop inductance compared to through-hole and bottom-side-cooled devices, while offering an excellent thermal performance.

1 Introduction

To maximize system efficiency and leverage the full potential of SiC MOSFETs, proper electrical and thermal layout design is essential. Close attention has to be payed to system parasitics, and how these are influenced by the cooling. This is of particular importance when high switching speeds (dv/dt) are targeted. Most importantly, the impact from the stray inductances in the power and gate loop have to be minimized, to ensure optimal switching performance, while still complying with the mechanical constraints of the cooling system. While SiC MOSFETs offer notably high switching frequency (typically above 200 kHz), poor layout design can lead to voltage overshoots and associated problems, which might lead to the designer needing to artificially slow down the devices, thus increasing the losses (and the requirements of the cooling).
Top-side cooled (TSC) power packages offer an ideal solution from the system perspective, allowing to decouple the electric path (at the bottom) from the thermal path (through the top). Significant benefit can be therefore obtained by layout optimization and by closing the commutation loop below the devices, due to reduced mutual inductance. Additionally, the cooling system is located on the top side, making it possible to directly mount water cooling or a heatsink on the devices, which can improve heat dissipation [1].
On the other hand, bottom-side cooled power packages have always presented a challenge in finding a balance between thermal vias (or similar concepts, such as copper inlays) and the power loop design. This often requires additional PCB space to achieve the desired thermal performance, and the power loop suffers, as the loop cannot be closed below the device where the vias are placed, but closes around the devices. This last effect leads to more PCB area required, and a worse commutation loop, which can be a limitation.

2 Parasitic Loop Inductances

In this section, the power (or commutation) and gate loop inductances are analyzed in depth. For this purpose, a typical half bridge configuration (operated in double pulse mode) is used to analyze the power loop and gate inductances (**Fig. 1**).

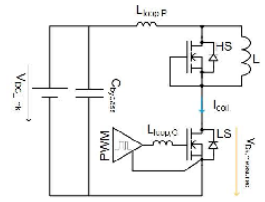


Fig. 1 Double pulse Setup for parasitic analysis.

The first part of the analysis focuses on the power inductance loop ($L_{loop,P}$). This loop comprises the

pcim

High Power Density Two-Level Switching Cells based on SiC MOSFET in Q-DPAK Top Side Cooled Package

Manuel Gomez[1], Jon Azurza Anderson[1]
[1] Infineon Technologies Austria AG, Austria

Corresponding author: Manuel Gomez, manuel.gomez@infienon.com

Abstract

High power density converters are an undeniable trend in power converters in the low-to-mid kW range. Top Side Cooled (TSC) Surface Mounted Devices (SMD) offer several advantages, like pick-and-place assembly and excellent electrical and thermal performance. Standard layout practices for TSC-SMD devices exist, however, for achieving the next level of power density, some topology-specific optimizations are possible. This article presents four high power-dense switching cells based on SiC MOSFETs housed in a Q-DPAK TSC package that have been optimized on the bases of clearance and creepage requirements, topology type (i.e. hard-switching or soft-switching), scalability, and the size of the magnetic components that will be used in conjunction with the switching cell (SW-Cell). Using a double pulse test (DPT), the SW-Cells' external gate resistors values have been optimized, and the power loop inductance were extracted and compared with values extracted from a multiphysics parasitic extraction. We show that a power loop inductance of down to 7nH is possible in a half-bridge with TSC devices in the size of Q-DPAK. With these results, design guidelines are given to choose the optimal power loop.

1 Introduction

The introduction of wide-bandgap (WBG) devices in SMD packages offer many advantages, like pick-and-place assembly, and the possibility to simultaneously have excellent electric and thermal performance by separating the electric and thermal paths. However, special attention must be paid to the minimization of the parasitic capacitances, gate loop inductances and power loop inductances of half-bridge SW-Cells in order to achieve power-dense designs [1]. So far, however, design constraints and requirements at system- and package-level, e.g., creepage and clearance, and the gate driving circuit contribution to the overall PCB area utilization of the SW-Cell, have not been accounted for the optimization of the SW-Cell [2],[3]. For example, the tie-bars that are required for the Q-DPAK fabrication, shown in **Fig. 1(a)**, are electrically connected to the drain, hence a polygon cut-out region must be defined in the outer layer of the PCB where the components are located and a minimum distance between devices should be respected (see **Fig 1(b)**) to avoid a clearance and creepage violation. The aforementioned cut out region shown in **Fig. 1(b)**, can be broken down in two regions, where the blue region is defined by the creepage limitation and the red region is defined by the clearance limitation.

Taking into consideration the clearance and creepage requirements at system level highlighted in **Fig. 1(b)**, the scalability of the switching cells, the driving scheme, and the size of the magnetic components that will be used in conjunction with the SW-Cell, four different switching cells have been proposed (see **Fig. 2**).

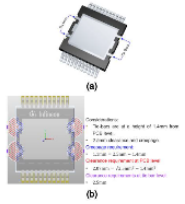


Fig. 1: Q-DPAK package **(a)** tie bars and **(b)** keep out region. The considered clearance and creepage requirements is 2.5mm, which is a typical value for voltage up to 430V, which has to be considered due to the tie bars.

Performance optimization of power MOSFETs in SMT top-side-cooling packages by system design

Severin Kampl
Infineon Technologies Austria AG
Villach, Austria
https://orcid.org/0009-0008-9386-6861

***Abstract*— This work presents easily applicable practices for optimizing the performance of power converters using discrete, top-side-cooled power packages. It demonstrates how parasitic elements in the power path can be minimized, using a full-bridge topology with novel Silicon-Carbide wide bandgap power semiconductors as an example. Furthermore, this paper explores two different methods for estimating power-loop inductances: one measurement based, and one simulation-based method. With the mismatch between the results being less than 10 percent, a total power-loop inductance of 7 nH (on average) could be achieved with the Silicon-Carbide second generation (G2) Power MOSFETs in Q-DPAK packages. Finally, suggestions for further optimization of the test board are offered. The recommendations and best practices outlined in this paper provide valuable insights for designers and developers of power conversion systems, facilitating faster design-in cycles for top-side-cooled power packages across various applications.**

Keywords—Power Electronics, Wide-Bandgap semiconductors, Silicon-Carbide, SMT, top-side-cooled packages, full-bridge topology, PCB layout, high power, Silicon Carbide, wide bandgap, optimization of electrical performance, best practice sharing.

I. Introduction

Reduced power-converter performance is significantly attributable to parasitic stray inductance in the converter's power-loops. Large parasitic stray inductances lead to a decline in switching speed, which is, in turn, a consequence of the reluctance exhibited by these parasitic elements. Moreover, the parasitic inductances contribute to unwanted energy accumulation within their magnetic fields in the power converter which cause elevated commutation losses and ultimately, limit the effective switching frequency of the power converter. Consequently, the impact of the stray inductance of power-loops has been extensively researched in literature [1-11].

This paper expands upon this research, focusing on top-side-cooled surface-mount-technology (SMT) packages, which offer a promising solution for enhanced thermal and high-class electrical performance. This work highlights the design process's degrees of freedom and their impact on electrical performance, specifically stray inductance, switching behavior, and voltage overshoots, using an optimized test board. Chapter II presents an overview of the test board and its fundamental underlying concepts, such as the power plane concept and the placement of the Q-DPAK top-side-cooled power packages. Chapter III explores the magnetic field compensation, a promising approach for minimizing the power-loop inductance. This chapter therefore displays the influence of geometrical factors given by the printed circuit board (PCB) design. Results show that excellent switching performance can be achieved by applying the magnetic field reduction principle, as demonstrated by the latest 750 V Silicon-Carbide (SiC) G2 automotive power switches in industry-standard top-side-cooled SMT packages (Q-DPAK). Subsequently, the power-loop inductance of the board is determined via two distinct methods: an experimental extraction of the stray inductance and a simulation of the stray inductances with a 3D FEM simulation. These two methods deliver closely aligned results, with the 3D FEM simulation offering deeper insights into board parasitics, including current distribution within the power-loops.

II. Description of Eval Board

The test vehicle used for this research is shown in **Fig. 1**. The board utilizes four latest-generation SiC power MOSFETs "AIMDQ75R016M2H" with 16 mΩ on-channel resistance, a rated voltage of 750 V and automotive qualification (AEC-Q101). This second generation of Infineon's SiC MOSFET technology offers industry leading figure-of-merits, which show their full benefit when these switches are used in low-parasitic environments.

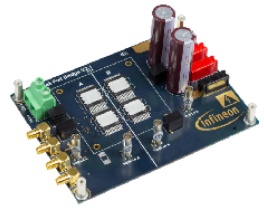


Fig. 1. Image of the full-bridge test PCB used for research (top-view)

Especially worth mentioning is, that the Silicon Carbide technology from Infineon is fully capable to be safely turned-off with 0 V while also enabling second-source compatibility by supporting negative turn-off voltages. This is enabled by a superior device design, an industry leading SiC technology

XXX-X-XXXX-XXXX-X/XX/$XX.00 ©20XX IEEE



- PDE: CoolSiC™ Gen2 in Q-DPAK (Wave 1) and H-D2PAK(Wave2)
- SIC4NIK (Gen1&Gen2) - main PDE/PAE contact for NIK customer

Anshul Tyagi



- PDE: CoolSiC™ Gen2 in Q-DPAK (Wave 3 – 4,7&11mΩ), Gen2 in TO263-7(Wave4) and Gen2 in TO247-4 (Wave6)
- Innovation Roadmap (TSC with DCB, integrated HB in H-DPAK TSC &TOLT)

Josef Wildauer



- PDE: Next Gen CoolSiC™ AUTO
- Innovation Roadmap (BDS H-DPAK & Cycloconverters)

Manuel Gomez



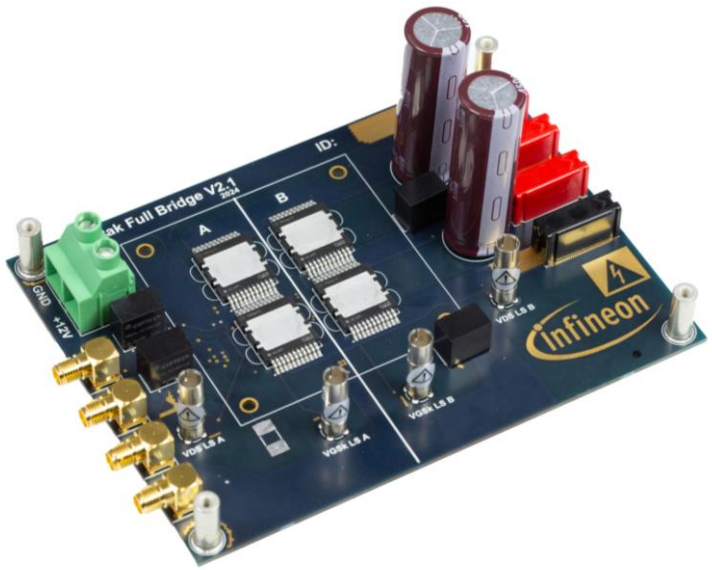
- PAE: G2M and Customer support for released CoolMOS™ and CoolSiC™ Gen1&Gen2 Products
- Tiny Power Box corporation with SAL
- Must Win Projects - TM support

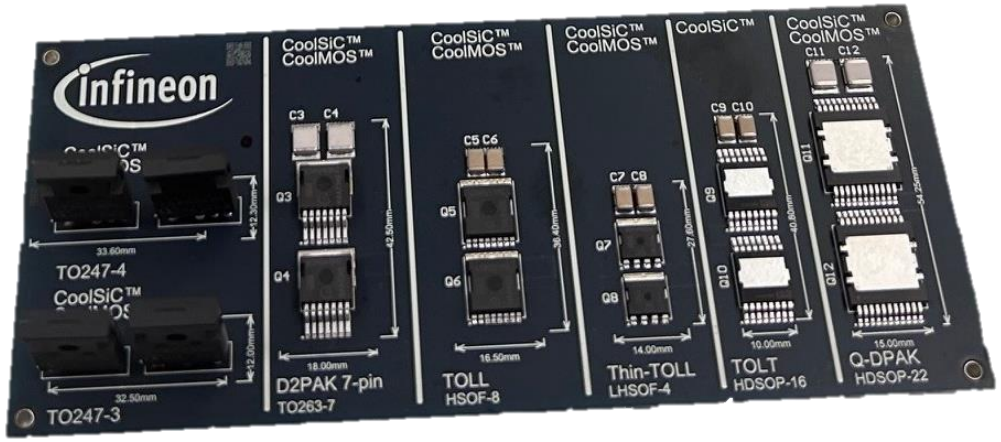
Severin Kampl

Copyright © Infineon Technologies AG 2025. All rights reserved.

Eval Boards

Goto/PL52_TM







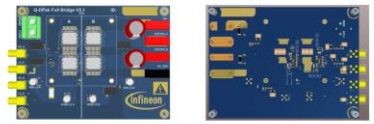
Eval Board "Q-DPAK Full-Bridge V2.1" with 750V SiC gen2 Auto MOSFETs

HQ contact: Severin Kampl, PSS PS HV (PL52)

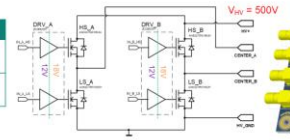
Why	**To fulfill customer demands; support customers in their Q-DPAK evaluation**
Planned Outcome	Eval Boards, ready to ship to customers, public design resources, public board description

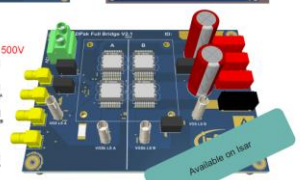
Description

- Simple eval board showing how to use SiC MOSFETs in Q-DPAK.
- Flexible board to evaluate top-side colling devices electrically and thermally in customer's lab.
- Guide customers in design-in of Q-DPAKs by offering a reference layout with optimized power- and gate-loop design.
- Eval board with Best-in-Class CoolSiC 750V Automotive gen2 devices
- Long-term support by TM team



S. No	Hero Part	Device
1	AIMDQ75R016M2H	IFX 750 SiC Auto gen2
2	2EDB9259Y	IFX HV isolated 2CH gate driver

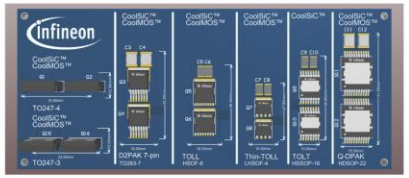




12 February 2025 Copyright © Infineon Technologies AG 2025. All rights reserved. 2

High Voltage Power Packages Demonstrator

Features	Benefits
• Innovative cooling concepts: BSC & TSC • Optimized design of the half bridge • Lower stray inductance	• Faster & cheaper in production assembly • Higher switching capabilities • Better control & reduced power losses



Potential Applications Automotive	Potential Applications Industry
• Uni- and bidirectional on-board chargers • HV-LV DC-DC converter for electric vehicles • Circuit breakers (HV battery disconnect switch, DC and AC low frequency switch, HV E-fuse)	• AC-DC power conversion for telecom infrastructure • EV charging • Motor Control • Photovoltaic



18 Mrz 2023 Copyright © Infineon Technologies AG 2023. All rights reserved. 3

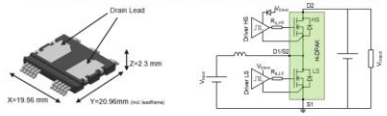
l Board H-DPAK Half-Bridge V1

Board components
50V CoolSiC™ Gen 2: AIMSH75H025M2H Gate Driver: 1ED3142MU12F

Main specifications
00 – 350 V nominal input voltage **A** nominal input current **00 V output voltage** -6 A nominal output current p to **2500 W output power** requency **100kHz** **Unipolar driving 0V/18V**

Features
l Board H-DPAK Half-Bridge V1 can be operated **louble-pulse, buck or boost converter**

Simple Schematic - Syn. Boost Converter



Typical appearance



2025-01-09 **restricted** Copyright © Infineon Technologies AG 2025. All rights reserved. 4

Copyright © Infineon Technologies AG 2025. All rights reserved.

Check out our additional information

Collaterals and brochures

- Product briefs
- Application brochures
- Presentations
- Press releases

Technical material

- Application notes
- Technical articles
- Simulation models
- Datasheets, MCDS files

Hardwares

- Evaluation boards

Training

- Training Videos

Application

- Application know-how

https://www.infineon.com/OBC

https://www.infineon.com/hv-dcdc

www.infineon.com/coolsic-g2

Scan QR-code for more info

Automotive SiC MOSFETs

https://www.infineon.com/cms/en/product/power/mosfet/silicon-carbide/750v/

Copyright © Infineon Technologies AG 2025. All rights reserved.


Infineon