Recommendations for board assembly of Infineon wafer level diode packages



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Acronyms and abbreviations

AOI	automated optical inspection
AXI	automated X-ray inspection
BTC	bottom terminated component
CSP	chip scale package
ESD	electrostatic discharge
MSL	moisture-sensitivity level
Ni(P)/Pd/Au	nickel-phosphorous/palladium/gold
NSMD	non-solder mask defined
PG	plastic green
PCB	printed circuit board
SAC	tin silver copper (SnAgCu)
SMD	solder mask defined pad
SMD	surface-mount device
SMT	surface-mount technology
SPI	solder paste inspection
TSSLP	thin super small leadless packages
TVS	transient voltage suppressor
WLL	wafer level leadless package
WLP	wafer level packages

1 Package description

This document provides information about the surface mount technology (SMT) board assembly of Infineon wafer level leadless (WLL) packages. The transient voltage suppressor (TVS) diode products can be applied as electrostatic discharge (ESD) protection in high component density circuitry. As bare silicon chip scale packages (CSP) without any packaging they feature smallest dimensions and are therefore especially appropriate for miniaturization in applications with limited space. The absence of internal interconnects (e.g. wire bonds or flip chip connections) or redistribution layers allow for high performance with low inductance.

This document does not discuss wafer level packages (WLP) or thin super small leadless packages (TSSLP) although the latter can have similar footprints (e.g. PG-TSSLP-2-1 vs. SG-WLL-2-1). These package families are described in separate documents.

1.1 WLL package type

Infineon WLL ESD diode packages are available with a 0201 (imperial code, relates to 0603 metric code) and 01005 (imperial code, relates to 0402 metric code). Metric dimensions are of 0.58 x 0.28 mm and 0.43 x 0.23 mm respectively with a very low thickness of less than 200 µm. **Figure 1** shows examples of the WLL package family.

- SG-WLL packages

SG = silicon green
WLL = wafer level leadless

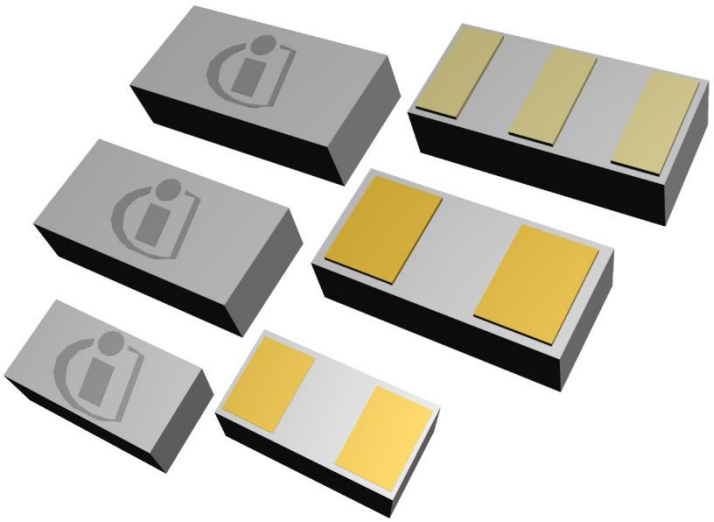


Figure 1 Examples of WLL packages.

1.2 Package features and general handling guidelines

General handling guidelines

Bare silicon semiconductor devices are sensitive to mechanical handling and contamination. Therefore, they require specific precautionary measures to ensure that they are not damaged during transport, storage, handling, and processing.

Manual handling of components in or out of the component packing may cause mechanical damage to the silicon body. The mechanical properties of the package body are mainly determined by the silicon, which is much more brittle than the mold compound of plastic package types. In case it is necessary to handle packages for purposes such as analysis, plastic tweezers should be used instead of metal ones. Vacuum tweezers would be the ideal choice.

Note: Any manual handling of WLL packages during board assembly should be avoided.

After board assembly WLL packages are mechanically fixed to the printed circuit boards (PCB) by the solder connection. However, their silicon bodies are not protected from the environment. When handling the assembled PCBs it is necessary to protect the components from any mechanical impact. One may consider the following items:

- Use support pins for solder-paste printing of the second PCB side.
- Take care during insertion of assembled PCBs into magazines or the housing of the application.
- Use specific clamping or support in adapters for electrical testing, or insertion of the assembled PCBs into the housing of the application.

The silicon body wafer level packages can be protected from mechanical impact by placing the passive components of a PCB design close to them. Due to their increased height they can act as distance holders. In case the PCB design does not allow for placing functional passives close to the packages they can also be used in a non-functional “dummy” configuration. The specific dimensions as well as the number of passive components per side needs to be chosen according to the package size of the WLL packages to protect.

For further information about component handling, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

Internal construction

The WLL packages are of bare silicon without additional packaging. Metallizations are directly applied onto the active silicon die. The absence of internal interconnects or redistribution layers allow for optimum package-to-chip ratio. An additional wettable surface finish forms the pads for board mounting. Open surfaces on the active side of the product are covered by silicon nitride passivation. A schematic of the inner setup of WLL packages is shown in **Figure 2**.

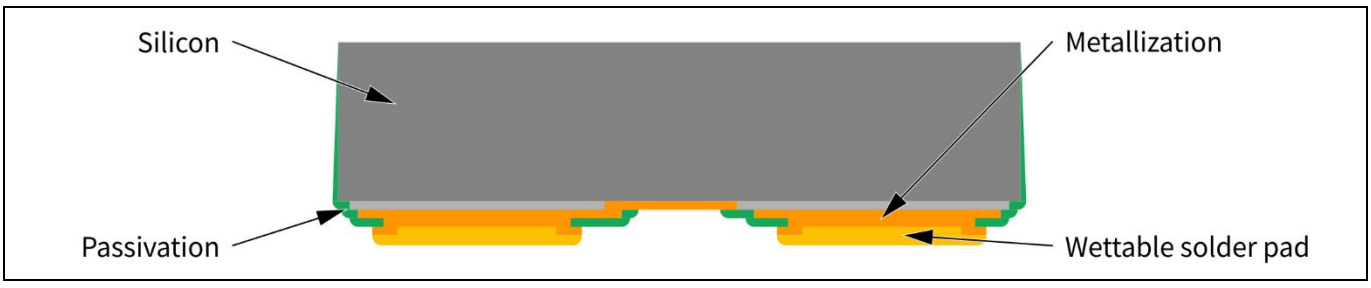


Figure 2 Schematic showing the inner setup of a WLL package.

Package description

Termination design

The leadless landing area of the WLL packages are forming a solder joint of bottom terminated component (BTC) type. As a result the solder joint is formed only beneath the component body as shown in **Figure 3**. When mounting the WLL to A PCB special attention should be given to the package-to-board stand-off as the solder joints are very small and the board most propably features a solder mask layer.

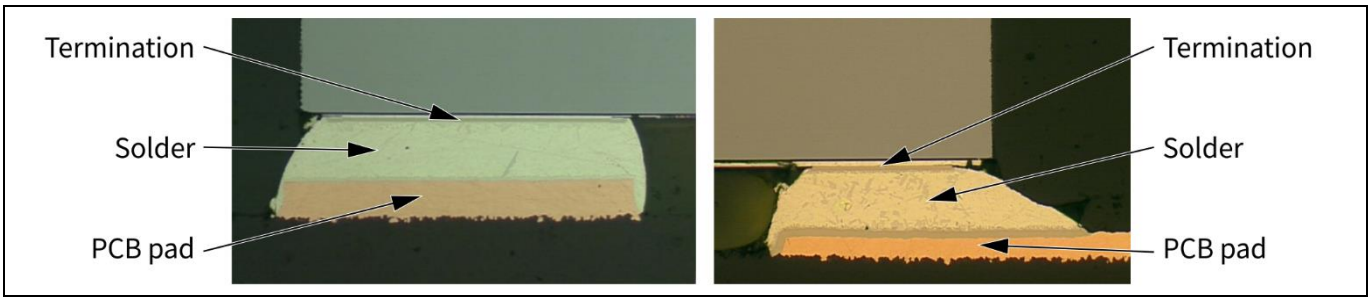


Figure 3 Cross-sections through SG-WLL solder joints of 0201 (left) and 01005 body size (right).

Termination plating

Infineon WLL packages are equipped with a nickel-phosphorous/palladium/gold (Ni(P)/Pd/Au) final finish stack-up providing a very stable solderability performance. During reflow the sacrificial Pd/Au layer is dissolved and the solder connection is then made with the Ni layer.

2 Printed circuit board

2.1 Routing

The small termination size of WLL packages implies the application of fine-line PCBs with conductor width/spacing of 100 µm or less (e.g. 75 µm). The specific PCB design strongly depends on the board technology (e.g. conventional technology with drilled vias, build-up technology with microvias, flex substrate), the conductor width/spacing, number of metal layers, and electrical restrictions.

Printed circuit board design and construction are key factors for achieving solder joints with high reliability. In case double sided mounting is used packages should generally not be placed opposite one another. That stiffens the assembly and results in earlier solder-joint fatigue compared to a design where the components are offset.

2.2 Pad design

The quality and reliability of interconnect solder joints to the board are affected by:

- Pad type (solder mask defined, SMD or non-solder mask defined, NSMD)
- Specific pad dimensions
- Pad finish (also called metallization or final finish)
- Via layout and technology

The size of the PCB pads is a key factor for a stable and reproducible soldering process. It is helpful to increase the PCB pad size slightly compared to the package pad size. The PCB pad designs for WLL packages must clearly be distinguished from those for passive components (typically resistors or capacitors). Although, their size can be classified by their outline dimensions in the same way (e.g. 0201), they feature a different termination geometry type. WLL packages feature no wettable sidewalls but are bottom-only terminated. The PCB pad dimensions for WLL devices are largely different from those for passive components to provide the optimum solderable area in each case. The Infineon recommended PCB pad designs will help to prevent excessive tilting or tombstoning of the WLL devices.

Note: The PCB pad designs for WLL devices must not be confused with those for passive components because they do not feature wettable sidewalls but are bottom-only terminated.

It is generally recommended to use an NSMD pad design for WLL packages. This offers the advantage of eliminating solder resist tolerances on the respective PCB footprint. Depending on the capabilities of the PCB manufacturer, it also might not be possible to separate two NSMD PCB pads of one WLL package by a solder mask dam. A single solder mask opening for both PCB pads is also suitable for generating the two separate solder joints of the component as shown in **Figure 4**.

The SG-WLL packages and their footprints are very small. Typical tolerances of the solder resist are therefore quite high in comparison with the pad dimensions. NSMD pads expose parts of the conductor tracks that are connecting the pads to the remaining circuitry because the solder mask opening is wider than the pad itself. The conductor tracks on the PCB should be as narrow as possible (100 µm or less) to minimize the influence of their additional wettable area. Furthermore, there should be only one connection per solder pad. In special case of the 3-pin WLL the conductor tracks are also forming the wettable PCB pads. It is important to extend these tracks below the solder mask on both sides of the package. Only then a symmetric pad definition can be achieved.

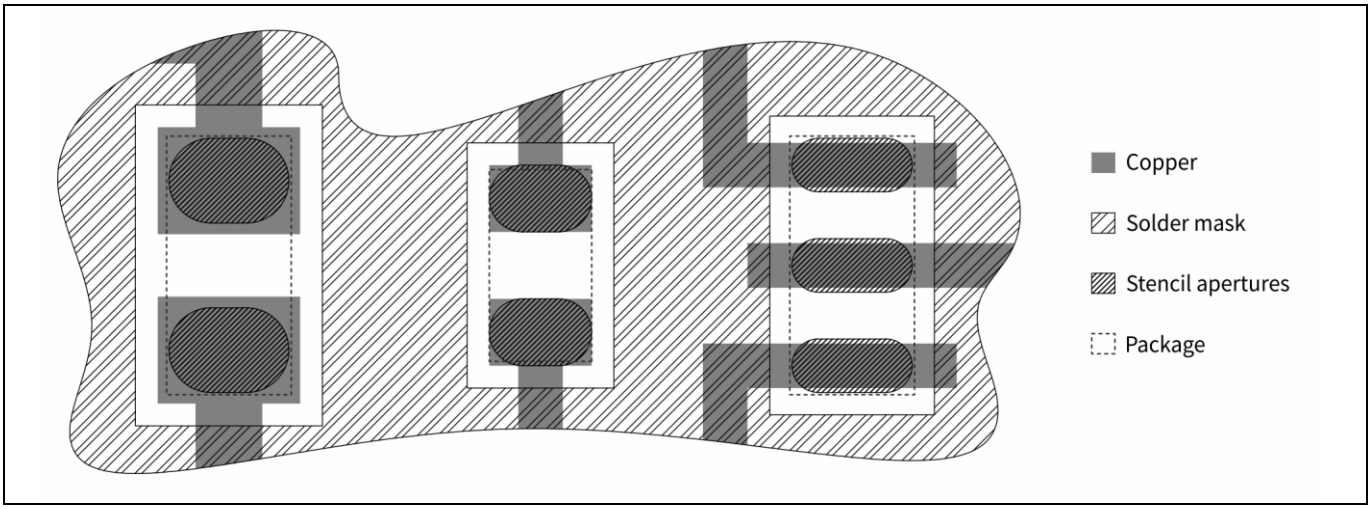


Figure 4 **Examples of pad and stencil design for 0201 2-pin WLL (left), 01005 2-pin WLL (center), and 0201 3-pin WLL package (right). In the footprint for 3-pin WLL package the conductor tracks are also forming the wettable pads. The therefore resulting half-side SMD character shall be arranged symmetrically.**

On typical 2-pin WLL the conductor tracks should be connected symmetrically and along the long side of the package. Using perpendicularly arranged tracks may cause the package to rotate due to the non-symmetric additional wettable area as shown in **Figure 5**.

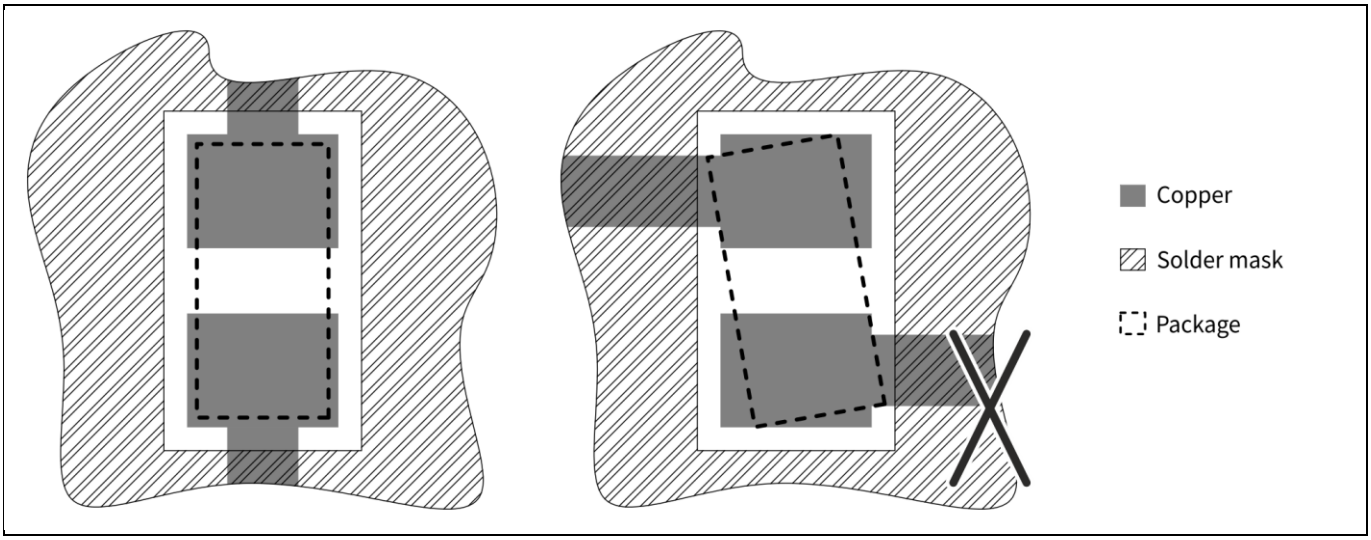


Figure 5 **Examples of a typical NSMD pad design for 2-pin WLL package (left) and of a non-prefered perpendicular arrangement of conductor tracks (right).**

An optimal PCB design generally depends on the specific application as well as on the specific design guidelines of the chosen board manufacturer.

For further information about PCB pad design, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3 PCB assembly

3.1 Solder paste stencil

In SMT the solder paste is applied onto the PCB metal pads by stencil printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. While an excessive solder paste volume will cause solder bridging, an insufficient solder paste volume can lead to reduced solder spreading between all contact surfaces. To ensure a uniform and sufficiently high solder paste transfer to the PCB, laser-cut (mostly made from stainless steel) or electroformed stencils (made from nickel) are preferred. The latter are applied especially when fine-pitch components are assembled. The quality of the small stencil aperture sidewalls is especially important for a stable and repeatable printing result. This should be taken into account when choosing the stencil technology. The application of so called “nano-coatings” on stainless steel stencils is recommended to increase stencil transfer efficiency.

In most cases, the thickness of a stencil has to match the needs of all components on the PCB. For the smallest components, however, the solder paste printing process is of specific importance to the quality of the final solder joint. The solder paste printing process should be well-controlled, especially when it comes to the alignment between the stencil apertures and the PCB pads. It is also recommended to focus specifically on the quality of such prints by facilitating an automated solder paste inspection (SPI). **Figure 6** shows typical SPI measurements of solder paste deposits for a WLL package size 0201 and 01005.

A stencil thickness of ≤ 90 µm, typically 80 µm (3 mil) for size 0201 and ≤ 70 µm, typically 60 µm (2 mil) for size 01005 is recommended for WLL packages. These values are based on the Infineon pad and stencil recommendations and an area ratio value of 0.66. The area ratio describes feasible stencil thicknesses in relation to their aperture sizes.

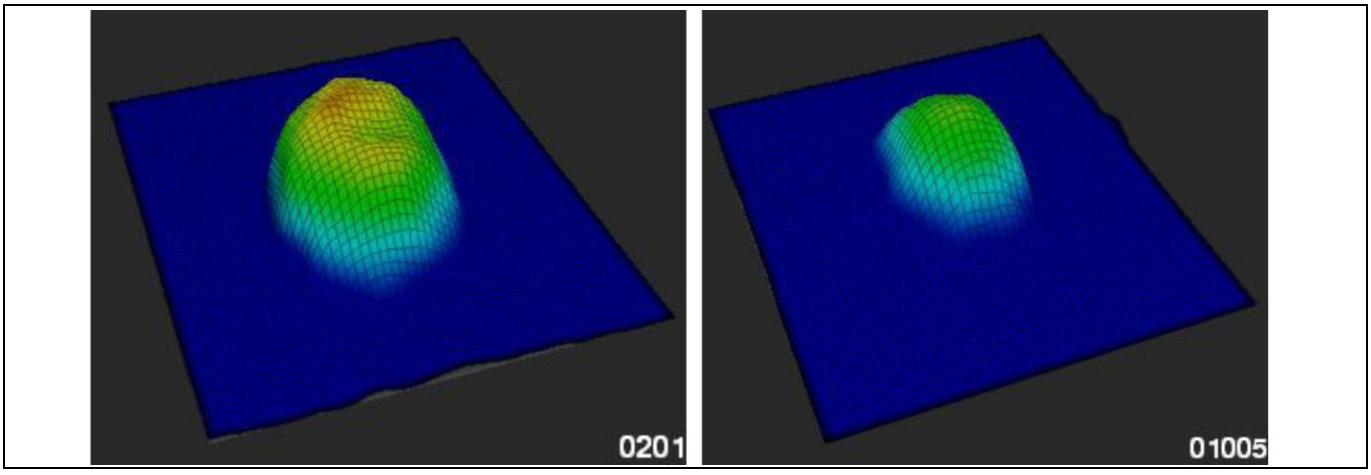


Figure 6 Typical SPI measurements of printed solder paste for 0201 (left) and 01005 (right) and WLL packages.

For individual design adaptations to reach the optimum amount of solder, the stencil thickness, the PCB pad finish, quality and solder masking, the via layout, and the solder paste type should be considered. In every case, application-specific experiments are recommended.

Further details and specific stencil aperture recommendations can be found in the package data base that is available on the Infineon web page [1]. Please choose a specific package when searching the data base, which will then show an example of the stencil aperture layout for each package.

For further information about solder stencil design, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.2 Solder paste

Pb-free solder pastes typically contain some type of SnAgCu alloy (SAC solder with typically 1-4% Ag and <1% Cu). The most common alloy is SAC305 (3.0% Ag and 0.5% Cu). The average alloy particle size must be suitable for printing the solder stencil aperture dimensions (aperture ratio, least number of solder spheres per opening). Using paste type 4 is usually applicable. Very small package pads such as those of 3-pin WLL may require a higher type with lower grain size of the solder alloy powder.

The solder alloy particles are dispersed in a blend of liquid flux and chemical additives (approx. 50% by volume or 10% by weight), forming a creamy paste. The flux and chemical solvents have various functions such as adjusting the viscosity of the paste for stencil printing or removing contaminants and oxides on the surface.

The solder paste solvents have to evaporate during reflow soldering, while residues of the flux will remain on the joint. The capacity of the flux additive for removing oxides is given by its activation level, which also affects the potential need for removing the flux residuals after the assembly. For WLL packages where the solder joint is formed mainly on the package bottom side, a “no clean” paste is recommended to avoid subsequent cleaning steps underneath the package. The small gaps make cleaning highly difficult if not impossible. Certain precautions have to be taken if any kinds of flux residues remain on the board prior to any kind of coating. Leakage currents and the potential for shortings below components have to be considered when choosing the specific flux type (e.g. halide-free vs. zero halides).

Generally, solder paste is sensitive to age, temperature, and humidity. Please follow the handling recommendations of the paste manufacturer.

3.3 Component placement

Manual handling and placement of the bare silicon WLL package body shall be avoided as it may lead to fractures and cratering. An automated pick-and-place machine is recommended to obtain reliable solder joints and to avoid damages to the silicon WLL package body.

WLL packages are very thin and therefore provided in similarily thin embossed plastic carrier tape. For smooth processing of the tape in the pick-and-place machine, the mechanical setup of the feeder should avoid any vibration during the movement of the tape into the machine. The tape in the area where the components will be picked from the tape should be properly clamped. Any mechanical supporting parts that touch the tape from the bottom that are mounted in the feeder below the tape should be removed. Such mechanical parts are only useful for paper tape.

It is necessary to select a suitable nozzle for the pick-and-place process. The nozzle size (outer dimensions) should not exceed the package dimensions. Larger nozzles can lead to pick-up errors. In most cases the WLL devices are picked “contactless”. The nozzle is positioned closely above the package and the grip will be established by activating the underpressure. Choosing the wrong nozzle might lead to damages of the silicon body edge or early wear out of the nozzle. The preferred nozzle materials are rubber and plastic. Metal and ceramic tools may cause scratches on the component surface and should therefore be avoided.

Note: *Rubber and plastic are preferred pick-and-place vacuum nozzle materials. Metal or ceramic tools may cause damages to the component surface.*

The components have to be placed accurately despite the self-alignment effect that is caused by the surface tension of the liquid solder. Component placement accuracies of +/-50 µm and less are obtained with modern

automatic component placement machines using vision systems. With these systems, both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB, or at additional individual mounting positions (local fiducials). It is recommended to “teach” the vision system to recognize the package pads in addition to the package outline. The maximum tolerable displacement of the components is 25% of the metal pad width on the PCB. For WLL packages, this means the displacement should be below 50 µm. An increased placement force may squeeze the solder paste causing solder joint shorts or beading. Special care must be taken when processing the smallest packages that allow no solder mask dam in between the PCB pads.

For further information about component placement, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.4 Reflow soldering

The widely used method of reflow soldering in a forced convection reflow oven is recommended for the PCB assembly of WLL packages. Soldering in a nitrogen atmosphere can generally improve the solder joint quality but is not necessary to create a reliable joint.

The soldering profile should be in accordance with the recommendations of the solder paste manufacturer to achieve optimal solder joint quality. The position and the surroundings of the component on the PCB, as well as the PCB thickness, can influence the solder joint temperature significantly. Especially for small components, it is recommended to optimize the reflow profile in such a way that excessive flux or solder spattering is avoided.

PCB assemblies usually carry a variety of package types and sizes. The reflow profile therefore has to meet the requirements of all components and materials. We recommend to measure the solder-joint temperatures by thermocouples beneath or close to the relevant packages. Components with large thermal masses do not heat up at the same speed as lightweight components. In addition, the position and the surroundings of the package on the PCB, as well as the PCB thickness, can influence the solder-joint temperature significantly.

Minimum reflow conditions

The lower temperatures and durations of an optimal reflow profile must stay above those of the wettability qualification. The solderability of the terminations of Infineon components is tested according to the standards IEC 60068-2-58 and J-STD-002 [2][3].

Maximum reflow conditions and cycles

Components that are moisture-sensitivity level (MSL) classified by Infineon have been tested by three reflow runs in accordance with the J-STD-020 standard, covering a double-sided reflow and one rework cycle. The maximum temperatures must not be exceeded during board assembly. Please refer to the product barcode label on the packing material that states this maximum reflow temperature according to the J-STD-020 [4] standard as well as the MSL according to the J-STD-033 standard [5].

Infineon WLL packages are generally suited for double-sided PCB mounting. That means that both sides of the PCB are fitted and reflowed one after another. As a consequence, the side that was initially assembled experiences two reflow cycles. During the second cycle, the components are hanging upside-down. Therefore, during the peak zone of the reflow profile (where the solder is liquid), the components are only held by wetting forces of the molten solder. Gravity acting in the opposite direction will elongate the solder joints especially of packages with higher mass. On the top side, gravity forces the components nearer to the PCB surface. These shapes will be frozen during cooling and therefore will result in a higher stand-off on the bottom side after the

reflow process. Any mechanical impacts on components that are undergoning reflow in an upside down position should be avoided.

For further information about reflow soldering, please refer to *the General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

4 Cleaning

Certain flux residues will remain on the board after the soldering process; especially near the solder joints. An effective cleaning beneath a component with bottom-only terminations is generally difficult up to impossible due to the small gap between the component body and the PCB. Therefore, a “no-clean” flux is recommended whose residues usually do not have to be removed after the soldering process.

In case the solder joints are cleaned, the cleaning method (e.g. ultrasonic, spray, or vapor cleaning) and cleaning solution have to be selected taking into account the type of package, the flux used in the solder paste (rosin/resin-based, water-soluble, etc.) as well as the environmental and safety aspects. Even small residues of the cleaning solution should be removed or dried out very thoroughly. For recommended cleaning solutions, please contact the solder paste or flux manufacturer.

5 Inspection

5.1 Optical solder joint inspection

A visual inspection of the solder joints of WLL packages with conventional automatic optical inspection (AOI) systems is not possible as the solder joints are formed only underneath the package. Manual visual inspection is limited to the outer surface of the solder joints. The solder joint quality may be judged by choosing an angular view. **Figure 7** shows top and angular views of 0201 and 01005 size WLL packages.

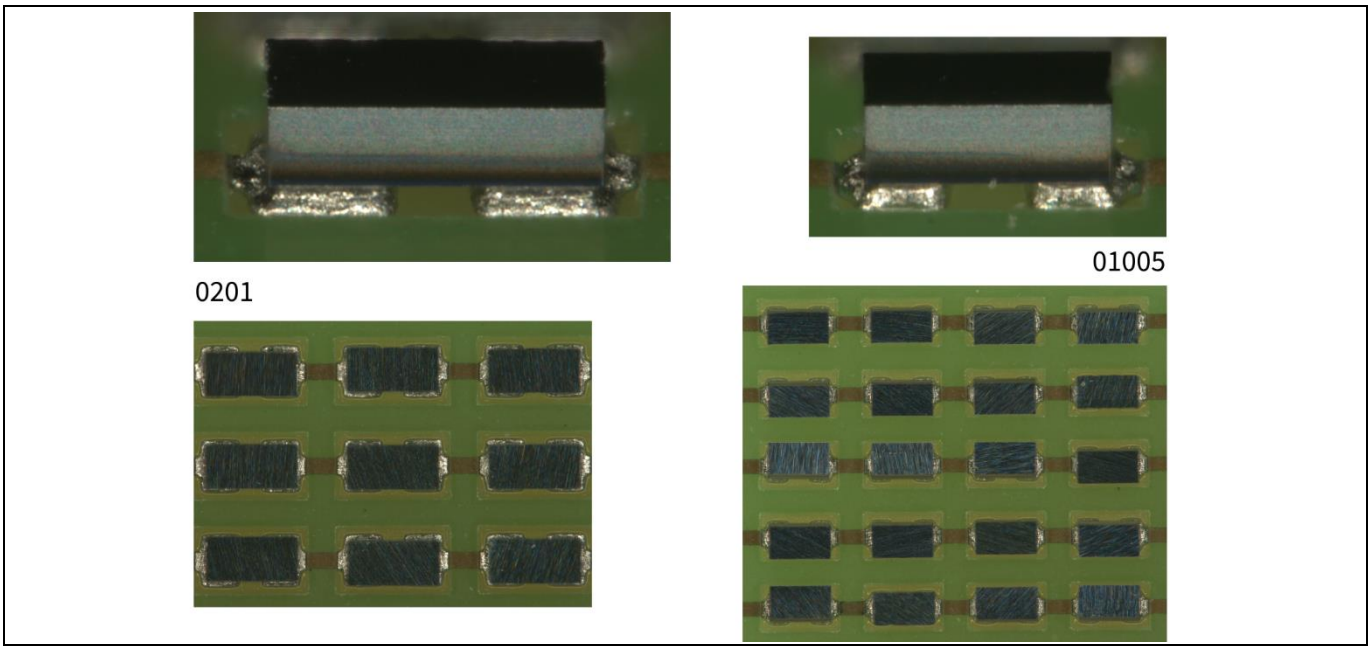


Figure 7 Top and side views of properly mounted WLL packages of 0201 (left) and 01005 size (right).

The bare silicon surface of the WLL package top side results in different light reflectivity even at slightes tilting angles. Judging the solder joint quality from such package back side reflection differences is not recommended as it is not displaying an actual deviation. The 2-pin packages always feature a certain tilt after board assembly. Internal investigations on the 2nd level reliability have proven that the natural tilt of Infineon WLL packages does not affect the solder joint lifetime.

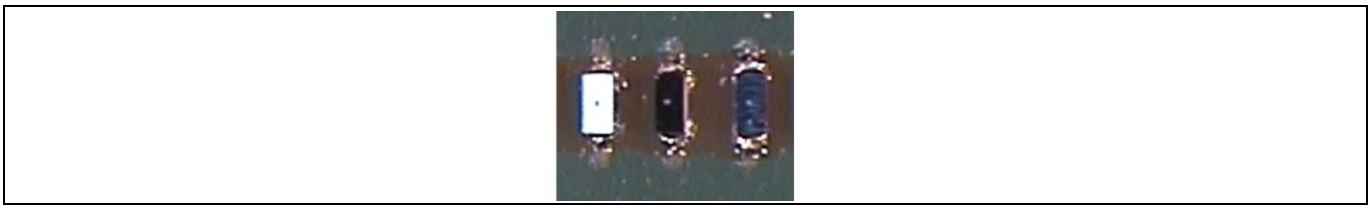


Figure 8 Mounted 2-pin WLL packages showing different light reflection due to slight tilting.

For engineering tasks, cross-sectioning can offer detailed information about the solder joint quality. Due to its destructive character, cross-sectioning during monitoring is naturally not practical.

5.2 X-ray solder joint inspection

automated X-ray inspection (AXI) systems are appropriate for efficient inline control of components that cannot be inspected properly by optical systems. AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hardware and software needed for inspecting, controlling, analyzing, and data transferring routines. These reliable systems enable the user to detect soldering defects such as poor soldering, bridging, voiding, and missing parts. However, other defects such as broken solder joints are not easily detectable by X-ray.

Figure 9 shows a typical X-ray photograph of a WLL package. The solder joints and PCB internal layers are visible. Voiding may occur due to the outgassing of the organic compounds from solder paste during reflow. Generally, the extent of voiding depends on the board pad size, the stencil layout, the solder paste, and the reflow profile.

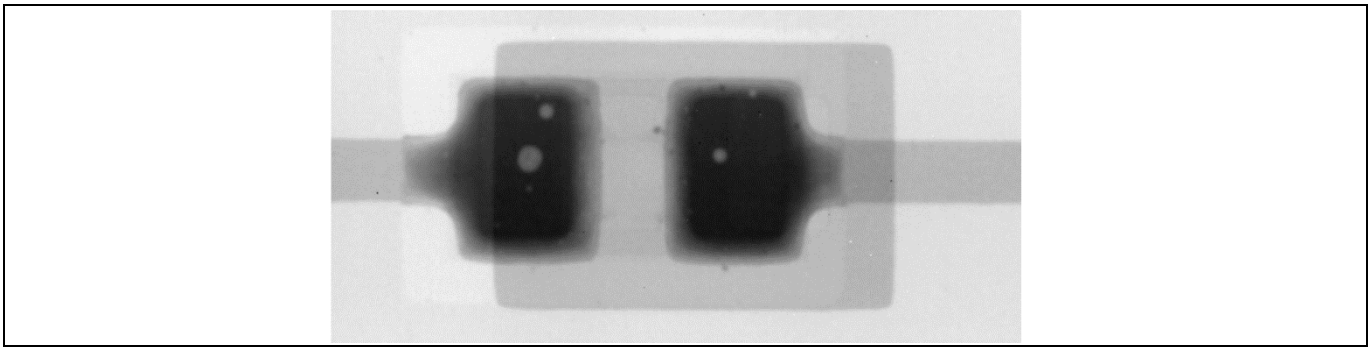


Figure 9 Typical X-ray image of a SG-WLL-2-1 package soldered to PCB. The view is slightly angled.

For the acceptability of electronic assemblies, please refer to the IPC-A-610 document [6].

6 Rework

Single solder joint repair of bottom-only terminated packages is highly difficult, if not impossible, and is therefore generally not recommended. Furthermore, the reuse of de-soldered components is not recommended. The de-soldered components should be replaced by new ones.

A rework process is commonly done on special rework equipment. There are various systems available that meet the requirements for reworking SMD packages. All handling guidelines discussed in this document have to be respected. Special focus should be on the following items:

- Due to the decreased automation level given by the general rework approach, even higher care compared to standard assembly must be taken. Tools that do not damage the component mechanically have to be chosen. Mechanical forces that do not necessarily cause visible external damage can still cause internal damage that reduces the component's reliability. A proper handling system with vacuum nozzle may be the gentlest process and is therefore recommended. However, the impact of rework tools has to be assessed properly. In general, more manual handling increases the effort for documentation, training, and monitoring of the rework process(es).
- During rework, special care must be taken concerning the proper moisture level of the component according to the J-STD-033. Drying the PCB and the component prior to rework might be necessary. A proper drying procedure for SMD packages is described in the international J-STD-033 standard [5]. Please also refer to the recommendations of your PCB manufacturer and take all specific needs of components, PCB, and other materials into account.
- Whatever heating system is used (hot air, infrared, hot plate, etc.), the applied temperature profile at the component must never exceed the maximum temperature according to the J-STD-020 standard. Depending on the specific heating profile used during rework, components adjacent to the mounting location might also experience a further "reflow run" in terms of the J-STD-020 standard [4]. Internal investigations have shown that the temperature profile must be recorded.

If a device is suspected to be defective and a failure analysis is planned, Infineon usually expects customers to desolder the component prior to return to Infineon. The component shall be returned in a proper condition according to the original package outlines.

In some special cases such as solder joint inspection Infineon may request that the PCB or part of the PCB with the component still attached should be sent to Infineon.

Note: *Before returning a device for failure analysis at Infineon, please clarify the return condition of the suspected component (i.e. onboard or desoldered) with the Infineon Application Engineer or Customer Quality Manager who supports your company.*

For further information about component rework on PCB, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

7 References

[1] Infineon: Packages. https://www.infineon.com/packages.

[2] International Electrotechnical Commission: IEC 60068-2-58. Environmental testing - Part 2-58: Tests - Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD).

[3] Electronic Components Industry Association, Assembly and Joining Processes and JEDEC Solid State Technology Association Committee: EIA/IPC/JEDEC J-STD-002. Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires.

[4] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-020. Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices.

[5] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-033. Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.

[6] Association Connecting Electronics Industries: IPC-A-610. Acceptability of Electronic Assemblies.

Revision history

Page or reference	Major changes since the last revision
Entire document	New document template
Entire document	Introduction of SG-WLL-3-1

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