NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:
   A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES 600-60808-01_03.TGZ OR 610-60808-01_03.ZIP.
   B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.
   C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.
   D. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381 [.015] MAX RADIUS.
   E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.
   F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2 DIELECTRIC MATERIAL:
   A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (RoHS COMPLIANT EPOXY-GLASS).
   B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF.076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.
   C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.
   D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

3. DRILLING:
   A. VIA DIAMETERS (TOL. = +.051/- DRILL DIAMETER [+.0020/- DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.
   B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.
   C. FOR NON HDI BOARDS(ONLY THROUGH HOLE VIA STRUCTURE)
      THIS DESIGN REQUIRES VIA FILLING AS PER IPC-4761:TYPE 6 OR BELOW CATAGORY NON-CONDUCTIVE EPOXY VIA FILLING IS MUST.
   D. FOR HDI BOARDS(BLIND/BURIED VIA STRUCTURE)
      THIS DESIGN REQUIRES VIA FILLING AS PER IPC-4761:TYPE 7 CONDUCTIVE VIA FILLING SHOULD BE DONE FOR ALL VIAS

4. SOLDER MASK:
   A. APPLY LPI SOLDER MASK USING PROVIDED DATA.
   B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR BLUE.
   C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

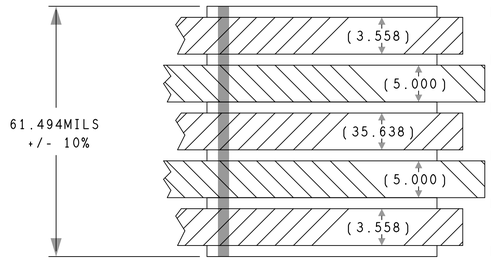
5. MARKING:
   A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

6 ELECTRICAL TEST:
   A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.
   B. ALL PCBS SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.
   C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY
7 TO PANEL RAILS IF SPACE DOES NOT PERMIT.

   FINAL FINISH:
   A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSION GOLD (ENIG) PER IPC-4552.

8. IMPEDANCE:
   A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.
   B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.

9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBS SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.



LAYER DESCRIPTION	START COPPER WT	SE IMP OHMS	SE TRACE WIDTH	REF LAYER	DIFF IMP OHMS	DIFF TRACE WIDTH/SPACE	REF LAYER	DIFF IMP OHMS	DIFF TRACE WIDTH/SPACE	REF LAYER
L01 - TOP	0.5 OZ	50E	5.9MIL	L02	90E	4.5/4.5	L02	100E	4.0/6.0	L02
L02 - PLANE	1.0 OZ	--	-----	---	---	----	---	---	----	---
L03 - SIGNAL	1.0 OZ	50E	6.2MIL	L02	---	----	---	---	----	----
L04 - SIGNAL	1.0 OZ	50E	6.2MIL	L05	---	----	---	---	----	----
L05 - PLANE	1.0 OZ	--	-----	---	---	----	---	---	----	---
L06 - BOTTOM	0.5 OZ	50E	5.9MIL	L05	90E	4.5-/4.5	L05	---	----	----

STACK-UP

RESTRICTED

SEE BOM	SEE BOM
NEXT ASSY	USED ON
APPLICATION	

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN METRIC WITH INCHES IN BRACKETS
.XXX ±.064 [±.005] .XX ±.13 [±.01] ANGLES ±.5°

MATERIAL 2

FINISH 7

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN PRAO	07/06/26
ENGINEER MADHU	07/06/26
CHECKER -	-
QA -	-
PROJ. ENG. -	-

Infineon Technologies AG
Am Campeon 1-15
85579 NEUBIBERG - GERMANY

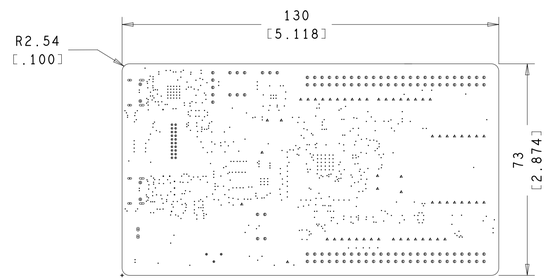
TITLE: PCB FABRICATION, PSoC CONTROL C3M6 EVALUATION KIT

SIZE	CAGE CODE	CY P/N	
D	-	610-60808-01	
SCALE 1/1		SHEET 1 OF X	REV 03

COMPUTER GENERATED DRAWING
DO NOT CHANGE MANUALLY

ALLEGRO FILE: 600-60808-01_03.BRD

ANT FILM - details



DRILL CHART: TOP to BOTTOM						
ALL UNITS ARE IN MILS						
FIGURE	FINISHED_SIZE	FINISHED_TOL	DRILLED_SIZE	DRILLED_TOL	PLATED	QTY
·	8.0	+3.0/-3.0	-	-	PLATED	672
·	12.0	+3.0/-3.0	-	-	PLATED	7
+	27.56	+3.0/-3.0	-	-	PLATED	20
+	29.92	+3.0/-3.0	-	-	PLATED	3
⊕	39.37	+3.0/-3.0	-	-	PLATED	118
^	40.16	+3.0/-3.0	-	-	PLATED	59
⊗	51.18	+3.0/-3.0	-	-	PLATED	2
⊕	25.59	+2.0/-2.0	-	-	NON-PLATED	4
⌔	55.12x23.62	+3.0/-3.0	-	-	PLATED	4
⌔	66.93x23.62	+3.0/-3.0	-	-	PLATED	4
					TOTAL HOLES:	893

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SIZE	CAGE CODE	CY P/N
D	-	610-60808-01
SCALE 1/1		SHEET 2 / REV 03

COMPUTER GENERATED DRAWING
DO NOT CHANGE MANUALLY

ALLEGRO FILE: 600-60808-01_03.BRD

ANT FILM - details