PSOC™ high-voltage (HV) precision analog (PA) MCU: PSOC™ HVPA-144K registers

Reference manual

About this document

Scope and purpose

The PSOC™ HV-PA-144K registers reference manual provides reference information for registers and contains respective programming details.

Intended audience

This reference manual is intended for the system designers, programmers, and so on who are designing, or programming using PSOC™ HV-PA-144K parts.

Definitions

Register Permission

The following table lists the register permission based on protection context and priviledges.

Permission	Description
READ	User mode = Read access, privilege mode = read, Non-secure = yes
PRIVILEGE - WRITE	User mode = Read access, privilege mode = Read and Write access, Non-secure = yes
NO-ACCESS	User mode = No access, Privilege mode = No access, Non-secure = yes
SECURE - READ	User mode = Read access, Privilege mode = Read access, Non-secure = No
FULL	Read and Write access in all modes, Non-secure = yes

Software Access

The following table lists the behavior of registers, on various Software Read/Write Accesses.

SW Access	HW Access	Software Reads Register	Software Writes Register	Software Description
R	any	Register contents	Ignored	Software read-only
RW	any	Register contents	Register takes data written	Software read and write
RW1S	any	Register contents	Every bit is set upon writing 1	Software read and write 1 to set
RW0S	any	Register contents	Every bit is set upon writing 0	Software read and write 0 to set
RW1C	any	Register contents	Every bit is cleared upon writing 1	Software read and write 1 to clear
RW0C	any	Register contents	Every bit is cleared upon writing 0	Software read and write 0 to clear
RW1SC	any	NA	NA	Illegal
RW0SC	any	NA	NA	Illegal
W	any	Zero	Register takes data written	Software write only
W1S	any	Zero	Every bit is set upon writing 1	Software write 1 to set (no read)
W0S	any	Zero	Every bit is set upon writing 0	Software write 0 to set (no read)
W1C	any	Zero	Every bit is cleared upon writing 1	Software write 1 to clear (no read)
W0C	any	Zero	Every bit is cleared upon writing 0	Software write 0 to clear (no read)
W1SC	any	NA	NA	Illegal
W0SC	any	NA	NA	Illegal
A	any	NA	NA	Illegal

Hardware Access

The following table lists the behavior of registers, on various Hardware Read/Write Accesses.

HW Access	SW Access	Hardware Description
any	R	Hardware read only
any	RW	Hardware read and write
any	RW1S	Hardware read and set
any	RW0S	Hardware read and set
any	RW1C	Hardware read and clear
any	RW0C	Hardware read and clear
any	RW1SC	Hardware read and set/clear
any	RW0SC	Hardware read and set/clear
any	W	Write access only
any	W1S	Hardware set
any	W0S	Hardware set
any	W1C	Hardware clear
any	W0C	Hardware clear
any	W1SC	Hardware set/clear
any	W0SC	Hardware set/clear
R	A	Not supported
RW	A	Hardware read and write
RW1S	A	Hardware read and set
RW0S	A	Hardware read and set
RW1C	A	Hardware read and clear
RW0C	A	Hardware read and clear
RW1SC	A	Not supported
RW0SC	A	Not supported
W	A	Not supported
W1S	A	Not supported
W0S	A	Not supported
W1C	A	Not supported
W0C	A	Not supported
W1SC	A	Not supported
W0SC	A	Not supported

Core, Bus and Memory Access

The Cortex-M0+ CPUSS uses AHB-Lite also for the system interconnect. Most of the IPs are compliant to the AHB-Lite protocol.

The AHB-Lite protocol is little endian; the least significant byte of a word is mapped onto the word's lowest byte address IPs use a bus data width of 32 bit.

This allows for byte (8-bit), halfword (16-bit) and word (32-bit) transfers. We distinguish two types of transfer types:
- MMIO registers: These registers are typically used for IP control and status information. Unless otherwise noted, transfers to these registers must be 32-bit transfers; any other transfer size generates an AHB-Lite bus error. An IP's MMIO registers do not necessarily fully occupy a consecutive memory region; i.e. holes may be present in the region
- Memory structures: This includes generic memory structures, such as system FLASH, system RAM and system ROM, but also IP specific memory structures. Transfer to these memory structures may be 8-bit, 16-bit or 32-bit transfers; any other transfer size generates an AHB-Lite bus error. A memory structure fully occupies a consecutive memory region; i.e. no holes are present in the memory structure region

A bus slave memory region may contain both MMIO registers and zero or more memory structures. Gaps might exist in the bus slave's memory region, either due to gaps in the MMIO memory region or gaps between the MMIO and memory structure region(s)

Gaps in the address space are reserved. Do not access these gaps, if accessed can result in Hard faults or BUS ERROR depending on which bus segment or a peripheral an address space is allocated to.

List of Partnumber

This TRM is valid for the following part numbers.

MPN	Package	Code Flash(KB)	Work Flash(KB)	SRAM(KB)
CY8C4126LCE-HV403	32-QFN	64	8	4
CY8C4126LCE-HV413	32-QFN	64	8	4
CY8C4126LCE-HV423	32-QFN	64	8	4
CY8C4127LCE-HV403	32-QFN	128	8	8
CY8C4127LCE-HV413	32-QFN	128	8	8
CY8C4127LCE-HV423	32-QFN	128	8	8
CY8C4147LCE-HV403	32-QFN	128	8	8
CY8C4147LCE-HV413	32-QFN	128	8	8
CY8C4147LCE-HV423	32-QFN	128	8	8

Memory mapping

MMIO	IP	Address	Description
CM0P	CM0P	0xe0000000	Cortex-M0+ System Bus (ARM PPB Peripherals)
CPUMEMSSV3_VER3	CPUSS	0x40100000	CPU Subsystem
	DMAC	0x40101000	DataWire/DMA Controller
	SPCIF	0x40110000	Flash Control Interface
	SPCIF1	0x40120000	Flash Control Interface
FAULT	FAULT	0x40130000	Fault structures
MMIO0	PERI	0x40010000	Peripheral Interconnect
	HSIOM	0x40020000	High Speed IO Matrix (HSIOM)
	SRSSHV	0x40030000	System Resources High Voltage Subsystem
	GPIO	0x40040000	GPIO port control/configuration
	HVSS	0x40060000	High Voltage Subsystem
MMIO1	TCPWM	0x40200000	Timer/Counter/PWM
	SCB	0x40240000	Serial Communications Block (SPI/UART/I2C)
	LIN	0x402d0000	LIN
MMIO2	PACSS	0x40300000	Programmable Analog Channel Sub-System
ROMTABLE	ROMTABLE	0xf0000000	CoreSight ROM-Table with Infineon Vendor/Silicon ID
SFLASH	SFLASH	0xfffe000	Supervisory Flash Area (Infineon Trim & Wounding Info)

1 CM0P

Description Cortex-M0+ System Bus (ARM PPB Peripherals)
Base Address 0xE0000000
Size 0x100000
Slave Num MEMORYMAP

Register Name	Address	Permission	Description
CM0P_DWT_CTRL	0xE0001000	FULL	Watchpoint Comparator Configuration
CM0P_DWT_PCSR	0xE000101C	FULL	Watchpoint Comparator PC Sample
CM0P_DWT_COMP0	0xE0001020	FULL	Watchpoint Comparator Compare Value
CM0P_DWT_MASK0	0xE0001024	FULL	Watchpoint Comparator Mask
CM0P_DWT_FUNCTION0	0xE0001028	FULL	Watchpoint Comparator Function
CM0P_DWT_COMP1	0xE0001030	FULL	Watchpoint Comparator Compare Value
CM0P_DWT_MASK1	0xE0001034	FULL	Watchpoint Comparator Mask
CM0P_DWT_FUNCTION1	0xE0001038	FULL	Watchpoint Comparator Function
CM0P_DWT_PID4	0xE0001FD0	FULL	Watchpoint Unit CoreSight ROM Table Peripheral ID #4
CM0P_DWT_PID0	0xE0001FE0	FULL	Watchpoint Unit CoreSight ROM Table Peripheral ID #0
CM0P_DWT_PID1	0xE0001FE4	FULL	Watchpoint Unit CoreSight ROM Table Peripheral ID #1
CM0P_DWT_PID2	0xE0001FE8	FULL	Watchpoint Unit CoreSight ROM Table Peripheral ID #2
CM0P_DWT_PID3	0xE0001FEC	FULL	Watchpoint Unit CoreSight ROM Table Peripheral ID #3
CM0P_DWT_CID0	0xE0001FF0	FULL	Watchpoint Unit CoreSight ROM Table Component ID #0
CM0P_DWT_CID1	0xE0001FF4	FULL	Watchpoint Unit CoreSight ROM Table Component ID #1
CM0P_DWT_CID2	0xE0001FF8	FULL	Watchpoint Unit CoreSight ROM Table Component ID #2
CM0P_DWT_CID3	0xE0001FFC	FULL	Watchpoint Unit CoreSight ROM Table Component ID #3
CM0P_BP_CTRL	0xE0002000	FULL	Breakpoint Unit Control
CM0P_BP_COMP0	0xE0002008	FULL	Breakpoint Compare Register
CM0P_BP_COMP1	0xE000200C	FULL	Breakpoint Compare Register
CM0P_BP_COMP2	0xE0002010	FULL	Breakpoint Compare Register
CM0P_BP_COMP3	0xE0002014	FULL	Breakpoint Compare Register
CM0P_BP_PID4	0xE0002FD0	FULL	Breakpoint Unit CoreSight ROM Table Peripheral ID #4
CM0P_BP_PID0	0xE0002FE0	FULL	Breakpoint Unit CoreSight ROM Table Peripheral ID #0
CM0P_BP_PID1	0xE0002FE4	FULL	Breakpoint Unit CoreSight ROM Table Peripheral ID #1
CM0P_BP_PID2	0xE0002FE8	FULL	Breakpoint Unit CoreSight ROM Table Peripheral ID #2
CM0P_BP_PID3	0xE0002FEC	FULL	Breakpoint Unit CoreSight ROM Table Peripheral ID #3
CM0P_BP_CID0	0xE0002FF0	FULL	Breakpoint Unit CoreSight ROM Table Component ID #0
CM0P_BP_CID1	0xE0002FF4	FULL	Breakpoint Unit CoreSight ROM Table Component ID #1
CM0P_BP_CID2	0xE0002FF8	FULL	Breakpoint Unit CoreSight ROM Table Component ID #2
CM0P_BP_CID3	0xE0002FFC	FULL	Breakpoint Unit CoreSight ROM Table Component ID #3
CM0P_ACTLR	0xE000E008	FULL	Auxiliary Control Register
CM0P_SYST_CSR	0xE000E010	FULL	SysTick Control & Status
CM0P_SYST_RVR	0xE000E014	FULL	SysTick Reload Value
CM0P_SYST_CVR	0xE000E018	FULL	SysTick Current Value
CM0P_SYST_CALIB	0xE000E01C	FULL	SysTick Calibration Value
CM0P_ISER	0xE000E100	FULL	Interrupt Set-Enable Register

Register Name	Address	Permission	Description
CM0P_ICER	0xE000E180	FULL	Interrupt Clear Enable Register
CM0P_ISPR	0xE000E200	FULL	Interrupt Set-Pending Register
CM0P_ICPR	0xE000E280	FULL	Interrupt Clear-Pending Register
CM0P_IPR0	0xE000E400	FULL	Interrupt Priority Registers
CM0P_IPR1	0xE000E404	FULL	Interrupt Priority Registers
CM0P_IPR2	0xE000E408	FULL	Interrupt Priority Registers
CM0P_IPR3	0xE000E40C	FULL	Interrupt Priority Registers
CM0P_IPR4	0xE000E410	FULL	Interrupt Priority Registers
CM0P_IPR5	0xE000E414	FULL	Interrupt Priority Registers
CM0P_IPR6	0xE000E418	FULL	Interrupt Priority Registers
CM0P_IPR7	0xE000E41C	FULL	Interrupt Priority Registers
CM0P_CPUID	0xE000ED00	FULL	CPUID Register
CM0P_ICSR	0xE000ED04	FULL	Interrupt Control State Register
CM0P_VTOR	0xE000ED08	FULL	Vector Table Offset Register
CM0P_AIRCR	0xE000ED0C	FULL	Application Interrupt and Reset Control Register
CM0P_SCR	0xE000ED10	FULL	System Control Register
CM0P_CCR	0xE000ED14	FULL	Configuration and Control Register
CM0P_SHPR2	0xE000ED1C	FULL	System Handler Priority Register 2
CM0P_SHPR3	0xE000ED20	FULL	System Handler Priority Register 3
CM0P_SHCSR	0xE000ED24	FULL	System Handler Control and State Register
CM0P_DFSR	0xE000ED30	FULL	Debug Fault Status Register
CM0P_DHCSR	0xE000EDF0	FULL	Debug Halting Control and Status Register
CM0P_DCRSR	0xE000EDF4	FULL	Debug Core Register Selector Register
CM0P_DCRDR	0xE000EDF8	FULL	Debug Core Register Data Register
CM0P_DEMCR	0xE000EDFC	FULL	Debug Exception and Monitor Control Register
CM0P_SCS_PID4	0xE000EFD0	FULL	System Control Space ROM Table Peripheral ID #4
CM0P_SCS_PID0	0xE000EFE0	FULL	System Control Space ROM Table Peripheral ID #0
CM0P_SCS_PID1	0xE000EFE4	FULL	System Control Space ROM Table Peripheral ID #1
CM0P_SCS_PID2	0xE000EFE8	FULL	System Control Space ROM Table Peripheral ID #2
CM0P_SCS_PID3	0xE000EFEC	FULL	System Control Space ROM Table Peripheral ID #3
CM0P_SCS_CID0	0xE000EFF0	FULL	System Control Space ROM Table Component ID #0
CM0P_SCS_CID1	0xE000EFF4	FULL	System Control Space ROM Table Component ID #1
CM0P_SCS_CID2	0xE000EFF8	FULL	System Control Space ROM Table Component ID #2
CM0P_SCS_CID3	0xE000EFFC	FULL	System Control Space ROM Table Component ID #3
CM0P_ROM_SCS	0xE00FF000	FULL	CM0+ CoreSight ROM Table Peripheral #0
CM0P_ROM_DWT	0xE00FF004	FULL	CM0+ CoreSight ROM Table Peripheral #1
CM0P_ROM_BPU	0xE00FF008	FULL	CM0+ CoreSight ROM Table Peripheral #2
CM0P_ROM_END	0xE00FF00C	FULL	CM0+ CoreSight ROM Table End Marker
CM0P_ROM_CSMT	0xE00FFFCC	FULL	CM0+ CoreSight ROM Table Memory Type
CM0P_ROM_PID4	0xE00FFFD0	FULL	CM0+ CoreSight ROM Table Peripheral ID #4
CM0P_ROM_PID0	0xE00FFFE0	FULL	CM0+ CoreSight ROM Table Peripheral ID #0
CM0P_ROM_PID1	0xE00FFFE4	FULL	CM0+ CoreSight ROM Table Peripheral ID #1
CM0P_ROM_PID2	0xE00FFFE8	FULL	CM0+ CoreSight ROM Table Peripheral ID #2
CM0P_ROM_PID3	0xE00FFFEC	FULL	CM0+ CoreSight ROM Table Peripheral ID #3
CM0P_ROM_CID0	0xE00FFFF0	FULL	CM0+ CoreSight ROM Table Component ID #0
CM0P_ROM_CID1	0xE00FFFF4	FULL	CM0+ CoreSight ROM Table Component ID #1
CM0P_ROM_CID2	0xE00FFFF8	FULL	CM0+ CoreSight ROM Table Component ID #2
CM0P_ROM_CID3	0xE00FFFFC	FULL	CM0+ CoreSight ROM Table Component ID #3

1.1 Register Details

1.1.1 CM0P_DWT_CTRL

Description: Watchpoint Comparator Configuration
Address: 0xE0001000
Offset: 0x1000
Retention: Retained
IsDeepSleep: No
Comment: Defines the number of comparators implemented
Default: 0x20000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	NUMCOMP [31:28]				None [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
28:31	NUMCOMP	R		2	Number of comparators available

1.1.2 CM0P_DWT_PCSR

Description: Watchpoint Comparator PC Sample
Address: 0xE000101C
Offset: 0x101C
Retention: Retained
IsDeepSleep: No
Comment: Samples the current value of the program counter. Unless DWT_PCSR reads as 0xFFFFFFFF, under the conditions described in Program counter sampling support on page C1-344, bit [0] is RAZ. When RAZ, bit [0] does not reflect instruction set state as is the case with similar functionality in other ARM architecture profiles.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	EIASAMPLE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	EIASAMPLE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	EIASAMPLE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	EIASAMPLE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	EIASAMPLE	R	W	X	Executed Instruction Address sample value

1.1.3 CM0P_DWT_COMP0

Description: Watchpoint Comparator Compare Value
Address: 0xE0001020
Offset: 0x1020
Retention: Retained
IsDeepSleep: No
Comment: Provides a reference value for use by comparator
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	COMP [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	COMP [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	COMP [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	COMP [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	COMP	RW	R	X	Reference value for comparison.

1.1.4 CM0P_DWT_MASK0

Description: Watchpoint Comparator Mask
Address: 0xE0001024
Offset: 0x1024
Retention: Retained
IsDeepSleep: No
Comment: Provides the size of the ignore mask applied to the access address range matching
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	MASK [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	MASK	RW	R	X	The size of the ignore mask applied to address range matching. The mask range is IMPLEMENTATION DEFINED. Writing all ones to this field and reading it back can be used to determine the maximum mask size supported.

1.1.5 CM0P_DWT_FUNCTION0

Description: Watchpoint Comparator Function
Address: 0xE0001028
Offset: 0x1028
Retention: Retained
IsDeepSleep: No
Comment: Controls the operation of the comparator
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				FUNCTION [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:25]							MATCHED [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	FUNCTION	RW	R	0	Select action on comparator match.
	DISABLE			0	Disabled
	IADDR			4	PC watchpoint event
	DADDR_RO			5	Watchpoint event
	DADDR_WO			6	Watchpoint event
	DADDR_RW			7	Watchpoint event
24	MATCHED	R	RW	0	Comparator match. It indicates that the operation defined by FUNCTION has occurred since the bit was last read: 0 the associated comparator has matched. 1 the associated comparator has not matched. Reading the register clears this bit to 0.

1.1.6 CM0P_DWT_COMP1

Description: Watchpoint Comparator Compare Value
Address: 0xE0001030
Offset: 0x1030
Retention: Retained
IsDeepSleep: No
Comment: Provides a reference value for use by comparator
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	COMP [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	COMP [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	COMP [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	COMP [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	COMP	RW	R	X	Reference value for comparison.

1.1.7 CM0P_DWT_MASK1

Description: Watchpoint Comparator Mask
Address: 0xE0001034
Offset: 0x1034
Retention: Retained
IsDeepSleep: No
Comment: Provides the size of the ignore mask applied to the access address range matching
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	MASK [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	MASK	RW	R	X	The size of the ignore mask applied to address range matching. The mask range is IMPLEMENTATION DEFINED. Writing all ones to this field and reading it back can be used to determine the maximum mask size supported.

1.1.8 CM0P_DWT_FUNCTION1

Description: Watchpoint Comparator Function
Address: 0xE0001038
Offset: 0x1038
Retention: Retained
IsDeepSleep: No
Comment: Controls the operation of the comparator
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				FUNCTION [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:25]							MATCHED [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	FUNCTION	RW	R	0	Select action on comparator match.
	DISABLE			0	Disabled
	IADDR			4	PC watchpoint event
	DADDR_RO			5	Watchpoint event
	DADDR_WO			6	Watchpoint event
	DADDR_RW			7	Watchpoint event
24	MATCHED	R	RW	0	Comparator match. It indicates that the operation defined by FUNCTION has occurred since the bit was last read: 0 the associated comparator has matched. 1 the associated comparator has not matched. Reading the register clears this bit to 0.

1.1.9 CM0P_DWT_PID4

Description: Watchpoint Unit CoreSight ROM Table Peripheral ID #4
Address: 0xE0001FD0
Offset: 0x1FD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		4	Peripheral ID #4

1.1.10 CM0P_DWT_PID0

Description: Watchpoint Unit CoreSight ROM Table Peripheral ID #0
Address: 0xE0001FE0
Offset: 0x1FE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xA

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		10	Peripheral ID #0

1.1.11 CM0P_DWT_PID1

Description: Watchpoint Unit CoreSight ROM Table Peripheral ID #1
Address: 0xE0001FE4
Offset: 0x1FE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		176	Peripheral ID #1

1.1.12 CM0P_DWT_PID2

Description: Watchpoint Unit CoreSight ROM Table Peripheral ID #2
Address: 0xE0001FE8
Offset: 0x1FE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		11	Peripheral ID #2

1.1.13 CM0P_DWT_PID3

Description: Watchpoint Unit CoreSight ROM Table Peripheral ID #3
Address: 0xE0001FEC
Offset: 0x1FEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		0	Peripheral ID #3

1.1.14 CM0P_DWT_CID0

Description: Watchpoint Unit CoreSight ROM Table Component ID #0
Address: 0xE0001FF0
Offset: 0x1FF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		13	Component ID #0

1.1.15 CM0P_DWT_CID1

Description: Watchpoint Unit CoreSight ROM Table Component ID #1
Address: 0xE0001FF4
Offset: 0x1FF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xE0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		224	Component ID #1

1.1.16 CM0P_DWT_CID2

Description: Watchpoint Unit CoreSight ROM Table Component ID #2
Address: 0xE0001FF8
Offset: 0x1FF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		5	Component ID #2

1.1.17 CM0P_DWT_CID3

Description: Watchpoint Unit CoreSight ROM Table Component ID #3
Address: 0xE0001FFC
Offset: 0x1FFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		177	Component ID #3

1.1.18 CM0P_BP_CTRL

Description: Breakpoint Unit Control
Address: 0xE0002000
Offset: 0x2000
Retention: Retained
IsDeepSleep: No
Comment: Provides BPU implementation information, and the global enable for the BPU.
Default: 0x40

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	NUM_CODE [7:4]				None [3:2]		KEY [1:1]	ENABLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ENABLE	RW	R	0	Enables the BPU: 0 BPU is disabled. 1 BPU is enabled.
1	KEY	RW	R	0	RAZ on reads, SBO for writes. If written as zero, the write to the register is ignored.
4:7	NUM_CODE	R		4	The number of breakpoint comparators. If NUM_CODE is zero, the implementation does not support any comparators.

1.1.19 CM0P_BP_COMP0

Description: Breakpoint Compare Register
Address: 0xE0002008
Offset: 0x2008
Retention: Retained
IsDeepSleep: No
Comment: Holds a breakpoint address for comparison with instruction addresses in the Code memory region, see The system address map on page B3-258 for more information.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	COMP_ADDR [7:2]						None [1:1]	ENABLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	COMP_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	COMP_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	MATCH [31:30]		None [29:29]	COMP_ADDR [28:24]				

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ENABLE	RW	R	0	Enables the comparator: Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator.
2:28	COMP_ADDR	RW	R	X	Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero.
30:31	MATCH	RW	R	X	BP_MATCH defines the behavior when the COMP address is matched.
	NONE			0	No breakpoint matching
	LOWER			1	Breakpoint on lower halfword, upper is unaffected.
	UPPER			2	Breakpoint on upper halfword, lower is unaffected.
	BOTH			3	Breakpoint on both lower and upper halfwords.

1.1.20 CM0P_BP_COMP1

Description: Breakpoint Compare Register
Address: 0xE000200C
Offset: 0x200C
Retention: Retained
IsDeepSleep: No
Comment: Holds a breakpoint address for comparison with instruction addresses in the Code memory region, see The system address map on page B3-258 for more information.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	COMP_ADDR [7:2]						None [1:1]	ENABLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	COMP_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	COMP_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	MATCH [31:30]		None [29:29]	COMP_ADDR [28:24]				

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ENABLE	RW	R	0	Enables the comparator: Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator.
2:28	COMP_ADDR	RW	R	X	Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero.
30:31	MATCH	RW	R	X	BP_MATCH defines the behavior when the COMP address is matched.
	NONE			0	No breakpoint matching
	LOWER			1	Breakpoint on lower halfword, upper is unaffected.
	UPPER			2	Breakpoint on upper halfword, lower is unaffected.
	BOTH			3	Breakpoint on both lower and upper halfwords.

1.1.21 CM0P_BP_COMP2

Description: Breakpoint Compare Register
Address: 0xE0002010
Offset: 0x2010
Retention: Retained
IsDeepSleep: No
Comment: Holds a breakpoint address for comparison with instruction addresses in the Code memory region, see The system address map on page B3-258 for more information.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	COMP_ADDR [7:2]						None [1:1]	ENABLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	COMP_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	COMP_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	MATCH [31:30]		None [29:29]	COMP_ADDR [28:24]				

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ENABLE	RW	R	0	Enables the comparator: Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator.
2:28	COMP_ADDR	RW	R	X	Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero.
30:31	MATCH	RW	R	X	BP_MATCH defines the behavior when the COMP address is matched.
	NONE			0	No breakpoint matching
	LOWER			1	Breakpoint on lower halfword, upper is unaffected.
	UPPER			2	Breakpoint on upper halfword, lower is unaffected.
	BOTH			3	Breakpoint on both lower and upper halfwords.

1.1.22 CM0P_BP_COMP3

Description: Breakpoint Compare Register
Address: 0xE0002014
Offset: 0x2014
Retention: Retained
IsDeepSleep: No
Comment: Holds a breakpoint address for comparison with instruction addresses in the Code memory region, see The system address map on page B3-258 for more information.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	COMP_ADDR [7:2]						None [1:1]	ENABLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	COMP_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	COMP_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	MATCH [31:30]		None [29:29]	COMP_ADDR [28:24]				

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ENABLE	RW	R	0	Enables the comparator. Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator.
2:28	COMP_ADDR	RW	R	X	Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero.
30:31	MATCH	RW	R	X	BP_MATCH defines the behavior when the COMP address is matched.
	NONE			0	No breakpoint matching
	LOWER			1	Breakpoint on lower halfword, upper is unaffected.
	UPPER			2	Breakpoint on upper halfword, lower is unaffected.
	BOTH			3	Breakpoint on both lower and upper halfwords.

1.1.23 CM0P_BP_PID4

Description: Breakpoint Unit CoreSight ROM Table Peripheral ID #4
Address: 0xE0002FD0
Offset: 0x2FD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		4	Peripheral ID #4

1.1.24 CM0P_BP_PID0

Description: Breakpoint Unit CoreSight ROM Table Peripheral ID #0
Address: 0xE0002FE0
Offset: 0x2FE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		11	Peripheral ID #0

1.1.25 CM0P_BP_PID1

Description: Breakpoint Unit CoreSight ROM Table Peripheral ID #1
Address: 0xE0002FE4
Offset: 0x2FE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		176	Peripheral ID #1

1.1.26 CM0P_BP_PID2

Description: Breakpoint Unit CoreSight ROM Table Peripheral ID #2
Address: 0xE0002FE8
Offset: 0x2FE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		11	Peripheral ID #2

1.1.27 CM0P_BP_PID3

Description: Breakpoint Unit CoreSight ROM Table Peripheral ID #3
Address: 0xE0002FEC
Offset: 0x2FEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		0	Peripheral ID #3

1.1.28 CM0P_BP_CID0

Description: Breakpoint Unit CoreSight ROM Table Component ID #0
Address: 0xE0002FF0
Offset: 0x2FF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		13	Component ID #0

1.1.29 CM0P_BP_CID1

Description: Breakpoint Unit CoreSight ROM Table Component ID #1
Address: 0xE0002FF4
Offset: 0x2FF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xE0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		224	Component ID #1

1.1.30 CM0P_BP_CID2

Description: Breakpoint Unit CoreSight ROM Table Component ID #2
Address: 0xE0002FF8
Offset: 0x2FF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		5	Component ID #2

1.1.31 CM0P_BP_CID3

Description: Breakpoint Unit CoreSight ROM Table Component ID #3
Address: 0xE0002FFC
Offset: 0x2FFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		177	Component ID #3

1.1.32 CM0P_ACTLR

Description: Auxiliary Control Register
Address: 0xE000E008
Offset: 0xE008
Retention: Retained
IsDeepSleep: No
Comment: Provides configuration and control options.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ACTRL [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ACTRL [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ACTRL [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ACTRL [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ACTRL	R		0	Always 0 for CM0+ r0p1

1.1.33 CM0P_SYST_CSR

Description: SysTick Control & Status
Address: 0xE000E010
Offset: 0xE010
Retention: Retained
IsDeepSleep: No
Comment: Controls the SysTick counter and provides status data. The SysTick counter is functional in the Active and Sleep power modes (and not functional in the DeepSleep, Hibernate and Stop power modes).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					CLKSOURCE [2:2]	TICKINT [1:1]	ENABLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:17]							COUNTFLAG [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ENABLE	RW	R	0	Indicates the enabled status of the SysTick counter: '0': counter is disabled. '1': counter is operating.
1	TICKINT	RW	R	0	Indicates whether counting to '0' causes the status of the SysTick exception to change to pending: '0': count to '0' does not affect the SysTick exception status. '1': count to '0' changes the SysTick exception status to pending. Changing the value of the counter to '0' by writing zero to the SYST_CVR register to '0' never changes the status of the SysTick exception.
2	CLKSOURCE	RW	R	0	Indicates the SysTick counter clock source: '0': SysTick uses the low frequency clock 'clk_lf'. For this mode to function, 'clk_lf' should be less than half the frequency of 'clk_sys'. Note that 'clk_lf' is generated by a low accuracy ILO (Internal Low power Oscillator), with a target frequency of 32.768 kHz (frequency can be as low as 15 kHz and as high as 60 kHz). '1': SysTick uses the system/processor clock 'clk_sys'. If SysTick counter functionality is not present in the device. This field should be set to '1', such that SysTick uses the system clock 'clk_sys'.

Bits	Name	SW	HW	Default or Enum	Description
16	COUNTFLAG	R	RW	0	Indicates whether the counter has counted to '0' since the last read of this register: '0': counter has not counted to '0'. '1': counter has counted to '0'. COUNTFLAG is set to '1' by a count transition from '1' to '0'. COUNTFLAG is cleared to '0' by a read of this register, and by any write to the SYST_CVR register.

1.1.34 CM0P_SYST_RVR

Description: SysTick Reload Value
Address: 0xE000E014
Offset: 0xE014
Retention: Retained
IsDeepSleep: No
Comment: Sets or reads the reload value of the SYST_CVR register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RELOAD [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RELOAD [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	RELOAD [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:23	RELOAD	RW	R	X	The value to load into the SYST_CVR register when the counter reaches 0.

1.1.35 CM0P_SYST_CVR

Description: SysTick Current Value
Address: 0xE000E018
Offset: 0xE018
Retention: Retained
IsDeepSleep: No
Comment: Reads or clears the current counter value. Any write to the register clears the register to 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CURRENT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CURRENT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	CURRENT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:23	CURRENT	RW	R	X	Current counter value. This is the value of the counter at the time it is sampled.

1.1.36 CM0P_SYST_CALIB

Description: SysTick Calibration Value
Address: 0xE000E01C
Offset: 0xE01C
Retention: Retained
IsDeepSleep: No
Comment: Reads the calibration value and parameters for SysTick.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	TENMS [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	TENMS [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	TENMS [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	NOREF [31:31]	SKEW [30:30]	None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:23	TENMS	R	RW	X	Optionally, holds a reload value to be used for 10ms (100Hz) timing, subject to system clock skew errors. If this field is '0', the calibration value is not known. In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is 0x00:00147. In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is 0x00:0000.
30	SKEW	R	RW	X	Indicates whether the 10ms calibration value is exact: '0': 10ms calibration value is exact. '1': 10ms calibration value is inexact, because of the clock frequency. In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is '1' (due to the low accuracy ILO). In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is '0'.
31	NOREF	R		0	Indicates whether a implementation defined reference clock is provided: '0': the reference clock is provided. '1': the reference clock is not provided. When this bit is '1', the SYST_CSR.CLKSOURCEis forced to '1' and cannot be cleared to '0'. In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is '0'. In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is '1'.

1.1.37 CM0P_ISER

Description: Interrupt Set-Enable Register
Address: 0xE000E100
Offset: 0xE100
Retention: Retained
IsDeepSleep: No
Comment: Enables, or reads the enabled state of one or more interrupts.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SETENA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SETENA [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	SETENA [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	SETENA [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	SETENA	RW1S	R	0	Enables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt.

1.1.38 CM0P_ICER

Description: Interrupt Clear Enable Register
Address: 0xE000E180
Offset: 0xE180
Retention: Retained
IsDeepSleep: No
Comment: Disables, or reads the enabled state of one or more interrupts
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CLRENA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CLRENA [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	CLRENA [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	CLRENA [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	CLRENA	RW1C	R	0	Disables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt.

1.1.39 CM0P_ISPR

Description: Interrupt Set-Pending Register
Address: 0xE000E200
Offset: 0xE200
Retention: Retained
IsDeepSleep: No
Comment: On writes, sets the status of one or more interrupts to pending. On reads, shows the pending status of the interrupts.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SETPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SETPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	SETPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	SETPEND [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	SETPEND	RW1S	R	0	Changes the state of one or more interrupts to pending. Each bit corresponds to the same numbered interrupt.

1.1.40 CM0P_ICPR

Description: Interrupt Clear-Pending Register
Address: 0xE000E280
Offset: 0xE280
Retention: Retained
IsDeepSleep: No
Comment: On writes, clears the status of one or more interrupts to pending. On reads, shows the pending status of the interrupts.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CLRPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CLRPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	CLRPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	CLRPEND [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	CLRPEND	RW1C	R	0	Changes the state of one or more interrupts to not pending. Each bit corresponds to the same numbered interrupt.

1.1.41 CM0P_IPR

Description: Interrupt Priority Registers
Address: 0xE000E400
Offset: 0xE400
Retention: Retained
IsDeepSleep: No
Comment: Sets or reads interrupt priorities. Register n contains priorities for interrupts N=4n .. 4n+3
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
Name	PRI_N3 [31:30]		None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
6:7	PRI_N0	RW	R	0	Priority of interrupt number N.
14:15	PRI_N1	RW	R	0	Priority of interrupt number N+1.
22:23	PRI_N2	RW	R	0	Priority of interrupt number N+2.
30:31	PRI_N3	RW	R	0	Priority of interrupt number N+3.

1.1.42 CM0P_CPUID

Description: CPUID Register
Address: 0xE000ED00
Offset: 0xED00
Retention: Retained
IsDeepSleep: No
Comment: Contains the part number, version, and implementation information that is specific to this processor.
Default: 0x410CC601

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PARTNO [7:4]				REVISION [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	PARTNO [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VARIANT [23:20]				CONSTANT [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	IMPLEMENTER [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	REVISION	R		1	Indicates revision. In ARM implementations this is the minor revision number n in the pn part of the rnpn revision status, see Product revision status on page xii. For release r0p1.
4:15	PARTNO	R		3168	Indicates part number, Cortex-M0+
16:19	CONSTANT	R		12	Indicates the architecture, ARMv6-M
20:23	VARIANT	R		0	Implementation defined. In ARM implementations this is the major revision number n in the rn part of the rnpn revision status, Product revision status on page xii.
24:31	IMPLEMENTER	R		65	Implementer code for ARM.

1.1.43 CM0P_ICSR

Description: Interrupt Control State Register
Address: 0xE000ED04
Offset: 0xED04
Retention: Retained
IsDeepSleep: No
Comment: Controls and provides status information for the ARMv6-M.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VECTACTIVE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VECTPENDING [15:12]				None [11:9]			VECTACTIVE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	ISRPREEMPT [23:23]	ISRPENDING [22:22]	None [21:21]	VECTPENDING [20:16]				

Bits	31	30	29	28	27	26	25	24
Name	NMIPENDSET [31:31]	None [30:29]		PENDSVSET [28:28]	PENDSVCLR [27:27]	PENDSTSETB [26:26]	PENDSTCLR [25:25]	None [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:8	VECTACTIVE	R	RW	0	The exception number for the current executing exception. 0= Thread mode. This is the same value as IPSR[8:0]
12:20	VECTPENDING	R	RW	0	The exception number for the highest priority pending exception. 0= No pending exceptions. The pending state includes the effect of memory-mapped enable and mask registers. It does not include the PRIMASK special-purpose register qualifier.
22	ISRPENDING	R	RW	0	Indicates if an external configurable, NVIC generated, interrupt is pending.
23	ISRPREEMPT	R	RW	0	Indicates whether a pending exception will be serviced on exit from debug halt state.
25	PENDSTCLR	RW1C	R	0	Clears a pending SysTick, whether set here or by the timer hardware.
26	PENDSTSETB	RW1S	RW	0	Sets a pending SysTick or reads back the current state. Writing PENDSTSET and PENDSTCLR to '1' concurrently is UNPREDICTABLE.
27	PENDSVCLR	RW1C	R	0	Clears a pending PendSV interrupt.
28	PENDSVSET	RW1S	RW	0	Sets a pending PendSV interrupt or reads back the current state. Use this normally to request a context switch. Writing PENDSVSET and PENDSVCLR to '1' concurrently is UNPREDICTABLE.
31	NMIPENDSET	RW1S	RW	0	Activates an NMI exception or reads back the current state. Because NMI is the highest priority exception, it activates as soon as it is registered.

1.1.44 CM0P_VTOR

Description: Vector Table Offset Register
Address: 0xE000ED08
Offset: 0xED08
Retention: Retained
IsDeepSleep: No
Comment: Holds the vector table offset address
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	TBLOFF [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	TBLOFF [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	TBLOFF [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
8:31	TBLOFF	RW	R	0	Table offset address. All bits of the Vector table address that are not defined by the VTOR are zero.

1.1.45 CM0P_AIRCR

Description: Application Interrupt and Reset Control Register
Address: 0xE000ED0C
Offset: 0xED0C
Retention: Retained
IsDeepSleep: No
Comment: Sets or returns interrupt control data.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					SYSRESETREQ [2:2]	VECTCLRACTIVE [1:1]	None [0:0]

Bits	15	14	13	12	11	10	9	8
Name	ENDIANNESS [15:15]	None [14:8]						

Bits	23	22	21	20	19	18	17	16
Name	VECTKEY [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VECTKEY [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
1	VECTCLRACTIVE	RW1C	R	0	Clears all active state information for fixed and configurable exceptions. The effect of writing a 1 to this bit if the processor is not halted in Debug state is UNPREDICTABLE.
2	SYSRESETREQ	RW1S	R	0	System Reset Request. Writing 1 to this bit asserts a signal to request a reset by the external system. This will cause a full system reset of the CPU and all other components in the device. See Reset management on page B1-240 for more information.
15	ENDIANNESS	R		0	Indicates the memory system data endianness: 0 little endian 1 big endian. See Endian support on page A3-44 for more information.
16:31	VECTKEY	RW	R	X	Vector Key. The value 0x05FA must be written to this register, otherwise the register write is UNPREDICTABLE. Readback value is UNKNOWN.

1.1.46 CM0P_SCR

Description: System Control Register
Address: 0xE000ED10
Offset: 0xED10
Retention: Retained
IsDeepSleep: No
Comment: Sets or returns system control data.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			SEVONPEND [4:4]	None [3:3]	SLEEPDEEP [2:2]	SLEEPONEXIT [1:1]	None [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
1	SLEEPONEXIT	RW	R	0	Determines whether, on an exit from an ISR that returns to the base level of execution priority, the processor enters a sleep state: 0 do not enter sleep state. 1 enter sleep state. See Power management on page B1-240 for more information.
2	SLEEPDEEP	RW	R	0	An implementation can use this bit to select DeepSleep/Hibernate power modes upon execution of WFI/WFE: 0: Select Sleep mode 1: Select DeepSleep/Hibernate (depends on PWR_CONTROL.HIBERNATE)
4	SEVONPEND	RW	R	0	Determines whether an interrupt transition from inactive state to pending state is a wakeup event: 0: transitions from inactive to pending are not wakeup events. 1: transitions from inactive to pending are wakeup events. See WFE on page A6-197 for more information.

1.1.47 CM0P_CCR

Description: Configuration and Control Register
Address: 0xE000ED14
Offset: 0xED14
Retention: Retained
IsDeepSleep: No
Comment: Returns configuration and control data.
Default: 0x208

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				UNALIGN_TRP [3:3]	None [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						STKALIGN [9:9]	None [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
3	UNALIGN_TRP	R		1	1: unaligned word and halfword accesses generate a HardFault exception.
9	STKALIGN	R		1	1: On exception entry, the SP used prior to the exception is adjusted to be 8-byte aligned and the context to restore it is saved. The SP is restored on the associated exception return.

1.1.48 CM0P_SHPR2

Description: System Handler Priority Register 2
Address: 0xE000ED1C
Offset: 0xED1C
Retention: Retained
IsDeepSleep: No
Comment: Sets or returns priority for system handler 11
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	PRI_11 [31:30]		None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
30:31	PRI_11	RW	R	0	Priority of system handler 11, SVCall

1.1.49 CM0P_SHPR3

Description: System Handler Priority Register 3
Address: 0xE000ED20
Offset: 0xED20
Retention: Retained
IsDeepSleep: No
Comment: Sets or returns priority for system handlers 14-15.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	PRI_14 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
Name	PRI_15 [31:30]		None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
22:23	PRI_14	RW	R	0	Priority of system handler 14, PendSV
30:31	PRI_15	RW	R	0	Priority of system handler 15, SysTick

1.1.50 CM0P_SHCSR

Description: System Handler Control and State Register
Address: 0xE000ED24
Offset: 0xED24
Retention: Retained
IsDeepSleep: No
Comment: Controls and provides the status of system handlers.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SVCALLPENDED [15:15]	None [14:8]						

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
15	SVCALLPENDED	RW	RW	0	0 SVCall is not pending. 1 SVCall is pending. This bit reflects the pending state on a read, and updates the pending state, to the value written, on a write. (Pending state bits are set to 1 when an exception occurs, and are cleared to 0 when an exception becomes active.)

1.1.51 CM0P_DFSR

Description: Debug Fault Status Register
Address: 0xE000ED30
Offset: 0xED30
Retention: Retained
IsDeepSleep: No
Comment: Provides the top level reason why a debug event has occurred. Writing 1 to a register bit clears that bit to 0. A read of the HALTED bit by an instruction executed by stepping returns an UNKNOWN value, For more information see Debug stepping on page C1-325.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			EXTERNAL [4:4]	VCATCH [3:3]	DWTTRAP [2:2]	BKPT [1:1]	HALTED [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	HALTED	RW1C	RW1S	0	Indicates a debug event generated by a C_HALT or C_STEP request, triggered by a write to the DHCSR: 0 no active halt request debug event. 1 halt request debug event active. See Debug Halting Control and Status Register, DHCSR for more information.
1	BKPT	RW1C	RW1S	0	Indicates a debug event generated by BKPT instruction execution or a breakpoint match in the BPU: 0 no breakpoint debug event. 1 at least one breakpoint debug event.
2	DWTTRAP	RW1C	RW1S	0	Indicates a debug event generated by the DWT: 0 no debug events generated by the DWT. 1 at least one debug event generated by the DWT.
3	VCATCH	RW1C	RW1S	0	Indicates whether a vector catch debug event was generated: 0 no vector catch debug event generated. 1 vector catch debug event generated. The corresponding FSR shows the primary cause of the exception.
4	EXTERNAL	RW1C	RW1S	0	Indicates an asynchronous debug event generated because of EDBGRQ being asserted: 0 no EDBGRQ debug event. 1 EDBGRQ debug event.

1.1.52 CM0P_DHCSR

Description: Debug Halting Control and Status Register
Address: 0xE000EDF0
Offset: 0xEDF0
Retention: Retained
IsDeepSleep: No
Comment: Controls halting debug. When C_DEBUGEN is set to 1, C_STEP and C_MASKINTS must not be
modified when the processor is running. Note: S_HALT is 0 when the processor is running. When C_DEBUGEN is set to 0, the processor ignores the values of all other bits in this register. For more information on the use of DHCSR, see Debug stepping on page C1-325. Note: any write to this register must have [31:16]=0xA05F - if not, the write is ignored.
Default: 0x2000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				C_MASKINTS [3:3]	C_STEP [2:2]	C_HALT [1:1]	C_DEBUGEN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	DBG_KEY_P1 [23:20]				S_LOCKUP [19:19]	S_SLEEP [18:18]	S_HALT [17:17]	S_REGRDY [16:16]

Bits	31	30	29	28	27	26	25	24
Name	DBG_KEY_P2 [31:26]						S_RESET_ST [25:25]	S_RETIRE_ST [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	C_DEBUGEN	RW	R	0	Halting debug enable bit. If a debugger writes to DHCSR to change the value of this bit from 0 to 1, it must also write 0 to the C_MASKINTS bit, otherwise behavior is UNPREDICTABLE. This bit can only be written from the DAP. Access to the DHCSR from software running on the processor is IMPLEMENTATION DEFINED. However, writes to this bit from software running on the processor are ignored.
1	C_HALT	RW	R	X	Processor halt bit. The effects of writes to this bit are: 0 Request a halted processor to run. 1 Request a running processor to halt. Table C1-7 on page C1-326 shows the effect of writes to this bit when the processor is in Debug state.
2	C_STEP	RW	R	X	Processor step bit. The effects of writes to this bit are: 0 Single-stepping disabled. 1 Single-stepping enabled. For more information about the use of this bit see Table C1-7 on page C1-326.

Bits	Name	SW	HW	Default or Enum	Description
3	C_MASKINTS	RW	R	X	When debug is enabled, the debugger can write to this bit to mask PendSV, SysTick and external configurable interrupts. The effect of any attempt to change the value of this bit is UNPREDICTABLE unless both: - before the write to DHCSR, the value of the C_HALT bit is 1 - the write to the DHCSR that changes the C_MASKINTS bit also writes 1 to the C_HALT bit This means that a single write to DHCSR cannot set the C_HALT to 0 and change the value of the C_MASKINTS bit. The bit does not affect NMI. When DHCSR.C_DEBUGEN is set to 0, the value of this bit is UNKNOWN. For more information about the use of this bit see Table C1-7 on page C1-326.
16	S_REGRDY	R	RW	X	A handshake flag for transfers through the DCRDR: - Writing to DCRSR clears the bit to 0. - Completion of the DCRDR transfer then sets the bit to 1. For more information about DCRDR transfers see Debug Core Register Data Register, DCRDR on page C1-337. 0: There has been a write to the DCRDR, but the transfer is not complete. 1: The transfer to or from the DCRDR is complete. This bit is only valid when the processor is in Debug state, otherwise the bit is UNKNOWN.
17	S_HALT	R	RW	0	Indicates whether the processor is in Debug state.
18	S_SLEEP	R	RW	0	Indicates whether the processor is sleeping. The debugger must set the DHCSR.C_HALT bit to 1 to gain control, or wait for an interrupt or other wakeup event to wakeup the system.
19	S_LOCKUP	R	RW	0	Indicates whether the processor is locked up because of an unrecoverable exception. See Unrecoverable exception cases on page B1-238 for more information. This bit can only read as 1 when accessed by a remote debugger using the DAP. The bit clears to 0 when the processor enters Debug state.
20:23	DBG_KEY_P1	W	R	X	Debug key: Software must write 0xA05F to [31:16] to enable write accesses to bits [15:0], otherwise the processor ignores the write access.
24	S_RETIRE_ST	R	RW	X	When not in Debug state, indicates whether the processor has completed execution of at least one instruction since the last read of DHCSR. This is a sticky bit, that clears to 0 on a read of DHCSR. This bit is UNKNOWN: - after a Local reset, but is set to 1 as soon as the processor completes execution of an instruction - when S_LOCKUP is set to 1 - when S_HALT is set to 1. When the processor is not in Debug state, a debugger can check this bit to determine if the processor is stalled on a load, store or fetch access.
25	S_RESET_ST	R	RW	1	Indicates whether the processor has been reset since the last read of DHCSR. This is a sticky bit, that clears to 0 on a read of DHCSR
26:31	DBG_KEY_P2	W	R	X	See description for Bit 20

1.1.53 CM0P_DCRSR

Description: Debug Core Register Selector Register
Address: 0xE000EDF4
Offset: 0xEDF4
Retention: Retained
IsDeepSleep: No
Comment: With the DCRDR, see Debug Core Register Data Register, DCRDR on page C1-337, the DCRSR provides debug access to the ARM core registers and special-purpose registers. A write to DCRSR specifies the register to transfer, whether the transfer is a read or a write, and starts the transfer. This register is only accessible in Debug state. When the processor is in Debug state, the debugger must preserve the Exception number bits in the IPSR, otherwise behavior is UNPREDICTABLE
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			REGSEL [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:17]							REGWNR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	REGSEL	RW	R	X	Specifies the ARM core register or special-purpose register to transfer.
	R0			0	CPU R0
	R1			1	CPU R1
	R2			2	CPU R2
	R3			3	CPU R3
	R4			4	CPU R4
	R5			5	CPU R5
	R6			6	CPU R6
	R7			7	CPU R7
	R8			8	CPU R8
	R9			9	CPU R9
	R10			10	CPU R10
	R11			11	CPU R11
	R12			12	CPU R12
	SP			13	Current Stack Pointer
	LR			14	CPU LR
	DBG_RA			15	DebugReturnAddress: the address of the first instruction to be executed on exit from Debug state.
	XPSR			16	xPSR
	MSP			17	Main stack pointer, MSP.
	PSP			18	Process stack pointer, PSP
	C_P			20	[31:24]: CONTROL [7:0]: PRIMASK.
16	REGWNR	RW	R	X	Specifies the type of access for the transfer.
	READ			0	Read transfer

Bits	Name	SW	HW	Default or Enum	Description
	WRITE			1	Write transfer

1.1.54 CM0P_DCRDR

Description: Debug Core Register Data Register
Address: 0xE000EDF8
Offset: 0xEDF8
Retention: Retained
IsDeepSleep: No
Comment: With the DCRSR, see Debug Core Register Selector Register, DCRSR on page C1-335, the DCRDR provides debug access to the ARM core registers and special-purpose registers. The DCRDR is the data register for these accesses.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DBGTMP [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DBGTMP [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	DBGTMP [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	DBGTMP [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	DBGTMP	RW	RW	X	Data temporary cache, for reading and writing CPU registers. This register is UNKNOWN: - on reset - when DHCSR.S_HALT = 0. - when DHCSR.S_REGRDY = 0 during execution of a DCRSR based transaction that updates the register

1.1.55 CM0P_DEMCR

Description: Debug Exception and Monitor Control Register
Address: 0xE000EDFC
Offset: 0xEDFC
Retention: Retained
IsDeepSleep: No
Comment: Manages vector catch behavior and enables the DWT.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							VC_CORERESET [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:11]					VC_HARDERR [10:10]	None [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:25]							DWTENA [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	VC_CORERESET	RW	R	0	Enable Reset Vector Catch. This causes a Local reset to halt a running system. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit.
10	VC_HARDERR	RW	R	0	Enable halting debug trap on a HardFault exception. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit.
24	DWTENA	RW	R	0	Global enable for all features configured and controlled by the DWT unit. When DWTENA is set to 0 DWT registers return UNKNOWN values on reads. In addition, it is IMPLEMENTATION DEFINED whether the processor ignores writes to the DWT while DWTENA is 0.

1.1.56 CM0P_SCS_PID4

Description: System Control Space ROM Table Peripheral ID #4
Address: 0xE000EFD0
Offset: 0xEFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		4	Peripheral ID #4

1.1.57 CM0P_SCS_PID0

Description: System Control Space ROM Table Peripheral ID #0
Address: 0xE000EFE0
Offset: 0xEFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x8

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		8	Peripheral ID #0

1.1.58 CM0P_SCS_PID1

Description: System Control Space ROM Table Peripheral ID #1
Address: 0xE000EFE4
Offset: 0xEFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		176	Peripheral ID #1

1.1.59 CM0P_SCS_PID2

Description: System Control Space ROM Table Peripheral ID #2
Address: 0xE000EFE8
Offset: 0xEFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		11	Peripheral ID #2

1.1.60 CM0P_SCS_PID3

Description: System Control Space ROM Table Peripheral ID #3
Address: 0xE000EFEC
Offset: 0xEFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		0	Peripheral ID #3

1.1.61 CM0P_SCS_CID0

Description: System Control Space ROM Table Component ID #0
Address: 0xE000EFF0
Offset: 0xEFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		13	Component ID #0

1.1.62 CM0P_SCS_CID1

Description: System Control Space ROM Table Component ID #1
Address: 0xE000EFF4
Offset: 0xEFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xE0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		224	Component ID #1

1.1.63 CM0P_SCS_CID2

Description: System Control Space ROM Table Component ID #2
Address: 0xE000EFF8
Offset: 0xEFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		5	Component ID #2

1.1.64 CM0P_SCS_CID3

Description: System Control Space ROM Table Component ID #3
Address: 0xE000EFFC
Offset: 0xEFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		177	Component ID #3

1.1.65 CM0P_ROM_SCS

Description: CM0+ CoreSight ROM Table Peripheral #0
Address: 0xE00FF000
Offset: 0xFF000
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFF0F003

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		4293980163	Offset to SCS ROM Table

1.1.66 CM0P_ROM_DWT

Description: CM0+ CoreSight ROM Table Peripheral #1
Address: 0xE00FF004
Offset: 0xFF004
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFF02003

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		4293926915	Offset to DWT ROM Table

1.1.67 CM0P_ROM_BPU

Description: CM0+ CoreSight ROM Table Peripheral #2
Address: 0xE00FF008
Offset: 0xFF008
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFF03003

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		4293931011	Offset to BPU ROM Table

1.1.68 CM0P_ROM_END

Description: CM0+ CoreSight ROM Table End Marker
Address: 0xE00FF00C
Offset: 0xFF00C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		0	End marker in peripheral list

1.1.69 CM0P_ROM_CSMT

Description: CM0+ CoreSight ROM Table Memory Type
Address: 0xE00FFFCC
Offset: 0xFFFCC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		1	Memory Type

1.1.70 CM0P_ROM_PID4

Description: CM0+ CoreSight ROM Table Peripheral ID #4
Address: 0xE00FFFD0
Offset: 0xFFFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		4	Peripheral ID #4

1.1.71 CM0P_ROM_PID0

Description: CM0+ CoreSight ROM Table Peripheral ID #0
Address: 0xE00FFFE0
Offset: 0xFFFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xC0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		192	Peripheral ID #0

1.1.72 CM0P_ROM_PID1

Description: CM0+ CoreSight ROM Table Peripheral ID #1
Address: 0xE00FFFE4
Offset: 0xFFFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB4

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		180	Peripheral ID #1

1.1.73 CM0P_ROM_PID2

Description: CM0+ CoreSight ROM Table Peripheral ID #2
Address: 0xE00FFFE8
Offset: 0xFFFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		11	Peripheral ID #2

1.1.74 CM0P_ROM_PID3

Description: CM0+ CoreSight ROM Table Peripheral ID #3
Address: 0xE00FFFEC
Offset: 0xFFFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		0	Peripheral ID #3

1.1.75 CM0P_ROM_CID0

Description: CM0+ CoreSight ROM Table Component ID #0
Address: 0xE00FFFF0
Offset: 0xFFFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		13	Component ID #0

1.1.76 CM0P_ROM_CID1

Description: CM0+ CoreSight ROM Table Component ID #1
Address: 0xE00FFFF4
Offset: 0xFFFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x10

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		16	Component ID #1

1.1.77 CM0P_ROM_CID2

Description: CM0+ CoreSight ROM Table Component ID #2
Address: 0xE00FFFF8
Offset: 0xFFFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		5	Component ID #2

1.1.78 CM0P_ROM_CID3

Description: CM0+ CoreSight ROM Table Component ID #3
Address: 0xE00FFFFC
Offset: 0xFFFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R		177	Component ID #3

2 CPUSS

Description CPU Subsystem
Base Address 0x40100000
Size 0x1000
Slave Num CPUMEMSSV3_VER3

Register Name	Address	Permission	Description
CPUSS_SYSREQ	0x40100004	FULL	SYSCALL control register
CPUSS_SYSARG	0x40100008	FULL	SYSARG control register
CPUSS_FLASH_CTL	0x40100030	FULL	FLASH control register
CPUSS_ROM_CTL	0x40100034	FULL	ROM control register Note:ARB is not available for this register
CPUSS_RAM_CTL	0x40100038	FULL	RAM control register
CPUSS_DMAC_CTL	0x4010003C	FULL	DMA controller register
CPUSS_FLASHC1_CTL	0x401000A8	FULL	FLASH Control1 control register
CPUSS_FAULT_CTL	0x401000AC	FULL	Fault Control Register
CPUSS_RAM_STATUS	0x401000D0	FULL	RAM Controller 0 Status
CPUSS_BOOT_RESULT_0	0x401000E0	FULL	Boot Result Register 0
CPUSS_BOOT_RESULT_1	0x401000E4	FULL	Boot Result Register 1
CPUSS_SL_CTL0	0x40100100	FULL	Slave control register
CPUSS_SL_CTL1	0x40100104	FULL	Slave control register
CPUSS_SL_CTL2	0x40100108	FULL	Slave control register
CPUSS_RAM_ECC_STATUS0	0x40100200	FULL	RAM ECC Status 0
CPUSS_RAM_ECC_STATUS1	0x40100204	FULL	RAM ECC Status 1
CPUSS_ECC_TEST	0x40100210	FULL	ECC Test
CPUSS_FLASHC_BERR_STATUS	0x40100500	FULL	Flash Bus Error Status
CPUSS_FLASHC1_BERR_STATUS	0x40100504	FULL	Flash 1 Bus Error Status
CPUSS_FLASHC_ECC_CTL	0x40100508	FULL	Flash ECC Control
CPUSS_FLASHC1_ECC_CTL	0x4010050C	FULL	Flash 1 ECC Control

2.1 Register Details

2.1.1 CPUSS_SYSREQ

Description: SYSCALL control register
Address: 0x40100004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x30000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SYSCALL_COMMAND [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SYSCALL_COMMAND [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	SYSCALL_REQ [31:31]	HMASTER_0 [30:30]	ROM_ACCESS_EN [29:29]	PRIVILEGED [28:28]	DIS_RESET_VECT_REL [27:27]	EXTERNAL_SYS_REQ [26:26]	None [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	SYSCALL_COMMAND	RW		0	Opcode of the system call being requested.
26	EXTERNAL_SYS_REQ	RW1C	RW1S	0	External HW SYS REQ. This bit is set by HW to cause a SYSCALL to BOOTROM. This bit may only be cleared by SW. When this bit is set, the SYSCALL_COMMAND, PRIVILEDGED, HMASTER0, and SYSCALL_ARG content are invalid.
27	DIS_RESET_VECT_REL	RW	R	0	Disable Reset Vector fetch relocation: '0': CPU accesses to locations 0x0000:0000 - 0x0000:0007 are redirected to ROM. '1': CPU accesses to locations 0x0000:0000 - 0x0000:0007 are made to flash. Note that this field defaults to '0' on reset, ensuring actual reset vector fetches are always made to ROM. Note that this field does not affect DAP accesses. Flash DfT routines may set this bit to '1' to enable uninhibited read-back of programmed data in the first flash page.
28	PRIVILEGED	RW	A	1	Indicates whether the system is in privileged ('1') or user mode ('0'). Only CPU SW executing from ROM can set this field to '1' when ROM_ACCESS_EN is '1' (the CPU is executing a SystemCall NMI interrupt handler). Any other write to this field sets is to '0'. This field is used as the AHB-Lite hprot[1] signal to implement Infineon proprietary user/privileged modes. These modes are used to enable/disable access to specific MMIO registers and memory regions.

Bits	Name	SW	HW	Default or Enum	Description
29	ROM_ACCESS_EN	R	RW	1	Indicates that executing from Boot ROM is enabled. HW sets this field to '1', on reset or when the SystemCall NMI vector is fetched from Boot ROM. HW sets this field to '0', when the CPU is NOT executing from either Boot or System ROM. This bit is used for debug purposes only.
30	HMASTER_0	R	W	0	Indicates the source of the write access to the SYSREQ register. '0': CPU write access. '1': DAP write access. For a SW write to the SYSREQ register, the HW will update this field based on the value of SYSCALL_REQ. SYSCALL_REQ = 0 : the current source of write access is captured. SYSCALL_REQ = 1 : the previous value (captured when SYSCALL_REQ was 0), is retained/maintained until the next SW write to this register.
31	SYSCALL_REQ	RW	R	0	CPU/DAP writes a '1' to this field to request a SystemCall. The HMASTER_0 field indicates the source of the write access. Setting this field to '1' immediate results in a NMI. The SystemCall NMI interrupt handler sets this field to '0' after servicing the request.

2.1.2 CPUSS_SYSARG

Description: SYSARG control register
Address: 0x40100008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment: Used to make system requests to SROM code. System Requests transition from User Mode to Privileged Mode. See SAS for more details. Firmware/ATE should write CPUSS_SYSARG first and CPUSS_SYSREQ register next.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SYSCALL_ARG [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SYSCALL_ARG [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	SYSCALL_ARG [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	SYSCALL_ARG [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	SYSCALL_ARG	RW		0	Argument to System Call specified in SYSREQ. Semantics of argument depends on system call made. Typically a pointer to a parameter block.

2.1.3 CPUSS_FLASH_CTL

Description: FLASH control register
Address: 0x40100030
Offset: 0x30
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			PREF_EN [4:4]	FLASH_WS [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							FLASH_INVALIDATE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:22]		FLASH_ERR_SILENT [21:21]	FLASH_ECC_INJ_EN [20:20]	None [19:18]		ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	FLASH_WS	RW	R	0	For Flash With ECC the number of wait states (WS): WS = 3 for SYSCLK <= FMAX WS = 2 for SYSCLK <= 3/4 * FMAX WS = 1 for SYSCLK <= 1/2 * FMAX WS = 0 for SYSCLK <= 1/4 * FMAX 4-15 : Future Use - To be used, if 3 Wait State is not sufficient.
4	PREF_EN	RW	R	0	Prefetch enable: '0': disabled. This is a desirable setting when FLASH_WS is 0 or when predictable execution time is required. '1': enabled.
8	FLASH_INVALIDATE	RW	RW1C	0	1': Invalidates the content of the flash controller's buffers.
16:17	ARB	RW	R	0	Arbitration policy: 0: CPU has priority 1: DW/DMA has priority 2: Roundrobin 3: Roundrobin - sticky
20	FLASH_ECC_INJ_EN	RW	R	0	Enable error injection for FLASH main interface. When'1', the parity (ECC_CTL.PARITY[7:0]) is used for a load from the ECC_CTL.WORD_ADDR[23:0] word address.

Bits	Name	SW	HW	Default or Enum	Description
21	FLASH_ERR_SILENT	RW	R	0	Specifies bus transfer behavior for a non-recoverable error on the FLASH macro main interface (either a non-correctable ECC error, a FLASH macro main interface internal error, a FLASH macro main interface memory hole access, a M0S8 protection violation error): 0: Bus transfer has a bus error. 1: Bus transfer does NOT have a bus error; i.e. the error is 'silent' In either case, a Zero value is returned. This field is ONLY used by CPU bus transfers. Non-CPU bus transfers always have a bus transfer with a bus error, in case of a non-recoverable error.

2.1.4 CPUSS_ROM_CTL

Description: ROM control register
Address: 0x40100034
Offset: 0x34
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							ROM_WS [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ROM_WS	RW	R	0	Amount of ROM wait states: '0': 0 wait states. Use this setting for newer, faster ROM design. Use this setting for older, slower ROM design and frequencies in the range [0, 24] MHz. '1': 1 wait state. Use this setting for older, slower ROM design and frequencies in the range <24, 48] MHz. Should always be set to 0.

2.1.5 CPUSS_RAM_CTL

Description: RAM control register
Address: 0x40100038
Offset: 0x38
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	ECC_BIST_SWITCH [6:6]	None [5:5]	ECC_INJ_EN [4:4]	None [3:3]	ECC_AUTO_CORRECT [2:2]	None [1:1]	ECC_ENABLE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ECC_ENABLE	RW	R	1	Enable ECC operation: '0': ECC Disabled - ECC is not generated/checked '1': ECC Enabled - ECC is generated/checked
2	ECC_AUTO_CORRECT	RW	R	1	HW ECC autocorrect functionality: '0': Disabled. '1': Enabled. HW automatically writes back SRAM with corrected data when a recoverable ECC error is detected.
4	ECC_INJ_EN	RW	R	0	Enable error injection. 0: Syndrome is source from ECC Syndrome hardware. 1: ECC_TEST.SYND_DATA is used when a full 32-bit write is done to the ECC_TEST.WORD_ADDR word address of SRAM0.
6	ECC_BIST_SWITCH	RW	R	0	ECC_BIST_SWITCH: Substitutes Syndrome bits for normal data path during BIST testing. Data bits 31:25 on the SRAM data path both to and from the SRAM are replaced with the SRAM Syndrome data bits 38:32 during BIST testing when this bit is set to 1. '0': Source normal datapath to BIST bus '1': Source Syndrome bits to BIST bus
16:17	ARB	RW	R	0	Arbitration Policy: '0': CPU has priority '1': DW/DMA has priority '2': Roundrobin '3': Roundrobin - sticky

2.1.6 CPUSS_DMAC_CTL

Description: DMA controller register
Address: 0x4010003C
Offset: 0x3C
Retention: Retained
IsDeepSleep: No
Comment: Arbitration control for the DMA controller AHB-Lite slave interface
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
16:17	ARB	RW	R	0	Arbitration policy: 0: CPU has priority 1: DW/DMA has priority 2: Roundrobin 3: Roundrobin - sticky

2.1.7 CPUSS_FLASHC1_CTL

Description: FLASH Control1 control register
Address: 0x401000A8
Offset: 0xA8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			PREF_EN [4:4]	FLASH_WS [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							FLASH_INVALIDATE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:22]		FLASH_ERR_SILENT [21:21]	FLASH_ECC_INJ_EN [20:20]	None [19:18]		ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	FLASH_WS	RW	R	0	Amount of ROM wait states: For Flash (without ECC). 0: 0 wait states (fast flash: [0, 24] MHz system frequency, slow flash: [0, 16] MHz system frequency) 1: 1 wait state (fast flash: [24, 48] MHz system frequency, slow flash: [16, 32] MHz system frequency) 2: 2 wait states (slow flash: [32, 48] MHz system frequency) 3-15 : Future Use. For Flash With ECC. 0: 0 wait states ([0, 12] MHz system frequency) 1: 1 wait state ([12, 24] MHz system frequency) 2: 2 wait states (24,36] MHz system frequency) 3: 3 wait states ([36,48] MHz System Frequency) 4-15 : Future Use - To be used, if 3 Wait State is not sufficient.
4	PREF_EN	RW	R	0	Prefetch enable: '0': disabled. This is a desirable setting when FLASH_WS is 0 or when predictable execution behavior is required. '1': enabled.
8	FLASH_INVALIDATE	RW	RW1C	0	1': Invalidates the content of the flash controller's buffers.
16:17	ARB	RW	R	0	Arbitration policy: 0: CPU has priority 1: DW/DMA has priority 2: Roundrobin 3: Roundrobin - sticky

Bits	Name	SW	HW	Default or Enum	Description
20	FLASH_ECC_INJ_EN	RW	R	0	Enable error injection for FLASH main interface. When'1', the parity (ECC_CTL.PARITY[7:0]) is used for a load from the ECC_CTL.WORD_ADDR[23:0] word address.
21	FLASH_ERR_SILENT	RW	R	0	Specifies bus transfer behavior for a non-recoverable error on the FLASH macro main interface (either a non-correctable ECC error, a FLASH macro main interface internal error, a FLASH macro main interface memory hole access, a M0S8 protection violation error): 0: Bus transfer has a bus error. 1: Bus transfer does NOT have a bus error; i.e. the error is 'silent' In either case, a Zero value is returned. This field is ONLY used by CPU bus transfers. Non-CPU bus transfers always have a bus transfer with a bus error, in case of a non-recoverable error

2.1.8 CPUSS_FAULT_CTL

Description: Fault Control Register
Address: 0x401000AC
Offset: 0xAC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
16:17	ARB	RW	R	0	Arbitration policy: 0: CPU has priority 1: DW/DMA has priority 2: Roundrobin 3: Roundrobin - sticky

2.1.9 CPUSS_RAM_STATUS

Description: RAM Controller 0 Status
Address: 0x401000D0
Offset: 0xD0
Retention: Retained
IsDeepSleep: No
Comment: This register is for the CPUSS system SRAM controller 0.
Default: 0x1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							WB _EMPTY [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WB_EMPTY	R	W	1	Write buffer empty. This information is used when entering DeepSleep power mode: WB_EMPTY must be '1' before a transition to system DeepSleep power mode. '0': Write buffer NOT empty. '1': Write buffer empty. Note: the SRAM controller write buffer is only used when ECC checking is enabled. (RAMi_CTL.ECC_EN is '1').

2.1.10 CPUSS_BOOT_RESULT_0

Description: Boot Result Register 0
Address: 0x401000E0
Offset: 0xE0
Retention: Not Retained
IsDeepSleep: No
Comment: This register contains details of any results from the Boot Process
Default: 0x1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BOOT_RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	BOOT_RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	BOOT_RESULT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	BOOT_RESULT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	BOOT_RESULT	RW		1	Record details of Boot Process.

2.1.11 CPUSS_BOOT_RESULT_1

Description: Boot Result Register 1
Address: 0x401000E4
Offset: 0xE4
Retention: Not Retained
IsDeepSleep: No
Comment: This register contains details of any results from the Boot Process
Default: 0x1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BOOT_RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	BOOT_RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	BOOT_RESULT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	BOOT_RESULT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	BOOT_RESULT	RW		1	Record details of Boot Process.

2.1.12 CPUSS_SL_CTL

Description: Slave control register
Address: 0x40100100
Offset: 0x100
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
16:17	ARB	RW	R	0	Arbitration policy: 0: CPU priority 1: DMA priority 2: Roundrobin 3: Roundrobin - sticky

2.1.13 CPUSS_RAM_ECC_STATUS0

Description: RAM ECC Status 0
Address: 0x40100200
Offset: 0x200
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ECC_CAPTURE_ADDR_31_2 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ECC_CAPTURE_ADDR_31_2 [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ECC_CAPTURE_ADDR_31_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ECC_CAPTURE_ADDR_SYNDROME_VALID [31:31]	None [30:30]	ECC_CAPTURE_ADDR_31_2 [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:29	ECC_CAPTURE_ADDR_31_2	R	RW	Undefined	Snapshot of CPUSS Address which caused the first correctable/un-correctable error interrupt. When first correctable/un-correctable error interrupt is generated, ECC_CAPTURE_ADDR_SYNDROME_VALID is transitioned from 0 to 1 , and this registered captures the first error address. The register only captures bits 31-2 of the address.
31	ECC_CAPTURE_ADDR_SYNDROME_VALID	RW1C	RW1S	0	ECC Capture address and Syndrome valid. 0: ECC_CAPTURE_ADDR_31_2 not valid 1: ECC_CAPTURE_ADDR_31_2 valid - SW writes a 1 to clear

2.1.14 CPUSS_RAM_ECC_STATUS1

Description: RAM ECC Status 1
Address: 0x40100204
Offset: 0x204
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	ECC_CAPTURE_SYNDROME [6:0]						

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:6	ECC_CAPTURE_SYNDROME	R	RW	Undefined	Snapshot of CPUSS Syndrome which caused the first correctable/un-correctable error interrupt. When first correctable/un-correctable error interrupt is generated, ECC_CAPTURE_ADDR_SYNDROME_VALID is transitioned from 0 to 1 , and this registered captures the first Syndrome corresponding to the Error.

2.1.15 CPUSS_ECC_TEST

Description: ECC Test
Address: 0x40100210
Offset: 0x210
Retention: Retained
IsDeepSleep: No
Comment: Register defines the address and supplies the Syndrome for ECC Testing
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	WORD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	WORD_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	WORD_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	SYND_DATA [31:25]							WORD_ADDR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:24	WORD_ADDR	RW	R	0	Specifies the word address where an error will be injected. - For SRAMs, the word address WORD_ADDR[24:0] is the device address A[26:2]. On a write transfer to this SRAM address and when the corresponding RAM_CTL.ECC_INJ_EN or RAM1_CTL.ECC_INJ_EN bit is '1', the parity (SYND_DATA[6:0]) is injected into the corresponding SRAM location.
25:31	SYND_DATA	RW	R	0	ECC syndrome to use for error injection at address WORD_ADDR.

2.1.16 CPUSS_FLASHC_BERR_STATUS

Description: Flash Bus Error Status
Address: 0x40100500
Offset: 0x500
Retention: Retained
IsDeepSleep: No
Comment: Reports Bus Error Causes for Flash bus transactions
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				FLASH_PROT_VIO [3:3]	FLASH_MEMORY_HOLE [2:2]	FLASH_UNCORRECTABLE [1:1]	INTERNAL_ERROR [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	INTERNAL_ERROR	RW1C	W1S	0	Specifies/registers the occurrence of a FLASH macro interface internal error (typically the result of a read access while a program erase operation is ongoing) as a result of a CM0+ access. SW clears this field to '0'. HW sets this field to '1' on a FLASH macro interface internal error. Typically, SW reads this field after a code section to detect the occurrence of an error. Note: this field is independent of FLASH_CTL.FLASH_ERR_SILENT.
1	FLASH_UNCORRECTABLE	RW1C	W1S	0	An Uncorrectable Read error occurred when accessing a Flash Macro. SW clears this field to '0'. HW sets this field to '1' on a FLASH macro uncorrectable error. Typically, SW reads this field after a code section to detect the occurrence of an error. Note: this field is independent of FLASH_CTL.FLASH_ERR_SILENT.
2	FLASH_MEMORY_HOLE	RW1C	W1S	0	An access to a non-existent Flash Address occurred. SW clears this field to '0'. HW sets this field to '1' on a FLASH macro access to a non-existent address. Typically, SW reads this field after a code section to detect the occurrence of an error. Note: this field is independent of FLASH_CTL.FLASH_ERR_SILENT.

Bits	Name	SW	HW	Default or Enum	Description
3	FLASH_PROT_VIO	RW1C	W1S	0	A protection violation occurred in Flash Controller. SW clears this field to '0'. HW sets this field to '1' on a protection violation occurred in Flash Controllers. Typically, SW reads this field after a code section to detect the occurrence of an error. Note: this field is independent of FLASH_CTL.FLASH_ERR_SILENT.

2.1.17 CPUSS_FLASHC1_BERR_STATUS

Description: Flash 1 Bus Error Status
Address: 0x40100504
Offset: 0x504
Retention: Retained
IsDeepSleep: No
Comment: Reports Bus Error Causes for Flash bus transactions
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				FLASH_PROT_VIO [3:3]	FLASH_MEMORY_HOLE [2:2]	FLASH_UNCORRECTABLE [1:1]	INTERNAL_ERROR [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	INTERNAL_ERROR	RW1C	W1S	0	See the Explanation for FLASHC_BERR_STATUS
1	FLASH_UNCORRECTABLE	RW1C	W1S	0	See the Explanation for FLASHC_BERR_STATUS
2	FLASH_MEMORY_HOLE	RW1C	W1S	0	See the Explanation for FLASHC_BERR_STATUS
3	FLASH_PROT_VIO	RW1C	W1S	0	See the Explanation for FLASHC_BERR_STATUS

2.1.18 CPUSS_FLASHC_ECC_CTL

Description: Flash ECC Control
Address: 0x40100508
Offset: 0x508
Retention: Retained
IsDeepSleep: No
Comment: Note that for cache SRAM and FLASH work interface ECC, the word address is for a 32-bit word. For FLASH main interface ECC, the word address is for a 64-bit word.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	FLASH_WORD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	FLASH_WORD_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	FLASH_WORD_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	PARITY [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:23	FLASH_WORD_ADDR	RW	R	0	Specifies the word address where an error will be injected. - For FLASH interface ECC, the word address WORD_ADDR[23:0] is device address A[26:3]. On a FLASH main interface read and when FLASH_CTL.MAIN_ECC_INJ_EN bit is '1', the parity (PARITY[7:0]) replaces the FLASH macro parity (FLASH main interface read path is manipulated).
24:31	PARITY	RW	R	0	ECC parity to use for ECC error injection at address WORD_ADDR. - For FLASH interface ECC, the 8-bit parity PARITY[7:0] is for a 64-bit word.

2.1.19 CPUSS_FLASHC1_ECC_CTL

Description: Flash 1 ECC Control
Address: 0x4010050C
Offset: 0x50C
Retention: Retained
IsDeepSleep: No
Comment: Note that for cache SRAM and FLASH work interface ECC, the word address is for a 32-bit word. For FLASH main interface ECC, the word address is for a 64-bit word.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	FLASH_WORD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	FLASH_WORD_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	FLASH_WORD_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	PARITY [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:23	FLASH_WORD_ADDR	RW	R	0	See the Explanation for FLASHC_ECC_CTL
24:31	PARITY	RW	R	0	See the Explanation for FLASHC_ECC_CTL

3 DMAC

Description DataWire/DMA Controller
Base Address 0x40101000
Size 0x1000
Slave Num CPUMEMSSV3_VER3

Register Name	Address	Permission	Description
DMAC_CTL	0x40101000	FULL	Control register
DMAC_STATUS	0x40101010	FULL	Status register
DMAC_STATUS_SRC_ADDR	0x40101014	FULL	Source address status register
DMAC_STATUS_DST_ADDR	0x40101018	FULL	Destination address register
DMAC_STATUS_CH_ACT	0x4010101C	FULL	Channel activation status register
DMAC_CH_CTL0	0x40101080	FULL	Channel control register
DMAC_CH_CTL1	0x40101084	FULL	Channel control register
DMAC_CH_CTL2	0x40101088	FULL	Channel control register
DMAC_CH_CTL3	0x4010108C	FULL	Channel control register
DMAC_CH_CTL4	0x40101090	FULL	Channel control register
DMAC_CH_CTL5	0x40101094	FULL	Channel control register
DMAC_CH_CTL6	0x40101098	FULL	Channel control register
DMAC_CH_CTL7	0x4010109C	FULL	Channel control register
DMAC_INTR	0x401017F0	FULL	Interrupt register
DMAC_INTR_SET	0x401017F4	FULL	Interrupt set register
DMAC_INTR_MASK	0x401017F8	FULL	Interrupt mask register
DMAC_INTR_MASKED	0x401017FC	FULL	Interrupt masked register

3.1 DESCR 0

Register Name	Address	Permission	Description
DMAC_DESCR0_PING_SRC	0x40101800	FULL	Ping source address
DMAC_DESCR0_PING_DST	0x40101804	FULL	Ping destination address
DMAC_DESCR0_PING_CTL	0x40101808	FULL	Ping control word
DMAC_DESCR0_PING_STATUS	0x4010180C	FULL	Ping status word
DMAC_DESCR0_PONG_SRC	0x40101810	FULL	Pong source address
DMAC_DESCR0_PONG_DST	0x40101814	FULL	Pong destination address
DMAC_DESCR0_PONG_CTL	0x40101818	FULL	Pong control word
DMAC_DESCR0_PONG_STATUS	0x4010181C	FULL	Pong status word

3.2 DESCR 1

Register Name	Address	Permission	Description
DMAC_DESCR1_PING_SRC	0x40101820	FULL	Ping source address
DMAC_DESCR1_PING_DST	0x40101824	FULL	Ping destination address
DMAC_DESCR1_PING_CTL	0x40101828	FULL	Ping control word
DMAC_DESCR1_PING_STATUS	0x4010182C	FULL	Ping status word
DMAC_DESCR1_PONG_SRC	0x40101830	FULL	Pong source address
DMAC_DESCR1_PONG_DST	0x40101834	FULL	Pong destination address
DMAC_DESCR1_PONG_CTL	0x40101838	FULL	Pong control word
DMAC_DESCR1_PONG_STATUS	0x4010183C	FULL	Pong status word

3.3 DESCR 2

Register Name	Address	Permission	Description
DMAC_DESCR2_PING_SRC	0x40101840	FULL	Ping source address
DMAC_DESCR2_PING_DST	0x40101844	FULL	Ping destination address
DMAC_DESCR2_PING_CTL	0x40101848	FULL	Ping control word
DMAC_DESCR2_PING_STATUS	0x4010184C	FULL	Ping status word
DMAC_DESCR2_PONG_SRC	0x40101850	FULL	Pong source address
DMAC_DESCR2_PONG_DST	0x40101854	FULL	Pong destination address
DMAC_DESCR2_PONG_CTL	0x40101858	FULL	Pong control word
DMAC_DESCR2_PONG_STATUS	0x4010185C	FULL	Pong status word

3.4 DESCR 3

Register Name	Address	Permission	Description
DMAC_DESCR3_PING_SRC	0x40101860	FULL	Ping source address
DMAC_DESCR3_PING_DST	0x40101864	FULL	Ping destination address
DMAC_DESCR3_PING_CTL	0x40101868	FULL	Ping control word
DMAC_DESCR3_PING_STATUS	0x4010186C	FULL	Ping status word
DMAC_DESCR3_PONG_SRC	0x40101870	FULL	Pong source address
DMAC_DESCR3_PONG_DST	0x40101874	FULL	Pong destination address
DMAC_DESCR3_PONG_CTL	0x40101878	FULL	Pong control word
DMAC_DESCR3_PONG_STATUS	0x4010187C	FULL	Pong status word

3.5 DESCR 4

Register Name	Address	Permission	Description
DMAC_DESCR4_PING_SRC	0x40101880	FULL	Ping source address
DMAC_DESCR4_PING_DST	0x40101884	FULL	Ping destination address
DMAC_DESCR4_PING_CTL	0x40101888	FULL	Ping control word
DMAC_DESCR4_PING_STATUS	0x4010188C	FULL	Ping status word
DMAC_DESCR4_PONG_SRC	0x40101890	FULL	Pong source address
DMAC_DESCR4_PONG_DST	0x40101894	FULL	Pong destination address
DMAC_DESCR4_PONG_CTL	0x40101898	FULL	Pong control word
DMAC_DESCR4_PONG_STATUS	0x4010189C	FULL	Pong status word

3.6 DESCR 5

Register Name	Address	Permission	Description
DMAC_DESCR5_PING_SRC	0x401018A0	FULL	Ping source address
DMAC_DESCR5_PING_DST	0x401018A4	FULL	Ping destination address
DMAC_DESCR5_PING_CTL	0x401018A8	FULL	Ping control word
DMAC_DESCR5_PING_STATUS	0x401018AC	FULL	Ping status word
DMAC_DESCR5_PONG_SRC	0x401018B0	FULL	Pong source address
DMAC_DESCR5_PONG_DST	0x401018B4	FULL	Pong destination address
DMAC_DESCR5_PONG_CTL	0x401018B8	FULL	Pong control word
DMAC_DESCR5_PONG_STATUS	0x401018BC	FULL	Pong status word

3.7 DESCR 6

Register Name	Address	Permission	Description
DMAC_DESCR6_PING_SRC	0x401018C0	FULL	Ping source address
DMAC_DESCR6_PING_DST	0x401018C4	FULL	Ping destination address
DMAC_DESCR6_PING_CTL	0x401018C8	FULL	Ping control word
DMAC_DESCR6_PING_STATUS	0x401018CC	FULL	Ping status word
DMAC_DESCR6_PONG_SRC	0x401018D0	FULL	Pong source address
DMAC_DESCR6_PONG_DST	0x401018D4	FULL	Pong destination address
DMAC_DESCR6_PONG_CTL	0x401018D8	FULL	Pong control word
DMAC_DESCR6_PONG_STATUS	0x401018DC	FULL	Pong status word

3.8 DESCR 7

Register Name	Address	Permission	Description
DMAC_DESCR7_PING_SRC	0x401018E0	FULL	Ping source address
DMAC_DESCR7_PING_DST	0x401018E4	FULL	Ping destination address
DMAC_DESCR7_PING_CTL	0x401018E8	FULL	Ping control word
DMAC_DESCR7_PING_STATUS	0x401018EC	FULL	Ping status word
DMAC_DESCR7_PONG_SRC	0x401018F0	FULL	Pong source address
DMAC_DESCR7_PONG_DST	0x401018F4	FULL	Pong destination address
DMAC_DESCR7_PONG_CTL	0x401018F8	FULL	Pong control word
DMAC_DESCR7_PONG_STATUS	0x401018FC	FULL	Pong status word

3.9 Register Details

3.9.1 DMAC_CTL

Description: Control register
Address: 0x40101000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
31	ENABLED	RW	R	0	0': IP is disabled. Non-retainable MMIO registers and logic functionality are reset (retainable MMIO registers are NOT reset): - INTR register is set to '0'. - DW/DMA functionality is aborted. - DW/DMA controller input/pending triggers are de-activated. - DW/DMA controller output triggers are de-activated. Disabling the IP has the same effect as an active 'rst_sys_act_n' reset in DeepSleep power mode. To prevent a loss of active (pending) DW/DMA triggers when disabling the IP or when transitioning from Active to DeepSleep power mode, the STATUS.ACTIVE and STATUS_CH_ACT.CH fields can be used. Note that most MMIO registers are retainable, and a transition from DeepSleep to Active/Sleep power modes makes the DW/DMA controller operational, and ready to react to DW/DMA input triggers that are activated after the transition. Triggers are Active/Sleep functionality. '1': IP is enabled.

3.9.2 DMAC_STATUS

Description: Status register
Address: 0x40101010
Offset: 0x10
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:19]					CH_ADDR [18:16]		

Bits	31	30	29	28	27	26	25	24
Name	ACTIVE [31:31]	PING_PONG [30:30]	PRIO [29:28]		None [27:27]	STATE [26:24]		

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	DATA_NR	R	W	Undefined	Specifies the index of the currently active data transfer. This value increases from '0' to CONTROL.DATA_NR.
16:18	CH_ADDR	R	W	Undefined	Specifies the channel number of the currently active channel. E.g. if we have 32 channels, the channel number address with CH_ADDR_WIDTH is LOG2 (32) = 5, and this field is a 5-bit field. If channel 7 is active, STATUS.ACTIVE is '1' and STATUS.CH_ADDR is '7'.
24:26	STATE	R	W	0	State of the data transfer engine. '0': DEFAULT state. '1': Loading descriptor (SRC, DST, CONTROL and STATUS words). '2': Loading data element from source location. '3': Storing data element to destination location. '4': Storing descriptor (STATUS word). '5': Wait for trigger de-activation. '6': Storing descriptor with error response (STATUS word).
28:29	PRIO	R	W	Undefined	Specifies the priority of the currently active channel.
30	PING_PONG	R	W	Undefined	Specifies the descriptor of the channel is currently in use. '0' - PING descriptor '1' - PONG descriptor
31	ACTIVE	R	W	0	Specifies if there is a currently active (pending) channel in the data transfer engine: '0': no currently active channel. '1': currently active channel.

3.9.3 DMAC_STATUS_SRC_ADDR

Description: Source address status register
Address: 0x40101014
Offset: 0x14
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ADDR [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ADDR	R	W	Undefined	Base address or current address of source location of currently active channel. The specific address information is cycle dependent. This field is provided for debug purposes. Functionally, no assumption should be made on whether the base or current address is provided. The specifics of the currently active channel are available through STATUS. Note while reading the STATUS, STATUS_SRC_ADDR and STATUS_DST_ADDR registers, the transfer engine may have moved from one active channel to another.

3.9.4 DMAC_STATUS_DST_ADDR

Description: Destination address register
Address: 0x40101018
Offset: 0x18
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ADDR [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ADDR	R	W	Undefined	Base address or current address of destination location of currently active channel. The specific address information is cycle dependent. This field is provided for debug purposes. Functionally, no assumption should be made on whether the base or current address is provided. The specifics of the currently active channel are available through STATUS. Note while reading the STATUS, STATUS_SRC_ADDR and STATUS_DST_ADDR registers, the transfer engine may have moved from one active channel to another.

3.9.5 DMAC_STATUS_CH_ACT

Description: Channel activation status register
Address: 0x4010101C
Offset: 0x1C
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	CH	R	W	0	Channel activation status. Bit i is associated to channel i, with i = 0, ..., CH_NR-1. Software reads this field to get information on all actively pending channels (either in pending or in the data transfer engine).

3.9.6 DMAC_CH_CTL

Description: Channel control register
Address: 0x40101080
Offset: 0x80
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	PING_PONG [30:30]	PRIO [29:28]		None [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
28:29	PRIO	RW	R	0	Channel priority, with '0' representing the highest priority and '3' representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel.
30	PING_PONG	RW	RW	0	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING ('0') and PONG ('1'). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to '1'.
31	ENABLED	RW	RW1C	0	'0': channel disabled. The channel's trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. '1': channel enabled. Software sets this field to '1' to enable a specific channel. Hardware sets this field to '0' on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channel's descriptor structure).

3.9.7 DMAC_INTR

Description: Interrupt register
Address: 0x401017F0
Offset: 0x7F0
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	CH	RW1C	RW1S	0	Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit.

3.9.8 DMAC_INTR_SET

Description: Interrupt set register
Address: 0x401017F4
Offset: 0x7F4
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	CH	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).

3.9.9 DMAC_INTR_MASK

Description: Interrupt mask register
Address: 0x401017F8
Offset: 0x7F8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	CH	RW	R	0	Mask for corresponding field in INTR register.

3.9.10 DMAC_INTR_MASKED

Description: Interrupt masked register
Address: 0x401017FC
Offset: 0x7FC
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_M_MASKED != 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	CH	R	W	0	Logical BITWISE AND of corresponding request and mask fields.

3.9.11 DESCR

3.9.11.1 DMAC_DESCR_PING_SRC

Description: Ping source address
Address: 0x40101800
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ADDR [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ADDR	RW	RW	Undefined	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address.

3.9.11.2 DMAC_DESCR_PING_DST

Description: Ping destination address
Address: 0x40101804
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ADDR [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ADDR	RW	RW	Undefined	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address.

3.9.11.3 DMAC_DESCR_PING_CTL

Description: Ping control word
Address: 0x40101808
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment: Bits 18 and 19 of this MMIO register are not used. A SW write operation should write '0' to the unused bits.
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	SRC_ADDR_INCR [23:23]	SRC_TRANSFER_SIZE [22:22]	DST_ADDR_INCR [21:21]	DST_TRANSFER_SIZE [20:20]	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	OPCODE [31:30]		FLIPPING [29:29]	PREEMPTABLE [28:28]	SET_CAUSE [27:27]	INV_DESCR [26:26]	WAIT_FOR_DEACT [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	DATA_NR	RW	RW	Undefined	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is '0') each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is '1' or '2') each trigger initiates the transfer of DATA_NR+1 data elements.

Bits	Name	SW	HW	Default or Enum	Description
16:17	DATA_SIZE	RW	RW	Undefined	Specifies the data element size: '0': Byte (8 bits). '1': Halfword (16 bits). '2': Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made '0') - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made '0') - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made '0') - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made '0') - DATA is 32 bit, SRC is 32 bit, DST is 32 bit
20	DST_TRANSFER_SIZE	RW	RW	Undefined	Specifies the bus transfer size to the destination location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element.
21	DST_ADDR_INCR	RW	RW	Undefined	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. '0' : No increment, typically used for transmit (TX) FIFO structures. '1': Increment, typically used for memory structures.
22	SRC_TRANSFER_SIZE	RW	RW	Undefined	Specifies the bus transfer size to the source location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element.
23	SRC_ADDR_INCR	RW	RW	Undefined	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. '0': No increment, typically used for receive (RX) FIFO structures. '1': Increment, typically used for memory structures.

Bits	Name	SW	HW	Default or Enum	Description
24:25	WAIT_FOR_DEACT	RW	RW	Undefined	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller's data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agent's trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to '0'). The wait cycles incurred by this field reduce DW/DMA controller performance. '0': Do not wait for de-activation (for pulse sensitive triggers). '1': Wait for up to 4 cycles. '2': Wait for up to 8 cycles. '3': Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent.
26	INV_DESCR	RW	RW	Undefined	'1': On completion of the current descriptor structure, the VALID bit of the descriptor's STATUS word is set to '0'.
27	SET_CAUSE	RW	RW	Undefined	'1': On completion of the current descriptor structure, the interrupt cause field of the channel is set to '1' (INTR.CH[i]).
28	PREEMPTABLE	RW	RW	Undefined	'1': Transfer is preemptable. In DMA mode (OPCODE is '1' or '2'), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled.
29	FLIPPING	RW	RW	Undefined	'1': On completion of the current descriptor structure, the current descriptor identifier CH_CTLi.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures.

Bits	Name	SW	HW	Default or Enum	Description
30:31	OPCODE	RW	RW	Undefined	Specifies the specific data transfer (only when the VALID bit of the descriptor's STATUS word is '1'): '0': A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). '1': A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. '2': A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CH_CTLi.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completion of the opcode (and waiting for de-activation, the channel's output trigger is activated).

3.9.11.4 DMAC_DESCR_PING_STATUS

Description: Ping status word
Address: 0x4010180C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment: Bits 30 down to 19 of this MMIO register are not used. A SW write operation should write '0' to the unused bits.
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
Name	VALID [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	CURR_DATA_NR	RW	RW	Undefined	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to '0' when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be '1'). At descriptor initialization, SW should set this field to '0'. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses.

Bits	Name	SW	HW	Default or Enum	Description
16:18	RESPONSE	RW	RW	Undefined	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). '0'/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to '1'. STATUS.VALID is NOT affected. CH_CTLi.ENABLED is NOT affected. CH_CTLi.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to '0'/NO_ERROR during descriptor initialization. '1'/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to '1' if CONTROL.SET_CAUSE is '1'. STATUS.VALID is set to '0' if CONTROL.INV_DESCR is '1'. CH_CTLi.ENABLED is NOT affected. CH_CTLi.PING_PONG is updated if CONTROL.FLIPPING is '1'. '2'/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to '1'. STATUS.VALID is set '0'. CH_CTLi.ENABLED is set to '0'. CH_CTLi.PING_PONG is not updated (it identifies the descriptor that caused the error). '3'/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to '1'. STATUS.VALID is set '0'. CH_CTLi.ENABLED is set to '0'. CH_CTLi.PING_PONG is not updated (it identifies the descriptor that caused the error). '4'/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to '1'. STATUS.VALID is set '0'. CH_CTLi.ENABLED is set to '0'. CH_CTLi.PING_PONG is not updated (it identifies the descriptor that caused the error). '5'/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to '1'. STATUS.VALID is set '0'. CH_CTLi.ENABLED is set to '0'. CH_CTLi.PING_PONG is not updated (it identifies the descriptor that caused the error). '6'/INVALID_DESCR: Invalid descriptor (STATUS.VALID is '0'). This occurs when an activated channel has an invalid descriptor. CH_CTLi.ENABLED is set to '0'. CH_CTLi.PING_PONG is not updated (it identifies the descriptor that caused the error).
31	VALID	RW	RW	Undefined	'0': Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to '1'). '1': Valid. Hardware set this field to '0' when a descriptor is done, but only if CONTROL.INV_DESCR is '1'. Software sets this field to '1' when a descriptor is initialized.

3.9.11.5 DMAC_DESCR_PONG_SRC

Description: Pong source address
Address: 0x40101810
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ADDR [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ADDR	RW	RW	Undefined	See description of PING_SRC.

3.9.11.6 DMAC_DESCR_PONG_DST

Description: Pong destination address
Address: 0x40101814
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ADDR [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ADDR	RW	RW	Undefined	See description of PING_DST.

3.9.11.7 DMAC_DESCR_PONG_CTL

Description: Pong control word
Address: 0x40101818
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment: Bits 18 and 19 of this MMIO register are not used. A SW write operation should write '0' to the unused bits.
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	SRC _ADDR_ INCR [23:23]	SRC _TRANS FER_SIZE [22:22]	DST_ADDR _INCR [21:21]	DST _TRANS FER_SIZE [20:20]	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	OPCODE [31:30]		FLIPPING [29:29]	PREEMPTAB LE [28:28]	SET _CAUSE [27:27]	INV _DESCR [26:26]	WAIT_FOR_DEACT [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	DATA_NR	RW	RW	Undefined	See description of PING_CTL.
16:17	DATA_SIZE	RW	RW	Undefined	See description of PING_CTL.
20	DST_TRANSFER_SIZE	RW	RW	Undefined	See description of PING_CTL.
21	DST_ADDR_INCR	RW	RW	Undefined	See description of PING_CTL.
22	SRC_TRANSFER_SIZE	RW	RW	Undefined	See description of PING_CTL.
23	SRC_ADDR_INCR	RW	RW	Undefined	See description of PING_CTL.
24:25	WAIT_FOR_DEACT	RW	RW	Undefined	See description of PING_CTL.
26	INV_DESCR	RW	RW	Undefined	See description of PING_CTL.
27	SET_CAUSE	RW	RW	Undefined	See description of PING_CTL.
28	PREEMPTABLE	RW	RW	Undefined	See description of PING_CTL.
29	FLIPPING	RW	RW	Undefined	See description of PING_CTL.
30:31	OPCODE	RW	RW	Undefined	See description of PING_CTL.

3.9.11.8 DMAC_DESCR_PONG_STATUS

Description: Pong status word
Address: 0x4010181C
Offset: 0x1C
Retention: Retained
IsDeepSleep: No
Comment: Bits 30 down to 19 of this MMIO register are not used. A SW write operation should write '0' to the unused bits.
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
Name	VALID [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	CURR_DATA_NR	RW	RW	Undefined	See description of PING_STATUS.
16:18	RESPONSE	RW	RW	Undefined	See description of PING_STATUS.
31	VALID	RW	RW	Undefined	See description of PING_STATUS.

4 FAULT

Description Fault structures
Base Address 0x40130000
Size 0x10000
Slave Num FAULT

4.1 STRUCT 0

Register Name	Address	Permission	Description
FAULT_STRUCT0_CTL	0x40130000	FULL	Fault control
FAULT_STRUCT0_STATUS	0x4013000C	FULL	Fault status
FAULT_STRUCT0_DATA0	0x40130010	FULL	Fault data
FAULT_STRUCT0_DATA1	0x40130014	FULL	Fault data
FAULT_STRUCT0_PENDING0	0x40130040	FULL	Fault pending 0
FAULT_STRUCT0_MASK0	0x40130050	FULL	Fault mask 0
FAULT_STRUCT0_INTR	0x401300C0	FULL	Interrupt
FAULT_STRUCT0_INTR_SET	0x401300C4	FULL	Interrupt set
FAULT_STRUCT0_INTR_MASK	0x401300C8	FULL	Interrupt mask
FAULT_STRUCT0_INTR_MASKED	0x401300CC	FULL	Interrupt masked

4.2 STRUCT 1

Register Name	Address	Permission	Description
FAULT_STRUCT1_CTL	0x40130100	FULL	Fault control
FAULT_STRUCT1_STATUS	0x4013010C	FULL	Fault status
FAULT_STRUCT1_DATA0	0x40130110	FULL	Fault data
FAULT_STRUCT1_DATA1	0x40130114	FULL	Fault data
FAULT_STRUCT1_PENDING0	0x40130140	FULL	Fault pending 0
FAULT_STRUCT1_MASK0	0x40130150	FULL	Fault mask 0
FAULT_STRUCT1_INTR	0x401301C0	FULL	Interrupt
FAULT_STRUCT1_INTR_SET	0x401301C4	FULL	Interrupt set
FAULT_STRUCT1_INTR_MASK	0x401301C8	FULL	Interrupt mask
FAULT_STRUCT1_INTR_MASKED	0x401301CC	FULL	Interrupt masked

4.3 Register Details

4.3.1 STRUCT

4.3.1.1 FAULT_STRUCT_CTL

Description: Fault control
Address: 0x40130000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: This register uses DeepSleep reset. Therefore, a DeepSleep reset (possibly as a result of CTL.RESET_EN) resets this register (including setting CTL.RESET_EN to '0').
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					RESET_REQ_EN [2:2]	OUT_EN [1:1]	TR_EN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TR_EN	RW	R	0	Trigger output enable: '0': Disabled. The trigger output 'tr_fault' is '0'. '1': Enabled. The trigger output 'tr_fault' reflects STATUS.VALID. The trigger can be used to initiate a Datawire transfer of the FAULT data (FAULT_DATA0 through FAULT_DATA1).
1	OUT_EN	RW	R	0	IO output signal enable: '0': Disabled. The IO output signal 'fault_out' is '0'. The IO output enable signal 'fault_out_en' is '0'. '1': Enabled. The IO output signal 'fault_out' reflects STATUS.VALID. The IO output enable signal 'fault_out_en' is '1'.
2	RESET_REQ_EN	RW	R	0	Reset request enable: '0': Disabled. '1': Enabled. The output reset request signal 'fault_reset_req' reflects STATUS.VALID. This reset causes a warm/soft/core reset. This warm/soft/core reset does not affect the fault logic STATUS, DATA0, ..., DATA1 registers (allowing for post soft reset failure analysis). The 'fault_reset_req' signals of the individual fault report structures are combined (logically OR'd) into a single SRSS 'fault_reset_req' signal.

4.3.1.2 FAULT_STRUCT_STATUS

Description: Fault status
Address: 0x4013000C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment: This register uses cold reset (and is NOT affected by Active or DeepSleep reset). This allows for failure analysis after a warm reset (DeepSleep reset).
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	IDX [6:0]						

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALID [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:6	IDX	RW	W	Undefined	The fault source index for which fault information is captured in DATA0 through DATA1. The fault information is fault source specific and differs per product. The encoding will align with the definition in the Product Srpeadsheet. Note: this register field (and associated fault source data in DATA0 through DATA1) should only be considered valid, when VALID is '1'.

Bits	Name	SW	HW	Default or Enum	Description
31	VALID	RW	RW1S	0	Valid indication: '0': Invalid. '1': Valid. STATUS.IDX, DATA0, ..., DATA1 specify the fault. Note: Typically, HW sets this field to '1' (on an activated HW fault source that is 'enabled' by the MASK registers) and SW clears this field to '0' (typically by boot code SW (after a warm system reset, when the fault is handled). In this typical use case scenario, the HW source fault data is simultaneously captured into DATA0, ..., DATA1 when the VALID field is set to '1'. An exceptional SW use case scenario is identified as well. In this scenario, SW sets this field to '1' with a fault source index different to one of the defined HW fault sources. SW update is not restricted by the MASK registers). In both use case scenarios, the following holds: - STATUS.IDX, DATA0, ..., DATA1 can only be written when STATUS.VALID is '0'; the fault structure is not in use yet. Writing STATUS.VALID to '1' effectively locks the fault structure (until SW clears STATUS.VALID to '0'). This restriction requires a SW update to sequentially update the DATA registers followed by an update of the STATUS register. Note: For the exceptional SW use case, sequential updates to the DATA and STATUS registers may be 'interrupted' by a HW fault capture. In this case, the SW DATA register updates are overwritten by the HW update (and the STATUS.IDX field will reflect the HW capture)

4.3.1.3 FAULT_STRUCT_DATA

Description: Fault data
Address: 0x40130010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: The DATA registers capture fault information.

These register use cold reset (and are NOT affected by Active or DeepSleep reset). This allows for failure analysis after a warm reset (DeepSleep reset).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	DATA [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	DATA	RW	W	Undefined	Captured fault source data. Note: the DATA registers can only be written when STATUS.VALID is '0'. Note: the fault source index STATUS.IDX specifies the format of the DATA registers.

4.3.1.4 FAULT_STRUCT_PENDING0

Description: Fault pending 0
Address: 0x40130040
Offset: 0x40
Retention: Not Retained
IsDeepSleep: No
Comment: The PENDING0 register specifies pending (not captured) fault sources. The fault source for which data is captured in DATA0 through DATA1 and which is validated by STATUS.VALID and identified by STATUS.IDX is NOT included in this list of pending fault sources. When a fault source is captured, its corresponding bit field in PENDING0s set to '0'.
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	SOURCE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	SOURCE	R	W	Undefined	Bit mask of source causing the Fault. See the Product Spreadsheet Fault tab to determine the bit ordering.

4.3.1.5 FAULT_STRUCT_MASK0

Description: Fault mask 0
Address: 0x40130050
Offset: 0x50
Retention: Retained
IsDeepSleep: No
Comment: The MASK0 register specifies 'enables' for fault sources. Only 'enabled' fault sources will be captured by this fault structure (and result in STATUS.VALID and INTR.FAULT being set to '1'). When a fault source is captured, its corresponding bit field in PENDING0 is set to '0'.

When multiple fault structures are present and the mask fields of the fault structures overlap (the same source is 'enabled' for multiple fault structures), an overlapping enabled pending fault source is captured by a single fault structure that has not captured a fault (the fault structure with the lowest index has precedence).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	SOURCE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	SOURCE	RW	R	0	Fault source enables: Bits 31-0: Fault sources 31 to 0.

4.3.1.6 FAULT_STRUCT_INTR

Description: Interrupt
Address: 0x401300C0
Offset: 0xC0
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							FAULT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	FAULT	RW1C	RW1S	0	This interrupt cause field is activated (HW sets the field to '1') when an enabled (MASK0 pending fault source is captured: - STATUS.VALID is set to '1'. - STATUS.IDX specifies the fault source index. - DATA0 through DATA1 captures the fault source data. SW writes a '1' to this field to clear the interrupt cause to '0'. SW clear STATUS.VALID to '0' to enable capture of the next fault. Note that when there is an enabled pending fault source, the pending fault source is captured immediately and INTR.FAULT is immediately activated (set to '1').

4.3.1.7 FAULT_STRUCT_INTR_SET

Description: Interrupt set
Address: 0x401300C4
Offset: 0xC4
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the INTR register. For debug purposes, SW can write a '1' to activate a specific interrupt cause (this allows for debug of the SW ISR, without relying on HW to activate the interrupt cause).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							FAULT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	FAULT	RW1S	A	0	SW writes a '1' to this field to set the corresponding field in the INTR register.

4.3.1.8 FAULT_STRUCT_INTR_MASK

Description: Interrupt mask
Address: 0x401300C8
Offset: 0xC8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							FAULT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	FAULT	RW	R	0	Mask bit for corresponding field in the INTR register.

4.3.1.9 FAULT_STRUCT_INTR_MASKED

Description: Interrupt masked
Address: 0x401300CC
Offset: 0xCC
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects 'a bitwise AND' between the INTR and INTR_MASK registers.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							FAULT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	FAULT	R	W	0	Logical and of corresponding INTR and INTR_MASK fields.

5 GPIO

Description GPIO port control/configuration
Base Address 0x40040000
Size 0x4000
Slave Num MMIO0

Register Name	Address	Permission	Description
GPIO_INTR_CAUSE	0x40041000	FULL	Interrupt port cause register
GPIO_DFT_IO_TEST	0x40041010	FULL	IO SELF TEST control register for DfT purposes only

5.1 PRT 0

Register Name	Address	Permission	Description
GPIO_PRT0_DR	0x40040000	FULL	Port output data register
GPIO_PRT0_PS	0x40040004	FULL	Port IO pad state register
GPIO_PRT0_PC	0x40040008	FULL	Port configuration register Note:PORT_HYST_TRIM PORT_SLEW_CTL are not available for this register
GPIO_PRT0_INTR_CFG	0x4004000C	FULL	Port interrupt configuration register
GPIO_PRT0_INTR	0x40040010	FULL	Port interrupt status register
GPIO_PRT0_PC2	0x40040018	FULL	Port configuration register 2
GPIO_PRT0_DR_SET	0x40040040	FULL	Port output data set register
GPIO_PRT0_DR_CLR	0x40040044	FULL	Port output data clear register
GPIO_PRT0_DR_INV	0x40040048	FULL	Port output data invert register

5.2 PRT 1

Register Name	Address	Permission	Description
GPIO_PRT1_DR	0x40040100	FULL	Port output data register Note:DATA3 DATA4 DATA5 DATA6 DATA7 are not available for this register
GPIO_PRT1_PS	0x40040104	FULL	Port IO pad state register Note:DATA3 DATA4 DATA5 DATA6 DATA7 are not available for this register
GPIO_PRT1_PC	0x40040108	FULL	Port configuration register Note:DM3 DM4 DM5 DM6 DM7 PORT_HYST_TRIM PORT_SLEW_CTL are not available for this register
GPIO_PRT1_INTR_CFG	0x4004010C	FULL	Port interrupt configuration register Note:EDGE3_SEL EDGE4_SEL EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register
GPIO_PRT1_INTR	0x40040110	FULL	Port interrupt status register Note:DATA3 DATA4 DATA5 DATA6 DATA7 PS_DATA3 PS_DATA4 PS_DATA5 PS_DATA6 PS_DATA7 are not available for this register
GPIO_PRT1_PC2	0x40040118	FULL	Port configuration register 2 Note:INP_DIS3 INP_DIS4 INP_DIS5 INP_DIS6 INP_DIS7 are not available for this register
GPIO_PRT1_DR_SET	0x40040140	FULL	Port output data set register
GPIO_PRT1_DR_CLR	0x40040144	FULL	Port output data clear register
GPIO_PRT1_DR_INV	0x40040148	FULL	Port output data invert register

5.3 PRT 2

Register Name	Address	Permission	Description
GPIO_PRT2_DR	0x40040200	FULL	Port output data register Note:DATA3 DATA4 DATA5 DATA6 DATA7 are not available for this register
GPIO_PRT2_PS	0x40040204	FULL	Port IO pad state register Note:DATA3 DATA4 DATA5 DATA6 DATA7 are not available for this register
GPIO_PRT2_INTR_CFG	0x4004020C	FULL	Port interrupt configuration register Note:EDGE3_SEL EDGE4_SEL EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register

Register Name	Address	Permission	Description
GPIO_PRT2_INTR	0x40040210	FULL	Port interrupt status register Note:DATA3 DATA4 DATA5 DATA6 DATA7 PS_DATA3 PS_DATA4 PS_DATA5 PS_DATA6 PS_DATA7 are not available for this register
GPIO_PRT2_DR_SET	0x40040240	FULL	Port output data set register
GPIO_PRT2_DR_CLR	0x40040244	FULL	Port output data clear register
GPIO_PRT2_DR_INV	0x40040248	FULL	Port output data invert register

5.4 Register Details

5.4.1 GPIO_INTR_CAUSE

Description: Interrupt port cause register
Address: 0x40041000
Offset: 0x1000
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					PORT_INT [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	PORT_INT	R	W	0	Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects 'interrupts_gpio[i]' for IO port i). The register is used when the system uses a shared/combined interrupt line 'interrupt_gpio'. The SW ISR reads the register to determine which IO port(s) is responsible for the shared/combined interrupt line 'interrupt_gpio'. Once, the IO port(s) is determined, the IO port's INTR register is read to determine the IO pad(s) in the IO port that caused the interrupt.

5.4.2 GPIO_DFT_IO_TEST

Description: IO SELF TEST control register for DfT purposes only
Address: 0x40041010
Offset: 0x1010
Retention: Retained
IsDeepSleep: No
Comment: This register is used to significantly reduce the test time for IO cells. It also avoids the need to develop a large amount of chip specific functional test vectors.
With ATPG it is not possible to get full stuck-at fault coverage for some IO cell inputs ('hld_ovr, oe_n, analog_en, analog_sel, analog_pol'). This register gives direct controllability on those inputs of all IO cells by bypassing the functional paths. That allows generic (not chip specific) ROOS code (also SWD IO cells are included) to get DfT fault-coverage for these signals. This register is used in conjunction with the GPIO.PC.dm[2:0], GPIO.DR.out and SRSS.CORE.PWR_STOP.FREEZE for control and results are observed through GPIO.PS.data.
Only one IO cell on the whole chip gets IO_TEST_0 and only one gets IO_TEST_1 and default values of IO_TEST_0 is '0' and IO_TEST_1 is '1'. Also only one IO cell on the whole chip gets assigned ADFT-0 and only one gets assigned ADFT-1. All four IO_TEST_0/1 and ADFT-0/1 pins are assigned in the product pin spreadsheet.
Default: 0x2020200

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						DFT_IO_TEST_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			DFT_ANA_POL_0 [12:12]	DFT_ANA_SEL_0 [11:11]	DFT_ANALOG_EN_0 [10:10]	DFT_OE_N_0 [9:9]	DFT_HLD_OVR_0 [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			DFT_ANA_POL_1 [20:20]	DFT_ANA_SEL_1 [19:19]	DFT_ANALOG_EN_1 [18:18]	DFT_OE_N_1 [17:17]	DFT_HLD_OVR_1 [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			DFT_ANA_POL_2 [28:28]	DFT_ANA_SEL_2 [27:27]	DFT_ANALOG_EN_2 [26:26]	DFT_OE_N_2 [25:25]	DFT_HLD_OVR_2 [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	DFT_IO_TEST_MODE	RW	R	0	DfT IO SELF TEST mode:
	OFF			0	Functional mode: disables the DfT IO SELF TEST; none of the 'DFT_*' control signals from this register control the IO cells.
	TEST_ADFT			1	select this mode during ADFT testing to control 'hld_ovr/oe_n/ analog_sel/ analog_pol/ analog_en' signals of IO cells as below: the ADFT-0 assigned IO cell connects to: DFT_*_0; the ADFT-1 assigned IO cell connects to: DFT_*_1; All other IO cells connect to: DFT_*_2;

Bits	Name	SW	HW	Default or Enum	Description
	TEST_ANA			2	select this mode for testing analog switches to control 'hld_ovr/oe_n/analog_en/analog_sel/analog_pol' signals of IO cells as below: the IO_TEST_0 assigned IO cell connects to: DFT_*_0; the IO_TEST_1 assigned IO cell connects to: DFT_*_1; All other IO cells connect to: DFT_*_2;
	TEST_GEN			3	select this mode for generic testing to control 'hld_ovr/oe_n/analog_en/analog_sel/analog_pol' signals of IO cells as below: All IO cells connect to: DFT_*_2;
8	DFT_HLD_OVR_0	RW	R	0	'hld_ovr' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'hld_ovr' of the ADFT-0 assigned IO cell. TEST_ANA: Connects to 'hld_ovr' of the IO_TEST_0 assigned IO cell. TEST_GEN: not used.
9	DFT_OE_N_0	RW	R	1	'oe_n' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'oe_n' of the ADFT-0 assigned IO cell. TEST_ANA: Connects to 'oe_n' of the IO_TEST_0 assigned IO cell. TEST_GEN: not used.
10	DFT_ANALOG_EN_0	RW	R	0	'analog_en' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_en' of the ADFT-0 assigned IO cell. TEST_ANA: Connects to 'analog_en' of the IO_TEST_0 assigned IO cell. TEST_GEN: not used.
11	DFT_ANA_SEL_0	RW	R	0	'analog_sel' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_sel' of the ADFT-0 assigned IO cell. TEST_ANA: Connects to 'analog_sel' of the IO_TEST_0 assigned IO cell. TEST_GEN: not used.
12	DFT_ANA_POL_0	RW	R	0	'analog_pol' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_pol' of the ADFT-0 assigned IO cell. TEST_ANA: Connects to 'analog_pol' of the IO_TEST_0 assigned IO cell. TEST_GEN: not used.
16	DFT_HLD_OVR_1	RW	R	0	'hld_ovr' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'hld_ovr' of the ADFT-1 assigned IO cell. TEST_ANA: Connects to 'hld_ovr' of the IO_TEST_1 assigned IO cell. TEST_GEN: not used.
17	DFT_OE_N_1	RW	R	1	'oe_n' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'oe_n' of the ADFT-1 assigned IO cell. TEST_ANA: Connects to 'oe_n' of the IO_TEST_1 assigned IO cell. TEST_GEN: not used.

Bits	Name	SW	HW	Default or Enum	Description
18	DFT_ANALOG_EN_1	RW	R	0	'analog_en' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_en' of the ADFT-1 assigned IO cell. TEST_ANA: Connects to 'analog_en' of the IO_TEST_1 assigned IO cell. TEST_GEN: not used.
19	DFT_ANA_SEL_1	RW	R	0	'analog_sel' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_sel' of the ADFT-1 assigned IO cell. TEST_ANA: Connects to 'analog_sel' of the IO_TEST_1 assigned IO cell. TEST_GEN: not used.
20	DFT_ANA_POL_1	RW	R	0	'analog_pol' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_pol' of the ADFT-1 assigned IO cell. TEST_ANA: Connects to 'analog_pol' of the IO_TEST_1 assigned IO cell. TEST_GEN: not used.
24	DFT_HLD_OVR_2	RW	R	0	'hld_ovr' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'hld_ovr' of all IO cells other than ADFT-0/1 . TEST_ANA: Connects to 'hld_ovr' of all IO cells other than IO_TEST_0/1. TEST_GEN: Connects to 'hld_ovr' of all IO cells.
25	DFT_OE_N_2	RW	R	1	'oe_n' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'oe_n' of all IO cells other than ADFT-0/1. TEST_ANA: Connects to 'oe_n' of all IO cells other than IO_TEST_0/1. TEST_GEN: Connects to 'oe_n' of all IO cells
26	DFT_ANALOG_EN_2	RW	R	0	'analog_en' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_en' of all IO cells other than ADFT-0/1. TEST_ANA: DFT_ANALOG_EN_2 && DM[0] connects to 'analog_en' of all IO cells other than IO_TEST_0/1. TEST_GEN: Connects to 'analog_en' of all IO cells
27	DFT_ANA_SEL_2	RW	R	0	'analog_sel' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_sel' of all IO cells other than ADFT-0/1. TEST_ANA: Connects to 'analog_sel' of all IO cells other than IO_TEST_0/1. TEST_GEN: Connects to 'analog_sel' of all IO cells.
28	DFT_ANA_POL_2	RW	R	0	'analog_pol' DfT control for IO cells depending on DFT_IO_TEST_MODE as given below. TEST_ADFT: Connects to 'analog_pol' of all IO cells other than ADFT-0/1. TEST_ANA: Connects to 'analog_pol' of all IO cells other than IO_TEST_0/1. TEST_GEN: Connects to 'analog_pol' of all IO cells.

5.4.3 PRT

5.4.3.1 GPIO_PRT_DR

Description: Port output data register
Address: 0x40040000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Used to read and write the output data for the IO pads in the port. A DR register write changes the output data to the written value. A DR register read reflects the output data (and not the current state of the input data for the IO pads). Using this DR register, Read-Modify-Write sequences are safely performed on a port with some IO pads configured as inputs.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA7 [7:7]	DATA6 [6:6]	DATA5 [5:5]	DATA4 [4:4]	DATA3 [3:3]	DATA2 [2:2]	DATA1 [1:1]	DATA0 [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	DATA0	RW	RW	0	IO pad 0 output data.
1	DATA1	RW	RW	0	IO pad 1 output data.
2	DATA2	RW	RW	0	IO pad 2 output data.
3	DATA3	RW	RW	0	IO pad 3 output data.
4	DATA4	RW	RW	0	IO pad 4 output data.
5	DATA5	RW	RW	0	IO pad 5 output data.
6	DATA6	RW	RW	0	IO pad 6 output data.
7	DATA7	RW	RW	0	IO pad 7 output data.

5.4.3.2 GPIO_PRT_PS

Description: Port IO pad state register
Address: 0x40040004
Offset: 0x4
Retention: Not Retained
IsDeepSleep: No
Comment: Used to read. Writes to this register have no effect. If the drive mode for the pin is set to high Z Analog, the state will read 0 independent of the voltage on the pin.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA7 [7:7]	DATA6 [6:6]	DATA5 [5:5]	DATA4 [4:4]	DATA3 [3:3]	DATA2 [2:2]	DATA1 [1:1]	DATA0 [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							FLT_DATA [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	DATA0	R	W	0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin.
1	DATA1	R	W	0	IO pad 1 state.
2	DATA2	R	W	0	IO pad 2 state.
3	DATA3	R	W	0	IO pad 3 state.
4	DATA4	R	W	0	IO pad 4 state.
5	DATA5	R	W	0	IO pad 5 state.
6	DATA6	R	W	0	IO pad 6 state.
7	DATA7	R	W	0	IO pad 7 state.
8	FLT_DATA	R	W	0	Reads of this register return the logical state of the filtered pin.

5.4.3.3 GPIO_PRT_PC

Description: Port configuration register
Address: 0x40040008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment: Configures the output drive and input buffer state for each pin, and the slew rate and input threshold selection for the whole port. One register is provided per port.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	DM5 [15:15]	DM4 [14:12]			DM3 [11:9]			DM2 [8:8]

Bits	23	22	21	20	19	18	17	16
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT _SLOW [25:25]	PORT _VTRIP _SEL [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	DM0	RW	R	0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus.
	OFF			0	Mode 0 (analog mode): Output buffer off (high Z). Input buffer off.
	INPUT			1	Mode 1: Output buffer off (high Z). Input buffer on.
	0_PU			2	Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. For GPIOV1P2_I2C, Strong pull down only.
	PD_1			3	Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. For GPIOV1P2_I2C: Weak pull down only.
	0_Z			4	Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. For GPIOV1P2_I2C, Strong pull down only.
	Z_1			5	Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. Illegal for GPIOV1P2_I2C
	0_1			6	Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. For GPIOV1P2_I2C, Strong pull down only.
	PD_PU			7	Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on. For GPIOV1P2_I2C: Weak pull down only.
3:5	DM1	RW	R	0	The GPIO drive mode for IO pad 1.
6:8	DM2	RW	R	0	The GPIO drive mode for IO pad 2.
9:11	DM3	RW	R	0	The GPIO drive mode for IO pad 3.
12:14	DM4	RW	R	0	The GPIO drive mode for IO pad 4.

Bits	Name	SW	HW	Default or Enum	Description
15:17	DM5	RW	R	0	The GPIO drive mode for IO pad 5.
18:20	DM6	RW	R	0	The GPIO drive mode for IO pad 6.
21:23	DM7	RW	R	0	The GPIO drive mode for IO pad 7.
24	PORT_VTRIP_SEL	RW	R	0	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. For GPIOV1P2 and GPIOV1P_I2C cells, PC.PORT_VTRIP_SEL is unused. Refer to DS register
25	PORT_SLOW	RW	R	0	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow.
30:31	PORT_IB_MODE_SEL	RW	R	0	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): '0'/'2': CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') '1'/'3': vcchib. For GPIO_OVTv2 and SIOv2 IO cells: '0': CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') '1': vcchib. '2': OVT. '3': Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). For GPIOV1P2 and GPIOV1P2_I2C cells, PC.PORT_IB_MODE_SEL unused. Refer to DS register.

5.4.3.4 GPIO_PRT_INTR_CFG

Description: Port interrupt configuration register
Address: 0x4004000C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment: This register configures the IRQ configuration for all pins in a port, with the IRQ type being individually pin-configurable.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	EDGE0_SEL	RW	R	0	Sets which edge will trigger an IRQ for IO pad 0.
	DISABLE			0	Disabled
	RISING			1	Rising edge
	FALLING			2	Falling edge
	BOTH			3	Both rising and falling edges
2:3	EDGE1_SEL	RW	R	0	Sets which edge will trigger an IRQ for IO pad 1.
4:5	EDGE2_SEL	RW	R	0	Sets which edge will trigger an IRQ for IO pad 2.
6:7	EDGE3_SEL	RW	R	0	Sets which edge will trigger an IRQ for IO pad 3.
8:9	EDGE4_SEL	RW	R	0	Sets which edge will trigger an IRQ for IO pad 4.
10:11	EDGE5_SEL	RW	R	0	Sets which edge will trigger an IRQ for IO pad 5.
12:13	EDGE6_SEL	RW	R	0	Sets which edge will trigger an IRQ for IO pad 6.
14:15	EDGE7_SEL	RW	R	0	Sets which edge will trigger an IRQ for IO pad 7.
16:17	FLT_EDGE_SEL	RW	R	0	Same for the glitch filtered pin (selected by FLT_SEL).
	DISABLE			0	Disabled
	RISING			1	Rising edge
	FALLING			2	Falling edge
	BOTH			3	Both rising and falling edges
18:20	FLT_SEL	RW	R	0	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt.

5.4.3.5 GPIO_PRT_INTR

Description: Port interrupt status register
Address: 0x40040010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: An interrupt cause is cleared (set to '0') by writing a '1' to the corresponding bit field. It is not recommended to write 0xff to clear all interrupt causes, as a new interrupt cause may have occurred between reading the register and clearing. Note that the interrupt cause fields and the associated interrupt provide Hibernate functionality (interrupt causes can be set to '1' and the interrupt can be activated in Hibernate power mode). The PS_DATA fields reflect the logical IO pad states of the port (also found in the PS register).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA7 [7:7]	DATA6 [6:6]	DATA5 [5:5]	DATA4 [4:4]	DATA3 [3:3]	DATA2 [2:2]	DATA1 [1:1]	DATA0 [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							FLT_DATA [8:8]

Bits	23	22	21	20	19	18	17	16
Name	PS_DATA7 [23:23]	PS_DATA6 [22:22]	PS_DATA5 [21:21]	PS_DATA4 [20:20]	PS_DATA3 [19:19]	PS_DATA2 [18:18]	PS_DATA1 [17:17]	PS_DATA0 [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:25]							PS_FLT_DATA [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	DATA0	RW1C	A	0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt.
1	DATA1	RW1C	A	0	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt.
2	DATA2	RW1C	A	0	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt.
3	DATA3	RW1C	A	0	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt.
4	DATA4	RW1C	A	0	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt.
5	DATA5	RW1C	A	0	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt.
6	DATA6	RW1C	A	0	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt.
7	DATA7	RW1C	A	0	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt.
8	FLT_DATA	RW1C	A	0	Deglitched interrupt pending (selected by FLT_SEL).
16	PS_DATA0	R	W	0	`
17	PS_DATA1	R	W	0	N/A
18	PS_DATA2	R	W	0	N/A
19	PS_DATA3	R	W	0	N/A
20	PS_DATA4	R	W	0	N/A
21	PS_DATA5	R	W	0	N/A
22	PS_DATA6	R	W	0	N/A

Bits	Name	SW	HW	Default or Enum	Description
23	PS_DATA7	R	W	0	N/A
24	PS_FLT_DATA	R	W	0	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation.

5.4.3.6 GPIO_PRT_PC2

Description: Port configuration register 2
Address: 0x40040018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment: Configures the input disable for each pin.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	INP_DIS7 [7:7]	INP_DIS6 [6:6]	INP_DIS5 [5:5]	INP_DIS4 [4:4]	INP_DIS3 [3:3]	INP_DIS2 [2:2]	INP_DIS1 [1:1]	INP_DIS0 [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	INP_DIS0	RW	R	0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver.
1	INP_DIS1	RW	R	0	Disables the input buffer for IO pad 1.
2	INP_DIS2	RW	R	0	Disables the input buffer for IO pad 2.
3	INP_DIS3	RW	R	0	Disables the input buffer for IO pad 3.
4	INP_DIS4	RW	R	0	Disables the input buffer for IO pad 4.
5	INP_DIS5	RW	R	0	Disables the input buffer for IO pad 5.
6	INP_DIS6	RW	R	0	Disables the input buffer for IO pad 6.
7	INP_DIS7	RW	R	0	Disables the input buffer for IO pad 7.

5.4.3.7 GPIO_PRT_DR_SET

Description: Port output data set register
Address: 0x40040040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment: Used to set output data of specific IO pads in the corresponding port to '1', without affecting the output data of the other IO pads in the port. A DR_SET register read returns the same value as a DR register read.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	DATA	RW	A	0	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'.

5.4.3.8 GPIO_PRT_DR_CLR

Description: Port output data clear register
Address: 0x40040044
Offset: 0x44
Retention: Retained
IsDeepSleep: No
Comment: Used to clear output data of specific IO pads in the corresponding port to '0', without affecting the output data of the other IO pads in the port. A DR_CLR register read returns the same value as a DR register read.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	DATA	RW	A	0	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'.

5.4.3.9 GPIO_PRT_DR_INV

Description: Port output data invert register
Address: 0x40040048
Offset: 0x48
Retention: Retained
IsDeepSleep: No
Comment: Used to invert output data of specific IO pads in the corresponding port, without affecting the output data of the other IO pads in the port. A DR_INV register read returns the same value as a DR register read.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	DATA	RW	A	0	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0').

6 HSIOM

Description High Speed IO Matrix (HSIOM)
Base Address 0x40020000
Size 0x4000
Slave Num MMIO0

6.1 PRT 0

Register Name	Address	Permission	Description
HSIOM_PORT_SEL0	0x40020000	FULL	Port selection register

6.2 PRT 1

Register Name	Address	Permission	Description
HSIOM_PORT_SEL1	0x40020100	FULL	Port selection register Note:IO3_SEL IO4_SEL IO5_SEL IO6_SEL IO7_SEL are not available for this register

6.3 PRT 2

Register Name	Address	Permission	Description
HSIOM_PORT_SEL2	0x40020200	FULL	Port selection register Note:IO3_SEL IO4_SEL IO5_SEL IO6_SEL IO7_SEL are not available for this register

6.4 Register Details

6.4.1 PRT

6.4.1.1 HSIOM_PORT_SEL

Description: Port selection register
Address: 0x40020000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Note: these fields are HW:W purely for DfT observe functionality, not for functional reasons.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	IO0_SEL	RW	RW	0	Selects connection for IO pad 0 route.
	GPIO			0	SW controlled GPIO.
	GPIO_DSI			1	SW controlled 'out', DSI controlled 'oe_n'.
	DSI_DSI			2	DSI controlled 'out' and 'oe_n'.
	DSI_GPIO			3	DSI controlled 'out', SW controlled 'oe_n'.
	CSD_SENSE			4	CapSense sense connection (analog mode)
	CSD_SHIELD			5	CapSense shield connection (analog mode)
	AMUXA			6	AMUXBUS A connection.
	AMUXB			7	AMUXBUS B connection.
	ACT_0			8	Chip specific Active source 0 connection.
	ACT_1			9	Chip specific Active source 1 connection.
	ACT_2			10	Chip specific Active source 2 connection.
	ACT_3			11	Chip specific Active source 3 connection.
	LCD_COM			12	LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block exists, is enabled, and is properly configured).
	LCD_SEG			13	LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).
	DS_0			12	Chip specific DeepSleep source 0 connection.
	DS_1			13	Chip specific DeepSleep source 1 connection.
	DS_2			14	Chip specific DeepSleep source 2 connection.
	DS_3			15	Chip specific DeepSleep source 3 connection.
4:7	IO1_SEL	RW	RW	0	Selects connection for IO pad 1 route.
8:11	IO2_SEL	RW	RW	0	Selects connection for IO pad 2 route.
12:15	IO3_SEL	RW	RW	0	Selects connection for IO pad 3 route.
16:19	IO4_SEL	RW	RW	0	Selects connection for IO pad 4 route.
20:23	IO5_SEL	RW	RW	0	Selects connection for IO pad 5 route.

Bits	Name	SW	HW	Default or Enum	Description
24:27	IO6_SEL	RW	RW	0	Selects connection for IO pad 6 route.
28:31	IO7_SEL	RW	RW	0	Selects connection for IO pad 7 route.

7 HVSS

Description High Voltage Subsystem
Base Address 0x40060000
Size 0x10000
Slave Num MMIO0

Register Name	Address	Permission	Description
HVSS_HVREG_STATUS	0x40060000	FULL	HVREG Status
HVSS_HVREG_BIST	0x40060004	FULL	HVREG Bist
HVSS_RDIV_CTL	0x40060010	FULL	Resistor Attenuator Control
HVSS_LIN_CTL	0x40060020	FULL	LIN Phy Control
HVSS_LIN_TIMER	0x40060024	FULL	LIN Timer Control
HVSS_LIN_STATUS	0x40060028	FULL	LIN Status
HVSS_LIN_BIST	0x4006002C	FULL	LIN BIST Control
HVSS_LIN_INTR	0x40060030	FULL	LIN Interrupt Request Register
HVSS_LIN_INTR_SET	0x40060034	FULL	LIN Interrupt set register
HVSS_LIN_INTR_MASK	0x40060038	FULL	LIN Interrupt mask register
HVSS_LIN_INTR_MASKED	0x4006003C	FULL	LIN Interrupt masked register
HVSS_HVSS_DDFT	0x40060040	FULL	HVSS DDFT Control
HVSS_HVREG_TRIM	0x4006FF00	FULL	HVREG Trim Settings, first byte
HVSS_LIN_TRIM	0x4006FF04	FULL	LIN Trim Settings

7.1 Register Details

7.1.1 HVSS_HVREG_STATUS

Description: HVREG Status
Address: 0x40060000
Offset: 0x0
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							PWR_GOOD [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	PWR_GOOD	R	W	0	High if regulator is settled and operating within normal limits

7.1.2 HVSS_HVREG_BIST

Description: HVREG Bist
Address: 0x40060004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			HVREG_DDFT [4:4]	None [3:3]	HVREG_ADFT [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							EN_BURN_IN [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	HVREG_ADFT	RW	R	0	Controls ADFT switches
	NORMAL			0	Normal operation, amuxbus_a=Z
	BIAS_CIRCUIT_CURRENT_MONITOR			1	Bias current monitor (NMOS drain) on amuxbus_a
	RESERVED_2			2	N/A
	RESERVED_3			3	N/A
	RESERVED_4			4	N/A
	RESERVED_5			5	N/A
	RESERVED_6			6	N/A
	RESERVED_7			7	N/A
4	HVREG_DDFT	RW	R	0	Enable HVREG DDFT outputs to DDFT interface when '1' (PG on ddft0, '0' on ddft1)
8	EN_BURN_IN	RW	R	0	Enable burn-in test mode with Vccd(1.8V) domain

7.1.3 HVSS_RDIV_CTL

Description: Resistor Attenuator Control
Address: 0x40060010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		RDIV _SCALE_1 [5:5]	RDIV _SCALE_0 [4:4]	None [3:3]	RDIV_ACT _EN [2:2]	RDIV_EN_1 [1:1]	RDIV_EN_0 [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	RDIV_EN_0	RW	R	0	Enable VS0 0=Disabled 1=Enabled during power modes selected by RDIVacten
1	RDIV_EN_1	RW	R	0	Enable VS1 0=Disabled 1=Enabled during power modes selected by RDIVacten
2	RDIV_ACT_EN	RW	R	0	Power modes where RDIV is enabled 0=Enable in Active and Deep-Sleep modes 1=Enable in Active mode only
4	RDIV_SCALE_0	RW	R	0	VS0 attenuation 0=16X attenuation 1=24X attenuation
5	RDIV_SCALE_1	RW	R	0	VS1 attenuation 0=16X attenuation 1=24X attenuation

7.1.4 HVSS_LIN_CTL

Description: LIN Phy Control
Address: 0x40060020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			RF _DETECT [4:4]	None [3:3]	LIN_MODE [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							USE_ALT_I NTERFACE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	LIN_EN [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	LIN_MODE	RW	R	0	N/A
	DISABLED			0	OFF (TX off, Rx off, Bias Circuits Off), LIN pin recessive
	SLEEP			1	TX off, RX on, LIN pin recessive (typically used in deep-sleep)
	STANDBY			2	TX off, RX off, Bias circuits on (faster turn-on, not normally used)
	DIAGNOSIS			3	TX on, RX on, TX w/weak pull-down (broken wire detect diag)
	NORMAL_1_0			4	TX on, RX on, 1.0V/us TX edge rate, may not meet all parameters of LIN spec at some operating conditions
	NORMAL_1_5			5	TX on, RX on, 1.5V/us TX edge rate, meets all parameters of LIN spec
	NORMAL_2_0			6	TX on, RX on, 2.0V/us TX edge rate, may not meet all parameters of LIN spec at some operating conditions
	FAST			7	Fast mode (non-lin compliant, up to 100kb/s capable)
4	RF_DETECT	RW	R	0	Renamed from SL_ROUND. 0=off; 1=on, reduce impact on LIN driver from incoming EMI.
8	USE_ALT_INTERFACE	RW	R	0	Selects Primary or Alternate interface for Phy. The primary use is to enable compliance testing by directly manipulating the Phy interface through GPIOs. 0 = Primary interface (connected to internal LIN controller through HSIOM) 1 = Alternate interface (connected to GPIOs through HSIOM)
31	LIN_EN	RW	R	0	Master enable of the LIN interface. 0=Interface is reset and LIN pin is in Hi-Z state 1=Enable the LIN interface

7.1.5 HVSS_LIN_TIMER

Description: LIN Timer Control
Address: 0x40060024
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	WAKEUP_TIMER [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				WAKEUP_TIMER [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	FAULT_TIMER [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	FAULT_TIMER_EN [31:31]	WAKEUP_TIMER_EN [30:30]	None [29:28]		FAULT_TIMER [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:11	WAKEUP_TIMER	RW	R	0	Number of LF_CLK edges before wakeup interrupt is triggered
16:27	FAULT_TIMER	RW	R	0	Number of LF_CLK edges before fault interrupt is triggered
30	WAKEUP_TIMER_EN	RW	R	0	Wakeup timer is running, required for full LIN compatibility if using Deep-sleep power mode
31	FAULT_TIMER_EN	RW	R	0	Dominant state fault timer is running, req'd for full LIN compatibility

7.1.6 HVSS_LIN_STATUS

Description: LIN Status
Address: 0x40060028
Offset: 0x28
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							LIN_RXD [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	LIN_RXD	R	W	0	Current state of LIN pin, except in lin_mode 0 or 2, when RXD = 1.

7.1.7 HVSS_LIN_BIST

Description: LIN BIST Control
Address: 0x4006002C
Offset: 0x2C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		LIN_DFT_START [5:5]	LIN_DDFT [4:4]	None [3:3]	LIN_ADFT [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	LIN_ADFT	RW	R	0	Enables Test Modes
	NORMAL			0	Normal Operation (DFT disabled), amuxbus_a=Z, dft<1:0>=0
	CURRENT_MONITOR_LWAVE			1	amuxbus_a=Iwave (PMOS drain), dft<1:0>=0
	VOLTAGE_MONITOR_ERRBUFF			2	amuxbus_a=ErrBuff, dft<1:0>=0
	WEAK OUTFET			3	OUTFET = 1/10, (amuxbus_a=Z, dft<1:0>=0)
	CURRENT_MONITOR_FOR BIAS_CKT			4	amuxbus_a=Ibias monitor (PMOS drain), dft<1:0>=0
	SL_ROUND			5	0=Normal, 1=More moderate (rounded) edge for lower EMI
	DDFT = OSC			6	amuxbus_a = Z dft<1> = LIN_DFT_START, dft<0> = LIN_OSC
	DDFT = DELAY			7	amuxbus_a = Z dft<1> = LIN_DFT_START, dft<0> = LIN_DELAY
4	LIN_DDFT	RW	R	0	Enable LIN DDFT outputs to DDFT interface ddft1 = dft<1>, ddft0 = dft<0>
5	LIN_DFT_START	RW	R	0	Delay line input

7.1.8 HVSS_LIN_INTR

Description: LIN Interrupt Request Register
Address: 0x40060030
Offset: 0x30
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						FAULT [1:1]	WAKEUP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKEUP	RW1C	RW1S	0	Master asserted dominant state wakeup (wakeup timer timeout)
1	FAULT	RW1C	RW1S	0	Interface asserted state for too long (dominant state timeout)

7.1.9 HVSS_LIN_INTR_SET

Description: LIN Interrupt set register
Address: 0x40060034
Offset: 0x34
Retention: Not Retained
IsDeepSleep: No
Comment: This register asserts an interrupt - used for s/w debugging. A read returns the content of the INTR register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						FAULT [1:1]	WAKEUP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKEUP	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
1	FAULT	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.

7.1.10 HVSS_LIN_INTR_MASK

Description: LIN Interrupt mask register
Address: 0x40060038
Offset: 0x38
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						FAULT [1:1]	WAKEUP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKEUP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
1	FAULT	RW	R	0	Mask bit for corresponding bit in interrupt request register.

7.1.11 HVSS_LIN_INTR_MASKED

Description: LIN Interrupt masked register
Address: 0x4006003C
Offset: 0x3C
Retention: Not Retained
IsDeepSleep: No
Comment: If the value is not zero then the CSD interrupt signal to the NVIC is high. When read, this register reflects a bitwise AND between the interrupt request and mask registers.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						FAULT [1:1]	WAKEUP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKEUP	R	W	0	Logical and of corresponding request and mask bits.
1	FAULT	R	W	0	Logical and of corresponding request and mask bits.

7.1.12 HVSS_HVSS_DDFT

Description: HVSS DDFT Control
Address: 0x40060040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							LSOUT _DDFT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	LSOUT_DDFT	RW	R	0	Enable LSOUT DDFT output to DDFT interface ddft1 = lsout_ddft, ddft0 = 0

7.1.13 HVSS_HVREG_TRIM

Description: HVREG Trim Settings, first byte
Address: 0x4006FF00
Offset: 0xFF00
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	TRIM	RW	R	0	Trim for VDDD output level, Currently using the 4 LSB 3:0, bits 7:4 are reserved. Nominal values: Default = 4'b0000 => 3.18V, 4'b1111 => 3.78V. Step size = 40 mV per code.

7.1.14 HVSS_LIN_TRIM

Description: LIN Trim Settings
Address: 0x4006FF04
Offset: 0xFF04
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SLEW_CTL [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	SLEW_CTL	RW	R	0	SLEW_CTL trim for LIN TX_DRV, (bits 3:0 used, 7:4 reserved))

8 LIN

Description LIN
Base Address 0x402D0000
Size 0x10000
Slave Num MMIO1

Register Name	Address	Permission	Description
LIN0_ERROR_CTL	0x402D0000	FULL	Error control
LIN0_TEST_CTL	0x402D0004	FULL	Test control

8.1 CH 0

Register Name	Address	Permission	Description
LIN0_CH0_CTL0	0x402D8000	FULL	Control 0
LIN0_CH0_CTL1	0x402D8004	FULL	Control 1
LIN0_CH0_STATUS	0x402D8008	FULL	Status
LIN0_CH0_CMD	0x402D8010	FULL	Command
LIN0_CH0_TX_RX_STATUS	0x402D8060	FULL	TX/RX status
LIN0_CH0_PID_CHECKSUM	0x402D8080	FULL	PID and checksum
LIN0_CH0_DATA0	0x402D8084	FULL	Response data 0
LIN0_CH0_DATA1	0x402D8088	FULL	Response data 1
LIN0_CH0_INTR	0x402D80C0	FULL	Interrupt
LIN0_CH0_INTR_SET	0x402D80C4	FULL	Interrupt set
LIN0_CH0_INTR_MASK	0x402D80C8	FULL	Interrupt mask
LIN0_CH0_INTR_MASKED	0x402D80CC	FULL	Interrupt masked

8.2 CH 1

Register Name	Address	Permission	Description
LIN0_CH1_CTL0	0x402D8100	FULL	Control 0
LIN0_CH1_CTL1	0x402D8104	FULL	Control 1
LIN0_CH1_STATUS	0x402D8108	FULL	Status
LIN0_CH1_CMD	0x402D8110	FULL	Command
LIN0_CH1_TX_RX_STATUS	0x402D8160	FULL	TX/RX status
LIN0_CH1_PID_CHECKSUM	0x402D8180	FULL	PID and checksum
LIN0_CH1_DATA0	0x402D8184	FULL	Response data 0
LIN0_CH1_DATA1	0x402D8188	FULL	Response data 1
LIN0_CH1_INTR	0x402D81C0	FULL	Interrupt
LIN0_CH1_INTR_SET	0x402D81C4	FULL	Interrupt set
LIN0_CH1_INTR_MASK	0x402D81C8	FULL	Interrupt mask
LIN0_CH1_INTR_MASKED	0x402D81CC	FULL	Interrupt masked

8.3 Register Details

8.3.1 LIN_ERROR_CTL

Description: Error control
Address: 0x402D0000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: This register supports error functionality: it enables HW injected channel transmitter errors. The receiver should detect these errors and report these errors through activation of corresponding interrupt causes.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CH_IDX [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	TX_CHECKSUM_STOP_ERROR [23:23]	TX_CHECKSUM_ERROR [22:22]	TX_DATA_STOP_ERROR [21:21]	None [20:20]	TX_PID_STOP_ERROR [19:19]	TX_PARITY_ERROR [18:18]	TX_SYNC_STOP_ERROR [17:17]	TX_SYNC_ERROR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	CH_IDX	RW	R	0	Specifies the channel index of the channel to which HW injected channel transmitter errors applies.
16	TX_SYNC_ERROR	RW	R	0	The synchronization field is changed from 0x55 to 0x00. At the receiver, this should result in INTR.RX_HEADER_SYNC_ERROR activation.
17	TX_SYNC_STOP_ERROR	RW	R	0	The synchronization field STOP bits are inverted to '0'. At the receiver, this should result in INTR.RX_HEADER_SYNC_ERROR or INTR.RX_HEADER_FRAME_ERROR activation.
18	TX_PARITY_ERROR	RW	R	0	In LIN mode, the PID parity bit P[1] is inverted from !(ID[5] ^ ID[4] ^ ID[3] ^ ID[1]) to (ID[5] ^ ID[4] ^ ID[3] ^ ID[1]). At the receiver, this should result in INTR.RX_HEADER_PARITY_ERROR activation. In UART mode, a data field's parity bit is inverted.
19	TX_PID_STOP_ERROR	RW	R	0	The PID field STOP bits are inverted to '0'. At the receiver, this should result in INTR.RX_HEADER_FRAME_ERROR activation.

Bits	Name	SW	HW	Default or Enum	Description
21	TX_DATA_STOP _ERROR	RW	R	0	The data field STOP bits are inverted to '0'. At the receiver, this should result in INTR.RX_RESPONSE_FRAME_ERROR activation. Note: Used in UART mode.
22	TX_CHECKSUM_ERROR	RW	R	0	The checksum field is inverted. At the receiver, this should result in INTR.RX_RESPONSE_CHECKSUM_ERROR activation.
23	TX_CHECKSUM_STOP _ERROR	RW	R	0	The checksum field STOP bits are inverted to '0'. At the receiver, this should result in INTR.RX_RESPONSE_FRAME_ERROR activation.
31	ENABLED	RW	R	0	Error injection enable: '0': Disabled. '1': Enabled.

8.3.2 LIN_TEST_CTL

Description: Test control
Address: 0x402D0004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: This register support test functionality.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CH_IDX [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:17]							MODE [16:16]

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	CH_IDX	RW	R	0	Specifies the channel index of the channel to which test applies. The channel IO signals of channel indices CH_IDX and CH_NR-1 are connected as specified by MODE. CH_IDX should be in the range [0, CH_NR-2], as channel index CH_NR-1 is always involved in test and cannot be connected to itself. The test mode allows BOTH of the two connected channels to be tested. Note: this testing functionality simplifies SW development, but may also be used in the field to verify correct channel functionality.

Bits	Name	SW	HW	Default or Enum	Description
16	MODE	RW	R	0	Test mode: '0': Partial disconnect from IOSS. This mode's isolation allows for device test without relying on an external LIN transceiver. The IOSS 'tx' IO cell can be used to observe messages outside of the device. - tx_in[CH_IDX] = IOSS lin_tx_in[CH_IDX]. - tx_in[CH_NR-1] = IOSS lin_tx_in[CH_IDX]. - rx_in[CH_IDX] = IOSS lin_tx_in[CH_IDX]. - rx_in[CH_NR-1] = IOSS lin_tx_in[CH_IDX]. - lin_tx_out[CH_IDX] = tx_out[CH_IDX] & tx_out[CH_NR-1]. - lin_tx_out[CH_NR-1] = tx_out[CH_IDX] & tx_out[CH_NR-1]. '1': Full disconnect from IOSS (the IOSS/HSIOM should disconnect 'tx_out' from the 'tx' IO cell). This mode's isolation allows for device test without effecting an operational LIN cluster. - tx_in[CH_IDX] = lin_tx_out[CH_IDX]. - tx_in[CH_NR-1] = lin_tx_out[CH_IDX]. - rx_in[CH_IDX] = lin_tx_out[CH_IDX]. - rx_in[CH_NR-1] = lin_tx_out[CH_IDX]. - lin_tx_out[CH_IDX] = tx_out[CH_IDX] & tx_out[CH_NR-1]. - lin_tx_out[CH_NR-1] = tx_out[CH_IDX] & tx_out[CH_NR-1].
31	ENABLED	RW	R	0	Test enable: '0': Disabled. Functional mode. - tx_in[CH_IDX] = IOSS lin_tx_in[CH_IDX]. - tx_in[CH_NR-1] = IOSS lin_tx_in[CH_NR-1]. - rx_in[CH_IDX] = IOSS lin_rx_in[CH_IDX]. - rx_in[CH_NR-1] = IOSS lin_rx_in[CH_NR-1]. - lin_tx_out[CH_IDX] = tx_out[CH_IDX]. - lin_tx_out[CH_NR-1] = tx_out[CH_NR-1]. '1': Enabled. Test mode, specific test mode is specified by MODE.

8.3.3 CH

8.3.3.1 LIN_CH_CTL0

Description: Control 0
Address: 0x402D8000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x400C0101

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			AUTO_EN [4:4]	None [3:2]		STOP_BITS [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						BREAK_DELIMITER_LENGTH [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			BREAK_WAKEUP_LENGTH [20:16]				

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	FILTER_EN [30:30]	PARITY_EN [29:29]	PARITY [28:28]	BIT_ERROR_IGNORE [27:27]	None [26:25]		MODE [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	STOP_BITS	RW	R	1	STOP bit periods: '0': 1/2 bit period. '1': 1 bit period. '2': 1 1/2 bit period. '3': 2 bit periods. In LIN mode, this field should be set to '1' (the default value) . In UART mode, this field can be programmed as desired. Note: receiver STOP bit frame errors can only be detected if the number of STOP bit periods is 1 or more bit period.
4	AUTO_EN	RW	R	0	LIN transceiver auto enable: '0': Disabled. '1': Enabled. The TX_RX_STATUS.EN_OUT field is controlled by HW.

Bits	Name	SW	HW	Default or Enum	Description
8:9	BREAK_DELIMITER_LENGTH	RW	R	1	In LIN mode, this field specifies the break delimiter length: (used in header transmission, not used in header reception). '0': 1 bit period. '1': 2 bit periods (default value). '2': 3 bit periods. '3': 4 bit periods. In UART mode, this field specifies the data field size: '0': 5 bit data field. '1': 6 bit data field. '2': 7 bit data field. '3': 8 bit data field. When the data field size is less than 8 bits, the most significant (unused) bits of the DATAx.DATAy[7:0] fields should be set to '0' for the transmitter.
16:20	BREAK_WAKEUP_LENGTH	RW	R	12	Break/wakeup length (minus 1) in bit periods: '0': 1 bit period. ... '10': 11 bit periods (break length for slave nodes) ... '12': 13 bit periods (break length for master nodes) ... '30': 31 bit periods. '31': Illegal (should NOT be used!!!) This field is used for transmission/reception of BOTH break and wakeup signals. Note that these functions are mutually exclusive: - When CMD.TX_HEADER is '1', the field specifies the transmitted break field. - When CMD.TX_WAKEUP is '1', the field specifies the transmitted wakeup field. - When CMD.RX_HEADER is '1', the field specifies the to be received break field. - Otherwise, the field specifies the to be received wakeup field. Per the standard, the master wakeup duration is between 250 us and 5 ms. To support uncalibrated slaves, a slave has a detection threshold of 150 us (3 bit periods at 20 kbps). After transmission of a break or wakeup signal, the INTR.TX_BREAK_WAKEUP_DONE interrupt cause is activated. After reception of a wakeup signal, the INTR.RX_BREAK_WAKEUP_DONE interrupt cause is activated. To specify longer wakeup signals in terms of absolute time (us/ms rather than bit periods), the associated PERI clock divider value can be (temporarily) increased to make the LIN bit period longer. Note: entering bus sleep mode is achieved with the 'go-to-sleep' command.
24	MODE	RW	R	0	Mode of operation: '0': LIN mode. '1': UART mode.
	LIN			0	LIN mode.
	UART			1	UART mode.

Bits	Name	SW	HW	Default or Enum	Description
27	BIT_ERROR_IGNORE	RW	R	0	Specifies behavior on a detected bit error during header or response transmission: '0': Message transfer is aborted. '1': Message transfer is NOT aborted. Note: this field does NOT effect the reporting of the bit error through INTR/STATUS.TX_HEADER/RESPONSE_BIT_ERROR; i.e. bit errors are always reported.
28	PARITY	RW	R	0	Parity mode: '0': Even parity: even number of '1' bits (including parity). '1': Odd parity. Note: Used in UART mode only.
29	PARITY_EN	RW	R	0	Parity generation enable: '0': Disabled. No parity bit is transferred. '1': Enabled. The parity bit is transferred after the last (most significant) data field bit. Note: Used in UART mode only.
30	FILTER_EN	RW	R	1	RX filter (for 'lin_rx_in'): '0': No filter. '1': Median 3 (default value) operates on the last three 'lin_rx_in' values. The sequences '000', '001', '010' and '100' result in a filtered value '0'. The sequences '111', '110', '101' and '011' result in a filtered value '1'.
31	ENABLED	RW	R	0	Channel enable: '0': Disabled. If a channel is disabled, all non-retained MMIO registers (e.g. the TX_RX_STATUS, and INTR registers) have their fields reset to their default value. '1': Enabled.

8.3.3.2 LIN_CH_CTL1

Description: Control 1
Address: 0x402D8004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: A master node is aware of a message's checksum mode and number of data fields. Therefore, a master node can set the CHECKSUM_ENHANCED and DATA_NR fields accordingly, BEFORE the message header transmission.

A slave node needs to derive a message's checksum mode and number of data fields from the received PID field, AFTER the message header reception. The INTR.RX_HEADER_DONE interrupt cause indicates that the message header is received and PID_CHECKSUM.PID contains the received PID field. Slave node SW can use this PID field information to set CHECKSUM_ENHANCED and DATA_NR fields accordingly. A minimum message response consists of at least 1 data field, and the CHECKSUM_ENHANCED and DATA_NR fields need to be set BEFORE the receipt of the STOP bit(s) of the first data field; i.e. SW effectively has a data field transfer duration to set the fields.
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					DATA_NR [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							CHECKSUM_ENHANCED [8:8]

Bits	23	22	21	20	19	18	17	16
Name	FRAME_TIMEOUT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:26]						FRAME_TIMEOUT_SEL [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	DATA_NR	RW	R	Undefined	Number of data fields (minus 1) in the response (not including the checksum): '0': 1 data field. '1': 2 data fields. ... '7': 8 data fields. Note: master and slave nodes need to agree upon the number of data fields before message transfer. In RX_RESPONSE case, When PID (header) is received, firmware has the time of one response data byte, to modify CTL1.DATA_NR.

Bits	Name	SW	HW	Default or Enum	Description
8	CHECKSUM_ ENHANCED	RW	R	Undefined	Checksum mode: '0': Classic mode. PID field is NOT included in the checksum calculation. '1': Enhanced mode. PID field is included in the checksum calculation. This mode requires special attention when the master node transmits the header and a (different) slave node transmits the response: the slave node will use the calculated partial checksum over the received PID field as a starting point for the calculation over the to be transmitted data fields. Note: If the frame identifier ID[5:0] is 0x3c or 0x3d, the classic mode will ALWAYS be used for transmission and assumed for reception, independent of the CHECKSUM_ENHANCED value.
16:23	FRAME_TIMEOUT	RW	R	Undefined	Specifies the maximum allowed length (timeout value) for a frame, frame header or frame response in bit periods. The LIN specification prescribes to set the maximum length to 1.4x the nominal length (Theader_max = 1.4 x Theader_nom and Tresponse_max = 1.4 x Tresponse_nom). The nominal header length Theader_nom is 34 bit periods and the nominal response length Tresponse_nom is 10 * (data_nr + 1) bit periods (data_nr is the number of data fields) Note: the LIN specification specifies the following: 'Tools and tests shall check the Tframe_max (= Theader_max + Tresponse_max). Nodes shall not check this time. The receiving node of the frame shall accept the frame up to the next frame slot (i.e. next break field), even if it is longer then Tframe_max).'
24:25	FRAME_TIMEOUT_SEL	RW	R	0	Specifies the frame timeout mode: '0': No timeout functionality (default value). '1': Frame mode: detects timeout from the start of break field to checksum field STOP bits (inclusive). The minimum FRAME_TIMEOUT value is 34+20 bit periods (header and a response with 1 data field). '2': Frame header mode: detects timeout from the start of break field to PID field STOP bits (inclusive). The minimum FRAME_TIMEOUT value is 34 bit periods (header). '3': Frame response mode: detects timeout from the PID field STOP bits (exclusive) to checksum field STOP bits (the response space is included in the frame response). The minimum FRAME_TIMEOUT value is 20 bit periods (response with 1 data field).

8.3.3.3 LIN_CH_STATUS

Description: Status
Address: 0x402D8008
Offset: 0x8
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.

This is a non-retained register; setting CTL.ENABLED to '0' clears all status fields to '0'.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		RX_DATA0_FRAME_ERROR [5:5]	HEADER_RESPONSE [4:4]	DATA_IDX [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		RX_DONE [13:13]	TX_DONE [12:12]	None [11:10]		RX_BUSY [9:9]	TX_BUSY [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						TX_RESPONSE_BIT_ERROR [17:17]	TX_HEADER_BIT_ERROR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			RX_RESPONSE_CHECKSUM_ERROR [28:28]	RX_RESPONSE_FRAME_ERROR [27:27]	RX_HEADER_PARITY_ERROR [26:26]	RX_HEADER_SYNC_ERROR [25:25]	RX_HEADER_FRAME_ERROR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	DATA_IDX	R	W	0	Number of transferred data and checksum fields in the response (also acts as an index/address into response data field and checksum field registers (DATA0, DATA1, PID_CHECKSUM)) : '0': No data fields transferred. '1': Data field 1 transferred. ... '7': Data fields 1, 2, 3, ... and 7 transferred. '8': Data fields 1, 2, 3, ... and 8 transferred. '9': Data fields 1, 2, 3, ..., 8 and checksum field transferred. '10'-'15': Unused. Set to '0' on the start of a TX_HEADER or RX_HEADER command.
4	HEADER_RESPONSE	R	W	0	Frame header / response identifier (only valid when TX_BUSY or RX_BUSY is '1'): '0': Frame header being transferred. '1': Frame response being transferred.

Bits	Name	SW	HW	Default or Enum	Description
5	RX_DATA0_FRAME_ERROR	R	W	0	Frame response, first data field frame error. HW sets this field to '1' when the received STOP bits of the first response data field have an unexpected value (only after a RX_HEADER command), and this data byte is 0x00. HW clears this field to '0' at the falling edge of SYNC start bit (after INTR.RX_HEADER_BREAK_WAKEUP_DONE). This field is used together with INTR.RX_RESPONSE_FRAME_ERROR to distinguish 'no response', 'error response' and 'correct response' scenarios. Note: The ongoing message transfer is NOT aborted.
8	TX_BUSY	R	W	0	Transmitter busy. - Set to '1' on the start of the following commands: TX_HEADER, TX_RESPONSE, TX_WAKEUP. - Set to '0' on successful completion of previous commands or when an error is detected. In the successful completion case, TX_BUSY is updated one cycle after TX_DONE. In 'TX_HEADER, RX_RESPONSE' case, set to '0' at the start bit falling edge in the first response data byte, after header transmission
9	RX_BUSY	R	W	0	Receiver busy. - Set to '1' on the start of the following commands: RX_HEADER, RX_RESPONSE. in RX_HEADER case, set at Break filed rising edge. in RX_RESPONSE case, set at the start bit falling edge in the first response data byte. - Set to '0' on successful completion of previous commands or when an error is detected. In the successful completion case, RX_BUSY is updated one cycle after RX_DONE.
12	TX_DONE	R	W	0	Transmitter done: - Set to '0' on the start of a new command. - Set to '1' on successful completion of the following command sequences (if CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble): - TX_HEADER. - TX_HEADER, TX_RESPONSE. - RX_HEADER, TX_RESPONSE. - TX_WAKEUP.
13	RX_DONE	R	W	0	Receiver done: - Set to '0' on the start of a new command. - Set to '1' on successful completion of the following command sequences (if CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble): - RX_HEADER, RX_RESPONSE. - TX_HEADER, RX_RESPONSE.
16	TX_HEADER_BIT_ERROR	R	W	0	Copy of INTR.TX_HEADER_BIT_ERROR.
17	TX_RESPONSE_BIT_ERROR	R	W	0	Copy of INTR.TX_RESPONSE_BIT_ERROR.
24	RX_HEADER_FRAME_ERROR	R	W	0	Copy of INTR.RX_HEADER_FRAME_ERROR.
25	RX_HEADER_SYNC_ERROR	R	W	0	Copy of INTR.RX_HEADER_SYNC_ERROR.

Bits	Name	SW	HW	Default or Enum	Description
26	RX_HEADER_PARITY_ERROR	R	W	0	Copy of INTR.RX_HEADER_PARITY_ERROR.
27	RX_RESPONSE_FRAME_ERROR	R	W	0	Copy of INTR.RX_RESPONSE_FRAME_ERROR.
28	RX_RESPONSE_CHECKSUM_ERROR	R	W	0	Copy of INTR.RX_RESPONSE_CHECKSUM_ERROR.

8.3.3.4 LIN_CH_CMD

Description: Command
Address: 0x402D8010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: The register fields are retained. When a LIN channel is disabled (CTL.ENABLED is set to '0'), HW sets all the register fields to '0'.

The following restrictions apply when programming the commands:
- TX_HEADER and RX_HEADER are mutually exclusive; i.e. cannot both be set to '1'.
- TX_WAKEUP is mutually exclusive with all other commands.
- TX_RESPONSE and RX_RESPONSE are NOT mutually exclusive, but are evaluated in the following order (of decreasing priority): TX_RESPONSE, RX_RESPONSE.

The CMD.TX_HEADER register field description provides all legal command sequences. The break or wakeup detection is always enabled, regardless of CMD register setting.

Note: LIN mode supports all commands, UART mode supports the TX_HEADER and RX_HEADER commands only.

Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					TX_WAKEUP [2:2]	TX_RESPONSE [1:1]	TX_HEADER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						RX_RESPONSE [9:9]	RX_HEADER [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TX_HEADER	RW1S	RW	0	SW sets this field to '1' to transmit a header. HW sets this field to '0' on successful completion of ANY of the following legal command sequences (also set to '0' when an error is detected): - TX_HEADER - TX_HEADER, TX_RESPONSE. - TX_HEADER, RX_RESPONSE. - RX_HEADER, TX_RESPONSE. - RX_HEADER, RX_RESPONSE. - TX_WAKEUP. The header is transmitted when the PID field STOP bits are transmitted (INTR.TX_HEADER_DONE). HW sets this field to '1', when the 'tr_cmd_tx_header' input trigger is activated. This allows for time triggered LIN message transfer. HW driven time triggered transfer eliminates the jitter that is typically associated with SW driven transfer. In UART mode, a single data field (DATA0.DATA1) is transmitted.
1	TX_RESPONSE	RW1S	RW1C	0	SW sets this field to '1' to transmit a response. HW sets this field to '0' on successful completion of ANY of the legal command sequences (also set to '0' when an error is detected). The response is transmitted when the checksum field STOP bits are transmitted (INTR.TX_RESPONSE_DONE).
2	TX_WAKEUP	RW1S	RW1C	0	SW sets this field to '1' to transmit a wakeup signal. HW sets this field to '0' on successful completion of ANY of the legal command sequences (also set to '0' when an error is detected). The command generates CTL.BREAK_WAKEUP_LENGTH bit periods in the dominant state (low/'0') and transitions to the recessive state (high/'1') (INTR.TX_WAKEUP_DONE).

Bits	Name	SW	HW	Default or Enum	Description
8	RX_HEADER	RW1S	RW1C	0	SW sets this field to '1' to receive a header. HW sets this field to '0' on successful completion of the ANY of the legal command sequences (NOT set to '0' when an error is detected in LIN mode). The header is received when the PID field STOP bits are received (INTR.RX_HEADER_DONE). Typically, a slave node SW sets both RX_HEADER and RX_RESPONSE to '1', anticipating a transfer of a response from the master node to this slave node. After receipt of the header PID field (INTR.RX_HEADER_PID_DONE is activated), the slave node may decide to set TX_RESPONSE to '1' (which has a higher priority than RX_RESPONSE) to transmit a response. the Break detection is performed regardless of CMD.RX_HEADER. INTR.RX_BREAK_WAKEUP_DONE will trigger at LIN_RX rising edge, when the low pulse meet CTL0.BREAK_WAKEUP_LENGTH. when Break is detected, HW check CMD.RX_HEADER before entering SYNC byte processing state. when RX_HEADER is cleared, SW has at least 11 bit times to set RX_HEADER again, before next Break is detected (RX_BREAK_WAKEUP_DONE). in this case, there is no gap, Break will never be missed. In UART mode, a single data field in received (in DATA0.DATA1). HW set this field to '0' when the data field is received, or when an error is detected.
9	RX_RESPONSE	RW1S	RW1C	0	SW sets this field to '1' to receive a response. HW sets this field to '0' on successful completion of ANY of the legal command sequences (NOT set to '0' when an error is detected). The response is received when the checksum field STOP bits are received (INTR.RX_RESPONSE_DONE).

8.3.3.5 LIN_CH_TX_RX_STATUS

Description: TX/RX status
Address: 0x402D8060
Offset: 0x60
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SYNC_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						RX_IN [17:17]	TX_IN [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:27]					EN_OUT [26:26]	None [25:25]	TX_OUT [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	SYNC_COUNTER	R	W	Undefined	Synchronization counter in LIN channel clock periods. After the receipt of a synchronization field, this fields reflects the duration of the synchronization field. Ideally, SYNC_COUNTER = 8*16 = 128 (the synchronization fields consists of eight bit period of 16 LIN channel clock periods each). - If SYNC_COUNTER is less than 128, the LIN channel clock is too slow and the PERI/PCLK divider value should be decreased. - If SYNC_COUNTER is greater than 128, the LIN channel clock is too fast and the PERI/PCLK divider value should be increased. The biggest master-slave clock discrepancy occurs when the master is slow and the slave is fast or vice versa. At a 0.5 percent master inaccuracy and a 14 percent slave inaccuracy, this results in the extreme synchronization values of (.86 * 128) / 1.005 = 109.5 and (1.14 *128) / 0.995 = 146.6. We add a little margin for a valid range of [106, 152]. Note: Only slave nodes with imprecise clocks require clock resynchronization. Master and slave nodes with precise clocks do NOT require clock resynchronization.
16	TX_IN	R	W	Undefined	LIN transmitter input ('tx_in', 'lin_tx_in' in functional mode). TX_IN and RX_IN can be used to determine a wakeup source. Note that wakeup source detection relies on the external transceiver functionality.
17	RX_IN	R	W	Undefined	LIN receiver input ('rx_in', 'lin_rx_in' in functional mode).
24	TX_OUT	R	W	1	LIN transmitter output ('tx_out', 'lin_tx_out').

Bits	Name	SW	HW	Default or Enum	Description
26	EN_OUT	RW	RW	1	LIN transceiver enable ('en_out', 'lin_en_out'). This field controls the enable (or low active sleep enable) of the external transceiver: '0': Disabled. '1': Enabled. If CTL.AUTO_EN is '0', SW controls this field to enable the external transceiver. If CTL.AUTO_EN is '1', HW controls this field to enable the external transceiver: - Before a legal command sequence, HW sets this field to '1', if it is '0'. The start of the command sequence is effectively postponed by a 4-bit period preamble. - After a legal command sequence, HW clears this field to '0'. The end of the command sequence is effectively postponed by a 4-bit period postamble. Note: external transceivers require a 'power up' or 'power down' period of 1 or 2 bit periods, so a 4-bit period suffices for all known transceivers.

8.3.3.6 LIN_CH_PID_CHECKSUM

Description: PID and checksum
Address: 0x402D8080
Offset: 0x80
Retention: Retained
IsDeepSleep: No
Comment: This register supports 8-bit, 16-bit and 32-bit accesses.

A LIN header has a single PID field. This field is SW accessible through this register. The field is used in BOTH transmit and receive modes.

A LIN response has a single checksum field. This field is SW accessible through this register. The field is used in BOTH transmit and receive modes.

Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PID [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CHECKSUM [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	PID	RW	RW	Undefined	Header protected identifier (PID). - Bits 5 down to 0: frame identifier ID[5:0]. Frame identifier 0x3c is for a 'master request' frame, 0x3d is for a 'slave response' frame, 0x3e and 0x3f are for future LIN enhancements. Frame identifier ID[5:4] is optionally used for length control; i.e. specifies the number of response data fields. - Bits 1 down to 0: parity bits P[1] and P[0]. - P[1] = ! (ID[5] ^ ID[4] ^ ID[3] ^ ID[1]) - P[0] = (ID[4] ^ ID[2] ^ ID[1] ^ ID[0]) Transmission: To be transmitted PID field. SW needs to calculate the PID field parity bits P[1] and P[0]. Reception: Received PID field. Slave node SW uses the PID field to determine how to handle the response for a received frame header: TX_RESPONSE or RX_RESPONSE.
8:15	CHECKSUM	R	RW	Undefined	Checksum. Transmission: HW calculated checksum (SW does not need to calculate the checksum) over the transmitted PID field (optional per CTL.CHECKSUM_ENHANCED) and data fields. Reception: Received checksum. Note that in case of a RX_CHECKSUM_ERROR, SW can use the received PID field and the received data fields to calculate the correct checksum value.

8.3.3.7 LIN_CH_DATA0

Description: Response data 0
Address: 0x402D8084
Offset: 0x84
Retention: Retained
IsDeepSleep: No
Comment: This register supports 8-bit, 16-bit and 32-bit accesses. This allows for a single 32-bit access to write or read four data fields.

A LIN response has a maximum of eight data fields. These data fields are SW accessible through the DATA0 and DATA1 registers. These register are used in BOTH transmit and receive modes. If the LIN response is both transmitted and received, the to be transmitted data fields (provided by SW) in this register are overwritten by the received data fields (provided by HW).

Data field DATA1 is the first response data field (first to be transmitted/received). The number of transmitted/received data fields is specified by CTL.DATA_NR.

Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA1 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA2 [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	DATA3 [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	DATA4 [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	DATA1	RW	RW	Undefined	Data field 1. Transmission: To be transmitted data field. SW provides data field. Reception: Received data field. SW uses the data field.
8:15	DATA2	RW	RW	Undefined	Data field 2.
16:23	DATA3	RW	RW	Undefined	Data field 3.
24:31	DATA4	RW	RW	Undefined	Data field 4.

8.3.3.8 LIN_CH_DATA1

Description: Response data 1
Address: 0x402D8088
Offset: 0x88
Retention: Retained
IsDeepSleep: No
Comment: This register supports 8-bit, 16-bit and 32-bit accesses. This allows for a single 32-bit access to write or read four data fields.
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA5 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA6 [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	DATA7 [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	DATA8 [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	DATA5	RW	RW	Undefined	Data field 5.
8:15	DATA6	RW	RW	Undefined	Data field 6.
16:23	DATA7	RW	RW	Undefined	Data field 7.
24:31	DATA8	RW	RW	Undefined	Data field 8.

8.3.3.9 LIN_CH_INTR

Description: Interrupt
Address: 0x402D80C0
Offset: 0xC0
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.

This is a non-retained register; setting CTL.ENABLED to '0' clears all command fields to '0'.

An activated error interrupt cause aborts an ongoing frame transfer (except for bit errors when CTL.BIT_ERROR_IGNORE is '1').

Note: LIN mode supports all interrupt causes. UART mode supports the RX_NOISE_DETECT, TX_HEADER_BIT_ERROR, RX_HEADER_FRAME_ERROR and RX_HEADER_PARITY_ERROR interrupt causes only.

Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					TX_WAKEUP_DONE [2:2]	TX_RESPONSE_DONE [1:1]	TX_HEADER_DONE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	TIMEOUT [14:14]	RX_NOISE_DETECT [13:13]	None [12:12]	RX_HEADER_SYNC_DONE [11:11]	RX_BREAK_WAKEUP_DONE [10:10]	RX_RESPONSE_DONE [9:9]	RX_HEADER_DONE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						TX_RESPONSE_BIT_ERROR [17:17]	TX_HEADER_BIT_ERROR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			RX_RESPONSE_CHECKSUM_ERROR [28:28]	RX_RESPONSE_FRAME_ERROR [27:27]	RX_HEADER_PARITY_ERROR [26:26]	RX_HEADER_SYNC_ERROR [25:25]	RX_HEADER_FRAME_ERROR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TX_HEADER_DONE	RW1C	RW1S	0	HW sets this field to '1', when a frame header (break field, synchronization field and PID field) is transmitted (the CMD.TX_HEADER is completed). Specifically: - When followed by CMD.TX_RESPONSE or CMD.RX_RESPONSE, this field is set to '1' after completion of the frame header transfer. - When not followed by a response command, this field is set to '1' after completion of the frame header transfer. If CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble. Note: used in UART mode.
1	TX_RESPONSE_DONE	RW1C	RW1S	0	HW sets this field to '1', when a frame response (data fields and checksum field) is transmitted (the CMD.TX_RESPONSE is completed). If CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble.
2	TX_WAKEUP_DONE	RW1C	RW1S	0	HW sets this field to '1', when a wakeup signal is transmitted (per CTL.BREAK_WAKEUP_LENGTH). This cause is activated on a transition from dominant/'0' state to recessive/'1' state; i.e. at the end of the wakeup signal.
8	RX_HEADER_DONE	RW1C	RW1S	0	HW sets this field to '1', when a frame header (break field, synchronization field and PID field) is received (the CMD.RX_HEADER is completed). Specifically: - When followed by CMD.TX_RESPONSE or CMD.RX_RESPONSE, this field is set to '1' after completion of the frame header transfer. - When not followed by a response command, this field is set to '1' after completion of the frame header transfer. If CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble. Note: used in UART mode.
9	RX_RESPONSE_DONE	RW1C	RW1S	0	HW sets this field to '1', when a frame response (data fields and checksum field) is received (the CMD.RX_RESPONSE is completed). If CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble. Note: activation implies that RX_RESPONSE_FRAME_ERROR and RX_RESPONSE_CHECKSUM_ERROR are not activated during response reception
10	RX_BREAK_WAKEUP_DONE	RW1C	RW1S	0	HW sets this field to '1', when a break or wakeup signal is received (per CTL.BREAK_WAKEUP_LENGTH). This cause is activated on a transition from dominant/'0' state to recessive/'1' state; i.e. at the end of the wakeup signal. The break or wakeup detection is always enabled, regardless of CMD register setting.
11	RX_HEADER_SYNC_DONE	RW1C	RW1S	0	HW sets this field to '1', when a synchronization field is received (including trailing STOP bits).

Bits	Name	SW	HW	Default or Enum	Description
13	RX_NOISE_DETECT	RW1C	RW1S	0	HW sets this field to '1', when isolated '0' or '1' 'in_rx_in' values are observed or when during sampling the last three 'lin_rx_in' values do NOT all have the same value. This mismatch is an indication of noise on the LIN line. Note: The ongoing frame transfer is NOT aborted. Note: Used in UART mode.
14	TIMEOUT	RW1C	RW1S	0	HW sets this field to '1', when a frame, frame header or frame response timeout is detected (per CTL.FRAME_TIMEOUT_SEL). Note: The ongoing frame transfer is NOT aborted.
16	TX_HEADER_BIT _ERROR	RW1C	RW1S	0	HW sets this field to '1', when a transmitted 'lin_tx_out' value does NOT match a received 'lin_rx_in' value (during header transmission). This specific test allows for delay through the external transceiver. This mismatch is an indication of bus collisions on the LIN line. The match is performed for the Wakeup, Break, SYNC and the PID fields (for the START bit, data Byte and STOP bit). Note: When CTL.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_HEADER_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'. Note: Used in UART mode.
17	TX_RESPONSE_BIT _ERROR	RW1C	RW1S	0	HW sets this field to '1', when a transmitted 'lin_tx_out' value does NOT match a received 'lin_rx_in' value (during response transmission). The match is performed for the data fields and the checksum field (for the START bit, data Byte and STOP bit). Note: When CTL.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_RESPONSE_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.
24	RX_HEADER_FRAME _ERROR	RW1C	RW1S	0	HW sets this field to '1', when the received START or STOP bits have an unexpected value (during header reception). Note: The ongoing message transfer is aborted (INTR.RX_HEADER_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'. Note: Used in UART mode.

Bits	Name	SW	HW	Default or Enum	Description
25	RX_HEADER_SYNC _ERROR	RW1C	RW1S	0	HW sets this field to '1', when the received synchronization field is not received within the synchronization counter range [106, 152] (see TX_RX_STATUS.SYNC_COUNTER). Note: The ongoing message transfer is aborted (INTR.RX_HEADER_SYNC_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.
26	RX_HEADER_PARITY _ERROR	RW1C	RW1S	0	HW sets this field to '1', when the received PID field has a parity error. Note: The ongoing message transfer is aborted (INTR.RX_PID_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'. +G119 HW sets this field to '1', when the received data field has a parity error (when CTL0.PARITY_EN is '1').
27	RX_RESPONSE_FRAME _ERROR	RW1C	RW1S	0	HW sets this field to '1', when the received START or STOP bits have an unexpected value (during response reception). HW does NOT use this field for the STOP bits of the first data field after a RX_HEADER command, if the received data byte is 0x00. (STATUS.RX_DATA0_FRAME_ERROR is used instead). Note: The ongoing message transfer is aborted (INTR.RX_RESPONSE_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.
28	RX_RESPONSE _CHECKSUM_ERROR	RW1C	RW1S	0	HW sets this field to '1', when the calculated checksum over the received PID and data fields is not the same as the received checksum. Note: The ongoing message transfer is aborted (INTR.RX_RESPONSE_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.

8.3.3.10 LIN_CH_INTR_SET

Description: Interrupt set
Address: 0x402D80C4
Offset: 0xC4
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the INTR register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					TX_WAKEUP_DONE [2:2]	TX_RESPONSE_DONE [1:1]	TX_HEADER_DONE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	TIMEOUT [14:14]	RX_NOISE_DETECT [13:13]	None [12:12]	RX_HEADER_SYNC_DONE [11:11]	RX_BREAK_WAKEUP_DONE [10:10]	RX_RESPONSE_DONE [9:9]	RX_HEADER_DONE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						TX_RESPONSE_BIT_ERROR [17:17]	TX_HEADER_BIT_ERROR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			RX_RESPONSE_CHECKSUM_ERROR [28:28]	RX_RESPONSE_FRAME_ERROR [27:27]	RX_HEADER_PARITY_ERROR [26:26]	RX_HEADER_SYNC_ERROR [25:25]	RX_HEADER_FRAME_ERROR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TX_HEADER_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
1	TX_RESPONSE_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
2	TX_WAKEUP_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
8	RX_HEADER_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
9	RX_RESPONSE_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
10	RX_BREAK_WAKEUP_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
11	RX_HEADER_SYNC_DONE	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
13	RX_NOISE_DETECT	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
14	TIMEOUT	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).

Bits	Name	SW	HW	Default or Enum	Description
16	TX_HEADER_BIT _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
17	TX_RESPONSE_BIT _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
24	RX_HEADER_FRAME _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
25	RX_HEADER_SYNC _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
26	RX_HEADER_PARITY _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
27	RX_RESPONSE_FRAME _ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).
28	RX_RESPONSE _CHECKSUM_ERROR	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect).

8.3.3.11 LIN_CH_INTR_MASK

Description: Interrupt mask
Address: 0x402D80C8
Offset: 0xC8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					TX_WAKEUP_DONE [2:2]	TX_RESPONSE_DONE [1:1]	TX_HEADER_DONE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	TIMEOUT [14:14]	RX_NOISE_DETECT [13:13]	None [12:12]	RX_HEADER_SYNC_DONE [11:11]	RX_BREAK_WAKEUP_DONE [10:10]	RX_RESPONSE_DONE [9:9]	RX_HEADER_DONE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						TX_RESPONSE_BIT_ERROR [17:17]	TX_HEADER_BIT_ERROR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			RX_RESPONSE_CHECKSUM_ERROR [28:28]	RX_RESPONSE_FRAME_ERROR [27:27]	RX_HEADER_PARITY_ERROR [26:26]	RX_HEADER_SYNC_ERROR [25:25]	RX_HEADER_FRAME_ERROR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TX_HEADER_DONE	RW	R	0	Mask for corresponding field in INTR register.
1	TX_RESPONSE_DONE	RW	R	0	Mask for corresponding field in INTR register.
2	TX_WAKEUP_DONE	RW	R	0	Mask for corresponding field in INTR register.
8	RX_HEADER_DONE	RW	R	0	Mask for corresponding field in INTR register.
9	RX_RESPONSE_DONE	RW	R	0	Mask for corresponding field in INTR register.
10	RX_BREAK_WAKEUP_DONE	RW	R	0	Mask for corresponding field in INTR register.
11	RX_HEADER_SYNC_DONE	RW	R	0	Mask for corresponding field in INTR register.
13	RX_NOISE_DETECT	RW	R	0	Mask for corresponding field in INTR register.
14	TIMEOUT	RW	R	0	Mask for corresponding field in INTR register.
16	TX_HEADER_BIT_ERROR	RW	R	0	Mask for corresponding field in INTR register.
17	TX_RESPONSE_BIT_ERROR	RW	R	0	Mask for corresponding field in INTR register.
24	RX_HEADER_FRAME_ERROR	RW	R	0	Mask for corresponding field in INTR register.

Bits	Name	SW	HW	Default or Enum	Description
25	RX_HEADER_SYNC _ERROR	RW	R	0	Mask for corresponding field in INTR register.
26	RX_HEADER_PARITY _ERROR	RW	R	0	Mask for corresponding field in INTR register.
27	RX_RESPONSE_FRAME _ERROR	RW	R	0	Mask for corresponding field in INTR register.
28	RX_RESPONSE _CHECKSUM_ERROR	RW	R	0	Mask for corresponding field in INTR register.

8.3.3.12 LIN_CH_INTR_MASKED

Description: Interrupt masked
Address: 0x402D80CC
Offset: 0xCC
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise AND between the INTR and INTR_MASK registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for INTR and one for INTR_MASK. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_MASKED != 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					TX_WAKEUP_DONE [2:2]	TX_RESPONSE_DONE [1:1]	TX_HEADER_DONE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	TIMEOUT [14:14]	RX_NOISE_DETECT [13:13]	None [12:12]	RX_HEADER_SYNC_DONE [11:11]	RX_BREAK_WAKEUP_DONE [10:10]	RX_RESPONSE_DONE [9:9]	RX_HEADER_DONE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						TX_RESPONSE_BIT_ERROR [17:17]	TX_HEADER_BIT_ERROR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			RX_RESPONSE_CHECKSUM_ERROR [28:28]	RX_RESPONSE_FRAME_ERROR [27:27]	RX_HEADER_PARITY_ERROR [26:26]	RX_HEADER_SYNC_ERROR [25:25]	RX_HEADER_FRAME_ERROR [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TX_HEADER_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
1	TX_RESPONSE_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
2	TX_WAKEUP_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
8	RX_HEADER_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
9	RX_RESPONSE_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
10	RX_BREAK_WAKEUP_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
11	RX_HEADER_SYNC_DONE	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.

Bits	Name	SW	HW	Default or Enum	Description
13	RX_NOISE_DETECT	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
14	TIMEOUT	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
16	TX_HEADER_BIT _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
17	TX_RESPONSE_BIT _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
24	RX_HEADER_FRAME _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
25	RX_HEADER_SYNC _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
26	RX_HEADER_PARITY _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
27	RX_RESPONSE_FRAME _ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.
28	RX_RESPONSE _CHECKSUM_ERROR	R	W	0	Logical AND of corresponding INTR and INTR_MASK fields.

9 PACSS

Description Programmable Analog Channel Sub-System
Base Address 0x40300000
Size 0x100000
Slave Num MMIO2

9.1 DCHAN 0

Register Name	Address	Permission	Description
PACSS_DCHAN0_DCHAN_CTL	0x40300000	FULL	Digital Channel Control
PACSS_DCHAN0_SMP_CTL	0x40300004	FULL	Sample Control
PACSS_DCHAN0_SMP_REF_CTL	0x40300008	FULL	Sample Reference Control
PACSS_DCHAN0_DEC_CTL	0x4030000C	FULL	Decimator Control
PACSS_DCHAN0_PP_CTL	0x40300010	FULL	Post Processing Control
PACSS_DCHAN0_OFST_COR	0x40300014	FULL	Offset Correction register
PACSS_DCHAN0_GAIN_COR	0x40300018	FULL	Gain Correction register
PACSS_DCHAN0_RANGE_LOW	0x4030001C	FULL	Range Detect low value register.
PACSS_DCHAN0_RANGE_HIGH	0x40300020	FULL	Range detect high value register.
PACSS_DCHAN0_PGA_GAIN_CTL	0x40300024	FULL	PGA Gain Control register
PACSS_DCHAN0_CAP_CFG0	0x40300028	FULL	Capacitor Configuration 0 register
PACSS_DCHAN0_CAP_CFG1	0x4030002C	FULL	Capacitor Configuration 1 register
PACSS_DCHAN0_CAP_CFG2	0x40300030	FULL	Capacitor Configuration 2 register
PACSS_DCHAN0_ACC_THRESH	0x40300034	FULL	Accumulated Data Threshold
PACSS_DCHAN0_RESULT	0x40300040	FULL	Channel result data register, updated at the end of each completed conversion
PACSS_DCHAN0_RESULT_TAG	0x40300044	FULL	Tag register associated and updated simultaneously with the RESULT register
PACSS_DCHAN0_ACC_RESULT	0x40300048	FULL	Channel Accumulated result data register
PACSS_DCHAN0_INTR	0x40300050	FULL	Interrupt request register
PACSS_DCHAN0_INTR_SET	0x40300054	FULL	Interrupt set request register
PACSS_DCHAN0_INTR_MASK	0x40300058	FULL	Interrupt mask register
PACSS_DCHAN0_INTR_MASKED	0x4030005C	FULL	Interrupt masked request register
PACSS_DCHAN0_STATUS	0x40300060	FULL	Status registesr

9.1.1 FCFG 0

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG0_COEF	0x40300100	FULL	Coefficient Value
PACSS_DCHAN0_FCFG0_TAP	0x40300108	FULL	Tap Value

9.1.2 FCFG 1

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG1_COEF	0x40300110	FULL	Coefficient Value
PACSS_DCHAN0_FCFG1_TAP	0x40300118	FULL	Tap Value

9.1.3 FCFG 2

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG2_COEF	0x40300120	FULL	Coefficient Value
PACSS_DCHAN0_FCFG2_TAP	0x40300128	FULL	Tap Value

9.1.4 FCFG 3

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG3_COEF	0x40300130	FULL	Coefficient Value
PACSS_DCHAN0_FCFG3_TAP	0x40300138	FULL	Tap Value

9.1.5 FCFG 4

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG4_COEF	0x40300140	FULL	Coefficient Value
PACSS_DCHAN0_FCFG4_TAP	0x40300148	FULL	Tap Value

9.1.6 FCFG 5

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG5_COEF	0x40300150	FULL	Coefficient Value
PACSS_DCHAN0_FCFG5_TAP	0x40300158	FULL	Tap Value

9.1.7 FCFG 6

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG6_COEF	0x40300160	FULL	Coefficient Value
PACSS_DCHAN0_FCFG6_TAP	0x40300168	FULL	Tap Value

9.1.8 FCFG 7

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG7_COEF	0x40300170	FULL	Coefficient Value
PACSS_DCHAN0_FCFG7_TAP	0x40300178	FULL	Tap Value

9.1.9 FCFG 8

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG8_COEF	0x40300180	FULL	Coefficient Value
PACSS_DCHAN0_FCFG8_TAP	0x40300188	FULL	Tap Value

9.1.10 FCFG 9

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG9_COEF	0x40300190	FULL	Coefficient Value
PACSS_DCHAN0_FCFG9_TAP	0x40300198	FULL	Tap Value

9.1.11 FCFG 10

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG10_COEF	0x403001A0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG10_TAP	0x403001A8	FULL	Tap Value

9.1.12 FCFG 11

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG11_COEF	0x403001B0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG11_TAP	0x403001B8	FULL	Tap Value

9.1.13 FCFG 12

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG12_COEF	0x403001C0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG12_TAP	0x403001C8	FULL	Tap Value

9.1.14 FCFG 13

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG13_COEF	0x403001D0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG13_TAP	0x403001D8	FULL	Tap Value

9.1.15 FCFG 14

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG14_COEF	0x403001E0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG14_TAP	0x403001E8	FULL	Tap Value

9.1.16 FCFG 15

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG15_COEF	0x403001F0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG15_TAP	0x403001F8	FULL	Tap Value

9.1.17 FCFG 16

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG16_COEF	0x40300200	FULL	Coefficient Value
PACSS_DCHAN0_FCFG16_TAP	0x40300208	FULL	Tap Value

9.1.18 FCFG 17

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG17_COEF	0x40300210	FULL	Coefficient Value
PACSS_DCHAN0_FCFG17_TAP	0x40300218	FULL	Tap Value

9.1.19 FCFG 18

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG18_COEF	0x40300220	FULL	Coefficient Value
PACSS_DCHAN0_FCFG18_TAP	0x40300228	FULL	Tap Value

9.1.20 FCFG 19

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG19_COEF	0x40300230	FULL	Coefficient Value
PACSS_DCHAN0_FCFG19_TAP	0x40300238	FULL	Tap Value

9.1.21 FCFG 20

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG20_COEF	0x40300240	FULL	Coefficient Value
PACSS_DCHAN0_FCFG20_TAP	0x40300248	FULL	Tap Value

9.1.22 FCFG 21

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG21_COEF	0x40300250	FULL	Coefficient Value
PACSS_DCHAN0_FCFG21_TAP	0x40300258	FULL	Tap Value

9.1.23 FCFG 22

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG22_COEF	0x40300260	FULL	Coefficient Value
PACSS_DCHAN0_FCFG22_TAP	0x40300268	FULL	Tap Value

9.1.24 FCFG 23

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG23_COEF	0x40300270	FULL	Coefficient Value
PACSS_DCHAN0_FCFG23_TAP	0x40300278	FULL	Tap Value

9.1.25 FCFG 24

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG24_COEF	0x40300280	FULL	Coefficient Value
PACSS_DCHAN0_FCFG24_TAP	0x40300288	FULL	Tap Value

9.1.26 FCFG 25

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG25_COEF	0x40300290	FULL	Coefficient Value
PACSS_DCHAN0_FCFG25_TAP	0x40300298	FULL	Tap Value

9.1.27 FCFG 26

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG26_COEF	0x403002A0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG26_TAP	0x403002A8	FULL	Tap Value

9.1.28 FCFG 27

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG27_COEF	0x403002B0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG27_TAP	0x403002B8	FULL	Tap Value

9.1.29 FCFG 28

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG28_COEF	0x403002C0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG28_TAP	0x403002C8	FULL	Tap Value

9.1.30 FCFG 29

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG29_COEF	0x403002D0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG29_TAP	0x403002D8	FULL	Tap Value

9.1.31 FCFG 30

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG30_COEF	0x403002E0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG30_TAP	0x403002E8	FULL	Tap Value

9.1.32 FCFG 31

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG31_COEF	0x403002F0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG31_TAP	0x403002F8	FULL	Tap Value

9.1.33 FCFG 32

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG32_COEF	0x40300300	FULL	Coefficient Value
PACSS_DCHAN0_FCFG32_TAP	0x40300308	FULL	Tap Value

9.1.34 FCFG 33

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG33_COEF	0x40300310	FULL	Coefficient Value
PACSS_DCHAN0_FCFG33_TAP	0x40300318	FULL	Tap Value

9.1.35 FCFG 34

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG34_COEF	0x40300320	FULL	Coefficient Value
PACSS_DCHAN0_FCFG34_TAP	0x40300328	FULL	Tap Value

9.1.36 FCFG 35

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG35_COEF	0x40300330	FULL	Coefficient Value
PACSS_DCHAN0_FCFG35_TAP	0x40300338	FULL	Tap Value

9.1.37 FCFG 36

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG36_COEF	0x40300340	FULL	Coefficient Value
PACSS_DCHAN0_FCFG36_TAP	0x40300348	FULL	Tap Value

9.1.38 FCFG 37

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG37_COEF	0x40300350	FULL	Coefficient Value
PACSS_DCHAN0_FCFG37_TAP	0x40300358	FULL	Tap Value

9.1.39 FCFG 38

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG38_COEF	0x40300360	FULL	Coefficient Value
PACSS_DCHAN0_FCFG38_TAP	0x40300368	FULL	Tap Value

9.1.40 FCFG 39

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG39_COEF	0x40300370	FULL	Coefficient Value
PACSS_DCHAN0_FCFG39_TAP	0x40300378	FULL	Tap Value

9.1.41 FCFG 40

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG40_COEF	0x40300380	FULL	Coefficient Value
PACSS_DCHAN0_FCFG40_TAP	0x40300388	FULL	Tap Value

9.1.42 FCFG 41

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG41_COEF	0x40300390	FULL	Coefficient Value
PACSS_DCHAN0_FCFG41_TAP	0x40300398	FULL	Tap Value

9.1.43 FCFG 42

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG42_COEF	0x403003A0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG42_TAP	0x403003A8	FULL	Tap Value

9.1.44 FCFG 43

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG43_COEF	0x403003B0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG43_TAP	0x403003B8	FULL	Tap Value

9.1.45 FCFG 44

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG44_COEF	0x403003C0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG44_TAP	0x403003C8	FULL	Tap Value

9.1.46 FCFG 45

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG45_COEF	0x403003D0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG45_TAP	0x403003D8	FULL	Tap Value

9.1.47 FCFG 46

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG46_COEF	0x403003E0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG46_TAP	0x403003E8	FULL	Tap Value

9.1.48 FCFG 47

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG47_COEF	0x403003F0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG47_TAP	0x403003F8	FULL	Tap Value

9.1.49 FCFG 48

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG48_COEF	0x40300400	FULL	Coefficient Value
PACSS_DCHAN0_FCFG48_TAP	0x40300408	FULL	Tap Value

9.1.50 FCFG 49

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG49_COEF	0x40300410	FULL	Coefficient Value
PACSS_DCHAN0_FCFG49_TAP	0x40300418	FULL	Tap Value

9.1.51 FCFG 50

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG50_COEF	0x40300420	FULL	Coefficient Value
PACSS_DCHAN0_FCFG50_TAP	0x40300428	FULL	Tap Value

9.1.52 FCFG 51

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG51_COEF	0x40300430	FULL	Coefficient Value
PACSS_DCHAN0_FCFG51_TAP	0x40300438	FULL	Tap Value

9.1.53 FCFG 52

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG52_COEF	0x40300440	FULL	Coefficient Value
PACSS_DCHAN0_FCFG52_TAP	0x40300448	FULL	Tap Value

9.1.54 FCFG 53

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG53_COEF	0x40300450	FULL	Coefficient Value
PACSS_DCHAN0_FCFG53_TAP	0x40300458	FULL	Tap Value

9.1.55 FCFG 54

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG54_COEF	0x40300460	FULL	Coefficient Value
PACSS_DCHAN0_FCFG54_TAP	0x40300468	FULL	Tap Value

9.1.56 FCFG 55

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG55_COEF	0x40300470	FULL	Coefficient Value
PACSS_DCHAN0_FCFG55_TAP	0x40300478	FULL	Tap Value

9.1.57 FCFG 56

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG56_COEF	0x40300480	FULL	Coefficient Value
PACSS_DCHAN0_FCFG56_TAP	0x40300488	FULL	Tap Value

9.1.58 FCFG 57

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG57_COEF	0x40300490	FULL	Coefficient Value
PACSS_DCHAN0_FCFG57_TAP	0x40300498	FULL	Tap Value

9.1.59 FCFG 58

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG58_COEF	0x403004A0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG58_TAP	0x403004A8	FULL	Tap Value

9.1.60 FCFG 59

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG59_COEF	0x403004B0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG59_TAP	0x403004B8	FULL	Tap Value

9.1.61 FCFG 60

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG60_COEF	0x403004C0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG60_TAP	0x403004C8	FULL	Tap Value

9.1.62 FCFG 61

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG61_COEF	0x403004D0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG61_TAP	0x403004D8	FULL	Tap Value

9.1.63 FCFG 62

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG62_COEF	0x403004E0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG62_TAP	0x403004E8	FULL	Tap Value

9.1.64 FCFG 63

Register Name	Address	Permission	Description
PACSS_DCHAN0_FCFG63_COEF	0x403004F0	FULL	Coefficient Value
PACSS_DCHAN0_FCFG63_TAP	0x403004F8	FULL	Tap Value

9.2 DCHAN 1

Register Name	Address	Permission	Description
PACSS_DCHAN1_DCHAN_CTL	0x40310000	FULL	Digital Channel Control
PACSS_DCHAN1_SMP_CTL	0x40310004	FULL	Sample Control
PACSS_DCHAN1_SMP_REF_CTL	0x40310008	FULL	Sample Reference Control
PACSS_DCHAN1_DEC_CTL	0x4031000C	FULL	Decimator Control
PACSS_DCHAN1_PP_CTL	0x40310010	FULL	Post Processing Control
PACSS_DCHAN1_OFST_COR	0x40310014	FULL	Offset Correction register
PACSS_DCHAN1_GAIN_COR	0x40310018	FULL	Gain Correction register
PACSS_DCHAN1_RANGE_LOW	0x4031001C	FULL	Range Detect low value register.
PACSS_DCHAN1_RANGE_HIGH	0x40310020	FULL	Range detect high value register.
PACSS_DCHAN1_PGA_GAIN_CTL	0x40310024	FULL	PGA Gain Control register
PACSS_DCHAN1_CAP_CFG0	0x40310028	FULL	Capacitor Configuration 0 register
PACSS_DCHAN1_CAP_CFG1	0x4031002C	FULL	Capacitor Configuration 1 register
PACSS_DCHAN1_CAP_CFG2	0x40310030	FULL	Capacitor Configuration 2 register
PACSS_DCHAN1_ACC_THRESH	0x40310034	FULL	Accumulated Data Threshold
PACSS_DCHAN1_RESULT	0x40310040	FULL	Channel result data register, updated at the end of each completed conversion

Register Name	Address	Permission	Description
PACSS_DCHAN1_RESULT_TAG	0x40310044	FULL	Tag register associated and updated simultaneously with the RESULT register
PACSS_DCHAN1_ACC_RESULT	0x40310048	FULL	Channel Accumulated result data register
PACSS_DCHAN1_INTR	0x40310050	FULL	Interrupt request register
PACSS_DCHAN1_INTR_SET	0x40310054	FULL	Interrupt set request register
PACSS_DCHAN1_INTR_MASK	0x40310058	FULL	Interrupt mask register
PACSS_DCHAN1_INTR_MASKED	0x4031005C	FULL	Interrupt masked request register
PACSS_DCHAN1_STATUS	0x40310060	FULL	Status registesr

9.2.1 FCFG 0

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG0_COEF	0x40310100	FULL	Coefficient Value
PACSS_DCHAN1_FCFG0_TAP	0x40310108	FULL	Tap Value

9.2.2 FCFG 1

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG1_COEF	0x40310110	FULL	Coefficient Value
PACSS_DCHAN1_FCFG1_TAP	0x40310118	FULL	Tap Value

9.2.3 FCFG 2

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG2_COEF	0x40310120	FULL	Coefficient Value
PACSS_DCHAN1_FCFG2_TAP	0x40310128	FULL	Tap Value

9.2.4 FCFG 3

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG3_COEF	0x40310130	FULL	Coefficient Value
PACSS_DCHAN1_FCFG3_TAP	0x40310138	FULL	Tap Value

9.2.5 FCFG 4

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG4_COEF	0x40310140	FULL	Coefficient Value
PACSS_DCHAN1_FCFG4_TAP	0x40310148	FULL	Tap Value

9.2.6 FCFG 5

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG5_COEF	0x40310150	FULL	Coefficient Value
PACSS_DCHAN1_FCFG5_TAP	0x40310158	FULL	Tap Value

9.2.7 FCFG 6

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG6_COEF	0x40310160	FULL	Coefficient Value
PACSS_DCHAN1_FCFG6_TAP	0x40310168	FULL	Tap Value

9.2.8 FCFG 7

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG7_COEF	0x40310170	FULL	Coefficient Value
PACSS_DCHAN1_FCFG7_TAP	0x40310178	FULL	Tap Value

9.2.9 FCFG 8

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG8_COEF	0x40310180	FULL	Coefficient Value
PACSS_DCHAN1_FCFG8_TAP	0x40310188	FULL	Tap Value

9.2.10 FCFG 9

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG9_COEF	0x40310190	FULL	Coefficient Value
PACSS_DCHAN1_FCFG9_TAP	0x40310198	FULL	Tap Value

9.2.11 FCFG 10

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG10_COEF	0x403101A0	FULL	Coefficient Value

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG10_TAP	0x403101A8	FULL	Tap Value

9.2.12 FCFG 11

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG11_COEF	0x403101B0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG11_TAP	0x403101B8	FULL	Tap Value

9.2.13 FCFG 12

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG12_COEF	0x403101C0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG12_TAP	0x403101C8	FULL	Tap Value

9.2.14 FCFG 13

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG13_COEF	0x403101D0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG13_TAP	0x403101D8	FULL	Tap Value

9.2.15 FCFG 14

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG14_COEF	0x403101E0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG14_TAP	0x403101E8	FULL	Tap Value

9.2.16 FCFG 15

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG15_COEF	0x403101F0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG15_TAP	0x403101F8	FULL	Tap Value

9.2.17 FCFG 16

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG16_COEF	0x40310200	FULL	Coefficient Value
PACSS_DCHAN1_FCFG16_TAP	0x40310208	FULL	Tap Value

9.2.18 FCFG 17

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG17_COEF	0x40310210	FULL	Coefficient Value
PACSS_DCHAN1_FCFG17_TAP	0x40310218	FULL	Tap Value

9.2.19 FCFG 18

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG18_COEF	0x40310220	FULL	Coefficient Value
PACSS_DCHAN1_FCFG18_TAP	0x40310228	FULL	Tap Value

9.2.20 FCFG 19

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG19_COEF	0x40310230	FULL	Coefficient Value
PACSS_DCHAN1_FCFG19_TAP	0x40310238	FULL	Tap Value

9.2.21 FCFG 20

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG20_COEF	0x40310240	FULL	Coefficient Value
PACSS_DCHAN1_FCFG20_TAP	0x40310248	FULL	Tap Value

9.2.22 FCFG 21

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG21_COEF	0x40310250	FULL	Coefficient Value
PACSS_DCHAN1_FCFG21_TAP	0x40310258	FULL	Tap Value

9.2.23 FCFG 22

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG22_COEF	0x40310260	FULL	Coefficient Value
PACSS_DCHAN1_FCFG22_TAP	0x40310268	FULL	Tap Value

9.2.24 FCFG 23

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG23_COEF	0x40310270	FULL	Coefficient Value
PACSS_DCHAN1_FCFG23_TAP	0x40310278	FULL	Tap Value

9.2.25 FCFG 24

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG24_COEF	0x40310280	FULL	Coefficient Value
PACSS_DCHAN1_FCFG24_TAP	0x40310288	FULL	Tap Value

9.2.26 FCFG 25

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG25_COEF	0x40310290	FULL	Coefficient Value
PACSS_DCHAN1_FCFG25_TAP	0x40310298	FULL	Tap Value

9.2.27 FCFG 26

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG26_COEF	0x403102A0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG26_TAP	0x403102A8	FULL	Tap Value

9.2.28 FCFG 27

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG27_COEF	0x403102B0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG27_TAP	0x403102B8	FULL	Tap Value

9.2.29 FCFG 28

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG28_COEF	0x403102C0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG28_TAP	0x403102C8	FULL	Tap Value

9.2.30 FCFG 29

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG29_COEF	0x403102D0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG29_TAP	0x403102D8	FULL	Tap Value

9.2.31 FCFG 30

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG30_COEF	0x403102E0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG30_TAP	0x403102E8	FULL	Tap Value

9.2.32 FCFG 31

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG31_COEF	0x403102F0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG31_TAP	0x403102F8	FULL	Tap Value

9.2.33 FCFG 32

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG32_COEF	0x40310300	FULL	Coefficient Value
PACSS_DCHAN1_FCFG32_TAP	0x40310308	FULL	Tap Value

9.2.34 FCFG 33

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG33_COEF	0x40310310	FULL	Coefficient Value
PACSS_DCHAN1_FCFG33_TAP	0x40310318	FULL	Tap Value

9.2.35 FCFG 34

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG34_COEF	0x40310320	FULL	Coefficient Value
PACSS_DCHAN1_FCFG34_TAP	0x40310328	FULL	Tap Value

9.2.36 FCFG 35

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG35_COEF	0x40310330	FULL	Coefficient Value
PACSS_DCHAN1_FCFG35_TAP	0x40310338	FULL	Tap Value

9.2.37 FCFG 36

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG36_COEF	0x40310340	FULL	Coefficient Value
PACSS_DCHAN1_FCFG36_TAP	0x40310348	FULL	Tap Value

9.2.38 FCFG 37

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG37_COEF	0x40310350	FULL	Coefficient Value
PACSS_DCHAN1_FCFG37_TAP	0x40310358	FULL	Tap Value

9.2.39 FCFG 38

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG38_COEF	0x40310360	FULL	Coefficient Value
PACSS_DCHAN1_FCFG38_TAP	0x40310368	FULL	Tap Value

9.2.40 FCFG 39

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG39_COEF	0x40310370	FULL	Coefficient Value
PACSS_DCHAN1_FCFG39_TAP	0x40310378	FULL	Tap Value

9.2.41 FCFG 40

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG40_COEF	0x40310380	FULL	Coefficient Value
PACSS_DCHAN1_FCFG40_TAP	0x40310388	FULL	Tap Value

9.2.42 FCFG 41

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG41_COEF	0x40310390	FULL	Coefficient Value
PACSS_DCHAN1_FCFG41_TAP	0x40310398	FULL	Tap Value

9.2.43 FCFG 42

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG42_COEF	0x403103A0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG42_TAP	0x403103A8	FULL	Tap Value

9.2.44 FCFG 43

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG43_COEF	0x403103B0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG43_TAP	0x403103B8	FULL	Tap Value

9.2.45 FCFG 44

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG44_COEF	0x403103C0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG44_TAP	0x403103C8	FULL	Tap Value

9.2.46 FCFG 45

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG45_COEF	0x403103D0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG45_TAP	0x403103D8	FULL	Tap Value

9.2.47 FCFG 46

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG46_COEF	0x403103E0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG46_TAP	0x403103E8	FULL	Tap Value

9.2.48 FCFG 47

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG47_COEF	0x403103F0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG47_TAP	0x403103F8	FULL	Tap Value

9.2.49 FCFG 48

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG48_COEF	0x40310400	FULL	Coefficient Value
PACSS_DCHAN1_FCFG48_TAP	0x40310408	FULL	Tap Value

9.2.50 FCFG 49

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG49_COEF	0x40310410	FULL	Coefficient Value
PACSS_DCHAN1_FCFG49_TAP	0x40310418	FULL	Tap Value

9.2.51 FCFG 50

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG50_COEF	0x40310420	FULL	Coefficient Value
PACSS_DCHAN1_FCFG50_TAP	0x40310428	FULL	Tap Value

9.2.52 FCFG 51

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG51_COEF	0x40310430	FULL	Coefficient Value
PACSS_DCHAN1_FCFG51_TAP	0x40310438	FULL	Tap Value

9.2.53 FCFG 52

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG52_COEF	0x40310440	FULL	Coefficient Value
PACSS_DCHAN1_FCFG52_TAP	0x40310448	FULL	Tap Value

9.2.54 FCFG 53

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG53_COEF	0x40310450	FULL	Coefficient Value
PACSS_DCHAN1_FCFG53_TAP	0x40310458	FULL	Tap Value

9.2.55 FCFG 54

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG54_COEF	0x40310460	FULL	Coefficient Value
PACSS_DCHAN1_FCFG54_TAP	0x40310468	FULL	Tap Value

9.2.56 FCFG 55

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG55_COEF	0x40310470	FULL	Coefficient Value
PACSS_DCHAN1_FCFG55_TAP	0x40310478	FULL	Tap Value

9.2.57 FCFG 56

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG56_COEF	0x40310480	FULL	Coefficient Value
PACSS_DCHAN1_FCFG56_TAP	0x40310488	FULL	Tap Value

9.2.58 FCFG 57

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG57_COEF	0x40310490	FULL	Coefficient Value
PACSS_DCHAN1_FCFG57_TAP	0x40310498	FULL	Tap Value

9.2.59 FCFG 58

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG58_COEF	0x403104A0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG58_TAP	0x403104A8	FULL	Tap Value

9.2.60 FCFG 59

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG59_COEF	0x403104B0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG59_TAP	0x403104B8	FULL	Tap Value

9.2.61 FCFG 60

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG60_COEF	0x403104C0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG60_TAP	0x403104C8	FULL	Tap Value

9.2.62 FCFG 61

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG61_COEF	0x403104D0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG61_TAP	0x403104D8	FULL	Tap Value

9.2.63 FCFG 62

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG62_COEF	0x403104E0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG62_TAP	0x403104E8	FULL	Tap Value

9.2.64 FCFG 63

Register Name	Address	Permission	Description
PACSS_DCHAN1_FCFG63_COEF	0x403104F0	FULL	Coefficient Value
PACSS_DCHAN1_FCFG63_TAP	0x403104F8	FULL	Tap Value

9.3 DCHAN 2

Register Name	Address	Permission	Description
PACSS_DCHAN2_DCHAN_CTL	0x40320000	FULL	Digital Channel Control Note:FIR_EN FIR_NUM_TAPS are not available for this register
PACSS_DCHAN2_SMP_CTL	0x40320004	FULL	Sample Control
PACSS_DCHAN2_SMP_REF_CTL	0x40320008	FULL	Sample Reference Control
PACSS_DCHAN2_DEC_CTL	0x4032000C	FULL	Decimator Control
PACSS_DCHAN2_PP_CTL	0x40320010	FULL	Post Processing Control
PACSS_DCHAN2_OFST_COR	0x40320014	FULL	Offset Correction register
PACSS_DCHAN2_GAIN_COR	0x40320018	FULL	Gain Correction register
PACSS_DCHAN2_RANGE_LOW	0x4032001C	FULL	Range Detect low value register.
PACSS_DCHAN2_RANGE_HIGH	0x40320020	FULL	Range detect high value register.
PACSS_DCHAN2_PGA_GAIN_CTL	0x40320024	FULL	PGA Gain Control register
PACSS_DCHAN2_CAP_CFG0	0x40320028	FULL	Capacitor Configuration 0 register
PACSS_DCHAN2_CAP_CFG1	0x4032002C	FULL	Capacitor Configuration 1 register
PACSS_DCHAN2_CAP_CFG2	0x40320030	FULL	Capacitor Configuration 2 register
PACSS_DCHAN2_ACC_THRESH	0x40320034	FULL	Accumulated Data Threshold
PACSS_DCHAN2_RESULT	0x40320040	FULL	Channel result data register, updated at the end of each completed conversion
PACSS_DCHAN2_RESULT_TAG	0x40320044	FULL	Tag register associated and updated simultaneously with the RESULT register
PACSS_DCHAN2_ACC_RESULT	0x40320048	FULL	Channel Accumulated result data register
PACSS_DCHAN2_INTR	0x40320050	FULL	Interrupt request register
PACSS_DCHAN2_INTR_SET	0x40320054	FULL	Interrupt set request register
PACSS_DCHAN2_INTR_MASK	0x40320058	FULL	Interrupt mask register
PACSS_DCHAN2_INTR_MASKED	0x4032005C	FULL	Interrupt masked request register
PACSS_DCHAN2_STATUS	0x40320060	FULL	Status registesr

9.4 DCHAN 3

Register Name	Address	Permission	Description
PACSS_DCHAN3_DCHAN_CTL	0x40330000	FULL	Digital Channel Control Note:FIR_EN FIR_NUM_TAPS are not available for this register
PACSS_DCHAN3_SMP_CTL	0x40330004	FULL	Sample Control
PACSS_DCHAN3_SMP_REF_CTL	0x40330008	FULL	Sample Reference Control
PACSS_DCHAN3_DEC_CTL	0x4033000C	FULL	Decimator Control
PACSS_DCHAN3_PP_CTL	0x40330010	FULL	Post Processing Control
PACSS_DCHAN3_OFST_COR	0x40330014	FULL	Offset Correction register
PACSS_DCHAN3_GAIN_COR	0x40330018	FULL	Gain Correction register
PACSS_DCHAN3_RANGE_LOW	0x4033001C	FULL	Range Detect low value register.
PACSS_DCHAN3_RANGE_HIGH	0x40330020	FULL	Range detect high value register.
PACSS_DCHAN3_PGA_GAIN_CTL	0x40330024	FULL	PGA Gain Control register
PACSS_DCHAN3_CAP_CFG0	0x40330028	FULL	Capacitor Configuration 0 register
PACSS_DCHAN3_CAP_CFG1	0x4033002C	FULL	Capacitor Configuration 1 register
PACSS_DCHAN3_CAP_CFG2	0x40330030	FULL	Capacitor Configuration 2 register
PACSS_DCHAN3_ACC_THRESH	0x40330034	FULL	Accumulated Data Threshold

Register Name	Address	Permission	Description
PACSS_DCHAN3_RESULT	0x40330040	FULL	Channel result data register, updated at the end of each completed conversion
PACSS_DCHAN3_RESULT_TAG	0x40330044	FULL	Tag register associated and updated simultaneously with the RESULT register
PACSS_DCHAN3_ACC_RESULT	0x40330048	FULL	Channel Accumulated result data register
PACSS_DCHAN3_INTR	0x40330050	FULL	Interrupt request register
PACSS_DCHAN3_INTR_SET	0x40330054	FULL	Interrupt set request register
PACSS_DCHAN3_INTR_MASK	0x40330058	FULL	Interrupt mask register
PACSS_DCHAN3_INTR_MASKED	0x4033005C	FULL	Interrupt masked request register
PACSS_DCHAN3_STATUS	0x40330060	FULL	Status registesr

9.5 ACHAN 0

Register Name	Address	Permission	Description
PACSS_ACHAN0_ACHAN_CTL	0x40340000	FULL	Analog Channel Control
PACSS_ACHAN0_TR_CTL	0x40340004	FULL	Trigger Control for Sequencer
PACSS_ACHAN0_CHOP_CTL	0x40340008	FULL	Chopping Control for Sequencer
PACSS_ACHAN0_PGA_CTL	0x4034000C	FULL	Programmable Gain Amplifier Control
PACSS_ACHAN0_MOD_CTL	0x40340010	FULL	Modulator Control
PACSS_ACHAN0_DPATH_CTL	0x40340014	FULL	Datapath Control
PACSS_ACHAN0_BUF_CTL	0x40340018	FULL	Buffer Control
PACSS_ACHAN0_PUMP_CTL	0x40340020	FULL	Pump Control
PACSS_ACHAN0_REF_CTL	0x40340024	FULL	Reference Control
PACSS_ACHAN0_START	0x40340028	FULL	Start Conversion
PACSS_ACHAN0_INMUX_CTL	0x4034002C	FULL	INMUX Control
PACSS_ACHAN0_DEM_CTL	0x40340030	FULL	Dynamic Element Matching Control
PACSS_ACHAN0_SWITCH	0x40340034	FULL	Firmware Switch Control
PACSS_ACHAN0_SWITCH_CLEAR	0x40340038	FULL	Firmware Switch Control Clear
PACSS_ACHAN0_SWITCH_SQ_CTL	0x4034003C	FULL	Switch Sequencer Control
PACSS_ACHAN0_SWITCH_STATUS	0x40340040	FULL	Switch Status
PACSS_ACHAN0_DFT_CTL	0x40340044	FULL	DFT Control Register
PACSS_ACHAN0_DFT_STATUS	0x40340048	FULL	DFT Status Register
PACSS_ACHAN0_TRIM_PGA0_CTL	0x4034FF00	FULL	PGA Trim 0 (lock protected)
PACSS_ACHAN0_TRIM_PGA1_CTL	0x4034FF04	FULL	PGA Trim 1 (lock protected)
PACSS_ACHAN0_TRIM_PGA2_CTL	0x4034FF08	FULL	PGA Trim 2 (lock protected)
PACSS_ACHAN0_TRIM_PGA3_CTL	0x4034FF0C	FULL	PGA Trim 3 (lock protected)
PACSS_ACHAN0_TRIM_PGA4_CTL	0x4034FF10	FULL	PGA Trim 4 (lock protected)
PACSS_ACHAN0_TRIM_BUF0_CTL	0x4034FF14	FULL	Buffer Trim 0 (lock protected)
PACSS_ACHAN0_TRIM_BUF1_CTL	0x4034FF18	FULL	Buffer Trim 1 (lock protected)
PACSS_ACHAN0_TRIM_BUF2_CTL	0x4034FF1C	FULL	Buffer Trim 2 (lock protected)
PACSS_ACHAN0_TRIM_BUF3_CTL	0x4034FF20	FULL	Buffer Trim 3 (lock protected)

9.6 ACHAN 1

Register Name	Address	Permission	Description
PACSS_ACHAN1_ACHAN_CTL	0x40350000	FULL	Analog Channel Control
PACSS_ACHAN1_TR_CTL	0x40350004	FULL	Trigger Control for Sequencer
PACSS_ACHAN1_CHOP_CTL	0x40350008	FULL	Chopping Control for Sequencer
PACSS_ACHAN1_PGA_CTL	0x4035000C	FULL	Programmable Gain Amplifier Control
PACSS_ACHAN1_MOD_CTL	0x40350010	FULL	Modulator Control
PACSS_ACHAN1_DPATH_CTL	0x40350014	FULL	Datapath Control
PACSS_ACHAN1_BUF_CTL	0x40350018	FULL	Buffer Control
PACSS_ACHAN1_PUMP_CTL	0x40350020	FULL	Pump Control
PACSS_ACHAN1_REF_CTL	0x40350024	FULL	Reference Control
PACSS_ACHAN1_START	0x40350028	FULL	Start Conversion
PACSS_ACHAN1_INMUX_CTL	0x4035002C	FULL	INMUX Control
PACSS_ACHAN1_DEM_CTL	0x40350030	FULL	Dynamic Element Matching Control
PACSS_ACHAN1_SWITCH	0x40350034	FULL	Firmware Switch Control
PACSS_ACHAN1_SWITCH_CLEAR	0x40350038	FULL	Firmware Switch Control Clear
PACSS_ACHAN1_SWITCH_SQ_CTL	0x4035003C	FULL	Switch Sequencer Control
PACSS_ACHAN1_SWITCH_STATUS	0x40350040	FULL	Switch Status
PACSS_ACHAN1_DFT_CTL	0x40350044	FULL	DFT Control Register
PACSS_ACHAN1_DFT_STATUS	0x40350048	FULL	DFT Status Register
PACSS_ACHAN1_TRIM_PGA0_CTL	0x4035FF00	FULL	PGA Trim 0 (lock protected)

Register Name	Address	Permission	Description
PACSS_ACHAN1_TRIM_PGA1_CTL	0x4035FF04	FULL	PGA Trim 1 (lock protected)
PACSS_ACHAN1_TRIM_PGA2_CTL	0x4035FF08	FULL	PGA Trim 2 (lock protected)
PACSS_ACHAN1_TRIM_PGA3_CTL	0x4035FF0C	FULL	PGA Trim 3 (lock protected)
PACSS_ACHAN1_TRIM_PGA4_CTL	0x4035FF10	FULL	PGA Trim 4 (lock protected)
PACSS_ACHAN1_TRIM_BUF0_CTL	0x4035FF14	FULL	Buffer Trim 0 (lock protected)
PACSS_ACHAN1_TRIM_BUF1_CTL	0x4035FF18	FULL	Buffer Trim 1 (lock protected)
PACSS_ACHAN1_TRIM_BUF2_CTL	0x4035FF1C	FULL	Buffer Trim 2 (lock protected)
PACSS_ACHAN1_TRIM_BUF3_CTL	0x4035FF20	FULL	Buffer Trim 3 (lock protected)

9.7 MMIO

Register Name	Address	Permission	Description
PACSS_MMIO_PACSS_CTL	0x403F0000	FULL	Precision Analog Channel Control Note:OCD0_EN OCD1_EN are not available for this register
PACSS_MMIO_AGC_CTL0	0x403F0004	FULL	Auto-Gain Correction Control 0
PACSS_MMIO_AGC_CTL1	0x403F0008	FULL	Auto-Gain Correction Control 1
PACSS_MMIO_AGC_CTL2	0x403F000C	FULL	Auto-Gain Correction Control 2
PACSS_MMIO_AGC_CTL3	0x403F0010	FULL	Auto-Gain Correction Control 3
PACSS_MMIO_TMPS_CTL	0x403F0020	FULL	Temperature Sensor Control
PACSS_MMIO_VPOS_PUMP_CTL	0x403F0024	FULL	Positive Pump Control
PACSS_MMIO_START	0x403F0030	FULL	Start Conversion
PACSS_MMIO_INTR	0x403F0040	FULL	System Interrupt request register Note:OCD0_TRIGGER OCD0_UNFILTERED OCD0_FAULT OCD1_TRIGGER OCD1_UNFILTERED OCD1_FAULT are not available for this register
PACSS_MMIO_INTR_SET	0x403F0044	FULL	System Interrupt set request register Note:OCD0_TRIGGER_SET OCD0_UNFILTERED_SET OCD0_FAULT_SET OCD1_TRIGGER_SET OCD1_UNFILTERED_SET OCD1_FAULT_SET are not available for this register
PACSS_MMIO_INTR_MASK	0x403F0048	FULL	System Interrupt mask register Note:OCD0_TRIGGER_MASK OCD0_UNFILTERED_MASK OCD0_FAULT_MASK OCD1_TRIGGER_MASK OCD1_UNFILTERED_MASK OCD1_FAULT_MASK are not available for this register
PACSS_MMIO_INTR_MASKED	0x403F004C	FULL	System Interrupt masked request register Note:OCD0_TRIGGER_MASKED OCD0_UNFILTERED_MASKED OCD0_FAULT_MASKED OCD1_TRIGGER_MASKED OCD1_UNFILTERED_MASKED OCD1_FAULT_MASKED are not available for this register
PACSS_MMIO_INTR_CAUSE	0x403F0050	FULL	Interrupt Cause Register
PACSS_MMIO_STATUS0	0x403F0060	FULL	Status Register 0
PACSS_MMIO_STATUS1	0x403F0064	FULL	Status Register 1
PACSS_MMIO_HPBGR_CTL	0x403F0500	FULL	High Precision Bandgap Reference Control
PACSS_MMIO_HPBGR_DFT_CTL	0x403F0510	FULL	High Precision Bandgap Reference DFT Control
PACSS_MMIO_AREF_CTL	0x403F0600	FULL	Analog Reference Control
PACSS_MMIO_AREF_DFT_CTL	0x403F0610	FULL	Analog Reference DFT Control
PACSS_MMIO_REG_PROT	0x403F0800	FULL	Register Protection
PACSS_MMIO_PDFT_CTL	0x403F0900	FULL	PACSS DFT Control
PACSS_MMIO_TRIM_REGL0_CTL	0x403FFF00	FULL	Regulator (LDO) Trim 0 (lock protected)
PACSS_MMIO_TRIM_HPBGR0_CTL	0x403FFF04	FULL	High Precision Bandgap Reference Trim Control 0 (lock protected)
PACSS_MMIO_TRIM_HPBGR1_CTL	0x403FFF08	FULL	High Precision Bandgap Reference Trim Control 1 (lock protected)
PACSS_MMIO_TRIM_HPBGR2_CTL	0x403FFF0C	FULL	High Precision Bandgap Reference Trim Control 2 (lock protected)
PACSS_MMIO_TRIM_HPBGR3_CTL	0x403FFF10	FULL	High Precision Bandgap Reference Trim Control 3 (lock protected)
PACSS_MMIO_TRIM_HPBGR4_CTL	0x403FFF14	FULL	High Precision Bandgap Reference Trim Control 4 (lock protected)
PACSS_MMIO_TRIM_AREF0_CTL	0x403FFF18	FULL	Analog Reference Trim Control 0 (lock protected)
PACSS_MMIO_TRIM_AREF1_CTL	0x403FFF1C	FULL	Analog Reference Trim Control 1 (lock protected)
PACSS_MMIO_TRIM_AREF2_CTL	0x403FFF20	FULL	Analog Reference Trim Control 2 (lock protected)

Register Name	Address	Permission	Description
PACSS_MMIO_TRIM_AREF3_CTL	0x403FFF24	FULL	Analog Reference Trim Control 3 (lock protected)
PACSS_MMIO_TRIM_AREF4_CTL	0x403FFF28	FULL	Analog Reference Trim Control 4 (lock protected)
PACSS_MMIO_TRIM_AREF5_CTL	0x403FFF2C	FULL	Analog Reference Trim Control 5 (lock protected)
PACSS_MMIO_TRIM_AREF6_CTL	0x403FFF30	FULL	Analog Reference Trim Control 6 (lock protected)

9.7.1 GAINLVL_STRUCT 0

Register Name	Address	Permission	Description
PACSS_MMIO_GAIN_CFG00	0x403F0100	FULL	Gain configuration register 0
PACSS_MMIO_GAIN_CFG10	0x403F0104	FULL	Gain configuration register 1
PACSS_MMIO_OFST_COR0	0x403F0108	FULL	Offset Correction register
PACSS_MMIO_GAIN_COR0	0x403F010C	FULL	Gain Correction register

9.7.2 GAINLVL_STRUCT 1

Register Name	Address	Permission	Description
PACSS_MMIO_GAIN_CFG01	0x403F0110	FULL	Gain configuration register 0
PACSS_MMIO_GAIN_CFG11	0x403F0114	FULL	Gain configuration register 1
PACSS_MMIO_OFST_COR1	0x403F0118	FULL	Offset Correction register
PACSS_MMIO_GAIN_COR1	0x403F011C	FULL	Gain Correction register

9.7.3 GAINLVL_STRUCT 2

Register Name	Address	Permission	Description
PACSS_MMIO_GAIN_CFG02	0x403F0120	FULL	Gain configuration register 0
PACSS_MMIO_GAIN_CFG12	0x403F0124	FULL	Gain configuration register 1
PACSS_MMIO_OFST_COR2	0x403F0128	FULL	Offset Correction register
PACSS_MMIO_GAIN_COR2	0x403F012C	FULL	Gain Correction register

9.7.4 GAINLVL_STRUCT 3

Register Name	Address	Permission	Description
PACSS_MMIO_GAIN_CFG03	0x403F0130	FULL	Gain configuration register 0
PACSS_MMIO_GAIN_CFG13	0x403F0134	FULL	Gain configuration register 1
PACSS_MMIO_OFST_COR3	0x403F0138	FULL	Offset Correction register
PACSS_MMIO_GAIN_COR3	0x403F013C	FULL	Gain Correction register

9.7.5 GAINLVL_STRUCT 4

Register Name	Address	Permission	Description
PACSS_MMIO_GAIN_CFG04	0x403F0140	FULL	Gain configuration register 0
PACSS_MMIO_GAIN_CFG14	0x403F0144	FULL	Gain configuration register 1
PACSS_MMIO_OFST_COR4	0x403F0148	FULL	Offset Correction register
PACSS_MMIO_GAIN_COR4	0x403F014C	FULL	Gain Correction register

9.7.6 GAINLVL_STRUCT 5

Register Name	Address	Permission	Description
PACSS_MMIO_GAIN_CFG05	0x403F0150	FULL	Gain configuration register 0
PACSS_MMIO_GAIN_CFG15	0x403F0154	FULL	Gain configuration register 1
PACSS_MMIO_OFST_COR5	0x403F0158	FULL	Offset Correction register
PACSS_MMIO_GAIN_COR5	0x403F015C	FULL	Gain Correction register

9.7.7 GAINLVL_STRUCT 6

Register Name	Address	Permission	Description
PACSS_MMIO_GAIN_CFG06	0x403F0160	FULL	Gain configuration register 0
PACSS_MMIO_GAIN_CFG16	0x403F0164	FULL	Gain configuration register 1
PACSS_MMIO_OFST_COR6	0x403F0168	FULL	Offset Correction register
PACSS_MMIO_GAIN_COR6	0x403F016C	FULL	Gain Correction register

9.7.8 GAINLVL_STRUCT 7

Register Name	Address	Permission	Description
PACSS_MMIO_GAIN_CFG07	0x403F0170	FULL	Gain configuration register 0
PACSS_MMIO_GAIN_CFG17	0x403F0174	FULL	Gain configuration register 1
PACSS_MMIO_OFST_COR7	0x403F0178	FULL	Offset Correction register
PACSS_MMIO_GAIN_COR7	0x403F017C	FULL	Gain Correction register

9.7.9 GAINLVL_STRUCT 8

Register Name	Address	Permission	Description
PACSS_MMIO_GAIN_CFG08	0x403F0180	FULL	Gain configuration register 0
PACSS_MMIO_GAIN_CFG18	0x403F0184	FULL	Gain configuration register 1
PACSS_MMIO_OFST_COR8	0x403F0188	FULL	Offset Correction register
PACSS_MMIO_GAIN_COR8	0x403F018C	FULL	Gain Correction register

9.7.10 GAINLVL_STRUCT 9

Register Name	Address	Permission	Description
PACSS_MMIO_GAIN_CFG09	0x403F0190	FULL	Gain configuration register 0
PACSS_MMIO_GAIN_CFG19	0x403F0194	FULL	Gain configuration register 1
PACSS_MMIO_OFST_COR9	0x403F0198	FULL	Offset Correction register
PACSS_MMIO_GAIN_COR9	0x403F019C	FULL	Gain Correction register

9.8 Register Details

9.8.1 DCHAN

9.8.1.1 PACSS_DCHAN_DCHAN_CTL

Description: Digital Channel Control
Address: 0x40300000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xF0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	FIR_NUM_TAPS [7:4]				None [3:3]	FIR_EN [2:2]	PP_EN [1:1]	AGC_GAIN_EN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						FIR_NUM_TAPS [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLE [31:31]	SEC_EN [30:30]	None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	AGC_GAIN_EN	RW	R	0	AGC Gain Enable 0 - Digital channel uses gain values from dchan configuration 1 - Digital channel uses gain values provided from AGC
1	PP_EN	RW	R	0	Post Processor Enable Enables all features of the post processor including the accumulated result register. When disabled the post processor is bypassed.
2	FIR_EN	RW	R	0	FIR Enable 0 - Disabled 1 - Enabled
4:9	FIR_NUM_TAPS	RW	R	15	FIR number of Taps. FIR_NUM_TAPS + 1 equals the numbers of Taps enabled in the FIR Filter

Bits	Name	SW	HW	Default or Enum	Description
30	SEC_EN	RW	R	0	Secondary Channel Enable Use case is for diagnostic or temperature measurements. When a digital channel is set as secondary, when it is triggered, by a secondary trigger, the conversion of the channel pends until the next primary conversion completes. Secondary channels should always have a higher dchan index than the enabled primary channels associated with the same analog channel (ACHAN). For example if both dchan0 and dchan1 are using achan0, then dchan0 should never be set as a secondary channel. 0 - digital channel is configured as primary channel 1 - digital channel is configured as secondary channel
31	ENABLE	RW	R	0	Enable Digital Channel

9.8.1.2 PACSS_DCHAN_SMP_CTL

Description: Sample Control
Address: 0x40300004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: The configuration of this register is applied to the analog channel on the start of a conversion, and maintained until its configuration is overwritten by the start of another digital channel configuration
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	POS_PIN_SEL [7:4]				None [3:1]			ACHAN _SEL [0:0]

Bits	15	14	13	12	11	10	9	8
Name	NEG_PIN_SEL [15:12]				None [11:11]	POS_PIN_SEL [10:8]		

Bits	23	22	21	20	19	18	17	16
Name	CH_SEL_DLY [23:20]				AAF _SHORT_R _EN [19:19]	BYPASS _AAF [18:18]	None [17:17]	NEG_PIN _SEL [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:31]	MOV_SUM [30:30]	AVG_MODE [29:28]		CH_SEL_DLY [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ACHAN_SEL	RW	R	0	Analog Channel Selection Select which analog to use with this digital channel. 0 - Analog Channel 0 1 - Analog Channel 1
4:10	POS_PIN_SEL	RW	R	0	Positive Pin Select (Sequencer controlled)
	POS_PIN_SEL_HVDIV0			0	0x00 - hvdiv0, High Voltage Divider 0 (If VSENS pin is a package pin, the divider is connected to this pin, otherwise the divider is built into the HV Regulator and connected to the VBAT pin)
	POS_PIN_SEL_HVDIV1			4	0x04 - hvdiv1, High Voltage Divider 1 (Not applicable if VDIAG pin is not a package pin, in which case these bits can be used as spare bits or ignored)
	POS_PIN_SEL_VTS			8	0x08 - vts, External (NTC) temperature
	POS_PIN_SEL_VTINT			12	0x0C - vtint, Internal Temp Sensor
	POS_PIN_SEL_VG0			16	0x10 - vg0, vssa
	POS_PIN_SEL_VG1			17	0x11 - vg1, vssd
	POS_PIN_SEL_VG2			18	0x12 - vg2, vssl
	POS_PIN_SEL_VG3			19	0x13 - vg3, vrefl
	POS_PIN_SEL_VG4			20	0x14 - vg4, unused (floating)
	POS_PIN_SEL_VG5			21	0x15 - vg5, vts_ret_k
	POS_PIN_SEL_VG6			22	0x16 - vg6, vtint_ret, internal temp sense
	POS_PIN_SEL_VG7			23	0x17 - vg7, vsub
	POS_PIN_SEL_VS0			24	0x18 - vs0, vccd2/2
	POS_PIN_SEL_VS1			25	0x19 - vs1, vcca_dsm/2

Bits	Name	SW	HW	Default or Enum	Description
	POS_PIN_SEL_VS2			26	0x1A - vs2, vdda/4
	POS_PIN_SEL_VS3			27	0x1B - vs3, vddd/4
	POS_PIN_SEL_VR0			28	0x1C - vr0, 1.2V vrefh (hpbgr)
	POS_PIN_SEL_VR1			29	0x1D - vr1, 0.8V vref (hpbgr)
	POS_PIN_SEL_VR2			30	0x1E - vr2, 0.7V vref (hpbgr)
	POS_PIN_SEL_VR3			31	0x1F - vr3, 1.2V vref (srss)
	POS_PIN_SEL_GPIO0			32	0x20 - gpio0
	POS_PIN_SEL_GPIO1			36	0x24 - gpio1
	POS_PIN_SEL_GPIO2			40	0x28 - gpio2
	POS_PIN_SEL_GPIO3			44	0x2C - gpio3
	POS_PIN_SEL_GPIO4			48	0x30 - gpio4
	POS_PIN_SEL_GPIO5			52	0x34 - gpio5
	POS_PIN_SEL_GPIO6			56	0x38 - gpio6
	POS_PIN_SEL_GPIO7			60	0x3C - gpio7
	POS_PIN_SEL_RSH0			64	0x40 - rsh0
	POS_PIN_SEL_RSH1			96	0x60 - rsh1
	POS_PIN_SEL_AMUXA			122	0x7A - amuxbusa, if selected neg_pin_sel should be set to amuxbusb
	POS_PIN_SEL_AMUXB			123	0x7B - amuxbusb, if selected neg_pin_sel should be set to amuxbusa
12:16	NEG_PIN_SEL	RW	R	0	Negative Pin Select
	NEG_PIN_SEL_VSSA			0	0x00 - vssa
	NEG_PIN_SEL_VSSA_K0			8	0x08 - vssa_k0, unused (floating)
	NEG_PIN_SEL_VSSA_K1			9	0x09 - vssa_k1, vrefl
	NEG_PIN_SEL_VSSA_K2			10	0x0A - vssa_k2, srss_vss
	NEG_PIN_SEL_VSSA_K3			11	0x0B - vssa_k3, vdiv_ret
	NEG_PIN_SEL_VSSA_K4			12	0x0C - vssa_k4, vts_ret
	NEG_PIN_SEL_VSSA_K5			13	0x0D - vssa_k5, vtint_ret
	NEG_PIN_SEL_VSSA_K6			14	0x0E - vssa_k6, gpio0
	NEG_PIN_SEL_VSSA_K7			15	0x0F - vssa_k7, gpio2
	NEG_PIN_SEL_RSL0			16	0x10 - rsl0
	NEG_PIN_SEL_RSL1			24	0x18 - rsl1
	NEG_PIN_SEL_AMUXA			26	0x1A - amuxbusa, if selected pos_pin_sel should be set to amuxbusb
	NEG_PIN_SEL_AMUXB			27	0x1B - amuxbusb, if selected pos_pin_sel should be set to amuxbusa
18	BYPASS_AAF	RW	R	0	Bypass the Anti-Aliasing Filter Open SW1, SW2, SW4, and close SW3 of the AAF during this channels conversion
19	AAF_SHORT_R_EN	RW	R	0	Automatically short the Anti-Aliasing Filter resistor during the channel selection delay. The expectation is that his will decrease the required settling time. Has no affect if BYPASS_AAF=1

Bits	Name	SW	HW	Default or Enum	Description
20:27	CH_SEL_DLY	RW	R	0	Channel Selection Delay. The value written to this field, plus 1, is the number of DSM clock cycles that will be inserted after the virtual channel configuration is loaded and before the decimator is started. Ex: write 7 for 8 clock cycles.
28:29	AVG_MODE	RW	R	0	Average Mode (moving average)) When enabled takes the moving average of sinc3/sinc4 decimator output. 0 - off 1 - moving average, last 2 samples 2 - moving average, last 4 samples 3 - reserved (DEC_CTL.DR2+1) must be greater than 1 if AVG_MODE is enabled. Otherwise results will never generate a data valid trigger/interrupt. The sample count and memory of the moving average/sum is reset at the start of every conversion.
30	MOV_SUM	RW	R	0	Moving Sum 0 - Off 1 - When AVG_MODE is enabled, no right shift occurs to divided result. Ex. If AVG_MODE=1 then the result is the sum of the last two samples. This register takes no affect when AVG_MODE=0.

9.8.1.3 PACSS_DCHAN_SMP_REF_CTL

Description: Sample Reference Control
Address: 0x40300008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment: The configuration of this register is applied to the analog channel on the start of a conversion, and maintained until its configuration is overwritten by the start of another digital channel configuration
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		VREFL_SEL [5:4]		None [3:3]	VREFH_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							VREF_BUF_EN [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:19]					RS_PULLUP_EN [18:18]	RS_PULLUP_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	VREFH_SEL	RW	R	0	VREFH selection
	VREFH_SEL_VREFH_DIRECT			0	VREFH Direct (HPBGR)
	VREFH_SEL_VREFH_BUFFERED			1	VREFH Buffered (HPBGR)
	VREFH_SEL_SRSS			2	VREF SRSS
	VREFH_SEL_VTS_REF			3	VTS_REF
	VREFH_SEL_VDDA_DIV4			4	VDDA/4
	VREF_HSEL_VDDA_DIV3			5	VDDA/3
4:5	VREFL_SEL	RW	R	0	VREFL selection
	VREFL_SEL_VREFL			0	VREFL
	VREFL_SEL_VSSA_SRSS			1	VSSA_SRSS
	VREFL_SEL_VSSA_KELVIN			2	VSSA_KELVIN
	VREFL_SEL_VTS_RET			3	VTS_RET

Bits	Name	SW	HW	Default or Enum	Description
8	VREF_BUF_EN	RW	R	0	VREF Buffer Enable VREF_BUF_EN should only be used when a reference other than the default reference (HPBGR 0.1 percent reference) is used. When the HPBGR reference is used, the reference is provided directly from the HPBGR with the help from external cap for the transients. If this bit is set on a secondary channel, vref_buf_en for the assigned analog channel will be set once the secondary channel is pended to allow enough ramp up time of the VREFH buffer so that it is ready to sample once the secondary channel is ready to convert. The required ramp-up time of the VREFH buffer is 6 us, it is on the user to ensure the secondary channel is pended early enough to ensure this ramp-up time if the associated primary channel does not have this bit set.
16:17	RS_PULLUP_SEL	RW	R	0	Resistor Pull-up Select Based on the selection, the pin is pulled-up to VDDA via 4k-ohm (typ) resistor for open wire detection.
	RS_PULLUP_SEL_RSH1			0	RSH[1] Pull-up Selected
	RS_PULLUP_SEL_RSH0			1	RSH[0] Pull-up Selected
	RS_PULLUP_SEL_RSL1			2	RSL[1] Pull-up Selected
	RS_PULLUP_SEL_RSL0			3	RSL[0] Pull-up Selected
18	RS_PULLUP_EN	RW	R	0	Resistor Pull-up Enable

9.8.1.4 PACSS_DCHAN_DEC_CTL

Description: Decimator Control
Address: 0x4030000C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x53F0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DR [7:4]				GCOR_EN [3:3]	OCOR_EN [2:2]	CONV_MODE [1:1]	SINC_MODE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	DR2 [15:12]				SAT_EN [11:11]	DR [10:8]		

Bits	23	22	21	20	19	18	17	16
Name	SHIFTL [23:20]				None [19:17]			DR2 [16:16]

Bits	31	30	29	28	27	26	25	24
Name	RR_SHIFTR [31:28]				DEC_SHIFTR [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	SINC_MODE	RW	R	0	Decimator Sinc Mode 0 - Sinc3, Decimator is configured as a 3-state CIC decimation filter 1 - Sinc4, Decimator is configured as a 4-stage CIC decimation filter
1	CONV_MODE	RW	R	0	Conversion Mode 0 - Incremental (Single Sample) 1 - Continuous This bit can be cleared during a continuous conversion to end the sample. In the expected use case: Primary channels should use Continuous, while secondary channels should be set to Incremental.

Bits	Name	SW	HW	Default or Enum	Description
2	OCOR_EN	RW	R	0	Offset Correction Enable This bit controls the offset correction feature of the Decimator filter. The offset value is programmed in the OCOR bits of the OFST_COR register. Conversion results are unpredictable if this bit is changed while the filter is running. This must be set to use DCHAN.OFST_COR or GAIN_LVL_STRUCT.OFST_COR, which one it chooses is based on DCHAN_CTL.AGC_GAIN_EN. If OCOR_EN and GCOR_EN are both disabled this prevents the capability to loop back the data valid HW trigger of this channel and use it as the conversion start HW trigger of this channel. If either GCOR or OCOR is enabled this is allowed.
3	GCOR_EN	RW	R	0	Gain Correction Enable This bit controls the gain correction feature of the Decimator filter. The gain coefficient is programmed in the GCOR bits of the GAIN_COR register. Which bits in this 16-bit field that are valid is set in GVAL. Conversion results are unpredictable if this bit is changed while the filter is running. When this feature is enabled, the DR register field must be set to a value higher than 32 (worst case) for proper operation. See the DR register definition of cases where values less than 32 are allowed. This must be set to use DCHAN.GAIN_COR or GAIN_LVL_STRUCT.GAIN_COR. The value chosen, is based on DCHAN_CTL.AGC_GAIN_EN If OCOR_EN and GCOR_EN are both disabled this prevents the capability to loop back the data valid HW trigger of this channel and use it as the conversion start HW trigger of this channel. If either GCOR or OCOR is enabled this is allowed.

Bits	Name	SW	HW	Default or Enum	Description
4:10	DR	RW	R	63	Decimation Ratio DR is an 7-bit field that sets the decimation ratio (DR+1) in the sinc3/sinc4 CIC filter. The decimation ratio minus one is the value that is programmed into this register. Changing this field during a conversion will disrupt the output value. Conversion results are unpredictable if these bits are changed while the filter is running. The suggested minimum value of DR is 0x3F. If a lower value is required, the minimum DR is determined by GVAL if gain is enabled. DR > (GCOR_COR.GVAL) * 2 when GCOR_EN is set to 1. An example of some acceptable values for DR/DR2: Data Rate: DR+1: DR2+1: 48ksps 64 1 8ksps 64 6 4ksps 128 6 2ksps 128 12 1ksps 128 24
11	SAT_EN	RW	R	0	Saturation Enable Controls saturation logic in the Decimator. When enabled, gain and offset calculations are held to the most positive or negative values, rather then wrapping around. Conversion results are unpredictable if this bit is changed while during a conversion. This bit is ignored if OCOR_EN and GCOR_EN are all 0. This feature is used to prevent wrap-around if the decimator is incorrectly configured. This bit should be set to 1 if OCOR_EN or GCOR_EN is set to 1.
12:16	DR2	RW	R	5	Decimation Ratio 2 DR2 is a 5-bit field that sets the decimation ratio (DR2+1) of the sinc2 rate reducer within the Decimator. The decimation ratio of the rate reducer minus one is the value that is programmed into this register. This field should not be changed during a conversion. DR2 must be less than DR/2. An example of some acceptable values for DR/DR2: Data Rate: DR+1: DR2+1: 48ksps 64 1 8ksps 64 6 4ksps 128 6 2ksps 128 12 1ksps 128 24

Bits	Name	SW	HW	Default or Enum	Description
20:23	SHIFTL	RW	R	0	Shift Left (Scaler) Value for left shift amount of modulator input data. Supported values are 0 - 9. Using values 10-15 may result in a loss of data This register provides control information to the input (left) shifter. SHIFTL is a 4-bit field that sets the amount of left shift that the Modulator input will be shifted. Disturbing this field during a conversion will disturb the output value. This register should only be updated while the CIC filter is in the Standby state. Conversion results are unpredictable if these bits are changed while the filter is running. A read of this register produces the last value written to this register. This value is overridden by the Gain Level setting when DCHAN_CTL.AGC_GAIN_EN=1
24:27	DEC_SHIFTR	RW	R	0	Decimator Output Right Shift The maximum data path of the sinc4 filter is 42-bits. This shift register is used to align the resolution down to 32-bits, otherwise the MSB bits will be truncated. To avoid truncation of relevant bits, the min value for this register should be: log2(qlev) + max(SHIFTL) + N*log2(DR +1) - (32 - log2(U)) Where U = 1 for moving sum disabled, 2 for moving sum with avg mode=2 samples, and 4 for moving sum w/ avg mode =4 samples where N = # of sinc stages (either 3 or 4 depending on sinc_mode field). In the equation above DR and DR2 are the values used in register programming (decimation ratios minus one)
28:31	RR_SHIFTR	RW	R	0	Rate Reducer Output Right Shift The maximum data path of the sinc2 rate reducer filter is 42-bits . This shift register is used to align the resolution down to 32-bits, otherwise the MSB bits will be truncated. To avoid truncation of relevant bits, the min value for this register should be: log2(qlev) + max(SHIFTL) + N*log2(DR +1) +2*log2(DR2+1) - DEC_SHIFTR - (32 - log2(U)) Where U = 1 for moving sum disabled, 2 for moving sum with avg mode=2 samples, and 4 for moving sum w/ avg mode =4 samples where DR2 is the values used in register programming (decimation ratios minus one)

9.8.1.5 PACSS_DCHAN_PP_CTL

Description: Post Processing Control
Address: 0x40300010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				PP_SHIFTR [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							CLAMP [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:22]		RANGE_COND [21:20]		None [19:18]		RANGE_DET_EN [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	RANGE_CNT_VAL [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	PP_SHIFTR	RW	R	0	Post Processor Right Shift Value for the amount of right shift for the input of the post processor (output of the FIR filter). The right shift operation is the first Post Processor operation. Processor. Functional values range from 0 to 15, 0 = no shift. This shift value will be based on the values of the FIR coefficients and the number of FIR taps. If the FIR is disabled, this value can be 0. If the FIR is enabled this shift value can be calculated by using the following: datapath bandwith: dp_bw = log2(qlev) + max(SHIFTL) + N*log2(DR +1) +2*log2(DR2+1) - DEC_SHIFTR - RR_SHIFTR FIR datapath adjustment: fir_dp_adj = log2(coeff[0] + coeff[1] + ... + coeff[n]) pp_shiftr = dp_bw + fir_adj -32
8	CLAMP	RW	R	0	Clamp 0 - Disabled (32-bit result) 1 - Clamps Result Data to 24-bits When enabled the max positive value will be clamped to 0x7FFFFF and the max negative value will be clamped to 0x800000.
16:17	RANGE_DET_EN	RW	R	0	Range Detection Enable 00 - off 01 - Range Detection Enabled 10 - Range Detection w/ counter (for glitch filtering) 11 - Reserved

Bits	Name	SW	HW	Default or Enum	Description
20:21	RANGE_COND	RW	R	0	Range Condition Select 0 - result < RANGE_LOW 1 - RANGE_LOW <= result < RANGE_HIGH 2 - RANGE_HIGH <= result 3 - result < RANGE_LOW || RANGE_HIGH <= result
24:31	RANGE_CNT_VAL	RW	R	4	Range Detection Count Value This register limits RANGE_INTR from asserting unless enough range detections have occurred. It is only used when RANGE_DET_EN=2'b10 mode. The range detection counter increments when a sample meets the range condition and decrements otherwise. When the range detection counter matches the RANGE_CNT_VAL the RANGE_INTR is asserted.

9.8.1.6 PACSS_DCHAN_OFST_COR

Description: Offset Correction register
Address: 0x40300014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	OCOR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	OCOR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				OCOR_SCLR [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	OCOR	RW	R	0	Decimator Offset Correction Coefficient OCOR is a 16-bit 2's compliment signed field that is the offset correction value used if the decimator Offset feature is enabled. This register may be written while the filter is running. OCOR<<OCOR_SCLR will be added to the decimation result.
16:19	OCOR_SCLR	RW	R	0	Decimator Offset Correction Coefficient Scaler OCOR_SCLR is the left shift amount to where the OCOR is applied to the decimation result. OCOR << OCOR_SCLR will be added to the decimation result.

9.8.1.7 PACSS_DCHAN_GAIN_COR

Description: Gain Correction register
Address: 0x40300018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xF0000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	GCOR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	GCOR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				GVAL [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	GCOR	RW	R	0	Decimator Gain Correction Coefficient
16:19	GVAL	RW	R	15	Number of valid bits minus one in Gain Coefficient registers GCOR GVAL is a 4-bit field that signifies to the HW how many bits of GCOR field are valid. The number of valid bits minus one should be written (0000b = 1 bit, 1111b = all 16 bits). Updates to this register will be ignored until the start of the next multiply. This register may be written while the filter is running. The valid field is measured from LSB (bit 0) up. Note that the HW always assumes the field specified by GVAL is left justified (starts at bit 0 of GCOR) and has a binary-point after the left-most digit. For example, if GVAL is programmed with a 7d, this means there are 8 valid bits in GCOR and they have the format x.xxxxxxxb. If GCOR holds the value 00000000 10100000b and GVAL is 7, only the low-order 8 bits are considered (10100000b) and the binary point is assumed after the left-most digit (1.0100000b). The multiply coefficient in the example would be 1.25d. Although a good explanation example, this isn't the most efficient way to multiply by 1.25d. Better would be GCOR holds the value 00000000 00000101b and GVAL is 2, which gives (1.01b). Another example: If it is desired to multiply by a gain coefficient of 0.125d (0.001b) then GCOR would be programmed with a value of 00000001b, GCORH with 00000000b and GVAL (GVAL) with 0011b - meaning there are 4 valid bits x.xxxb. The multiplier thus has a coefficient range of 1/(2^15) to 2.0-(1/(2^15)) in steps of 1/(2^15)

9.8.1.8 PACSS_DCHAN_RANGE_LOW

Description: Range Detect low value register.
Address: 0x4030001C
Offset: 0x1C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RANGE_LOW [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RANGE_LOW [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	RANGE_LOW [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	RANGE_LOW [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	RANGE_LOW	RW	R	0	Low threshold for range detect

9.8.1.9 PACSS_DCHAN_RANGE_HIGH

Description: Range detect high value register.
Address: 0x40300020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x7FFFFFFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RANGE_HIGH [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RANGE_HIGH [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	RANGE_HIGH [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	RANGE_HIGH [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	RANGE_HIGH	RW	R	2147483647	High threshold for range detect

9.8.1.10 PACSS_DCHAN_PGA_GAIN_CTL

Description: PGA Gain Control register
Address: 0x40300024
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					GAIN [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	GAIN	RW	R	0	PGA Gain setting of 1,2,4,8,16, 32 are supported This gain setting is overridden by AGC values if PACSS_CTL.AGC_EN=1 and DCHAN_CTL.AGC_GAIN_EN=1. Therefore the current value of the PGA gain can not be read from this register during AGC mode
	GAIN_1X			0	1x
	GAIN_2X			1	2x
	GAIN_4X			2	4x
	GAIN_8X			3	8x
	GAIN_16X			4	16x
	GAIN_32X			5	32x

9.8.1.11 PACSS_DCHAN_CAP_CFG0

Description: Capacitor Configuration 0 register
Address: 0x40300028
Offset: 0x28
Retention: Retained
IsDeepSleep: No
Comment: CR4-7
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	FCAP1 [6:0]						

Bits	15	14	13	12	11	10	9	8
Name	FCAP2 [15:12]				None [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	FCAP3 [23:20]				None [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:31]	RESCAP [30:28]			None [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:6	FCAP1	RW	R	0	binary weighted first stage integrating capacitance
	FCAP1_min			0	Min Value = 100 fF
	FCAP1_max			127	Max Value = 12.8 pF
	FCAP1_100fF			1	FCAP1[0] set -> +100 fF
	FCAP1_200fF			2	FCAP1[1] set -> +200 fF
	FCAP1_400fF			4	FCAP1[2] set -> +400 fF
	FCAP1_800fF			8	FCAP1[3] set -> +800 fF
	FCAP1_1600fF			16	FCAP1[4] set -> +1600 fF
	FCAP1_3200fF			32	FCAP1[5] set -> +3200 fF
	FCAP1_6400fF			64	FCAP1[6] set -> +6400 fF
12:15	FCAP2	RW	R	0	The second state integrating capacitance
	FCAP2_50fF			0	50fF
	FCAP2_100fF			1	100fF
	FCAP2_150fF			2	150fF
	FCAP2_200fF			3	200fF
	FCAP2_250fF			4	250fF
	FCAP2_300fF			5	300fF
	FCAP2_350fF			6	350fF
	FCAP2_400fF			7	400fF
	FCAP2_450fF			8	450fF
	FCAP2_500fF			9	500fF
	FCAP2_550fF			10	550fF
	FCAP2_600fF			11	600fF
	FCAP2_650fF			12	650fF
	FCAP2_700fF			13	700fF
	FCAP2_750fF			14	750fF
	FCAP2_800fF			15	800fF
20:23	FCAP3	RW	R	0	The third stage integrating capacitance
	FCAP3_100fF			0	100fF
	FCAP3_200fF			1	200fF

Bits	Name	SW	HW	Default or Enum	Description
	FCAP3_300fF			2	300fF
	FCAP3_400fF			3	400fF
	FCAP3_500fF			4	500fF
	FCAP3_600fF			5	600fF
	FCAP3_700fF			6	700fF
	FCAP3_800fF			7	800fF
	FCAP3_900fF			8	900fF
	FCAP3_1000fF			9	1000fF
	FCAP3_1100fF			10	1100fF
	FCAP3_1200fF			11	1200fF
	FCAP3_1300fF			12	1300fF
	FCAP3_1400fF			13	1400fF
	FCAP3_1500fF			14	1500fF
	FCAP3_1600fF			15	1600fF
28:30	RESCAP	RW	R	0	Reserved. The resonator loop feature has been disabled in the design; programming these bits does not produce any change in the ADC outcome

9.8.1.12 PACSS_DCHAN_CAP_CFG1

Description: Capacitor Configuration 1 register
Address: 0x4030002C
Offset: 0x2C
Retention: Retained
IsDeepSleep: No
Comment: CR8-11
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		DACCAP [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		IPCAP1 [13:8]					

Bits	23	22	21	20	19	18	17	16
Name	None [23:23]	IPCAP2 [22:20]			None [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:27]					IPCAP3 [26:24]		

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	DACCAP	RW	R	0	Binary weighted first stage DAC capacitance
	DACCAP_min			0	Min Value = 96 fF
	DACCAP_max			63	Max Value = 6.4 pF
	DACCAP_96fF			1	DACCAP[0] set -> add 12*8= +96 fF
	DACCAP_192fF			2	DACCAP[1] set -> add 24*8= +192 fF
	DACCAP_400fF			4	DACCAP[2] set -> add 50*8= +400 fF
	DACCAP_800fF			8	DACCAP[3] set -> add 100*8= +800 fF
	DACCAP_1600fF			16	DACCAP[4] set -> add 200*8= +1600 fF
	DACCAP_3200fF			32	DACCAP[5] set -> add 400*8= +3200 fF
8:13	IPCAP1	RW	R	0	Binary weighted first stage input sampling capacitance
	IPCAP1_min			0	Min Value = 100 fF
	IPCAP1_max			63	Max Value = 6.4 pF
	IPCAP1_100fF			1	IPCAP1[0] set -> +100 fF
	IPCAP1_200fF			2	IPCAP1[1] set -> +200 fF
	IPCAP1_400fF			4	IPCAP1[2] set -> +400 fF
	IPCAP1_80fF			8	IPCAP1[3] set -> +800 fF
	IPCAP1_1600fF			16	IPCAP1[4] set -> +1600 fF
	IPCAP1_3200fF			32	IPCAP1[5] set -> +3200 fF
20:22	IPCAP2	RW	R	0	Binary weighted second stage input sampling capacitance
	IPCAP2_50fF			0	50fF
	IPCAP2_100fF			1	100fF
	IPCAP2_150fF			2	150fF
	IPCAP2_200fF			3	200fF
	IPCAP2_250fF			4	250fF
	IPCAP2_300fF			5	300fF
	IPCAP2_350fF			6	350fF
	IPCAP2_400fF			7	400fF
24:26	IPCAP3	RW	R	0	Binary weighted third stage input sampling capacitance

Bits	Name	SW	HW	Default or Enum	Description
	IPCAP3_50fF			0	50fF
	IPCAP3_100fF			1	100fF
	IPCAP3_150fF			2	150fF
	IPCAP3_200fF			3	200fF
	IPCAP3_250fF			4	250fF
	IPCAP3_300fF			5	300fF
	IPCAP3_350fF			6	350fF
	IPCAP3_400fF			7	400fF

9.8.1.13 PACSS_DCHAN_CAP_CFG2

Description: Capacitor Configuration 2 register
Address: 0x40300030
Offset: 0x30
Retention: Retained
IsDeepSleep: No
Comment: CR12,14,15,16
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			SUMCAPIN [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	SUMCAP2 [14:12]			None [11:11]	SUMCAP1 [10:8]		

Bits	23	22	21	20	19	18	17	16
Name	SUMCAPFB [23:20]				None [19:19]	SUMCAP3 [18:16]		

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	SUMCAPIN	RW	R	0	The summer capacitance that lies on the path where the input signal is summed (50fF to 1.6pF in 50f steps)
	SUMCAPIN_50fF			0	50fF
	SUMCAPIN_100fF			1	100fF
	SUMCAPIN_150fF			2	150fF
	SUMCAPIN_200fF			3	200fF
	SUMCAPIN_250fF			4	250fF
	SUMCAPIN_300fF			5	300fF
	SUMCAPIN_350fF			6	350fF
	SUMCAPIN_400fF			7	400fF
	SUMCAPIN_450fF			8	450fF
	SUMCAPIN_500fF			9	500fF
	SUMCAPIN_550fF			10	550fF
	SUMCAPIN_600fF			11	600fF
	SUMCAPIN_650fF			12	650fF
	SUMCAPIN_700fF			13	700fF
	SUMCAPIN_750fF			14	750fF
	SUMCAPIN_800fF			15	800fF
	SUMCAPIN_850fF			16	850fF
	SUMCAPIN_900fF			17	900fF
	SUMCAPIN_950fF			18	950fF
	SUMCAPIN_1000fF			19	1000fF
	SUMCAPIN_1050fF			20	1050fF
	SUMCAPIN_1100fF			21	1100fF
	SUMCAPIN_1150fF			22	1150fF
	SUMCAPIN_1200fF			23	1200fF
	SUMCAPIN_1250fF			24	1250fF
	SUMCAPIN_1300fF			25	1300fF
	SUMCAPIN_1350fF			26	1350fF

Bits	Name	SW	HW	Default or Enum	Description
	SUMCAPIN_1400fF			27	1400fF
	SUMCAPIN_1450fF			28	1450fF
	SUMCAPIN_1500fF			29	1500fF
	SUMCAPIN_1550fF			30	1550fF
	SUMCAPIN_1600fF			31	1600fF
8:10	SUMCAP1	RW	R	0	The summer capacitance that lies on the feed-forward path from the first integrator output (0fF to 350f, 50fF steps)
	SUMCAP1_50fF			0	50fF
	SUMCAP1_100fF			1	100fF
	SUMCAP1_150fF			2	150fF
	SUMCAP1_200fF			3	200fF
	SUMCAP1_250fF			4	250fF
	SUMCAP1_300fF			5	300fF
	SUMCAP1_350fF			6	350fF
	SUMCAP1_400fF			7	400fF
12:14	SUMCAP2	RW	R	0	The summer capacitance that lies on the feed-forward path from the second integrator output (0fF to 350 in 50fF steps)
	SUMCAP2_50fF			0	50fF
	SUMCAP2_100fF			1	100fF
	SUMCAP2_150fF			2	150fF
	SUMCAP2_200fF			3	200fF
	SUMCAP2_250fF			4	250fF
	SUMCAP2_300fF			5	300fF
	SUMCAP2_350fF			6	350fF
	SUMCAP2_400fF			7	400fF
16:18	SUMCAP3	RW	R	0	The summer capacitance that lies on the feed-forward path from the third integrator output (0fF to 350fF in 50fF step)
	SUMCAP3_50fF			0	50fF
	SUMCAP3_100fF			1	100fF
	SUMCAP3_150fF			2	150fF
	SUMCAP3_200fF			3	200fF
	SUMCAP3_250fF			4	250fF
	SUMCAP3_300fF			5	300fF
	SUMCAP3_350fF			6	350fF
	SUMCAP3_400fF			7	400fF
20:23	SUMCAPFB	RW	R	0	The summer feedback capacitance
	SUMCAPFB_50fF			0	50fF
	SUMCAPFB_100fF			1	100fF
	SUMCAPFB_150fF			2	150fF
	SUMCAPFB_200fF			3	200fF
	SUMCAPFB_250fF			4	250fF
	SUMCAPFB_300fF			5	300fF
	SUMCAPFB_350fF			6	350fF
	SUMCAPFB_400fF			7	400fF
	SUMCAPFB_450fF			8	450fF
	SUMCAPFB_500fF			9	500fF
	SUMCAPFB_550fF			10	550fF
	SUMCAPFB_600fF			11	600fF
	SUMCAPFB_650fF			12	650fF
	SUMCAPFB_700fF			13	700fF

Bits	Name	SW	HW	Default or Enum	Description
	SUMCAPFB_750fF			14	750fF
	SUMCAPFB_800fF			15	800fF

9.8.1.14 PACSS_DCHAN_ACC_THRESH

Description: Accumulated Data Threshold
Address: 0x40300034
Offset: 0x34
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x7FFFFFFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ACC_THRESH [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ACC_THRESH [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ACC_THRESH [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ACC_THRESH [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ACC_THRESH	RW	R	2147483647	Accumulated Threshold Once the ACC_RESULT register surpasses the threshold value written to this register the ACC_RESULT the ACC_THRESH_INTR is set. This value is signed and follows the two's-complement notation. If ACC_THRESH is set to a positive value, the ACC_RESULT must surpass the positive value of the ACC_THRESH to set the ACC_THRESH_INTR. If ACC_THRESH is set to a negative value, the ACC_RESULT must surpass the negative value (a greater magnitude) of the ACC_THRESH to set the ACC_THRESH_INTR.

9.8.1.15 PACSS_DCHAN_RESULT

Description: Channel result data register, updated at the end of each completed conversion
Address: 0x40300040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	RESULT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	RESULT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	RESULT	R	RW	0	Channel Result Data Register (signed) This is a two's complement value that is updated at the end of each completed conversion

9.8.1.16 PACSS_DCHAN_RESULT_TAG

Description: Tag register associated and updated simultaneously with the RESULT register
Address: 0x40300044
Offset: 0x44
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	RESULT_PARITY [6:0]						

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		SMP_COUNT [13:8]					

Bits	23	22	21	20	19	18	17	16
Name	DATA_TYPE [23:20]				None [19:18]		DCH_ID [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:27]					DATA_TYPE [26:24]		

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:6	RESULT_PARITY	R	W	0	Result Parity (ECC Parity) This 7-bit ECC parity is generated from the 32-bit result data and is updated simultaneously with the result data.
8:13	SMP_COUNT	R	W	0	Sample Count This field can be used as a sequence ID, this field increments for every valid sample For example if moving average is enabled and set to 4. SMP_COUNT will equal one on the fourth sample, which will be the first data valid (interrupt). If moving average is disabled, the first sample will be valid. This value is set simultaneously with the result data. The count value is reset with PACSS_MMIO.PACSS_CTL.ENABLE=0 or DCHAN.DCHAN_CTL.ENABLE=0.
16:17	DCH_ID	R	W	0	Digital Channel ID This field is a constant value of the digital channel(DCHAN) number this register is read from. The DCH_ID will be set immediately, before any sample completes.
20:26	DATA_TYPE	R	W	0	Result Data Type Represents the value of PACSS.DCHAN[]_SMP_CTL.POS_PIN_SEL.DATA_TYPE used during the conversion. Note that the DATA_TYPE is latched at the start of the conversion to ensure a constant input selection during the conversion, but is updated here at the end of conversion simultaneously with the RESULT register and the other RESULT_TAG fields.

9.8.1.17 PACSS_DCHAN_ACC_RESULT

Description: Channel Accumulated result data register
Address: 0x40300048
Offset: 0x48
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ACC_RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ACC_RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ACC_RESULT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ACC_RESULT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ACC_RESULT	RW0C	RW	0	Accumulator Output result register. Write '0s' to clear. This register will only be updated if the post processor is enabled. This register must be manually cleared, it is not cleared after ACC_THRESH_INTR.

9.8.1.18 PACSS_DCHAN_INTR

Description: Interrupt request register
Address: 0x40300050
Offset: 0x50
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RANGE _INTR [7:7]	ACC _THRESH _INTR [6:6]	SATURATE _INTR [5:5]	OVERLOAD _INTR [4:4]	HWT _COLLI SION_INTR [3:3]	FWT _COLLI SION_INTR [2:2]	OVERFLOW _INTR [1:1]	DATA_VAL _INTR [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	DATA_VAL_INTR	RW1C	RW1S	0	Data Valid Interrupt 0: hardware sets this interrupt after completing a scan of all the enabled channels. Write with '1' to clear bit.
1	OVERFLOW_INTR	RW1C	RW1S	0	Overflow Interrupt: hardware sets this interrupt when it sets a new DATA_VAL_INTR while that bit was not yet cleared by the firmware. Write with '1' to clear bit.
2	FWT_COLLISION_INTR	RW1C	RW1S	0	Firmware Trigger Collision Interrupt 0: hardware sets this interrupt when FW_TRIGGER is asserted while the DSM is BUSY. Raising this interrupt is delayed to when the scan caused by the FW_TRIGGER has been completed, i.e. not when the preceding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit.
3	HWT_COLLISION_INTR	RW1C	RW1S	0	Hardware Trigger Collision Interrupt 0: hardware sets this interrupt when the HW trigger signal is asserted while the DSM is BUSY. Raising this interrupt is delayed to when the scan caused by the HW trigger has been completed, i.e. not when the preceding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit.
4	OVERLOAD_INTR	RW1C	RW1S	0	Overload Interrupt: hardware sets this interrupt for each channel if the modulator output is all zeros or all ones. This is an indication that the modulator is overloaded. Write with '1' to clear bit.
5	SATURATE_INTR	RW1C	RW1S	0	Saturate Interrupt: hardware sets this interrupt if a conversion result is prevented from overflowing in either the decimator or the post processor when PP_CTL.SAT_EN=1. Write with '1' to clear bit.

Bits	Name	SW	HW	Default or Enum	Description
6	ACC_THRESH_INTR	RW1C	RW1S	0	Accumulated Threshold Interrupt: hardware sets this interrupt when the accumulated threshold value has been surpassed.
7	RANGE_INTR	RW1C	RW1S	0	Range detect Interrupt: hardware sets this interrupt if the conversion result of that channel met the condition specified by the RANGE_LOW and RANGE_HIGH registers. Write with '1' to clear bit.

9.8.1.19 PACSS_DCHAN_INTR_SET

Description: Interrupt set request register
Address: 0x40300054
Offset: 0x54
Retention: Not Retained
IsDeepSleep: No
Comment: Not really a register, intended for verification/debug. When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RANGE_SET [7:7]	ACC_THRESH_SET [6:6]	SATURATE_SET [5:5]	OVERLOAD_SET [4:4]	HWT_COLLISION_SET [3:3]	FWT_COLLISION_SET [2:2]	OVERFLOW_SET [1:1]	DATA_VAL_SET [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	DATA_VAL_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
1	OVERFLOW_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
2	FWT_COLLISION_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
3	HWT_COLLISION_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
4	OVERLOAD_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
5	SATURATE_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
6	ACC_THRESH_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
7	RANGE_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.

9.8.1.20 PACSS_DCHAN_INTR_MASK

Description: Interrupt mask register
Address: 0x40300058
Offset: 0x58
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RANGE_MASK [7:7]	ACC_THRESH_MASK [6:6]	SATURATE_MASK [5:5]	OVERLOAD_MASK [4:4]	HWT_COLLISION_MASK [3:3]	FWT_COLLISION_MASK [2:2]	OVERFLOW_MASK [1:1]	DATA_VAL_MASK [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	DATA_VAL_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
1	OVERFLOW_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
2	FWT_COLLISION_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
3	HWT_COLLISION_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
4	OVERLOAD_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
5	SATURATE_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
6	ACC_THRESH_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
7	RANGE_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.

9.8.1.21 PACSS_DCHAN_INTR_MASKED

Description: Interrupt masked request register
Address: 0x4030005C
Offset: 0x5C
Retention: Not Retained
IsDeepSleep: No
Comment: If the value is not zero then the DSM interrupt signal to the NVIC is high. When read, this register reflects a bitwise AND between the interrupt request and mask registers.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RANGE_MASKED [7:7]	ACC_THRESH_MASKED [6:6]	SATURATE_MASKED [5:5]	OVERLOAD_MASKED [4:4]	HWT_COLLISION_MASKED [3:3]	FWT_COLLISION_MASKED [2:2]	OVERFLOW_MASKED [1:1]	DATA_VAL_MASKED [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	DATA_VAL_MASKED	R	W	0	Logical and of corresponding request and mask bits.
1	OVERFLOW_MASKED	R	W	0	Logical and of corresponding request and mask bits.
2	FWT_COLLISION_MASKED	R	W	0	Logical and of corresponding request and mask bits.
3	HWT_COLLISION_MASKED	R	W	0	Logical and of corresponding request and mask bits.
4	OVERLOAD_MASKED	R	W	0	Logical and of corresponding request and mask bits.
5	SATURATE_MASKED	R	W	0	Logical and of corresponding request and mask bits.
6	ACC_THRESH_MASKED	R	W	0	Logical and of corresponding request and mask bits.
7	RANGE_MASKED	R	W	0	Logical and of corresponding request and mask bits.

9.8.1.22 PACSS_DCHAN_STATUS

Description: Status registesr
Address: 0x40300060
Offset: 0x60
Retention: Not Retained
IsDeepSleep: No
Comment: Channel Status
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							OVERLOAD_CAUSE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	OVERLOAD_CAUSE	R	W	0	To be read after OVERLOAD_INTR issues. If read returns 0, overload is due to all 0s. If read returns 1, overload is due to all 1s

9.8.1.23 FCFG

9.8.1.23.1 PACSS_DCHAN_FCFG_COEF

Description: Coefficient Value
Address: 0x40300100
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	COEF [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	COEF [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	COEF	RW	R	Undefined	FIR Coefficient Value The coefficient values can range from -1+1/(2^15) to 1-1/(2^15) with a resolution of 1/(2^15). The coefficient uses twos-complement notation and the decimal point is fixed to the right of the most significant bit. Examples: -0.25 = 0xE000 and 0.25 = 0x2000 Note: The Coefficient values are stored in SRAM, not registers. They are not initialized during a reset. They also cannot be accessed during a conversion.

9.8.1.23.2 PACSS_DCHAN_FCFG_TAP

Description: Tap Value
Address: 0x40300108
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	TAP [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	TAP [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	TAP [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	TAP [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	TAP	RW	RW	Undefined	Tap value, Witten by hardware readable by software. Note: The TAP values are stored in SRAM, not registers. They are not initialized during a reset. They also cannot be accessed during a conversion.

9.8.2 ACHAN

9.8.2.1 PACSS_ACHAN_ACHAN_CTL

Description: Analog Channel Control
Address: 0x40340000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				REF_EN [3:3]	BUF_EN [2:2]	PGA_EN [1:1]	MOD_EN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:11]					VCM_BUF_EN [10:10]	VDDA_RES_EN [9:9]	VCCA_RES_EN [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						AAF_CUTOFF_FREQ [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	ENABLE [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	MOD_EN	RW	R	0	Modulator Enable (also enables INMUX)
1	PGA_EN	RW	R	0	Programmable Gain Amplifier Enable (also enables VNEG Pump)
2	BUF_EN	RW	R	0	Buffer Enable Enables the buffer, when disabled all buffer controls from BUF_CTL are disabled.
3	REF_EN	RW	R	0	Reference Enable It enables the *_SEL controls in the REF_CTL registers, which allows switch closure for the reference selection.
8	VCCA_RES_EN	RW	R	0	VCCA Resistor Reference Enable This is one of the options for the VCM voltage. The default is 0.8V from HPBGR. This is added for risk-mitigation.
9	VDDA_RES_EN	RW	R	0	VDDA Resistor Reference Enable This is one of the reference options for the modulator. It is meant to be used for diagnostics.
10	VCM_BUF_EN	RW	R	0	VCM Buffer Enable VCM_BUF is the buffer that provides the common mode for the differential amplifiers in the modulator. It also provides input common mode to the sampling capacitor of the integrators.

Bits	Name	SW	HW	Default or Enum	Description
16:17	AAF_CUTOFF_FREQ	RW	R	0	Anti-Aliasing Filter Cut-off Frequency 00 - 30 kHz 01 - 10 kHz (sets aaf_f10k) 10 - 20 kHz (sets aaf_f20k) 11 - Reserved
31	ENABLE	RW	R	0	Analog Channel Enable

9.8.2.2 PACSS_ACHAN_TR_CTL

Description: Trigger Control for Sequencer
Address: 0x40340004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x44

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PEND_SEC_TR_EN [7:7]	SYNC_SEC_TR [6:6]	PEND_SEC_TR_SEL [5:4]		PRIM_TR_EN [3:3]	SYNC_PRIM_TR [2:2]	PRIM_TR_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	PRIM_TR_SEL	RW	R	0	Select for Primary Trigger. Triggers starts conversion on all primary digital channels linked to this analog channel. 0 - select HW tr_start[0] 1 - select HW tr_start[1] 2 - select HW tr_start[2] 3 - select HW tr_start[3] Only applicable to HW triggers
2	SYNC_PRIM_TR	RW	R	1	Synchronize Primary Trigger 0 - bypass clock domain synchronization of the trigger signal. 1 - synchronize the trigger signal to the DSM clock domain, if needed an edge detect is done in the peripheral clock domain. Only applicable to HW triggers
3	PRIM_TR_EN	RW	R	0	Primary Trigger Enable (enables HW triggers) if disabled, conversion can still be started via user SW
4:5	PEND_SEC_TR_SEL	RW	R	0	Select for Trigger that pends secondary digital channels linked to this analog channel to convert on the next primary trigger. 0 - select HW tr_start[0] 1 - select HW tr_start[1] 2 - select HW tr_start[2] 3 - select HW tr_start[3] Only applicable to HW triggers

Bits	Name	SW	HW	Default or Enum	Description
6	SYNC_SEC_TR	RW	R	1	Synchronize Secondary Trigger 0 - bypass clock domain synchronization of the trigger signal. 1 - synchronize the trigger signal to the DSM clock domain, if needed an edge detect is done in the peripheral clock domain. Only applicable to HW triggers
7	PEND_SEC_TR_EN	RW	R	0	Secondary Trigger Enable (enables HW triggers) if disabled, conversion can still be pended via user SW

9.8.2.3 PACSS_ACHAN_CHOP_CTL

Description: Chopping Control for Sequencer
Address: 0x40340008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x60000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				SMP_CNT [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	AAF_SHORT_R_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	DEC_BLANK_CNT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	CHOP_RST_EN [31:31]	CIRCUIT_2ND_EN [30:30]	CIRCUIT_CHOP [29:28]		None [27:26]		CHOP_MODE [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	SMP_CNT	RW	R	0	Chopping Sample Count Number of samples to count before toggling modbit. (SMP_CNT+1). The samples counted rely only on the DR value set in DEC_CTL or SEQ_CTL. Depending on which one the Decimator is using.
8:15	AAF_SHORT_R_CNT	RW	R	0	Anti-Aliasing Filter Short Resistor Count Number of DSM clock cycles (AAF_SHORT_CNT) to short the AAF resistor after a toggle of the modbit.
16:23	DEC_BLANK_CNT	RW	R	0	Decimator Blanking Count Number of DSM clock cycles (DEC_BLANK_CNT) where the decimator will be disconnected from the modulator output stream, and connected to a circular FIFO of the last 32 data values after the modbit toggles
24:25	CHOP_MODE	RW	R	0	Chopping Mode 00 - OFF: Buffer Cross Chopping Disabled 01 - Not supported 11 - Buffer Cross Chopping Enabled 10 - Not supported Buffer cross chopping is on the input and output of the buffer using the modbit. This mode toggles the modbit when the SMP_CNT value is reached. Buffer cross chopping is only functional in the configurations where ACHAN0 is only mapped to DCHAN0, or ACHAN1 (if present) is only mapped to DCHAN1 (if present).

Bits	Name	SW	HW	Default or Enum	Description
28:29	CIRCUIT_CHOP	RW	R	2	Circuit Chopping 0 - Off 1 - Disconnect AAF (SW1) for 1 DSM clock cycle after fchop clock edge 2 - Disconnect AAF (SW1) for 2 DSM clock cycle after fchop clock edge 3 - Disconnect AAF (SW1) for 4 DSM clock cycle after fchop clock edge Circuit chopping differs from the other fields in this register, it has no interaction with the modbit. When enabled it disconnects the AAF for the set number of clock cycles after a fchop clock edge.
30	CIRCUIT_2ND_EN	RW	R	1	2nd Stage Circuit Chopping Enable Enables Circuit Chopping on the 2nd integrator in the modulator
31	CHOP_RST_EN	RW	R	0	Reserved (no functionality)

9.8.2.4 PACSS_ACHAN_PGA_CTL

Description: Programmable Gain Amplifier Control
Address: 0x4034000C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x133

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		PGA_IDAC_EN [5:5]	PGA_CHOP_EN [4:4]	None [3:2]		PGA_PWR_LEVELS [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:11]					PGA_BW_BOOST_EN [10:10]	PGA_DYN_DIODE_BIAS [9:9]	PGA_OVERLAP_EN [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	PGA_PWR_LEVELS	RW	R	3	PGA Power Levels 00 - 39 percent Power Mode 01 - 58 percent Power Mode 10 - 78 percent Power Mode 11 - 100 percent Power Mode
4	PGA_CHOP_EN	RW	R	1	Chopping Enable
5	PGA_IDAC_EN	RW	R	1	IDAC Enable
8	PGA_OVERLAP_EN	RW	R	1	PGA Overlap Enable Enable overlapping for the PGA chopping clocks. When disabled, PGA chopping clocks are non-overlapping
9	PGA_DYN_DIODE_BIAS	RW	R	0	TBD - Currently not used
10	PGA_BW_BOOST_EN	RW	R	0	TBD - Currently not used

9.8.2.5 PACSS_ACHAN_MOD_CTL

Description: Modulator Control
Address: 0x40340010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: CR12,14,15,16
Default: 0xC003236

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	POWER2_3 [6:4]			None [3:3]	POWER1 [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	POWER_SUM [14:12]			None [11:10]		POWER_COMP [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:28]				MOD_CHOP_EN [27:27]	MOD_FCHOP [26:24]		

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	POWER1	RW	R	6	First stage Opamp power level control
	POWER1_44uA			0	10 percent Power Mode
	POWER1_135uA			1	31 percent Power Mode
	POWER1_190uA			2	44 percent Power Mode
	POWER1_271uA			3	63 percent Power Mode
	POWER1_325uA			4	75 percent Power Mode
	POWER1_380uA			5	88 percent Power Mode
	POWER1_433uA			6	100 percent Power Mode
	POWER1_652uA			7	150 percent Power Mode
4:6	POWER2_3	RW	R	3	The power control for the second and third integrator stages
	POWER2_3_97uA			0	75 percent Power Mode
	POWER2_3_106uA			1	81 percent Power Mode
	POWER2_3_122uA			2	94 percent Power Mode
	POWER2_3_130uA			3	100 percent Power Mode
	POWER2_3_193uA			4	150 percent Power Mode
	POWER2_3_130uA_2			5	100 percent Power Mode
	POWER2_3_130uA_3			6	100 percent Power Mode
	POWER2_3_130uA_4			7	100 percent Power Mode
8:9	POWER_COMP	RW	R	2	The power control for the quantizer block
	POWER_COMP_50			0	50 percent Power Mode
	POWER_COMP_75			1	75 percent Power Mode
	POWER_COMP_100			2	100 percent Power Mode
	POWER_COMP_200			3	200 percent Power Mode
12:14	POWER_SUM	RW	R	3	The power control for the summer block
	POWER_SUM_53uA			0	75 percent Power Mode
	POWER_SUM_58uA			1	81 percent Power Mode
	POWER_SUM_67uA			2	94 percent Power Mode

Bits	Name	SW	HW	Default or Enum	Description
	POWER_SUM_71uA			3	100 percent Power Mode
	POWER_SUM_105uA			4	150 percent Power Mode
	POWER_SUM_71uA_2			5	N/A
	POWER_SUM_71uA_3			6	N/A
	POWER_SUM_71uA_4			7	N/A
24:26	MOD_FCHOP	RW	R	4	Modulator Chopping Clock Frequency Selection
	FCLOCKDIV2			0	chopping frequency is Fclock/2
	FCLOCKDIV4			1	chopping frequency is Fclock/4
	FCLOCKDIV8			2	chopping frequency is Fclock/8
	FCLOCKDIV16			3	chopping frequency is Fclock/16
	FCLOCKDIV32			4	chopping frequency is Fclock/32
	FCLOCKDIV64			5	chopping frequency is Fclock/64
	FCLOCKDIV128			6	chopping frequency is Fclock/128
	FCLOCKDIV256			7	chopping frequency is Fclock/256
27	MOD_CHOP_EN	RW	R	1	Modulator Chopping Enable

9.8.2.6 PACSS_ACHAN_DPATH_CTL

Description: Datapath Control
Address: 0x40340014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xC0002

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				NONOV [3:2]		QLEV [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	MX_DIN [14:14]	OD_EN [13:13]	ODET_TH [12:8]				

Bits	23	22	21	20	19	18	17	16
Name	None [23:23]	RESET3 _EN [22:22]	RESET2 _EN [21:21]	RESET1 _EN [20:20]	BUF_PGA _CHOP _CLK_EN [19:19]	BUF_PGA_FCHOP [18:16]		

Bits	31	30	29	28	27	26	25	24
Name	None [31:29]			FCLOCK _EN [28:28]	None [27:26]		MX_DOUT [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	QLEV	RW	R	2	Quantization Level of Modulator 2'h0: 2 level quantization 2'h1: 3 level quantization 2'h2: 9 level quantization 2'h3: Reserved
2:3	NONOV	RW	R	0	Non-Overlap delay of clock phases 2'h0: low (1.57ns, typ) 2'h1: medium (2.54ns, typ) 2'h2: high (6.47ns, typ) 2'h3: very high (9.91ns, typ) Default is low, other settings are for risk mitigation
8:12	ODET_TH	RW	R	0	Overload detection threshold. If the number of continuous 1s or 0s coming out of quantizer exceeds this number, the overload detection flag is set
13	OD_EN	RW	R	0	Overload Detect Enable
14	MX_DIN	RW	R	0	Select the data source of the Decimator input : 0: modulator data is selected as input to decimator 1: dbg_io[3:0] is selected as the input to the decimator. In this mode dbg_io[5:4] are outputs. dbg_io[5:4]={modrst, clk_dsm_ana} Previously named DPMODE
16:18	BUF_PGA_FCHOP	RW	R	4	Chopping Clock Frequency selection for Buffer and PGA
	FCLOCKDIV2			0	Fclock/2
	FCLOCKDIV4			1	Fclock/4

Bits	Name	SW	HW	Default or Enum	Description
	FCLOCKDIV8			2	Fclock/8
	FCLOCKDIV16			3	Fclock/16
	FCLOCKDIV32			4	Fclock/32
	FCLOCKDIV64			5	Fclock/64
	FCLOCKDIV128			6	Fclock/128
	FCLOCKDIV256			7	Fclock/256
19	BUF_PGA_CHOP_CLK_EN	RW	R	1	Buffer and PGA Chopping Clock enable for Buffer and PGA This bit should be set to 1 by SW in the default use case.
20	RESET1_EN	RW	R	0	Allow first stage integrating capacitance to be reset. If enabled this reset is triggered by an overload detection
21	RESET2_EN	RW	R	0	Allow second stage integrating capacitance to be reset. If enabled this reset is triggered by an overload detection
22	RESET3_EN	RW	R	0	Allow third stage integrating capacitance to be reset. If enabled this reset is triggered by an overload detection
24:25	MX_DOUT	RW	R	0	Select the DSM data routed to the dbg_io output: 2'h0: none 2'h1: dbg_io[5:0] = {modrst, clk_dsm_ana, dout2scomp[3:0]} 2'h2: dbg_io[5:0] = {ovdcause, ovdflag, agc_gain_lvl[3:0]} 2'h3: dbg_io[5:0] = {modrst, clk_dsm_ana, agc_gain_lvl[3:0]}
28	FCLOCK_EN	RW	R	0	Modulator Clock Enable (FCLOCK) By default the modulator clock only runs when converting a sample. Setting FCLOCK_CLK_EN=1 makes FCLOCK free running.

9.8.2.7 PACSS_ACHAN_BUF_CTL

Description: Buffer Control
Address: 0x40340018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x33

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		BUF_IDAC_EN [5:5]	BUF_CHOP_EN [4:4]	None [3:2]		BUF_PWR_LEVELS [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	BUF_PWR_LEVELS	RW	R	3	Buffer Power Levels 00 - 32 percent Power Mode 01 - 55 percent Power Mode 10 - 78 percent Power Mode 11 - 100 percent Power Mode
4	BUF_CHOP_EN	RW	R	1	Buffer chopping enable
5	BUF_IDAC_EN	RW	R	1	Buffer IDAC enable

9.8.2.8 PACSS_ACHAN_PUMP_CTL

Description: Pump Control
Address: 0x40340020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		CLOCK_SEL [5:4]		None [3:2]		VNEG_PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	VNEG_PWR_MODE	RW	R	0	Negative pump power mode. Trim for risk mitigation, not intended for customer use.
4:5	CLOCK_SEL	RW	R	0	Negative Pump Clock selection The negative pump requires a 24 MHz clock For bit decode use the following: 00: pump clock sourced by clk_pump/2, use if clk_pump is set to 48MHz 01: pump clock sourced by clk_pump/1, use if clk_pump is set to 24 MHz 10: pump clock sourced by clk_hf/2, use if clk_hf is set to 48 MHz 11: pump clock sourced by clk_hf/1, use if clk_hf is set to 24 MHz

9.8.2.9 PACSS_ACHAN_REF_CTL

Description: Reference Control
Address: 0x40340024
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xA

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	VREF_QTZ_SEL [6:6]	VCM_SEL [5:4]		VCM_PWR [3:2]		VREF_PWR [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	VREF_PWR	RW	R	2	Power control for the voltage reference buffer for the sigma delta ADC
	VREF_26uA			0	VREF Buffer is operating in Low Power (26 uA) mode
	VREF_32uA			1	VREF Buffer is operating in Medium Power (32 uA) mode
	VREF_118uA			2	VREF Buffer is operating in High Power (118 uA) mode
	VREF_232uA			3	VREF Buffer is operating in Turbo Power (232 uA) mode
2:3	VCM_PWR	RW	R	2	Power Control for the Voltage Common Mode Buffer for the Sigma Delta ADC
	VCM_18uA			0	VCM Buffer is operating in Low Power (18 uA) mode
	VCM_28uA			1	VCM Buffer is operating in Medium Power (28 uA) mode
	VCM_55uA			2	VCM Buffer is operating in High Power (55 uA) mode
	VCM_114uA			3	VCM Buffer is operating in Turbo Power (114 uA) mode
4:5	VCM_SEL	RW	R	0	VCM selection 0 - VREF 0.8V 1 - VREF 0.7V 2 - VCCA/2 3 - Reserved
6	VREF_QTZ_SEL	RW	R	0	VREF_QTZ selection 0 - VREFH CDAC 1 - VCCA_KELVIN

9.8.2.10 PACSS_ACHAN_START

Description: Start Conversion
Address: 0x40340028
Offset: 0x28
Retention: Not Retained
IsDeepSleep: No
Comment: ACHAN!E20
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							START_PRIM [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							PEND_SEC [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	START_PRIM	RW1S	RW1C	0	Start Primary Conversion (FW Trigger) . A write of 1 to this bit starts a primary conversion. This bit is cleared once the conversion is started. A write of 1 while the sequencer is busy is ignored and the FWT_COLLISION interrupt is set for the digital channels assigned to this sequencer.
8	PEND_SEC	RW1S	RW1C	0	Pend Secondary Conversion (FW Trigger) A write of 1 to this bit pends a secondary conversion. This bit is cleared after the next primary conversion completes.

9.8.2.11 PACSS_ACHAN_INMUX_CTL

Description: INMUX Control
Address: 0x4034002C
Offset: 0x2C
Retention: Retained
IsDeepSleep: No
Comment: ACHAN!E21
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	POS_PIN_SEL [6:0]						

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			NEG_PIN_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
Name	None [23:17]							DECODE _EN [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:6	POS_PIN_SEL	RW	R	0	Positive Pin Select This register is only functional when the sequencer control of the INMUX is disabled. See SWITCH_SQ_CTL.INMUX. This register is the manual (non-sequencer) configuration of INMUX positive pin selection.
	POS_PIN_SEL_HVDIV0			0	0x00 - hvdiv0, High Voltage Divider 0 (If VSENS pin is a package pin, the divider is connected to this pin, otherwise the divider is built into the HV Regulator and connected to the VBAT pin)
	POS_PIN_SEL_HVDIV1			4	0x04 - hvdiv1, High Voltage Divider 1 (Not applicable if VDIAG pin is not a package pin, in which case these bits can be used as spare bits or ignored)
	POS_PIN_SEL_VTS			8	0x08 - vts, External (NTC) temperature
	POS_PIN_SEL_VTINT			12	0x0C - vtint, Internal Temp Sensor
	POS_PIN_SEL_VG0			16	0x10 - vg0, vssa
	POS_PIN_SEL_VG1			17	0x11 - vg1, vssd
	POS_PIN_SEL_VG2			18	0x12 - vg2, vssl
	POS_PIN_SEL_VG3			19	0x13 - vg3, vrefl
	POS_PIN_SEL_VG4			20	0x14 - vg4, unused (floating)
	POS_PIN_SEL_VG5			21	0x15 - vg5, vts_ret_k
	POS_PIN_SEL_VG6			22	0x16 - vg6, vtint_ret, internal temp sense
	POS_PIN_SEL_VG7			23	0x17 - vg7, vsub
	POS_PIN_SEL_VS0			24	0x18 - vs0, vccd2/2
	POS_PIN_SEL_VS1			25	0x19 - vs1, vcca_dsm/2
	POS_PIN_SEL_VS2			26	0x1A - vs2, vdda/4
	POS_PIN_SEL_VS3			27	0x1B - vs3, vddd/4
	POS_PIN_SEL_VR0			28	0x1C - vr0, 1.2V vrefh (hpbgr)
	POS_PIN_SEL_VR1			29	0x1D - vr1, 0.8V vref (hpbgr)
	POS_PIN_SEL_VR2			30	0x1E - vr2, 0.7V vref (hpbgr)
	POS_PIN_SEL_VR3			31	0x1F - vr3, 1.2V vref (srss)

Bits	Name	SW	HW	Default or Enum	Description
	POS_PIN_SEL_GPIO0			32	0x20 - gpio0
	POS_PIN_SEL_GPIO1			36	0x24 - gpio1
	POS_PIN_SEL_GPIO2			40	0x28 - gpio2
	POS_PIN_SEL_GPIO3			44	0x2C - gpio3
	POS_PIN_SEL_GPIO4			48	0x30 - gpio4
	POS_PIN_SEL_GPIO5			52	0x34 - gpio5
	POS_PIN_SEL_GPIO6			56	0x38 - gpio6
	POS_PIN_SEL_GPIO7			60	0x3C - gpio7
	POS_PIN_SEL_RSH0			64	0x40 - rsh0
	POS_PIN_SEL_RSH1			96	0x60 - rsh1
8:12	NEG_PIN_SEL	RW	R	0	Negative Pin Select This register is only functional when the sequencer control of the INMUX is disabled. See SWITCH_SQ_CTL.INMUX. This register is the manual (non-sequencer) configuration of INMUX negative pin selection.
	NEG_PIN_SEL_VSSA			0	0x00 - vssa
	NEG_PIN_SEL_VSSA_K0			8	0x08 - vssa_k0, unused (floating)
	NEG_PIN_SEL_VSSA_K1			9	0x09 - vssa_k1, vrefl
	NEG_PIN_SEL_VSSA_K2			10	0x0A - vssa_k2, srss_vss
	NEG_PIN_SEL_VSSA_K3			11	0x0B - vssa_k3, vdiv_ret
	NEG_PIN_SEL_VSSA_K4			12	0x0C - vssa_k4, vts_ret
	NEG_PIN_SEL_VSSA_K5			13	0x0D - vssa_k5, vtint_ret
	NEG_PIN_SEL_VSSA_K6			14	0x0E - vssa_k6, gpio0
	NEG_PIN_SEL_VSSA_K7			15	0x0F - vssa_k7, gpio2
	NEG_PIN_SEL_RSL0			16	0x10 - rsl0
	NEG_PIN_SEL_RSL1			24	0x18 - rsl1
16	DECODE_EN	RW	R	0	Enables Decode Logic to close switches. This must be set to '1' allow usage of POS_PIN_SEL and NEG_PIN_SEL. If set to '0' all switches in the INMUX will be open. This register is only applicable when SWITCH_SQ_CTL.INMUX=0

9.8.2.12 PACSS_ACHAN_DEM_CTL

Description: Dynamic Element Matching Control
Address: 0x40340030
Offset: 0x30
Retention: Retained
IsDeepSleep: No
Comment: ACHAN!E21
Default: 0x4

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					DEM_EN [2:2]	SCRAM1 _EN [1:1]	SCRAM0 _EN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	SCRAM0_EN	RW	R	0	Enable Scrambler 0 Also known as EN_ADWA
1	SCRAM1_EN	RW	R	0	Enable Scrambler 1 Also known as EN_BIDWA
2	DEM_EN	RW	R	1	Enable DEM Bi-directional Data Weighted Averaging (DWA) based Dynamic Element Matching (DEM) scheme for mismatch cancellation. Bi-directional DWA alters the direction of pointers used for rotation every cycle for avoiding repetition pattern of the DWA for low value DC inputs. DWA mode: SCRAM0_EN=0, SCRAM1_EN=0 Alternate DWA mode (not preferred): SCRAM0_EN=1, SCRAM1_EN=0 Bi-DWA mode: SCRAM0_EN=0, SCRAM1_EN=1 Not used: SCRAM0_EN=1, SCRAM1_EN=1

9.8.2.13 PACSS_ACHAN_SWITCH

Description: Firmware Switch Control
Address: 0x40340034
Offset: 0x34
Retention: Retained
IsDeepSleep: No
Comment: Firmware control for INMUX and AAF switches. This register is used to manually close switches via FW for debug and test purposes.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	AAF_SW4 [7:7]	AAF_SW3 [6:6]	AAF_SW2 [5:5]	AAF_SW1 [4:4]	INMUX_ABUSB_VMINUS [3:3]	INMUX_ABUSA_VMINUS [2:2]	INMUX_ABUSB_VPLUS [1:1]	INMUX_ABUSA_VPLUS [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	INMUX_ABUSA_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between VPLUS and AMUXBUSA output. Write with '1' to set bit. This switch can be closed while the sequencer is controls the INMUX pin selection
1	INMUX_ABUSB_VPLUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between VPLUS and AMUXBUSB. Write with '1' to set bit. This switch can be closed while the sequencer is controls the INMUX pin selection
2	INMUX_ABUSA_VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between VMINUS and AMUXBUSA output. Write with '1' to set bit. This switch can be closed while the sequencer is controls the INMUX pin selection
3	INMUX_ABUSB_VMINUS	RW1S	RW1C	0	Firmware control: 0=open, 1=close switch between VMINUS and AMUXBUSB. Write with '1' to set bit. This switch can be closed while the sequencer is controls the INMUX pin selection
4	AAF_SW1	RW1S	RW1C	0	Firmware control: 0=open, 1=close AAF switch 1. Write with '1' to set bit. This switch can only be closed via this register if SWITCH_SQ_CTL.AAF=0
5	AAF_SW2	RW1S	RW1C	0	Firmware control: 0=open, 1=close AAF switch 2. Write with '1' to set bit. This switch can only be closed via this register if SWITCH_SQ_CTL.AAF=0
6	AAF_SW3	RW1S	RW1C	0	Firmware control: 0=open, 1=close AAF switch 3. Write with '1' to set bit. This switch can only be closed via this register if SWITCH_SQ_CTL.AAF=0.
7	AAF_SW4	RW1S	RW1C	0	Firmware control: 0=open, 1=close AAF switch 4. Write with '1' to set bit. This switch can only be closed via this register if SWITCH_SQ_CTL.AAF=0

9.8.2.14 PACSS_ACHAN_SWITCH_CLEAR

Description: Firmware Switch Control Clear
Address: 0x40340038
Offset: 0x38
Retention: Not Retained
IsDeepSleep: No
Comment: Not really a register, when read gives value from the SWITCH register. Used to open switches that were closed via the SWITCH register. To use the AAF fields of this register set SWITCH_SQ_CTL.AAF=0
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	AAF_SW4 [7:7]	AAF_SW3 [6:6]	AAF_SW2 [5:5]	AAF_SW1 [4:4]	INMUX_ABUSB_VMINUS [3:3]	INMUX_ABUSA_VMINUS [2:2]	INMUX_ABUSB_VPLUS [1:1]	INMUX_ABUSA_VPLUS [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	INMUX_ABUSA_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in the SWITCH register
1	INMUX_ABUSB_VPLUS	RW1C	A	0	Write '1' to clear corresponding bit in the SWITCH register
2	INMUX_ABUSA_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in the SWITCH register
3	INMUX_ABUSB_VMINUS	RW1C	A	0	Write '1' to clear corresponding bit in the SWITCH register
4	AAF_SW1	RW1C	A	0	Write '1' to clear corresponding bit in the SWITCH register
5	AAF_SW2	RW1C	A	0	Write '1' to clear corresponding bit in the SWITCH register
6	AAF_SW3	RW1C	A	0	Write '1' to clear corresponding bit in the SWITCH register
7	AAF_SW4	RW1C	A	0	Write '1' to clear corresponding bit in the SWITCH register

9.8.2.15 PACSS_ACHAN_SWITCH_SQ_CTL

Description: Switch Sequencer Control
Address: 0x4034003C
Offset: 0x3C
Retention: Retained
IsDeepSleep: No
Comment: Enable Sequencer control for the INMUX and AAF switches. Defaults to sequencer control, set fields to 0 to use INMUX_CTL and SWITCH registers for debug and test purposes. This allows FW control of switches
Default: 0x11

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			AAF [4:4]	None [3:1]			INMUX [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	INMUX	RW	R	1	Allow sequencer control for the provided switches
4	AAF	RW	R	1	Allow sequencer control for the provided switches

9.8.2.16 PACSS_ACHAN_SWITCH_STATUS

Description: Switch Status
Address: 0x40340040
Offset: 0x40
Retention: Not Retained
IsDeepSleep: No
Comment: gives the current switch status including Firmware (SWITCH register) and sequencer controls
Default: 0x90

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	AAF_SW4 [7:7]	AAF_SW3 [6:6]	AAF_SW2 [5:5]	AAF_SW1 [4:4]	INMUX_ABUSB_VMINUS [3:3]	INMUX_ABUSA_VMINUS [2:2]	INMUX_ABUSB_VPLUS [1:1]	INMUX_ABUSA_VPLUS [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	INMUX_ABUSA_VPLUS	R	W	0	switch status of corresponding bit in the SWITCH register
1	INMUX_ABUSB_VPLUS	R	W	0	switch status of corresponding bit in the SWITCH register
2	INMUX_ABUSA_VMINUS	R	W	0	switch status of corresponding bit in the SWITCH register
3	INMUX_ABUSB_VMINUS	R	W	0	switch status of corresponding bit in the SWITCH register
4	AAF_SW1	R	W	1	switch status of corresponding bit in the SWITCH register
5	AAF_SW2	R	W	0	switch status of corresponding bit in the SWITCH register
6	AAF_SW3	R	W	0	switch status of corresponding bit in the SWITCH register
7	AAF_SW4	R	W	1	switch status of corresponding bit in the SWITCH register

9.8.2.17 PACSS_ACHAN_DFT_CTL

Description: DFT Control Register
Address: 0x40340044
Offset: 0x44
Retention: Not Retained
IsDeepSleep: No
Comment: ACHAN!E29
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	MUX_EN [7:7]	MUXB_SEL [6:4]			None [3:3]	MUXA_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		VNEG_PMP_TEST_EN [13:13]	PGA_TEST_EN [12:12]	None [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	SPARE_CTL [23:20]				CHOP_PHASE_CTL [19:19]	RS1_PULLDOWN [18:18]	RS0_PULLDOWN [17:17]	FRC_ANA_EN_LOW [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:25]							SPARE_CTL [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	MUXA_SEL	RW	R	0	DFT MUX Selection for AMUXBUSA
	VCCA_DSM_DFT_KELVIN			0	dft_out = vcca_dsm_dft_kelvin
	VCM			1	dft_out = vcm
	VREF_DAC			2	dft_out = vref_dac
	AAF_IN_P			3	dft_out = aaf_in_p
	IREF_4P8U			4	dft_out = iref_4p8u - current source of PGA top amp cascode device
	BUFFIN_VPLUS			5	dft_out = buffin_vplus
	BUFFIN_VMINUS			6	dft_out = buffin_vminus
	BUFOUT_VPLUS			7	dft_out = bufout_vplus
4:6	MUXB_SEL	RW	R	0	DFT MUX Selection for AMUXBUSB
	VCCA_DSM_DFT			0	dft_out = vcca_dsm_dft
	REFOUT			1	dft_out = refout
	VREF_QTZ			2	dft_out = vref_qtz
	AAF_IN_N			3	dft_out = aaf_in_n
	IREF_2P4U			4	dft_out = iref_2p4u - current source of buffer top amp cascode device
	BUFFIN_VMINUS			5	dft_out = buffin_vminus
	BUFFIN_VPLUS			6	dft_out = buffin_vplus
	BUFOUT_VMINUS			7	dft_out = bufout_vminus
7	MUX_EN	RW	R	0	DFT MUX Enable
12	PGA_TEST_EN	RW	R	0	PGA Test Mode
13	VNEG_PMP_TEST_EN	RW	R	0	Negative Pump Test Enable

Bits	Name	SW	HW	Default or Enum	Description
16	FRC_ANA_EN_LOW	RW	R	0	Force global analog enable low (enable_scanoff_hv) to test for any SA1 faults on the level-shifter enables.
17	RS0_PULLDOWN	RW	R	0	RS0 Pull-down. Enables pull down on RSH0/RSL0 input pair for offset calibration.
18	RS1_PULLDOWN	RW	R	0	RS1 Pull-down. Enables pull down on RSH1/RSL1 input pair for offset calibration.
19	CHOP_PHASE_CTL	RW	R	0	Circuit chopping phase control. Inverts circuit chopping phase
20:24	SPARE_CTL	RW	R	0	Spare MMIO Controls for analog

9.8.2.18 PACSS_ACHAN_DFT_STATUS

Description: DFT Status Register
Address: 0x40340048
Offset: 0x48
Retention: Not Retained
IsDeepSleep: No
Comment: ACHAN!E29
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							OBSVR_LS_OUT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	OBSVR_LS_OUT	R	W	0	Observation point of level-shifters output. Used for detection of SA1 faults on the level-shifter enables. The read back value of this register changes based on the configuration and trims of the ACHAN and PACSS_MMIO registers.

9.8.2.19 PACSS_ACHAN_TRIM_PGA0_CTL

Description: PGA Trim 0 (lock protected)
Address: 0x4034FF00
Offset: 0xFF00
Retention: Retained
IsDeepSleep: No
Comment: ACHAN!E29
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		OFST_P [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	OFST_P	RW	R	0	Offset Plus Trim

9.8.2.20 PACSS_ACHAN_TRIM_PGA1_CTL

Description: PGA Trim 1 (lock protected)
Address: 0x4034FF04
Offset: 0xFF04
Retention: Retained
IsDeepSleep: No
Comment: ACHAN!E29
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		OFST_SLOPE_P [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	OFST_SLOPE_P	RW	R	0	Offset Slope Plus Trim

9.8.2.21 PACSS_ACHAN_TRIM_PGA2_CTL

Description: PGA Trim 2 (lock protected)
Address: 0x4034FF08
Offset: 0xFF08
Retention: Retained
IsDeepSleep: No
Comment: ACHAN!E29
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		OFST_M [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	OFST_M	RW	R	0	Offset Minus Trim

9.8.2.22 PACSS_ACHAN_TRIM_PGA3_CTL

Description: PGA Trim 3 (lock protected)
Address: 0x4034FF0C
Offset: 0xFF0C
Retention: Retained
IsDeepSleep: No
Comment: ACHAN!E29
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		OFST_SLOPE_M [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	OFST_SLOPE_M	RW	R	0	Offset Slope Minus Trim

9.8.2.23 PACSS_ACHAN_TRIM_PGA4_CTL

Description: PGA Trim 4 (lock protected)
Address: 0x4034FF10
Offset: 0xFF10
Retention: Retained
IsDeepSleep: No
Comment: ACHAN!E29
Default: 0x4

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					CM [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	CM	RW	R	4	Common Mode (Output Range) Trim

9.8.2.24 PACSS_ACHAN_TRIM_BUF0_CTL

Description: Buffer Trim 0 (lock protected)
Address: 0x4034FF14
Offset: 0xFF14
Retention: Retained
IsDeepSleep: No
Comment: ACHAN!E29
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		OFST_P [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	OFST_P	RW	R	0	Offset Plus Trim

9.8.2.25 PACSS_ACHAN_TRIM_BUF1_CTL

Description: Buffer Trim 1 (lock protected)
Address: 0x4034FF18
Offset: 0xFF18
Retention: Retained
IsDeepSleep: No
Comment: ACHAN!E29
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		OFST_PTAT_P [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	OFST_PTAT_P	RW	R	0	Offset PTAT Plus Trim

9.8.2.26 PACSS_ACHAN_TRIM_BUF2_CTL

Description: Buffer Trim 2 (lock protected)
Address: 0x4034FF1C
Offset: 0xFF1C
Retention: Retained
IsDeepSleep: No
Comment: ACHAN!E29
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		OFST_M [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	OFST_M	RW	R	0	Offset Minus Trim

9.8.2.27 PACSS_ACHAN_TRIM_BUF3_CTL

Description: Buffer Trim 3 (lock protected)
Address: 0x4034FF20
Offset: 0xFF20
Retention: Retained
IsDeepSleep: No
Comment: ACHAN!E29
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		OFST_PTAT_M [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	OFST_PTAT_M	RW	R	0	Offset PTAT Minus Trim

9.8.3 MMIO

9.8.3.1 PACSS_MMIO_PACSS_CTL

Description: Precision Analog Channel Control
Address: 0x403F0000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		VPOS _PMP_EN [5:5]	HPBGR _EN [4:4]	AREF_EN [3:3]	TMPS_EN [2:2]	LDO_EN [1:1]	AGC_EN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						HVDIVG_MUX_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLE [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	AGC_EN	RW	R	0	Auto-Gain Correction Enable
1	LDO_EN	RW	R	0	Low Dropout Regulator Enable Enables modulator voltage supply
2	TMPS_EN	RW	R	0	Temperature Sensor Enable
3	AREF_EN	RW	R	0	AREF Enable
4	HPBGR_EN	RW	R	0	High Precision Bandgap Reference Enable
5	VPOS_PMP_EN	RW	R	0	Positive Pump Enable
8:9	HVDIVG_MUX_SEL	RW	R	0	High Voltage Divider Ground Reference Mux Select 0 - Select VSSA 1 - Select VSSA 2 - Select RSH[0] 3 - Select RSL[0] This field is not applicable if VDIAG pin is not a package pin, in which case the selection is forced to VSSA regardless of how this field is set.
31	ENABLE	RW	R	0	Global Enable

9.8.3.2 PACSS_MMIO_AGC_CTL0

Description: Auto-Gain Correction Control 0
Address: 0x403F0004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x7003010

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	LO_THRESH [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	HI_THRESH [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	MIN_LVL [23:20]				INIT_LVL [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:30]		FAST_DEC_SCLR [29:28]		MAX_LVL [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	LO_THRESH	RW	R	16	Low Threshold value Magnitude of lower threshold value. This is an absolute value comparison. If the fast decimator result is lower than this threshold value, the gain level will be incremented. Gain levels must be configured from lowest to highest gain. modulator output ranges from -4 to 4. The max value will be 4* (FAST_DR+1) Based on default values: 4*16 = 64, default is 25 percent (16=0x10) Ex: set to 0x20 to set to -32 (decimal) or 32 (decimal)
8:15	HI_THRESH	RW	R	48	High Threshold value Magnitude of high threshold value. This is an absolute value comparison. If the fast decimator result is higher than this threshold value, the gain level will be decremented. Gain levels must be configured from lowest to highest gain. modulator output ranges from -4 to 4. The max value will be 4* (FAST_DR+1) Based on default values: 4*16 = 64, default is 75 percent (48=0x30) Ex: set 0x64 to set to -100 (decimal) or 100 (decimal)
16:19	INIT_LVL	RW	R	0	Initial Gain level The gain level that the AGC is initialized to once a conversion starts. Acceptable values are 0 - 9.

Bits	Name	SW	HW	Default or Enum	Description
20:23	MIN_LVL	RW	R	0	Minimum Gain Level The minimum gain level the AGC is allowed to reach when decrementing. Acceptable values are 0 - 9, but MIN_LVL <= INIT_LVL <= MAX_LVL
24:27	MAX_LVL	RW	R	7	Maximum Gain level The maximum gain level that the AGC is allowed to reach when incrementing Acceptable values are 0 - 9, but MIN_LVL <= INIT_LVL <= MAX_LVL
28:29	FAST_DEC_SCLR	RW	R	0	Fast Decimator Scaler Used to apply digital gain to output of the AGC's fast decimator. Intended to be used when digital gain is applied to the system via moving sum. 0 : FAST_DEC_RESULT = RESULT 1 : FAST_DEC_RESULT = RESULT << 1 2 : FAST_DEC_RESULT = RESULT << 2 3 : FAST_DEC_RESULT = RESULT << 3

9.8.3.3 PACSS_MMIO_AGC_CTL1

Description: Auto-Gain Correction Control 1
Address: 0x403F0008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x700000F

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	AAF _BLANK _MODE [7:7]	None [6:5]		FAST_DR [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	AAF_BLANK_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	DEC_BLANK_CNT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	SCALER_BLANK_CNT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	FAST_DR	RW	R	15	Fast Decimator Decimation Ratio (FAST_DR+1) sets the decimation ratio for the AGC's Fast Decimator The fast decimator will run continuously with this FAST_DR value while the DCHAN0 decimator is running.
7	AAF_BLANK_MODE	RW	R	0	Anti-Aliasing Filter (AAF) Blanking Mode 0 - Short AAF resistor (close SW2) 1 - Bypass AAF (open SW1) Shorting the AAF reduces the settling time
8:15	AAF_BLANK_CNT	RW	R	0	AAF Blank Count Number of DSM clock cycles (AAF_BLANK_CNT) where the AAF will either be shorted or disconnected after a gain level change.
16:23	DEC_BLANK_CNT	RW	R	0	Decimator Blank Count Number of DSM clock cycles (DEC_BLANK_CNT) where the decimator will be disconnected from the modulator output stream, and connected to a circular FIFO of the last 32 data values after a gain level change.
24:31	SCALER_BLANK_CNT	RW	R	7	Scaler Blank Count Number of DSM clock cycles (SCALER_BLANKT_CNT) where the gain scaler of next gain level will be delayed after a gain level change. The scaler will use its previous value until this count value is reached.

9.8.3.4 PACSS_MMIO_AGC_CTL2

Description: Auto-Gain Correction Control 2
Address: 0x403F000C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							LO _THRESH _FLT _MODE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	LO_THRESH_CNT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	LO_THRESH_CNT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	LO_THRESH_FLT _MODE	RW	R	0	Low Threshold Filter Mode 0 - counter mode 1 - integrator mode
16:31	LO_THRESH_CNT	RW	R	0	Low Threshold Filter Counter LO_THRESH_CNT + 1, is the count value used for filtering the next gain level change.

9.8.3.5 PACSS_MMIO_AGC_CTL3

Description: Auto-Gain Correction Control 3
Address: 0x403F0010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							HI _THRESH _FLT _MODE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	HI_THRESH_CNT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	HI_THRESH_CNT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	HI_THRESH_FLT_MODE	RW	R	0	High Threshold Filter Mode 0 - counter mode 1 - integrator mode
16:31	HI_THRESH_CNT	RW	R	0	High Threshold Filter Counter HI_THRESH_CNT + 1, is the count value used for filtering the next gain level change.

9.8.3.6 PACSS_MMIO_TMPS_CTL

Description: Temperature Sensor Control
Address: 0x403F0020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	IREF_UNIT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	BIPOLAR_UNIT [15:12]				IREF_SEL [11:11]	None [10:9]		IREF_UNIT [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			BIPOLAR_UNIT [20:16]				

Bits	31	30	29	28	27	26	25	24
Name	VTEMP_RET_SEL [31:31]	VTEMP_SEL [30:30]	VTEMP_SUP_SEL [29:29]	AMUXB_SEL [28:28]	AMUXA_SEL [27:27]	None [26:26]	LOAD_MODE [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:8	IREF_UNIT	RW	R	0	Number of units, between 0 (all switches open) and 9 IREF current = 9.6uA * (# of bits set) Each bit set of IREF_UNIT adds a multiple of 9.6uA.
11	IREF_SEL	RW	R	0	Temperature Sensor Current Reference Select Select between SRSS and AREF current reference 0 - selects AREF as current reference source 1 - selects SRSS as current reference source
12:20	BIPOLAR_UNIT	RW	R	0	Number of bipolar transistors, between 0 (all switches open) and 9 Each bit set of BIPOLAR_UNIT, adds a BIPOLAR transistors Only applicable for PNP and NPN load modes
24:25	LOAD_MODE	RW	R	0	Temperature Sensor Load Mode 0 - PNP 1 - NPN 2 - Resistor (5KOhms) 3 - Reserved
27	AMUXA_SEL	RW	R	0	Select amuxbus_a as a current source for biasing BJTs or Resistor
28	AMUXB_SEL	RW	R	0	Select amuxbus_b to be connected to temp sensor vbe/vres output.
29	VTEMP_SUP_SEL	RW	R	0	Select external current source to bias the BJTs or Resistor.
30	VTEMP_SEL	RW	R	0	Connect VTEMP pin to vbe/vres output voltage.
31	VTEMP_RET_SEL	RW	R	0	Connect VTEMP_RET pin to the vssa_kelvin of the BJTs and resistor.

9.8.3.7 PACSS_MMIO_VPOS_PUMP_CTL

Description: Positive Pump Control
Address: 0x403F0024
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		CLOCK_SEL [5:4]		VPOS _BYPASS _EN [3:3]	VPOS_PWR_MODE [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	VPOS_PWR_MODE	RW	R	0	Positive Pump Power Mode 000 - High -100 percent - (Fs = 3 MHz) 010 - Medium - 65 percent - (Fs = 3 MHz) 011 - Medium Low - 60 percent - (Fs = 750 kHz) 110 - Low - 50 percent - (Fs = 200 kHz) Other settings are reserved configurations
3	VPOS_BYPASS_EN	RW	R	0	Reserved, bit not used. Pump automatically bypassed to vdda when disabled.
4:5	CLOCK_SEL	RW	R	0	Positive Pump Clock selection The positive pump requires a 24 MHz clock For bit decode use the following: 00: pump clock sourced by clk_pump/2, use if clk_pump is set to 48MHz 01: pump clock sourced by clk_pump/1, use if clk_pump is set to 24 MHz 10: pump clock sourced by clk_hf/2, use if clk_hf is set to 48 MHz 11: pump clock sourced by clk_hf/1, use if clk_hf is set to 24 MHz

9.8.3.8 PACSS_MMIO_START

Description: Start Conversion
Address: 0x403F0030
Offset: 0x30
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							START_PRIM [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							PEND_SEC [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	START_PRIM	RW1S	RW1C	0	Start Primary Conversion (FW Trigger) . A write of 1 to this bit starts a primary conversion on both sequencers simultaneously. This bit is cleared once the conversion is started. A write of 1 while the sequencer(s) is busy is ignored and the FWT_COLLISION interrupt is set for the digital channels assigned to sequencer(s) that are busy.
8	PEND_SEC	RW1S	RW1C	0	Pend Secondary Conversion (FW Trigger) A write of 1 to this bit pends a secondary conversion. This bit is cleared after the next primary conversion completes.

9.8.3.9 PACSS_MMIO_INTR

Description: System Interrupt request register
Address: 0x403F0040
Offset: 0x40
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							AGC_GLVL_CHG [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	AGC_GLVL_CHG	RW1C	RW1S	0	AGC Gain Level Change Interrupt Hardware sets this interrupt when a gain level change occurs. Write with '1' to clear bit.

9.8.3.10 PACSS_MMIO_INTR_SET

Description: System Interrupt set request register
Address: 0x403F0044
Offset: 0x44
Retention: Not Retained
IsDeepSleep: No
Comment: Not really a register, intended for verification/debug. When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							AGC_GLVL_CHG_SET [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	AGC_GLVL_CHG_SET	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.

9.8.3.11 PACSS_MMIO_INTR_MASK

Description: System Interrupt mask register
Address: 0x403F0048
Offset: 0x48
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							AGC_GLVL_CHG_MASK [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	AGC_GLVL_CHG_MASK	RW	R	0	Mask bit for corresponding bit in interrupt request register.

9.8.3.12 PACSS_MMIO_INTR_MASKED

Description: System Interrupt masked request register
Address: 0x403F004C
Offset: 0x4C
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							AGC_GLVL_CHG_MASKED [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	AGC_GLVL_CHG_MASKED	R	W	0	Logical and of corresponding request and mask bits.

9.8.3.13 PACSS_MMIO_INTR_CAUSE

Description: Interrupt Cause Register
Address: 0x403F0050
Offset: 0x50
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			PACSS _INT [4:4]	DCH3_INT [3:3]	DCH2_INT [2:2]	DCH1_INT [1:1]	DCH0_INT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	DCH0_INT	R	W	0	Digital Channel 0 Interrupt Pending
1	DCH1_INT	R	W	0	Digital Channel 1 Interrupt Pending
2	DCH2_INT	R	W	0	Digital Channel 2 Interrupt Pending
3	DCH3_INT	R	W	0	Digital Channel 3 Interrupt Pending
4	PACSS_INT	R	W	0	System (PACSS_MMIO) Interrupt Pending

9.8.3.14 PACSS_MMIO_STATUS0

Description: Status Register 0
Address: 0x403F0060
Offset: 0x60
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	AGC_CURR_GLVL [7:4]				None [3:2]		SEQ_BUSY [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	AGC_FAST_DEC_RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				AGC_FAST_DEC_RESULT [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	SEQ_BUSY	R	W	0	Sequencer Busy, bit per analog channel
4:7	AGC_CURR_GLVL	R	W	0	AGC Current gain level
8:19	AGC_FAST_DEC _RESULT	R	W	0	AGC Fast Decimator Result

9.8.3.15 PACSS_MMIO_STATUS1

Description: Status Register 1
Address: 0x403F0064
Offset: 0x64
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	LO_THRESH_CNTR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	LO_THRESH_CNTR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	HI_THRESH_CNTR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	HI_THRESH_CNTR [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	LO_THRESH_CNTR	R	W	0	Status of Low threshold counter
16:31	HI_THRESH_CNTR	R	W	0	Status of High threshold counter

9.8.3.16 PACSS_MMIO_HPBGR_CTL

Description: High Precision Bandgap Reference Control
Address: 0x403F0500
Offset: 0x500
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x200

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			SEL_PHC [4:4]	None [3:3]	CHOP _POS [2:2]	CHOP_CLK _SEL [1:1]	CHOP_EN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:11]					HPBGR_FCHOP [10:8]		

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	CHOP_EN	RW	R	0	HPBGR Chopping Enable (1: enable, 0: disable) ACHAN0 must be enabled, along with ACHAN0.ACHAN_CTL.MOD_EN for this bit to take affect. Setting this bit also enables a free running clock to the ACHAN0's modulator. This bit should be set to 1 by SW in the default use case.
1	CHOP_CLK_SEL	RW	R	0	Bgr core chopping phase select input (0: normal phase, 1: reverse phase)
2	CHOP_POS	RW	R	0	Chopping position select (0: normal phase, 1: reverse phase. Applies to output buffer and BGR core; BGR core is also affected by CHOP_CLK_SEL). Only applies when CHOP_EN=0.
4	SEL_PHC	RW	R	0	Buffer phase compensation option for external capacitor (0: cap present, 1: cap absent)
8:10	HPBGR_FCHOP	RW	R	2	High Precision Bandgap Reference Chopping Clock Frequency selection
	FCLOCKDIV2			0	Fclock/2
	FCLOCKDIV4			1	Fclock/4
	FCLOCKDIV8			2	Fclock/8
	FCLOCKDIV16			3	Fclock/16
	FCLOCKDIV32			4	Fclock/32
	FCLOCKDIV64			5	Fclock/64
	FCLOCKDIV128			6	Fclock/128
	FCLOCKDIV256			7	Fclock/256

9.8.3.17 PACSS_MMIO_HPBGR_DFT_CTL

Description: High Precision Bandgap Reference DFT Control
Address: 0x403F0510
Offset: 0x510
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					ADFT_MODE [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	ADFT_MODE	RW	R	0	ADFT mode select input 0 - Hi-Z 1 - IPTAT 2 - ICTAT 3 - INL1 4 - INL2 5 - VBGR_CORE 6 - Reserved 7 - Reserved

9.8.3.18 PACSS_MMIO_AREF_CTL

Description: Analog Reference Control
Address: 0x403F0600
Offset: 0x600
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							LP_MODE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	LP_MODE	RW	R	0	Low Power Mode 0 - Full power, all currents available 1 - No 2.4uA currents available, others are available AREF automatically enters low power mode when the device is DeepSleep, this bit can be used to enter low power mode when the device is in Active mode.

9.8.3.19 PACSS_MMIO_AREF_DFT_CTL

Description: Analog Reference DFT Control
Address: 0x403F0610
Offset: 0x610
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			DFT_SUM [4:4]	None [3:3]	DFT_SOURCE [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		DFT_RSEL [13:12]		DFT_CURR_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:23]	AREF_SPARE [22:20]			None [19:17]			DFT_OUT_SEL [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	DFT_SOURCE	RW	R	0	Source for current monitor directed to ADFT output 0 - Off (Hi-Z) 1 - CTAT 600nA, PTAT 600nA, CASC, PTAT 60nA 2 - PTAT 2.4uA 3 - ZTAT 2.4uA 4 - reserved 5 - reserved 6 - reserved 7 - reserved
4	DFT_SUM	RW	R	0	DFT outputs sum (0: Single currents to ADFT, 1: Sum of all currents of type selected by DFT_SOURCE are sent to ADFT)
8:11	DFT_CURR_SEL	RW	R	0	Selects which single current from DFT_SOURCE type to send to ADFT. (0: first current, 1: second current, etc, to max of available currents)
12:13	DFT_RSEL	RW	R	0	DFT Resistor Select For applying an internal pulldown resistor on the current output to amuxbus. When the pulldown is activated, both amuxbus_a and amuxbus_b connect to the resistor, allowing for kelvin connection to measure the resistor. 0 - No resistor (current output only) 1 - 10k resistor pulldown 2 - 200k resistor pulldown 3 - 1.2M resistor pulldown
16	DFT_OUT_SEL	RW	R	0	ADFT output select (0: to amuxbusa, 1: to amuxbusb)
20:22	AREF_SPARE	RW	R	0	Reserved

9.8.3.20 PACSS_MMIO_REG_PROT

Description: Register Protection
Address: 0x403F0800
Offset: 0x800
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0xF08169E7

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	MAGIC [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	MAGIC [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	MAGIC [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	MAGIC [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	MAGIC	RW	R	4035013095	Setting this register to the value 0xf08169e7 unlocks access to Lock Protected Registers. These registers can not be written to unless this value has been written into this register. Writing a value OTHER than the magic key will disable access to the registers. The register POR value is set to 'unlock' the register access.

9.8.3.21 PACSS_MMIO_PDFT_CTL

Description: PACSS DFT Control
Address: 0x403F0900
Offset: 0x900
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DDFT1_MUX_SEL [7:4]				DDFT0_MUX_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						VPOS _PMP_ TEST_EN [17:17]	LDO _BYPASS [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	DDFT0_MUX_SEL	RW	R	0	DDFT0 Output 0 - off (Low) 1 - reserved 2 - ocd1_ddft[0] 3 - ocd0_ddft[0] 4 - ocd0_dft_ls 5 - hpbgr_ddft 6 - hpbgr_en 7 - aref_lp_mode 8 - aref_enable reserved (7-15)
4:7	DDFT1_MUX_SEL	RW	R	0	DDFT1 Output 0 - off (Low) 1 - reserved 2 - ocd1_ddft[1] 3 - ocd0_ddft[1] 4 - ocd1_dft_ls 5 - hpbgr_ddft 6 - hpbgr_en 7 - aref_lp_mode 8 - aref_enable reserved (7-15)
16	LDO_BYPASS	RW	R	0	Reserved - not used
17	VPOS_PMP_TEST_EN	RW	R	0	Positive Pump Test Enable

9.8.3.22 PACSS_MMIO_TRIM_REGL0_CTL

Description: Regulator (LDO) Trim 0 (lock protected)
Address: 0x403FFF00
Offset: 0xFF00
Retention: Retained
IsDeepSleep: No
Comment: ACHAN!E29
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			COARSE [4:4]	None [3:3]	FINE [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	FINE	RW	R	0	Fine Trim
4	COARSE	RW	R	0	Coarse Trim

9.8.3.23 PACSS_MMIO_TRIM_HPBGR0_CTL

Description: High Precision Bandgap Reference Trim Control 0 (lock protected)
Address: 0x403FFF04
Offset: 0xFF04
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x80

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VREF_OS [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	VREF_OS	RW	R	128	Offset trim for HPBGR 1.2V output

9.8.3.24 PACSS_MMIO_TRIM_HPBGR1_CTL

Description: High Precision Bandgap Reference Trim Control 1 (lock protected)
Address: 0x403FFF08
Offset: 0xFF08
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x40

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	VREF_TC [6:0]						

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:6	VREF_TC	RW	R	64	First order temp-co correction trim

9.8.3.25 PACSS_MMIO_TRIM_HPBGR2_CTL

Description: High Precision Bandgap Reference Trim Control 2 (lock protected)
Address: 0x403FFF0C
Offset: 0xFF0C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x88

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VREF_NL2 [7:4]				VREF_NL1 [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	VREF_NL1	RW	R	8	Low temperature second order temp-co correction trim
4:7	VREF_NL2	RW	R	8	High temperature second order temp-co correction trim

9.8.3.26 PACSS_MMIO_TRIM_HPBGR3_CTL

Description: High Precision Bandgap Reference Trim Control 3 (lock protected)
Address: 0x403FFF10
Offset: 0xFF10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x90

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	NL_COREC _DIS [7:7]	None [6:5]		VREF_AMP [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	VREF_AMP	RW	R	16	Chopping amplifier trim
7	NL_COREC_DIS	RW	R	1	Second order temp-co correction enable (0: correction, 1: no correction)

9.8.3.27 PACSS_MMIO_TRIM_HPBGR4_CTL

Description: High Precision Bandgap Reference Trim Control 4 (lock protected)
Address: 0x403FFF14
Offset: 0xFF14
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	NL2GAIN [7:6]		NL2TEMP [5:4]		NL1GAIN [3:2]		NL1TEMP [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	NL1TEMP	RW	R	0	Non-linearity Temperature Trim 1
2:3	NL1GAIN	RW	R	0	Non-linearity Gain Trim 1
4:5	NL2TEMP	RW	R	0	Non-linearity Temperature Trim 2
6:7	NL2GAIN	RW	R	0	Non-linearity Gain Trim 2

9.8.3.28 PACSS_MMIO_TRIM_AREF0_CTL

Description: Analog Reference Trim Control 0 (lock protected)
Address: 0x403FFF18
Offset: 0xFF18
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			ICTAT [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	ICTAT	RW	R	0	Trim for AREF CTAT currents

9.8.3.29 PACSS_MMIO_TRIM_AREF1_CTL

Description: Analog Reference Trim Control 1 (lock protected)
Address: 0x403FFF1C
Offset: 0xFF1C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				IPTAT_COARSE [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	IPTAT_COARSE	RW	R	0	Coarse Trim for AREF PTAT currents

9.8.3.30 PACSS_MMIO_TRIM_AREF2_CTL

Description: Analog Reference Trim Control 2 (lock protected)
Address: 0x403FFF20
Offset: 0xFF20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			IPTAT_FINE [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	IPTAT_FINE	RW	R	0	Fine Trim for AREF PTAT currents

9.8.3.31 PACSS_MMIO_TRIM_AREF3_CTL

Description: Analog Reference Trim Control 3 (lock protected)
Address: 0x403FFF24
Offset: 0xFF24
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					PTAT_DAC [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	PTAT_DAC	RW	R	0	Trim for AREF PTAT DAC

9.8.3.32 PACSS_MMIO_TRIM_AREF4_CTL

Description: Analog Reference Trim Control 4 (lock protected)
Address: 0x403FFF28
Offset: 0xFF28
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				ZTAT_COARSE [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	ZTAT_COARSE	RW	R	0	Coarse Trim for AREF ZTAT

9.8.3.33 PACSS_MMIO_TRIM_AREF5_CTL

Description: Analog Reference Trim Control 5 (lock protected)
Address: 0x403FFF2C
Offset: 0xFF2C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			ZTAT_FINE [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	ZTAT_FINE	RW	R	0	Fine Trim for AREF ZTAT Only bits [3:0] are functional. Bit 4 is a spare bit.

9.8.3.34 PACSS_MMIO_TRIM_AREF6_CTL

Description: Analog Reference Trim Control 6 (lock protected)
Address: 0x403FFF30
Offset: 0xFF30
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				CTAT_COARSE [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	CTAT_COARSE	RW	R	0	Coarse Trim for AREF CTAT

9.8.3.35 GAINLVL_STRUCT

9.8.3.35.1 PACSS_MMIO_GAIN_CFG0

Description: Gain configuration register 0
Address: 0x403F0100
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: CR8-11
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SHIFT1 [7:4]				None [3:3]	PGA_GAIN [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:22]		DACCAP [21:16]					

Bits	31	30	29	28	27	26	25	24
Name	None [31:30]		IPCAP1 [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	PGA_GAIN	RW	R	0	Gain setting of 1,2,4,8,16, 32 are supported
	GAIN_1X			0	1x
	GAIN_2X			1	2x
	GAIN_4X			2	4x
	GAIN_8X			3	8x
	GAIN_16X			4	16x
	GAIN_32X			5	32x
4:7	SHIFT1	RW	R	0	Value for left shift amount (see SHIFTL in DEC_CTL)
16:21	DACCAP	RW	R	0	Binary weighted first stage DAC capacitance
	DACCAP_min			0	Min Value = 96 fF
	DACCAP_max			63	Max Value = 6.4 pF
	DACCAP_96fF			1	DACCAP[0] set -> add 12*8= +96 fF
	DACCAP_192fF			2	DACCAP[1] set -> add 24*8= +192 fF
	DACCAP_400fF			4	DACCAP[2] set -> add 50*8= +400 fF
	DACCAP_800fF			8	DACCAP[3] set -> add 100*8= +800 fF
	DACCAP_1600fF			16	DACCAP[4] set -> add 200*8= +1600 fF
	DACCAP_3200fF			32	DACCAP[5] set -> add 400*8= +3200 fF
24:29	IPCAP1	RW	R	0	Binary weighted first stage integrating capacitance
	IPCAP1_min			0	Min Value = 100 fF
	IPCAP1_max			63	Max Value = 6.4 pF
	IPCAP1_100fF			1	IPCAP1[0] set -> +100 fF
	IPCAP1_200fF			2	IPCAP1[1] set -> +200 fF
	IPCAP1_400fF			4	IPCAP1[2] set -> +400 fF
	IPCAP1_80fF			8	IPCAP1[3] set -> +800 fF
	IPCAP1_1600fF			16	IPCAP1[4] set -> +1600 fF
	IPCAP1_3200fF			32	IPCAP1[5] set -> +3200 fF

9.8.3.35.2 PACSS_MMIO_GAIN_CFG1

Description: Gain configuration register 1
Address: 0x403F0104
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: CR12,14,15,16
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			SUMCAPIN [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	SUMCAP2 [14:12]			None [11:11]	SUMCAP1 [10:8]		

Bits	23	22	21	20	19	18	17	16
Name	SUMCAPFB [23:20]				None [19:19]	SUMCAP3 [18:16]		

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	SUMCAPIN	RW	R	0	The summer capacitance that lies on the path where the input signal is summed
	SUMCAPIN_50fF			0	50fF
	SUMCAPIN_100fF			1	100fF
	SUMCAPIN_150fF			2	150fF
	SUMCAPIN_200fF			3	200fF
	SUMCAPIN_250fF			4	250fF
	SUMCAPIN_300fF			5	300fF
	SUMCAPIN_350fF			6	350fF
	SUMCAPIN_400fF			7	400fF
	SUMCAPIN_450fF			8	450fF
	SUMCAPIN_500fF			9	500fF
	SUMCAPIN_550fF			10	550fF
	SUMCAPIN_600fF			11	600fF
	SUMCAPIN_650fF			12	650fF
	SUMCAPIN_700fF			13	700fF
	SUMCAPIN_750fF			14	750fF
	SUMCAPIN_800fF			15	800fF
	SUMCAPIN_850fF			16	850fF
	SUMCAPIN_900fF			17	900fF
	SUMCAPIN_950fF			18	950fF
	SUMCAPIN_1000fF			19	1000fF
	SUMCAPIN_1050fF			20	1050fF
	SUMCAPIN_1100fF			21	1100fF
	SUMCAPIN_1150fF			22	1150fF
	SUMCAPIN_1200fF			23	1200fF
	SUMCAPIN_1250fF			24	1250fF
	SUMCAPIN_1300fF			25	1300fF
	SUMCAPIN_1350fF			26	1350fF

Bits	Name	SW	HW	Default or Enum	Description
	SUMCAPIN_1400fF			27	1400fF
	SUMCAPIN_1450fF			28	1450fF
	SUMCAPIN_1500fF			29	1500fF
	SUMCAPIN_1550fF			30	1550fF
	SUMCAPIN_1600fF			31	1600fF
8:10	SUMCAP1	RW	R	0	The summer capacitance that lies on the feed-forward path from the first integrator output
	SUMCAP1_50fF			0	50fF
	SUMCAP1_100fF			1	100fF
	SUMCAP1_150fF			2	150fF
	SUMCAP1_200fF			3	200fF
	SUMCAP1_250fF			4	250fF
	SUMCAP1_300fF			5	300fF
	SUMCAP1_350fF			6	350fF
	SUMCAP1_400fF			7	400fF
12:14	SUMCAP2	RW	R	0	The summer capacitance that lies on the feed-forward path from the second integrator output
	SUMCAP2_50fF			0	50fF
	SUMCAP2_100fF			1	100fF
	SUMCAP2_150fF			2	150fF
	SUMCAP2_200fF			3	200fF
	SUMCAP2_250fF			4	250fF
	SUMCAP2_300fF			5	300fF
	SUMCAP2_350fF			6	350fF
	SUMCAP2_400fF			7	400fF
16:18	SUMCAP3	RW	R	0	The summer capacitance that lies on the feed-forward path from the third integrator output
	SUMCAP3_50fF			0	50fF
	SUMCAP3_100fF			1	100fF
	SUMCAP3_150fF			2	150fF
	SUMCAP3_200fF			3	200fF
	SUMCAP3_250fF			4	250fF
	SUMCAP3_300fF			5	300fF
	SUMCAP3_350fF			6	350fF
	SUMCAP3_400fF			7	400fF
20:23	SUMCAPFB	RW	R	0	The summer feedback capacitance
	SUMCAPFB_50fF			0	50fF
	SUMCAPFB_100fF			1	100fF
	SUMCAPFB_150fF			2	150fF
	SUMCAPFB_200fF			3	200fF
	SUMCAPFB_250fF			4	250fF
	SUMCAPFB_300fF			5	300fF
	SUMCAPFB_350fF			6	350fF
	SUMCAPFB_400fF			7	400fF
	SUMCAPFB_450fF			8	450fF
	SUMCAPFB_500fF			9	500fF
	SUMCAPFB_550fF			10	550fF
	SUMCAPFB_600fF			11	600fF
	SUMCAPFB_650fF			12	650fF
	SUMCAPFB_700fF			13	700fF
	SUMCAPFB_750fF			14	750fF
	SUMCAPFB_800fF			15	800fF

9.8.3.35.3 PACSS_MMIO_OFST_COR

Description: Offset Correction register
Address: 0x403F0108
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	OCOR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	OCOR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	OCOR	RW	R	0	Decimator Offset Correction Coefficient See DCHAN.OCOR_COR for description details

9.8.3.35.4 PACSS_MMIO_GAIN_COR

Description: Gain Correction register
Address: 0x403F010C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	GCOR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	GCOR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	GCOR	RW	R	0	Decimator Gain Correction Coefficient See DCHAN.GAIN_COR for description details

10 PERI

Description Peripheral Interconnect
Base Address 0x40010000
Size 0x10000
Slave Num MMIO0

Register Name	Address	Permission	Description
PERI_DIV_CMD	0x40010000	FULL	Divider command register
PERI_PCLK_CTL0	0x40010100	FULL	Programmable clock control register
PERI_PCLK_CTL1	0x40010104	FULL	Programmable clock control register
PERI_PCLK_CTL2	0x40010108	FULL	Programmable clock control register
PERI_PCLK_CTL3	0x4001010C	FULL	Programmable clock control register
PERI_PCLK_CTL4	0x40010110	FULL	Programmable clock control register
PERI_PCLK_CTL5	0x40010114	FULL	Programmable clock control register
PERI_PCLK_CTL6	0x40010118	FULL	Programmable clock control register
PERI_PCLK_CTL7	0x4001011C	FULL	Programmable clock control register
PERI_DIV_16_CTL0	0x40010300	FULL	Divider control register (for 16.0 divider)
PERI_DIV_16_CTL1	0x40010304	FULL	Divider control register (for 16.0 divider)
PERI_DIV_16_CTL2	0x40010308	FULL	Divider control register (for 16.0 divider)
PERI_DIV_16_CTL3	0x4001030C	FULL	Divider control register (for 16.0 divider)
PERI_DIV_16_5_CTL0	0x40010400	FULL	Divider control register (for 16.5 divider)
PERI_DIV_16_5_CTL1	0x40010404	FULL	Divider control register (for 16.5 divider)
PERI_TR_CTL	0x40010600	FULL	Trigger control register

10.1 TR_GROUP 0

Register Name	Address	Permission	Description
PERI_TR_GROUP0_TR_OUT_CTL0	0x40012000	FULL	Trigger control register
PERI_TR_GROUP0_TR_OUT_CTL1	0x40012004	FULL	Trigger control register
PERI_TR_GROUP0_TR_OUT_CTL2	0x40012008	FULL	Trigger control register
PERI_TR_GROUP0_TR_OUT_CTL3	0x4001200C	FULL	Trigger control register
PERI_TR_GROUP0_TR_OUT_CTL4	0x40012010	FULL	Trigger control register
PERI_TR_GROUP0_TR_OUT_CTL5	0x40012014	FULL	Trigger control register
PERI_TR_GROUP0_TR_OUT_CTL6	0x40012018	FULL	Trigger control register
PERI_TR_GROUP0_TR_OUT_CTL7	0x4001201C	FULL	Trigger control register

10.2 TR_GROUP 1

Register Name	Address	Permission	Description
PERI_TR_GROUP1_TR_OUT_CTL0	0x40012200	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL1	0x40012204	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL2	0x40012208	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL3	0x4001220C	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL4	0x40012210	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL5	0x40012214	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL6	0x40012218	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL7	0x4001221C	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL8	0x40012220	FULL	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL9	0x40012224	FULL	Trigger control register

10.3 TR_GROUP 2

Register Name	Address	Permission	Description
PERI_TR_GROUP2_TR_OUT_CTL0	0x40012400	FULL	Trigger control register
PERI_TR_GROUP2_TR_OUT_CTL1	0x40012404	FULL	Trigger control register
PERI_TR_GROUP2_TR_OUT_CTL2	0x40012408	FULL	Trigger control register
PERI_TR_GROUP2_TR_OUT_CTL3	0x4001240C	FULL	Trigger control register

10.4 TR_GROUP 3

Register Name	Address	Permission	Description
PERI_TR_GROUP3_TR_OUT_CTL0	0x40012600	FULL	Trigger control register
PERI_TR_GROUP3_TR_OUT_CTL1	0x40012604	FULL	Trigger control register

10.5 Register Details

10.5.1 PERI_DIV_CMD

Description: Divider command register
Address: 0x40010000
Offset: 0x0
Retention: Not Retained
IsDeepSleep: No
Comment: The (PA_SEL_TYPE, PA_SEL_DIV) field pair allows a divider to be phase aligned with another divider. E.g., consider a 48 MHz 'clk_hf', and a need for a 12 MHz divided clock A and a 8 MHz divided clock B. Clock A uses 8.0 integer divider 0 and is created by aligning it to 'clk_hf' ((PA_SEL_TYPE, PA_SEL_DIV) is (3, 63)) and DIV_8_CTL0.INT8_DIV is '4-1'. Clock B uses 8.0 integer divider 1 and is created by aligning it to clock A ((PA_SEL_TYPE, PA_SEL_DIV) is (0, 0)) and DIV_8_CTL1.INT8_DIV is '6-1'. This guarantees that clock B is phase aligned with clock B: as the smallest common multiple of the two clock periods is 12 'clk_hf' cycles, the clocks A and B will be aligned every 12 'clk_hf' cycles. Note: clock B is phase aligned to clock A, but still uses 'clk_hf' as a reference clock for its divider value.
Default: 0xFFFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SEL_TYPE [7:6]		SEL_DIV [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	PA_SEL_TYPE [15:14]		PA_SEL_DIV [13:8]					

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLE [31:31]	DISABLE [30:30]	None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	SEL_DIV	RW	R	63	(SEL_TYPE, SEL_DIV) specifies the divider on which the command (DISABLE/ENABLE) is performed. If SEL_DIV is '63' and 'SEL_TYPE' is '3' (default/reset value), no divider is specified and no clock signal(s) are generated.
6:7	SEL_TYPE	RW	R	3	Specifies the divider type of the divider on which the command is performed: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers.
8:13	PA_SEL_DIV	RW	R	63	(PA_SEL_TYPE, PA_SEL_DIV) specifies the divider to which phase alignment is performed for the clock enable command. Any enabled divider can be used as reference. This allows all dividers to be aligned with each other, even when they are enabled at different times. If PA_SEL_DIV is '63' and 'PA_SEL_TYPE' is '3', 'clk_hf' is used as reference.

Bits	Name	SW	HW	Default or Enum	Description
14:15	PA_SEL_TYPE	RW	R	3	Specifies the divider type of the divider to which phase alignment is performed for the clock enable command: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers.
30	DISABLE	RW	RW1C	0	Clock divider disable command (mutually exclusive with ENABLE). SW sets this field to '1' and HW sets this field to '0'. The SEL_DIV and SEL_TYPE fields specify which divider is to be disabled. The HW sets the DISABLE field to '0' immediately and the HW sets the DIV_XXX_CTL.EN field of the divider to '0' immediately.
31	ENABLE	RW	RW1C	0	Clock divider enable command (mutually exclusive with DISABLE). Typically, SW sets this field to '1' to enable a divider and HW sets this field to '0' to indicate that divider enabling has completed. When a divider is enabled, its integer and fractional (if present) counters are initialized to '0'. If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps: 0: Disable the divider using the DIV_CMD.DISABLE field. 1: Configure the divider's DIV_XXX_CTL register. 2: Enable the divider using the DIV_CMD_ENABLE field. The SEL_DIV and SEL_TYPE fields specify which divider is to be enabled. The enabled divider may be phase aligned to either 'clk_hf' (typical usage) or to ANY enabled divider. The PA_SEL_DIV and P_SEL_TYPE fields specify the reference divider. The HW sets the ENABLE field to '0' when the enabling is performed and the HW sets the DIV_XXX_CTL.EN field of the divider to '1' when the enabling is performed. Note that enabling with phase alignment to a low frequency divider takes time. E.g. To align to a divider that generates a clock of 'clk_hf'/n (with n being the integer divider value INT_DIV+1), up to n cycles may be required to perform alignment. Phase alignment to 'clk_hf' takes affect immediately. SW can set this field to '0' during phase alignment to abort the enabling process.

10.5.2 PERI_PCLK_CTL

Description: Programmable clock control register
Address: 0x40010100
Offset: 0x100
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SEL_TYPE [7:6]		SEL_DIV [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	SEL_DIV	RW	R	63	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is '63' and 'SEL_TYPE' is '3' (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one 'clk_hf' cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is '63' and 'SEL_TYPE' is '3') for a transition time that is larger than the smaller of the two divider periods.
6:7	SEL_TYPE	RW	R	3	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers.

10.5.3 PERI_DIV_16_CTL

Description: Divider control register (for 16.0 divider)
Address: 0x40010300
Offset: 0x300
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							EN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	EN	R	RW	0	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode.
8:23	INT16_DIV	RW	R	0	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50 percent duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 percent duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode.

10.5.4 PERI_DIV_16_5_CTL

Description: Divider control register (for 16.5 divider)
Address: 0x40010400
Offset: 0x400
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	FRAC5_DIV [7:3]					None [2:1]		EN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	EN	R	RW	0	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode.
3:7	FRAC5_DIV	RW	R	0	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 'clk_hf' cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode.
8:23	INT16_DIV	RW	R	0	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50 percent duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode.

10.5.5 PERI_TR_CTL

Description: Trigger control register
Address: 0x40010600
Offset: 0x600
Retention: Not Retained
IsDeepSleep: No
Comment: This register provides SW control over trigger activation. This is useful for SW initiated triggers (e.g. DW/DMA transfers) or for debugging purposes. The control enables SW activation of one specific input trigger or output trigger of the trigger multiplexer structure.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	TR_SEL [6:0]						

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				TR_GROUP [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	TR_COUNT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	TR_ACT [31:31]	TR_OUT [30:30]	None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:6	TR_SEL	RW	R	0	Specifies the activated trigger when TR_ACT is '1'. TR_OUT specifies whether the activated trigger is an input trigger or output trigger to the trigger multiplexer. During activation (TR_ACT is '1'), SW should not modify this register field. If the specified trigger is not present, the trigger activation has no effect.
8:11	TR_GROUP	RW	R	0	Specifies the trigger group.
16:23	TR_COUNT	RW	RW	0	Amount of cycles a specific trigger is activated. During activation (TR_ACT is '1'), HW decrements this field to '0' using a cycle counter. During activation, SW should not modify this register field. A value of 255 is a special case: HW does NOT decrement this field to '0' and trigger activation is under direct control of TR_ACT: when TR_ACT is '1' the trigger is activated and when TR_ACT is '0' the trigger is deactivated.
30	TR_OUT	RW	R	0	Specifies whether trigger activation is for a specific input or output trigger of the trigger multiplexer. Activation of a specific input trigger, will result in activation of all output triggers that have the specific input trigger selected through their TR_OUT_CTL.SEL field. Activation of a specific output trigger, will result in activation of the specified TR_SEL output trigger only. '0': TR_SEL selection and trigger activation is for an input trigger to the trigger multiplexer. '1': TR_SEL selection and trigger activation is for an output trigger from the trigger multiplexer.

Bits	Name	SW	HW	Default or Enum	Description
31	TR_ACT	RW	RW1C	0	SW sets this field to '1' to activate (set to '1') a trigger as identified by TR_SEL and TR_OUT for TR_COUNT cycles. HW sets this field to '0' when the cycle counter is decremented to '0'. Note: a TR_COUNT value of 255 is a special case and trigger activation is under direct control of the TR_ACT field (the counter is not decremented). Note: when TR_ACT is '1', SW should not modify the other register fields. SW MUST NOT set TR_ACT bit to '1' while updating the other register bits simultaneously. At first the SW MUST update the other register bits as needed, and then set TR_ACT to '1' with a new register write.'

10.5.6 TR_GROUP

10.5.6.1 PERI_TR_GROUP_TR_OUT_CTL

Description: Trigger control register
Address: 0x40012000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: This register specifies the input trigger for a specific output trigger in trigger group 0. Note that for SW initiated triggers, SW is responsible for activating the output trigger, rather than relying on a specific HW input trigger. For this reason, input trigger 0 is typically connected to a constant signal level of '0' at chip integration (design decision) and SW initiated output triggers are all connected to input trigger 0 (SW responsibility: TR_OUT_CTL.TR_SEL should be set to '0' to select the constant signal level '0' from chip level). As a result, SW initiated triggers can never be activated by a HW input trigger to the trigger multiplexer.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	SEL [6:0]						

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:6	SEL	RW	R	0	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger.

11 ROMTABLE

Description CoreSight ROM-Table with Infineon Vendor/Silicon ID
Base Address 0xF0000000
Size 0x1000
Slave Num MEMORYMAP

Register Name	Address	Permission	Description
ROMTABLE_ADDR	0xF0000000	FULL	Link to Cortex M0 ROM Table.
ROMTABLE_DID	0xF0000FCC	FULL	Device Type Identifier register.
ROMTABLE_PID4	0xF0000FD0	FULL	Peripheral Identification Register 4.
ROMTABLE_PID5	0xF0000FD4	FULL	Peripheral Identification Register 5.
ROMTABLE_PID6	0xF0000FD8	FULL	Peripheral Identification Register 6.
ROMTABLE_PID7	0xF0000FDC	FULL	Peripheral Identification Register 7.
ROMTABLE_PID0	0xF0000FE0	FULL	Peripheral Identification Register 0.
ROMTABLE_PID1	0xF0000FE4	FULL	Peripheral Identification Register 1.
ROMTABLE_PID2	0xF0000FE8	FULL	Peripheral Identification Register 2.
ROMTABLE_PID3	0xF0000FEC	FULL	Peripheral Identification Register 3.
ROMTABLE_CID0	0xF0000FF0	FULL	Component Identification Register 0.
ROMTABLE_CID1	0xF0000FF4	FULL	Component Identification Register 1.
ROMTABLE_CID2	0xF0000FF8	FULL	Component Identification Register 2.
ROMTABLE_CID3	0xF0000FFC	FULL	Component Identification Register 3.

11.1 Register Details

11.1.1 ROMTABLE_ADDR

Description: Link to Cortex M0 ROM Table.
Address: 0xF0000000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xF00FF003

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						FORMAT_32BIT [1:1]	PRESENT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	ADDR_OFFSET [15:12]				None [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	ADDR_OFFSET [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ADDR_OFFSET [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	PRESENT	R	R	1	Entry present.
1	FORMAT_32BIT	R	R	1	ROM Table format: '0: 8-bit format. '1': 32-bit format.
12:31	ADDR_OFFSET	R	R	983295	Address offset of the Cortex-M0 ROM Table base address (0xe00f:f000) wrt. Infineon chip specific ROM Table base address (0xf000:0000). ADDR_OFFSET[19:0] = 0xe00f:f - 0xf000:0 = 0xf00f:f.

11.1.2 ROMTABLE_DID

Description: Device Type Identifier register.
Address: 0xF0000FCC
Offset: 0xFCC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R	R	1	.

11.1.3 ROMTABLE_PID4

Description: Peripheral Identification Register 4.
Address: 0xF0000FD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	COUNT [7:4]				JEP_CONTINUATION [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	JEP_CONTINUATION	R	R	Undefined	JEP106 continuation code. This value is product specific and specified as part of the product definition in the CPUSS.JEPCONTINUATION parameter.
4:7	COUNT	R	R	0	Size of ROM Table is 2^COUNT * 4 KByte.

11.1.4 ROMTABLE_PID5

Description: Peripheral Identification Register 5.
Address: 0xF0000FD4
Offset: 0xFD4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R	R	0	.

11.1.5 ROMTABLE_PID6

Description: Peripheral Identification Register 6.
Address: 0xF0000FD8
Offset: 0xFD8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R	R	0	.

11.1.6 ROMTABLE_PID7

Description: Peripheral Identification Register 7.
Address: 0xF0000FDC
Offset: 0xFDC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R	R	0	.

11.1.7 ROMTABLE_PID0

Description: Peripheral Identification Register 0.
Address: 0xF0000FE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PN_MIN [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	PN_MIN	R	R	Undefined	JEP106 part number. 4 lsbs of CPUSS.PARTNUMBER parameter.

11.1.8 ROMTABLE_PID1

Description: Peripheral Identification Register 1.
Address: 0xF0000FE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	JEPID_MIN [7:4]				PN_MAJ [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	PN_MAJ	R	R	Undefined	JEP106 part number. 4 msbs of CPUSS.PARTNUMBER parameter.
4:7	JEPID_MIN	R	R	Undefined	JEP106 vendor id. 4 lsbs of CPUSS.JEPID parameter.

11.1.9 ROMTABLE_PID2

Description: Peripheral Identification Register 2.
Address: 0xF0000FE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	REV [7:4]				JEPID_MAJ [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	JEPID_MAJ	R	R	Undefined	JEP106 vendor id. 4 msbs of CPUSS.JEPID parameter.
4:7	REV	R	R	Undefined	Major REVision number (chip specific). Identifies the design iteration of the component. For first tape out: 0x1. This field is incremented on subsequent tape outs.

11.1.10 ROMTABLE_PID3

Description: Peripheral Identification Register 3.
Address: 0xF0000FEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	REV_AND [7:4]				CM [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	CM	R	R	0	Customer modified field. This field is used to track modifications to the original component design as a result of component IP reuse.
4:7	REV_AND	R	R	Undefined	Minor REVision number (chip specific). For first tape out: 0x1. This field is incremented on subsequent tape outs.

11.1.11 ROMTABLE_CID0

Description: Component Identification Register 0.
Address: 0xF0000FF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R	R	13	Component identification byte 0 of 4-byte component identification 0xB105:100D.

11.1.12 ROMTABLE_CID1

Description: Component Identification Register 1.
Address: 0xF0000FF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x10

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R	R	16	Component identification byte 1 of 4-byte component identification 0xB105:100D. Component class: 'ROM Table'.

11.1.13 ROMTABLE_CID2

Description: Component Identification Register 2.
Address: 0xF0000FF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R	R	5	Component identification byte 2 of 4-byte component identification 0xB105:100D.

11.1.14 ROMTABLE_CID3

Description: Component Identification Register 3.
Address: 0xF0000FFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	VALUE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	VALUE	R	R	177	Component identification byte 3 of 4-byte component identification 0xB105:100D.

12 SCB

Description Serial Communications Block (SPI/UART/I2C)
Base Address 0x40240000
Size 0x10000
Slave Num MMIO1

Register Name	Address	Permission	Description
SCB_CTRL	0x40240000	FULL	Generic control register.
SCB_STATUS	0x40240004	FULL	Generic status register.
SCB_CMD_RESP_CTRL	0x40240008	FULL	Command/response control register.
SCB_CMD_RESP_STATUS	0x4024000C	FULL	Command/response status register.
SCB_SPI_CTRL	0x40240020	FULL	SPI control register.
SCB_SPI_STATUS	0x40240024	FULL	SPI status register.
SCB_UART_CTRL	0x40240040	FULL	UART control register.
SCB_UART_TX_CTRL	0x40240044	FULL	UART transmitter control register.
SCB_UART_RX_CTRL	0x40240048	FULL	UART receiver control register.
SCB_UART_RX_STATUS	0x4024004C	FULL	UART receiver status register.
SCB_I2C_CTRL	0x40240060	FULL	I2C control register.
SCB_I2C_STATUS	0x40240064	FULL	I2C status register.
SCB_I2C_M_CMD	0x40240068	FULL	I2C master command register.
SCB_I2C_S_CMD	0x4024006C	FULL	I2C slave command register.
SCB_I2C_CFG	0x40240070	FULL	I2C configuration register.
SCB_TX_CTRL	0x40240200	FULL	Transmitter control register.
SCB_TX_FIFO_CTRL	0x40240204	FULL	Transmitter FIFO control register.
SCB_TX_FIFO_STATUS	0x40240208	FULL	Transmitter FIFO status register.
SCB_TX_FIFO_WR	0x40240240	FULL	Transmitter FIFO write register.
SCB_RX_CTRL	0x40240300	FULL	Receiver control register.
SCB_RX_FIFO_CTRL	0x40240304	FULL	Receiver FIFO control register.
SCB_RX_FIFO_STATUS	0x40240308	FULL	Receiver FIFO status register.
SCB_RX_MATCH	0x40240310	FULL	Slave address and mask register.
SCB_RX_FIFO_RD	0x40240340	FULL	Receiver FIFO read register.
SCB_RX_FIFO_RD_SILENT	0x40240344	FULL	Receiver FIFO read register.
SCB_EZ_DATA0	0x40240400	FULL	Memory buffer registers.
SCB_EZ_DATA1	0x40240404	FULL	Memory buffer registers.
SCB_EZ_DATA2	0x40240408	FULL	Memory buffer registers.
SCB_EZ_DATA3	0x4024040C	FULL	Memory buffer registers.
SCB_EZ_DATA4	0x40240410	FULL	Memory buffer registers.
SCB_EZ_DATA5	0x40240414	FULL	Memory buffer registers.
SCB_EZ_DATA6	0x40240418	FULL	Memory buffer registers.
SCB_EZ_DATA7	0x4024041C	FULL	Memory buffer registers.
SCB_EZ_DATA8	0x40240420	FULL	Memory buffer registers.
SCB_EZ_DATA9	0x40240424	FULL	Memory buffer registers.
SCB_EZ_DATA10	0x40240428	FULL	Memory buffer registers.
SCB_EZ_DATA11	0x4024042C	FULL	Memory buffer registers.
SCB_EZ_DATA12	0x40240430	FULL	Memory buffer registers.
SCB_EZ_DATA13	0x40240434	FULL	Memory buffer registers.
SCB_EZ_DATA14	0x40240438	FULL	Memory buffer registers.
SCB_EZ_DATA15	0x4024043C	FULL	Memory buffer registers.
SCB_EZ_DATA16	0x40240440	FULL	Memory buffer registers.
SCB_EZ_DATA17	0x40240444	FULL	Memory buffer registers.
SCB_EZ_DATA18	0x40240448	FULL	Memory buffer registers.
SCB_EZ_DATA19	0x4024044C	FULL	Memory buffer registers.
SCB_EZ_DATA20	0x40240450	FULL	Memory buffer registers.
SCB_EZ_DATA21	0x40240454	FULL	Memory buffer registers.
SCB_EZ_DATA22	0x40240458	FULL	Memory buffer registers.
SCB_EZ_DATA23	0x4024045C	FULL	Memory buffer registers.
SCB_EZ_DATA24	0x40240460	FULL	Memory buffer registers.
SCB_EZ_DATA25	0x40240464	FULL	Memory buffer registers.
SCB_EZ_DATA26	0x40240468	FULL	Memory buffer registers.
SCB_EZ_DATA27	0x4024046C	FULL	Memory buffer registers.
SCB_EZ_DATA28	0x40240470	FULL	Memory buffer registers.

Register Name	Address	Permission	Description
SCB_EZ_DATA29	0x40240474	FULL	Memory buffer registers.
SCB_EZ_DATA30	0x40240478	FULL	Memory buffer registers.
SCB_EZ_DATA31	0x4024047C	FULL	Memory buffer registers.
SCB_INTR_CAUSE	0x40240E00	FULL	Active clocked interrupt signal register
SCB_INTR_I2C_EC	0x40240E80	FULL	Externally clocked I2C interrupt request register
SCB_INTR_I2C_EC_MASK	0x40240E88	FULL	Externally clocked I2C interrupt mask register
SCB_INTR_I2C_EC_MASKED	0x40240E8C	FULL	Externally clocked I2C interrupt masked register
SCB_INTR_SPI_EC	0x40240EC0	FULL	Externally clocked SPI interrupt request register
SCB_INTR_SPI_EC_MASK	0x40240EC8	FULL	Externally clocked SPI interrupt mask register
SCB_INTR_SPI_EC_MASKED	0x40240ECC	FULL	Externally clocked SPI interrupt masked register
SCB_INTR_M	0x40240F00	FULL	Master interrupt request register.
SCB_INTR_M_SET	0x40240F04	FULL	Master interrupt set request register
SCB_INTR_M_MASK	0x40240F08	FULL	Master interrupt mask register.
SCB_INTR_M_MASKED	0x40240F0C	FULL	Master interrupt masked request register
SCB_INTR_S	0x40240F40	FULL	Slave interrupt request register.
SCB_INTR_S_SET	0x40240F44	FULL	Slave interrupt set request register.
SCB_INTR_S_MASK	0x40240F48	FULL	Slave interrupt mask register.
SCB_INTR_S_MASKED	0x40240F4C	FULL	Slave interrupt masked request register
SCB_INTR_TX	0x40240F80	FULL	Transmitter interrupt request register.
SCB_INTR_TX_SET	0x40240F84	FULL	Transmitter interrupt set request register
SCB_INTR_TX_MASK	0x40240F88	FULL	Transmitter interrupt mask register.
SCB_INTR_TX_MASKED	0x40240F8C	FULL	Transmitter interrupt masked request register
SCB_INTR_RX	0x40240FC0	FULL	Receiver interrupt request register.
SCB_INTR_RX_SET	0x40240FC4	FULL	Receiver interrupt set request register.
SCB_INTR_RX_MASK	0x40240FC8	FULL	Receiver interrupt mask register.
SCB_INTR_RX_MASKED	0x40240FCC	FULL	Receiver interrupt masked request register

12.1 Register Details

12.1.1 SCB_CTRL

Description: Generic control register.
Address: 0x40240000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x300000F

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			CMD_RESP_MODE [12:12]	BYTE_MODE [11:11]	EZ_MODE [10:10]	EC_OP_MODE [9:9]	EC_AM_MODE [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						BLOCK [17:17]	ADDR_ACCEPT [16:16]

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	None [30:26]					MODE [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	OVS	RW	R	15	Serial interface bit period oversampling factor expressed in SCB clock cycles. Used for SPI and UART functionality. OVS + 1 SCB clock cycles constitute a single serial interface clock/bit cycle. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period. In SPI master mode, the valid range is [3, 15]. At an SCB frequency of 48 MHz, the maximum SPI bit rate is 12 Mbps, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock to SPI MISO input round trip delay is significant (multiple SPI output clock cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the SPI input clock (IF) on the interface to guarantee functional correct behavior. This requirement is expressed as a ratio: SCB clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support 'late MISO sample' functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO 'late MISO sample functionality': SCB clock/IF clock >= 6. At a SCB frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has 'late MISO sample functionality': SCB clock/IF clock >= 3. At a SCB frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO 'late MISO sample functionality': SCB clock/IF clock >= 8. At a SCB frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has 'late MISO sample functionality': SCB clock/IF clock >= 4. At a SCB frequency of 48 MHz, the maximum bit rate is 12 Mbps. As discussed earlier, the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15].

Bits	Name	SW	HW	Default or Enum	Description
					(Continuation) In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. SCB clock frequency of 16*115.2 kHz for 115.2 kbps. SCB clock frequency of 16*57.6 kHz for 57.6 kbps. SCB clock frequency of 16*38.4 kHz for 38.4 kbps. SCB clock frequency of 16*19.2 kHz for 19.2 kbps. SCB clock frequency of 16*9.6 kHz for 9.6 kbps. SCB clock frequency of 16*2.4 kHz for 2.4 kbps. SCB clock frequency of 16*1.2 kHz for 1.2 kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The SCB clock (as provided by the programmable clock block) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 kHz for 115.2 kbps. SCB clock frequency of 16*57.6 kHz for 57.6 kbps. SCB clock frequency of 16*38.4 kHz for 38.4 kbps. SCB clock frequency of 16*19.2 kHz for 19.2 kbps. SCB clock frequency of 16*9.6 kHz for 9.6 kbps. SCB clock frequency of 16*2.4 kHz for 2.4 kbps. SCB clock frequency of 16*1.2 kHz for 1.2 kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 kHz for 115.2 kbps. - 1: 32 times oversampling. SCB clock frequency of 32*57.6 kHz for 57.6 kbps. - 2: 48 times oversampling. SCB clock frequency of 48*38.4 kHz for 38.4 kbps. - 3: 96 times oversampling. SCB clock frequency of 96*19.2 kHz for 19.2 kbps. - 4: 192 times oversampling.

Bits	Name	SW	HW	Default or Enum	Description
					(Continuation) SCB clock frequency of 192*9.6 kHz for 9.6 kbps. - 5: 768 times oversampling. SCB clock frequency of 768*2.4 kHz for 2.4 kbps. - 6: 1536 times oversampling. SCB clock frequency of 1536*1.2 kHz for 1.2 kbps. - all other values are not used in low power mode.
8	EC_AM_MODE	RW	R	0	This field specifies the clocking for the address matching (I2C) or slave selection detection logic (SPI) '0': Internally clocked mode '1': Externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. The clocking for the rest of the logic is determined by CTRL.EC_OP_MODE. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'.
9	EC_OP_MODE	RW	R	0	This field specifies the clocking for the SCB block '0': Internally clocked mode '1': externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'.
10	EZ_MODE	RW	R	0	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames not separated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'.

Bits	Name	SW	HW	Default or Enum	Description
11	BYTE_MODE	RW	R	0	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7].
12	CMD_RESP_MODE	RW	R	0	Determines CMD_RESP mode of operation: '0': CMD_RESP mode disabled. '1': CMD_RESP mode enabled (also requires EC_AM_MODE and EC_OP_MODE to be set to '1').
16	ADDR_ACCEPT	RW	R	0	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO.
17	BLOCK	RW	R	0	Only used in externally clocked mode. If the externally clocked logic and the internal CPU accesses to EZ memory coincide/collide, this bit determines whether the CPU access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is '0' and the accesses collide, CPU read operations return 0xffff:ffff and CPU write operations are ignored. Colliding accesses are registered as interrupt causes: INTR_TX.BLOCKED and INTR_RX.BLOCKED.
24:25	MODE	RW	R	3	Mode of operation (3: Reserved)
	I2C			0	Inter-Integrated Circuits (I2C) mode.
	SPI			1	Serial Peripheral Interface (SPI) mode.
	UART			2	Universal Asynchronous Receiver/Transmitter (UART) mode.
31	ENABLED	RW	R	0	SCB block is enabled ('1') or not ('0'). The proper order in which to initialize SCB is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL registers. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL register to enable SCB, select the specific operation mode and oversampling factor. When this block is enabled, no control information should be changed. Changes should be made AFTER disabling this block, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the block is re-enabled. Note that disabling the block will cause re-initialization of the design and associated state is lost (e.g. FIFO content).

12.1.2 SCB_STATUS

Description: Generic status register.
Address: 0x40240004
Offset: 0x4
Retention: Not Retained
IsDeepSleep: Yes
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							EC_BUSY [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	EC_BUSY	R	W	Undefined	Indicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic.

12.1.3 SCB_CMD_RESP_CTRL

Description: Command/response control register.
Address: 0x40240008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			BASE_RD_ADDR [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			BASE_WR_ADDR [20:16]				

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	BASE_RD_ADDR	RW	R	0	I2C/SPI read base address for CMD_RESP mode. At the start of a read transfer this BASE_RD_ADDR is copied to CMD_RESP_STATUS.CURR_RD_ADDR. This field should not be modified during ongoing bus transfers.
16:20	BASE_WR_ADDR	RW	R	0	I2C/SPI write base address for CMD_RESP mode. At the start of a write transfer this BASE_WR_ADDR is copied to CMD_RESP_STATUS.CURR_WR_ADDR. This field should not be modified during ongoing bus transfers.

12.1.4 SCB_CMD_RESP_STATUS

Description: Command/response status register.
Address: 0x4024000C
Offset: 0xC
Retention: Not Retained
IsDeepSleep: Yes
Comment: The register fields reflect register states without a default/reset value (CURR_RD_ADDR and CURR_WR_ADDR) or reflect an external bus state. Therefore, these registers are undefined after the IP is enabled.
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CURR_RD_ADDR [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:21]			CURR_WR_ADDR [20:16]				

Bits	31	30	29	28	27	26	25	24
Name	CMD_RESP_EC_BUSY [31:31]	CMD_RESP_EC_BUS_BUSY [30:30]	None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	CURR_RD_ADDR	R	W	Undefined	I2C/SPI read current address for CMD_RESP mode. HW increments the field after a read access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximum memory buffer address). The field is used to determine how many bytes have been read (# bytes = CURR_RD_ADDR - CMD_RESP_CTRL.BASE_RD_ADDR). This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e. when CMD_RESP_EC_BUSY is '0', the field is reliable.
16:20	CURR_WR_ADDR	R	W	Undefined	I2C/SPI write current address for CMD_RESP mode. HW increments the field after a write access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximum memory buffer address). The field is used to determine how many bytes have been written (# bytes = CURR_WR_ADDR - CMD_RESP_CTRL.BASE_WR_ADDR). This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e. when CMD_RESP_EC_BUSY is '0', the field is reliable.

Bits	Name	SW	HW	Default or Enum	Description
30	CMD_RESP_EC_BUS_BUSY	R	W	Undefined	Indicates whether there is an ongoing bus transfer to the IP. '0': no ongoing bus transfer. '1': ongoing bus transfer. For SPI, the field is '1' when slave mode is selected. For I2C, the field is set to '1' at a I2C START/RESTART. In case of an address match, the field is set to '0' on a I2C STOP. In case of NO address match, the field is set to '0' after the failing address match.
31	CMD_RESP_EC_BUSY	R	W	Undefined	Indicates whether the CURR_RD_ADDR and CURR_WR_ADDR fields in this register are reliable (when CMD_RESP_EC_BUSY is '0') or not reliable (when CMD_RESP_EC_BUSY is '1'). Note: - When there is no ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable). - When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable), when the CURR_RD_ADDR and CURR_WR_ADDR are not being updated by the HW. - When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '1' (not reliable), when the CURR_RD_ADDR or CURR_WR_ADDR are being updated by the HW. Note that this update lasts one I2C clock cycle, or two SPI clock cycles.

12.1.5 SCB_SPI_CTRL

Description: SPI control register.
Address: 0x40240020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		SCLK_CONTINUOUS [5:5]	LATE_MISO_SAMPLE [4:4]	CPOL [3:3]	CPHA [2:2]	SELECT_PRECEDE [1:1]	CONTINUOUS [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				SSEL_POLARITY3 [11:11]	SSEL_POLARITY2 [10:10]	SSEL_POLARITY1 [9:9]	SSEL_POLARITY0 [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:17]							LOOPBACK [16:16]

Bits	31	30	29	28	27	26	25	24
Name	MASTER_MODE [31:31]	None [30:28]			SLAVE_SELECT [27:26]		MODE [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	CONTINUOUS	RW	R	0	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled individual data frame transfers are not necessarily separated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always separated by slave deselection: independent of the availability of TX FIFO data frames, data frames are sent out with slave deselection.
1	SELECT_PRECEDE	RW	R	0	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the Slave SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the Slave SELECT line that coincides with the transfer of the first data frame bit.

Bits	Name	SW	HW	Default or Enum	Description
2	CPHA	RW	R	0	Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is '0', CPHA is '0': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is '0', CPHA is '1': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is '1', CPHA is '0': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is '1', CPHA is '1': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK.
3	CPOL	RW	R	0	Indicates the clock polarity. Only used in SPI Motorola submode. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is '0': SCLK is '0' when not transmitting data. - CPOL is '1': SCLK is '1' when not transmitting data.
4	LATE_MISO_SAMPLE	RW	R	0	Changes the SCLK edge on which MISO is captured. Only used in master mode. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master.
5	SCLK_CONTINUOUS	RW	R	0	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality.
8	SSEL_POLARITY0	RW	R	0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). only SPI_SELECT[0] is used in slave mode. For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Instruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse.
9	SSEL_POLARITY1	RW	R	0	Slave select polarity. SSEL_POLARITY1 applies to the outgoing SPI slave select signal 1 (master mode).
10	SSEL_POLARITY2	RW	R	0	Slave select polarity. SSEL_POLARITY2 applies to the outgoing SPI slave select signal 2 (master mode).
11	SSEL_POLARITY3	RW	R	0	Slave select polarity. SSEL_POLARITY3 applies to the outgoing SPI slave select signal 3 (master mode).

Bits	Name	SW	HW	Default or Enum	Description
16	LOOPBACK	RW	R	0	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': No local loopback '1': the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loopback mode the SPI master receives on MISO what it transmits on MOSI.
24:25	MODE	RW	R	3	Submode of SPI operation (3: Reserved).
	SPI_MOTOROLA			0	SPI Motorola submode. In master mode, when not transmitting data (Slave SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.
	SPI_TI			1	SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive; i.e. no pulse is generated.
	SPI_NS			2	SPI National Semiconductors submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.
26:27	SLAVE_SELECT	RW	R	0	Selects one of the four outgoing SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. SCB block should be disabled when changes are made to this field.
31	MASTER_MODE	RW	R	0	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full.

12.1.6 SCB_SPI_STATUS

Description: SPI status register.
Address: 0x40240024
Offset: 0x24
Retention: Not Retained
IsDeepSleep: Yes
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						SPI_EC_BUSY [1:1]	BUS_BUSY [0:0]

Bits	15	14	13	12	11	10	9	8
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	BUS_BUSY	R	W	Undefined	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection (low active) is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted.
1	SPI_EC_BUSY	R	W	Undefined	Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable.
8:15	CURR_EZ_ADDR	R	W	Undefined	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design.
16:23	BASE_EZ_ADDR	R	W	Undefined	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design.

12.1.7 SCB_UART_CTRL

Description: UART control register.
Address: 0x40240040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:17]							LOOPBACK [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:26]						MODE [25:24]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
16	LOOPBACK	RW	R	0	Local loopback control (does NOT affect the information on the pins). 0: Loopback is not enabled 1: UART_TX is connected to UART_RX. UART_RTS is connected to UART_CTS. This allows a SCB UART transmitter to communicate with its receiver counterpart.
24:25	MODE	RW	R	3	Submode of UART operation (3: Reserved)
	UART_STD			0	Standard UART submode.
	UART_SMARTCARD			1	SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side.
	UART_IRDA			2	Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS should be set to 15.

12.1.8 SCB_UART_TX_CTRL

Description: UART transmitter control register.
Address: 0x40240044
Offset: 0x44
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x2

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		PARITY_ENABLED [5:5]	PARITY [4:4]	None [3:3]	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							RETRY_ON_NACK [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	STOP_BITS	RW	R	2	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period.
4	PARITY	RW	R	0	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes.
5	PARITY_ENABLED	RW	R	0	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware
8	RETRY_ON_NACK	RW	R	0	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode.

12.1.9 SCB_UART_RX_CTRL

Description: UART receiver control register.
Address: 0x40240048
Offset: 0x48
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xA0002

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	POLARITY [6:6]	PARITY _ENABLED [5:5]	PARITY [4:4]	None [3:3]	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		SKIP _START [13:13]	LIN_MODE [12:12]	None [11:11]	MP_MODE [10:10]	DROP_ON _FRAME _ERROR [9:9]	DROP_ON _PARITY _ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	STOP_BITS	RW	R	2	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle ('1') time between data frames and the data frame value.
4	PARITY	RW	R	0	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes.
5	PARITY_ENABLED	RW	R	0	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware.
6	POLARITY	RW	R	0	Inverts incoming RX line signal. Inversion is after local loopback. This functionality is intended for IrDA receiver functionality.

Bits	Name	SW	HW	Default or Enum	Description
8	DROP_ON_PARITY_ERROR	RW	R	0	Behavior when a parity check fails. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field).
9	DROP_ON_FRAME_ERROR	RW	R	0	Behavior when an error is detected in a start or stop period. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost.
10	MP_MODE	RW	R	0	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame separates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped.
12	LIN_MODE	RW	R	0	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minimum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte.
13	SKIP_START	RW	R	0	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit.

Bits	Name	SW	HW	Default or Enum	Description
16:19	BREAK_WIDTH	RW	R	10	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ('break field' detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value.

12.1.10 SCB_UART_RX_STATUS

Description: UART receiver status register.
Address: 0x4024004C
Offset: 0x4C
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:11	BR_COUNTER	R	W	Undefined	Amount of SCB clock periods that constitute the transmission of a 0x55 data frame (sent least significant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of SCB clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'.

12.1.11 SCB_I2C_CTRL

Description: I2C control register.
Address: 0x40240060
Offset: 0x60
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFB88

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	S_NOT_READY_DATA_NACK [15:15]	S_NOT_READY_ADDR_NACK [14:14]	S_READY_DATA_ACK [13:13]	S_READY_ADDR_ACK [12:12]	S_GENERAL_IGNORE [11:11]	None [10:10]	M_NOT_READY_DATA_NACK [9:9]	M_READY_DATA_ACK [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:17]							LOOPBACK [16:16]

Bits	31	30	29	28	27	26	25	24
Name	MASTER_MODE [31:31]	SLAVE_MODE [30:30]	None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	HIGH_PHASE_OVS	RW	R	8	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 SCB clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 SCB clock cycles and <= 16 SCB clock cycles. Without input signal median filtering, the IF high time should be >= 5 SCB clock cycles and <= 16 SCB clock cycles.
4:7	LOW_PHASE_OVS	RW	R	8	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 SCB clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular (no stretching) interface (IF) low time to guarantee functionally correct behavior. With input signal median filtering, the IF low time should be >= 8 SCB clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 SCB clock cycles and <= 16 SCB clock cycles.

Bits	Name	SW	HW	Default or Enum	Description
8	M_READY_DATA_ACK	RW	R	1	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full.
9	M_NOT_READY_DATA_NACK	RW	R	1	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full).
11	S_GENERAL_IGNORE	RW	R	1	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure.
12	S_READY_ADDR_ACK	RW	R	1	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'.
13	S_READY_DATA_ACK	RW	R	1	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'.
14	S_NOT_READY_ADDR_NACK	RW	R	1	This field is used during an address match or general call address in internally clocked mode Only used when: - EC_AM_MODE is '0', EC_OP_MODE is '0', S_GENERAL_IGNORE is '0] and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the SCB clock is available (in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2).SCB clock is not present (in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the SCB clock is available). The logic will handle the ongoing transfer as soon as the clock is enabled.
15	S_NOT_READY_DATA_NACK	RW	R	1	Only used when: - non EZ mode Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full).

Bits	Name	SW	HW	Default or Enum	Description
16	LOOPBACK	RW	R	0	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', no loopback When '1', loopback is enabled internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself.
30	SLAVE_MODE	RW	R	0	Slave mode enabled ('1') or not ('0').
31	MASTER_MODE	RW	R	0	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself.

12.1.12 SCB_I2C_STATUS

Description: I2C status register.
Address: 0x40240064
Offset: 0x64
Retention: Not Retained
IsDeepSleep: Yes
Comment:
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		M_READ [5:5]	S_READ [4:4]	None [3:2]		I2C_EC_BUSY [1:1]	BUS_BUSY [0:0]

Bits	15	14	13	12	11	10	9	8
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	BUS_BUSY	R	W	0	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If SCB block is disabled, BUS_BUSY is '0'. After enabling the block, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions).
1	I2C_EC_BUSY	R	W	Undefined	Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_EZ_ADDR or CURR_EZ_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_EZ_ADDR and CURR_EZ_ADDR are reliable.
4	S_READ	R	W	0	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0".
5	M_READ	R	W	0	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0".

Bits	Name	SW	HW	Default or Enum	Description
8:15	CURR_EZ_ADDR	R	W	Undefined	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design.
16:23	BASE_EZ_ADDR	R	W	Undefined	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design.

12.1.13 SCB_I2C_M_CMD

Description: I2C master command register.
Address: 0x40240068
Offset: 0x68
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			M_STOP [4:4]	M_NACK [3:3]	M_ACK [2:2]	M_START_ON_IDLE [1:1]	M_START [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	M_START	RW	RW1C	0	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'.
1	M_START_ON_IDLE	RW	RW1C	0	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'.
2	M_ACK	RW	RW1C	0	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'.
3	M_NACK	RW	RW1C	0	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'.

Bits	Name	SW	HW	Default or Enum	Description
4	M_STOP	RW	RW1C	0	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. I2C_M_CMD.M_START has a higher priority than this command: in situations where both a STOP and a REPEATED START could be transmitted, M_START takes precedence over M_STOP.

12.1.14 SCB_I2C_S_CMD

Description: I2C slave command register.
Address: 0x4024006C
Offset: 0x6C
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						S_NACK [1:1]	S_ACK [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	S_ACK	RW	RW1C	0	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode).
1	S_NACK	RW	RW1C	0	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK.

12.1.15 SCB_I2C_CFG

Description: I2C configuration register.
Address: 0x40240070
Offset: 0x70
Retention: Retained
IsDeepSleep: No
Comment: The filters are used to remove glitches and to guarantee I2C compliant SCL and SDA setup and hold times. The filters are trimmable.
Default: 0x2A1013

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			SDA_IN_FILT_SEL [4:4]	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			SCL_IN_FILT_SEL [12:12]	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	SDA_IN_FILT_TRIM	RW	R	3	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required
4	SDA_IN_FILT_SEL	RW	R	1	Enable for 50ns glitch filter on SDA input '0': 0 ns. '1: 50 ns (filter enabled).
8:9	SCL_IN_FILT_TRIM	RW	R	0	Trim settings for the 50ns glitch filter on the SCL input. Default setting meets the I2C glitch rejections specs. Programmability available if required
12	SCL_IN_FILT_SEL	RW	R	1	Enable for 50ns glitch filter on SCL input '0': 0 ns. '1: 50 ns (filter enabled).
16:17	SDA_OUT_FILT0_TRIM	RW	R	2	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required
18:19	SDA_OUT_FILT1_TRIM	RW	R	2	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required
20:21	SDA_OUT_FILT2_TRIM	RW	R	2	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required

Bits	Name	SW	HW	Default or Enum	Description
28:29	SDA_OUT_FILT_SEL	RW	R	0	Selection of cumulative filter delay on SDA output to meet tHD_DAT parameter '0': 0 ns. '1': 50 ns (filter 0 enabled). '2': 100 ns (filters 0 and 1 enabled). '3': 150 ns (filters 0, 1 and 2 enabled).

12.1.16 SCB_TX_CTRL

Description: Transmitter control register.
Address: 0x40240200
Offset: 0x200
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x107

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							MSB _FIRST [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	DATA_WIDTH	RW	R	7	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7.
8	MSB_FIRST	RW	R	1	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'.

12.1.17 SCB_TX_FIFO_CTRL

Description: Transmitter FIFO control register.
Address: 0x40240204
Offset: 0x204
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						FREEZE [17:17]	CLEAR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	TRIGGER_LEVEL	RW	R	0	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event INTR_TX.TRIGGER is generated.
16	CLEAR	RW	R	0	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period.
17	FREEZE	RW	R	0	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer.

12.1.18 SCB_TX_FIFO_STATUS

Description: Transmitter FIFO status register.
Address: 0x40240208
Offset: 0x208
Retention: Not Retained
IsDeepSleep: No
Comment: This register is not used in EZ and CMD_RESP modes.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	SR_VALID [15:15]	None [14:8]						

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:28]				WR_PTR [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	USED	R	W	0	Amount of entries in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2).
15	SR_VALID	R	W	0	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is transmitted next (when the protocol state machine is not transmitting a data frame).
16:19	RD_PTR	R	W	0	FIFO read pointer: FIFO location from which a data frame is read by the hardware.
24:27	WR_PTR	R	W	0	FIFO write pointer: FIFO location at which a new data frame is written.

12.1.19 SCB_TX_FIFO_WR

Description: Transmitter FIFO write register.
Address: 0x40240240
Offset: 0x240
Retention: Not Retained
IsDeepSleep: No
Comment: When the IP is disabled (CTRL.ENABLED is '0') or when the TX FIFO is full, a write to this register is dropped. This register should only be used in FIFO mode (and not in EZ or CMD_RESP modes). This register is 'write only'; a read from this register returns '0'.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	DATA	W	R	0	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'.

12.1.20 SCB_RX_CTRL

Description: Receiver control register.
Address: 0x40240300
Offset: 0x300
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x107

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						MEDIAN [9:9]	MSB _FIRST [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	DATA_WIDTH	RW	R	7	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7.
8	MSB_FIRST	RW	R	1	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'.
9	MEDIAN	RW	R	0	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptibility to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'.

12.1.21 SCB_RX_FIFO_CTRL

Description: Receiver FIFO control register.
Address: 0x40240304
Offset: 0x304
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:18]						FREEZE [17:17]	CLEAR [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	TRIGGER_LEVEL	RW	R	0	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event INTR_RX.TRIGGER is generated.
16	CLEAR	RW	R	0	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period.
17	FREEZE	RW	R	0	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer.

12.1.22 SCB_RX_FIFO_STATUS

Description: Receiver FIFO status register.
Address: 0x40240308
Offset: 0x308
Retention: Not Retained
IsDeepSleep: No
Comment: This register is not used in EZ and CMD_RESP modes.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	SR_VALID [15:15]	None [14:8]						

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:28]				WR_PTR [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	USED	R	W	0	Amount of entries in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2).
15	SR_VALID	R	W	0	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame).
16:19	RD_PTR	R	W	0	FIFO read pointer: FIFO location from which a data frame is read.
24:27	WR_PTR	R	W	0	FIFO write pointer: FIFO location at which a new data frame is written by the hardware.

12.1.23 SCB_RX_MATCH

Description: Slave address and mask register.
Address: 0x40240310
Offset: 0x310
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	ADDR	RW	R	0	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read).
16:23	MASK	RW	R	0	Slave device address mask. This field is a mask that specifies which of the slave address bits take part in the matching. MATCH = ((ADDR & MASK) == ('slave address' & MASK)).

12.1.24 SCB_RX_FIFO_RD

Description: Receiver FIFO read register.
Address: 0x40240340
Offset: 0x340
Retention: Not Retained
IsDeepSleep: No
Comment: When the IP is disabled (CTRL.ENABLED is '0') or when the RX FIFO is empty, a read from this register returns 0xffff:ffff. This register should only be used in FIFO mode (and not in EZ or CMD_RESP modes). This register is 'read only'; a write to this register is ignored.
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	DATA	R	W	Undefined	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. When this register is read through the debugger, the data frame will not be removed from the FIFO. Similar in operation to RX_FIFO_RD_SILENT

12.1.25 SCB_RX_FIFO_RD_SILENT

Description: Receiver FIFO read register.
Address: 0x40240344
Offset: 0x344
Retention: Not Retained
IsDeepSleep: No
Comment: When the IP is disabled (CTRL.ENABLED is '0') or when the RX FIFO is empty, a read from this register returns 0xffff:ffff. This register should only be used in FIFO mode (and not in EZ or CMD_RESP modes).
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	DATA	R	W	Undefined	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'.

12.1.26 SCB_EZ_DATA

Description: Memory buffer registers.
Address: 0x40240400
Offset: 0x400
Retention: Retained
IsDeepSleep: Yes
Comment: When the IP is disabled (CTRL.ENABLED is '0'), a read from these registers return 0xffff:ffff. It is under MMIO register control whether accesses to this register should introduce bus wait states or be discarded when the externally clocked logic is accessing the memory structure. These registers should only be used in EZ and CMD_RESP modes (and not in FIFO mode).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	EZ_DATA	RW	RW	Undefined	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value.

12.1.27 SCB_INTR_CAUSE

Description: Active clocked interrupt signal register
Address: 0x40240E00
Offset: 0xE00
Retention: Retained
IsDeepSleep: Yes
Comment: Enables software to determine the source of the combined interrupt output signals 'interrupt_ic', 'interrupt_ec' and 'interrupt'.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		SPI_EC [5:5]	I2C_EC [4:4]	RX [3:3]	TX [2:2]	S [1:1]	M [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	M	R	W	0	Master interrupt active ('interrupt_master'): INTR_M_MASKED != 0.
1	S	R	W	0	Slave interrupt active ('interrupt_slave'): INTR_S_MASKED != 0.
2	TX	R	W	0	Transmitter interrupt active ('interrupt_tx'): INTR_TX_MASKED != 0.
3	RX	R	W	0	Receiver interrupt active ('interrupt_rx'): INTR_RX_MASKED != 0.
4	I2C_EC	R	W	0	Externally clock I2C interrupt active ('interrupt_i2c_ec'): INTR_I2C_EC_MASKED != 0.
5	SPI_EC	R	W	0	Externally clocked SPI interrupt active ('interrupt_spi_ec'): INTR_SPI_EC_MASKED != 0.

12.1.28 SCB_INTR_I2C_EC

Description: Externally clocked I2C interrupt request register
Address: 0x40240E80
Offset: 0xE80
Retention: Retained
IsDeepSleep: Yes
Comment: The fields in this register are set by HW and are cleared by software by writing a '1'. These interrupt causes are generated by externally clocked logic. HW clears the interrupt causes to '0', when the IP is disabled.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				EZ_READ_STOP [3:3]	EZ_WRITE_STOP [2:2]	EZ_STOP [1:1]	WAKE_UP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKE_UP	RW1C	A	0	Wake up request. Active on incoming slave request (with address match). Only used when CTRL.EC_AM_MODE is '1'.
1	EZ_STOP	RW1C	A	0	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'.
2	EZ_WRITE_STOP	RW1C	A	0	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'.
3	EZ_READ_STOP	RW1C	A	0	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'.

12.1.29 SCB_INTR_I2C_EC_MASK

Description: Externally clocked I2C interrupt mask register
Address: 0x40240E88
Offset: 0xE88
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				EZ_READ_STOP [3:3]	EZ_WRITE_STOP [2:2]	EZ_STOP [1:1]	WAKE_UP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKE_UP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
1	EZ_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
2	EZ_WRITE_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
3	EZ_READ_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.

12.1.30 SCB_INTR_I2C_EC_MASKED

Description: Externally clocked I2C interrupt masked register
Address: 0x40240E8C
Offset: 0xE8C
Retention: Retained
IsDeepSleep: Yes
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_I2C_EC_MASKED != 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				EZ_READ_STOP [3:3]	EZ_WRITE_STOP [2:2]	EZ_STOP [1:1]	WAKE_UP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKE_UP	R	W	0	Logical and of corresponding request and mask bits.
1	EZ_STOP	R	W	0	Logical and of corresponding request and mask bits.
2	EZ_WRITE_STOP	R	W	0	Logical and of corresponding request and mask bits.
3	EZ_READ_STOP	R	W	0	Logical and of corresponding request and mask bits.

12.1.31 SCB_INTR_SPI_EC

Description: Externally clocked SPI interrupt request register
Address: 0x40240EC0
Offset: 0xEC0
Retention: Retained
IsDeepSleep: Yes
Comment: The fields in this register are set by HW and are cleared by software by writing a '1'. These interrupt causes are generated by externally clocked logic. HW clears the interrupt causes to '0', when the IP is disabled.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				EZ_READ_STOP [3:3]	EZ_WRITE_STOP [2:2]	EZ_STOP [1:1]	WAKE_UP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKE_UP	RW1C	A	0	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when CTRL.EC_AM_MODE is '1'.
1	EZ_STOP	RW1C	A	0	STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when CTRL.EC_OP_MODE is '1'.
2	EZ_WRITE_STOP	RW1C	A	0	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI deselection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'.
3	EZ_READ_STOP	RW1C	A	0	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI deselection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'.

12.1.32 SCB_INTR_SPI_EC_MASK

Description: Externally clocked SPI interrupt mask register
Address: 0x40240EC8
Offset: 0xEC8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				EZ_READ_STOP [3:3]	EZ_WRITE_STOP [2:2]	EZ_STOP [1:1]	WAKE_UP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKE_UP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
1	EZ_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
2	EZ_WRITE_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
3	EZ_READ_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.

12.1.33 SCB_INTR_SPI_EC_MASKED

Description: Externally clocked SPI interrupt masked register
Address: 0x40240ECC
Offset: 0xECC
Retention: Retained
IsDeepSleep: Yes
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_SPI_EC_MASKED != 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				EZ_READ_STOP [3:3]	EZ_WRITE_STOP [2:2]	EZ_STOP [1:1]	WAKE_UP [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WAKE_UP	R	W	0	Logical and of corresponding request and mask bits.
1	EZ_STOP	R	W	0	Logical and of corresponding request and mask bits.
2	EZ_WRITE_STOP	R	W	0	Logical and of corresponding request and mask bits.
3	EZ_READ_STOP	R	W	0	Logical and of corresponding request and mask bits.

12.1.34 SCB_INTR_M

Description: Master interrupt request register.
Address: 0x40240F00
Offset: 0xF00
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained In DeepSleep power mode: HW clears the interrupt causes to '0', when coming out of DeepSleep power mode. In addition, HW clears the interrupt causes to '0', when the IP is disabled. As a result, the interrupt causes are only available in Active/Sleep power modes; they are generated by internally clocked logic (this logic operates on a clock that is only available in Active/Sleep power modes).

The interrupt causes should only be used for internally clocked operation; i.e. EC_OP is '0'.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			I2C_STOP [4:4]	None [3:3]	I2C_ACK [2:2]	I2C_NACK [1:1]	I2C_ARB_LOST [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						SPI_DONE [9:9]	I2C_BUS_ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	I2C_ARB_LOST	RW1C	RW1S	0	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line.
1	I2C_NACK	RW1C	RW1S	0	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data).
2	I2C_ACK	RW1C	RW1S	0	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data).
4	I2C_STOP	RW1C	RW1S	0	I2C master STOP. Set to '1', when the master has transmitted a STOP.
8	I2C_BUS_ERROR	RW1C	RW1S	0	I2C master bus error (unexpected detection of START or STOP condition).
9	SPI_DONE	RW1C	RW1S	0	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO and shift register are empty.

12.1.35 SCB_INTR_M_SET

Description: Master interrupt set request register
Address: 0x40240F04
Offset: 0xF04
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			I2C_STOP [4:4]	None [3:3]	I2C_ACK [2:2]	I2C_NACK [1:1]	I2C_ARB_LOST [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						SPI_DONE [9:9]	I2C_BUS_ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	I2C_ARB_LOST	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
1	I2C_NACK	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
2	I2C_ACK	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
4	I2C_STOP	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
8	I2C_BUS_ERROR	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
9	SPI_DONE	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.

12.1.36 SCB_INTR_M_MASK

Description: Master interrupt mask register.
Address: 0x40240F08
Offset: 0xF08
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			I2C_STOP [4:4]	None [3:3]	I2C_ACK [2:2]	I2C_NACK [1:1]	I2C_ARB_LOST [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						SPI_DONE [9:9]	I2C_BUS_ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	I2C_ARB_LOST	RW	R	0	Mask bit for corresponding bit in interrupt request register.
1	I2C_NACK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
2	I2C_ACK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
4	I2C_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
8	I2C_BUS_ERROR	RW	R	0	Mask bit for corresponding bit in interrupt request register.
9	SPI_DONE	RW	R	0	Mask bit for corresponding bit in interrupt request register.

12.1.37 SCB_INTR_M_MASKED

Description: Master interrupt masked request register
Address: 0x40240F0C
Offset: 0xF0C
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_M_MASKED != 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			I2C_STOP [4:4]	None [3:3]	I2C_ACK [2:2]	I2C_NACK [1:1]	I2C_ARB_LOST [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						SPI_DONE [9:9]	I2C_BUS_ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	I2C_ARB_LOST	R	W	0	Logical and of corresponding request and mask bits.
1	I2C_NACK	R	W	0	Logical and of corresponding request and mask bits.
2	I2C_ACK	R	W	0	Logical and of corresponding request and mask bits.
4	I2C_STOP	R	W	0	Logical and of corresponding request and mask bits.
8	I2C_BUS_ERROR	R	W	0	Logical and of corresponding request and mask bits.
9	SPI_DONE	R	W	0	Logical and of corresponding request and mask bits.

12.1.38 SCB_INTR_S

Description: Slave interrupt request register.
Address: 0x40240F40
Offset: 0xF40
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained In DeepSleep power mode: HW clears the interrupt causes to '0', when coming out of DeepSleep power mode. In addition, HW clears the interrupt causes to '0', when the IP is disabled. As a result, the interrupt causes are only available in Active/Sleep power modes; they are generated by internally clocked logic (this logic operates on a clock that is only available in Active/Sleep power modes).

The interrupt causes should only be used for internally clocked operation; i.e. EC_OP is '0'.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	I2C_GENERAL [7:7]	I2C_ADDR_MATCH [6:6]	I2C_START [5:5]	I2C_STOP [4:4]	I2C_WRITE_STOP [3:3]	I2C_ACK [2:2]	I2C_NACK [1:1]	I2C_ARB_LOST [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				SPI_BUS_ERROR [11:11]	SPI_EZ_STOP [10:10]	SPI_EZ_WRITE_STOP [9:9]	I2C_BUS_ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	I2C_ARB_LOST	RW1C	RW1S	0	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine aborts the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error.
1	I2C_NACK	RW1C	RW1S	0	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data).
2	I2C_ACK	RW1C	RW1S	0	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data).

Bits	Name	SW	HW	Default or Enum	Description
3	I2C_WRITE_STOP	RW1C	RW1S	0	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected).
4	I2C_STOP	RW1C	RW1S	0	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd.
5	I2C_START	RW1C	RW1S	0	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL.
6	I2C_ADDR_MATCH	RW1C	RW1S	0	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected.
7	I2C_GENERAL	RW1C	RW1S	0	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected.

Bits	Name	SW	HW	Default or Enum	Description
8	I2C_BUS_ERROR	RW1C	RW1S	0	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error.
9	SPI_EZ_WRITE_STOP	RW1C	RW1S	0	SPI slave deselected after a write EZ SPI transfer occurred.
10	SPI_EZ_STOP	RW1C	RW1S	0	SPI slave deselected after any EZ SPI transfer occurred.
11	SPI_BUS_ERROR	RW1C	RW1S	0	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error.

12.1.39 SCB_INTR_S_SET

Description: Slave interrupt set request register.
Address: 0x40240F44
Offset: 0xF44
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	I2C_GENERAL [7:7]	I2C_ADDR_MATCH [6:6]	I2C_START [5:5]	I2C_STOP [4:4]	I2C_WRITE_STOP [3:3]	I2C_ACK [2:2]	I2C_NACK [1:1]	I2C_ARB_LOST [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				SPI_BUS_ERROR [11:11]	SPI_EZ_STOP [10:10]	SPI_EZ_WRITE_STOP [9:9]	I2C_BUS_ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	I2C_ARB_LOST	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
1	I2C_NACK	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
2	I2C_ACK	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
3	I2C_WRITE_STOP	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
4	I2C_STOP	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
5	I2C_START	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
6	I2C_ADDR_MATCH	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
7	I2C_GENERAL	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
8	I2C_BUS_ERROR	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
9	SPI_EZ_WRITE_STOP	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
10	SPI_EZ_STOP	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
11	SPI_BUS_ERROR	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.

12.1.40 SCB_INTR_S_MASK

Description: Slave interrupt mask register.
Address: 0x40240F48
Offset: 0xF48
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	I2C_GENERAL [7:7]	I2C_ADDR_MATCH [6:6]	I2C_START [5:5]	I2C_STOP [4:4]	I2C_WRITE_STOP [3:3]	I2C_ACK [2:2]	I2C_NACK [1:1]	I2C_ARB_LOST [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				SPI_BUS_ERROR [11:11]	SPI_EZ_STOP [10:10]	SPI_EZ_WRITE_STOP [9:9]	I2C_BUS_ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	I2C_ARB_LOST	RW	R	0	Mask bit for corresponding bit in interrupt request register.
1	I2C_NACK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
2	I2C_ACK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
3	I2C_WRITE_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
4	I2C_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
5	I2C_START	RW	R	0	Mask bit for corresponding bit in interrupt request register.
6	I2C_ADDR_MATCH	RW	R	0	Mask bit for corresponding bit in interrupt request register.
7	I2C_GENERAL	RW	R	0	Mask bit for corresponding bit in interrupt request register.
8	I2C_BUS_ERROR	RW	R	0	Mask bit for corresponding bit in interrupt request register.
9	SPI_EZ_WRITE_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
10	SPI_EZ_STOP	RW	R	0	Mask bit for corresponding bit in interrupt request register.
11	SPI_BUS_ERROR	RW	R	0	Mask bit for corresponding bit in interrupt request register.

12.1.41 SCB_INTR_S_MASKED

Description: Slave interrupt masked request register
Address: 0x40240F4C
Offset: 0xF4C
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_S_MASKED != 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	I2C_GENERAL [7:7]	I2C_ADDR_MATCH [6:6]	I2C_START [5:5]	I2C_STOP [4:4]	I2C_WRITE_STOP [3:3]	I2C_ACK [2:2]	I2C_NACK [1:1]	I2C_ARB_LOST [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				SPI_BUS_ERROR [11:11]	SPI_EZ_STOP [10:10]	SPI_EZ_WRITE_STOP [9:9]	I2C_BUS_ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	I2C_ARB_LOST	R	W	0	Logical and of corresponding request and mask bits.
1	I2C_NACK	R	W	0	Logical and of corresponding request and mask bits.
2	I2C_ACK	R	W	0	Logical and of corresponding request and mask bits.
3	I2C_WRITE_STOP	R	W	0	Logical and of corresponding request and mask bits.
4	I2C_STOP	R	W	0	Logical and of corresponding request and mask bits.
5	I2C_START	R	W	0	Logical and of corresponding request and mask bits.
6	I2C_ADDR_MATCH	R	W	0	Logical and of corresponding request and mask bits.
7	I2C_GENERAL	R	W	0	Logical and of corresponding request and mask bits.
8	I2C_BUS_ERROR	R	W	0	Logical and of corresponding request and mask bits.
9	SPI_EZ_WRITE_STOP	R	W	0	Logical and of corresponding request and mask bits.
10	SPI_EZ_STOP	R	W	0	Logical and of corresponding request and mask bits.
11	SPI_BUS_ERROR	R	W	0	Logical and of corresponding request and mask bits.

12.1.42 SCB_INTR_TX

Description: Transmitter interrupt request register.
Address: 0x40240F80
Offset: 0xF80
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained In DeepSleep power mode: HW clears the interrupt causes to '0', when coming out of DeepSleep power mode. In addition, HW clears the interrupt causes to '0', when the IP is disabled. As a result, the interrupt causes are only available in Active/Sleep power modes; they are generated by internally clocked logic (this logic operates on a clock that is only available in Active/Sleep power modes).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BLOCKED [7:7]	UNDERFLOW [6:6]	OVERFLOW [5:5]	EMPTY [4:4]	None [3:2]		NOT_FULL [1:1]	TRIGGER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:11]					UART_ARB_LOST [10:10]	UART_DONE [9:9]	UART_NACK [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TRIGGER	RW1C	RW1S	0	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL. Only used in FIFO mode.
1	NOT_FULL	RW1C	RW1S	0	TX FIFO is not full. Dependent on CTRL.BYTE_MODE: (FF_DATA_NR = EZ_DATA_NR/2) BYTE_MODE is '0': # entries != FF_DATA_NR/2. BYTE_MODE is '1': # entries != FF_DATA_NR. Only used in FIFO mode.
4	EMPTY	RW1C	RW1S	0	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode.
5	OVERFLOW	RW1C	RW1S	0	Attempt to write to a full TX FIFO. Only used in FIFO mode.
6	UNDERFLOW	RW1C	RW1S	0	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode.
7	BLOCKED	RW1C	RW1S	0	SW cannot get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'.
8	UART_NACK	RW1C	RW1S	0	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit.

Bits	Name	SW	HW	Default or Enum	Description
9	UART_DONE	RW1C	RW1S	0	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is '1'. Set to '1', when event is detected. Write with '1' to clear bit.
10	UART_ARB_LOST	RW1C	RW1S	0	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is useful when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit.

12.1.43 SCB_INTR_TX_SET

Description: Transmitter interrupt set request register
Address: 0x40240F84
Offset: 0xF84
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BLOCKED [7:7]	UNDERFLOW [6:6]	OVERFLOW [5:5]	EMPTY [4:4]	None [3:2]		NOT_FULL [1:1]	TRIGGER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:11]					UART_ARB_LOST [10:10]	UART_DONE [9:9]	UART_NACK [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TRIGGER	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
1	NOT_FULL	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
4	EMPTY	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
5	OVERFLOW	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
6	UNDERFLOW	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
7	BLOCKED	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
8	UART_NACK	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
9	UART_DONE	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
10	UART_ARB_LOST	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.

12.1.44 SCB_INTR_TX_MASK

Description: Transmitter interrupt mask register.
Address: 0x40240F88
Offset: 0xF88
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BLOCKED [7:7]	UNDERFLOW [6:6]	OVERFLOW [5:5]	EMPTY [4:4]	None [3:2]		NOT_FULL [1:1]	TRIGGER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:11]					UART_ARB_LOST [10:10]	UART_DONE [9:9]	UART_NACK [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TRIGGER	RW	R	0	Mask bit for corresponding bit in interrupt request register.
1	NOT_FULL	RW	R	0	Mask bit for corresponding bit in interrupt request register.
4	EMPTY	RW	R	0	Mask bit for corresponding bit in interrupt request register.
5	OVERFLOW	RW	R	0	Mask bit for corresponding bit in interrupt request register.
6	UNDERFLOW	RW	R	0	Mask bit for corresponding bit in interrupt request register.
7	BLOCKED	RW	R	0	Mask bit for corresponding bit in interrupt request register.
8	UART_NACK	RW	R	0	Mask bit for corresponding bit in interrupt request register.
9	UART_DONE	RW	R	0	Mask bit for corresponding bit in interrupt request register.
10	UART_ARB_LOST	RW	R	0	Mask bit for corresponding bit in interrupt request register.

12.1.45 SCB_INTR_TX_MASKED

Description: Transmitter interrupt masked request register
Address: 0x40240F8C
Offset: 0xF8C
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_TX_MASKED != 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BLOCKED [7:7]	UNDERFLOW [6:6]	OVERFLOW [5:5]	EMPTY [4:4]	None [3:2]		NOT_FULL [1:1]	TRIGGER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:11]					UART_ARB_LOST [10:10]	UART_DONE [9:9]	UART_NACK [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TRIGGER	R	W	0	Logical and of corresponding request and mask bits.
1	NOT_FULL	R	W	0	Logical and of corresponding request and mask bits.
4	EMPTY	R	W	0	Logical and of corresponding request and mask bits.
5	OVERFLOW	R	W	0	Logical and of corresponding request and mask bits.
6	UNDERFLOW	R	W	0	Logical and of corresponding request and mask bits.
7	BLOCKED	R	W	0	Logical and of corresponding request and mask bits.
8	UART_NACK	R	W	0	Logical and of corresponding request and mask bits.
9	UART_DONE	R	W	0	Logical and of corresponding request and mask bits.
10	UART_ARB_LOST	R	W	0	Logical and of corresponding request and mask bits.

12.1.46 SCB_INTR_RX

Description: Receiver interrupt request register.
Address: 0x40240FC0
Offset: 0xFC0
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained In DeepSleep power mode: HW clears the interrupt causes to '0', when coming out of DeepSleep power mode. In addition, HW clears the interrupt causes to '0', when the IP is disabled. As a result, the interrupt causes are only available in Active/Sleep power modes; they are generated by internally clocked logic (this logic operates on a clock that is only available in Active/Sleep power modes).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BLOCKED [7:7]	UNDERFLOW [6:6]	OVERFLOW [5:5]	None [4:4]	FULL [3:3]	NOT _EMPTY [2:2]	None [1:1]	TRIGGER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				BREAK _DETECT [11:11]	BAUD _DETECT [10:10]	PARITY _ERROR [9:9]	FRAME _ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TRIGGER	RW1C	RW1S	0	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FIFO_CTL. Only used in FIFO mode.
2	NOT_EMPTY	RW1C	RW1S	0	RX FIFO is not empty. Only used in FIFO mode.
3	FULL	RW1C	RW1S	0	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.BYTE_MODE: (FF_DATA_NR = EZ_DATA_NR/2) BYTE_MODE is '0': # entries == FF_DATA_NR/2. BYTE_MODE is '1': # entries == FF_DATA_NR. Only used in FIFO mode.
5	OVERFLOW	RW1C	RW1S	0	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode.
6	UNDERFLOW	RW1C	RW1S	0	Attempt to read from an empty RX FIFO. Only used in FIFO mode.
7	BLOCKED	RW1C	RW1S	0	SW cannot get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'.

Bits	Name	SW	HW	Default or Enum	Description
8	FRAME_ERROR	RW1C	RW1S	0	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames.
9	PARITY_ERROR	RW1C	RW1S	0	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO.
10	BAUD_DETECT	RW1C	RW1S	0	LIN baudrate detection is completed. The receiver software uses the UART_RX_STATUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit.
11	BREAK_DETECT	RW1C	RW1S	0	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. 'break-in-data' is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is expected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit.

12.1.47 SCB_INTR_RX_SET

Description: Receiver interrupt set request register.
Address: 0x40240FC4
Offset: 0xFC4
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BLOCKED [7:7]	UNDERFLOW [6:6]	OVERFLOW [5:5]	None [4:4]	FULL [3:3]	NOT _EMPTY [2:2]	None [1:1]	TRIGGER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				BREAK _DETECT [11:11]	BAUD _DETECT [10:10]	PARITY _ERROR [9:9]	FRAME _ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TRIGGER	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
2	NOT_EMPTY	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.
3	FULL	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.
5	OVERFLOW	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.
6	UNDERFLOW	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.
7	BLOCKED	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.
8	FRAME_ERROR	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.
9	PARITY_ERROR	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.
10	BAUD_DETECT	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.
11	BREAK_DETECT	RW1S	A	0	Write with '1' to set corresponding bit in interrupt status register.

12.1.48 SCB_INTR_RX_MASK

Description: Receiver interrupt mask register.
Address: 0x40240FC8
Offset: 0xFC8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BLOCKED [7:7]	UNDERFLOW [6:6]	OVERFLOW [5:5]	None [4:4]	FULL [3:3]	NOT _EMPTY [2:2]	None [1:1]	TRIGGER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				BREAK _DETECT [11:11]	BAUD _DETECT [10:10]	PARITY _ERROR [9:9]	FRAME _ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TRIGGER	RW	R	0	Mask bit for corresponding bit in interrupt request register.
2	NOT_EMPTY	RW	R	0	Mask bit for corresponding bit in interrupt request register.
3	FULL	RW	R	0	Mask bit for corresponding bit in interrupt request register.
5	OVERFLOW	RW	R	0	Mask bit for corresponding bit in interrupt request register.
6	UNDERFLOW	RW	R	0	Mask bit for corresponding bit in interrupt request register.
7	BLOCKED	RW	R	0	Mask bit for corresponding bit in interrupt request register.
8	FRAME_ERROR	RW	R	0	Mask bit for corresponding bit in interrupt request register.
9	PARITY_ERROR	RW	R	0	Mask bit for corresponding bit in interrupt request register.
10	BAUD_DETECT	RW	R	0	Mask bit for corresponding bit in interrupt request register.
11	BREAK_DETECT	RW	R	0	Mask bit for corresponding bit in interrupt request register.

12.1.49 SCB_INTR_RX_MASKED

Description: Receiver interrupt masked request register
Address: 0x40240FCC
Offset: 0xFCC
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_RX_MASKED != 0.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	BLOCKED [7:7]	UNDERFLOW [6:6]	OVERFLOW [5:5]	None [4:4]	FULL [3:3]	NOT _EMPTY [2:2]	None [1:1]	TRIGGER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				BREAK _DETECT [11:11]	BAUD _DETECT [10:10]	PARITY _ERROR [9:9]	FRAME _ERROR [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TRIGGER	R	W	0	Logical and of corresponding request and mask bits.
2	NOT_EMPTY	R	W	0	Logical and of corresponding request and mask bits.
3	FULL	R	W	0	Logical and of corresponding request and mask bits.
5	OVERFLOW	R	W	0	Logical and of corresponding request and mask bits.
6	UNDERFLOW	R	W	0	Logical and of corresponding request and mask bits.
7	BLOCKED	R	W	0	Logical and of corresponding request and mask bits.
8	FRAME_ERROR	R	W	0	Logical and of corresponding request and mask bits.
9	PARITY_ERROR	R	W	0	Logical and of corresponding request and mask bits.
10	BAUD_DETECT	R	W	0	Logical and of corresponding request and mask bits.
11	BREAK_DETECT	R	W	0	Logical and of corresponding request and mask bits.

13 SFLASH

Description Supervisory Flash Area (Infineon Trim & Wounding Info)
Base Address 0xFFFE000
Size 0x800
Slave Num MEMORYMAP

Register Name	Address	Permission	Description
SFLASH_SILICON_ID	0xFFFE000	FULL	Silicon ID
SFLASH_SWD_CONFIG	0xFFFE002	FULL	SWD pinout selector
SFLASH_DPSLP_KEY_DELAY	0xFFFE012	FULL	DeepSleep wakeup value for PWR_KEY_DELAY
SFLASH_SWD_LISTEN	0xFFFE014	FULL	Listen Window Length
SFLASH_FLASH_START	0xFFFE018	FULL	Flash Image Start Address
SFLASH_USER_SFLASH_AREA0	0xFFFE040	FULL	Pointer to between 0 and 2 customer usable SFLASH regions
SFLASH_USER_SFLASH_AREA1	0xFFFE044	FULL	Pointer to between 0 and 2 customer usable SFLASH regions
SFLASH_DIE_UNIQUE_ID0	0xFFFE050	FULL	Uses manufacturing identity to create a unique die ID
SFLASH_DIE_UNIQUE_ID1	0xFFFE054	FULL	Uses manufacturing identity to create a unique die ID
SFLASH_DIE_UNIQUE_ID2	0xFFFE058	FULL	Uses manufacturing identity to create a unique die ID
SFLASH_DIE_UNIQUE_ID3	0xFFFE05C	FULL	Uses manufacturing identity to create a unique die ID
SFLASH_DIE_UNIQUE_ID4	0xFFFE060	FULL	Uses manufacturing identity to create a unique die ID
SFLASH_DIE_UNIQUE_ID5	0xFFFE064	FULL	Uses manufacturing identity to create a unique die ID
SFLASH_IMO_TRIM_LT0	0xFFFE200	FULL	IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TRIM_LT1	0xFFFE201	FULL	IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TRIM_LT2	0xFFFE202	FULL	IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TRIM_LT3	0xFFFE203	FULL	IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TRIM_LT4	0xFFFE204	FULL	IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TRIM_LT5	0xFFFE205	FULL	IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TRIM_LT6	0xFFFE206	FULL	IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TRIM_LT7	0xFFFE207	FULL	IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TCTRIM_LT0	0xFFFE208	FULL	IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TCTRIM_LT1	0xFFFE209	FULL	IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TCTRIM_LT2	0xFFFE20A	FULL	IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TCTRIM_LT3	0xFFFE20B	FULL	IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TCTRIM_LT4	0xFFFE20C	FULL	IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TCTRIM_LT5	0xFFFE20D	FULL	IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TCTRIM_LT6	0xFFFE20E	FULL	IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_TCTRIM_LT7	0xFFFE20F	FULL	IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_STEPSIZE_LT0	0xFFFE210	FULL	IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz

Register Name	Address	Permission	Description
SFLASH_IMO_STEPSIZE_LT1	0xFFFE211	FULL	IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_STEPSIZE_LT2	0xFFFE212	FULL	IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_STEPSIZE_LT3	0xFFFE213	FULL	IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_STEPSIZE_LT4	0xFFFE214	FULL	IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_STEPSIZE_LT5	0xFFFE215	FULL	IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_STEPSIZE_LT6	0xFFFE216	FULL	IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_STEPSIZE_LT7	0xFFFE217	FULL	IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz
SFLASH_IMO_4PCT_LIM	0xFFFE218	FULL	IMO trim 4 percent deviation from nominal
SFLASH_IMO_3PCT_LIM	0xFFFE219	FULL	IMO trim 3 percent deviation from nominal
SFLASH_PILO_6PCT_LIM	0xFFFE21A	FULL	PILO trim 6 percent deviation from nominal
SFLASH_PACSS_CHAN0_2TEMP_TRIM0	0xFFFE280	FULL	Channel 0 two temperature trim values for software lookup. Note:A is not available for this register
SFLASH_PACSS_CHAN0_2TEMP_TRIM1	0xFFFE284	FULL	Channel 0 two temperature trim values for software lookup. Note:B is not available for this register
SFLASH_PACSS_CHAN0_2TEMP_TRIM2	0xFFFE288	FULL	Channel 0 two temperature trim values for software lookup. Note:C is not available for this register
SFLASH_PACSS_CHAN0_2TEMP_TRIM3	0xFFFE28C	FULL	Channel 0 two temperature trim values for software lookup. Note:G is not available for this register
SFLASH_PACSS_CHAN0_2TEMP_TRIM4	0xFFFE290	FULL	Channel 0 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN0_2TEMP_TRIM5	0xFFFE294	FULL	Channel 0 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN0_2TEMP_TRIM6	0xFFFE298	FULL	Channel 0 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN0_2TEMP_TRIM7	0xFFFE29C	FULL	Channel 0 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN0_2TEMP_TRIM8	0xFFFE2A0	FULL	Channel 0 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN0_2TEMP_TRIM9	0xFFFE2A4	FULL	Channel 0 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN0_2TEMP_TRIM10	0xFFFE2A8	FULL	Channel 0 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN0_2TEMP_TRIM11	0xFFFE2AC	FULL	Channel 0 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN0_2TEMP_TRIM12	0xFFFE2B0	FULL	Channel 0 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN0_2TEMP_TRIM13	0xFFFE2B4	FULL	Channel 0 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN0_2TEMP_TRIM14	0xFFFE2B8	FULL	Channel 0 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN0_2TEMP_TRIM15	0xFFFE2BC	FULL	Channel 0 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN0_2TEMP_TRIM16	0xFFFE2C0	FULL	Channel 0 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN0_2TEMP_TRIM17	0xFFFE2C4	FULL	Channel 0 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN0_2TEMP_TRIM18	0xFFFE2C8	FULL	Channel 0 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN0_2TEMP_TRIM19	0xFFFE2CC	FULL	Channel 0 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM0	0xFFFE2D0	FULL	Channel 1 two temperature trim values for software lookup. Note:A1 is not available for this register

Register Name	Address	Permission	Description
SFLASH_PACSS_CHAN1_2TEMP_TRIM1	0xFFFE2D4	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM2	0xFFFE2D8	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM3	0xFFFE2DC	FULL	Channel 1 two temperature trim values for software lookup. Note:A2 is not available for this register
SFLASH_PACSS_CHAN1_2TEMP_TRIM4	0xFFFE2E0	FULL	Channel 1 two temperature trim values for software lookup. Note:A0 is not available for this register
SFLASH_PACSS_CHAN1_2TEMP_TRIM5	0xFFFE2E4	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM6	0xFFFE2E8	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM7	0xFFFE2EC	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM8	0xFFFE2F0	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM9	0xFFFE2F4	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM10	0xFFFE2F8	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM11	0xFFFE2FC	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM12	0xFFFE300	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM13	0xFFFE304	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM14	0xFFFE308	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM15	0xFFFE30C	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM16	0xFFFE310	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM17	0xFFFE314	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM18	0xFFFE318	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM19	0xFFFE31C	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM20	0xFFFE320	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_2TEMP_TRIM21	0xFFFE324	FULL	Channel 1 two temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_3TEMP_TRIM0	0xFFFE328	FULL	Channel 1 three temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_3TEMP_TRIM1	0xFFFE32C	FULL	Channel 1 three temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_3TEMP_TRIM2	0xFFFE330	FULL	Channel 1 three temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_3TEMP_TRIM3	0xFFFE334	FULL	Channel 1 three temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_3TEMP_TRIM4	0xFFFE338	FULL	Channel 1 three temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_3TEMP_TRIM5	0xFFFE33C	FULL	Channel 1 three temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_3TEMP_TRIM6	0xFFFE340	FULL	Channel 1 three temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_3TEMP_TRIM7	0xFFFE344	FULL	Channel 1 three temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_3TEMP_TRIM8	0xFFFE348	FULL	Channel 1 three temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_3TEMP_TRIM9	0xFFFE34C	FULL	Channel 1 three temperature trim values for software lookup.

Register Name	Address	Permission	Description
SFLASH_PACSS_CHAN1_3TEMP_TRIM10	0xFFFE350	FULL	Channel 1 three temperature trim values for software lookup.
SFLASH_PACSS_CHAN1_3TEMP_TRIM11	0xFFFE354	FULL	Channel 1 three temperature trim values for software lookup.
SFLASH_PACSS_CHAN_3TEMP_CENTERTEMP	0xFFFE358	FULL	Defines the center temperature for three temperature trim values
SFLASH_PACSS_CHAN_OFFSET_SCLR	0xFFFE359	FULL	Defines the offset scaler for all offset calibration values
SFLASH_PACSS_DIAG_RSH_PURES	0xFFFE35A	FULL	Measured RSH pull-up resistor value for shunt open testing
SFLASH_PACSS_DIAG_RSL_PURES	0xFFFE35C	FULL	Measured RSL pull-up resistor value for shunt open testing
SFLASH_PACSS_DIAG_RSH2_PURES	0xFFFE35E	FULL	Measured RSH2 pull-up resistor value for shunt open testing Note:A_0 is not available for this register
SFLASH_PACSS_DIAG_RSL2_PURES	0xFFFE360	FULL	Measured RSL2 pull-up resistor value for shunt open testing
SFLASH_PACSS_CHAN1_ETEMP_TRIM	0xFFFE362	FULL	Channel 1 gain adjust to be used with external temperature measurements, -40C value Note:A_2 is not available for this register
SFLASH_PACSS_DIAG_TEMP_P_CAL_S	0xFFFE364	FULL	Primary temperature calibration data setup
SFLASH_PACSS_DIAG_TEMP_P_CAL_A2	0xFFFE368	FULL	Primary temperature calibration data polynomial a2
SFLASH_PACSS_DIAG_TEMP_P_CAL_A1	0xFFFE36A	FULL	Primary temperature calibration data polynomial a1
SFLASH_PACSS_DIAG_TEMP_P_CAL_A0	0xFFFE36C	FULL	Primary temperature calibration data polynomial a0
SFLASH_PACSS_CHAN1_ETEMP_TRIM_2	0xFFFE36E	FULL	Channel 1 gain adjust to be used with external temperature measurements, 150C value
SFLASH_PACSS_DIAG_TEMP_A_CAL_S	0xFFFE370	FULL	Alternate temperature calibration data setup
SFLASH_PACSS_DIAG_TEMP_A_CAL_A2	0xFFFE374	FULL	Alternate temperature calibration data polynomial a2
SFLASH_PACSS_DIAG_TEMP_A_CAL_A1	0xFFFE376	FULL	Alternate temperature calibration data polynomial a1 Note:A_0 is not available for this register
SFLASH_PACSS_DIAG_TEMP_A_CAL_A0	0xFFFE378	FULL	Alternate temperature calibration data polynomial a0

13.1 Register Details

13.1.1 SFLASH_SILICON_ID

Description: Silicon ID
Address: 0xFFFE000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Copied during Boot to CPUSS.SILICON_ID
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SI_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SI_ID [15:8]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	SI_ID	RW	R	X	Silicon ID

13.1.2 SFLASH_SWD_CONFIG

Description: SWD pinout selector
Address: 0xFFFE002
Offset: 0x2
Retention: Retained
IsDeepSleep: No
Comment: Used in BootROM to determine primary or alternate SWD location.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							SWD _SELECT [0:0]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	SWD_SELECT	RW	R	X	0: Use Primary SWD location 1: Use Alternate SWD location (if defined)

13.1.3 SFLASH_DPSLP_KEY_DELAY

Description: DeepSleep wakeup value for PWR_KEY_DELAY
Address: 0xFFFE012
Offset: 0x12
Retention: Retained
IsDeepSleep: No
Comment: Used by firmware during exit from DeepSleep
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:9	WAKEUP_HOLDOFF	RW	R	X	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from DeepSleep. PBOD is ignored and system does not resume until this delay expires.

13.1.4 SFLASH_SWD_LISTEN

Description: Listen Window Length
Address: 0xFFFE014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment: Number of clock cycles to wait for SWD acquire to occur during boot.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CYCLES [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CYCLES [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	CYCLES [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	CYCLES [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	CYCLES	RW		X	Number of clock cycles

13.1.5 SFLASH_FLASH_START

Description: Flash Image Start Address
Address: 0xFFFE018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment: Flash Image start address. If this field is FFFF_FFFF (recommended) the firmware start address is loaded from vector table locations 0,1 (0000_0000 - 0000_0007). If this field is not FFFF_FFFF it is assumed to be a valid firmware start address.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ADDRESS [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ADDRESS [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ADDRESS [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ADDRESS [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ADDRESS	RW		X	Start Address

13.1.6 SFLASH_USER_SFLASH_AREA

Description: Pointer to between 0 and 2 customer usable SFLASH regions
Address: 0xFFFE040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment: The SIZE field indicates whether each area is available
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	LOCATION [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	LOCATION [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	SIZE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	SIZE [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	LOCATION	RW		X	Specifies the lower 16 bits of the absolute address pointer to the start of a user available SFLASH. The upper bits of the pointer are hardcoded as '0x0FFF'.
16:31	SIZE	RW		X	Specifies the size in bytes of the user area. A size of zero indicates that this area is not valid.

13.1.7 SFLASH_DIE_UNIQUE_ID

Description: Uses manufacturing identity to create a unique die ID
Address: 0xFFFE050
Offset: 0x50
Retention: Retained
IsDeepSleep: No
Comment: Manufacturing Data used to form Unique DieID.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ID [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	ID	RW		X	ID Data composed of manufacturing data. Includes manufacturing date (day, month, and year), die identity (fabrication lot, wafer number, x & y coordinates), minor revision number, and test details. The first 64 bits cannot repeat more than once per 10 years The first 96 bits are guaranteed never to repeat Up to 192 bits can be used

13.1.8 SFLASH_IMO_TRIM_LT

Description: IMO Frequency Trim Register (SRSS-Lite) - From 24 to 48 MHz in steps of 4 MHz
Address: 0xFFFE200
Offset: 0x200
Retention: Retained
IsDeepSleep: No
Comment: CLK_IMO_TRIM1 for each frequency 24..48MHz step 4MHz, plus one special frequency
IMO_TRIM_LT[0]: 24 MHz
IMO_TRIM_LT[1]: 28 MHz
IMO_TRIM_LT[2]: 32 MHz
IMO_TRIM_LT[3]: 36 MHz
IMO_TRIM_LT[4]: 40 MHz
IMO_TRIM_LT[5]: 44 MHz
IMO_TRIM_LT[6]: 48 MHz
IMO_TRIM_LT[7]: Special frequency if defined in the architecture TRM
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	OFFSET [7:0]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	OFFSET	RW		X	Frequency trim bits. These bits are determined at manufacturing time for each frequency setting.

13.1.9 SFLASH_IMO_TCTRIM_LT

Description: IMO Temperature Compensation Trim - From 24 to 48 MHz in steps of 4 MHz
Address: 0xFFFE208
Offset: 0x208
Retention: Retained
IsDeepSleep: No
Comment: CLK_IMO_TRIM2 for each frequency 24..48MHz step 4MHz, plus one special frequency
IMO_TCTRIM_LT[0]: 24 MHz
IMO_TCTRIM_LT[1]: 28 MHz
IMO_TCTRIM_LT[2]: 32 MHz
IMO_TCTRIM_LT[3]: 36 MHz
IMO_TCTRIM_LT[4]: 40 MHz
IMO_TCTRIM_LT[5]: 44 MHz
IMO_TCTRIM_LT[6]: 48 MHz
IMO_TCTRIM_LT[7]: Special frequency if defined in the architecture TRM
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	TCTRIM [7:4]				None [3:3]	FSOFFSET [2:0]		

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	FSOFFSET	RW		X	Frequency trim bits. These bits are determined at manufacturing time for each frequency setting.
4:7	TCTRIM	RW		X	IMO temperature compensation trim. These bits are determined at manufacturing time for each frequency setting.

13.1.10 SFLASH_IMO_STEPSIZE_LT

Description: IMO Stepsize Trim - From 24 to 48 MHz in steps of 4 MHz
Address: 0xFFFE210
Offset: 0x210
Retention: Retained
IsDeepSleep: No
Comment: CLK_IMO_TRIM3 for each frequency 24..48MHz step 4MHz, plus one special frequency
IMO_STEPSIZE_LT[0]: 24 MHz
IMO_STEPSIZE_LT[1]: 28 MHz
IMO_STEPSIZE_LT[2]: 32 MHz
IMO_STEPSIZE_LT[3]: 36 MHz
IMO_STEPSIZE_LT[4]: 40 MHz
IMO_STEPSIZE_LT[5]: 44 MHz
IMO_STEPSIZE_LT[6]: 48 MHz
IMO_STEPSIZE_LT[7]: Special frequency if defined in the architecture TRM
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			STEPSIZE [4:0]				

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	STEPSIZE	RW		X	IMO trim stepsize bits. These bits are determined at manufacturing time for each frequency setting.

13.1.11 SFLASH_IMO_4PCT_LIM

Description: IMO trim 4 percent deviation from nominal
Address: 0xFFFE218
Offset: 0x218
Retention: Retained
IsDeepSleep: No
Comment: For parts with HPOSC, and applications which use HPOSC to provide run-time calibration of the IMO frequency.

This register provides a limit for the deviation (either positive or negative) from the nominal IMO trim expressed as an 11 bit value (OFFSET|FSOFFSET). Trims beyond this limit indicate that the IMO has been shifted more than 4 percent from nominal frequency. The 4 percent limit should be applied when conditions support a 3 percent IMO accuracy. 1 percent HPOSC accuracy + 3 percent IMO accuracy means that a > 4 percent deviation is likely caused by a hardware failure in HPOSC, IMO, and/or calibration counters.

This limit only applies when SRSS_CLK_IMO_SELECT.FREQ is set to 48_MHZ.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	TRIM_LIMIT [7:0]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	TRIM_LIMIT	RW		X	TRIM_LIMIT expressed as a positive integer. This value should be added to and subtracted from the nominal IMO trim to create upper/lower limits.

13.1.12 SFLASH_IMO_3PCT_LIM

Description: IMO trim 3 percent deviation from nominal
Address: 0xFFFE219
Offset: 0x219
Retention: Retained
IsDeepSleep: No
Comment: For parts with HPOSC, and applications which use HPOSC to provide run-time calibration of the IMO frequency.

This register provides a limit for the deviation (either positive or negative) from the nominal IMO trim expressed as an 11 bit value (OFFSET|FSOFFSET). Trims beyond this limit indicate that the IMO has been shifted more than 3 percent from nominal frequency. The 3 percent limit should be applied when conditions support a 2 percent IMO accuracy. 1 percent HPOSC accuracy + 2 percent IMO accuracy means that a > 3 percent deviation is likely caused by a hardware failure in HPOSC, IMO, and/or calibration counters.

This limit only applies when SRSS_CLK_IMO_SELECT.FREQ is set to 48_MHZ.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	TRIM_LIMIT [7:0]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	TRIM_LIMIT	RW		X	TRIM_LIMIT expressed as a positive integer. This value should be added to and subtracted from the nominal IMO trim

13.1.13 SFLASH_PILO_6PCT_LIM

Description: PILO trim 6 percent deviation from nominal
Address: 0xFFFE21A
Offset: 0x21A
Retention: Retained
IsDeepSleep: No
Comment: For parts with HPOSC, and applications which use HPOSC to provide run-time calibration of the PILO frequency.

This register provides a limit for the deviation (either positive or negative) from the nominal PILO trim expressed as an 8 bit value (TR_CAP). Trims beyond this limit indicate that the PILO has been shifted more than 6 percent from nominal frequency. As 1 percent HPOSC accuracy + 5 percent PILO accuracy means that a > 6 percent deviation is likely caused by a hardware failure in HPOSC, PILO, and/or calibration counters.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	TRIM_LIMIT [7:0]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	TRIM_LIMIT	RW		X	TRIM_LIMIT expressed as a positive integer. This value should be added to and subtracted from the nominal PILO trim

13.1.14 SFLASH_PACSS_CHAN0_2TEMP_TRIM

Description: Channel 0 two temperature trim values for software lookup.
Address: 0xFFFE280
Offset: 0x280
Retention: Retained
IsDeepSleep: No
Comment: GAIN and OFFSET trim values for PACSS Analog Channel 0. This register is repeated to represent different gains and temperatures:

Index - Description
0 - Gain 1, -40C
1 - Gain 1, 150C
2 - Gain 2, -40C
3 - Gain 2, 150C
4 - Gain 4, -40C
5 - Gain 4, 150C
6 - Gain 8, -40C
7 - Gain 8, 150C
8 - Gain 16, -40C
9 - Gain 16, 150C
10 - Gain 32, -40C
11 - Gain 32, 150C
12 - Gain 64, -40C
13 - Gain 64, 150C
14 - Gain 128, -40C
15 - Gain 128, 150C
16 - Gain 256, -40C
17 - Gain 256, 150C
18 - Gain 512, -40C
19 - Gain 512, 150C

The actual trim value should be a linear interpolation of the provided trims, using the measured junction temperature.

This calibration data is only valid when using the gain settings documented in the Architecture TRM document.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	OFFSETADJ [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	OFFSETADJ [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	GAINADJ [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	GAINADJ [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	OFFSETADJ	RW		X	OFFSET adjustment value, to be loaded in PACSS_DCHAN_OFST_COR.OCOR
16:31	GAINADJ	RW		X	GAIN adjustment value, to be loaded in PACSS_DCHAN_GAIN_COR.GCOR

13.1.15 SFLASH_PACSS_CHAN1_2TEMP_TRIM

Description: Channel 1 two temperature trim values for software lookup.
Address: 0xFFFE2D0
Offset: 0x2D0
Retention: Retained
IsDeepSleep: No
Comment: GAIN and OFFSET trim values for PACSS Analog Channel 1. This register is repeated to represent different gains and temperatures:

Index - Description
0 - Gain 0.5, -40C
1 - Gain 0.5, 150C
2 - Gain 1, -40C
3 - Gain 1, 150C
4 - Gain 2, -40C
5 - Gain 2, 150C
6 - Gain 4, -40C
7 - Gain 4, 150C
8 - Gain 8, -40C
9 - Gain 8, 150C
10 - Gain 16, -40C
11 - Gain 16, 150C
12 - Gain 32, -40C
13 - Gain 32, 150C
14 - Gain 64, -40C
15 - Gain 64, 150C
16 - Gain 128, -40C
17 - Gain 128, 150C
18 - Gain 256, -40C
19 - Gain 256, 150C
20 - Gain 512, -40C
21 - Gain 512, 150C

The actual trim value should be a linear interpolation of the provided trims, using the measured junction temperature.

This calibration data is only valid when using the gain settings documented in the Architecture TRM document.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	OFFSETADJ [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	OFFSETADJ [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	GAINADJ [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	GAINADJ [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	OFFSETADJ	RW		X	OFFSET adjustment value, to be loaded in PACSS_DCHAN_OFST_COR.OCOR

Bits	Name	SW	HW	Default or Enum	Description
16:31	GAINADJ	RW		X	GAIN adjustment value, to be loaded in PACSS_DCHAN_GAIN_COR.GCOR

13.1.16 SFLASH_PACSS_CHAN1_3TEMP_TRIM

Description: Channel 1 three temperature trim values for software lookup.
Address: 0xFFFE328
Offset: 0x328
Retention: Retained
IsDeepSleep: No
Comment: GAIN and OFFSET trim values for PACSS Analog Channel 1. This register is repeated to represent different gains and temperatures:

Index - Definition
0 - VSENSE/16, -40C
1 - VSENSE/16, CENTERTEMP
2 - VSENSE/16, 150C
3 - VSENSE/24, -40C
4 - VSENSE/24, CENTERTEMP
5 - VSENSE/24, 150C
6 - VDIAG/16, -40C
7 - VDIAG/16, CENTERTEMP
8 - VDIAG/16, 150C
9 - VDIAG/24, -40C
10 - VDIAG/24, CENTERTEMP
11 - VDIAG/24, 150C

The actual trim should be a linear interpolation of the provided trims, using the measured junction temperature.

This calibration data is only valid when using the gain settings documented in the Architecture TRM document.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	OFFSETADJ [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	OFFSETADJ [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	GAINADJ [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	GAINADJ [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	OFFSETADJ	RW		X	OFFSET adjustment value, to be loaded in PACSS_DCHAN_OFST_COR.OCOR
16:31	GAINADJ	RW		X	GAIN adjustment value, to be loaded in PACSS_DCHAN_GAIN_COR.GCOR

13.1.17 SFLASH_PACSS_CHAN_3TEMP_CENTERTEMP

Description: Defines the center temperature for three temperature trim values
Address: 0xFFFE358
Offset: 0x358
Retention: Retained
IsDeepSleep: No
Comment: Defines the center temperature for three temperature trim values. Expressed as an unsigned integer degrees in Celsius.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CENTERTEMP [7:0]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	CENTERTEMP	RW		X	Center temperature for 3 temperature calibration, degrees Celsius.

13.1.18 SFLASH_PACSS_CHAN_OFFSET_SCLR

Description: Defines the offset scaler for all offset calibration values
Address: 0xFFFE359
Offset: 0x359
Retention: Retained
IsDeepSleep: No
Comment: Defines the offset scaler to be used with the OFFSETADJ for all 2TEMP and 3TEMP calibration values.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	OFFSETSCLR [7:0]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	OFFSETSCLR	RW		X	Offset scaler, to be loaded in PACSS_DCHAN_OFST_COR.OCOR_SCLR

13.1.19 SFLASH_PACSS_DIAG_RSH_PURES

Description: Measured RSH pull-up resistor value for shunt open testing
Address: 0xFFFE35A
Offset: 0x35A
Retention: Retained
IsDeepSleep: No
Comment: Resistance of pull-up resistor, measured during manufacturing. This resistance can be used to reduce the variation of the open-shunt diagnostic test.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RES_COLD [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RES_HOT [15:8]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	RES_COLD	RW		X	Resistance/32 in Ohms, measured at -40C
8:15	RES_HOT	RW		X	Resistance/32 in Ohms, measured at 150C

13.1.20 SFLASH_PACSS_DIAG_RSL_PURES

Description: Measured RSL pull-up resistor value for shunt open testing
Address: 0xFFFE35C
Offset: 0x35C
Retention: Retained
IsDeepSleep: No
Comment: Resistance of pull-up resistor, measured during manufacturing. This resistance can be used to reduce the variation of the open-shunt diagnostic test.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RES_COLD [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RES_HOT [15:8]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	RES_COLD	RW		X	Resistance/32 in Ohms, measured at -40C
8:15	RES_HOT	RW		X	Resistance/32 in Ohms, measured at 150C

13.1.21 SFLASH_PACSS_DIAG_RSH2_PURES

Description: Measured RSH2 pull-up resistor value for shunt open testing
Address: 0xFFFE35E
Offset: 0x35E
Retention: Retained
IsDeepSleep: No
Comment: Resistance of pull-up resistor, measured during manufacturing. This resistance can be used to reduce the variation of the open-shunt diagnostic test.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RES_COLD [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RES_HOT [15:8]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	RES_COLD	RW		X	Resistance/32 in Ohms, measured at -40C
8:15	RES_HOT	RW		X	Resistance/32 in Ohms, measured at 150C

13.1.22 SFLASH_PACSS_DIAG_RSL2_PURES

Description: Measured RSL2 pull-up resistor value for shunt open testing
Address: 0xFFFE360
Offset: 0x360
Retention: Retained
IsDeepSleep: No
Comment: Resistance of pull-up resistor, measured during manufacturing. This resistance can be used to reduce the variation of the open-shunt diagnostic test.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RES_COLD [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	RES_HOT [15:8]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	RES_COLD	RW		X	Resistance/32 in Ohms, measured at -40C
8:15	RES_HOT	RW		X	Resistance/32 in Ohms, measured at 150C

13.1.23 SFLASH_PACSS_CHAN1_ETEMP_TRIM

Description: Channel 1 gain adjust to be used with external temperature measurements, -40C value
Address: 0xFFFE362
Offset: 0x362
Retention: Retained
IsDeepSleep: No
Comment: GAIN PACSS Analog Channel 1 to be used when making external thermistor based temperature measurements. This gain compensates for the error in the VDD/3 resistor divider, improving overall accuracy. Use with the OFFSETADJ value derived from PACSS_CHAN1_2TEMP_TRIM for Gain 1. Use in combination with PACSS_CHAN1_ETEMP_TRIM_2 for interpolated gain calibration.

This calibration data is only valid when using the gain settings documented in the Architecture TRM document.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ETGAINADJ [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ETGAINADJ [15:8]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	ETGAINADJ	RW		X	GAIN adjustment value, to be loaded in PACSS_DCHAN_GAIN_COR.GCOR

13.1.24 SFLASH_PACSS_DIAG_TEMP_P_CAL_S

Description: Primary temperature calibration data setup
Address: 0xFFFE364
Offset: 0x364
Retention: Retained
IsDeepSleep: No
Comment: Defines the primary measurement conditions. The temperature is calculated from ADC voltage measurements as follows:
dVBE = ADC(UNIT) - ADC(1) with a 29 bit signed result size
ratio = ADC(UNIT)/ADC(1) into test resistor instead of BJT
x = dVBE = dVBE*(A*ratio + B) where A and B are specified in the architecture TRM
T = (a2*(x^2)/2^34 + a1*x/2^9 + a0*2^14)/2^20
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	IREF_1_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	BIPOLAR_1_MASK [15:10]						None [9:9]	IREF_1_MASK [8:8]

Bits	23	22	21	20	19	18	17	16
Name	IREF_BIPOLAR_UNIT_MASK [23:20]				None [19:19]	BIPOLAR_1_MASK [18:16]		

Bits	31	30	29	28	27	26	25	24
Name	LOAD_MODE [31:31]	IREF_SEL [30:30]	UNIT_MODE [29:29]	IREF_BIPOLAR_UNIT_MASK [28:24]				

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:8	IREF_1_MASK	RW		X	Specifies which IREF segments are selected, either when UNIT_MODE = BIPOLAR, or when performing the ADC(1) measurement. Load this directly into the PACSS_MMIO_TMPS_CTL.IREF_UNIT bit field.
10:18	BIPOLAR_1_MASK	RW		X	Specifies which BIPOLAR devices are selected, either when UNIT_MODE = IREF, or when performing the ADC(1) measurement. Load this directly into the PACSS_MMIO_TMS_CTL_BIPOLAR_UNIT bit field.
20:28	IREF_BIPOLAR_UNIT_MASK	RW		X	Defines the elements of the unit that can participate in the temperature sensing during the 'ADC(UNIT)' measurement. Load this directly into the PACSS_MMIO_TMS_CTL.IREF_UNIT or .BIPOLAR_UNIT bit field based on the value of UNIT_MODE.
29	UNIT_MODE	RW		X	Defines which element to modulate for the ADC(UNIT) measurement
	IREF			0	Modulate IREF units
	BIPOLAR			1	Modulate BIPOLAR (NPN/PNP) units
30	IREF_SEL	RW		X	Defines which IREF source to use for the measurements

Bits	Name	SW	HW	Default or Enum	Description
	AREF			0	Use the IREF from the AREF block
	SRSS			1	Use the IREF from the System Resources block
31	LOAD_MODE	RW		X	Defines the type of BJT used for the measurements
	PNP			0	PNP device
	NPN			1	NPN device

13.1.25 SFLASH_PACSS_DIAG_TEMP_P_CAL_A2

Description: Primary temperature calibration data polynomial a2
Address: 0xFFFE368
Offset: 0x368
Retention: Retained
IsDeepSleep: No
Comment: Defines the linear and constant coefficients of the primary temperature polynomial
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	A2 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	A2 [15:8]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	A2	RW		X	Temperature calculation polynomial square coefficient

13.1.26 SFLASH_PACSS_DIAG_TEMP_P_CAL_A1

Description: Primary temperature calibration data polynomial a1
Address: 0xFFFE36A
Offset: 0x36A
Retention: Retained
IsDeepSleep: No
Comment: Defines the linear and constant coefficients of the primary temperature polynomial
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	A1 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	A1 [15:8]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	A1	RW		X	Temperature calculation polynomial linear coefficient

13.1.27 SFLASH_PACSS_DIAG_TEMP_P_CAL_A0

Description: Primary temperature calibration data polynomial a0
Address: 0xFFFE36C
Offset: 0x36C
Retention: Retained
IsDeepSleep: No
Comment: Defines the linear and constant coefficients of the primary temperature polynomial
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	A0 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	A0 [15:8]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	A0	RW		X	Temperature calculation polynomial constant coefficient

13.1.28 SFLASH_PACSS_CHAN1_ETEMP_TRIM_2

Description: Channel 1 gain adjust to be used with external temperature measurements, 150C value
Address: 0xFFFE36E
Offset: 0x36E
Retention: Retained
IsDeepSleep: No
Comment: GAIN PACSS Analog Channel 1 to be used when making external thermistor based temperature measurements. This gain compensates for the error in the VDD/3 resistor divider, improving overall accuracy. Use with the OFFSETADJ value derived from PACSS_CHAN1_2TEMP_TRIM for Gain 1. Use in combination with PACSS_CHAN1_ETEMP_TRIM for interpolated gain calibration.

This calibration data is only valid when using the gain settings documented in the Architecture TRM document.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	ETGAINADJ2 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	ETGAINADJ2 [15:8]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	ETGAINADJ2	RW		X	GAIN adjustment value, to be loaded in PACSS_DCHAN_GAIN_COR.GCOR

13.1.29 SFLASH_PACSS_DIAG_TEMP_A_CAL_S

Description: Alternate temperature calibration data setup
Address: 0xFFFE370
Offset: 0x370
Retention: Retained
IsDeepSleep: No
Comment: Defines the alternate measurement conditions. The temperature is calculated from ADC voltage measurements as follows:
dVBE = ADC(UNIT) - ADC(1) with a 29 bit signed result size
ratio = ADC(UNIT)/ADC(1) into test resistor instead of BJT
x = dVBE = dVBE*(A*ratio + B) where A and B are specified in the architecture TRM
T = (a2*(x^2)/2^34 + a1*x/2^9 + a0*2^14)/2^20
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	IREF_1_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	BIPOLAR_1_MASK [15:10]						None [9:9]	IREF_1_MASK [8:8]

Bits	23	22	21	20	19	18	17	16
Name	IREF_BIPOLAR_UNIT_MASK [23:20]				None [19:19]	BIPOLAR_1_MASK [18:16]		

Bits	31	30	29	28	27	26	25	24
Name	LOAD_MODE [31:31]	IREF_SEL [30:30]	UNIT_MODE [29:29]	IREF_BIPOLAR_UNIT_MASK [28:24]				

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:8	IREF_1_MASK	RW		X	Specifies which IREF segments are selected, either when UNIT_MODE = BIPOLAR, or when performing the ADC(1) measurement. Load this directly into the PACSS_MMIO_TMS_CTL_IREF_UNIT bit field.
10:18	BIPOLAR_1_MASK	RW		X	Specifies which BIPOLAR devices are selected, either when UNIT_MODE = IREF, or when performing the ADC(1) measurement. Load this directly into the PACSS_MMIO_TMS_CTL_BIPOLAR_UNIT bit field.
20:28	IREF_BIPOLAR_UNIT_MASK	RW		X	Defines the elements of the unit that can participate in the temperature sensing during the 'ADC(UNIT)' measurement. Load this directly into the PACSS_MMIO_TMS_CTL.IREF_UNIT or .BIPOLAR_UNIT bit field based on the value of UNIT_MODE.
29	UNIT_MODE	RW		X	Defines which element to modulate for the ADC(UNIT) measurement
	IREF			0	Modulate IREF units
	BIPOLAR			1	Modulate BIPOLAR (NPN/PNP) units
30	IREF_SEL	RW		X	Defines which IREF source to use for the measurements

Bits	Name	SW	HW	Default or Enum	Description
	AREF			0	Use the IREF from the AREF block
	SRSS			1	Use the IREF from the System Resources block
31	LOAD_MODE	RW		X	Defines the type of BJT used for the measurements
	PNP			0	PNP device
	NPN			1	NPN device

13.1.30 SFLASH_PACSS_DIAG_TEMP_A_CAL_A2

Description: Alternate temperature calibration data polynomial a2
Address: 0xFFFE374
Offset: 0x374
Retention: Retained
IsDeepSleep: No
Comment: Defines the linear and constant coefficients of the alternate temperature polynomial
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	A2 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	A2 [15:8]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	A2	RW		X	Temperature calculation polynomial square coefficient

13.1.31 SFLASH_PACSS_DIAG_TEMP_A_CAL_A1

Description: Alternate temperature calibration data polynomial a1
Address: 0xFFFE376
Offset: 0x376
Retention: Retained
IsDeepSleep: No
Comment: Defines the linear and constant coefficients of the alternate temperature polynomial
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	A1 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	A1 [15:8]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	A1	RW		X	Temperature calculation polynomial linear coefficient

13.1.32 SFLASH_PACSS_DIAG_TEMP_A_CAL_A0

Description: Alternate temperature calibration data polynomial a0
Address: 0xFFFE378
Offset: 0x378
Retention: Retained
IsDeepSleep: No
Comment: Defines the linear and constant coefficients of the alternate temperature polynomial
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	A0 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	A0 [15:8]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	A0	RW		X	Temperature calculation polynomial constant coefficient

14 SPCIF

Description Flash Control Interface
Base Address 0x40110000
Size 0x10000
Slave Num CPUMEMSSV3_VER3

Register Name	Address	Permission	Description
SPCIF_GEOMETRY	0x40110000	FULL	Flash/NVL geometry information Note:NVL is not available for this register
SPCIF_FLASH_LOCK	0x40110060	FULL	Flash Lock Register
SPCIF_FLASH_MACRO_WE	0x40110064	FULL	Flash Macro Write Enable
SPCIF_INTR	0x401107F0	FULL	SPCIF interrupt request register
SPCIF_INTR_SET	0x401107F4	FULL	SPCIF interrupt set request register
SPCIF_INTR_MASK	0x401107F8	FULL	SPCIF interrupt mask register
SPCIF_INTR_MASKED	0x401107FC	FULL	SPCIF interrupt masked request register

14.1 Register Details

14.1.1 SPCIF_GEOMETRY

Description: Flash/NVL geometry information
Address: 0x40110000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: This register indicates the flash/NVLatch geometry parameters for the current device. This does not take wounding into account, which may restrict access to flash memory. Note that the default values of the read-only fields are determined by the CPUSS design time configuration.
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	FLASH [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SFLASH [15:14]		FLASH [13:8]					

Bits	23	22	21	20	19	18	17	16
Name	FLASH_ROW [23:22]		NUM_FLASH [21:20]		SFLASH [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	DE_CPD _LP [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:13	FLASH	R	W	Undefined	Regular flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the flash capacity of all flash macros together: '0': 256 Bytes. '1': 2*256 Bytes. ... '16383': 16384*256 Bytes.
14:19	SFLASH	R	W	Undefined	Supervisory flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the supervisory flash capacity of all flash macros together: '0': 256 Bytes. '1': 2*256 Bytes. ... '63': 64*256 Bytes.
20:21	NUM_FLASH	R	W	Undefined	Number of flash macros (chip dependent): '0': 1 flash macro '1': 2 flash macros '2': 3 flash macros '3': 4 flash macros

Bits	Name	SW	HW	Default or Enum	Description
22:23	FLASH_ROW	R	W	Undefined	Page size in 64 Byte multiples (chip dependent): '0': 64 byte '1': 128 byte '2': 192 byte '3': 256 byte The page size is used to determine the number of Bytes in a page for Flash page based operations (e.g. PGM_PAGE). Note: the field name FLASH_ROW is misleading, as this field specifies the number of Bytes in a page, rather than the number of Bytes in a row. In a single plane flash macro architecture, a page consists of a single row. However, in a multi plane flash macro architecture, a page consists of multiple rows from different planes.
31	DE_CPD_LP	RW		0	0': SRAM busy wait loop has not been copied. '1': Busy wait loop has been written into SRAM.

14.1.2 SPCIF_FLASH_LOCK

Description: Flash Lock Register
Address: 0x40110060
Offset: 0x60
Retention: Retained
IsDeepSleep: No
Comment: Locks Macro Write enables when key is written to register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	KEY [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	KEY	W	R	0	Write Only register that locks/unlocks access to the FLASH MACRO_WE register by writing a key value to the register. The Key is the 32 bit value '0xF56B3A81'. When this specific bit pattern is written to the register, write access to FLASH_MACRO_WE is toggled between locked and unlocked. The bit FLASH_MACRO_WE.LOCKED toggles upon receipt of the required key value.

14.1.3 SPCIF_FLASH_MACRO_WE

Description: Flash Macro Write Enable
Address: 0x40110064
Offset: 0x64
Retention: Not Retained
IsDeepSleep: No
Comment: Locks Macro Write enables when key is written to register.
Default: 0xF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						MAC_WRITE_EN [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	LOCKED [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	MAC_WRITE_EN	RW	A	3	Access control to Flash Macros Write Access. This is a bit mask where each bit controls Program/Erase Access to the corresponding Macro. When the bit is set to '1' then the Macro may be programmed/erased, when the bit is set to '0', the Macro content is locked. The content of this register may only be changed when FLASH_MACRO_WE.LOCKED is '0'.
31	LOCKED	R	W	0	When set indicates that write access to FLASH_MACRO_WE.MAC_WRITE_EN is blocked. The value of this bit toggles when the key value is written into FLASH_LOCK.KEY.

14.1.4 SPCIF_INTR

Description: SPCIF interrupt request register
Address: 0x401107F0
Offset: 0x7F0
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							TIMER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TIMER	RW1C	RW1S	0	Timer counter value reaches '0'. Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit.

14.1.5 SPCIF_INTR_SET

Description: SPCIF interrupt set request register
Address: 0x401107F4
Offset: 0x7F4
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							TIMER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TIMER	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field.

14.1.6 SPCIF_INTR_MASK

Description: SPCIF interrupt mask register
Address: 0x401107F8
Offset: 0x7F8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							TIMER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TIMER	RW	R	0	Mask for corresponding field in INTR register.

14.1.7 SPCIF_INTR_MASKED

Description: SPCIF interrupt masked request register
Address: 0x401107FC
Offset: 0x7FC
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							TIMER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TIMER	R	W	0	Logical and of corresponding request and mask fields.

15 SPCIF1

Description Flash Control Interface
Base Address 0x40120000
Size 0x10000
Slave Num CPUMEMSSV3_VER3

Register Name	Address	Permission	Description
SPCIF1_GEOMETRY	0x40120000	FULL	Flash/NVL geometry information Note:NVL is not available for this register
SPCIF1_FLASH_LOCK	0x40120060	FULL	Flash Lock Register
SPCIF1_FLASH_MACRO_WE	0x40120064	FULL	Flash Macro Write Enable
SPCIF1_INTR	0x401207F0	FULL	SPCIF interrupt request register
SPCIF1_INTR_SET	0x401207F4	FULL	SPCIF interrupt set request register
SPCIF1_INTR_MASK	0x401207F8	FULL	SPCIF interrupt mask register
SPCIF1_INTR_MASKED	0x401207FC	FULL	SPCIF interrupt masked request register

15.1 Register Details

15.1.1 SPCIF1_GEOMETRY

Description: Flash/NVL geometry information
Address: 0x40120000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: This register indicates the flash/NVLatch geometry parameters for the current device. This does not take wounding into account, which may restrict access to flash memory. Note that the default values of the read-only fields are determined by the CPUSS design time configuration.
Default: Undefined as one or more bit fields have a default value that is undefined

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	FLASH [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	SFLASH [15:14]		FLASH [13:8]					

Bits	23	22	21	20	19	18	17	16
Name	FLASH_ROW [23:22]		NUM_FLASH [21:20]		SFLASH [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	DE_CPD _LP [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:13	FLASH	R	W	Undefined	Regular flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the flash capacity of all flash macros together: '0': 256 Bytes. '1': 2*256 Bytes. ... '16383': 16384*256 Bytes.
14:19	SFLASH	R	W	Undefined	Supervisory flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the supervisory flash capacity of all flash macros together: '0': 256 Bytes. '1': 2*256 Bytes. ... '63': 64*256 Bytes.
20:21	NUM_FLASH	R	W	Undefined	Number of flash macros (chip dependent): '0': 1 flash macro '1': 2 flash macros '2': 3 flash macros '3': 4 flash macros

Bits	Name	SW	HW	Default or Enum	Description
22:23	FLASH_ROW	R	W	Undefined	Page size in 64 Byte multiples (chip dependent): '0': 64 byte '1': 128 byte '2': 192 byte '3': 256 byte The page size is used to determine the number of Bytes in a page for Flash page based operations (e.g. PGM_PAGE). Note: the field name FLASH_ROW is misleading, as this field specifies the number of Bytes in a page, rather than the number of Bytes in a row. In a single plane flash macro architecture, a page consists of a single row. However, in a multi plane flash macro architecture, a page consists of multiple rows from different planes.
31	DE_CPD_LP	RW		0	0': SRAM busy wait loop has not been copied. '1': Busy wait loop has been written into SRAM.

15.1.2 SPCIF1_FLASH_LOCK

Description: Flash Lock Register
Address: 0x40120060
Offset: 0x60
Retention: Retained
IsDeepSleep: No
Comment: Locks Macro Write enables when key is written to register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	KEY [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	KEY	W	R	0	Write Only register that locks/unlocks access to the FLASH MACRO_WE register by writing a key value to the register. The Key is the 32 bit value '0xF56B3A81'. When this specific bit pattern is written to the register, write access to FLASH_MACRO_WE is toggled between locked and unlocked. The bit FLASH_MACRO_WE.LOCKED toggles upon receipt of the required key value.

15.1.3 SPCIF1_FLASH_MACRO_WE

Description: Flash Macro Write Enable
Address: 0x40120064
Offset: 0x64
Retention: Not Retained
IsDeepSleep: No
Comment: Locks Macro Write enables when key is written to register.
Default: 0xF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							MAC_WRITE_EN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	LOCKED [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	MAC_WRITE_EN	RW	A	1	Access control to Flash Macros Write Access. This is a bit mask where each bit controls Program/Erase Access to the corresponding Macro. When the bit is set to '1' then the Macro may be programmed/erased, when the bit is set to '0', the Macro content is locked. The content of this register may only be changed when FLASH_MACRO_WE.LOCKED is '0'.
31	LOCKED	R	W	0	When set indicates that write access to FLASH_MACRO_WE.MAC_WRITE_EN is blocked. The value of this bit toggles when the key value is written into FLASH_LOCK.KEY.

15.1.4 SPCIF1_INTR

Description: SPCIF interrupt request register
Address: 0x401207F0
Offset: 0x7F0
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							TIMER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TIMER	RW1C	RW1S	0	Timer counter value reaches '0'. Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit.

15.1.5 SPCIF1_INTR_SET

Description: SPCIF interrupt set request register
Address: 0x401207F4
Offset: 0x7F4
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							TIMER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TIMER	RW1S	A	0	Write INTR_SET field with '1' to set corresponding INTR field.

15.1.6 SPCIF1_INTR_MASK

Description: SPCIF interrupt mask register
Address: 0x401207F8
Offset: 0x7F8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							TIMER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TIMER	RW	R	0	Mask for corresponding field in INTR register.

15.1.7 SPCIF1_INTR_MASKED

Description: SPCIF interrupt masked request register
Address: 0x401207FC
Offset: 0x7FC
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							TIMER [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TIMER	R	W	0	Logical and of corresponding request and mask fields.

16 SRSSHV

Description System Resources High Voltage Subsystem
Base Address 0x40030000
Size 0x10000
Slave Num MMIO0

Register Name	Address	Permission	Description
PWR_CONTROL	0x40030000	FULL	Power Mode Control (Lock Protected)
PWR_KEY_DELAY	0x40030004	FULL	Power System Key&Delay Register (Lock Protected)
TST_MODE	0x40030014	FULL	Test Mode Control Register
CLK_CAL_CNT1	0x4003001C	FULL	Clock Calibration Counter 1
CLK_CAL_CNT2	0x40030020	FULL	Clock Calibration Counter 2
CLK_SELECT	0x40030028	FULL	Clock Select Register (Lock Protected)
CLK_ILO_CONFIG	0x4003002C	FULL	ILO Configuration (Lock Protected)
CLK_IMO_CONFIG	0x40030030	FULL	IMO Configuration (Lock Protected)
CLK_DFT_SELECT	0x40030034	FULL	Clock DFT Mode Selection Register
SRSS_MASKED	0x40030040	FULL	SRSS Interrupt Masked Register
SRSS_INTR	0x40030044	FULL	SRSS Interrupt Register
SRSS_INTR_SET	0x40030048	FULL	SRSS Interrupt Set Register
SRSS_INTR_MASK	0x4003004C	FULL	SRSS Interrupt Mask Register
RES_CAUSE	0x40030054	FULL	Reset Cause Observation Register
REG_PROT	0x40030080	FULL	Register Protection
CRWDT_CTL	0x40030090	FULL	Challenge Response WatchDog Control (Lock Protected)
CRWDT_CHALLENGE	0x40030094	FULL	Challenge Response WatchDog Challenge Value
CRWDT_RESPONSE	0x40030098	FULL	Challenge Response WatchDog Response Value
CRWDT_UPCNT	0x4003009C	FULL	Challenge Response WatchDog Up Counter
CRWDT_EARLY	0x400300A0	FULL	Challenge Response WatchDog Early Limit (Lock Protected)
CRWDT_WARN	0x400300A4	FULL	Challenge Response WatchDog Warning Limit (Lock Protected)
CRWDT_LATE	0x400300A8	FULL	Challenge Response WatchDog Late Limit (Lock Protected)
CRWDT_CONFIG	0x400300AC	FULL	Challenge Response WatchDog Configuration
LIFETIME_CTL	0x400300B0	FULL	Liftetime Counter Control (Lock Protected)
LIFETIME_WAKEUP	0x400300B4	FULL	Lifetime Wakeup Value
LIFETIME_COUNTER	0x400300B8	FULL	Lifetime Counter Current Value
PWR_SSV_CTL	0x400300E0	FULL	Supply Supervisory Control Register (Lock Protected)
PWR_SSV_STATUS	0x400300E4	FULL	Supply Supervision Status Register
HPOSC_CTL	0x40030300	FULL	High Precision Oscillator Control (Lock Protected)
PILO_CTL	0x40030400	FULL	Precision Low Power Oscillator Control (Lock Protected)
PWR_BG_TRIM1	0x4003FF00	FULL	Bandgap Trim Register (Lock Protected)
PWR_BG_TRIM2	0x4003FF04	FULL	Bandgap Trim Register (Lock Protected)
CLK_IMO_SELECT	0x4003FF08	FULL	IMO Frequency Select Register (Lock Protected)
CLK_IMO_TRIM1	0x4003FF0C	FULL	IMO Trim Register (Lock Protected)
CLK_IMO_TRIM2	0x4003FF10	FULL	IMO Trim Register (Lock Protected)
CLK_IMO_TRIM3	0x4003FF14	FULL	IMO Trim Register (Lock Protected)
PWR_PWRSYS_TRIM1	0x4003FF18	FULL	Power System Trim Register (Lock Protected)
TRIM_BODVCCD	0x4003FF1C	FULL	Brown Out Detect Trim (VCCD) (Lock Protected)
TRIM_OVDVCCD	0x4003FF20	FULL	Over Voltage Detect Trim (VCCD) (Lock Protected)
TRIM_HPOSC0_CTL	0x4003FF24	FULL	High Precision Oscillator Trim Control 0 (Lock Protected)
TRIM_HPOSC1_CTL	0x4003FF28	FULL	High Precision Oscillator Trim Control 1 (Lock Protected)
TRIM_HPOSC2_CTL	0x4003FF2C	FULL	High Precision Oscillator Trim Control 2 (Lock Protected)
TRIM_HPOSC3_CTL	0x4003FF30	FULL	High Precision Oscillator Trim Control 3 (Lock Protected)

Register Name	Address	Permission	Description
TRIM_HPOSC4_CTL	0x4003FF34	FULL	High Precision Oscillator Trim Control 4 (Lock Protected)
TRIM_PILO0_CTL	0x4003FF38	FULL	Low Frequency Oscillator Trim Control 0 (Lock Protected)
TRIM_PILO1_CTL	0x4003FF3C	FULL	Low Frequency Oscillator Trim Control 1 (Lock Protected)
TRIM_PILO2_CTL	0x4003FF40	FULL	Low Frequency Oscillator Trim Control 2 (Lock Protected)
TRIM_PILO3_CTL	0x4003FF44	FULL	Low Frequency Oscillator Trim Control 3 (Lock Protected)
TRIM_PILO4_CTL	0x4003FF48	FULL	Low Frequency Oscillator Trim Control 4 (Lock Protected)
TRIM_PILO5_CTL	0x4003FF4C	FULL	Low Frequency Oscillator Trim Control 5 (Lock Protected)
TRIM_BODVDDD	0x4003FF50	FULL	Brown Out Detect Trim (VDDD) (Lock Protected)
TRIM_OVDVDDD	0x4003FF54	FULL	Over Voltage Detect Trim (VDDD) (Lock Protected)

16.1 WDT

Register Name	Address	Permission	Description
WDT_CTL	0x40030100	FULL	WDT Control Register
WDT_LOWER_LIMIT	0x40030104	FULL	WDT Lower Limit Register
WDT_UPPER_LIMIT	0x40030108	FULL	WDT Upper Limit Register
WDT_WARN_LIMIT	0x4003010C	FULL	WDT Warn Limit Register
WDT_CONFIG	0x40030110	FULL	WDT Configuration Register
WDT_CNT	0x40030114	FULL	WDT Count Register
WDT_LOCK	0x40030140	FULL	WDT Lock register
WDT_SERVICE	0x40030144	FULL	WDT Service register
WDT_INTR	0x40030150	FULL	WDT Interrupt Register
WDT_INTR_SET	0x40030154	FULL	WDT Interrupt Set Register
WDT_INTR_MASK	0x40030158	FULL	WDT Interrupt Mask Register
WDT_INTR_MASKED	0x4003015C	FULL	WDT Interrupt Masked Register

16.2 Register Details

16.2.1 PWR_CONTROL

Description: Power Mode Control (Lock Protected)
Address: 0x40030000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Controls the device power mode options and allows observation of current state.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		LPM _READY [5:5]	DEBUG _SESSION [4:4]	POWER_MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	EXT_VCCD [23:23]	None [22:20]			SPARE [19:18]		OVER _TEMP _THRESH [17:17]	OVER _TEMP_EN [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	POWER_MODE	R	RW	0	Current power mode of the device. Note that this field cannot be read in all power modes on actual silicon.
	RESET			0	RESET state
	ACTIVE			1	ACTIVE state
	SLEEP			2	SLEEP state
	DEEP_SLEEP			3	DEEP_SLEEP state
4	DEBUG_SESSION	R	RW	0	Indicates whether a debug session is active (CDBGPWRUPREQ signal is 1)
	NO_SESSION			0	No debug session active
	SESSION_ACTIVE			1	Debug session is active
5	LPM_READY	R	RW	0	Indicates whether the low power mode regulator is ready to enter DeepSleep mode. 0: If DeepSleep mode is requested, device will enter SLEEP mode. When low power regulators are ready, device will automatically enter the originally requested mode. 1: Normal operation. DeepSleep works as described.
16	OVER_TEMP_EN	RW	R	0	Enables the die over temperature sensor. Must be enabled when using the TEMP_HIGH interrupt.
17	OVER_TEMP_THRESH	RW	R	0	Over-temperature threshold. 0: TEMP_HIGH condition occurs between 110C and 145C. 1: TEMP_HIGH condition occurs between 50C and 90C (used for testing).
18:19	SPARE	R	RW	0	Spare AHB readback bits that are hooked to PWR_PWRSYS_TRIM1.SPARE_TRIM[1:0] through spare logic equivalent to bitwise inversion. Engineering only, should always be set to default.

Bits	Name	SW	HW	Default or Enum	Description
23	EXT_VCCD	RW	A	0	Always write 0 except as noted below. PSoC4-S0 and Streetfighter CapSense products may set this bit if Vccd is provided externally (on Vccd pin). Setting this bit turns off the active regulator and will lead to system reset (BOD) unless both Vddd and Vccd pins are supplied externally. This register field reset with hard reset (power related, XRES, WDT).

16.2.2 PWR_KEY_DELAY

Description: Power System Key&Delay Register (Lock Protected)
Address: 0x40030004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xF8

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:9	WAKEUP_HOLDOFF	RW	R	248	Delay to wait for references to settle on wakeup from DeepSleep. BOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. The default assumes the output of the predivider is 48MHz + 3 percent. Firmware may scale this setting according to the fastest actual clock frequency that can occur when waking from DeepSleep.

16.2.3 TST_MODE

Description: Test Mode Control Register
Address: 0x40030014
Offset: 0x14
Retention: Retained
IsDeepSleep: Yes
Comment: Controls primary test mode. This is a single bit that can be written directly from the ATE/Programmer in any protection mode. It's main function is to signal to the Boot ROM that normal firmware execution is not to commence after boot is complete. Instead the Boot ROM will enter a wait loop for system commands.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					SWD_CONNECTED [2:2]	None [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	TEST_MODE [31:31]	TEST_KEY_DFT_EN [30:30]	None [29:29]	BLOCK_ALT_XRES [28:28]	None [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
2	SWD_CONNECTED	R	RW	0	0: SWD not active 1: SWD activated (Line Reset & Connect sequence passed) (Note: this bit replaces TST_CTRL.SWD_CONNECTED and is present in all M0S8 products except TSG4)
28	BLOCK_ALT_XRES	RW	A	0	Relevant only for parts that have the alternate XRES mechanism of overloading a GPIO pin temporarily as alternate XRES during test. When set, this bit blocks the alternate XRES function, such that the pin can be used for normal I/O or for ddft/adft observation. This register field resets with hard reset (power related, XRES, WDT)
30	TEST_KEY_DFT_EN	R	RW	0	This bit is set when a XRES test mode key is shifted in. It is the value of the test_key_dft_en signal. When this bit is set, the BootROM will not yield execution to the FLASH image (same function as setting TEST_MODE bit below).
31	TEST_MODE	RW	R	0	0: Normal operation mode 1: Test mode (any test mode) Setting this bit will prevent BootROM from yielding execution to Flash image.

16.2.4 CLK_CAL_CNT1

Description: Clock Calibration Counter 1
Address: 0x4003001C
Offset: 0x1C
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x80000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CAL_COUNTER1 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CAL_COUNTER1 [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	CAL_COUNTER_DONE [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	CAL_COUNTER1	RW	A	0	Down-counter clocked on DFT output #0 (see CLK_DFT_SELECT). This register always reads as zero. Counting starts internally when this register is written with a nonzero value. CAL_COUNTER_DONE goes immediately low to indicate that the counter has started and will be asserted when the counters are done. Do not write this field unless CAL_COUNTER_DONE==1. Both clocks must be running or the measurement will not complete. A stalled counter can be recovered by selecting valid clocks, waiting until the measurement completes, and discarding the first result. CAL_COUNTER1 should always be > 1. Due to internal clock synchronization CAL_COUNTER1 should be at least 5 times the 1/F_cnt2.
31	CAL_COUNTER_DONE	R	W	1	Status bit indicating that the internal counter #1 is finished counting and CLK_CAL_CNT2.COUNTER stopped counting up

16.2.5 CLK_CAL_CNT2

Description: Clock Calibration Counter 2
Address: 0x40030020
Offset: 0x20
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CAL_COUNTER2 [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CAL_COUNTER2 [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	CAL_COUNTER2	R	RW	0	Up-counter clocked on DFT output #1 (see CLK_DFT_SELECT). When CLK_CAL_CNT1.CAL_COUNTER_DONE==1, the counter is stopped and can be read by SW. Do not read this value unless CAL_COUNTER_DONE==1. The expected final value is related to the ratio of clock frequencies used for the two counters and the value loaded into counter 1: CLK_CAL_CNT2.CAL_COUNTER2=(F_cnt2/F_cnt1)*(CLK_CAL_CNT1.CAL_COUNTER1)

16.2.6 CLK_SELECT

Description: Clock Select Register (Lock Protected)
Address: 0x40030028
Offset: 0x28
Retention: Retained
IsDeepSleep: No
Comment: Configures direction of all clock multiplexers and selectors. See clock startup times for clock sources for wait periods before switching to them. Selecting a clock source that is not supported/not enabled will result in undefined behavior. It takes about 3 cycles of the new selected clock to switch away from the old clock to the new clock. Do not disable the original clock during this time.
Default: 0x8

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SYSCLK_DIV [7:6]		PUMP_SEL [5:4]		HFCLK_DIV [3:2]		HFCLK_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:9]							LFCLK _SEL [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	HFCLK_SEL	RW	R	0	Selects a source for clk_hf and dsi_in[0]. Note that not all products support all clock sources. Selecting a clock source that is not supported or enabled will result in undefined behavior. It takes about 3 cycles of the new selected clock to switch away from the old clock to the new clock. Do not disable the original clock during this time.
	IMO			0	IMO - Internal R/C Oscillator
	EXTCLK			1	EXTCLK - External Clock Pin
	ECO			2	ECO - External-Crystal Oscillator or PLL subsystem output
	HPOSC			3	HPOSC - High Precision Oscillator. Only if HPOSC_PRESENT=1
2:3	HFCLK_DIV	RW	R	2	Selects clk_hf predivider value. It will take 3-4 clock cycles to switch to the new predivder value
	NO_DIV			0	Transparent mode, feed through selected clock source w/o dividing.
	DIV_BY_2			1	Divide selected clock source by 2
	DIV_BY_4			2	Divide selected clock source by 4
	DIV_BY_8			3	Divide selected clock source by 8
4:5	PUMP_SEL	RW	R	0	Selects clock source for charge pump clock. This clock is not guaranteed to be glitch free when changing any of its sources or settings.
	GND			0	No clock, connect to gnd
	IMO			1	Use main IMO output
	HFCLK			2	Use clk_hf (using selected source after predivider but before prescaler)
6:7	SYSCLK_DIV	RW	R	0	Select clk_sys prescaler value.

Bits	Name	SW	HW	Default or Enum	Description
	NO_DIV			0	clk_sys= clk_hf/1
	DIV_BY_2			1	clk_sys= clk_hf/2
	DIV_BY_4			2	clk_sys= clk_hf/4
	DIV_BY_8			3	clk_sys= clk_hf/8
8	LFCLK_SEL	RW	A	0	Low Frequency Clock Select. Selecting a clock source that is not enabled will result in undefined behavior. If a clock source is disabled while selected, then the clock merely stops to all sources that receive it. In such a scenario, the disabled clock must be re-enabled, prior to switching FROM this clock source. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. It takes about 3 cycles of the new selected clock to switch away from the old clock to the new clock. Do not disable the original clock during this time. This register field resets with hard reset (power related, XRES, WDT).
	ILO			0	ILO - Internal Low Frequency Oscillator
	PILO			1	PILO - Precision Internal Low Frequency Oscillator. Only if PILO_PRESENT=1

16.2.7 CLK_ILO_CONFIG

Description: ILO Configuration (Lock Protected)
Address: 0x4003002C
Offset: 0x2C
Retention: Retained
IsDeepSleep: No
Comment: Internal slow speed R/C oscillator (32kHz) configuration register.
Default: 0x80000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLE [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
31	ENABLE	RW	A	1	Master enable for ILO oscillator. Clearing this bit will disable the ILO. Do not disable this clock if the CLK_LF uses it clock the source. Writes to this field are ignored when LFCLK_SEL is using this clock as the source and WDT is locked using WDT_LOCK register. This register resets when there is power related reset POR/XRES/BOD/OVD/WDT

16.2.8 CLK_IMO_CONFIG

Description: IMO Configuration (Lock Protected)
Address: 0x40030030
Offset: 0x30
Retention: Retained
IsDeepSleep: No
Comment: Internal high speed R/C oscillator configuration register. Note that this oscillator comes up active on power up. The oscillator provides the primary system clock (HFCLK) on power up until firmware configures differently. This oscillator is also used before system start to count out power up delays. This is done in fast IMO (FIMO) mode that does not require any external references and runs at a fixed 12MHz.
Default: 0x80000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLE [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
31	ENABLE	RW	R	1	Master enable for IMO oscillator. Clearing this bit will disable the IMO. Don't do this if the system is running off it.

16.2.9 CLK_DFT_SELECT

Description: Clock DFT Mode Selection Register
Address: 0x40030034
Offset: 0x34
Retention: Retained
IsDeepSleep: No
Comment: Selects which clock sources to route to the Calibration Counters.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:7]	DFT_EDGE0 [6:6]	DFT_DIV0 [5:4]		DFT_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:15]	DFT_EDGE1 [14:14]	DFT_DIV1 [13:12]		DFT_SEL1 [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	DFT_SEL0	RW	R	0	Select clock for Calibration Counter #1
	NC			0	Disabled - output is 0
	ILO			1	ILO output
	IMO			2	IMO output
	ECO			3	ECO output (if available)
	EXTCLK			4	External clock input
	HFCLK			5	Not appropriate for use with calibration counters
	LFCLK			6	Not appropriate for use with calibration counters
	SYSCLK			7	Not appropriate for use with calibration counters
	PUMPCLK			8	Not appropriate for use with calibration counters
	SLPCTRLCLK			9	Not appropriate for use with calibration counters
	HPOSC			10	HPOSC output. Applicable only if HPOSC_PRESENT=1
	PILO			11	PILO output. Applicable only if PILO_PRESENT=1
	ILO_EN			12	Not appropriate for use with calibration counters
	IMO_EN			13	Not appropriate for use with calibration counters
	HPOSC_EN			14	Not appropriate for use with calibration counters
	PILO_EN			15	Not appropriate for use with calibration counters
4:5	DFT_DIV0	RW	R	0	Calibration Counter #1 pre-divider
	NO_DIV			0	Direct Output
	DIV_BY_2			1	Divide by 2
	DIV_BY_4			2	Divide by 4
	DIV_BY_8			3	Divide by 8
6	DFT_EDGE0	RW	R	0	Edge sensitivity for pre-divider (only relevant when DIV0>0).
	POSEDGE			0	Use posedge for divider
	NEGEDGE			1	Use negedge for divider

Bits	Name	SW	HW	Default or Enum	Description
8:11	DFT_SEL1	RW	R	0	Select clock for Calibration Counter #2
	NC			0	Disabled - output is 0
	ILO			1	ILO output
	IMO			2	IMO output
	ECO			3	ECO output (if available)
	EXTCLK			4	External clock input
	HFCLK			5	Not appropriate for use with calibration counters
	LFCLK			6	Not appropriate for use with calibration counters
	SYSCLK			7	Not appropriate for use with calibration counters
	PUMPCLK			8	Not appropriate for use with calibration counters
	SLPCTRLCLK			9	Not appropriate for use with calibration counters
	HPOSC			10	HPOSC output. Applicable only if HPOSC_PRESENT=1
	PILO			11	PILO output. Applicable only if PILO_PRESENT=1
	ILO_EN			12	Not appropriate for use with calibration counters
	IMO_EN			13	Not appropriate for use with calibration counters
	HPOSC_EN			14	Not appropriate for use with calibration counters
	PILO_EN			15	Not appropriate for use with calibration counters
12:13	DFT_DIV1	RW	R	0	Calibration Counter #2 pre-divider
	NO_DIV			0	Direct Output
	DIV_BY_2			1	Divide by 2
	DIV_BY_4			2	Divide by 4
	DIV_BY_8			3	Divide by 8
14	DFT_EDGE1	RW	R	0	Edge sensitivity for pre-divider (only relevant when DIV0>0).
	POSEDGE			0	Use posedge for divider
	NEGEDGE			1	Use negedge for divider

16.2.10 SRSS_MASKED

Description: SRSS Interrupt Masked Register
Address: 0x40030040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment: Bitwise 'AND' between the interrupt request and mask registers so firmware can read the status of all mask enabled interrupt causes with a single load operation
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CRWDT [4:4]	CLK_CAL [3:3]	LIFETIME_ WAKEUP [2:2]	TEMP _HIGH [1:1]	None [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
1	TEMP_HIGH	R	RW	0	Logical and of corresponding request and mask bits.
2	LIFETIME_WAKEUP	R	RW	0	Logical and of corresponding request and mask bits.
3	CLK_CAL	R	RW	0	Logical and of corresponding request and mask bits.
4	CRWDT	R	RW	0	Logical and of corresponding request and mask bits.

16.2.11 SRSS_INTR

Description: SRSS Interrupt Register
Address: 0x40030044
Offset: 0x44
Retention: Retained
IsDeepSleep: No
Comment: Interrupt signals from SRSS
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CRWDT [4:4]	CLK_CAL [3:3]	LIFETIME_ WAKEUP [2:2]	TEMP _HIGH [1:1]	None [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
1	TEMP_HIGH	RW1C	A	0	Regulator over-temp interrupt. This interrupt can occur when a short circuit exists on the vccd pin or when extreme loads are applied on IO-cells causing the die to overheat. Firmware is encourage to shutdown all IO cells and then go to DeepSleep mode when this interrupt occurs if protection against such conditions is desired.
2	LIFETIME_WAKEUP	RW1C	A	0	Wakeup Interrupt from LIFETIME Counter. This bit is set when LIFETIME_COUNTER ==LIFETIME_WAKEUP. This is a DeepSleep Interrupt. The interrupt source will reset only with hard reset (power related, XRES, WDT).
3	CLK_CAL	RW1C	A	0	Clock calibration counter is done. This field is reset during DeepSleep mode.
4	CRWDT	RW1C	A	0	Interrupt from CRWDT. This bit is set by the CRWDT when enabled by CRWDT_CONFIG.

16.2.12 SRSS_INTR_SET

Description: SRSS Interrupt Set Register
Address: 0x40030048
Offset: 0x48
Retention: Retained
IsDeepSleep: No
Comment: Can be used to set interrupts for firmware testing.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CRWDT [4:4]	CLK_CAL [3:3]	LIFETIME_ WAKEUP [2:2]	TEMP _HIGH [1:1]	None [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
1	TEMP_HIGH	RW1S	A	0	Writing 1 to this bit internally sets the overtemp interrupt. This can be observed by reading SRSS_INTR.TEMP_HIGH. This bit always reads back as zero.
2	LIFETIME_WAKEUP	RW1S	A	0	Writing 1 to this bit internally sets the LIFETIME_WAKEUP interrupt. Reads back same as SRSS_INTR.LIFETIME_WAKEUP. The interrupt source will reset only with hard reset (power related, XRES, WDT).
3	CLK_CAL	RW1S	A	0	Set interrupt for clock calibration counter done. This field is reset during DeepSleep mode. Reads back same as SRSS_INTR.CLK_CAL.
4	CRWDT	RW1S	A	0	Set interrupt for Challenge/Response Interrupt. Reads back same as SRSS_INTR.CRWDT.

16.2.13 SRSS_INTR_MASK

Description: SRSS Interrupt Mask Register
Address: 0x4003004C
Offset: 0x4C
Retention: Retained
IsDeepSleep: No
Comment: Controls whether interrupt is forwarded to CPU.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CRWDT [4:4]	CLK_CAL [3:3]	LIFETIME_ WAKEUP [2:2]	TEMP _HIGH [1:1]	None [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
1	TEMP_HIGH	RW	R	0	Masks REG_OVERTEMP interrupt
2	LIFETIME_WAKEUP	RW	R	0	Mask for lifetime counter
3	CLK_CAL	RW	R	0	Mask for clock calibration done
4	CRWDT	RW	R	0	Mask for CRWDT interrupt

16.2.14 RES_CAUSE

Description: Reset Cause Observation Register
Address: 0x40030054
Offset: 0x54
Retention: Retained
IsDeepSleep: No
Comment: Indicates the cause for the latest reset(s) that occurred in the system. All bits in this register assert when the corresponding reset cause occurs and must be cleared by firmware. Low-voltage cause bits are reset whenever the low-voltage supply is initialized, including XRES, POR, brown-out, WDT.

High-voltage cause bit: caused by condition that could involve or imply loss of system state
- BOD/OVD because we are operating outside of the timing closure window
- WDT because the lack of servicing could imply a fundamental problem causing loss of state

Low-voltage cause bit: typically caused by soft errors
- CRWDT because processor might have lost state
- Fault, likely due to multiple bit ECC error
- Soft reset requested by the processor

Default: 0x40000000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			RESET_SOFT [4:4]	RESET_PROT_FAULT [3:3]	None [2:2]	RESET_ACT_FAULT [1:1]	RESET_WDT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						RESET_CRWDT [9:9]	None [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:23]	RESET_OVD VCCD [22:22]	None [21:21]	RESET_OVD VDDD [20:20]	RESET_BOD VCCD [19:19]	None [18:18]	RESET_BOD VDDD [17:17]	RESET_XRES [16:16]

Bits	31	30	29	28	27	26	25	24
Name	None [31:31]	RESET_POR VDDD [30:30]	None [29:25]					RESET_BODHVSS [24:24]

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	RESET_WDT	RW1C	A	0	A WatchDog Timer reset has occurred since last power cycle. This is a high-voltage cause detection, this bit blocks recording of other high-voltage cause bits, except RESET_PORVDDD and XRES. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits.
1	RESET_ACT_FAULT	RW1C	A	0	Reset caused by the Fault Infrastructure. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above).

Bits	Name	SW	HW	Default or Enum	Description
3	RESET_PROT_FAULT	RW1C	A	0	A protection violation occurred that requires a RESET. This includes, but is not limited to, hitting a debug breakpoint while in Privileged Mode.
4	RESET_SOFT	RW1C	A	0	Cortex-M0 requested a system reset through it's SYSRESETREQ. This can be done via a debugger probe or in firmware.
9	RESET_CRWDT	RW1C	A	0	Challenge/Response Watchdog reset. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above).
16	RESET_XRES	RW1C	A	0	External XRES pin was asserted. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits.
17	RESET_BODVDDD	RW1C	A	0	Internal VDDD supply crossed brown-out limit. Note that this cause will only be observable as long as the VDDD supply does not go below the POR (power on reset) detection limit. Below this limit it is not possible to reliably retain information in the device. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD and RESET_XRES. Hardware clears this bit during POR.
19	RESET_BODVCCD	RW1C	A	0	Internal VCCD core supply crossed the brown-out limit. Note that this detector will detect gross issues with the internal core supply, but may not catch all brown-out conditions. Functional and timing supervision (CSV, WDT) is provided to create fully failsafe internal crash detection. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD and RESET_XRES. Hardware clears this bit during POR.
20	RESET_OVDVDDD	RW1C	A	0	Overvoltage detection on the external VDDD supply. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD and RESET_XRES. Hardware clears this bit during POR.
22	RESET_OVDVCCD	RW1C	A	0	Overvoltage detection on the internal core VCCD supply. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD and RESET_XRES. Hardware clears this bit during POR.
24	RESET_BODHVSS	RW1C	A	0	Internal VDDD supply crossed brown-out limit. Note that this cause will only be observable as long as the VDDD supply does not go below the POR (power on reset) detection limit. Below this limit it is not possible to reliably retain information in the device. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD and RESET_XRES. Hardware clears this bit during POR. This detector is a backup detector in the high voltage sub-system that is on even in deep sleep. This detector is used for engineering debug purposes only.
30	RESET_PORVDDD	RW1C	A	1	Indicator that a POR occurred. This is a high-voltage cause bit, and hardware clears the other bits when this one is set. It does not block further recording of other high-voltage causes.

16.2.15 REG_PROT

Description: Register Protection
Address: 0x40030080
Offset: 0x80
Retention: Retained
IsDeepSleep: No
Comment: Unlocks access to Lock Protected Registers when the Magic Number is written into the register.
Default: 0xF08169E7

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	MAGIC [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	MAGIC [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	MAGIC [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	MAGIC [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	MAGIC	RW	R	4035013095	Setting this register to the value 0xf08169e7 unlocks access to Lock Protected Registers. These registers can not be written to unless this value has been written into this register. Writing a value OTHER than the magic key will disable access to the registers. The register POR value is set to 'unlock' the register access. The registers locked are PWR_CONTROL, PWR_KEY_DELAY, CLK_SELECT, CLK_ILO_CONFIG, CLK_IMO_CONFIG, CRWDT_CTL, CRWDT_EARLY, PWR_SSV_CTL, CRWDT_WARN, CRWDT_LATE, LIFETIME_CTL,HPOSC_CTL(if HPOSC_PRESENT=1), PILO_CTL(if PILO_PRESENT=1), and all trim registers

16.2.16 CRWDT_CTL

Description: Challenge Response WatchDog Control (Lock Protected)
Address: 0x40030090
Offset: 0x90
Retention: Retained
IsDeepSleep: No
Comment: Window WatchDog Control Register - locked when REG_PROT.MAGIC != Magic Number
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	STATUS _ENABLED [30:30]	None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
30	STATUS_ENABLED	R	RW	0	Indicates actual state of CRWDT enable. May lag ENABLED by up to one clk_lf cycles.
31	ENABLED	RW	R	0	When set to '1' enables Challenge/Response WatchDog Timer to Count. Will require 2 clk_lf cycles to take effect.

16.2.17 CRWDT_CHALLENGE

Description: Challenge Response WatchDog Challenge Value
Address: 0x40030094
Offset: 0x94
Retention: Retained
IsDeepSleep: No
Comment: Challenge register for Windowed WatchDog.
Default: 0xFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CHALLENGE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	CHALLENGE	R	RW	255	Challenge/Response WatchDog Challenge value. Implements the LFSR CCRC8-AutoSar using the polynomial x^8+x^5+x^3+x^2+x+1. The next value in the LFSR sequence is used to compare against the value subsequently written to the CRWDT_RESPONSE register. Incremented by write to CRWDT_RESPONSE to LFSR value next in the LFSR sequence after the value written to CRWDT_RESPONSE. Also incremented each time this register before a response is written to CRWDT_RESPONSE.

16.2.18 CRWDT_RESPONSE

Description: Challenge Response WatchDog Response Value
Address: 0x40030098
Offset: 0x98
Retention: Retained
IsDeepSleep: No
Comment: Response register for Windowed WatchDog
Default: 0xFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	RESPONSE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	RESPONSE	RW	R	255	Challenge/Response WatchDog Response value. Value is compared against the expected next value in the LFSR sequence following the value obtained from CRWDT_CHALLENGE. If the values match, the CRWDT_UPCNT resets. If the values miscompare, the action selected by CRWDT_CONFIG.CHALLENGE_FAIL_ACTION occurs.

16.2.19 CRWDT_UPCNT

Description: Challenge Response WatchDog Up Counter
Address: 0x4003009C
Offset: 0x9C
Retention: Retained
IsDeepSleep: No
Comment: Response register for Windowed WatchDog
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	UPCNT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	UPCNT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	UPCNT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:23	UPCNT	R	RW	0	Challenge/Response WatchDog Up Counter. The counter upcounts upon every clk_lf occurrence when enabled. If a match occurs between CRWDT_CHALLENGE and CRWDT_RESPONSE, the counter resets. If there is a mismatch, the action is taken selected by CRWDT_CONFIG.CHALLENGE_FAIL_ACTION. The counter will also reset when CRWDT_UPCNT=CRWDT_LATE. CRWDT_CTL.ENABLED=0 - Counter reset CRWDT_CTL.ENABLED=1 - Counter Increments

16.2.20 CRWDT_EARLY

Description: Challenge Response WatchDog Early Limit (Lock Protected)
Address: 0x400300A0
Offset: 0xA0
Retention: Retained
IsDeepSleep: No
Comment: Windowed WatchDog Early Count value
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	EARLY [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	EARLY [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	EARLY [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:23	EARLY	RW	R	0	Challenge/Response Early Value will cause the action selected by CRWDT_CONFIG.EARLY_ACTION if CRWDT_UPCNT < CRWDT_EARLY and there is a CRWDT_CHALLENGE/CRWDT_RESPONSE match. Writes to this register are ignored when CRWDT_CTL.ENABLED<>0.

16.2.21 CRWDT_WARN

Description: Challenge Response WatchDog Warning Limit (Lock Protected)
Address: 0x400300A4
Offset: 0xA4
Retention: Retained
IsDeepSleep: No
Comment: Windowed WatchDog Warning Value
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	WARNING [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	WARNING [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	WARNING [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:23	WARNING	RW	R	0	Challenge/Response Warning Value will cause the action selected by CRWDT_CONFIGWARN_ACTION if CRWDT_UPCNT>CRWDT_WARN and there is a CRWDT_CHALLENGE/CRWDT_RESPONSE match. Writes to this register are ignored when CRWDT_CTL.ENABLED<>0.

16.2.22 CRWDT_LATE

Description: Challenge Response WatchDog Late Limit (Lock Protected)
Address: 0x400300A8
Offset: 0xA8
Retention: Retained
IsDeepSleep: No
Comment: Windowed WatchDog Late Value
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	LATE [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	LATE [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	LATE [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:23	LATE	RW	R	0	Challenge/Response Late Value will cause action selected by CRWDT_CONFIG.LATE_ACTION if CRWDT_UPCNT = CRWDT_LATE. Writes to this register are ignored when CRWDT_CTL.ENABLED<>0.

16.2.23 CRWDT_CONFIG

Description: Challenge Response WatchDog Configuration
Address: 0x400300AC
Offset: 0xAC
Retention: Retained
IsDeepSleep: No
Comment: Configuration for watchdog.
Default: 0x810

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			LATE_ACTION [4:4]	None [3:1]			EARLY_ACTION [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				CHALLENGE_FAIL_ACTION [11:11]	None [10:9]		WARN_ACTION [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	DEBUG_RUN [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	EARLY_ACTION	RW	A	0	Action taken if this watchdog when the proper response is written to CRWDT_RESPONSE before CRWDT_UPCNT reaches CRWDT_EARLY. EARLY_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected. For CRWDT_EARLY > CRWDT_UPCNT: The action is triggered on same edge as when it meets this condition. For CRWDT_EARLY <= CRWDT_UPCNT: No action is triggered. Writes to this register are ignored when CRWDT_CTL.ENABLED<>0.
	NOTHING			0	Do nothing
	FAULT_AND_INT			1	Trigger a Fault and interrupt
4	LATE_ACTION	RW	A	1	Action taken if this watchdog is not serviced before CRWDT_LATE s reached. The counter resets CRWDT_UPCNT when CRWDT_LATE is reached, regardless of CRWDT_CONFIG.LATE_ACTION setting. LATE_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected. For CRWDT_LATE == CRWDT_UPCNT: The action is triggered on same edge as when it meets this condition. For CRWDT_LATE > CRWDT_UPCNT: No action is taken Writes to this register are ignored when CRWDT_CTL.ENABLED<>0.

Bits	Name	SW	HW	Default or Enum	Description
	NOTHING			0	Do nothing
	FAULT_RESET			1	Trigger a fault. Further, trigger a system-wide reset if the CRWDT is not disabled within 6 clk_lf cycles.
8	WARN_ACTION	RW	A	0	Action taken if this watchdog when the proper response is written to CRWDT_RESPONSE and CRWDT_UPCNT reaches CRWDT_WARN and CRWDT_UPCNT<CRWDT_LATE. WARN_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected. For CRWDT_WARN == CRWDT_UPCNT && CRWDT_LATE > CRWDT_UPCNT: The action is triggered on same edge as when it meets this condition. For CRWDT_WARN <CRWDT_UPCNT: No action is triggered. Writes to this register are ignored when CRWDT_CTL.ENABLED<>0.
	NOTHING			0	Do nothing
	FAULT_AND_INT			1	Trigger a Fault and interrupt
11	CHALLENGE_FAIL_ACTION	RW	A	1	Action taken when a failed response occurs, i.e. the expected LFSR value is different than the expected value. Writes to this register are ignored when CRWDT_CTL.ENABLED<>0.
	NOTHING			0	Do nothing
	RESET			1	Trigger a reset
31	DEBUG_RUN	RW	A	0	Pauses/runs this counter while a debugger is connected. Other behaviors are unchanged during debugging, including service, configuration updates and enable/disable. Note it may take up to two clk_lf cycles for the counter to pause and another two cycles to unpause, due to internal synchronization. If the debugger is connected for at least two clk_lf cycles, the EARLY_ACTION is ignored until after the first service after the debugger is disconnected. This prevents an unintentional trigger of the EARLY_ACTION before the firmware realigns the servicing period. After the first service, EARLY_ACTION behaves as configured. If the debugger is disconnected before two clk_lf cycles, the EARLY_ACTION may or may not be ignored. 0: When debugger connected, counter pauses incrementing. 1: When debugger connected, counter increments normally, but reset generation is blocked. Writes to this register are ignored when CRWDT_CTL.ENABLED<>0.

16.2.24 LIFETIME_CTL

Description: Liftetime Counter Control (Lock Protected)
Address: 0x400300B0
Offset: 0xB0
Retention: Retained
IsDeepSleep: No
Comment: This register resets with hard reset (power related, XRES, WDT).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					PRESEL [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLED [31:31]	STATUS _ENABLED [30:30]	None [29:24]					

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	PRESEL	RW	A	0	Select Divide ratio for Preselector. Legal values are 0-4. Values 5, 6, and 7 yield the same result as PERSEL_DIV32. Do not change this setting when lifetime counter is enabled (LIFETIME_CTL.ENABLED=1). Due to internal synchronization, it takes about 1 LFCLK cycles to update the counters after a write to this register. This register bit only resets for XRES, POR, or a detected BOD.
	PRESEL_DIV2			0	Divide CLK_LF by 2
	PRESEL_DIV4			1	Divide CLK_LF by 4
	PRESEL_DIV8			2	Divide CLK_LF by 8
	PRESEL_DIV16			3	Divide CLK_LF by 16
	PRESEL_DIV32			4	Divide CLK_LF by 32
30	STATUS_ENABLED	R	RW	0	Indicates actual state of lifetime counter enable. May lag ENABLED by up to one clk_lf cycles.
31	ENABLED	RW	A	0	When set to '1' enables LIFETIME_COUNTER to increment. Due to internal synchronization, may take up to one clk_lf cycles to take effect. The synchronization can be checked by waiting until ENABLED==STATUS_ENABLED whenever ENABLED is changed. When ENABLE changes from 1->0, the counter can be loaded with new COUNT value. Refer to LIFETIME_COUNTER.COUNT for details. User can enter DeepSleep without waiting for synchronization to complete (ENABLED==STATUS_ENABLED). This register bit only resets for XRES, POR, or a detected BOD.

16.2.25 LIFETIME_WAKEUP

Description: Lifetime Wakeup Value
Address: 0x400300B4
Offset: 0xB4
Retention: Retained
IsDeepSleep: No
Comment: This register resets with hard reset (power related, XRES, WDT).
Default: 0xFFFFFFFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	WAKEUP [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	WAKEUP [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	WAKEUP [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	WAKEUP [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	WAKEUP	RW	A	4294967295	Compare the WAKEUP value against LIFETIME_COUNTER. If they are equal interrupt_wakeup to set. Due to internal synchronization, it may take up to 1 LFCLK cycles to update the counters after a write to this register. This register bit only resets for XRES, POR, or a detected BOD.

16.2.26 LIFETIME_COUNTER

Description: Lifetime Counter Current Value
Address: 0x400300B8
Offset: 0xB8
Retention: Retained
IsDeepSleep: No
Comment: This register resets with hard reset (power related, XRES, WDT).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	COUNT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	COUNT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	COUNT	RW	A	0	Lifetime Counter which clocks on the output of the CLK_LF PreScalar output controlled by LIFETIME_CTL.PRESEL. The counter doesn't increment unless LIFETIME_CTL.STATUS_ENABLED =1. FW is responsible for initializing this value after reset and maintaining the running value. SW writes will be ignored when LIFETIME_CTL.ENABLED=1. The counter needs to be disabled one LFCLK cycle (or LIFETIME_CTL.STATUS_ENABLED=0) for the internal synchronization of this field to take place. This register bit only resets for XRES, POR, or a detected BOD.

16.2.27 PWR_SSV_CTL

Description: Supply Supervisory Control Register (Lock Protected)
Address: 0x400300E0
Offset: 0xE0
Retention: Retained
IsDeepSleep: No
Comment: Controls for brownout and over-voltage detectors. This register resets with hard reset (power related, XRES, WDT).
Default: 0x808

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				BODVDDD_ENABLE [3:3]	None [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				BODVCCD_ENABLE [11:11]	None [10:8]		

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				OVDVDDD_ENABLE [19:19]	None [18:16]		

Bits	31	30	29	28	27	26	25	24
Name	BODHVSS_ENABLE [31:31]	None [30:28]			OVDVCCD_ENABLE [27:27]	None [26:24]		

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
3	BODVDDD_ENABLE	RW	A	1	Enable for BOD on vddd. This cannot be disabled during normal operation.
11	BODVCCD_ENABLE	RW	A	1	Enable for BOD on vccd. This cannot be disabled during normal operation.
19	OVDVDDD_ENABLE	RW	A	0	Enable for OVD on vddd. FW should enable this after the OVD trims are set during boot-up and keep it enabled.
27	OVDVCCD_ENABLE	RW	A	0	Enable for OVD on vccd. FW should enable this after the OVD trims are set during boot-up and keep it enabled.
31	BODHVSS_ENABLE	RW	A	0	Enable for BOD on vddd from HVSS. This gives BOD robustness during DeepSleep. FW should enable during boot-up and keep it enabled.

16.2.28 PWR_SSV_STATUS

Description: Supply Supervision Status Register
Address: 0x400300E4
Offset: 0xE4
Retention: Retained
IsDeepSleep: No
Comment: Status for brownout and over-voltage detectors.
Default: 0x1005

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					BODVCCD_OK [2:2]	None [1:1]	BODVDDD_OK [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			BODHVSS_OK [12:12]	None [11:11]	OVDVCCD_OK [10:10]	None [9:9]	OVDVDDD_OK [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	BODVDDD_OK	R	RW	1	BOD indicates vddd is ok. This will always read 1, because a detected brownout will reset the chip.
2	BODVCCD_OK	R	RW	1	BOD indicates vccd is ok. This will always read 1, because a detected brownout will reset the chip.
8	OVDVDDD_OK	R	RW	0	OVD indicates vddd is ok. After OVDVDDD is enabled it will always read 1, because a detected over-voltage condition will reset the chip.
10	OVDVCCD_OK	R	RW	0	OVD indicates vccd is ok. After OVDVCCD is enabled it will always read 1, because a detected over-over-voltage condition will reset the chip.
12	BODHVSS_OK	R	RW	1	BODHVSS indicates vddd is ok. This will always read 1, because a detected brownout will reset the chip.

16.2.29 HPOSC_CTL

Description: High Precision Oscillator Control (Lock Protected)
Address: 0x40030300
Offset: 0x300
Retention: Retained
IsDeepSleep: No
Comment: High Precision Osc Control
Default: 0x1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CTAT_SWB [4:4]	None [3:2]		CTAT_SEL [1:1]	LEAKC _DIS [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	IMO_EN [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	LEAKC_DIS	RW	R	1	RESERVED
1	CTAT_SEL	RW	R	0	CTAT generator selection, only valid when CTAT_SW = 1. 0 - Low noise type CTAT generator 1 - Fast start-up type CTAT generator
4	CTAT_SWB	RW	R	0	Selection control for internal CTAT generator. 0 - Auto Select (Fast start followed by low noise generator) 1 - Generator selected by CTAT_SEL
31	IMO_EN	RW	R	0	HPOSC enable. Setting this bit will enable the HPOSC and clearing this bit will disable the HPOSC. Don't disable this clock if the system is using this clock as the source.

16.2.30 PILO_CTL

Description: Precision Low Power Oscillator Control (Lock Protected)
Address: 0x40030400
Offset: 0x400
Retention: Retained
IsDeepSleep: No
Comment: Precision Low Power Oscillator Control.
Default: 0xC001

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			CTAT_SWB [4:4]	None [3:2]		CTAT_SEL [1:1]	LEAKC _DIS [0:0]

Bits	15	14	13	12	11	10	9	8
Name	TR_CAP [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ILO_EN [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	LEAKC_DIS	RW	R	1	RESERVED
1	CTAT_SEL	RW	R	0	CTAT generator selection, only valid when CTAT_SW = 1. 0 - Low noise type CTAT generator 1 - Fast start-up type CTAT generator
4	CTAT_SWB	RW	R	0	Selection control for internal CTAT generator. 0 - Auto Select (Fast start followed by low noise generator) 1 - Generator selected by CTAT_SEL
8:15	TR_CAP	RW	A	192	PILO user temperature fine trim. This register field resets with hard reset (power related, XRES, WDT)..
31	ILO_EN	RW	A	0	PILO enable. Setting this bit will enable the PILO and clearing this bit will disable it. Do not disable this clock prior to changing CLK_LF to use the PILO as a source. CLK_LF must be configured to use PILO as a source while the PILO clock is enabled prior to making such a change. Writes to this field are ignored when LFCLK_SEL is using this clock as the source and WDT is locked using WDT_LOCK register. Consequently, if CLK_LF is sourced by the PILO and the PILO is to be disabled, clear WDT_LOCK beforehand. This register field resets with hard reset (power related, XRES, WDT).

16.2.31 PWR_BG_TRIM1

Description: Bandgap Trim Register (Lock Protected)
Address: 0x4003FF00
Offset: 0xFF00
Retention: Retained
IsDeepSleep: No
Comment: Trim bits for Reference System
Default: 0xD

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		REF_VTRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	REF_VTRIM	RW	R	13	Trims the bandgap reference voltage output. Used to trim the VBG to the voltage where its temperature curvature is minimal. Bit [5] is unused within the bandgap block.

16.2.32 PWR_BG_TRIM2

Description: Bandgap Trim Register (Lock Protected)
Address: 0x4003FF04
Offset: 0xFF04
Retention: Retained
IsDeepSleep: No
Comment: Trim bits for Reference System
Default: 0x23

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		REF_ITRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:5	REF_ITRIM	RW	R	35	Trims the bandgap reference current output. Used to trim the IBG to the voltage where its temperature curvature is minimal.

16.2.33 CLK_IMO_SELECT

Description: IMO Frequency Select Register (Lock Protected)
Address: 0x4003FF08
Offset: 0xFF08
Retention: Retained
IsDeepSleep: No
Comment: Selects the operating frequency of the IMO
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					FREQ [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	FREQ	RW	R	0	Select operating frequency
	24_MHZ			0	IMO runs at 24 MHz
	28_MHZ			1	IMO runs at 28 MHz
	32_MHZ			2	IMO runs at 32 MHz
	36_MHZ			3	IMO runs at 36 MHz
	40_MHZ			4	IMO runs at 40 MHz
	44_MHZ			5	IMO runs at 44 MHz
	48_MHZ			6	IMO runs at 48 MHz

16.2.34 CLK_IMO_TRIM1

Description: IMO Trim Register (Lock Protected)
Address: 0x4003FF0C
Offset: 0xFF0C
Retention: Retained
IsDeepSleep: No
Comment: Trims IMO frequency to within datasheet accuracy, or allows for trimming IMO to frequency lock to a more accurate frequency source.
Default: 0x6C

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	OFFSET	RW	RW	108	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. This field is hardware updated during USB osclock mode. This field is mapped to the most significant bits of the IMO trim imo_clk_trim[10:3]. The step size of 1 LSB on this field is nominally 160 kHz.

16.2.35 CLK_IMO_TRIM2

Description: IMO Trim Register (Lock Protected)
Address: 0x4003FF10
Offset: 0xFF10
Retention: Retained
IsDeepSleep: No
Comment: IMO Trim Bits
Default: 0xA0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	TCTRIM [7:4]				None [3:3]	FSOFFSET [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	FSOFFSET	RW	RW	0	Frequency trim bits. These bits are not trimmed during manufacturing and kept at 0 under normal operation. This field is hardware updated during USB osclock mode. This field is mapped to the least significant bits of the IMO trim imo_clk_trim[2:0]. The step size of 1 LSB on this field is nominally 20 kHz.
4:7	TCTRIM	RW	R	10	IMO temperature compensation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Infineon provided frequency change algorithm.

16.2.36 CLK_IMO_TRIM3

Description: IMO Trim Register (Lock Protected)
Address: 0x4003FF14
Offset: 0xFF14
Retention: Retained
IsDeepSleep: No
Comment: IMO Trim Bits
Default: 0xF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			STEPSIZE [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	STEPSIZE	RW	R	15	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims.

16.2.37 PWR_PWRSYS_TRIM1

Description: Power System Trim Register (Lock Protected)
Address: 0x4003FF18
Offset: 0xFF18
Retention: Retained
IsDeepSleep: No
Comment: Power System Trim Bits
Default: 0x10

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	SPARE_TRIM [7:4]				DPSLP_REF_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	DPSLP_REF_TRIM	RW	R	0	Trims the DeepSleep reference that is used by the DeepSleep regulator and DeepSleep power comparator.
4:7	SPARE_TRIM	RW	R	1	Active-Reference temperature compensation trim (repurposed from spare bits). Bits [7:6] - trim the Active-Reference IREF temperature coefficient (TC). 00: TC = 0 (unchanged) 01: TC = +80ppm/C 10: TC = -80ppm/C 11: TC = -150ppm/C Bits [5:4] - trim the Active-Reference VREF temperature coefficient (TC). 00: TC = 0 (unchanged) 01: TC = -50ppm/C 10: TC = -80ppm/C 11: TC = +150ppm/C

16.2.38 TRIM_BODVCCD

Description: Brown Out Detect Trim (VCCD) (Lock Protected)
Address: 0x4003FF1C
Offset: 0xFF1C
Retention: Retained
IsDeepSleep: No
Comment: Power System Trim Bits. This register resets with hard reset (power related, XRES, WDT).
Default: 0x8

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			BOD_RANGE_SELECT_VCCD [4:4]	BOD_TRIPSEL_VCCD [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	BOD_TRIPSEL_VCCD	RW	A	8	BOD VCCD trim (production)
4	BOD_RANGE_SELECT_VCCD	RW	A	0	Range select between 1.6V Vs 1.69V nominal.

16.2.39 TRIM_OVDVCCD

Description: Over Voltage Detect Trim (VCCD) (Lock Protected)
Address: 0x4003FF20
Offset: 0xFF20
Retention: Retained
IsDeepSleep: No
Comment: Power System Trim Bits. This register resets with hard reset (power related, XRES, WDT).
Default: 0x7

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				OVD_TRIPSEL_VCCD [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	OVD_TRIPSEL_VCCD	RW	A	7	OVD VCCD trim (options)

16.2.40 TRIM_HPOSC0_CTL

Description: High Precision Oscillator Trim Control 0 (Lock Protected)
Address: 0x4003FF24
Offset: 0xFF24
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PTATEC [7:6]		CTATEC [5:4]		PTATEF [3:2]		CTATEF [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	CTATEF	RW	R	3	HPOSC frequency CTAT extra-fine trim
2:3	PTATEF	RW	R	3	Fine trim for HPOSC PTAT current
4:5	CTATEC	RW	R	0	Coarse trim for HPOSC CTAT current
6:7	PTATEC	RW	R	0	Coarse trim for HPOSC PTAT current

16.2.41 TRIM_HPOSC1_CTL

Description: High Precision Oscillator Trim Control 1 (Lock Protected)
Address: 0x4003FF28
Offset: 0xFF28
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			TCF [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	TCF	RW	R	13	HPOSC temp-co fine trim

16.2.42 TRIM_HPOSC2_CTL

Description: High Precision Oscillator Trim Control 2 (Lock Protected)
Address: 0x4003FF2C
Offset: 0xFF2C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xA4

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PTAT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	PTAT	RW	R	164	HPOSC PTAT trim

16.2.43 TRIM_HPOSC3_CTL

Description: High Precision Oscillator Trim Control 3 (Lock Protected)
Address: 0x4003FF30
Offset: 0xFF30
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CTAT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	CTAT	RW	R	177	HPOSC CTAT trim

16.2.44 TRIM_HPOSC4_CTL

Description: High Precision Oscillator Trim Control 4 (Lock Protected)
Address: 0x4003FF34
Offset: 0xFF34
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	HPOSC_LEAK [7:3]					TOC [2:0]		

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:2	TOC	RW	R	3	HPOSC temp-co coarse trim
3:7	HPOSC_LEAK	RW	R	0	HPOSC leakage cancellation trim

16.2.45 TRIM_PILO0_CTL

Description: Low Frequency Oscillator Trim Control 0 (Lock Protected)
Address: 0x4003FF38
Offset: 0xFF38
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PTATEC [7:6]		CTATEC [5:4]		PTATEF [3:2]		CTATEF [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	CTATEF	RW	A	0	PILO frequency CTAT extra-fine trim
2:3	PTATEF	RW	A	0	PILO frequency PTATextra-fine trim
4:5	CTATEC	RW	A	0	PILO temperature CTAT extra-coarse trim
6:7	PTATEC	RW	A	0	PILO temperature PTATextra-coarse trim

16.2.46 TRIM_PILO1_CTL

Description: Low Frequency Oscillator Trim Control 1 (Lock Protected)
Address: 0x4003FF3C
Offset: 0xFF3C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			TCF [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	TCF	RW	A	0	PILO temp-co fine trim (MSB, bit 4, is not used)

16.2.47 TRIM_PILO2_CTL

Description: Low Frequency Oscillator Trim Control 2 (Lock Protected)
Address: 0x4003FF40
Offset: 0xFF40
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PTAT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	PTAT	RW	A	0	PILO frequency PTAT coarse trim

16.2.48 TRIM_PILO3_CTL

Description: Low Frequency Oscillator Trim Control 3 (Lock Protected)
Address: 0x4003FF44
Offset: 0xFF44
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CTAT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:7	CTAT	RW	A	0	PILO frequency CTAT coarse trim

16.2.49 TRIM_PILO4_CTL

Description: Low Frequency Oscillator Trim Control 4 (Lock Protected)
Address: 0x4003FF48
Offset: 0xFF48
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				TCC [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	TCC	RW	A	0	PILO temperature coarse trim

16.2.50 TRIM_PILO5_CTL

Description: Low Frequency Oscillator Trim Control 5 (Lock Protected)
Address: 0x4003FF4C
Offset: 0xFF4C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			PILO_TR_LEAK [4:0]				

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:4	PILO_TR_LEAK	RW	A	0	PILO leakage cancellation trim

16.2.51 TRIM_BODVDDD

Description: Brown Out Detect Trim (VDDD) (Lock Protected)
Address: 0x4003FF50
Offset: 0xFF50
Retention: Retained
IsDeepSleep: No
Comment: Power System Trim Bits. This register resets with hard reset (power related, XRES, WDT).
Default: 0x8

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				BOD_TRIPSEL_VDDD [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	BOD_TRIPSEL_VDDD	RW	A	8	BOD VDDD trim (options)

16.2.52 TRIM_OVDVDDD

Description: Over Voltage Detect Trim (VDDD) (Lock Protected)
Address: 0x4003FF54
Offset: 0xFF54
Retention: Retained
IsDeepSleep: No
Comment: Power System Trim Bits. This register resets with hard reset (power related, XRES, WDT).
Default: 0x7

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			OVD_RANGE_SELECT_VDDD [4:4]	OVD_TRIPSEL_VDDD [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	OVD_TRIPSEL_VDDD	RW	A	7	OVD VDDD trim (options)
4	OVD_RANGE_SELECT_VDDD	RW	A	0	Range select between 3.8V Vs 5.77V nominal.

16.2.53 WDT

16.2.53.1 WDT_CTL

Description: WDT Control Register
Address: 0x40030100
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Control register for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0).
Default: 0x80000001

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							ENABLED [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	ENABLE [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	ENABLED	R	RW	1	Indicates actual state of watchdog. May lag ENABLE by up to three clk_lf cycles.
31	ENABLE	RW	A	1	Enable watchdog. May take up to three clk_lf cycles to take effect. When ENABLE changes from 1->0, the counter is cleared. Do not enter DeepSleep if ENABLE<>ENABLED. This can be done by waiting until ENABLE==ENABLED whenever ENABLE is changed. 0: Counter is disabled (not clocked). 1: Counter is enabled (counting up)

16.2.53.2 WDT_LOWER_LIMIT

Description: WDT Lower Limit Register
Address: 0x40030104
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: Lower limit for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	LOWER_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	LOWER_LIMIT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	LOWER_LIMIT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	LOWER_LIMIT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	LOWER_LIMIT	RW	A	0	Lower limit for watchdog. See LOWER_ACTION.

16.2.53.3 WDT_UPPER_LIMIT

Description: WDT Upper Limit Register
Address: 0x40030108
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment: Upper limit for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1).
Default: 0x8000

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	UPPER_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	UPPER_LIMIT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	UPPER_LIMIT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	UPPER_LIMIT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	UPPER_LIMIT	RW	A	32768	Upper limit for watchdog. See UPPER_ACTION.

16.2.53.4 WDT_WARN_LIMIT

Description: WDT Warn Limit Register
Address: 0x4003010C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment: Warn limit for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	WARN_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	WARN_LIMIT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	WARN_LIMIT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	WARN_LIMIT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	WARN_LIMIT	RW	A	0	Warn limit for watchdog. See WARN_ACTION.

16.2.53.5 WDT_CONFIG

Description: WDT Configuration Register
Address: 0x40030110
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: Configuration for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1).
Default: 0x10

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:5]			UPPER_ACTION [4:4]	None [3:1]			LOWER_ACTION [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:13]			AUTO_SERVICE [12:12]	None [11:9]			WARN_ACTION [8:8]

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	DEBUG_RUN [31:31]	None [30:30]	DPSLP_PAUSE [29:29]	DEBUG_TRIGGER_EN [28:28]	None [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	LOWER_ACTION	RW	A	0	Action taken if this watchdog is serviced before LOWER_LIMIT is reached. LOWER_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected and/or when the chip is in DeepSleep modes. For LOWER_LIMIT >= 1: The action is triggered on same edge when it meets this condition. For LOWER_LIMIT == 0: No action is triggered.
	NOTHING			0	Do nothing
	RESET			1	Trigger a reset.
4	UPPER_ACTION	RW	A	1	Action taken if this watchdog is not serviced before UPPER_LIMIT is reached. The counter stops counting when UPPER_LIMIT is reached, regardless of UPPER_ACTION setting. UPPER_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected. For UPPER_LIMIT >= 2: The action is triggered on same edge when it meets this condition. For UPPER_LIMIT < 2: The action may take up to one extra clk_lf cycle to trigger.
	NOTHING			0	Do nothing
	RESET			1	Trigger a reset.

Bits	Name	SW	HW	Default or Enum	Description
8	WARN_ACTION	RW	A	0	Action taken when the count value reaches WARN_LIMIT. The minimum setting to achieve a periodic interrupt is WARN_LIMIT==1. A setting of zero will trigger once but not periodically. For WARN_LIMIT >= 2: The action is triggered on same edge when it meets this condition. For WARN_LIMIT < 2 : The action may take up to one extra clk_lf cycle to trigger.
	NOTHING			0	Do nothing
	INT			1	Trigger an interrupt.
12	AUTO_SERVICE	RW	A	0	Automatically service when the count value reaches WARN_LIMIT. This allows creation of a periodic interrupt if this counter is not needed as a watchdog. This field is ignored when LOWER_ACTION<>NOTHING or when UPPER_ACTION<>NOTHING.
28	DEBUG_TRIGGER_EN	RW	A	0	Enables the trigger input for WDT to pause the counter during debug mode. To pause at a breakpoint while debugging, configure the trigger matrix to connect the related CPU halted signal to the trigger input for this WDT, and then set this bit. It takes up to two clk_lf cycles for the trigger signal to be processed. Triggers that are less than two clk_lf cycles may be missed. Synchronization error can accumulate each time it is halted. 0: Pauses the counter whenever a debug probe is connected. 1: Pauses the counter whenever a debug probe is connected and the trigger input is high.
29	DPSLP_PAUSE	RW	A	0	Pauses/runs this counter when the system is in DeepSleep. Note it may take up to two clk_lf cycles for the counter to pause, due to internal synchronization. During DeepSleep wakeup, the pause request is removed when clk_hf starts clocking, and then it may take up to two clk_lf cycles for the counter to start. After wakeup, the LOWER_ACTION is ignored until after the first service. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured. 0: Counter behaves normally during DeepSleep. 1: Counter pauses during DeepSleep.
31	DEBUG_RUN	RW	A	0	Pauses/runs this counter while a debugger is connected. Other behaviors are unchanged during debugging, including service, configuration updates and enable/disable. Note it may take up to two clk_lf cycles for the counter to pause and another two cycles to unpause, due to internal synchronization. If the debugger is connected for at least two clk_lf cycles, the LOWER_ACTION is ignored until after the first service after the debugger is disconnected. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured. If the debugger is disconnected before two clk_lf cycles, the LOWER_ACTION may or may not be ignored. 0: When debugger connected, counter pauses incrementing as configured in DEBUG_TRIGGER_EN. 1: When debugger connected, counter increments normally, but reset generation is blocked.

16.2.53.6 WDT_CNT

Description: WDT Count Register
Address: 0x40030114
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment: Count value for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1).
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	CNT [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	CNT [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:31	CNT	RW	A	0	Current value of subcounter for this WDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled.

16.2.53.7 WDT_LOCK

Description: WDT Lock register
Address: 0x40030140
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment: Lock or unlock the registers in this WDT
Default: 0x3

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						WDT_LOCK [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	WDT_LOCK	RW	A	3	Prohibits writing control and configuration registers related to this WDT when not equal 0 (as specified in the other register descriptions). Requires at least two different writes to unlock. Note that this field is 2 bits to force multiple writes only. This register also locks the clk_lf settings.
	NO_CHG			0	No effect
	CLR0			1	Clears bit 0
	CLR1			2	Clears bit 1
	SET01			3	Sets both bits 0 and 1

16.2.53.8 WDT_SERVICE

Description: WDT Service register
Address: 0x40030144
Offset: 0x44
Retention: Retained
IsDeepSleep: No
Comment: Control the behavior of the Watchdog counters. Writes to this register are ignored when LOCK.WDT_LOCK<>0. All fields in this register can be used while counter is in operation.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							SERVICE [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	SERVICE	RW1S	RW1C	0	Services the watchdog. This resets the count value to zero. This may take up to three clk_lf cycle to take effect. Hardware clears this bit, after necessary synchronization. To ensure a pending SERVICE write is reflected, firmware should wait until this bit reads low before attempting to write SERVICE=1. If WDT is disabled, SERVICE will not trigger a LOWER_ACTION and will not clear a preloaded count value.

16.2.53.9 WDT_INTR

Description: WDT Interrupt Register
Address: 0x40030150
Offset: 0x50
Retention: Retained
IsDeepSleep: No
Comment: Interrupt signal from WDT. Reset with power resets, xres and WDT
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							WDT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WDT	RW1C	A	0	WDT Interrupt Request. This bit is set as configured by WDT action and limits. Due to internal synchronization, it takes up to 8 SYSCLK cycles to update after a W1C or reading this register and during this time AHB bus is stalled.

16.2.53.10 WDT_INTR_SET

Description: WDT Interrupt Set Register
Address: 0x40030154
Offset: 0x54
Retention: Retained
IsDeepSleep: No
Comment: Can be used to set interrupts for firmware testing.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							WDT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WDT	RW1S	A	0	Set interrupt. Due to internal synchronization, it takes up to 8 SYSCLK cycles to update after a W1S or reading from this register and during this time AHB bus is stalled. Reads back same as WDT_B.INTR.WDT

16.2.53.11 WDT_INTR_MASK

Description: WDT Interrupt Mask Register
Address: 0x40030158
Offset: 0x58
Retention: Retained
IsDeepSleep: No
Comment: Controls whether interrupt is forwarded to CPU. All masks block the interrupt when 0 and forward the interrupt when 1
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							WDT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WDT	RW	R	0	Mask for watchdog timer. Clearing this bit will not forward the interrupt to the CPU.

16.2.53.12 WDT_INTR_MASKED

Description: WDT Interrupt Masked Register
Address: 0x4003015C
Offset: 0x5C
Retention: Retained
IsDeepSleep: No
Comment: Bitwise AND between the interrupt request and mask registers so firmware can read the status of all mask enabled interrupt causes with a single load operation
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							WDT [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	WDT	R	RW	0	Logical and of corresponding request and mask bits. Due to internal synchronization, it takes up to 8 SYSCLK cycles to read from this register. During this time AHB bus is stalled.

17 TCPWM

Description Timer/Counter/PWM
Base Address 0x40200000
Size 0x10000
Slave Num MMIO1

Register Name	Address	Permission	Description
TCPWM_CTRL	0x40200000	FULL	TCPWM control register 0.
TCPWM_CMD	0x40200008	FULL	TCPWM command register.
TCPWM_INTR_CAUSE	0x4020000C	FULL	TCPWM Counter interrupt cause register.

17.1 CNT 0

Register Name	Address	Permission	Description
TCPWM_CNT0_CTRL	0x40200100	FULL	Counter control register
TCPWM_CNT0_STATUS	0x40200104	FULL	Counter status register
TCPWM_CNT0_COUNTER	0x40200108	FULL	Counter count register
TCPWM_CNT0_CC	0x4020010C	FULL	Counter compare/capture register
TCPWM_CNT0_CC_BUFF	0x40200110	FULL	Counter buffered compare/capture register
TCPWM_CNT0_PERIOD	0x40200114	FULL	Counter period register
TCPWM_CNT0_PERIOD_BUFF	0x40200118	FULL	Counter buffered period register
TCPWM_CNT0_TR_CTRL0	0x40200120	FULL	Counter trigger control register 0
TCPWM_CNT0_TR_CTRL1	0x40200124	FULL	Counter trigger control register 1
TCPWM_CNT0_TR_CTRL2	0x40200128	FULL	Counter trigger control register 2
TCPWM_CNT0_INTR	0x40200130	FULL	Interrupt request register.
TCPWM_CNT0_INTR_SET	0x40200134	FULL	Interrupt set request register.
TCPWM_CNT0_INTR_MASK	0x40200138	FULL	Interrupt mask register.
TCPWM_CNT0_INTR_MASKED	0x4020013C	FULL	Interrupt masked request register

17.2 CNT 1

Register Name	Address	Permission	Description
TCPWM_CNT1_CTRL	0x40200140	FULL	Counter control register
TCPWM_CNT1_STATUS	0x40200144	FULL	Counter status register
TCPWM_CNT1_COUNTER	0x40200148	FULL	Counter count register
TCPWM_CNT1_CC	0x4020014C	FULL	Counter compare/capture register
TCPWM_CNT1_CC_BUFF	0x40200150	FULL	Counter buffered compare/capture register
TCPWM_CNT1_PERIOD	0x40200154	FULL	Counter period register
TCPWM_CNT1_PERIOD_BUFF	0x40200158	FULL	Counter buffered period register
TCPWM_CNT1_TR_CTRL0	0x40200160	FULL	Counter trigger control register 0
TCPWM_CNT1_TR_CTRL1	0x40200164	FULL	Counter trigger control register 1
TCPWM_CNT1_TR_CTRL2	0x40200168	FULL	Counter trigger control register 2
TCPWM_CNT1_INTR	0x40200170	FULL	Interrupt request register.
TCPWM_CNT1_INTR_SET	0x40200174	FULL	Interrupt set request register.
TCPWM_CNT1_INTR_MASK	0x40200178	FULL	Interrupt mask register.
TCPWM_CNT1_INTR_MASKED	0x4020017C	FULL	Interrupt masked request register

17.3 CNT 2

Register Name	Address	Permission	Description
TCPWM_CNT2_CTRL	0x40200180	FULL	Counter control register
TCPWM_CNT2_STATUS	0x40200184	FULL	Counter status register
TCPWM_CNT2_COUNTER	0x40200188	FULL	Counter count register
TCPWM_CNT2_CC	0x4020018C	FULL	Counter compare/capture register
TCPWM_CNT2_CC_BUFF	0x40200190	FULL	Counter buffered compare/capture register
TCPWM_CNT2_PERIOD	0x40200194	FULL	Counter period register
TCPWM_CNT2_PERIOD_BUFF	0x40200198	FULL	Counter buffered period register
TCPWM_CNT2_TR_CTRL0	0x402001A0	FULL	Counter trigger control register 0
TCPWM_CNT2_TR_CTRL1	0x402001A4	FULL	Counter trigger control register 1
TCPWM_CNT2_TR_CTRL2	0x402001A8	FULL	Counter trigger control register 2
TCPWM_CNT2_INTR	0x402001B0	FULL	Interrupt request register.
TCPWM_CNT2_INTR_SET	0x402001B4	FULL	Interrupt set request register.
TCPWM_CNT2_INTR_MASK	0x402001B8	FULL	Interrupt mask register.
TCPWM_CNT2_INTR_MASKED	0x402001BC	FULL	Interrupt masked request register

17.4 CNT 3

Register Name	Address	Permission	Description
TCPWM_CNT3_CTRL	0x402001C0	FULL	Counter control register
TCPWM_CNT3_STATUS	0x402001C4	FULL	Counter status register
TCPWM_CNT3_COUNTER	0x402001C8	FULL	Counter count register
TCPWM_CNT3_CC	0x402001CC	FULL	Counter compare/capture register
TCPWM_CNT3_CC_BUFF	0x402001D0	FULL	Counter buffered compare/capture register
TCPWM_CNT3_PERIOD	0x402001D4	FULL	Counter period register
TCPWM_CNT3_PERIOD_BUFF	0x402001D8	FULL	Counter buffered period register
TCPWM_CNT3_TR_CTRL0	0x402001E0	FULL	Counter trigger control register 0
TCPWM_CNT3_TR_CTRL1	0x402001E4	FULL	Counter trigger control register 1
TCPWM_CNT3_TR_CTRL2	0x402001E8	FULL	Counter trigger control register 2
TCPWM_CNT3_INTR	0x402001F0	FULL	Interrupt request register.
TCPWM_CNT3_INTR_SET	0x402001F4	FULL	Interrupt set request register.
TCPWM_CNT3_INTR_MASK	0x402001F8	FULL	Interrupt mask register.
TCPWM_CNT3_INTR_MASKED	0x402001FC	FULL	Interrupt masked request register

17.5 Register Details

17.5.1 TCPWM_CTRL

Description: TCPWM control register 0.
Address: 0x40200000
Offset: 0x0
Retention: Not Retained
IsDeepSleep: No
Comment: Used to disable/enable the counters.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				COUNTER_ENABLED [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	COUNTER_ENABLED	RW	R	0	Counter enables for counters 0 up to CNT_NR-1. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_CTRL0, TR_CTRL1, and TR_CTRL2 register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ('tr_overflow', 'tr_underflow' and 'tr_compare_match'). - the counter's line outputs ('line_out' and 'line_compl_out').

17.5.2 TCPWM_CMD

Description: TCPWM command register.
Address: 0x40200008
Offset: 0x8
Retention: Not Retained
IsDeepSleep: No
Comment: Enables software controlled counter operation.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				COUNTER_CAPTURE [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				COUNTER_RELOAD [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				COUNTER_STOP [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:28]				COUNTER_START [27:24]			

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	COUNTER_CAPTURE	RW1S	RW1C	0	Counters SW capture trigger. When written with '1', a capture trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.COUNTER_ENABLED, the field is immediately set to '0'.
8:11	COUNTER_RELOAD	RW1S	RW1C	0	Counters SW reload trigger. For HW behavior, see COUNTER_CAPTURE field.
16:19	COUNTER_STOP	RW1S	RW1C	0	Counters SW stop trigger. For HW behavior, see COUNTER_CAPTURE field.
24:27	COUNTER_START	RW1S	RW1C	0	Counters SW start trigger. For HW behavior, see COUNTER_CAPTURE field.

17.5.3 TCPWM_INTR_CAUSE

Description: TCPWM Counter interrupt cause register.
Address: 0x4020000C
Offset: 0xC
Retention: Not Retained
IsDeepSleep: No
Comment: Enables software to determine the source of the combined interrupt output signal 'interrupt'. The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				COUNTER_INT [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	COUNTER_INT	R	W	0	Counters interrupt signal active. If the counter is disabled through CTRL.COUNTER_ENABLED, the associated interrupt field is immediately set to '0'.

17.5.4 CNT

17.5.4.1 TCPWM_CNT_CTRL

Description: Counter control register
Address: 0x40200100
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:4]				PWM _STOP_ON _KILL [3:3]	PWM _SYNC_ KILL [2:2]	AUTO _RELOAD _PERIOD [1:1]	AUTO _RELOAD _CC [0:0]

Bits	15	14	13	12	11	10	9	8
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:22]		QUADRATURE_MODE [21:20]		None [19:19]	ONE _SHOT [18:18]	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
Name	None [31:27]					MODE [26:24]		

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	AUTO_RELOAD_CC	RW	R	0	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event.
1	AUTO_RELOAD _PERIOD	RW	R	0	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event.
2	PWM_SYNC_KILL	RW	R	0	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the 'dt_line_out' and 'dt_line_compl_out' signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the 'dt_line_out' and 'dt_line_compl_out' signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'.

Bits	Name	SW	HW	Default or Enum	Description
3	PWM_STOP_ON_KILL	RW	R	0	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only.
8:15	GENERIC	RW	R	0	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock.
	DIVBY1			0	Divide by 1 (other-than-PWM_DT mode)
	DIVBY2			1	Divide by 2 (other-than-PWM_DT mode)
	DIVBY4			2	Divide by 4 (other-than-PWM_DT mode)
	DIVBY8			3	Divide by 8 (other-than-PWM_DT mode)
	DIVBY16			4	Divide by 16 (other-than-PWM_DT mode)
	DIVBY32			5	Divide by 32 (other-than-PWM_DT mode)
	DIVBY64			6	Divide by 64 (other-than-PWM_DT mode)
	DIVBY128			7	Divide by 128 (other-than-PWM_DT mode)
16:17	UP_DOWN_MODE	RW	R	0	Determines counter direction.
	COUNT_UP			0	Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD, and is changed to a different value. A terminal count event is generated when the counter reaches PERIOD, and is changed to a different value.
	COUNT_DOWN			1	Count down (to '0'). An underflow event is generated when the counter reaches '0', and is changed to a different value. A terminal count event is generated when the counter reaches '0', and is changed to a different value.
	COUNT_UPDN1			2	Count up (to PERIOD), then count down (to '0'). An overflow event is generated when the counter reaches PERIOD, and is changed to a different value. An underflow event is generated when the counter reaches '0', and is changed to a different value. A terminal count event is generated when the counter reaches '0', and is changed to a different value.
	COUNT_UPDN2			3	Count up (to PERIOD), then count down (to '0'). An overflow event is generated when the counter reaches PERIOD, and is changed to a different value. An underflow event is generated when the counter reaches '0', and is changed to a different value. A terminal count event is generated when the counter reaches '0', and is changed to a different value AND when the counter reaches PERIOD, and is changed to a different value. (this counter direction can be used for PWM functionality with asymmetrical updates).
18	ONE_SHOT	RW	R	0	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated.
20:21	QUADRATURE_MODE	RW	R	0	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert 'dt_line_out' and 'dt_line_compl_out'. Inversion is the last step in generation of 'dt_line_out' and 'dt_line_compl_out'; i.e. a disabled output line 'dt_line_out' has the value QUADRATURE_MODE[0] and a disabled output line 'dt_line_compl_out' has the value QUADRATURE_MODE[1].

Bits	Name	SW	HW	Default or Enum	Description
	X1			0	X1 encoding (QUAD mode)
	X2			1	X2 encoding (QUAD mode)
	X4			2	X4 encoding (QUAD mode)
	INV_OUT			1	When bit 0 is '1', QUADRATURE_MODE[0] inverts 'dt_line_out' (PWM/PWM_DT modes)
	INV_COMPL_OUT			2	When bit 1 is '1', QUADRATURE_MODE[1] inverts 'dt_line_compl_out' (PWM/PWM_DT modes)
24:26	MODE	RW	R	0	Counter mode.
	TIMER			0	Timer mode
	CAPTURE			2	Capture mode
	QUAD			3	Quadrature encoding mode
	PWM			4	Pulse width modulation (PWM) mode
	PWM_DT			5	PWM with deadtime insertion mode
	PWM_PR			6	Pseudo random pulse width modulation

17.5.4.2 TCPWM_CNT_STATUS

Description: Counter status register
Address: 0x40200104
Offset: 0x4
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:1]							DOWN [0:0]

Bits	15	14	13	12	11	10	9	8
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	RUNNING [31:31]	None [30:24]						

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	DOWN	R	RW	0	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented.
8:15	GENERIC	R	RW	0	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality.
31	RUNNING	R	RW	0	When '0', the counter is NOT running. When '1', the counter is running.

17.5.4.3 TCPWM_CNT_COUNTER

Description: Counter count register
Address: 0x40200108
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	COUNTER	RW	RW	0	16-bit counter value. It is advised to not write to this field when the counter is running.

17.5.4.4 TCPWM_CNT_CC

Description: Counter compare/capture register
Address: 0x4020010C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	CC	RW	RW	65535	In CAPTURE mode, captures the counter value. In other modes, compared to counter value.

17.5.4.5 TCPWM_CNT_CC_BUFF

Description: Counter buffered compare/capture register
Address: 0x40200110
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	CC	RW	RW	65535	Additional buffer for counter CC register.

17.5.4.6 TCPWM_CNT_PERIOD

Description: Counter period register
Address: 0x40200114
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	PERIOD	RW	RW	65535	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1.

17.5.4.7 TCPWM_CNT_PERIOD_BUFF

Description: Counter buffered period register
Address: 0x40200118
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:15	PERIOD	RW	RW	65535	Additional buffer for counter PERIOD register.

17.5.4.8 TCPWM_CNT_TR_CTRL0

Description: Counter trigger control register 0
Address: 0x40200120
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment: Used to select triggers for specific counter events.
Default: 0x10

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:3	CAPTURE_SEL	RW	R	0	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger 1 is always '1'. Input trigger 2 is the first external trigger line (tcpwm.tr_in[0]). In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts.
4:7	COUNT_SEL	RW	R	1	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'.
8:11	RELOAD_SEL	RW	R	0	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register.
12:15	STOP_SEL	RW	R	0	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event.
16:19	START_SEL	RW	R	0	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B).

17.5.4.9 TCPWM_CNT_TR_CTRL1

Description: Counter trigger control register 1
Address: 0x40200124
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment: Used to determine edge detection for specific counter triggers. Events will only take effect on enabled counters.
Default: 0x3FF

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	CAPTURE_EDGE	RW	R	3	A capture event will copy the counter value into the CC register.
	RISING_EDGE			0	Rising edge. Any rising edge generates an event.
	FALLING_EDGE			1	Falling edge. Any falling edge generates an event.
	BOTH_EDGES			2	Rising AND falling edge. Any odd amount of edges generates an event.
	NO_EDGE_DET			3	No edge detection, use trigger as is.
2:3	COUNT_EDGE	RW	R	3	A counter event will increase or decrease the counter by '1'.
	RISING_EDGE			0	Rising edge. Any rising edge generates an event.
	FALLING_EDGE			1	Falling edge. Any falling edge generates an event.
	BOTH_EDGES			2	Rising AND falling edge. Any odd amount of edges generates an event.
	NO_EDGE_DET			3	No edge detection, use trigger as is.
4:5	RELOAD_EDGE	RW	R	3	A reload event will initialize the counter. When counting up, the counter is initialized to '0'. When counting down, the counter is initialized with PERIOD.
	RISING_EDGE			0	Rising edge. Any rising edge generates an event.
	FALLING_EDGE			1	Falling edge. Any falling edge generates an event.
	BOTH_EDGES			2	Rising AND falling edge. Any odd amount of edges generates an event.
	NO_EDGE_DET			3	No edge detection, use trigger as is.
6:7	STOP_EDGE	RW	R	3	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter.
	RISING_EDGE			0	Rising edge. Any rising edge generates an event.
	FALLING_EDGE			1	Falling edge. Any falling edge generates an event.
	BOTH_EDGES			2	Rising AND falling edge. Any odd amount of edges generates an event.
	NO_EDGE_DET			3	No edge detection, use trigger as is.

Bits	Name	SW	HW	Default or Enum	Description
8:9	START_EDGE	RW	R	3	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does.
	RISING_EDGE			0	Rising edge. Any rising edge generates an event.
	FALLING_EDGE			1	Falling edge. Any falling edge generates an event.
	BOTH_EDGES			2	Rising AND falling edge. Any odd amount of edges generates an event.
	NO_EDGE_DET			3	No edge detection, use trigger as is.

17.5.4.10 TCPWM_CNT_TR_CTRL2

Description: Counter trigger control register 2
Address: 0x40200128
Offset: 0x28
Retention: Retained
IsDeepSleep: No
Comment: Used to control counter 'line_out', 'dt_line_out' and 'dt_line_compl_out' output signals.
Default: 0x3F

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0:1	CC_MATCH_MODE	RW	R	3	Determines the effect of a compare match event (COUNTER equals CC register) on the 'line_out' output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0 percent, the counter CC register should be set to '0'. For a 100 percent duty cycle, the counter CC register should be set to larger than the counter PERIOD register.
	SET			0	Set to '1'
	CLEAR			1	Set to '0'
	INVERT			2	Invert
	NO_CHANGE			3	No Change
2:3	OVERFLOW_MODE	RW	R	3	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the 'line_out' output signals.
	SET			0	Set to '1'
	CLEAR			1	Set to '0'
	INVERT			2	Invert
	NO_CHANGE			3	No Change
4:5	UNDERFLOW_MODE	RW	R	3	Determines the effect of a counter underflow event (COUNTER reaches '0') on the 'line_out' output signals.
	SET			0	Set to '1'
	CLEAR			1	Set to '0'
	INVERT			2	Invert
	NO_CHANGE			3	No Change

17.5.4.11 TCPWM_CNT_INTR

Description: Interrupt request register.
Address: 0x40200130
Offset: 0x30
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode. HW clears the interrupt causes to '0', when the counter is disabled.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						CC _MATCH [1:1]	TC [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TC	RW1C	RW1S	0	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit.
1	CC_MATCH	RW1C	RW1S	0	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit.

17.5.4.12 TCPWM_CNT_INTR_SET

Description: Interrupt set request register.
Address: 0x40200134
Offset: 0x34
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						CC _MATCH [1:1]	TC [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TC	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.
1	CC_MATCH	RW1S	A	0	Write with '1' to set corresponding bit in interrupt request register.

17.5.4.13 TCPWM_CNT_INTR_MASK

Description: Interrupt mask register.
Address: 0x40200138
Offset: 0x38
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						CC _MATCH [1:1]	TC [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TC	RW	R	0	Mask bit for corresponding bit in interrupt request register.
1	CC_MATCH	RW	R	0	Mask bit for corresponding bit in interrupt request register.

17.5.4.14 TCPWM_CNT_INTR_MASKED

Description: Interrupt masked request register
Address: 0x4020013C
Offset: 0x3C
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise AND between the interrupt request and mask registers.
Default: 0x0

Bit-field Table

Bits	7	6	5	4	3	2	1	0
Name	None [7:2]						CC _MATCH [1:1]	TC [0:0]

Bits	15	14	13	12	11	10	9	8
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
Name	None [31:24]							

Bit-fields

Bits	Name	SW	HW	Default or Enum	Description
0	TC	R	W	0	Logical and of corresponding request and mask bits.
1	CC_MATCH	R	W	0	Logical and of corresponding request and mask bits.

References

[1] 002-29223: PSOC™ high-voltage (HV) precision analog (PA) MCU architecture reference manual

Revision history

Document revision	Date	Description of changes
**	2020-08-13	Specification for new silicon
*A	2020-12-03	Updated Sflash registers Corrections applied to internal registers PACSS gain and trim values updated PACSS some filter details updated along with other descriptions
*B	2021-04-29	rev_b updates. Updated Copyrights.
*C	2021-07-07	rev_c updates and corrections (refer to PSoC4HVPA144K_RegistersTRM_Diff_Rev0B_Rev0C.pdf attached). Updated Copyrights.
*D	2021-12-03	Updated the registers (refer to PSoC_HVPA144K_RegistersTRM_Diff_Rev0C_Rev0D.pdf attached).
*E	2022-11-17	Synchronization between HTML and PDF contents for some registers corrected Detailed register level differences are captured in the Delta log PDF
*F	2026-08-22	• New Register added • Updated the following: – IMO Trim Default values – Flash Write Enable Retention – Overtemperature Threshold

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