PSOC™ Control C1 MCU registers

Reference manual

About this document

Scope and purpose

This reference manual lists all the registers in the mapping tables of the PSOC™ Control C1 MCU in address order. For architecture details, see PSOC™ Control C1 MCU architecture reference manual.

Intended audience

This reference manual is intended for the embedded hardware engineers, software developers, and system architects who want to understand the register details of the Infineon PSOC™ Control C1 series of microcontrollers.

Register access modes

Read and write access to registers and memory locations are sometimes restricted. In memory and register access tables, the following terms are used.

Table 1 Register access modes

Symbol	Description
PV (SV), U	Access permitted in Privileged (Supervisor) Mode. *Note: Arm® Cortex®-M0 processor does not support different privilege levels. Only Privileged (Supervisor) Mode is supported in PSC1Mx Family. Symbol "U" and Symbol "PV" can be used to represent the access permitted in this mode.*
BP	Indicates that this register can only be access when the bit protection is disabled. See detailed description of Bit Protection Scheme in the Memory Organisation chapter.
32	Only 32-bit word accesses are permitted to this register/address range.
NC	No change, indicated register is not changed.
BE	Indicates that an access to this address range generates a Bus Error.
nBE	Indicates that no Bus Error is generated when accessing this address range.

Reserved bits

Register bit fields named **Reserved** or **0** indicate unimplemented functions with the following behavior.

- Reading these bit fields returns 0.
- These bit fields should be written with 0 if the bit field is defined as r or rh.
- These bit fields have to be written with 0 if the bit field is defined as rw.

These bit fields are reserved. The detailed description of these bit fields can be found in the register descriptions.

Abbreviations and acronyms

The following acronyms and terms are used in this document.

Table 2 Abbreviations and acronyms

ACMP	Analog Comparator
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
ANACTRL	Analog Control Unit
APB	Advanced Peripheral Bus
ASC	Asynchronous Serial Channel
BCCU	Brightness and Colour Control Unit
BMI	Boot Mode Index
CMSIS	Cortex® Microcontroller Software Interface Standard
CPU	Central Processing Unit
CCU4	Capture Compare Unit 4
CCU8	Capture Compare Unit 8
CRC	Cyclic Redundancy Code
DCO	Digitally Controlled Oscillator
ECC	Error Correction Code

Register access modes

Table 2 Abbreviations and acronyms (continued)

ERU	Event Request Unit
EVR	Embedded Voltage Regulator
FPU	Floating Point Unit
GPIO	General Purpose Input/Output
HMI	Human-Machine Interface
IIC	Inter Integrated Circuit (also known as I2C)
IIS	Inter-IC Sound Interface
I/O	Input/Output
JTAG	Joint Test Action Group = IEEE1149.1
LED	Light Emitting Diode
MSB	Most Significant Bit
NC	Not Connected
NMI	Non-Maskable Interrupt
NVIC	Nested Vectored Interrupt Controller
ORC	Out of Range Comparator
PAU	Peripheral Access Unit
POSIF	Position Interface
PRNG	Pseudo Random Number Generator
ROM	Read-Only Memory
RAM	Random Access Memory
RTC	Real Time Clock
SCU	System Control Unit
SFR	Special Function Register
SHS	Sample and Hold Sequencer
SPI	Serial Peripheral Interface
SRAM	Static RAM
SR	Service Request
SSC	Synchronous Serial Channel
SSW	Start-up Software
TSE	Temperature Sensor
UART	Universal Asynchronous Receiver Transmitter
USIC	Universal Serial Interface Channel
VADC	Versatile Analog-to-Digital Converter
WDT	Watchdog Timer

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1 Brightness and Color Control Unit Registers

BCCU Unit 0

1.1 Register overview

Instance	Base address
BCCU0	0x50030000
BCCU0_CH0	0x5003003C
BCCU0_CH1	0x50030050
BCCU0_CH2	0x50030064
BCCU0_CH3	0x50030078
BCCU0_CH4	0x5003008C
BCCU0_CH5	0x500300A0
BCCU0_CH6	0x500300B4
BCCU0_CH7	0x500300C8
BCCU0_CH8	0x500300DC
BCCU0_DE0	0x5003017C
BCCU0_DE1	0x50030188
BCCU0_DE2	0x50030194

Register name	Offset	Reset	Description
GLOBCON	0x00	0x03200000	Global Control
GLOBCLK	0x04	0x00DB0190	Global Clock
ID	0x08	0x00F3C000	Module Identification
CHEN	0x0C	0x00000000	Channel Enable
CHOCON	0x10	0x00000000	Channel Output Control
CHTRIG	0x14	0x00000000	Channel Trigger
CHSTRCON	0x18	0x00000000	Channel Shadow Transfer
LTCHOL	0x1C	0x00000000	Last Trigger Channel Output Level
DEEN	0x20	0x00000000	Dimming Engine Enable
DESTRCON	0x24	0x00000000	Dimming Shadow Transfer
GLOBDIM	0x28	0x00000000	Global Dimming Level
EVIER	0x2C	0x00000000	Event Interrupt Enable
EVFR	0x30	0x00000000	Event Flag
EVFSR	0x34	0x00000000	Event Flag Set
EVFCR	0x38	0x00000000	Event Flag Clear

1.2 Register details

1.2.1 GLOBCON

Global Control

Reset 0x03200000

Width 32

Bit-field table (31 … 16)

0				WDMBN [27:16]											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

LTRS [15:12]				0	TRAP ED [10]	TRAPIS [9:6]				SUSCFG [5:4]		TRDEL [3:2]		0	TM [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	TM	read-write	Trigger Mode value1 = #0 (Mode 0: BCCU trigger occurs if there is any channel trigger (OR logic)) value2 = #1 (Mode 1: BCCU trigger occurs if there is a channel trigger event on the active channel. When this happens, the next trigger-enabled channel will be active following the round robin.)
3:2	TRDEL	read-write	Trigger Delay value1 = #00 (No delay) value2 = #01 (BCCU trigger occurs a quarter bit time after the channel trigger that caused it; only to be used if BCCU_GLOBCLK.BCS is 0) value3 = #10 (BCCU trigger occurs half a bit time after the channel trigger that caused it; only to be used if BCCU_GLOBCLK.BCS is 0) value4 = #11 (No delay)
5:4	SUSCFG	read-write	Suspend Mode Configuration value1 = #00 (Suspend request is ignored and the module cannot get suspended) value2 = #01 (All channels stop running immediately and freeze in the last state without any safe stop) value3 = #10 (All channels stop running immediately and freeze in the last state; all outputs go to passive state to achieve safe stop)
9:6	TRAPIS	read-write	Trap Input Pin Selector value1 = #0000 (BCCU.TRAPINA) value2 = #0001 (BCCU.TRAPINB) value3 = #0010 (BCCU.TRAPINC) value4 = #0011 (BCCU.TRAPIND) value5 = #0100 (BCCU.TRAPINE) value6 = #0101 (BCCU.TRAPINF) value7 = #0110 (BCCU.TRAPING) value8 = #0111 (BCCU.TRAPINH) value9 = #1000 (BCCU.TRAPINI) value10 = #1001 (BCCU.TRAPING) value11 = #1010 (BCCU.TRAPINK) value12 = #1011 (BCCU.TRAPINL) value13 = #1100 (BCCU.TRAPINM) value14 = #1101 (BCCU.TRAPINN) value15 = #1110 (BCCU.TRAPINO) value16 = #1111 (BCCU.TRAPINP)
10	TRAPED	read-write	Trap Edge value1 = #0 (Trap occurs (trap flag is set) on rising edge of the BCCU.TRAPL signal) value2 = #1 (Trap occurs (trap flag is set) on falling edge of the BCCU.TRAPL signal)

Bits	Field	Access	Description
15:12	LTRS	read-only	Last Trigger Source value1 = #0000 (The last trigger occurred in channel turn 0) value2 = #0001 (The last trigger occurred in channel turn 1) value3 = #0010 (The last trigger occurred in channel turn 2) value4 = #0011 (The last trigger occurred in channel turn 3) value5 = #0100 (The last trigger occurred in channel turn 4) value6 = #0101 (The last trigger occurred in channel turn 5) value7 = #0110 (The last trigger occurred in channel turn 6) value8 = #0111 (The last trigger occurred in channel turn 7) value9 = #1000 (The last trigger occurred in channel turn 8)
27:16	WDMBN	read-write	Watchdog Maximum Bitnumber
28-31, 11, 1 0		read	Reserved

1.2.2 GLOBCLK

Global Clock

Reset	0x00DB0190
Width	32

Bit-field table (31 … 16)

0	DCLK_PS [27:16]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

BCS [15]	0	FCLK_PS [11:0]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
11:0	FCLK_PS	read-write	Fast Clock Prescaler Factor value1 = 0 (No clock) value2 = 1 (Divide by 1) value3 = 4095 (Divide by 4095)
15	BCS	read-write	Bit-Clock Selector value1 = #0 (Normal Mode: BCCU_bclk is generated from BCCU_fclk by a division of 4) value2 = #1 (Fast Mode: BCCU_bclk is the same as BCCU_fclk)
27:16	DCLK_PS	read-write	Dimmer Clock Prescaler Factor value1 = 0 (No clock) value2 = 1 (Divide by 1) value3 = 4095 (Divide by 4095)
28-31, 12-14	0	read	Reserved

1.2.3 ID

Module Identification

Reset	0x00F3C000
Width	32

Bit-field table (31 … 16)

MOD_NUMBER [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

MOD_TYPE0 [15:8]								MOD_REV [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	MOD_REV	read-only	Module Revision Number
15:8	MOD_TYPE0	read-only	Module Type
31:16	MOD_NUMBER	read-only	Module Number Value

1.2.4 CHEN

Channel Enable

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0							ECH8 [8]	ECH7 [7]	ECH6 [6]	ECH5 [5]	ECH4 [4]	ECH3 [3]	ECH2 [2]	ECH1 [1]	ECH0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	ECH0	read-write	Channel 0 Enable value1 = #0 (Channel is disabled, the output level is passive; the Linear Walker and the Sigma-Delta Modulator are reset, the Packer FIFO is flushed; all internal logic and INTy are reset when the channel gets disabled) value2 = #1 (Channel is enabled)
1	ECH1	read-write	Channel 1 Enable value1 = #0 (Channel is disabled, the output level is passive; the Linear Walker and the Sigma-Delta Modulator are reset, the Packer FIFO is flushed; all internal logic and INTy are reset when the channel gets disabled) value2 = #1 (Channel is enabled)
2	ECH2	read-write	Channel 2 Enable value1 = #0 (Channel is disabled, the output level is passive; the Linear Walker and the Sigma-Delta Modulator are reset, the Packer FIFO is flushed; all internal logic and INTy are reset when the channel gets disabled) value2 = #1 (Channel is enabled)
3	ECH3	read-write	Channel 3 Enable value1 = #0 (Channel is disabled, the output level is passive; the Linear Walker and the Sigma-Delta Modulator are reset, the Packer FIFO is flushed; all internal logic and INTy are reset when the channel gets disabled) value2 = #1 (Channel is enabled)
4	ECH4	read-write	Channel 4 Enable value1 = #0 (Channel is disabled, the output level is passive; the Linear Walker and the Sigma-Delta Modulator are reset, the Packer FIFO is flushed; all internal logic and INTy are reset when the channel gets disabled) value2 = #1 (Channel is enabled)
5	ECH5	read-write	Channel 5 Enable value1 = #0 (Channel is disabled, the output level is passive; the Linear Walker and the Sigma-Delta Modulator are reset, the Packer FIFO is flushed; all internal logic and INTy are reset when the channel gets disabled) value2 = #1 (Channel is enabled)
6	ECH6	read-write	Channel 6 Enable value1 = #0 (Channel is disabled, the output level is passive; the Linear Walker and the Sigma-Delta Modulator are reset, the Packer FIFO is flushed; all internal logic and INTy are reset when the channel gets disabled) value2 = #1 (Channel is enabled)
7	ECH7	read-write	Channel 7 Enable value1 = #0 (Channel is disabled, the output level is passive; the Linear Walker and the Sigma-Delta Modulator are reset, the Packer FIFO is flushed; all internal logic and INTy are reset when the channel gets disabled) value2 = #1 (Channel is enabled)

Bits	Field	Access	Description
8	ECH8	read-write	Channel 8 Enable value1 = #0 (Channel is disabled, the output level is passive; the Linear Walker and the Sigma-Delta Modulator are reset, the Packer FIFO is flushed; all internal logic and INTy are reset when the channel gets disabled) value2 = #1 (Channel is enabled)
9-31	0	read	Reserved

1.2.5 CHOCON

Channel Output Control

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0							CH8TPE [24]	CH7TPE [23]	CH6TPE [22]	CH5TPE [21]	CH4TPE [20]	CH3TPE [19]	CH2TPE [18]	CH1TPE [17]	CH0TPE [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0							CH8OP [8]	CH7OP [7]	CH6OP [6]	CH5OP [5]	CH4OP [4]	CH3OP [3]	CH2OP [2]	CH1OP [1]	CH0OP [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	CH0OP	read-write	Channel 0 Output Passive Level value1 = #0 (Active high) value2 = #1 (Active low)
1	CH1OP	read-write	Channel 1 Output Passive Level value1 = #0 (Active high) value2 = #1 (Active low)
2	CH2OP	read-write	Channel 2 Output Passive Level value1 = #0 (Active high) value2 = #1 (Active low)
3	CH3OP	read-write	Channel 3 Output Passive Level value1 = #0 (Active high) value2 = #1 (Active low)
4	CH4OP	read-write	Channel 4 Output Passive Level value1 = #0 (Active high) value2 = #1 (Active low)
5	CH5OP	read-write	Channel 5 Output Passive Level value1 = #0 (Active high) value2 = #1 (Active low)
6	CH6OP	read-write	Channel 6 Output Passive Level value1 = #0 (Active high) value2 = #1 (Active low)
7	CH7OP	read-write	Channel 7 Output Passive Level value1 = #0 (Active high) value2 = #1 (Active low)
8	CH8OP	read-write	Channel 8 Output Passive Level value1 = #0 (Active high) value2 = #1 (Active low)
16	CH0TPE	read-write	Channel 0 Trap Enable value1 = #0 (Trap function on channel is disabled) value2 = #1 (Trap function on channel is enabled, the output goes to passive level when trap occurs)
17	CH1TPE	read-write	Channel 1 Trap Enable value1 = #0 (Trap function on channel is disabled) value2 = #1 (Trap function on channel is enabled, the output goes to passive level when trap occurs)
18	CH2TPE	read-write	Channel 2 Trap Enable value1 = #0 (Trap function on channel is disabled) value2 = #1 (Trap function on channel is enabled, the output goes to passive level when trap occurs)
19	CH3TPE	read-write	Channel 3 Trap Enable value1 = #0 (Trap function on channel is disabled) value2 = #1 (Trap function on channel is enabled, the output goes to passive level when trap occurs)

Bits	Field	Access	Description
20	CH4TPE	read-write	Channel 4 Trap Enable value1 = #0 (Trap function on channel is disabled) value2 = #1 (Trap function on channel is enabled, the output goes to passive level when trap occurs)
21	CH5TPE	read-write	Channel 5 Trap Enable value1 = #0 (Trap function on channel is disabled) value2 = #1 (Trap function on channel is enabled, the output goes to passive level when trap occurs)
22	CH6TPE	read-write	Channel 6 Trap Enable value1 = #0 (Trap function on channel is disabled) value2 = #1 (Trap function on channel is enabled, the output goes to passive level when trap occurs)
23	CH7TPE	read-write	Channel 7 Trap Enable value1 = #0 (Trap function on channel is disabled) value2 = #1 (Trap function on channel is enabled, the output goes to passive level when trap occurs)
24	CH8TPE	read-write	Channel 8 Trap Enable value1 = #0 (Trap function on channel is disabled) value2 = #1 (Trap function on channel is enabled, the output goes to passive level when trap occurs)
25-31, 9-15	0	read	Reserved

1.2.6 CHTRIG

Channel Trigger

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0							TOS8 [24]	TOS7 [23]	TOS6 [22]	TOS5 [21]	TOS4 [20]	TOS3 [19]	TOS2 [18]	TOS1 [17]	TOS0 [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0							ET8 [8]	ET7 [7]	ET6 [6]	ET5 [5]	ET4 [4]	ET3 [3]	ET2 [2]	ET1 [1]	ET0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	ET0	read-write	Channel 0 Trigger Enable value1 = #0 (Channel trigger is disabled) value2 = #1 (Channel trigger is enabled)
1	ET1	read-write	Channel 1 Trigger Enable value1 = #0 (Channel trigger is disabled) value2 = #1 (Channel trigger is enabled)
2	ET2	read-write	Channel 2 Trigger Enable value1 = #0 (Channel trigger is disabled) value2 = #1 (Channel trigger is enabled)
3	ET3	read-write	Channel 3 Trigger Enable value1 = #0 (Channel trigger is disabled) value2 = #1 (Channel trigger is enabled)
4	ET4	read-write	Channel 4 Trigger Enable value1 = #0 (Channel trigger is disabled) value2 = #1 (Channel trigger is enabled)
5	ET5	read-write	Channel 5 Trigger Enable value1 = #0 (Channel trigger is disabled) value2 = #1 (Channel trigger is enabled)
6	ET6	read-write	Channel 6 Trigger Enable value1 = #0 (Channel trigger is disabled) value2 = #1 (Channel trigger is enabled)
7	ET7	read-write	Channel 7 Trigger Enable value1 = #0 (Channel trigger is disabled) value2 = #1 (Channel trigger is enabled)
8	ET8	read-write	Channel 8 Trigger Enable value1 = #0 (Channel trigger is disabled) value2 = #1 (Channel trigger is enabled)
16	TOS0	read-write	Channel 0 Trigger Output Select value1 = #0 (The channel trigger pulse will appear on BCCU_TRIGOUT0) value2 = #1 (The channel trigger pulse will appear on BCCU_TRIGOUT1)
17	TOS1	read-write	Channel 1 Trigger Output Select value1 = #0 (The channel trigger pulse will appear on BCCU_TRIGOUT0) value2 = #1 (The channel trigger pulse will appear on BCCU_TRIGOUT1)
18	TOS2	read-write	Channel 2 Trigger Output Select value1 = #0 (The channel trigger pulse will appear on BCCU_TRIGOUT0) value2 = #1 (The channel trigger pulse will appear on BCCU_TRIGOUT1)

Bits	Field	Access	Description
19	TOS3	read-write	Channel 3 Trigger Output Select value1 = #0 (The channel trigger pulse will appear on BCCU_TRIGOUT0) value2 = #1 (The channel trigger pulse will appear on BCCU_TRIGOUT1)
20	TOS4	read-write	Channel 4 Trigger Output Select value1 = #0 (The channel trigger pulse will appear on BCCU_TRIGOUT0) value2 = #1 (The channel trigger pulse will appear on BCCU_TRIGOUT1)
21	TOS5	read-write	Channel 5 Trigger Output Select value1 = #0 (The channel trigger pulse will appear on BCCU_TRIGOUT0) value2 = #1 (The channel trigger pulse will appear on BCCU_TRIGOUT1)
22	TOS6	read-write	Channel 6 Trigger Output Select value1 = #0 (The channel trigger pulse will appear on BCCU_TRIGOUT0) value2 = #1 (The channel trigger pulse will appear on BCCU_TRIGOUT1)
23	TOS7	read-write	Channel 7 Trigger Output Select value1 = #0 (The channel trigger pulse will appear on BCCU_TRIGOUT0) value2 = #1 (The channel trigger pulse will appear on BCCU_TRIGOUT1)
24	TOS8	read-write	Channel 8 Trigger Output Select value1 = #0 (The channel trigger pulse will appear on BCCU_TRIGOUT0) value2 = #1 (The channel trigger pulse will appear on BCCU_TRIGOUT1)
25-31, 9-15	0	read	Reserved

1.2.7 CHSTRCON

Channel Shadow Transfer

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0							CH8A [24]	CH7A [23]	CH6A [22]	CH5A [21]	CH4A [20]	CH3A [19]	CH2A [18]	CH1A [17]	CH0A [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0							CH8S [8]	CH7S [7]	CH6S [6]	CH5S [5]	CH4S [4]	CH3S [3]	CH2S [2]	CH1S [1]	CH0S [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	CH0S	read-write	Channel 0 Shadow Transfer value1 = #0 (No action) value2 = #1 (Initiate channel y target intensity shadow transfer. The linear walk will start and channel y intensity will start to change towards the target. Cleared by hardware when the linear walk is complete and the target has been reached.)
1	CH1S	read-write	Channel 1 Shadow Transfer value1 = #0 (No action) value2 = #1 (Initiate channel y target intensity shadow transfer. The linear walk will start and channel y intensity will start to change towards the target. Cleared by hardware when the linear walk is complete and the target has been reached.)
2	CH2S	read-write	Channel 2 Shadow Transfer value1 = #0 (No action) value2 = #1 (Initiate channel y target intensity shadow transfer. The linear walk will start and channel y intensity will start to change towards the target. Cleared by hardware when the linear walk is complete and the target has been reached.)
3	CH3S	read-write	Channel 3 Shadow Transfer value1 = #0 (No action) value2 = #1 (Initiate channel y target intensity shadow transfer. The linear walk will start and channel y intensity will start to change towards the target. Cleared by hardware when the linear walk is complete and the target has been reached.)
4	CH4S	read-write	Channel 4 Shadow Transfer value1 = #0 (No action) value2 = #1 (Initiate channel y target intensity shadow transfer. The linear walk will start and channel y intensity will start to change towards the target. Cleared by hardware when the linear walk is complete and the target has been reached.)
5	CH5S	read-write	Channel 5 Shadow Transfer value1 = #0 (No action) value2 = #1 (Initiate channel y target intensity shadow transfer. The linear walk will start and channel y intensity will start to change towards the target. Cleared by hardware when the linear walk is complete and the target has been reached.)
6	CH6S	read-write	Channel 6 Shadow Transfer value1 = #0 (No action) value2 = #1 (Initiate channel y target intensity shadow transfer. The linear walk will start and channel y intensity will start to change towards the target. Cleared by hardware when the linear walk is complete and the target has been reached.)
7	CH7S	read-write	Channel 7 Shadow Transfer value1 = #0 (No action) value2 = #1 (Initiate channel y target intensity shadow transfer. The linear walk will start and channel y intensity will start to change towards the target. Cleared by hardware when the linear walk is complete and the target has been reached.)

Bits	Field	Access	Description
8	CH8S	read-write	Channel 8 Shadow Transfer value1 = #0 (No action) value2 = #1 (Initiate channel y target intensity shadow transfer. The linear walk will start and channel y intensity will start to change towards the target. Cleared by hardware when the linear walk is complete and the target has been reached.)
16	CH0A	write-only	Channel 0 Linear Walk Abort value1 = #0 (No action) value2 = #1 (Abort linear walk; CHyS is cleared, channel y intensity stops changing)
17	CH1A	write-only	Channel 1 Linear Walk Abort value1 = #0 (No action) value2 = #1 (Abort linear walk; CHyS is cleared, channel y intensity stops changing)
18	CH2A	write-only	Channel 2 Linear Walk Abort value1 = #0 (No action) value2 = #1 (Abort linear walk; CHyS is cleared, channel y intensity stops changing)
19	CH3A	write-only	Channel 3 Linear Walk Abort value1 = #0 (No action) value2 = #1 (Abort linear walk; CHyS is cleared, channel y intensity stops changing)
20	CH4A	write-only	Channel 4 Linear Walk Abort value1 = #0 (No action) value2 = #1 (Abort linear walk; CHyS is cleared, channel y intensity stops changing)
21	CH5A	write-only	Channel 5 Linear Walk Abort value1 = #0 (No action) value2 = #1 (Abort linear walk; CHyS is cleared, channel y intensity stops changing)
22	CH6A	write-only	Channel 6 Linear Walk Abort value1 = #0 (No action) value2 = #1 (Abort linear walk; CHyS is cleared, channel y intensity stops changing)
23	CH7A	write-only	Channel 7 Linear Walk Abort value1 = #0 (No action) value2 = #1 (Abort linear walk; CHyS is cleared, channel y intensity stops changing)
24	CH8A	write-only	Channel 8 Linear Walk Abort value1 = #0 (No action) value2 = #1 (Abort linear walk; CHyS is cleared, channel y intensity stops changing)
25-31, 9-15	0	read	Reserved

1.2.8 LTCHOL

Last Trigger Channel Output Level

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0							LTOL8 [8]	LTOL7 [7]	LTOL6 [6]	LTOL5 [5]	LTOL4 [4]	LTOL3 [3]	LTOL2 [2]	LTOL1 [1]	LTOL0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	LTOL0	read-only	Last Trigger Channel Output value1 = #0 (Passive) value2 = #1 (Active)
1	LTOL1	read-only	Last Trigger Channel Output value1 = #0 (Passive) value2 = #1 (Active)
2	LTOL2	read-only	Last Trigger Channel Output value1 = #0 (Passive) value2 = #1 (Active)
3	LTOL3	read-only	Last Trigger Channel Output value1 = #0 (Passive) value2 = #1 (Active)
4	LTOL4	read-only	Last Trigger Channel Output value1 = #0 (Passive) value2 = #1 (Active)
5	LTOL5	read-only	Last Trigger Channel Output value1 = #0 (Passive) value2 = #1 (Active)
6	LTOL6	read-only	Last Trigger Channel Output value1 = #0 (Passive) value2 = #1 (Active)
7	LTOL7	read-only	Last Trigger Channel Output value1 = #0 (Passive) value2 = #1 (Active)
8	LTOL8	read-only	Last Trigger Channel Output value1 = #0 (Passive) value2 = #1 (Active)
9-31	0	read	Reserved

1.2.9 DEEN

Dimming Engine Enable

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0													EDE2 [2]	EDE1 [1]	EDE0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	EDE0	read-write	Dimming Engine 0 Enable value1 = #0 (Dimming Engine is disabled;Channel brightness gets written with the value of channel intensity) value2 = #1 (Dimming Engine is enabled)
1	EDE1	read-write	Dimming Engine 1 Enable value1 = #0 (Dimming Engine is disabled;Channel brightness gets written with the value of channel intensity) value2 = #1 (Dimming Engine is enabled)
2	EDE2	read-write	Dimming Engine 2 Enable value1 = #0 (Dimming Engine is disabled;Channel brightness gets written with the value of channel intensity) value2 = #1 (Dimming Engine is enabled)
3-31	0	read	Reserved

1.2.10 DESTRCON

Dimming Shadow Transfer

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0													DE2A [18]	DE1A [17]	DE0A [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0													DE2S [2]	DE1S [1]	DE0S [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	DE0S	read-write	Dimming Engine 0 Shadow Transfer value1 = #0 (No action) value2 = #1 (Initiate target dimming level shadow transfer. The dimming process will start and the dimming level will change towards the target. Cleared by hardware when the dimming process is complete and the target has been reached after the configured dimming period.)
1	DE1S	read-write	Dimming Engine 1 Shadow Transfer value1 = #0 (No action) value2 = #1 (Initiate target dimming level shadow transfer. The dimming process will start and the dimming level will change towards the target. Cleared by hardware when the dimming process is complete and the target has been reached after the configured dimming period.)
2	DE2S	read-write	Dimming Engine 2 Shadow Transfer value1 = #0 (No action) value2 = #1 (Initiate target dimming level shadow transfer. The dimming process will start and the dimming level will change towards the target. Cleared by hardware when the dimming process is complete and the target has been reached after the configured dimming period.)
16	DE0A	write-only	Dimming Engine 0 Dimming Abort value1 = #0 (No action) value2 = #1 (Abort dimming; DEzS is cleared, BCCU_DLz.DLEV stops changing)
17	DE1A	write-only	Dimming Engine 1 Dimming Abort value1 = #0 (No action) value2 = #1 (Abort dimming; DEzS is cleared, BCCU_DLz.DLEV stops changing)
18	DE2A	write-only	Dimming Engine 2 Dimming Abort value1 = #0 (No action) value2 = #1 (Abort dimming; DEzS is cleared, BCCU_DLz.DLEV stops changing)
19-31, 3-15	0	read	Reserved

1.2.11 GLOBDIM

Global Dimming Level

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0				GLOBDIM [11:0]											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
11:0	GLOBDIM	read-write	Global Dimming Level
12-31	0	read	Reserved

1.2.12 EVIER

Event Interrupt Enable

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0											TPIEN [4]	EIEN [3]	FIEN [2]	T1IEN [1]	T0IEN [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	T0IEN	read-write	Trigger 0 Interrupt Enable value1 = #0 (Trigger 0 interrupt generation is disabled) value2 = #1 (BCCU trigger 0 (BCCU_TRIGOUT0) generates an interrupt on SR0)
1	T1IEN	read-write	Trigger 1 Interrupt Enable value1 = #0 (Trigger 1 interrupt generation is disabled) value2 = #1 (BCCU trigger 1 (BCCU_TRIGOUT1) generates an interrupt on SR0)
2	FIEN	read-write	FIFO Full Interrupt Enable value1 = #0 (FIFO-full interrupt generation is disabled) value2 = #1 (An interrupt is generated on SR0 if any of the packer FIFOs is full when there is a write attempt by the on-time or off-time counter)
3	EIEN	read-write	FIFO Empty Interrupt Enable value1 = #0 (FIFO-full interrupt generation is disabled) value2 = #1 (An interrupt is generated on SR0 if any of the packer FIFOs is empty when there is a read attempt by the output generator)
4	TPIEN	read-write	Trap Interrupt Enable value1 = #0 (Trap interrupt generation is disabled) value2 = #1 (An interrupt is generated on SR0 if a trap occurs)
5-31	0	read	Reserved

1.2.13 EVFR

Event Flag

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0								TPINL [7]	TPSF [6]	0	TPF [4]	EF [3]	FF [2]	T1F [1]	T0F [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	T0F	read-only	Trigger 0 Flag value1 = #0 (No trigger event has been detected on BCCU trigger line 0 (BCCU_TRIGOUT0)) value2 = #1 (A trigger event has been detected on BCCU trigger line 0 (BCCU_TRIGOUT0))
1	T1F	read-only	Trigger 1 Flag value1 = #0 (No trigger event has been detected on BCCU trigger line 1 (BCCU_TRIGOUT1)) value2 = #1 (A trigger event has been detected on BCCU trigger line 1 (BCCU_TRIGOUT1))
2	FF	read-only	FIFO Full Flag value1 = #0 (No FIFO full event has been detected) value2 = #1 (A FIFO full event has been detected because one of the packer FIFOs is full and there has been a write attempt by the on-time or off-time counter)
3	EF	read-only	FIFO Empty Flag value1 = #0 (No FIFO full event has been detected) value2 = #1 (A FIFO full event has been detected because one of the packer FIFOs is empty and there has been a read attempt by the output generator)
4	TPF	read-only	Trap Flag value1 = #0 (No trap event has been detected) value2 = #1 (A trap event has been detected)
6	TPSF	read-only	Trap State Flag value1 = #0 (BCCU is not in a trap state) value2 = #1 (BCCU is in a trap state, the affected channel outputs are at their passive levels)
7	TPINL	read-only	Trap Input Level value1 = #0 (The current level of BCCU.TRAPL is low) value2 = #1 (The current level of BCCU.TRAPL is high)
8-31, 5	0	read	Reserved

1.2.14 EVFSR

Event Flag Set

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0									TPS [6]	0	TPFS [4]	EFS [3]	FFS [2]	T1FS [1]	T0FS [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	T0FS	write-only	Trigger 0 Flag Set value1 = #0 (No action) value2 = #1 (Sets the Trigger 0 Flag in EVFR and an interrupt will be generated if enabled in EVIER)
1	T1FS	write-only	Trigger 1 Flag Set value1 = #0 (No action) value2 = #1 (Sets the Trigger 1 Flag in EVFR and an interrupt will be generated if enabled in EVIER)
2	FFS	write-only	FIFO Full Flag Set value1 = #0 (No action) value2 = #1 (Sets the FIFO Full Flag in EVFR and an interrupt will be generated if enabled in EVIER)
3	EFS	write-only	FIFO Empty Flag Set value1 = #0 (No action) value2 = #1 (Sets the FIFO Empty Flag in EVFR and an interrupt will be generated if enabled in EVIER)
4	TPFS	write-only	Trap Flag Set value1 = #0 (No action) value2 = #1 (Sets the Trap Flag in EVFR and an interrupt will be generated if enabled in EVIER, no trap will occur)
6	TPS	write-only	Trap Set value1 = #0 (No action) value2 = #1 (Sets the Trap State Flag and Trap Flag in EVFR, a trap will be generated and an interrupt will be generated if enabled in EVIER)
7-31, 5	0	read	Reserved

1.2.15 EVFCR

Event Flag Clear

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0									TPC [6]	0	TPFC [4]	EFC [3]	FFC [2]	T1FC [1]	T0FC [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	T0FC	write-only	Trigger 0 Flag Clear value1 = #0 (No action) value2 = #1 (Clears the Trigger 0 Flag in EVFR)
1	T1FC	write-only	Trigger 1 Flag Clear value1 = #0 (No action) value2 = #1 (Clears the Trigger 1 Flag in EVFR)
2	FFC	write-only	FIFO Full Flag Clear value1 = #0 (No action) value2 = #1 (Clears the FIFO Full Flag in EVFR)
3	EFC	write-only	FIFO Empty Flag Clear value1 = #0 (No action) value2 = #1 (Clears the FIFO Empty Flag in EVFR)
4	TPFC	write-only	Trap Flag Clear value1 = #0 (No action) value2 = #1 (Clears the Trap Flag in EVFR)
6	TPC	write-only	Trap Clear value1 = #0 (No action) value2 = #1 (Clears the Trap State Flag in EVFR; trap state is exited, the affected channels will return to their normal output levels)
7-31, 5	0	read	Reserved

2 CaptureCompare Unit 4 (CCU4) Registers

Capture Compare Unit 4 - Unit 0

2.1 Register overview

Instance	Base address
CCU40	0x48040000
CCU41	0x48044000
CCU40_CC40	0x48040100
CCU40_CC41	0x48040200
CCU40_CC42	0x48040300
CCU40_CC43	0x48040400
CCU41_CC40	0x48044100
CCU41_CC41	0x48044200
CCU41_CC42	0x48044300
CCU41_CC43	0x48044400

Register name	Offset	Reset	Description
GCTRL	0x00	0x00000000	Global Control Register
GSTAT	0x04	0x0000000F	Global Status Register
GIDLS	0x08	0x00000000	Global Idle Set
GIDLC	0x0C	0x00000000	Global Idle Clear
GCSS	0x10	0x00000000	Global Channel Set
GCSC	0x14	0x00000000	Global Channel Clear
GCST	0x18	0x00000000	Global Channel Status
MIDR	0x80	0x00B6C000	Module Identification

2.2 Register details

2.2.1 GCTRL

Global Control Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

MSDE [15:14]		MSE3 [13]	MSE2 [12]	MSE1 [11]	MSE0 [10]	SUSCFG [9:8]		0		PCIS [5:4]		0	PRBC [2:0]		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
2:0	PRBC	read-write	Prescaler Clear Configuration value1 = #000 (SW only) value2 = #001 (GSTATThe register contains the status of the prescaler and each timer slice (idle mode or running)..PRB and prescaler registers are cleared when the Run Bit of CC40 is cleared.) value3 = #010 (GSTATThe register contains the status of the prescaler and each timer slice (idle mode or running)..PRB and prescaler registers are cleared when the Run Bit of CC41 is cleared.) value4 = #011 (GSTATThe register contains the status of the prescaler and each timer slice (idle mode or running)..PRB and prescaler registers are cleared when the Run Bit of CC42 is cleared.) value5 = #100 (GSTATThe register contains the status of the prescaler and each timer slice (idle mode or running)..PRB and prescaler registers are cleared when the Run Bit of CC43 is cleared.)
5:4	PCIS	read-write	Prescaler Input Clock Selection value1 = #00 (Module clock) value2 = #01 (CCU4x.ECLKA) value3 = #10 (CCU4x.ECLKB) value4 = #11 (CCU4x.ECLKC)
9:8	SUSCFG	read-write	Suspend Mode Configuration value1 = #00 (Suspend request ignored. The module never enters in suspend) value2 = #01 (Stops all the running slices immediately. Safe stop is not applied.) value3 = #10 (Stops the block immediately and clamps all the outputs to PASSIVE state. Safe stop is applied.) value4 = #11 (Waits for the roll over of each slice to stop and clamp the slices outputs. Safe stop is applied.)
10	MSE0	read-write	Slice 0 Multi Channel shadow transfer enable value1 = #0 (Shadow transfer can only be requested by SW) value2 = #1 (Shadow transfer can be requested via SW and via the CCU4x.MCSS input.)
11	MSE1	read-write	Slice 1 Multi Channel shadow transfer enable value1 = #0 (Shadow transfer can only be requested by SW) value2 = #1 (Shadow transfer can be requested via SW and via the CCU4x.MCSS input.)
12	MSE2	read-write	Slice 2 Multi Channel shadow transfer enable value1 = #0 (Shadow transfer can only be requested by SW) value2 = #1 (Shadow transfer can be requested via SW and via the CCU4x.MCSS input.)
13	MSE3	read-write	Slice 3 Multi Channel shadow transfer enable value1 = #0 (Shadow transfer can only be requested by SW) value2 = #1 (Shadow transfer can be requested via SW and via the CCU4x.MCSS input.)

Bits	Field	Access	Description
15:14	MSDE	read-write	Multi Channel shadow transfer request configuration value1 = #00 (Only the shadow transfer for period and compare values is requested) value2 = #01 (Shadow transfer for the compare, period and prescaler compare values is requested) value4 = #11 (Shadow transfer for the compare, period, prescaler and dither compare values is requested)
16-31, 6-7,	30	read	Reserved

2.2.2 GSTAT

Global Status Register

Reset	0x0000000F
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0							PRB [8]	0				S3I [3]	S2I [2]	S1I [1]	S0I [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	S0I	read-only	CC40 IDLE status value1 = #0 (Running) value2 = #1 (Idle)
1	S1I	read-only	CC41 IDLE status value1 = #0 (Running) value2 = #1 (Idle)
2	S2I	read-only	CC42 IDLE status value1 = #0 (Running) value2 = #1 (Idle)
3	S3I	read-only	CC43 IDLE status value1 = #0 (Running) value2 = #1 (Idle)
8	PRB	read-only	Prescaler Run Bit value1 = #0 (Prescaler is stopped) value2 = #1 (Prescaler is running)
9-31, 4-7	0	read	Reserved

2.2.3 GIDLS

Global Idle Set

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0						PSIC [9]	CPRB [8]	0				SS3I [3]	SS2I [2]	SS1I [1]	SS0I [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	SS0I	write-only	CC40 IDLE mode set
1	SS1I	write-only	CC41 IDLE mode set
2	SS2I	write-only	CC42 IDLE mode set
3	SS3I	write-only	CC43 IDLE mode set
8	CPRB	write-only	Prescaler Run Bit Clear
9	PSIC	write-only	Prescaler clear
10-31, 4-7	0	read	Reserved

2.2.4 GIDLC

Global Idle Clear

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0							SPRB [8]	0				CS3I [3]	CS2I [2]	CS1I [1]	CS0I [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	CS0I	write-only	CC40 IDLE mode clear
1	CS1I	write-only	CC41 IDLE mode clear
2	CS2I	write-only	CC42 IDLE mode clear
3	CS3I	write-only	CC43 IDLE mode clear
8	SPRB	write-only	Prescaler Run Bit Set
9-31, 4-7	0	read	Reserved

2.2.5 GCSS

Global Channel Set

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0												S3STS [19]	S2STS [18]	S1STS [17]	S0STS [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0	S3PSE [14]	S3DSE [13]	S3SE [12]	0	S2PSE [10]	S2DSE [9]	S2SE [8]	0	S1PSE [6]	S1DSE [5]	S1SE [4]	0	S0PSE [2]	S0DSE [1]	S0SE [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	S0SE	write-only	Slice 0 shadow transfer set enable
1	S0DSE	write-only	Slice 0 Dither shadow transfer set enable
2	S0PSE	write-only	Slice 0 Prescaler shadow transfer set enable
4	S1SE	write-only	Slice 1 shadow transfer set enable
5	S1DSE	write-only	Slice 1 Dither shadow transfer set enable
6	S1PSE	write-only	Slice 1 Prescaler shadow transfer set enable
8	S2SE	write-only	Slice 2 shadow transfer set enable
9	S2DSE	write-only	Slice 2 Dither shadow transfer set enable
10	S2PSE	write-only	Slice 2 Prescaler shadow transfer set enable
12	S3SE	write-only	Slice 3 shadow transfer set enable
13	S3DSE	write-only	Slice 3 Dither shadow transfer set enable
14	S3PSE	write-only	Slice 3 Prescaler shadow transfer set enable
16	S0STS	write-only	Slice 0 status bit set
17	S1STS	write-only	Slice 1 status bit set
18	S2STS	write-only	Slice 2 status bit set
19	S3STS	write-only	Slice 3 status bit set
20-31, 15, 11, 7, 3	0	read	Reserved

2.2.6 GCSC

Global Channel Clear

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0												S3STC [19]	S2STC [18]	S1STC [17]	S0STC [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0	S3PSC [14]	S3DSC [13]	S3SC [12]	0	S2PSC [10]	S2DSC [9]	S2SC [8]	0	S1PSC [6]	S1DSC [5]	S1SC [4]	0	S0PSC [2]	S0DSC [1]	S0SC [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	S0SC	write-only	Slice 0 shadow transfer clear
1	S0DSC	write-only	Slice 0 Dither shadow transfer clear
2	S0PSC	write-only	Slice 0 Prescaler shadow transfer clear
4	S1SC	write-only	Slice 1 shadow transfer clear
5	S1DSC	write-only	Slice 1 Dither shadow transfer clear
6	S1PSC	write-only	Slice 1 Prescaler shadow transfer clear
8	S2SC	write-only	Slice 2 shadow transfer clear
9	S2DSC	write-only	Slice 2 Dither shadow transfer clear
10	S2PSC	write-only	Slice 2 Prescaler shadow transfer clear
12	S3SC	write-only	Slice 3 shadow transfer clear
13	S3DSC	write-only	Slice 3 Dither shadow transfer clear
14	S3PSC	write-only	Slice 3 Prescaler shadow transfer clear
16	S0STC	write-only	Slice 0 status bit clear
17	S1STC	write-only	Slice 1 status bit clear
18	S2STC	write-only	Slice 2 status bit clear
19	S3STC	write-only	Slice 3 status bit clear
20-31, 15, 11, 7, 3	0	read	Reserved

2.2.7 GCST

Global Channel Status

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0												CC43ST [19]	CC42ST [18]	CC41ST [17]	CC40ST [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0	S3PSS [14]	S3DSS [13]	S3SS [12]	0	S2PSS [10]	S2DSS [9]	S2SS [8]	0	S1PSS [6]	S1DSS [5]	S1SS [4]	0	S0PSS [2]	S0DSS [1]	S0SS [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	S0SS	read-only	Slice 0 shadow transfer status value1 = #0 (Shadow transfer has not been requested) value2 = #1 (Shadow transfer has been requested)
1	S0DSS	read-only	Slice 0 Dither shadow transfer status value1 = #0 (Dither shadow transfer has not been requested) value2 = #1 (Dither shadow transfer has been requested)
2	S0PSS	read-only	Slice 0 Prescaler shadow transfer status value1 = #0 (Prescaler shadow transfer has not been requested) value2 = #1 (Prescaler shadow transfer has been requested)
4	S1SS	read-only	Slice 1 shadow transfer status value1 = #0 (Shadow transfer has not been requested) value2 = #1 (Shadow transfer has been requested)
5	S1DSS	read-only	Slice 1 Dither shadow transfer status value1 = #0 (Dither shadow transfer has not been requested) value2 = #1 (Dither shadow transfer has been requested)
6	S1PSS	read-only	Slice 1 Prescaler shadow transfer status value1 = #0 (Prescaler shadow transfer has not been requested) value2 = #1 (Prescaler shadow transfer has been requested)
8	S2SS	read-only	Slice 2 shadow transfer status value1 = #0 (Shadow transfer has not been requested) value2 = #1 (Shadow transfer has been requested)
9	S2DSS	read-only	Slice 2 Dither shadow transfer status value1 = #0 (Dither shadow transfer has not been requested) value2 = #1 (Dither shadow transfer has been requested)
10	S2PSS	read-only	Slice 2 Prescaler shadow transfer status value1 = #0 (Prescaler shadow transfer has not been requested) value2 = #1 (Prescaler shadow transfer has been requested)
12	S3SS	read-only	Slice 3 shadow transfer status value1 = #0 (Shadow transfer has not been requested) value2 = #1 (Shadow transfer has been requested)
13	S3DSS	read-only	Slice 3 Dither shadow transfer status value1 = #0 (Dither shadow transfer has not been requested) value2 = #1 (Dither shadow transfer has been requested)
14	S3PSS	read-only	Slice 3 Prescaler shadow transfer status value1 = #0 (Prescaler shadow transfer has not been requested) value2 = #1 (Prescaler shadow transfer has been requested)
16	CC40ST	read-only	Slice 0 status bit
17	CC41ST	read-only	Slice 1 status bit
18	CC42ST	read-only	Slice 2 status bit
19	CC43ST	read-only	Slice 3 status bit
20-31, 15, 11, 7, 3	0	read	Reserved

2.2.8 MIDR

Module Identification

Reset	0x00B6C000
Width	32

Bit-field table (31 … 16)

MODN [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

MODT [15:8]								MODR [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	MODR	read-only	Module Revision
15:8	MODT	read-only	Module Type
31:16	MODN	read-only	Module Number

3 CaptureCompare Unit 8 (CCU8) Registers

Capture Compare Unit 8 - Unit 0

3.1 Register overview

Instance	Base address
CCU80	0x50000000
CCU81	0x50004000
CCU80_CC80	0x50000100
CCU80_CC81	0x50000200
CCU80_CC82	0x50000300
CCU80_CC83	0x50000400
CCU81_CC80	0x50004100
CCU81_CC81	0x50004200
CCU81_CC82	0x50004300
CCU81_CC83	0x50004400

Register name	Offset	Reset	Description
GCTRL	0x00	0x00000000	Global Control Register
GSTAT	0x04	0x0000000F	Global Status Register
GIDLS	0x08	0x00000000	Global Idle Set
GIDLC	0x0C	0x00000000	Global Idle Clear
GCSS	0x10	0x00000000	Global Channel Set
GCSC	0x14	0x00000000	Global Channel Clear
GCST	0x18	0x00000000	Global Channel status
GPCHK	0x1C	0x00000000	Parity Checker Configuration
MIDR	0x80	0x00B7C000	Module Identification

3.2 Register details

3.2.1 GCTRL

Global Control Register

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

MSDE [15:14]		MSE3 [13]	MSE2 [12]	MSE1 [11]	MSE0 [10]	SUSCFG [9:8]		0		PCIS [5:4]		0	PRBC [2:0]		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
2:0	PRBC	read-write	Prescaler Clear Configuration value1 = #000 (SW only) value2 = #001 (GSTATThe register contains the status of the prescaler and each timer slice (idle mode or running)..PRB and prescaler registers are cleared when the Run Bit of CC80 is cleared.) value3 = #010 (GSTATThe register contains the status of the prescaler and each timer slice (idle mode or running)..PRB and prescaler registers are cleared when the Run Bit of CC81 is cleared.) value4 = #011 (GSTATThe register contains the status of the prescaler and each timer slice (idle mode or running)..PRB and prescaler registers are cleared when the Run Bit of CC82 is cleared.) value5 = #100 (GSTATThe register contains the status of the prescaler and each timer slice (idle mode or running)..PRB and prescaler registers are cleared when the Run Bit of CC83 is cleared.)
5:4	PCIS	read-write	Prescaler Input Clock Selection value1 = #00 (Module clock) value2 = #01 (CCU8x.ECLKA) value3 = #10 (CCU8x.ECLKB) value4 = #11 (CCU8x.ECLKC)
9:8	SUSCFG	read-write	Suspend Mode Configuration value1 = #00 (Suspend request ignored. The module never enters in suspend) value2 = #01 (Stops all the running slices immediately. Safe stop is not applied.) value3 = #10 (Stops the block immediately and clamps all the outputs to PASSIVE state. Safe stop is applied.) value4 = #11 (Waits for the roll over of each slice to stop and clamp the slices outputs. Safe stop is applied.)
10	MSE0	read-write	Slice 0 Multi Channel shadow transfer enable value1 = #0 (Shadow transfer can only be requested by SW) value2 = #1 (Shadow transfer can be requested via SW and via the CCU8x.MCSS input.)
11	MSE1	read-write	Slice 1 Multi Channel shadow transfer enable value1 = #0 (Shadow transfer can only be requested by SW) value2 = #1 (Shadow transfer can be requested via SW and via the CCU8x.MCSS input.)
12	MSE2	read-write	Slice 2 Multi Channel shadow transfer enable value1 = #0 (Shadow transfer can only be requested by SW) value2 = #1 (Shadow transfer can be requested via SW and via the CCU8xMCSS input.)
13	MSE3	read-write	Slice 3 Multi Channel shadow transfer enable value1 = #0 (Shadow transfer can only be requested by SW) value2 = #1 (Shadow transfer can be requested via SW and via the CCU8x.MCSS input.)

Bits	Field	Access	Description
15:14	MSDE	read-write	Multi Channel shadow transfer request configuration value1 = #00 (Only the shadow transfer for period and compare values is requested) value2 = #01 (Shadow transfer for the compare, period and prescaler compare values is requested) value4 = #11 (Shadow transfer for the compare, period, prescaler and dither compare values is requested)
16-31, 6-7,	30	read	Reserved

3.2.2 GSTAT

Global Status Register

Reset	0x0000000F
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0					PCRB [10]	0	PRB [8]	0				S3I [3]	S2I [2]	S1I [1]	S0I [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	S0I	read-only	CC80 IDLE status value1 = #0 (Running) value2 = #1 (Idle)
1	S1I	read-only	CC81 IDLE status value1 = #0 (Running) value2 = #1 (Idle)
2	S2I	read-only	CC82 IDLE status value1 = #0 (Running) value2 = #1 (Idle)
3	S3I	read-only	CC83 IDLE status value1 = #0 (Running) value2 = #1 (Idle)
8	PRB	read-only	Prescaler Run Bit value1 = #0 (Prescaler is stopped) value2 = #1 (Prescaler is running)
10	PCRB	read-only	Parity Checker Run Bit value1 = #0 (Parity Checker is stopped) value2 = #1 (Parity Checker is running)
11-31, 9, 4-70		read	Reserved

3.2.3 GIDLS

Global Idle Set

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0					CPCH [10]	PSIC [9]	CPRB [8]	0				SS3I [3]	SS2I [2]	SS1I [1]	SS0I [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	SS0I	write-only	CC80 IDLE mode set
1	SS1I	write-only	CC81 IDLE mode set
2	SS2I	write-only	CC82 IDLE mode set
3	SS3I	write-only	CC83 IDLE mode set
8	CPRB	write-only	Prescaler# Run Bit Clear
9	PSIC	write-only	Prescaler clear
10	CPCH	write-only	Parity Checker Run bit clear
11-31, 4-7	0	read	Reserved

3.2.4 GIDLC

Global Idle Clear

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0					SPCH [10]	0	SPRB [8]	0				CS3I [3]	CS2I [2]	CS1I [1]	CS0I [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	CS0I	write-only	CC80 IDLE mode clear
1	CS1I	write-only	CC81 IDLE mode clear
2	CS2I	write-only	CC82 IDLE mode clear
3	CS3I	write-only	CC83 IDLE mode clear
8	SPRB	write-only	Prescaler Run Bit Set
10	SPCH	write-only	Parity Checker run bit set
11-31, 9, 4-7	0	read	Reserved

3.2.5 GCSS

Global Channel Set

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0								S3ST2S [23]	S2ST2S [22]	S1ST2S [21]	S0ST2S [20]	S3ST1S [19]	S2ST1S [18]	S1ST1S [17]	S0ST1S [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0	S3PSE [14]	S3DSE [13]	S3SE [12]	0	S2PSE [10]	S2DSE [9]	S2SE [8]	0	S1PSE [6]	S1DSE [5]	S1SE [4]	0	S0PSE [2]	S0DSE [1]	S0SE [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	S0SE	write-only	Slice 0 shadow transfer set enable
1	S0DSE	write-only	Slice 0 Dither shadow transfer set enable
2	S0PSE	write-only	Slice 0 Prescaler shadow transfer set enable
4	S1SE	write-only	Slice 1 shadow transfer set enable
5	S1DSE	write-only	Slice 1 Dither shadow transfer set enable
6	S1PSE	write-only	Slice 1 Prescaler shadow transfer set enable
8	S2SE	write-only	Slice 2 shadow transfer set enable
9	S2DSE	write-only	Slice 2 Dither shadow transfer set enable
10	S2PSE	write-only	Slice 2 Prescaler shadow transfer set enable
12	S3SE	write-only	Slice 3 shadow transfer set enable
13	S3DSE	write-only	Slice 3 Dither shadow transfer set enable
14	S3PSE	write-only	Slice 3 Prescaler shadow transfer set enable
16	S0ST1S	write-only	Slice 0 status bit 1 set
17	S1ST1S	write-only	Slice 1 status bit 1 set
18	S2ST1S	write-only	Slice 2 status bit 1 set
19	S3ST1S	write-only	Slice 3 status bit 1 set
20	S0ST2S	write-only	Slice 0 status bit 2 set
21	S1ST2S	write-only	Slice 1 status bit 2 set
22	S2ST2S	write-only	Slice 2 status bit 2 set
23	S3ST2S	write-only	Slice 3 status bit 2 set
24-31, 15, 11, 7, 3	0	read	Reserved

3.2.6 GCSC

Global Channel Clear

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0								S3ST2C [23]	S2ST2C [22]	S1ST2C [21]	S0ST2C [20]	S3ST1C [19]	S2ST1C [18]	S1ST1C [17]	S0ST1C [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0	S3PSC [14]	S3DSC [13]	S3SC [12]	0	S2PSC [10]	S2DSC [9]	S2SC [8]	0	S1PSC [6]	S1DSC [5]	S1SC [4]	0	S0PSC [2]	S0DSC [1]	S0SC [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	S0SC	write-only	Slice 0 shadow transfer request clear
1	S0DSC	write-only	Slice 0 Dither shadow transfer clear
2	S0PSC	write-only	Slice 0 Prescaler shadow transfer clear
4	S1SC	write-only	Slice 1 shadow transfer clear
5	S1DSC	write-only	Slice 1 Dither shadow transfer clear
6	S1PSC	write-only	Slice 1 Prescaler shadow transfer clear
8	S2SC	write-only	Slice 2 shadow transfer clear
9	S2DSC	write-only	Slice 2 Dither shadow transfer clear
10	S2PSC	write-only	Slice 2 Prescaler shadow transfer clear
12	S3SC	write-only	Slice 3 shadow transfer clear
13	S3DSC	write-only	Slice 3 Dither shadow transfer clear
14	S3PSC	write-only	Slice 3 Prescaler shadow transfer clear
16	S0ST1C	write-only	Slice 0 status bit 1 clear
17	S1ST1C	write-only	Slice 1 status bit 1 clear
18	S2ST1C	write-only	Slice 2 status bit 1 clear
19	S3ST1C	write-only	Slice 3 status bit 1 clear
20	S0ST2C	write-only	Slice 0 status bit 2 clear
21	S1ST2C	write-only	Slice 1 status bit 2 clear
22	S2ST2C	write-only	Slice 2 status bit 2 clear
23	S3ST2C	write-only	Slice 3 status bit 2 clear
24-31, 15, 11, 7, 3	0	read	Reserved

3.2.7 GCST

Global Channel status

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0								CC83S T2 [23]	CC82S T2 [22]	CC81S T2 [21]	CC80S T2 [20]	CC83S T1 [19]	CC82S T1 [18]	CC81S T1 [17]	CC80S T1 [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0	S3PSS [14]	S3DSS [13]	S3SS [12]	0	S2PSS [10]	S2DSS [9]	S2SS [8]	0	S1PSS [6]	S1DSS [5]	S1SS [4]	0	S0PSS [2]	S0DSS [1]	S0SS [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	S0SS	read-only	Slice 0 shadow transfer status value1 = #0 (Shadow transfer has not been requested) value2 = #1 (Shadow transfer has been requested)
1	S0DSS	read-only	Slice 0 Dither shadow transfer status value1 = #0 (Dither shadow transfer has not been requested) value2 = #1 (Dither shadow transfer has been requested)
2	S0PSS	read-only	Slice 0 Prescaler shadow transfer status value1 = #0 (Prescaler shadow transfer has not been requested) value2 = #1 (Prescaler shadow transfer has been requested)
4	S1SS	read-only	Slice 1 shadow transfer status value1 = #0 (Shadow transfer has not been requested) value2 = #1 (Shadow transfer has been requested)
5	S1DSS	read-only	Slice 1 Dither shadow transfer status value1 = #0 (Dither shadow transfer has not been requested) value2 = #1 (Dither shadow transfer has been requested)
6	S1PSS	read-only	Slice 1 Prescaler shadow transfer status value1 = #0 (Prescaler shadow transfer has not been requested) value2 = #1 (Prescaler shadow transfer has been requested)
8	S2SS	read-only	Slice 2 shadow transfer status value1 = #0 (Shadow transfer has not been requested) value2 = #1 (Shadow transfer has been requested)
9	S2DSS	read-only	Slice 2 Dither shadow transfer status value1 = #0 (Dither shadow transfer has not been requested) value2 = #1 (Dither shadow transfer has been requested)
10	S2PSS	read-only	Slice 2 Prescaler shadow transfer status value1 = #0 (Prescaler shadow transfer has not been requested) value2 = #1 (Prescaler shadow transfer has been requested)
12	S3SS	read-only	Slice 3 shadow transfer status value1 = #0 (Shadow transfer has not been requested) value2 = #1 (Shadow transfer has been requested)
13	S3DSS	read-only	Slice 3 Dither shadow transfer status value1 = #0 (Dither shadow transfer has not been requested) value2 = #1 (Dither shadow transfer has been requested)
14	S3PSS	read-only	Slice 3 Prescaler shadow transfer status value1 = #0 (Prescaler shadow transfer has not been requested) value2 = #1 (Prescaler shadow transfer has been requested)
16	CC80ST1	read-only	Slice 0 compare channel 1 status bit
17	CC81ST1	read-only	Slice 1 compare channel 1 status bit
18	CC82ST1	read-only	Slice 2 compare channel 1 status bit
19	CC83ST1	read-only	Slice 3 compare channel 1 status bit
20	CC80ST2	read-only	Slice 0 compare channel 2 status bit
21	CC81ST2	read-only	Slice 1 compare channel 2 status bit
22	CC82ST2	read-only	Slice 2 compare channel 2 status bit

Bits	Field	Access	Description
23	CC83ST2	read-only	Slice 3 compare channel 2 status bit
24-31, 15, 11, 7, 3	0	read	Reserved

3.2.8 GPCHK

Parity Checker Configuration

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PCSEL3 [31:28]				PCSEL2 [27:24]				PCSEL1 [23:20]				PCSEL0 [19:16]			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PCST [15]	0							PCTS [7]	PCDS [6:5]		PISEL [4:3]		PACS [2:1]		PASE [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	PASE	read-write	Parity Checker Automatic start/stop
2:1	PACS	read-write	Parity Checker Automatic start/stop selector value1 = #00 (CC80) value2 = #01 (CC81) value3 = #10 (CC82) value4 = #11 (CC83)
4:3	PISEL	read-write	Driver Input signal selector value1 = #00 (CC8x.GP01 - driver output is connected to event 1 of slice 0) value2 = #01 (CC8x.GP11 - drive output is connected to event 1 of slice 1) value3 = #10 (CC8x.GP21 - driver output is connected to event 1 of slice 2) value4 = #11 (CC8x.GP31 - driver output is connected to event 1 of slice 3)
6:5	PCDS	read-write	Parity Checker Delay Input Selector value1 = #00 (CCU8x.IGBTA) value2 = #01 (CCU8x.IGBTB) value3 = #10 (CCU8x.IGBTC) value4 = #11 (CCU8x.IGBTD)
7	PCTS	read-write	Parity Checker type selector value1 = #0 (Even parity enabled) value2 = #1 (Odd parity enabled)
15	PCST	read-only	Parity Checker XOR status
19:16	PCSEL0	read-write	Parity Checker Slice 0 output selection
23:20	PCSEL1	read-write	Parity Checker Slice 1 output selection
27:24	PCSEL2	read-write	Parity Checker Slice 2 output selection
31:28	PCSEL3	read-write	Parity Checker Slice 3 output selection
8-14	0	read	Reserved

3.2.9 MIDR

Module Identification

Reset	0x00B7C000
Width	32

Bit-field table (31 … 16)

MODN [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

MODT [15:8]								MODR [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	MODR	read-only	Module Revision
15:8	MODT	read-only	Module Type
31:16	MODN	read-only	Module Number

4 Comparators Registers

System Control Unit

4.1 Register overview

Instance	Base address
COMPARATOR	0x40010500

Register name	Offset	Reset	Description
ORCCTRL	0x00	0x00000000	Out Of Range Comparator Control Register
ANACMP0	0xB5C	0x0020	Analog Comparator 0 Control Register
ANACMP1	0xB60	0x0020	Analog Comparator 1 Control Register
ANACMP2	0xB64	0x0020	Analog Comparator 2 Control Register
ANACMP3	0xB68	0x0020	Analog Comparator 3 Control Register

4.2 Register details

4.2.1 ORCCTRL

Out Of Range Comparator Control Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0								CNF7 [23]	CNF6 [22]	CNF5 [21]	CNF4 [20]	CNF3 [19]	CNF2 [18]	CNF1 [17]	CNF0 [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0								ENOR C7 [7]	ENOR C6 [6]	ENOR C5 [5]	ENOR C4 [4]	ENOR C3 [3]	ENOR C2 [2]	ENOR C1 [1]	ENOR C0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	ENORC0	read-write	Enable Out of Range Comparator 0 value1 = #0 (Out of range comparator disabled.) value2 = #1 (Out of range comparator enabled.)
1	ENORC1	read-write	Enable Out of Range Comparator 1 value1 = #0 (Out of range comparator disabled.) value2 = #1 (Out of range comparator enabled.)
2	ENORC2	read-write	Enable Out of Range Comparator 2 value1 = #0 (Out of range comparator disabled.) value2 = #1 (Out of range comparator enabled.)
3	ENORC3	read-write	Enable Out of Range Comparator 3 value1 = #0 (Out of range comparator disabled.) value2 = #1 (Out of range comparator enabled.)
4	ENORC4	read-write	Enable Out of Range Comparator 4 value1 = #0 (Out of range comparator disabled.) value2 = #1 (Out of range comparator enabled.)
5	ENORC5	read-write	Enable Out of Range Comparator 5 value1 = #0 (Out of range comparator disabled.) value2 = #1 (Out of range comparator enabled.)
6	ENORC6	read-write	Enable Out of Range Comparator 6 value1 = #0 (Out of range comparator disabled.) value2 = #1 (Out of range comparator enabled.)
7	ENORC7	read-write	Enable Out of Range Comparator 7 value1 = #0 (Out of range comparator disabled.) value2 = #1 (Out of range comparator enabled.)
16	CNF0	read-write	Out of Range Comparator Flag 0 value1 = #0 (Falling edge trigger out of range event register.) value2 = #1 (Rising edge trigger out of range event register.)
17	CNF1	read-write	Out of Range Comparator Flag 1 value1 = #0 (Falling edge trigger out of range event register.) value2 = #1 (Rising edge trigger out of range event register.)
18	CNF2	read-write	Out of Range Comparator Flag 2 value1 = #0 (Falling edge trigger out of range event register.) value2 = #1 (Rising edge trigger out of range event register.)
19	CNF3	read-write	Out of Range Comparator Flag 3 value1 = #0 (Falling edge trigger out of range event register.) value2 = #1 (Rising edge trigger out of range event register.)
20	CNF4	read-write	Out of Range Comparator Flag 4 value1 = #0 (Falling edge trigger out of range event register.) value2 = #1 (Rising edge trigger out of range event register.)
21	CNF5	read-write	Out of Range Comparator Flag 5 value1 = #0 (Falling edge trigger out of range event register.) value2 = #1 (Rising edge trigger out of range event register.)
22	CNF6	read-write	Out of Range Comparator Flag 6 value1 = #0 (Falling edge trigger out of range event register.) value2 = #1 (Rising edge trigger out of range event register.)

Bits	Field	Access	Description
23	CNF7	read-write	Out of Range Comparator Flag 7 value1 = #0 (Falling edge trigger out of range event register.) value2 = #1 (Rising edge trigger out of range event register.)
24-31, 8-15	0	read	Reserved

4.2.2 ANACMP0

Analog Comparator 0 Control Register

Reset 0x0020

Width 16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

CMP_OUT [15]	0	CMP_LPWR [8]	0	ACMP0_SEL [6]	CMP_HYST_ADJ [5:4]	CMP_INV_OUT [3]	0	CMP_FLT_OFF [1]	CMP_EN [0]
15	14 13 12 11 10 9	8	7	6	5 4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	CMP_EN	read-write	Comparator enable value1 = #0 (Comparator is disabled) value2 = #1 (Comparator is enabled)
1	CMP_FLT_OFF	read-write	Disables comparator filter value1 = #0 (filter is active) value2 = #1 (filter is switched off (to prevent a filter delay))
3	CMP_INV_OUT	read-write	Inverted Comparator output value1 = #0 (no inversion of comparator signal) value2 = #1 (comparator signal is inverted)
5:4	CMP_HYST_ADJ	read-write	Comparator hysteresis adjust value1 = #00 (Comparator hysteresis is switched off) value2 = #01 (Hysteresis_typ = 10mV) value3 = #10 (Hysteresis_typ = 15mV) value4 = #11 (Hysteresis_typ = 20mV)
6	ACMP0_SEL	read-write	Connect ACMP0.INN to ACMP1.INP value1 = #0 (ACMP0.INN is not connected) value2 = #1 (ACMP0.INN is connected to ACMP1.INP)
8	CMP_LPWR	read-write	Low Power Mode value1 = #0 (High Power Mode) value2 = #1 (Low Power Mode)
15	CMP_OUT	read-only	Comparator output monitor bit value1 = #0 (state "Vminus > Vplus") value2 = #1 (state "Vminus < Vplus")
9-14, 7, 2	0	read	Reserved

4.2.3 ANACMP1

Analog Comparator 1 Control Register

Reset	0x0020
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

CMP_OUT [15]	0	REF_DIV_EN [6]	CMP_HYST_ADJ [5:4]	CMP_INV_OUT [3]	0	CMP_FLT_OFF [1]	CMP_EN [0]
15	14 13 12 11 10 9 8 7	6	5 4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	CMP_EN	read-write	Comparator enable value1 = #0 (Comparator is disabled) value2 = #1 (Comparator is enabled)
1	CMP_FLT_OFF	read-write	Disables comparator filter value1 = #0 (filter is active) value2 = #1 (filter is switched off (to prevent a filter delay))
3	CMP_INV_OUT	read-write	Inverted Comparator output value1 = #0 (no inversion of comparator signal) value2 = #1 (comparator signal is inverted)
5:4	CMP_HYST_ADJ	read-write	Comparator hysteresis adjust value1 = #00 (Comparator hysteresis is switched off) value2 = #01 (Hysteresis_typ = 10mV) value3 = #10 (Hysteresis_typ = 15mV) value4 = #11 (Hysteresis_typ = 20mV)
6	REF_DIV_EN	read-write	Resistor Divider is enabled and Reference Voltage is applied to ACMP1 value1 = #0 (no resistor is connected) value2 = #1 (the divider resistor is enabled and the voltage is applied to ACMP1.INP)
15	CMP_OUT	read-only	Comparator output monitor bit value1 = #0 (state "Vminus > Vplus") value2 = #1 (state "Vminus < Vplus")
7-14, 2	0	read	Reserved

4.2.4 ANACMP2

Analog Comparator 2 Control Register

Reset	0x0020
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

CMP_OUT [15]	0								ACMP2_SEL [6]	CMP_HYST_ADJ [5:4]		CMP_INV_OUT [3]	0	CMP_FLT_OFF [1]	CMP_EN [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	CMP_EN	read-write	Comparator enable value1 = #0 (Comparator is disabled) value2 = #1 (Comparator is enabled)
1	CMP_FLT_OFF	read-write	Disables comparator filter value1 = #0 (filter is active) value2 = #1 (filter is switched off (to prevent a filter delay))
3	CMP_INV_OUT	read-write	Inverted Comparator output value1 = #0 (no inversion of comparator signal) value2 = #1 (comparator signal is inverted)
5:4	CMP_HYST_ADJ	read-write	Comparator hysteresis adjust value1 = #00 (Comparator hysteresis is switched off) value2 = #01 (Hysteresis_typ = 10mV) value3 = #10 (Hysteresis_typ = 15mV) value4 = #11 (Hysteresis_typ = 20mV)
6	ACMP2_SEL	read-write	Connect ACMP2.INP to ACMP1.INP value1 = #0 (ACMP2.INP is not connected) value2 = #1 (ACMP2.INP is connected to ACMP1.INP)
15	CMP_OUT	read-only	Comparator output monitor bit value1 = #0 (state "Vminus > Vplus") value2 = #1 (state "Vminus < Vplus")
7-14, 2	0	read	Reserved

4.2.5 ANACMP3

Analog Comparator 3 Control Register

Reset	0x0020
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

CMP_OUT [15]	0								ACMP3_SEL [6]	CMP_HYST_ADJ [5:4]		CMP_INV_OUT [3]	0	CMP_FLT_OFF [1]	CMP_EN [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	CMP_EN	read-write	Comparator enable value1 = #0 (Comparator is disabled) value2 = #1 (Comparator is enabled)
1	CMP_FLT_OFF	read-write	Disables comparator filter value1 = #0 (filter is active) value2 = #1 (filter is switched off (to prevent a filter delay))
3	CMP_INV_OUT	read-write	Inverted Comparator output value1 = #0 (no inversion of comparator signal) value2 = #1 (comparator signal is inverted)
5:4	CMP_HYST_ADJ	read-write	Comparator hysteresis adjust value1 = #00 (Comparator hysteresis is switched off) value2 = #01 (Hysteresis_typ = 10mV) value3 = #10 (Hysteresis_typ = 15mV) value4 = #11 (Hysteresis_typ = 20mV)
6	ACMP3_SEL	read-write	Connect ACMP3.INP to ACMP1.INP value1 = #0 (ACMP3.INP is not connected) value2 = #1 (ACMP3.INP is connected to ACMP1.INP)
15	CMP_OUT	read-only	Comparator output monitor bit value1 = #0 (state "Vminus > Vplus") value2 = #1 (state "Vminus < Vplus")
7-14, 2	0	read	Reserved

5 Controller Area Network Controller (MultiCAN+) Registers

Controller Area Networks

5.1 Register overview

Instance	Base address
CAN	0x50040000
CAN_NODE0	0x50040200
CAN_NODE1	0x50040300
CAN_MO	0x50041000

Register name	Offset	Reset	Description
CLC	0x00	0x00000003	CAN Clock Control Register
ID	0x08	0x00B5C000	Module Identification Register
FDR	0x0C	0x00000000	CAN Fractional Divider Register
LIST[%s]	0x100	0x00000000	List Register
MSPND[%s]	0x140	0x00000000	Message Pending Register
MSID[%s]	0x180	0x00000020	Message Index Register
MSIMASK	0x1C0	0x00000000	Message Index Mask Register
PANCTR	0x1C4	0x00000301	Panel Control Register
MCR	0x1C8	0x00000000	Module Control Register
MITR	0x1CC	0x00000000	Module Interrupt Trigger Register

5.2 Register details

5.2.1 CLC

CAN Clock Control Register

Reset	0x00000003
Width	32

Bit-field table (31 … 16)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															

Bit-field table (15 … 0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												EDIS [3]	0	DISS [1]	DISR [0]

Bit-fields

Bits	Field	Access	Description
0	DISR	read-write	Module Disable Request Bit
1	DISS	read-only	Module Disable Status Bit
3	EDIS	read-write	Sleep Mode Enable Control
4-31, 2	0	read	Reserved

5.2.2 ID

Module Identification Register

Reset	0x00B5C000
Width	32

Bit-field table (31 … 16)

MOD_NUMBER [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

MOD_TYPE [15:8]								MOD_REV [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	MOD_REV	read-only	Module Revision Number
15:8	MOD_TYPE	read-only	Module Type value1 = 0xC0 (Define the module as a 32-bit module.)
31:16	MOD_NUMBER	read-only	Module Number Value

5.2.3 FDR

CAN Fractional Divider Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

DM [15:14]		0				STEP [9:0]									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
9:0	STEP	read-write	Step Value
15:14	DM	read-write	Divider Mode
16-31, 10-13	0	read	Reserved

5.2.4 LIST[%s]

List Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0	EMPTY [24]	SIZE [23:16]
31 30 29 28 27 26 25	24	23 22 21 20 19 18 17 16

Bit-field table (15 … 0)

END [15:8]	BEGIN [7:0]
15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0

Bit-fields

Bits	Field	Access	Description
7:0	BEGIN	read-only	List Begin
15:8	END	read-only	List End
23:16	SIZE	read-only	List Size
24	EMPTY	read-only	List Empty Indication value1 = #0 (At least one message object is allocated to list i.) value2 = #1 (No message object is allocated to the list i. List i is empty.)
25-31	0	read	Reserved

5.2.5 MSPND[%s]

Message Pending Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PND [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PND [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:0	PND	read-write	Message Pending

5.2.6 MSID[%s]

Message Index Register

Reset	0x00000020
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0										INDEX [5:0]					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
5:0	INDEX	read-only	Message Pending Index
6-31	0	read	Reserved

5.2.7 MSIMASK

Message Index Mask Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

IM [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

IM [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:0	IM	read-write	Message Index Mask

5.2.8 PANCTR

Panel Control Register

Reset	0x00000301
Width	32

Bit-field table (31 … 16)

PANAR2 [31:24]								PANAR1 [23:16]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0						RBUSY [9]	BUSY [8]	PANCMD [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	PANCMD	read-write	Panel Command
8	BUSY	read-only	Panel Busy Flag value1 = #0 (Panel has finished command and is ready to accept a new command.) value2 = #1 (Panel operation is in progress.)
9	RBUSY	read-only	Result Busy Flag value1 = #0 (No update of PANAR1 and PANAR2 is scheduled by the list controller.) value2 = #1 (A list command is running (BUSY = 1) that will write results to PANAR1 and PANAR2, but the results are not yet available.)
23:16	PANAR1	read-write	Panel Argument 1
31:24	PANAR2	read-write	Panel Argument 2
10-15	0	read	Reserved

5.2.9 MCR

Module Control Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

MPSEL [15:12]				0								CLKSEL [3:0]			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
3:0	CLKSEL	read-write	Baud Rate Logic Clock Select value1 = #0000 (No clock supplied) value2 = #0001 (fMCLK) value3 = #0010 (fOSC_HP) value4 = #0100 (hard wired to 0) value5 = #1000 (hard wired to 0)
15:12	MPSEL	read-write	Message Pending Selector
16-31, 4-11	0	read	Reserved

5.2.10 MITR

Module Interrupt Trigger Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0								IT [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	IT	write-only	Interrupt Trigger
8-31	0	read	Reserved

6 Event Request Unit Registers

Event Request Unit 0

6.1 Register overview

Instance	Base address
ERU0	0x40010600
ERU1	0x40010630

Register name	Offset	Reset	Description
EXISEL	0x00	0x00000000	Event Input Select
EXICON[%s]	0x10	0x00000000	Event Input Control
EXOCON[%s]	0x20	0x00000008	Event Output Trigger Control

6.2 Register details

6.2.1 EXISEL

Event Input Select

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

EXS3B [15:14]		EXS3A [13:12]		EXS2B [11:10]		EXS2A [9:8]		EXS1B [7:6]		EXS1A [5:4]		EXS0B [3:2]		EXS0A [1:0]	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
1:0	EXS0A	read-write	Event Source Select for A0 (ERS0) value1 = #00 (Input ERU_0A0 is selected) value2 = #01 (Input ERU_0A1 is selected) value3 = #10 (Input ERU_0A2 is selected) value4 = #11 (Input ERU_0A3 is selected)
3:2	EXS0B	read-write	Event Source Select for B0 (ERS0) value1 = #00 (Input ERU_0B0 is selected) value2 = #01 (Input ERU_0B1 is selected) value3 = #10 (Input ERU_0B2 is selected) value4 = #11 (Input ERU_0B3 is selected)
5:4	EXS1A	read-write	Event Source Select for A1 (ERS1) value1 = #00 (Input ERU_1A0 is selected) value2 = #01 (Input ERU_1A1 is selected) value3 = #10 (Input ERU_1A2 is selected) value4 = #11 (Input ERU_1A3 is selected)
7:6	EXS1B	read-write	Event Source Select for B1 (ERS1) value1 = #00 (Input ERU_1B0 is selected) value2 = #01 (Input ERU_1B1 is selected) value3 = #10 (Input ERU_1B2 is selected) value4 = #11 (Input ERU_1B3 is selected)
9:8	EXS2A	read-write	Event Source Select for A2 (ERS2) value1 = #00 (Input ERU_2A0 is selected) value2 = #01 (Input ERU_2A1 is selected) value3 = #10 (Input ERU_2A2 is selected) value4 = #11 (Input ERU_2A3 is selected)
11:10	EXS2B	read-write	Event Source Select for B2 (ERS2) value1 = #00 (Input ERU_2B0 is selected) value2 = #01 (Input ERU_2B1 is selected) value3 = #10 (Input ERU_2B2 is selected) value4 = #11 (Input ERU_2B3 is selected)
13:12	EXS3A	read-write	Event Source Select for A3 (ERS3) value1 = #00 (Input ERU_3A0 is selected) value2 = #01 (Input ERU_3A1 is selected) value3 = #10 (Input ERU_3A2 is selected) value4 = #11 (Input ERU_3A3 is selected)
15:14	EXS3B	read-write	Event Source Select for B3 (ERS3) value1 = #00 (Input ERU_3B0 is selected) value2 = #01 (Input ERU_3B1 is selected) value3 = #10 (Input ERU_3B2 is selected) value4 = #11 (Input ERU_3B3 is selected)
16-31	0	read	Reserved

6.2.2 EXICON[%s]

Event Input Control

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0				NB [11]	NA [10]	SS [9:8]		FL [7]	OCS [6:4]			FE [3]	RE [2]	LD [1]	PE [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	PE	read-write	Output Trigger Pulse Enable for ETLx value1 = #0 (The trigger pulse generation is disabled) value2 = #1 (The trigger pulse generation is enabled)
1	LD	read-write	Rebuild Level Detection for Status Flag for ETLx value1 = #0 (The status flag FL is not cleared by hardware and is used as "sticky" bit. Once set, it is not influenced by any edge until it becomes cleared by software.) value2 = #1 (The status flag FL rebuilds a level detection of the desired event. It becomes automatically set with a rising edge if RE = 1 or with a falling edge if FE = 1. It becomes automatically cleared with a rising edge if RE = 0 or with a falling edge if FE = 0.)
2	RE	read-write	Rising Edge Detection Enable ETLx value1 = #0 (A rising edge is not considered as edge event) value2 = #1 (A rising edge is considered as edge event)
3	FE	read-write	Falling Edge Detection Enable ETLx value1 = #0 (A falling edge is not considered as edge event) value2 = #1 (A falling edge is considered as edge event)
6:4	OCS	read-write	Output Channel Select for ETLx Output Trigger Pulse value1 = #000 (Trigger pulses are sent to OGU0) value2 = #001 (Trigger pulses are sent to OGU1) value3 = #010 (Trigger pulses are sent to OGU2) value4 = #011 (Trigger pulses are sent to OGU3)
7	FL	read-write	Status Flag for ETLx value1 = #0 (The enabled edge event has not been detected) value2 = #1 (The enabled edge event has been detected)
9:8	SS	read-write	Input Source Select for ERSx value1 = #00 (Input A without additional combination) value2 = #01 (Input B without additional combination) value3 = #10 (Input A OR input B) value4 = #11 (Input A AND input B)
10	NA	read-write	Input A Negation Select for ERSx value1 = #0 (Input A is used directly) value2 = #1 (Input A is inverted)
11	NB	read-write	Input B Negation Select for ERSx value1 = #0 (Input B is used directly) value2 = #1 (Input B is inverted)
12-31	0	read	Reserved

6.2.3 EXOCON[%s]

Event Output Trigger Control

Reset	0x00000008
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

IPEN3 [15]	IPEN2 [14]	IPEN1 [13]	IPEN0 [12]	0						GP [5:4]		PDR [3]	GEEN [2]	ISS [1:0]	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
1:0	ISS	read-write	Internal Trigger Source Selection value1 = #00 (The peripheral trigger function is disabled) value2 = #01 (Input ERU_OGUy1 is selected) value3 = #10 (Input ERU_OGUy2 is selected) value4 = #11 (Input ERU_OGUy3 is selected)
2	GEEN	read-write	Gating Event Enable value1 = #0 (The event detection is disabled) value2 = #1 (The event detection is enabled)
3	PDR	read-only	Pattern Detection Result Flag value1 = #0 (A pattern miss is detected) value2 = #1 (A pattern match is detected)
5:4	GP	read-write	Gating Selection for Pattern Detection Result value1 = #00 (ERU_GOUTy is always disabled and ERU_IOUTy can not be activated) value2 = #01 (ERU_GOUTy is always enabled and ERU_IOUTy becomes activated with each activation of ERU_TOUTy) value3 = #10 (ERU_GOUTy is equal to ERU_PDOUTy and ERU_IOUTy becomes activated with an activation of ERU_TOUTy while the desired pattern is detected (pattern match PDR = 1)) value4 = #11 (ERU_GOUTy is inverted to ERU_PDOUTy and ERU_IOUTy becomes activated with an activation of ERU_TOUTy while the desired pattern is not detected (pattern miss PDR = 0))
12	IPEN0	read-write	Pattern Detection Enable for ETL0 value1 = #0 (Flag EXICONx.FL is excluded from the pattern detection) value2 = #1 (Flag EXICONx.FL is included in the pattern detection)
13	IPEN1	read-write	Pattern Detection Enable for ETL1 value1 = #0 (Flag EXICONx.FL is excluded from the pattern detection) value2 = #1 (Flag EXICONx.FL is included in the pattern detection)
14	IPEN2	read-write	Pattern Detection Enable for ETL2 value1 = #0 (Flag EXICONx.FL is excluded from the pattern detection) value2 = #1 (Flag EXICONx.FL is included in the pattern detection)
15	IPEN3	read-write	Pattern Detection Enable for ETL3 value1 = #0 (Flag EXICONx.FL is excluded from the pattern detection) value2 = #1 (Flag EXICONx.FL is included in the pattern detection)
16-31, 6-11	0	read	Reserved

7 General Purpose IO Ports (Ports) – GPIO Registers

Port 0

7.1 Register overview

Instance	Base address
PORT0	0x40040000

Register name	Offset	Reset	Description
OUT	0x00	0x00000000	Port 0 Output Register
OMR	0x04	0x00000000	Port 0 Output Modification Register
IOCR0	0x10	0x00000000	Port 0 Input/Output Control Register 0
IOCR4	0x14	0x00000000	Port 0 Input/Output Control Register 4
IOCR8	0x18	0x00000000	Port 0 Input/Output Control Register 8
IOCR12	0x1C	0x00000000	Port 0 Input/Output Control Register 12
PHCR0	0x40	0x00000000	Port 0 Pad Hysteresis Control Register 0
PHCR1	0x44	0x00000000	Port 0 Pad Hysteresis Control Register 1
PDISC	0x60	0x00000000	Port 0 Pin Function Decision Control Register
IN	0x24	0x00000000	Port 0 Input Register
PPS	0x70	0x00000000	Port 0 Pin Power Save Register
HWSEL	0x74	0x00000000	Port 0 Pin Hardware Select Register

7.2 Register details

7.2.1 OUT

Port 0 Output Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

P15 [15]	P14 [14]	P13 [13]	P12 [12]	P11 [11]	P10 [10]	P9 [9]	P8 [8]	P7 [7]	P6 [6]	P5 [5]	P4 [4]	P3 [3]	P2 [2]	P1 [1]	P0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	P0	read-write	Port 0 Output Bit 0 value1 = #0 (The output level of P0.x is 0.) value2 = #1 (The output level of P0.x is 1.)
1	P1	read-write	Port 0 Output Bit 1 value1 = #0 (The output level of P0.x is 0.) value2 = #1 (The output level of P0.x is 1.)
2	P2	read-write	Port 0 Output Bit 2 value1 = #0 (The output level of P0.x is 0.) value2 = #1 (The output level of P0.x is 1.)
3	P3	read-write	Port 0 Output Bit 3 value1 = #0 (The output level of P0.x is 0.) value2 = #1 (The output level of P0.x is 1.)
4	P4	read-write	Port 0 Output Bit 4 value1 = #0 (The output level of P0.x is 0.) value2 = #1 (The output level of P0.x is 1.)
5	P5	read-write	Port 0 Output Bit 5 value1 = #0 (The output level of P0.x is 0.) value2 = #1 (The output level of P0.x is 1.)
6	P6	read-write	Port 0 Output Bit 6 value1 = #0 (The output level of P0.x is 0.) value2 = #1 (The output level of P0.x is 1.)
7	P7	read-write	Port 0 Output Bit 7 value1 = #0 (The output level of P0.x is 0.) value2 = #1 (The output level of P0.x is 1.)
8	P8	read-write	Port 0 Output Bit 8 value1 = #0 (The output level of P0.x is 0.) value2 = #1 (The output level of P0.x is 1.)
9	P9	read-write	Port 0 Output Bit 9 value1 = #0 (The output level of P0.x is 0.) value2 = #1 (The output level of P0.x is 1.)
10	P10	read-write	Port 0 Output Bit 10 value1 = #0 (The output level of P0.x is 0.) value2 = #1 (The output level of P0.x is 1.)
11	P11	read-write	Port 0 Output Bit 11 value1 = #0 (The output level of P0.x is 0.) value2 = #1 (The output level of P0.x is 1.)
12	P12	read-write	Port 0 Output Bit 12 value1 = #0 (The output level of P0.x is 0.) value2 = #1 (The output level of P0.x is 1.)
13	P13	read-write	Port 0 Output Bit 13 value1 = #0 (The output level of P0.x is 0.) value2 = #1 (The output level of P0.x is 1.)
14	P14	read-write	Port 0 Output Bit 14 value1 = #0 (The output level of P0.x is 0.) value2 = #1 (The output level of P0.x is 1.)

Bits	Field	Access	Description
15	P15	read-write	Port 0 Output Bit 15 value1 = #0 (The output level of P0.x is 0.) value2 = #1 (The output level of P0.x is 1.)
16-31	0	read	Reserved

7.2.2 OMR

Port 0 Output Modification Register

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

PR15 [31]	PR14 [30]	PR13 [29]	PR12 [28]	PR11 [27]	PR10 [26]	PR9 [25]	PR8 [24]	PR7 [23]	PR6 [22]	PR5 [21]	PR4 [20]	PR3 [19]	PR2 [18]	PR1 [17]	PR0 [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PS15 [15]	PS14 [14]	PS13 [13]	PS12 [12]	PS11 [11]	PS10 [10]	PS9 [9]	PS8 [8]	PS7 [7]	PS6 [6]	PS5 [5]	PS4 [4]	PS3 [3]	PS2 [2]	PS1 [1]	PS0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	PS0	write-only	Port 0 Set Bit 0
1	PS1	write-only	Port 0 Set Bit 1
2	PS2	write-only	Port 0 Set Bit 2
3	PS3	write-only	Port 0 Set Bit 3
4	PS4	write-only	Port 0 Set Bit 4
5	PS5	write-only	Port 0 Set Bit 5
6	PS6	write-only	Port 0 Set Bit 6
7	PS7	write-only	Port 0 Set Bit 7
8	PS8	write-only	Port 0 Set Bit 8
9	PS9	write-only	Port 0 Set Bit 9
10	PS10	write-only	Port 0 Set Bit 10
11	PS11	write-only	Port 0 Set Bit 11
12	PS12	write-only	Port 0 Set Bit 12
13	PS13	write-only	Port 0 Set Bit 13
14	PS14	write-only	Port 0 Set Bit 14
15	PS15	write-only	Port 0 Set Bit 15
16	PR0	write-only	Port 0 Reset Bit 0
17	PR1	write-only	Port 0 Reset Bit 1
18	PR2	write-only	Port 0 Reset Bit 2
19	PR3	write-only	Port 0 Reset Bit 3
20	PR4	write-only	Port 0 Reset Bit 4
21	PR5	write-only	Port 0 Reset Bit 5
22	PR6	write-only	Port 0 Reset Bit 6
23	PR7	write-only	Port 0 Reset Bit 7
24	PR8	write-only	Port 0 Reset Bit 8
25	PR9	write-only	Port 0 Reset Bit 9
26	PR10	write-only	Port 0 Reset Bit 10
27	PR11	write-only	Port 0 Reset Bit 11
28	PR12	write-only	Port 0 Reset Bit 12
29	PR13	write-only	Port 0 Reset Bit 13
30	PR14	write-only	Port 0 Reset Bit 14
31	PR15	write-only	Port 0 Reset Bit 15

7.2.3 IOCR0

Port 0 Input/Output Control Register 0

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PC3 [31:26]						0		PC2 [23:18]						0	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PC1 [15:10]						0		PC0 [7:2]						0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:2	PC0	read-write	Port Control for Port n Pin 0 to 3 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
15:10	PC1	read-write	Port Control for Port n Pin 0 to 3 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
23:18	PC2	read-write	Port Control for Port n Pin 0 to 3 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
31:26	PC3	read-write	Port Control for Port n Pin 0 to 3 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)
24-25, 16-17, 8-9, 0-1		read	Reserved

7.2.4 IOCR4

Port 0 Input/Output Control Register 4

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PC7 [31:26]						0		PC6 [23:18]						0	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PC5 [15:10]						0		PC4 [7:2]						0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:2	PC4	read-write	Port Control for Port n Pin 4 to 7 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
15:10	PC5	read-write	Port Control for Port n Pin 4 to 7 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
23:18	PC6	read-write	Port Control for Port n Pin 4 to 7 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
31:26	PC7	read-write	Port Control for Port n Pin 4 to 7 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)
24-25, 16-17, 8-9, 0-1		read	Reserved

7.2.5 IOCR8

Port 0 Input/Output Control Register 8

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PC11 [31:26]						0		PC10 [23:18]						0	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PC9 [15:10]						0		PC8 [7:2]						0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:2	PC8	read-write	Port Control for Port n Pin 8 to 11 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
15:10	PC9	read-write	Port Control for Port n Pin 8 to 11 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
23:18	PC10	read-write	Port Control for Port n Pin 8 to 11 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
31:26	PC11	read-write	Port Control for Port n Pin 8 to 11 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)
24-25, 16-17	08-9, 0-1	read	Reserved

7.2.6 IOCR12

Port 0 Input/Output Control Register 12

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PC15 [31:26]						0		PC14 [23:18]						0	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PC13 [15:10]						0		PC12 [7:2]						0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:2	PC12	read-write	Port Control for Port n Pin 12 to 15 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
15:10	PC13	read-write	Port Control for Port n Pin 12 to 15 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
23:18	PC14	read-write	Port Control for Port n Pin 12 to 15 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
31:26	PC15	read-write	Port Control for Port n Pin 12 to 15 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)
24-25, 16-17	08-9, 0-1	read	Reserved

7.2.7 PHCR0

Port 0 Pad Hysteresis Control Register 0

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0	PH7 [30]	0	PH6 [26]	0	PH5 [22]	0	PH4 [18]	0
31	30	29 28 27	26	25 24 23	22	21 20 19	18	17 16

Bit-field table (15 … 0)

0	PH3 [14]	0	PH2 [10]	0	PH1 [6]	0	PH0 [2]	0
15	14	13 12 11	10	9 8 7	6	5 4 3	2	1 0

Bit-fields

Bits	Field	Access	Description
2	PH0	read-write	Pad Hysteresis for Pn.0
6	PH1	read-write	Pad Hysteresis for Pn.1
10	PH2	read-write	Pad Hysteresis for Pn.2
14	PH3	read-write	Pad Hysteresis for Pn.3
18	PH4	read-write	Pad Hysteresis for Pn.4
22	PH5	read-write	Pad Hysteresis for Pn.5
26	PH6	read-write	Pad Hysteresis for Pn.6
30	PH7	read-write	Pad Hysteresis for Pn.7
31, 27-29, 23-25, 19-21, 15-17, 11-13, 7-9, 3-5, 0-1		read	Reserved

7.2.8 PHCR1

Port 0 Pad Hysteresis Control Register 1

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0	PH15 [30]	0			PH14 [26]	0			PH13 [22]	0			PH12 [18]	0	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0	PH11 [14]	0			PH10 [10]	0			PH9 [6]	0			PH8 [2]	0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
2	PH8	read-write	Pad Hysteresis for P0.8
6	PH9	read-write	Pad Hysteresis for P0.9
10	PH10	read-write	Pad Hysteresis for P0.10
14	PH11	read-write	Pad Hysteresis for P0.11
18	PH12	read-write	Pad Hysteresis for P0.12
22	PH13	read-write	Pad Hysteresis for P0.13
26	PH14	read-write	Pad Hysteresis for P0.14
30	PH15	read-write	Pad Hysteresis for P0.15
31, 27-29, 23-25, 19-21, 15-17, 11-13, 7-9, 3-5, 0-1		read	Reserved

7.2.9 PDISC

Port 0 Pin Function Decision Control Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PDIS15 [15]	PDIS14 [14]	PDIS13 [13]	PDIS12 [12]	PDIS11 [11]	PDIS10 [10]	PDIS9 [9]	PDIS8 [8]	PDIS7 [7]	PDIS6 [6]	PDIS5 [5]	PDIS4 [4]	PDIS3 [3]	PDIS2 [2]	PDIS1 [1]	PDIS0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	PDIS0	read-only	Pad Disable for Port 0 Pin 0 value1 = #0 (Pad P0.x is enabled.) value2 = #1 (Pad P0.x is disabled.)
1	PDIS1	read-only	Pad Disable for Port 0 Pin 1 value1 = #0 (Pad P0.x is enabled.) value2 = #1 (Pad P0.x is disabled.)
2	PDIS2	read-only	Pad Disable for Port 0 Pin 2 value1 = #0 (Pad P0.x is enabled.) value2 = #1 (Pad P0.x is disabled.)
3	PDIS3	read-only	Pad Disable for Port 0 Pin 3 value1 = #0 (Pad P0.x is enabled.) value2 = #1 (Pad P0.x is disabled.)
4	PDIS4	read-only	Pad Disable for Port 0 Pin 4 value1 = #0 (Pad P0.x is enabled.) value2 = #1 (Pad P0.x is disabled.)
5	PDIS5	read-only	Pad Disable for Port 0 Pin 5 value1 = #0 (Pad P0.x is enabled.) value2 = #1 (Pad P0.x is disabled.)
6	PDIS6	read-only	Pad Disable for Port 0 Pin 6 value1 = #0 (Pad P0.x is enabled.) value2 = #1 (Pad P0.x is disabled.)
7	PDIS7	read-only	Pad Disable for Port 0 Pin 7 value1 = #0 (Pad P0.x is enabled.) value2 = #1 (Pad P0.x is disabled.)
8	PDIS8	read-only	Pad Disable for Port 0 Pin 8 value1 = #0 (Pad P0.x is enabled.) value2 = #1 (Pad P0.x is disabled.)
9	PDIS9	read-only	Pad Disable for Port 0 Pin 9 value1 = #0 (Pad P0.x is enabled.) value2 = #1 (Pad P0.x is disabled.)
10	PDIS10	read-only	Pad Disable for Port 0 Pin 10 value1 = #0 (Pad P0.x is enabled.) value2 = #1 (Pad P0.x is disabled.)
11	PDIS11	read-only	Pad Disable for Port 0 Pin 11 value1 = #0 (Pad P0.x is enabled.) value2 = #1 (Pad P0.x is disabled.)
12	PDIS12	read-only	Pad Disable for Port 0 Pin 12 value1 = #0 (Pad P0.x is enabled.) value2 = #1 (Pad P0.x is disabled.)
13	PDIS13	read-only	Pad Disable for Port 0 Pin 13 value1 = #0 (Pad P0.x is enabled.) value2 = #1 (Pad P0.x is disabled.)
14	PDIS14	read-only	Pad Disable for Port 0 Pin 14 value1 = #0 (Pad P0.x is enabled.) value2 = #1 (Pad P0.x is disabled.)

Bits	Field	Access	Description
15	PDIS15	read-only	Pad Disable for Port 0 Pin 15 value1 = #0 (Pad P0.x is enabled.) value2 = #1 (Pad P0.x is disabled.)
16-31	0	read	Reserved

7.2.10 IN

Port 0 Input Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

P15 [15]	P14 [14]	P13 [13]	P12 [12]	P11 [11]	P10 [10]	P9 [9]	P8 [8]	P7 [7]	P6 [6]	P5 [5]	P4 [4]	P3 [3]	P2 [2]	P1 [1]	P0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	P0	read-only	Port 0 Input Bit 0 value1 = #0 (The input level of P0.x is 0.) value2 = #1 (The input level of P0.x is 1.)
1	P1	read-only	Port 0 Input Bit 1 value1 = #0 (The input level of P0.x is 0.) value2 = #1 (The input level of P0.x is 1.)
2	P2	read-only	Port 0 Input Bit 2 value1 = #0 (The input level of P0.x is 0.) value2 = #1 (The input level of P0.x is 1.)
3	P3	read-only	Port 0 Input Bit 3 value1 = #0 (The input level of P0.x is 0.) value2 = #1 (The input level of P0.x is 1.)
4	P4	read-only	Port 0 Input Bit 4 value1 = #0 (The input level of P0.x is 0.) value2 = #1 (The input level of P0.x is 1.)
5	P5	read-only	Port 0 Input Bit 5 value1 = #0 (The input level of P0.x is 0.) value2 = #1 (The input level of P0.x is 1.)
6	P6	read-only	Port 0 Input Bit 6 value1 = #0 (The input level of P0.x is 0.) value2 = #1 (The input level of P0.x is 1.)
7	P7	read-only	Port 0 Input Bit 7 value1 = #0 (The input level of P0.x is 0.) value2 = #1 (The input level of P0.x is 1.)
8	P8	read-only	Port 0 Input Bit 8 value1 = #0 (The input level of P0.x is 0.) value2 = #1 (The input level of P0.x is 1.)
9	P9	read-only	Port 0 Input Bit 9 value1 = #0 (The input level of P0.x is 0.) value2 = #1 (The input level of P0.x is 1.)
10	P10	read-only	Port 0 Input Bit 10 value1 = #0 (The input level of P0.x is 0.) value2 = #1 (The input level of P0.x is 1.)
11	P11	read-only	Port 0 Input Bit 11 value1 = #0 (The input level of P0.x is 0.) value2 = #1 (The input level of P0.x is 1.)
12	P12	read-only	Port 0 Input Bit 12 value1 = #0 (The input level of P0.x is 0.) value2 = #1 (The input level of P0.x is 1.)
13	P13	read-only	Port 0 Input Bit 13 value1 = #0 (The input level of P0.x is 0.) value2 = #1 (The input level of P0.x is 1.)
14	P14	read-only	Port 0 Input Bit 14 value1 = #0 (The input level of P0.x is 0.) value2 = #1 (The input level of P0.x is 1.)

Bits	Field	Access	Description
15	P15	read-only	Port 0 Input Bit 15 value1 = #0 (The input level of P0.x is 0.) value2 = #1 (The input level of P0.x is 1.)
16-31	0	read	Reserved

7.2.11 PPS

Port 0 Pin Power Save Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PPS15 [15]	PPS14 [14]	PPS13 [13]	PPS12 [12]	PPS11 [11]	PPS10 [10]	PPS9 [9]	PPS8 [8]	PPS7 [7]	PPS6 [6]	PPS5 [5]	PPS4 [4]	PPS3 [3]	PPS2 [2]	PPS1 [1]	PPS0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	PPS0	read-write	Port 0 Pin Power Save Bit 0 value1 = #0 (Pin Power Save of P0.x is disabled.) value2 = #1 (Pin Power Save of P0.x is enabled.)
1	PPS1	read-write	Port 0 Pin Power Save Bit 1 value1 = #0 (Pin Power Save of P0.x is disabled.) value2 = #1 (Pin Power Save of P0.x is enabled.)
2	PPS2	read-write	Port 0 Pin Power Save Bit 2 value1 = #0 (Pin Power Save of P0.x is disabled.) value2 = #1 (Pin Power Save of P0.x is enabled.)
3	PPS3	read-write	Port 0 Pin Power Save Bit 3 value1 = #0 (Pin Power Save of P0.x is disabled.) value2 = #1 (Pin Power Save of P0.x is enabled.)
4	PPS4	read-write	Port 0 Pin Power Save Bit 4 value1 = #0 (Pin Power Save of P0.x is disabled.) value2 = #1 (Pin Power Save of P0.x is enabled.)
5	PPS5	read-write	Port 0 Pin Power Save Bit 5 value1 = #0 (Pin Power Save of P0.x is disabled.) value2 = #1 (Pin Power Save of P0.x is enabled.)
6	PPS6	read-write	Port 0 Pin Power Save Bit 6 value1 = #0 (Pin Power Save of P0.x is disabled.) value2 = #1 (Pin Power Save of P0.x is enabled.)
7	PPS7	read-write	Port 0 Pin Power Save Bit 7 value1 = #0 (Pin Power Save of P0.x is disabled.) value2 = #1 (Pin Power Save of P0.x is enabled.)
8	PPS8	read-write	Port 0 Pin Power Save Bit 8 value1 = #0 (Pin Power Save of P0.x is disabled.) value2 = #1 (Pin Power Save of P0.x is enabled.)
9	PPS9	read-write	Port 0 Pin Power Save Bit 9 value1 = #0 (Pin Power Save of P0.x is disabled.) value2 = #1 (Pin Power Save of P0.x is enabled.)
10	PPS10	read-write	Port 0 Pin Power Save Bit 10 value1 = #0 (Pin Power Save of P0.x is disabled.) value2 = #1 (Pin Power Save of P0.x is enabled.)
11	PPS11	read-write	Port 0 Pin Power Save Bit 11 value1 = #0 (Pin Power Save of P0.x is disabled.) value2 = #1 (Pin Power Save of P0.x is enabled.)
12	PPS12	read-write	Port 0 Pin Power Save Bit 12 value1 = #0 (Pin Power Save of P0.x is disabled.) value2 = #1 (Pin Power Save of P0.x is enabled.)
13	PPS13	read-write	Port 0 Pin Power Save Bit 13 value1 = #0 (Pin Power Save of P0.x is disabled.) value2 = #1 (Pin Power Save of P0.x is enabled.)
14	PPS14	read-write	Port 0 Pin Power Save Bit 14 value1 = #0 (Pin Power Save of P0.x is disabled.) value2 = #1 (Pin Power Save of P0.x is enabled.)

Bits	Field	Access	Description
15	PPS15	read-write	Port 0 Pin Power Save Bit 15 value1 = #0 (Pin Power Save of P0.x is disabled.) value2 = #1 (Pin Power Save of P0.x is enabled.)
16-31	0	read	Reserved

7.2.12 HWSEL

Port 0 Pin Hardware Select Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

HW15 [31:30]		HW14 [29:28]		HW13 [27:26]		HW12 [25:24]		HW11 [23:22]		HW10 [21:20]		HW9 [19:18]		HW8 [17:16]	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

HW7 [15:14]		HW6 [13:12]		HW5 [11:10]		HW4 [9:8]		HW3 [7:6]		HW2 [5:4]		HW1 [3:2]		HW0 [1:0]	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
1:0	HW0	read-write	Port 0 Pin Hardware Select Bit 0 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
3:2	HW1	read-write	Port 0 Pin Hardware Select Bit 1 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
5:4	HW2	read-write	Port 0 Pin Hardware Select Bit 2 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
7:6	HW3	read-write	Port 0 Pin Hardware Select Bit 3 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
9:8	HW4	read-write	Port 0 Pin Hardware Select Bit 4 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
11:10	HW5	read-write	Port 0 Pin Hardware Select Bit 5 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
13:12	HW6	read-write	Port 0 Pin Hardware Select Bit 6 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
15:14	HW7	read-write	Port 0 Pin Hardware Select Bit 7 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)

Bits	Field	Access	Description
17:16	HW8	read-write	Port 0 Pin Hardware Select Bit 8 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
19:18	HW9	read-write	Port 0 Pin Hardware Select Bit 9 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
21:20	HW10	read-write	Port 0 Pin Hardware Select Bit 10 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
23:22	HW11	read-write	Port 0 Pin Hardware Select Bit 11 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
25:24	HW12	read-write	Port 0 Pin Hardware Select Bit 12 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
27:26	HW13	read-write	Port 0 Pin Hardware Select Bit 13 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
29:28	HW14	read-write	Port 0 Pin Hardware Select Bit 14 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
31:30	HW15	read-write	Port 0 Pin Hardware Select Bit 15 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)

8 General Purpose IO Ports (Ports) – PORTS Registers

Port 1

8.1 Register overview

Instance	Base address
PORT1	0x40040100
PORT2	0x40040200
PORT3	0x40040300
PORT4	0x40040400

Register name	Offset	Reset	Description
OUT	0x00	0x00000000	Port 1 Output Register
OMR	0x04	0x00000000	Port 1 Output Modification Register
IOCR0	0x10	0x00000000	Port 1 Input/Output Control Register 0
IOCR4	0x14	0x00000000	Port 1 Input/Output Control Register 4
IOCR8	0x18	0x00000000	Port 1 Input/Output Control Register 8
PHCR0	0x40	0x00000000	Port 1 Pad Hysteresis Control Register 0
PHCR1	0x44	0x00000000	Port 1 Pad Hysteresis Control Register 1
PDISC	0x60	0x00000000	Port 1 Pin Function Decision Control Register
IN	0x24	0x00000000	Port 1 Input Register
PPS	0x70	0x00000000	Port 1 Pin Power Save Register
HWSEL	0x74	0x00000000	Port 1 Pin Hardware Select Register

8.2 Register details

8.2.1 OUT

Port 1 Output Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0									P6 [6]	P5 [5]	P4 [4]	P3 [3]	P2 [2]	P1 [1]	P0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	P0	read-write	Port 1 Output Bit 0 value1 = #0 (The output level of P1.x is 0.) value2 = #1 (The output level of P1.x is 1.)
1	P1	read-write	Port 1 Output Bit 1 value1 = #0 (The output level of P1.x is 0.) value2 = #1 (The output level of P1.x is 1.)
2	P2	read-write	Port 1 Output Bit 2 value1 = #0 (The output level of P1.x is 0.) value2 = #1 (The output level of P1.x is 1.)
3	P3	read-write	Port 1 Output Bit 3 value1 = #0 (The output level of P1.x is 0.) value2 = #1 (The output level of P1.x is 1.)
4	P4	read-write	Port 1 Output Bit 4 value1 = #0 (The output level of P1.x is 0.) value2 = #1 (The output level of P1.x is 1.)
5	P5	read-write	Port 1 Output Bit 5 value1 = #0 (The output level of P1.x is 0.) value2 = #1 (The output level of P1.x is 1.)
6	P6	read-write	Port 1 Output Bit 6 value1 = #0 (The output level of P1.x is 0.) value2 = #1 (The output level of P1.x is 1.)
7-31	0	read	Reserved

8.2.2 OMR

Port 1 Output Modification Register

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0									PR6 [22]	PR5 [21]	PR4 [20]	PR3 [19]	PR2 [18]	PR1 [17]	PR0 [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0									PS6 [6]	PS5 [5]	PS4 [4]	PS3 [3]	PS2 [2]	PS1 [1]	PS0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	PS0	write-only	Port 1 Set Bit 0
1	PS1	write-only	Port 1 Set Bit 1
2	PS2	write-only	Port 1 Set Bit 2
3	PS3	write-only	Port 1 Set Bit 3
4	PS4	write-only	Port 1 Set Bit 4
5	PS5	write-only	Port 1 Set Bit 5
6	PS6	write-only	Port 1 Set Bit 6
16	PR0	write-only	Port 1 Reset Bit 0
17	PR1	write-only	Port 1 Reset Bit 1
18	PR2	write-only	Port 1 Reset Bit 2
19	PR3	write-only	Port 1 Reset Bit 3
20	PR4	write-only	Port 1 Reset Bit 4
21	PR5	write-only	Port 1 Reset Bit 5
22	PR6	write-only	Port 1 Reset Bit 6
23-31, 7-15	0	read	Reserved

8.2.3 IOCR0

Port 1 Input/Output Control Register 0

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PC3 [31:26]						0		PC2 [23:18]						0	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PC1 [15:10]						0		PC0 [7:2]						0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:2	PC0	read-write	Port Control for Port n Pin 0 to 3 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
15:10	PC1	read-write	Port Control for Port n Pin 0 to 3 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
23:18	PC2	read-write	Port Control for Port n Pin 0 to 3 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
31:26	PC3	read-write	Port Control for Port n Pin 0 to 3 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)
24-25, 16-17, 8-9, 0-1		read	Reserved

8.2.4 IOCR4

Port 1 Input/Output Control Register 4

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PC7 [31:26]						0		PC6 [23:18]						0	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PC5 [15:10]						0		PC4 [7:2]						0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:2	PC4	read-write	Port Control for Port n Pin 4 to 7 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
15:10	PC5	read-write	Port Control for Port n Pin 4 to 7 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
23:18	PC6	read-write	Port Control for Port n Pin 4 to 7 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)

Bits	Field	Access	Description
31:26	PC7	read-write	Port Control for Port n Pin 4 to 7 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)
24-25, 16-17, 8-9, 0-1		read	Reserved

8.2.5 IOCR8

Port 1 Input/Output Control Register 8

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0								PC8 [7:2]						0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:2	PC8	read-write	Port Control for Port n Pin 8 value1 = #000000 (Input - No internal pull device active) value2 = #000001 (Input - Internal pull-down device active) value3 = #000010 (Input - Internal pull-up device active) value4 = #000011 (Input - No internal pull device, Pn_OUTx = input value) value5 = #000100 (Input inverted - No internal pull device active) value6 = #000101 (Input inverted - Internal pull-down device active) value7 = #000110 (Input inverted - Internal pull-up device active) value8 = #000111 (Input inverted - No internal pull device, Pn_OUTx = input value) value9 = #100000 (Output Push-Pull - General-purpose output) value10 = #100001 (Output Push-Pull - Alternate output function 1) value11 = #100010 (Output Push-Pull - Alternate output function 2) value12 = #100011 (Output Push-Pull - Alternate output function 3) value13 = #100100 (Output Push-Pull - Alternate output function 4) value14 = #100101 (Output Push-Pull - Alternate output function 5) value15 = #100110 (Output Push-Pull - Alternate output function 6) value16 = #100111 (Output Push-Pull - Alternate output function 7) value17 = #101000 (Output Push-Pull - Alternate output function 8) value18 = #101001 (Output Push-Pull - Alternate output function 9) value19 = #110000 (Output Open Drain - General-purpose output) value20 = #110001 (Output Open Drain - Alternate output function 1) value21 = #110010 (Output Open Drain - Alternate output function 2) value22 = #110011 (Output Open Drain - Alternate output function 3) value23 = #110100 (Output Open Drain - Alternate output function 4) value24 = #110101 (Output Open Drain - Alternate output function 5) value25 = #110110 (Output Open Drain - Alternate output function 6) value26 = #110111 (Output Open Drain - Alternate output function 7) value27 = #111000 (Output Open Drain - Alternate output function 8) value28 = #111001 (Output Open Drain - Alternate output function 9)
8-31, 0-1	0	read	Reserved

8.2.6 PHCR0

Port 1 Pad Hysteresis Control Register 0

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0	PH7 [30]	0	PH6 [26]	0	PH5 [22]	0	PH4 [18]	0
31	30	29 28 27	26	25 24 23	22	21 20 19	18	17 16

Bit-field table (15 … 0)

0	PH3 [14]	0	PH2 [10]	0	PH1 [6]	0	PH0 [2]	0
15	14	13 12 11	10	9 8 7	6	5 4 3	2	1 0

Bit-fields

Bits	Field	Access	Description
2	PH0	read-write	Pad Hysteresis for P1.0
6	PH1	read-write	Pad Hysteresis for P1.1
10	PH2	read-write	Pad Hysteresis for P1.2
14	PH3	read-write	Pad Hysteresis for P1.3
18	PH4	read-write	Pad Hysteresis for P1.4
22	PH5	read-write	Pad Hysteresis for P1.5
26	PH6	read-write	Pad Hysteresis for P1.6
30	PH7	read-write	Pad Hysteresis for P1.7
31, 27-29, 23-25, 19-21, 15-17, 11-13, 7-9, 3-5, 0-1	0	read	Reserved

8.2.7 PHCR1

Port 1 Pad Hysteresis Control Register 1

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0													PH8 [2]	0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
2	PH8	read-write	Pad Hysteresis for P1.8
3-31, 0-1	0	read	Reserved

8.2.8 PDISC

Port 1 Pin Function Decision Control Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0									PDIS6 [6]	PDIS5 [5]	PDIS4 [4]	PDIS3 [3]	PDIS2 [2]	PDIS1 [1]	PDIS0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	PDIS0	read-only	Pad Disable for Port 1 Pin 0 value1 = #0 (Pad P1.x is enabled.) value2 = #1 (Pad P1.x is disabled.)
1	PDIS1	read-only	Pad Disable for Port 1 Pin 1 value1 = #0 (Pad P1.x is enabled.) value2 = #1 (Pad P1.x is disabled.)
2	PDIS2	read-only	Pad Disable for Port 1 Pin 2 value1 = #0 (Pad P1.x is enabled.) value2 = #1 (Pad P1.x is disabled.)
3	PDIS3	read-only	Pad Disable for Port 1 Pin 3 value1 = #0 (Pad P1.x is enabled.) value2 = #1 (Pad P1.x is disabled.)
4	PDIS4	read-only	Pad Disable for Port 1 Pin 4 value1 = #0 (Pad P1.x is enabled.) value2 = #1 (Pad P1.x is disabled.)
5	PDIS5	read-only	Pad Disable for Port 1 Pin 5 value1 = #0 (Pad P1.x is enabled.) value2 = #1 (Pad P1.x is disabled.)
6	PDIS6	read-only	Pad Disable for Port 1 Pin 6 value1 = #0 (Pad P1.x is enabled.) value2 = #1 (Pad P1.x is disabled.)
7-31	0	read	Reserved

8.2.9 IN

Port 1 Input Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0									P6 [6]	P5 [5]	P4 [4]	P3 [3]	P2 [2]	P1 [1]	P0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	P0	read-only	Port 1 Input Bit 0 value1 = #0 (The input level of P1.x is 0.) value2 = #1 (The input level of P1.x is 1.)
1	P1	read-only	Port 1 Input Bit 1 value1 = #0 (The input level of P1.x is 0.) value2 = #1 (The input level of P1.x is 1.)
2	P2	read-only	Port 1 Input Bit 2 value1 = #0 (The input level of P1.x is 0.) value2 = #1 (The input level of P1.x is 1.)
3	P3	read-only	Port 1 Input Bit 3 value1 = #0 (The input level of P1.x is 0.) value2 = #1 (The input level of P1.x is 1.)
4	P4	read-only	Port 1 Input Bit 4 value1 = #0 (The input level of P1.x is 0.) value2 = #1 (The input level of P1.x is 1.)
5	P5	read-only	Port 1 Input Bit 5 value1 = #0 (The input level of P1.x is 0.) value2 = #1 (The input level of P1.x is 1.)
6	P6	read-only	Port 1 Input Bit 6 value1 = #0 (The input level of P1.x is 0.) value2 = #1 (The input level of P1.x is 1.)
7-31	0	read	Reserved

8.2.10 PPS

Port 1 Pin Power Save Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0									PPS6 [6]	PPS5 [5]	PPS4 [4]	PPS3 [3]	PPS2 [2]	PPS1 [1]	PPS0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	PPS0	read-write	Port 1 Pin Power Save Bit 0 value1 = #0 (Pin Power Save of P1.x is disabled.) value2 = #1 (Pin Power Save of P1.x is enabled.)
1	PPS1	read-write	Port 1 Pin Power Save Bit 1 value1 = #0 (Pin Power Save of P1.x is disabled.) value2 = #1 (Pin Power Save of P1.x is enabled.)
2	PPS2	read-write	Port 1 Pin Power Save Bit 2 value1 = #0 (Pin Power Save of P1.x is disabled.) value2 = #1 (Pin Power Save of P1.x is enabled.)
3	PPS3	read-write	Port 1 Pin Power Save Bit 3 value1 = #0 (Pin Power Save of P1.x is disabled.) value2 = #1 (Pin Power Save of P1.x is enabled.)
4	PPS4	read-write	Port 1 Pin Power Save Bit 4 value1 = #0 (Pin Power Save of P1.x is disabled.) value2 = #1 (Pin Power Save of P1.x is enabled.)
5	PPS5	read-write	Port 1 Pin Power Save Bit 5 value1 = #0 (Pin Power Save of P1.x is disabled.) value2 = #1 (Pin Power Save of P1.x is enabled.)
6	PPS6	read-write	Port 1 Pin Power Save Bit 6 value1 = #0 (Pin Power Save of P1.x is disabled.) value2 = #1 (Pin Power Save of P1.x is enabled.)
7-31	0	read	Reserved

8.2.11 HWSEL

Port 1 Pin Hardware Select Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0		HW6 [13:12]		HW5 [11:10]		HW4 [9:8]		HW3 [7:6]		HW2 [5:4]		HW1 [3:2]		HW0 [1:0]	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
1:0	HW0	read-write	Port 1 Pin Hardware Select Bit 0 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
3:2	HW1	read-write	Port 1 Pin Hardware Select Bit 1 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
5:4	HW2	read-write	Port 1 Pin Hardware Select Bit 2 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
7:6	HW3	read-write	Port 1 Pin Hardware Select Bit 3 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
9:8	HW4	read-write	Port 1 Pin Hardware Select Bit 4 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
11:10	HW5	read-write	Port 1 Pin Hardware Select Bit 5 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
13:12	HW6	read-write	Port 1 Pin Hardware Select Bit 6 value1 = #00 (Software control only.) value2 = #01 (HW0 control path can override the software configuration.) value3 = #10 (HW1 control path can override the software configuration.)
14-31	0	read	Reserved

9 MATH Registers

MATH Unit

9.1 Register overview

Instance	Base address
MATH	0x40030000

Register name	Offset	Reset	Description
GLBCON	0x04	0x00000000	Global Control Register
ID	0x08	0x00F2C000	Module Identification Register
EVIER	0x0C	0x00000000	Event Interrupt Enable Register
EVFR	0x10	0x00000000	Event Flag Register
EVFSR	0x14	0x00000000	Event Flag Set Register
EVFCR	0x18	0x00000000	Event Flag Clear Register
DVD	0x20	0x00000000	Dividend Register
DVS	0x24	0x00000000	Divisor Register
QUOT	0x28	0x00000000	Quotient Register
RMD	0x2C	0x00000000	Remainder Register
DIVST	0x30	0x00000000	Divider Status Register
DIVCON	0x34	0x00000000	Divider Control Register
STATC	0x40	0x00000000	CORDIC Status and Data Control Register
CON	0x44	0x00000062	CORDIC Control Register
CORDX	0x48	0x00000000	CORDIC X Data Register
CORDY	0x4C	0x00000000	CORDIC Y Data Register
CORDZ	0x50	0x00000000	CORDIC Z Data Register
CORRX	0x54	0x00000000	CORDIC X Result Register
CORRY	0x58	0x00000000	CORDIC Y Result Register
CORRZ	0x5C	0x00000000	CORDIC Z Result Register

9.2 Register details

9.2.1 GLBCON

Global Control Register

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0														SUSCFG [17:16]	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0		CORDZRC [13:12]		0	CORDYRC [10:9]		0	CORDXRC [7:6]		DVSRC [5:3]			DVDRC [2:0]		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
2:0	DVDRC	read-write	Dividend Register Result Chaining value1 = #000 (No result chaining is selected) value2 = #001 (QUOT register is the selected source) value3 = #010 (RMD register is the selected source) value4 = #011 (CORRX is the selected source) value5 = #100 (CORRY is the selected source) value6 = #101 (CORRZ is the selected source)
5:3	DVSRC	read-write	Divisor Register Result Chaining value1 = #000 (No result chaining is selected) value2 = #001 (QUOT register is the selected source) value3 = #010 (RMD register is the selected source) value4 = #011 (CORRX is the selected source) value5 = #100 (CORRY is the selected source) value6 = #101 (CORRZ is the selected source)
7:6	CORDXRC	read-write	CORDX Register Result Chaining value1 = #00 (No result chaining is selected) value2 = #01 (QUOT register is the selected source) value3 = #10 (RMD register is the selected source)
10:9	CORDYRC	read-write	CORDY Register Result Chaining value1 = #00 (No result chaining is selected) value2 = #01 (QUOT register is the selected source) value3 = #10 (RMD register is the selected source)
13:12	CORDZRC	read-write	CORDZ Register Result Chaining value1 = #00 (No result chaining is selected) value2 = #01 (QUOT register is the selected source) value3 = #10 (RMD register is the selected source)
17:16	SUSCFG	read-write	Suspend Mode Configuration value1 = #00 (Suspend mode is never entered.) value2 = #01 (Hard suspend mode will be entered when CPU is halted.) value3 = #10 (Soft suspend mode will be entered when CPU is halted.)
18-31, 14-15, 11, 8		read	Reserved

9.2.2 ID

Module Identification Register

Reset	0x00F2C000
Width	32

Bit-field table (31 … 16)

MOD_NUMBER [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

MOD_TYPE [15:8]								MOD_REV [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	MOD_REV	read-only	Module Revision Number
15:8	MOD_TYPE	read-only	Module Type
31:16	MOD_NUMBER	read-only	Module Number Value

9.2.3 EVIER

Event Interrupt Enable Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0												CDERRIEN [3]	CDEOCIEN [2]	DIVERRIEN [1]	DIVEOCIEN [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	DIVEOCIEN	read-write	Divider End of Calculation Interrupt Enable value1 = #0 (Divider end of calculation interrupt generation is disabled.) value2 = #1 (Divider end of calculation interrupt generation is enabled.)
1	DIVERRIEN	read-write	Divider Error Interrupt Enable value1 = #0 (Divider error interrupt generation is disabled) value2 = #1 (Divider error interrupt generation is enabled)
2	CDEOCIEN	read-write	CORDIC End of Calculation Interrupt Enable value1 = #0 (CORDIC end of calculation interrupt generation is disabled.) value2 = #1 (CORDIC end of calculation interrupt generation is enabled.)
3	CDERRIEN	read-write	CORDIC Error Interrupt Enable value1 = #0 (CORDIC error interrupt generation is disabled) value2 = #1 (CORDIC error interrupt generation is enabled)
4-31	0	read	Reserved

9.2.4 EVFR

Event Flag Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0												CDERR [3]	CDEOC [2]	DIVERR [1]	DIVEOC [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	DIVEOC	read-only	Divider End of Calculation Event Flag value1 = #0 (Divider end of calculation event has not been detected.) value2 = #1 (Divider end of calculation event has been detected.)
1	DIVERR	read-only	Divider Error Event Flag value1 = #0 (Divider error event has not been detected) value2 = #1 (Divider error event has been detected)
2	CDEOC	read-only	CORDIC End of Calculation Event Flag value1 = #0 (CORDIC end of calculation event has not been detected.) value2 = #1 (CORDIC end of calculation event has been detected.)
3	CDERR	read-only	CORDIC Error Event Flag value1 = #0 (CORDIC error event has not been detected) value2 = #1 (CORDIC error event has been detected)
4-31	0	read	Reserved

9.2.5 EVFSR

Event Flag Set Register

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															

Bit-field table (15 … 0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												CDERRS [3]	CDEOCS [2]	DIVERRS [1]	DIVEOCS [0]

Bit-fields

Bits	Field	Access	Description
0	DIVEOCS	write-only	Divider End of Calculation Event Flag Set value1 = #0 (No effect.) value2 = #1 (Sets the Divider end of calculation event flag in EVFR register. Interrupt will be generated if enabled in EVIER register.)
1	DIVERRS	write-only	Divider Error Event Flag Set value1 = #0 (No effect.) value2 = #1 (Sets the Divider error event flag in EVFR register. Interrupt will be generated if enabled in EVIER register.)
2	CDEOCS	write-only	CORDIC Event Flag Set value1 = #0 (No effect.) value2 = #1 (Sets the CORDIC end of calculation event flag in EVFR register. Interrupt will be generated if enabled in EVIER register.)
3	CDERRS	write-only	CORDIC Error Event Flag Set value1 = #0 (No effect.) value2 = #1 (Sets the CORDIC error event flag in EVFR register. Interrupt will be generated if enabled in EVIER register.)
4-31	0	read	Reserved

9.2.6 EVFCR

Event Flag Clear Register

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0												CDERRC [3]	CDEOCC [2]	DIVERRC [1]	DIVEOCC [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	DIVEOCC	write-only	Divider End of Calculation Event Flag Clear value1 = #0 (No effect.) value2 = #1 (Clears the Divider end of calculation event flag in EVFR register.)
1	DIVERRC	write-only	Divider Error Event Flag Clear value1 = #0 (No effect.) value2 = #1 (Clears the Divider error event flag in EVFR register.)
2	CDEOCC	write-only	CORDIC End of Calculation Event Flag Clear value1 = #0 (No effect.) value2 = #1 (Clears the CORDIC end of calculation event flag in EVFR register.)
3	CDERRC	write-only	CORDIC Error Event Flag Clear value1 = #0 (No effect.) value2 = #1 (Clears the CORDIC error event flag in EVFR register.)
4-31	0	read	Reserved

9.2.7 DVD

Dividend Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

VAL [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

VAL [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:0	VAL	read-write	Dividend Value

9.2.8 DVS

Divisor Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

VAL [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

VAL [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:0	VAL	read-write	Divisor Value

9.2.9 QUOT

Quotient Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

VAL [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

VAL [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:0	VAL	read-only	Quotient Value

9.2.10 RMD

Remainder Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

VAL [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

VAL [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:0	VAL	read-only	Remainder Value

9.2.11 DIVST

Divider Status Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0															BSY [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	BSY	read-only	Busy Indication value1 = #0 (Divider is not running any division operation.) value2 = #1 (Divider is still running a division operation.)
1-31	0	read	Reserved

9.2.12 DIVCON

Divider Control Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0			DVSSRC [28:24]					0			DVDSLC [20:16]				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

QSDIR [15]	0		QSCNT [12:8]					0			DIVMODE [4:3]		USIGN [2]	STMODE [1]	ST [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	ST	read-write	Start Bit value1 = #0 (No effect) value2 = #1 (Start the division operation when STMODE=1#)
1	STMODE	read-write	Start Mode value1 = #0 (Calculation is automatically started with a write to DVS register) value2 = #1 (Calculation is started by setting the ST bit to 1)
2	USIGN	read-write	Unsigned Division Enable value1 = #0 (Signed division is selected) value2 = #1 (Unsigned division is selected)
4:3	DIVMODE	read-write	Division Mode value1 = #00 (32-bit divide by 32-bit) value2 = #01 (32-bit divide by 16-bit) value3 = #10 (16-bit divide by 16-bit)
12:8	QSCNT	read-write	Quotient Shift Count
15	QSDIR	read-write	Quotient Shift Direction value1 = #0 (Left shift) value2 = #1 (Right shift)
20:16	DVDSLC	read-write	Dividend Shift Left Count
28:24	DVSSRC	read-write	Divisor Shift Right Count
29-31, 21-23	13-14, 5-7	read	Reserved

9.2.13 STATC

CORDIC Status and Data Control Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0								KEEPZ [7]	KEEP Y [6]	KEEP X [5]	0				BSY [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	BSY	read-only	Busy Indication
5	KEEPX	read-write	Last X Result as Initial Data for New Calculation
6	KEEPY	read-write	Last Y Result as Initial Data for New Calculation
7	KEEPZ	read-write	Last Z Result as Initial Data for New Calculation
8-31, 1-4	0	read	Reserved

9.2.14 CON

CORDIC Control Register

Reset	0x00000062
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0								MPS [7:6]		X_USIGN [5]	ST_MODE [4]	ROTVEC [3]	MODE [2:1]		ST [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	ST	read-write	Start Calculation
2:1	MODE	read-write	Operating Mode value1 = #00 (Linear Mode) value2 = #01 (Circular Mode (default)) value4 = #11 (Hyperbolic Mode)
3	ROTVEC	read-write	Rotation Vectoring Selection value1 = #0 (Vectoring Mode (default)) value2 = #1 (Rotation Mode)
4	ST_MODE	read-write	Start Method value1 = #0 (Auto start of calculation after write access to X parameter data register CORDX(default).) value2 = #1 (Start calculation only after bit ST is set)
5	X_USIGN	read-write	Result Data Format for X in Circular Vectoring Mode value1 = #0 (Signed, twos complement) value2 = #1 (Unsigned (default))
7:6	MPS	read-write	X and Y Magnitude Prescaler value1 = #00 (Divide by 1) value2 = #01 (Divide by 2 (default)) value3 = #10 (Divide by 4) value4 = #11 (Reserved, retain the last MPS setting)
8-31	0	read	Reserved

9.2.15 CORDX

CORDIC X Data Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

DATA [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

DATA [15:8]								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:8	DATA	read-write	Initial X Parameter Data
0-7	0	read	Reserved

9.2.16 CORDY

CORDIC Y Data Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

DATA [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

DATA [15:8]								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:8	DATA	read-write	Initial Y Parameter Data
0-7	0	read	Reserved

9.2.17 CORDZ

CORDIC Z Data Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

DATA [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

DATA [15:8]								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:8	DATA	read-write	Initial Z Parameter Data
0-7	0	read	Reserved

9.2.18 CORRX

CORDIC X Result Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

RESULT [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

RESULT [15:8]								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:8	RESULT	read-only	X Calculation Result
0-7	0	read	Reserved

9.2.19 CORRY

CORDIC Y Result Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

RESULT [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

RESULT [15:8]								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:8	RESULT	read-only	Y Calculation Result
0-7	0	read	Reserved

9.2.20 CORRZ

CORDIC Z Result Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

RESULT [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

RESULT [15:8]								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:8	RESULT	read-only	Z Calculation Result
0-7	0	read	Reserved

10 Non volatile memory Registers

NVM Unit

10.1 Register overview

Instance	Base address
NVM	0x40050000

Register name	Offset	Reset	Description
NVMSTATUS	0x00	0x0002	NVM Status Register
NVMPROG	0x04	0x0000	NVM Programming Control Register
NVMCONF	0x08	0x9000	NVM Configuration Register

10.2 Register details

10.2.1 NVMSTATUS

NVM Status Register

Reset	0x0002
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0									WRPERR [6]	ECC2READ [5]	ECC1READ [4]	VERR [3:2]		SLEEP [1]	BUSY [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	BUSY	read-only	Busy value1 = #0 (The NVM is not busy. Memory reads from the cell array and register write accesses are possible.) value2 = #1 (The NVM is busy. Memory reads and register write accesses are not possible.)
1	SLEEP	read-only	Sleep Mode value1 = #0 (NVM not in sleep mode, and no sleep or wake up procedure in progress.) value2 = #1 (NVM in sleep mode, or busy due to a sleep or wake up procedure.)
3:2	VERR	read-only	Verify Error value1 = #00 (No fail bit.) value2 = #01 (One fail bit in one data block.) value3 = #10 (Two fail bits in two different data blocks.) value4 = #11 (Two or more fail bits in one data block, or three or more fail bits overall.)
4	ECC1READ	read-only	ECC1 Read value1 = #0 (No ECC single bit failure occurred.) value2 = #1 (At least one ECC single bit failure was detected and corrected.)
5	ECC2READ	read-only	ECC2 Read value1 = #0 (No ECC two bit failure during memory read operations.) value2 = #1 (At least one ECC two bit failure was detected.)
6	WRPERR	read-only	Write Protocol Error value1 = #0 (No write protocol failure occurred.) value2 = #1 (At least one write protocol failure was detected.)
7-15	0	read	Reserved

10.2.2 NVMPROG

NVM Programming Control Register

Reset	0x0000
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0		RSTECC [13]	RSTVERR [12]	0				ACTION [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	ACTION	read-write	ACTION: [VERIFY, ONE_SHOT, OPTYPE] value1 = 0x00 (Idle state, no action triggered. Writing 0x00 exits current mode.) value2 = 0x51 (Start one-shot write operation with automatic verify.) value3 = 0x91 (Start one-shot write operation without verify.) value4 = 0x61 (Start continuous write operation with automatic verify of every write.) value5 = 0xA1 (Start continuous write operation without verify.) value6 = 0x92 (Start one-shot page erase operation.) value7 = 0x94 (Start one-shot sector erase operation.) value8 = 0xA4 (Start continuous sector erase operation.) value9 = 0xA2 (Start continuous page erase operation.) value10 = 0xD0 (Start one-shot verify-only: Written data is compared to array content.) value11 = 0xE0 (Start continuous verify-only: Written data is compared to array content.)
12	RSTVERR	read-write	Reset Verify Error value1 = #0 (No action.) value2 = #1 (Reset of .VERR.)
13	RSTECC	read-write	Reset ECC value1 = #0 (No action.) value2 = #1 (Reset of .ECCxREAD and NVMSTATUS.WRPERR.)
14-15, 8-11	0	read	Reserved

10.2.3 NVMCONF

NVM Configuration Register

Reset	0x9000
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

NVM_ ON [15]	INT_O N [14]	0	SECPROT [11:4]	0	HRLEV [2:1]	0
15	14	13 12	11 10 9 8 7 6 5 4	3	2 1	0

Bit-fields

Bits	Field	Access	Description
2:1	HRLEV	read-write	Hardread Level value1 = #00 (Normal read) value2 = #01 (Hardread written) value3 = #10 (Hardread erased)
11:4	SECPROT	read-write	Sector Protection
14	INT_ON	read-write	Interrupt On value1 = #0 (No NVM ready interrupts are generated.) value2 = #1 (NVM ready interrupts are generated.)
15	NVM_ON	read-write	NVM On value1 = #0 (NVM is switched to or stays in sleep mode.) value2 = #1 (NVM is switched to or stays in normal mode.)
12-13, 3, 0	0	read	Reserved

11 Peripheral Access Unit Registers

PAU Unit

11.1 Register overview

Instance	Base address
PAU	0x40000000

Register name	Offset	Reset	Description
AVAIL0	0x40	0x07FF00FF	Peripheral Availability Register 0
AVAIL1	0x44	0x1E071FF7	Peripheral Availability Register 1
AVAIL2	0x48	0x30BFF00F	Peripheral Availability Register 2
PRIVDIS0	0x80	0x00000000	Peripheral Privilege Access Register 0
PRIVDIS1	0x84	0x00000000	Peripheral Privilege Access Register 1
PRIVDIS2	0x88	0x00000000	Peripheral Privilege Access Register 2
ROMSIZE	0x400	0x00000B00	ROM Size Register
FLSIZE	0x404	0x00033000	Flash Size Register
RAM0SIZE	0x410	0x00001000	RAM0 Size Register

11.2 Register details

11.2.1 AVAIL0

Peripheral Availability Register 0

Reset	0x07FF00FF
Width	32

Bit-field table (31 … 16)

0					AVAIL 26 [26]	AVAIL 25 [25]	AVAIL 24 [24]	AVAIL 23 [23]	AVAIL 22 [22]	AVAIL 21 [21]	AVAIL 20 [20]	0			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0								AVAIL 7 [7]	AVAIL 6 [6]	AVAIL 5 [5]	0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
5	AVAIL5	read-only	RAM Block 1 Availability Flag value1 = #0 (RAM block 1 is not available.) value2 = #1 (RAM block 1 is available.)
6	AVAIL6	read-only	RAM Block 2 Availability Flag value1 = #0 (RAM block 2 is not available.) value2 = #1 (RAM block 2 is available.)
7	AVAIL7	read-only	RAM Block 3 Availability Flag value1 = #0 (RAM block 3 is not available.) value2 = #1 (RAM block 3 is available.)
20	AVAIL20	read-only	MATH Global SFRs and Divider Availability Flag value1 = #0 (MATH Global SFRs and Divider are not available.) value2 = #1 (MATH Global SFRs and Divider are available.)
21	AVAIL21	read-only	MATH CORDIC Availability Flag value1 = #0 (MATH CORDIC is not available.) value2 = #1 (MATH CORDIC is available.)
22	AVAIL22	read-only	Port 0 Availability Flag value1 = #0 (Port 0 is not available.) value2 = #1 (Port 0 is available.)
23	AVAIL23	read-only	Port 1 Availability Flag value1 = #0 (Port 1 is not available.) value2 = #1 (Port 1 is available.)
24	AVAIL24	read-only	Port 2 Availability Flag value1 = #0 (Port 2 is not available.) value2 = #1 (Port 2 is available.)
25	AVAIL25	read-only	Port 3 Availability Flag value1 = #0 (Port 3 is not available.) value2 = #1 (Port 3 is available.)
26	AVAIL26	read-only	Port 4 Availability Flag value1 = #0 (Port 4 is not available.) value2 = #1 (Port 4 is available.)
27-31, 8-19, 0-4		read	Reserved

11.2.2 AVAIL1

Peripheral Availability Register 1

Reset 0x1E071FF7

Width 32

Bit-field table (31 … 16)

0			AVAIL 28 [28]	AVAIL 27 [27]	AVAIL 26 [26]	AVAIL 25 [25]	0							AVAIL 17 [17]	AVAIL 16 [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0			AVAIL 12 [12]	AVAIL 11 [11]	AVAIL 10 [10]	AVAIL 9 [9]	AVAIL 8 [8]	AVAIL 7 [7]	AVAIL 6 [6]	AVAIL 5 [5]	AVAIL 4 [4]	0		AVAIL 1 [1]	AVAIL 0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	AVAIL0	read-only	USIC0 Channel 0 Availability Flag value1 = #0 (USIC0 Channel 0 is not available.) value2 = #1 (USIC0 Channel 0 is available.)
1	AVAIL1	read-only	USIC0 Channel 1 Availability Flag value1 = #0 (USIC0 Channel 1 is not available.) value2 = #1 (USIC0 Channel 1 is available.)
4	AVAIL4	read-only	PRNG Availability Flag value1 = #0 (PRNG is not available.) value2 = #1 (PRNG is available.)
5	AVAIL5	read-only	VADC0 Basic SFRs Availability Flag value1 = #0 (VADC0 Basic SFRs are not available.) value2 = #1 (VADC0 Basic SFRs are available.)
6	AVAIL6	read-only	VADC0 Group 0 SFRs Availability Flag value1 = #0 (VADC0 Group 0 SFRs are not available.) value2 = #1 (VADC0 Group 0 SFRs are available.)
7	AVAIL7	read-only	VADC0 Group 1 SFRs Availability Flag value1 = #0 (VADC0 Group 1 SFRs are not available.) value2 = #1 (VADC0 Group 1 SFRs are available.)
8	AVAIL8	read-only	SHS0 Availability Flag value1 = #0 (SHS0 is not available.) value2 = #1 (SHS0 is available.)
9	AVAIL9	read-only	CCU40 kernel SFRs and CC40 Availability Flag value1 = #0 (CCU40 kernel SFRs and CC40 is not available.) value2 = #1 (CCU40 kernel SFRs and CC40 is available.)
10	AVAIL10	read-only	CCU40 CC41 Availability Flag value1 = #0 (CCU40 CC41 is not available.) value2 = #1 (CCU40 CC41 is available.)
11	AVAIL11	read-only	CCU40 CC42 Availability Flag value1 = #0 (CCU40 CC42 is not available.) value2 = #1 (CCU40 CC42 is available.)
12	AVAIL12	read-only	CCU40 CC43 Availability Flag value1 = #0 (CCU40 CC43 is not available.) value2 = #1 (CCU40 CC43 is available.)
16	AVAIL16	read-only	USIC1 Channel 0 Availability Flag value1 = #0 (USIC1 Channel 0 is not available.) value2 = #1 (USIC1 Channel 0 is available.)
17	AVAIL17	read-only	USIC1 Channel 1 Availability Flag value1 = #0 (USIC1 Channel 1 is not available.) value2 = #1 (USIC1 Channel 1 is available.)
25	AVAIL25	read-only	CCU41 kernel SFRs and CC40 Availability Flag value1 = #0 (CCU41 kernel SFRs and CC40 is not available.) value2 = #1 (CCU41 kernel SFRs and CC40 is available.)
26	AVAIL26	read-only	CCU41 CC41 Availability Flag value1 = #0 (CCU41 CC41 is not available.) value2 = #1 (CCU41 CC41 is available.)

Bits	Field	Access	Description
27	AVAIL27	read-only	CCU41 CC42 Availability Flag value1 = #0 (CCU41 CC42 is not available.) value2 = #1 (CCU41 CC42 is available.)
28	AVAIL28	read-only	CCU41 CC43 Availability Flag value1 = #0 (CCU41 CC43 is not available.) value2 = #1 (CCU41 CC43 is available.)
29-31, 18-24, 13-15, 2-3		read	Reserved

11.2.3 AVAIL2

Peripheral Availability Register 2

Reset 0x30BFF00F

Width 32

Bit-field table (31 … 16)

0			AVAIL 28 [28]	0				AVAIL 23 [23]	0	AVAIL 21 [21]	AVAIL 20 [20]	AVAIL 19 [19]	AVAIL 18 [18]	AVAIL 17 [17]	AVAIL 16 [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

AVAIL 15 [15]	0		AVAIL 12 [12]	0								AVAIL 3 [3]	AVAIL 2 [2]	AVAIL 1 [1]	AVAIL 0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	AVAIL0	read-only	CCU80 kernel SFRs and CC80 Availability Flag value1 = #0 (CC80 and CCU80 kernel SFRs are not available.) value2 = #1 (CC80 and CCU80 kernel SFRs are available.)
1	AVAIL1	read-only	CCU80 CC81 Availability Flag value1 = #0 (CCU80 CC81 is not available.) value2 = #1 (CCU80 CC81 is available.)
2	AVAIL2	read-only	CCU80 CC82 Availability Flag value1 = #0 (CCU80 CC82 is not available.) value2 = #1 (CCU80 CC82 is available.)
3	AVAIL3	read-only	CCU80 CC83 Availability Flag value1 = #0 (CCU80 CC83 is not available.) value2 = #1 (CCU80 CC83 is available.)
12	AVAIL12	read-only	POSIF0 Availability Flag value1 = #0 (POSIF0 is not available.) value2 = #1 (POSIF0 is available.)
15	AVAIL15	read-only	BCCU0 Availability Flag value1 = #0 (BCCU0 is not available.) value2 = #1 (BCCU0 is available.)
16	AVAIL16	read-only	CCU81 kernel SFRs and CC80 Availability Flag value1 = #0 (CCU81 kernel SFRs and CC80 are not available.) value2 = #1 (CCU81 kernel SFRs and CC80 are available.)
17	AVAIL17	read-only	CCU81 CC81 Availability Flag value1 = #0 (CCU81 CC81 is not available.) value2 = #1 (CCU81 CC81 is available.)
18	AVAIL18	read-only	CCU81 CC82 Availability Flag value1 = #0 (CCU81 CC82 is not available.) value2 = #1 (CCU81 CC82 is available.)
19	AVAIL19	read-only	CCU81 CC83 Availability Flag value1 = #0 (CCU81 CC83 is not available.) value2 = #1 (CCU81 CC83 is available.)
20	AVAIL20	read-only	MultiCAN Node 0 and Global SFRs Availability Flag value1 = #0 (MultiCAN node 0 and Global SFRs are not available.) value2 = #1 (MultiCAN node 0 and Global SFRs are available.)
21	AVAIL21	read-only	MultiCAN Node 1 Availability Flag value1 = #0 (MultiCAN node 1 is not available.) value2 = #1 (MultiCAN node 1 is available.)
23	AVAIL23	read-only	MultiCAN Message Object SFRs Availability Flag value1 = #0 (MultiCAN message object SFRs are not available.) value2 = #1 (MultiCAN message object SFRs are available.)
28	AVAIL28	read-only	POSIF1 Availability Flag value1 = #0 (POSIF1 is not available.) value2 = #1 (POSIF1 is available.)
29-31, 24-27, 22, 13-14, 4-11		read	Reserved

11.2.4 PRIVDIS0

Peripheral Privilege Access Register 0

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0					PDIS26 [26]	PDIS25 [25]	PDIS24 [24]	PDIS23 [23]	PDIS22 [22]	PDIS21 [21]	PDIS20 [20]	PDIS19 [19]	0		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0								PDIS7 [7]	PDIS6 [6]	PDIS5 [5]	0		PDIS2 [2]	0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
2	PDIS2	read-write	Flash SFRs Privilege Disable Flag value1 = #0 (Flash SFRs are accessible.) value2 = #1 (Flash SFRs are not accessible.)
5	PDIS5	read-write	RAM Block 1 Privilege Disable Flag value1 = #0 (RAM Block 1 is accessible.) value2 = #1 (RAM Block 1 is not accessible.)
6	PDIS6	read-write	RAM Block 2 Privilege Disable Flag value1 = #0 (RAM Block 2 is accessible.) value2 = #1 (RAM Block 2 is not accessible.)
7	PDIS7	read-write	RAM Block 3 Privilege Disable Flag value1 = #0 (RAM Block 3 is accessible.) value2 = #1 (RAM Block 3 is not accessible.)
19	PDIS19	read-write	WDT Privilege Disable Flag value1 = #0 (WDT is accessible.) value2 = #1 (WDT is not accessible.)
20	PDIS20	read-write	MATH Global SFRs and Divider Privilege Disable Flag value1 = #0 (MATH Global SFRs and Divider are accessible.) value2 = #1 (MATH Global SFRs and Divider are not accessible.)
21	PDIS21	read-write	MATH CORDIC Privilege Disable Flag value1 = #0 (MATH CORDIC is accessible.) value2 = #1 (MATH CORDIC is not accessible.)
22	PDIS22	read-write	Port 0 Privilege Disable Flag value1 = #0 (Port 0 is accessible.) value2 = #1 (Port 0 is not accessible.)
23	PDIS23	read-write	Port 1 Privilege Disable Flag value1 = #0 (Port 1 is accessible.) value2 = #1 (Port 1 is not accessible.)
24	PDIS24	read-write	Port 2 Privilege Disable Flag value1 = #0 (Port 2 is accessible.) value2 = #1 (Port 2 is not accessible.)
25	PDIS25	read-write	Port 3 Privilege Disable Flag value1 = #0 (Port 3 is accessible.) value2 = #1 (Port 3 is not accessible.)
26	PDIS26	read-write	Port 4 Privilege Disable Flag value1 = #0 (Port 4 is accessible.) value2 = #1 (Port 4 is not accessible.)
27-31, 8-18, 0-4, 0-1	0	read	Reserved

11.2.5 PRIVDIS1

Peripheral Privilege Access Register 1

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0			PDIS28 [28]	PDIS27 [27]	PDIS26 [26]	PDIS25 [25]	0							PDIS17 [17]	PDIS16 [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0			PDIS12 [12]	PDIS11 [11]	PDIS10 [10]	PDIS9 [9]	PDIS8 [8]	PDIS7 [7]	PDIS6 [6]	PDIS5 [5]	0			PDIS1 [1]	PDIS0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	PDIS0	read-write	USIC0 Channel 0 Privilege Disable Flag value1 = #0 (USIC0 Channel 0 is accessible.) value2 = #1 (USIC0 Channel 0 is not accessible.)
1	PDIS1	read-write	USIC0 Channel 1 Privilege Disable Flag value1 = #0 (USIC0 Channel 1 is accessible.) value2 = #1 (USIC0 Channel 1 is not accessible.)
5	PDIS5	read-write	VADC0 Basic SFRs Privilege Disable Flag value1 = #0 (VADC0 Basic SFRs are accessible.) value2 = #1 (VADC0 Basic SFRs are not accessible.)
6	PDIS6	read-write	VADC0 Group 0 SFRs Privilege Disable Flag value1 = #0 (VADC0 Group 0 SFRs are accessible.) value2 = #1 (VADC0 Group 0 SFRs are not accessible.)
7	PDIS7	read-write	VADC0 Group 1 SFRs Privilege Disable Flag value1 = #0 (VADC0 Group 1 SFRs are accessible.) value2 = #1 (VADC0 Group 1 SFRs are not accessible.)
8	PDIS8	read-write	SHS0 Privilege Disable Flag value1 = #0 (SHS0 is accessible.) value2 = #1 (SHS0 is not accessible.)
9	PDIS9	read-write	CC40 and CCU40 Kernel SFRs Privilege Disable Flag value1 = #0 (CC40 and CCU40 Kernel SFRs are accessible.) value2 = #1 (CC40 and CCU40 Kernel SFRs are not accessible.)
10	PDIS10	read-write	CCU40 CC41 Privilege Disable Flag value1 = #0 (CCU40 CC41 is accessible.) value2 = #1 (CCU40 CC41 is not accessible.)
11	PDIS11	read-write	CCU40 CC42 Privilege Disable Flag value1 = #0 (CCU40 CC42 is accessible.) value2 = #1 (CCU40 CC42 is not accessible.)
12	PDIS12	read-write	CCU40 CC43 Privilege Disable Flag value1 = #0 (CCU40 CC43 is accessible.) value2 = #1 (CCU40 CC43 is not accessible.)
16	PDIS16	read-write	USIC1 Channel 0 Privilege Disable Flag value1 = #0 (USIC1 Channel 0 is accessible.) value2 = #1 (USIC1 Channel 0 is not accessible.)
17	PDIS17	read-write	USIC1 Channel 1 Privilege Disable Flag value1 = #0 (USIC1 Channel 1 is accessible.) value2 = #1 (USIC1 Channel 1 is not accessible.)
25	PDIS25	read-write	CCU41 Kernel SFRs and CC40 Privilege Disable Flag value1 = #0 (CCU41 Kernel SFRs and CC40 are accessible.) value2 = #1 (CCU41 Kernel SFRs and CC40 are not accessible.)
26	PDIS26	read-write	CCU41 CC41 Privilege Disable Flag value1 = #0 (CCU41 CC41 is accessible.) value2 = #1 (CCU41 CC41 is not accessible.)
27	PDIS27	read-write	CCU41 CC42 Privilege Disable Flag value1 = #0 (CCU41 CC42 is accessible.) value2 = #1 (CCU41 CC42 is not accessible.)

Bits	Field	Access	Description
28	PDIS28	read-write	CCU41 CC43 Privilege Disable Flag value1 = #0 (CCU41 CC43 is accessible.) value2 = #1 (CCU41 CC43 is not accessible.)
29-31, 18-24, 13-15, 2-4		read	Reserved

11.2.6 PRIVDIS2

Peripheral Privilege Access Register 2

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0			PDIS28 [28]	0				PDIS23 [23]	0	PDIS21 [21]	PDIS20 [20]	PDIS19 [19]	PDIS18 [18]	PDIS17 [17]	PDIS16 [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PDIS15 [15]	0		PDIS12 [12]	0								PDIS3 [3]	PDIS2 [2]	PDIS1 [1]	PDIS0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	PDIS0	read-write	CC80 and CCU80 Kernel SFRs Privilege Disable Flag value1 = #0 (CC80 and CCU80 Kernel SFRs are accessible.) value2 = #1 (CC80 and CCU80 Kernel SFRs are not accessible.)
1	PDIS1	read-write	CCU80 CC81 Privilege Disable Flag value1 = #0 (CCU80 CC81 is accessible.) value2 = #1 (CCU80 CC81 is not accessible.)
2	PDIS2	read-write	CCU80 CC82 Privilege Disable Flag value1 = #0 (CCU80 CC82 is accessible.) value2 = #1 (CCU80 CC82 is not accessible.)
3	PDIS3	read-write	CCU80 CC83 Privilege Disable Flag value1 = #0 (CCU80 CC83 is accessible.) value2 = #1 (CCU80 CC83 is not accessible.)
12	PDIS12	read-write	POSIF0 Privilege Disable Flag value1 = #0 (POSIF0 is accessible.) value2 = #1 (POSIF0 is not accessible.)
15	PDIS15	read-write	BCCU0 Privilege Disable Flag value1 = #0 (BCCU0 is accessible.) value2 = #1 (BCCU0 is not accessible.)
16	PDIS16	read-write	CCU81 Kernel SFRs and CC80 Privilege Disable Flag value1 = #0 (CCU81 Kernel SFRs and CC80 are accessible.) value2 = #1 (CCU81 Kernel SFRs and CC80 are not accessible.)
17	PDIS17	read-write	CCU81 CC81 Privilege Disable Flag value1 = #0 (CCU81 CC81 is accessible.) value2 = #1 (CCU81 CC81 is not accessible.)
18	PDIS18	read-write	CCU81 CC82 Privilege Disable Flag value1 = #0 (CCU81 CC82 is accessible.) value2 = #1 (CCU81 CC82 is not accessible.)
19	PDIS19	read-write	CCU81 CC83 Privilege Disable Flag value1 = #0 (CCU81 CC83 is accessible.) value2 = #1 (CCU81 CC83 is not accessible.)
20	PDIS20	read-write	MultiCAN Node 0 and Global SFRs Privilege Disable Flag value1 = #0 (MultiCAN node 0 and global SFRs are accessible.) value2 = #1 (MultiCAN node 0 and global SFRs are not accessible.)
21	PDIS21	read-write	MultiCAN Node 1 Privilege Disable Flag value1 = #0 (MultiCAN node 1 is accessible.) value2 = #1 (MultiCAN node 1 is not accessible.)
23	PDIS23	read-write	MultiCAN Message Object SFRs Privilege Disable Flag value1 = #0 (MultiCAN message object SFRs are accessible.) value2 = #1 (MultiCAN message object SFRs are not accessible.)
28	PDIS28	read-write	POSIF1 Privilege Disable Flag value1 = #0 (POSIF1 is accessible.) value2 = #1 (POSIF1 is not accessible.)
29-31, 24-27, 22, 13-14, 4-11		read	Reserved

11.2.7 ROMSIZE

ROM Size Register

Reset	0x00000B00
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0							ADDR [13:8]								0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
13:8	ADDR	read-only	ROM Size
14-31, 0-7	0	read	Reserved

11.2.8 FLSIZE

Flash Size Register

Reset	0x00033000
Width	32

Bit-field table (31 … 16)

0														ADDR [17:16]	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

ADDR [15:12]				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
17:12	ADDR	read-only	Flash Size
18-31, 0-11	0	read	Reserved

11.2.9 RAM0SIZE

RAM0 Size Register

Reset	0x00001000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0			ADDR [12:8]					0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
12:8	ADDR	read-only	RAM0 Size
13-31, 0-7	0	read	Reserved

12 Position Interface Unit Registers

Position Interface 0

12.1 Register overview

Instance	Base address
POSIF0	0x50010000
POSIF1	0x50014000

Register name	Offset	Reset	Description
PCONF	0x00	0x00000000	CORDIC Coprocessor configuration
PSUS	0x04	0x00000000	CORDIC Coprocessor Suspend Config
PRUNS	0x08	0x00000000	CORDIC Coprocessor Run Bit Set
PRUNC	0x0C	0x00000000	CORDIC Coprocessor Run Bit Clear
PRUN	0x10	0x00000000	CORDIC Coprocessor Run Bit Status
MIDR	0x20	0x00A8C000	Module Identification register
HALP	0x30	0x00000000	Hall Sensor Patterns
HALPS	0x34	0x00000000	Hall Sensor Shadow Patterns
MCM	0x40	0x00000000	Multi-Channel Pattern
MCSM	0x44	0x00000000	Multi-Channel Shadow Pattern
MCMS	0x48	0x00000000	Multi-Channel Pattern Control set
MCMC	0x4C	0x00000000	Multi-Channel Pattern Control clear
MCMF	0x50	0x00000000	Multi-Channel Pattern Control flag
QDC	0x60	0x00000000	Quadrature Decoder Control
PFLG	0x70	0x00000000	CORDIC Coprocessor Interrupt Flags
PFLGE	0x74	0x00000000	CORDIC Coprocessor Interrupt Enable
SPFLG	0x78	0x00000000	CORDIC Coprocessor Interrupt Set
RPFLG	0x7C	0x00000000	CORDIC Coprocessor Interrupt Clear
PDBG	0x100	0x00000000	CORDIC Coprocessor Debug register

12.2 Register details

12.2.1 PCONF

CORDIC Coprocessor configuration

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0	LPC [30:28]			EWIL [27]	EWIE [26]	EWIS [25:24]		MSYNS [23:22]		MSES [21]	MSETS [20:18]			SPES [17]	DSEL [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0		INSEL2 [13:12]		INSEL1 [11:10]		INSEL0 [9:8]		0		MCUE [5]	HIDG [4]	0	QDCM [2]	FSEL [1:0]	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
1:0	FSEL	read-write	Function Selector value1 = #00 (Hall Sensor Mode enabled) value2 = #01 (Quadrature Decoder Mode enabled) value3 = #10 (stand-alone Multi-Channel Mode enabled) value4 = #11 (Quadrature Decoder and stand-alone Multi-Channel Mode enabled)
2	QDCM	read-write	Position Decoder Mode selection value1 = #0 (Position encoder is in Quadrature Mode) value2 = #1 (Position encoder is in Direction Count Mode.)
4	HIDG	read-write	Idle generation enable
5	MCUE	read-write	Multi-Channel Pattern SW update enable value1 = #0 (Multi-Channel pattern update is controlled via HW) value2 = #1 (Multi-Channel pattern update is controlled via SW)
9:8	INSEL0	read-write	PhaseA/Hal input 1 selector value1 = #00 (POSIFx.IN0A) value2 = #01 (POSIFx.IN0B) value3 = #10 (POSIFx.IN0C) value4 = #11 (POSIFx.IN0D)
11:10	INSEL1	read-write	PhaseB/Hall input 2 selector value1 = #00 (POSIFx.IN1A) value2 = #01 (POSIFx.IN1B) value3 = #10 (POSIFx.IN1C) value4 = #11 (POSIFx.IN1D)
13:12	INSEL2	read-write	Index/Hall input 3 selector value1 = #00 (POSIFx.IN2A) value2 = #01 (POSIFx.IN2B) value3 = #10 (POSIFx.IN2C) value4 = #11 (POSIFx.IN2D)
16	DSEL	read-write	Delay Pin selector value1 = #0 (POSIFx.HSDA) value2 = #1 (POSIFx.HSDB)
17	SPES	read-write	Edge selector for the sampling trigger value1 = #0 (Rising edge) value2 = #1 (Falling edge)
20:18	MSETS	read-write	Pattern update signal select value1 = #000 (POSIFx.MSETA) value2 = #001 (POSIFx.MSETB) value3 = #010 (POSIFx.MSETC) value4 = #011 (POSIFx.MSETD) value5 = #100 (POSIFx.MSETE) value6 = #101 (POSIFx.MSETF) value7 = #110 (POSIFx.MSETG) value8 = #111 (POSIFx.MSETH)

Bits	Field	Access	Description
21	MSES	read-write	Multi-Channel pattern update trigger edge value1 = #0 (The signal used to enable a pattern update is active on the rising edge) value2 = #1 (The signal used to enable a pattern update is active on the falling edge)
23:22	MSYNS	read-write	PWM synchronization signal selector value1 = #00 (POSIFx.MSYNCA) value2 = #01 (POSIFx.MSYNCB) value3 = #10 (POSIFx.MSYNCC) value4 = #11 (POSIFx.MSYNCD)
25:24	EWIS	read-write	Wrong Hall Event selection value1 = #00 (POSIFx.EWHEA) value2 = #01 (POSIFx.EWHEB) value3 = #10 (POSIFx.EWHEC) value4 = #11 (POSIFx.EWHED)
26	EWIE	read-write	External Wrong Hall Event enable value1 = #0 (External wrong hall event emulation signal, POSIFx.EWHE[D...A], is disabled) value2 = #1 (External wrong hall event emulation signal, POSIFx.EWHE[D...A], is enabled.)
27	EWIL	read-write	External Wrong Hall Event active level value1 = #0 (POSIFx.EWHE[D...A] signal is active HIGH) value2 = #1 (POSIFx.EWHE[D...A] signal is active LOW)
30:28	LPC	read-write	Low Pass Filters Configuration value1 = #000 (Low pass filter disabled) value2 = #001 (Low pass of 1 clock cycle) value3 = #010 (Low pass of 2 clock cycles) value4 = #011 (Low pass of 4 clock cycles) value5 = #100 (Low pass of 8 clock cycles) value6 = #101 (Low pass of 16 clock cycles) value7 = #110 (Low pass of 32 clock cycles) value8 = #111 (Low pass of 64 clock cycles)
31, 14-15, 6-7, 3		read	Reserved

12.2.2 PSUS

CORDIC Coprocessor Suspend Config

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0												MSUS [3:2]		QSUS [1:0]	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
1:0	QSUS	read-write	Quadrature Mode Suspend Config value1 = #00 (Suspend request ignored) value2 = #01 (Stop immediately) value3 = #10 (Suspend in the next index occurrence) value4 = #11 (Suspend in the next phase (PhaseA or PhaseB) occurrence)
3:2	MSUS	read-write	Multi-Channel Mode Suspend Config value1 = #00 (Suspend request ignored) value2 = #01 (Stop immediately. Multi-Channel pattern is not set to the reset value.) value3 = #10 (Stop immediately. Multi-Channel pattern is set to the reset value.) value4 = #11 (Suspend with the synchronization of the PWM signal. Multi-Channel pattern is set to the reset value at the same time of the synchronization.)
4-31	0	read	Reserved

12.2.3 PRUNS

CORDIC Coprocessor Run Bit Set

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0															SRB [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	SRB	write-only	Set Run bit
1-31	0	read	Reserved

12.2.4 PRUNC

CORDIC Coprocessor Run Bit Clear

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0														CSM [1]	CRB [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	CRB	write-only	Clear Run bit
1	CSM	write-only	Clear Current internal status
2-31	0	read	Reserved

12.2.5 PRUN

CORDIC Coprocessor Run Bit Status

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0															RB [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	RB	read-only	Run Bit value1 = #0 (IDLE) value2 = #1 (Running)
1-31	0	read	Reserved

12.2.6 MIDR

Module Identification register

Reset	0x00A8C000
Width	32

Bit-field table (31 … 16)

MODN [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

MODT [15:8]								MODR [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	MODR	read-only	Module Revision
15:8	MODT	read-only	Module Type
31:16	MODN	read-only	Module Number

12.2.7 HALP

Hall Sensor Patterns

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0										HEP [5:3]			HCP [2:0]		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
2:0	HCP	read-only	Hall Current Pattern
5:3	HEP	read-only	Hall Expected Pattern
6-31	0	read	Reserved

12.2.8 HALPS

Hall Sensor Shadow Patterns

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0										HEPS [5:3]			HCPS [2:0]		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
2:0	HCPS	read-write	Shadow Hall Current Pattern
5:3	HEPS	read-write	Shadow Hall expected Pattern
6-31	0	read	Reserved

12.2.9 MCM

Multi-Channel Pattern

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

MCMP [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
15:0	MCMP	read-only	Multi-Channel Pattern
16-31	0	read	Reserved

12.2.10 MCSM

Multi-Channel Shadow Pattern

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

MCMPS [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
15:0	MCMPS	read-write	Shadow Multi-Channel Pattern
16-31	0	read	Reserved

12.2.11 MCMS

Multi-Channel Pattern Control set

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0													STMR [2]	STHR [1]	MNPS [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	MNPS	write-only	Multi-Channel Pattern Update Enable Set
1	STHR	write-only	Hall Pattern Shadow Transfer Request
2	STMR	write-only	Multi-Channel Shadow Transfer Request
3-31	0	read	Reserved

12.2.12 MCMC

Multi-Channel Pattern Control clear

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0														MPC [1]	MNPC [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	MNPC	write-only	Multi-Channel Pattern Update Enable Clear
1	MPC	write-only	Multi-Channel Pattern clear
2-31	0	read	Reserved

12.2.13 MCMF

Multi-Channel Pattern Control flag

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0															MSS [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	MSS	read-only	Multi-Channel Pattern update status value1 = #0 (Update of the Multi-Channel pattern is set) value2 = #1 (Update of the Multi-Channel pattern is not set)
1-31	0	read	Reserved

12.2.14 QDC

Quadrature Decoder Control

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0							DVAL [8]	0		ICM [5:4]		0	PHS [2]	PBLS [1]	PALS [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	PALS	read-write	Phase A Level selector value1 = #0 (Phase A is active HIGH) value2 = #1 (Phase A is active LOW)
1	PBLS	read-write	Phase B Level selector value1 = #0 (Phase B is active HIGH) value2 = #1 (Phase B is active LOW)
2	PHS	read-write	Phase signals swap value1 = #0 (Phase A is the leading signal for clockwise rotation) value2 = #1 (Phase B is the leading signal for clockwise rotation)
5:4	ICM	read-write	Index Marker generations control value1 = #00 (No index marker generation on POSIFx.OUT3) value2 = #01 (Only first index occurrence generated on POSIFx.OUT3) value3 = #10 (All index occurrences generated on POSIFx.OUT3)
8	DVAL	read-only	Current rotation direction value1 = #0 (Counterclockwise rotation) value2 = #1 (Clockwise rotation)
9-31, 6-7, 3	0	read	Reserved

12.2.15 PFLG

CORDIC Coprocessor Interrupt Flags

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0			PCLKS [12]	DIRS [11]	CNTS [10]	ERRS [9]	INDXS [8]	0			MSTS [4]	0	HIES [2]	WHES [1]	CHES [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	CHES	read-only	Correct Hall Event Status value1 = #0 (Correct Hall Event not detected) value2 = #1 (Correct Hall Event detected)
1	WHES	read-only	Wrong Hall Event Status value1 = #0 (Wrong Hall Event not detected) value2 = #1 (Wrong Hall Event detected)
2	HIES	read-only	Hall Inputs Update Status value1 = #0 (Transition on the Hall Inputs not detected) value2 = #1 (Transition on the Hall Inputs detected)
4	MSTS	read-only	Multi-Channel pattern shadow transfer status value1 = #0 (Shadow transfer not done) value2 = #1 (Shadow transfer done)
8	INDXS	read-only	Quadrature Index Status value1 = #0 (Index event not detected) value2 = #1 (Index event detected)
9	ERRS	read-only	Quadrature Phase Error Status value1 = #0 (Phase Error event not detected) value2 = #1 (Phase Error event detected)
10	CNTS	read-only	Quadrature CLK Status value1 = #0 (Quadrature clock not generated) value2 = #1 (Quadrature clock generated)
11	DIRS	read-only	Quadrature Direction Change value1 = #0 (Change on direction not detected) value2 = #1 (Change on direction detected)
12	PCLKS	read-only	Quadrature Period Clk Status value1 = #0 (Period clock not generated) value2 = #1 (Period clock generated)
13-31, 5-7, 30		read	Reserved

12.2.16 PFLGE

CORDIC Coprocessor Interrupt Enable

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0			PCLSEL [28]	DIRSEL [27]	CNTSEL [26]	ERRSEL [25]	INDSEL [24]	0			MSTSEL [20]	0	HIESEL [18]	WHESEL [17]	CHESEL [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0			EPCLK [12]	EDIR [11]	ECNT [10]	EERR [9]	EINDX [8]	0			EMST [4]	0	EHIE [2]	EWHE [1]	ECHE [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	ECHE	read-write	Correct Hall Event Enable value1 = #0 (Correct Hall Event interrupt disabled) value2 = #1 (Correct Hall Event interrupt enabled)
1	EWHE	read-write	Wrong Hall Event Enable value1 = #0 (Wrong Hall Event interrupt disabled) value2 = #1 (Wrong Hall Event interrupt enabled)
2	EHIE	read-write	Hall Input Update Enable value1 = #0 (Update of the Hall Inputs interrupt is disabled) value2 = #1 (Update of the Hall Inputs interrupt is enabled)
4	EMST	read-write	Multi-Channel pattern shadow transfer enable value1 = #0 (Shadow transfer event interrupt disabled) value2 = #1 (Shadow transfer event interrupt enabled)
8	EINDX	read-write	Quadrature Index Event Enable value1 = #0 (Index event interrupt disabled) value2 = #1 (Index event interrupt enabled)
9	EERR	read-write	Quadrature Phase Error Enable value1 = #0 (Phase error event interrupt disabled) value2 = #1 (Phase error event interrupt enabled)
10	ECNT	read-write	Quadrature CLK interrupt Enable value1 = #0 (Quadrature CLK event interrupt disabled) value2 = #1 (Quadrature CLK event interrupt enabled)
11	EDIR	read-write	Quadrature direction change interrupt Enable value1 = #0 (Direction change event interrupt disabled) value2 = #1 (Direction change event interrupt enabled)
12	EPCLK	read-write	Quadrature Period CLK interrupt Enable value1 = #0 (Quadrature Period CLK event interrupt disabled) value2 = #1 (Quadrature Period CLK event interrupt enabled)
16	CHESEL	read-write	Correct Hall Event Service Request Selector value1 = #0 (Correct Hall Event interrupt forward to POSIFx.SR0) value2 = #1 (Correct Hall Event interrupt forward to POSIFx.SR1)
17	WHESEL	read-write	Wrong Hall Event Service Request Selector value1 = #0 (Wrong Hall Event interrupt forward to POSIFx.SR0) value2 = #1 (Wrong Hall Event interrupt forward to POSIFx.SR1)
18	HIESEL	read-write	Hall Inputs Update Event Service Request Selector value1 = #0 (Hall Inputs Update Event interrupt forward to POSIFx.SR0) value2 = #1 (Hall Inputs Update Event interrupt forward to POSIFx.SR1)
20	MSTSEL	read-write	Multi-Channel pattern Update Event Service Request Selector value1 = #0 (Multi-Channel pattern Update Event interrupt forward to POSIFx.SR0) value2 = #1 (Multi-Channel pattern Update Event interrupt forward to POSIFx.SR1)

Bits	Field	Access	Description
24	INDSEL	read-write	Quadrature Index Event Service Request Selector value1 = #0 (Quadrature Index Event interrupt forward to POSIFx.SR0) value2 = #1 (Quadrature Index Event interrupt forward to POSIFx.SR1)
25	ERRSEL	read-write	Quadrature Phase Error Event Service Request Selector value1 = #0 (Quadrature Phase error Event interrupt forward to POSIFx.SR0) value2 = #1 (Quadrature Phase error Event interrupt forward to POSIFx.SR1)
26	CNTSEL	read-write	Quadrature Clock Event Service Request Selector value1 = #0 (Quadrature Clock Event interrupt forward to POSIFx.SR0) value2 = #1 (Quadrature Clock Event interrupt forward to POSIFx.SR1)
27	DIRSEL	read-write	Quadrature Direction Update Event Service Request Selector value1 = #0 (Quadrature Direction Update Event interrupt forward to POSIFx.SR0) value2 = #1 (Quadrature Direction Update Event interrupt forward to POSIFx.SR1)
28	PCLSEL	read-write	Quadrature Period clock Event Service Request Selector value1 = #0 (Quadrature Period clock Event interrupt forward to POSIFx.SR0) value2 = #1 (Quadrature Period clock Event interrupt forward to POSIFx.SR1)
29-31, 21-23019, 13-15, 5-7, 3		read	Reserved

12.2.17 SPFLG

CORDIC Coprocessor Interrupt Set

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0			SPCLK [12]	SDIR [11]	SCNT [10]	SERR [9]	SINDX [8]	0			SMST [4]	0	SHIE [2]	SWHE [1]	SCHE [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	SCHE	write-only	Correct Hall Event flag set
1	SWHE	write-only	Wrong Hall Event flag set
2	SHIE	write-only	Hall Inputs Update Event flag set
4	SMST	write-only	Multi-Channel Pattern shadow transfer flag set
8	SINDX	write-only	Quadrature Index flag set
9	SERR	write-only	Quadrature Phase Error flag set
10	SCNT	write-only	Quadrature CLK flag set
11	SDIR	write-only	Quadrature Direction flag set
12	SPCLK	write-only	Quadrature period clock flag set
13-31, 5-7, 30		read	Reserved

12.2.18 RPFLG

CORDIC Coprocessor Interrupt Clear

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0			RPCLK [12]	RDIR [11]	RCNT [10]	RERR [9]	RINDX [8]	0			RMST [4]	0	RHIE [2]	RWHE [1]	RCHE [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	RCHE	write-only	Correct Hall Event flag clear
1	RWHE	write-only	Wrong Hall Event flag clear
2	RHIE	write-only	Hall Inputs Update Event flag clear
4	RMST	write-only	Multi-Channel Pattern shadow transfer flag clear
8	RINDX	write-only	Quadrature Index flag clear
9	RERR	write-only	Quadrature Phase Error flag clear
10	RCNT	write-only	Quadrature CLK flag clear
11	RDIR	write-only	Quadrature Direction flag clear
12	RPCLK	write-only	Quadrature period clock flag clear
13-31, 5-7, 30		read	Reserved

12.2.19 PDBG

CORDIC Coprocessor Debug register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0	LPP2 [27:22]	LPP1 [21:16]
31 30 29 28	27 26 25 24 23 22	21 20 19 18 17 16

Bit-field table (15 … 0)

0	LPP0 [13:8]	HSP [7:5]	IVAL [4]	QPSV [3:2]	QCSV [1:0]
15 14	13 12 11 10 9 8	7 6 5	4	3 2	1 0

Bit-fields

Bits	Field	Access	Description
1:0	QCSV	read-only	Quadrature Decoder Current state
3:2	QPSV	read-only	Quadrature Decoder Previous state
4	IVAL	read-only	Current Index Value
7:5	HSP	read-only	Hall Current Sampled Pattern
13:8	LPP0	read-only	Actual count of the Low Pass Filter for POSI0
21:16	LPP1	read-only	Actual count of the Low Pass Filter for POSI1
27:22	LPP2	read-only	Actual count of the Low Pass Filter for POSI2
28-31, 14-15	0	read	Reserved

13 Private peripheral bus Registers

Cortex-M0 Private Peripheral Block

13.1 Register overview

Instance	Base address
PPB	0xE000E000

Register name	Offset	Reset	Description
SYST_CSR	0x10	0x00000000	SysTick Control and Status Register
SYST_RVR	0x14	0x00000000	SysTick Reload Value Register
SYST_CVR	0x18	0x00000000	SysTick Current Value Register
SYST_CALIB	0x1C	0x40000147	SysTick Calibration Value Register
NVIC_ISER	0x100	0x00000000	Interrupt Set-enable Register
NVIC_ICER	0x180	0x00000000	IInterrupt Clear-enable Register
NVIC_ISPR	0x200	0x00000000	Interrupt Set-pending Register
NVIC_ICPR	0x280	0x00000000	Interrupt Clear-pending Register
NVIC_IPR0	0x400	0x00000000	Interrupt Priority Register 0
NVIC_IPR1	0x404	0x00000000	Interrupt Priority Register 1
NVIC_IPR2	0x408	0x00000000	Interrupt Priority Register 2
NVIC_IPR3	0x40C	0x00000000	Interrupt Priority Register 3
NVIC_IPR4	0x410	0x00000000	Interrupt Priority Register 4
NVIC_IPR5	0x414	0x00000000	Interrupt Priority Register 5
NVIC_IPR6	0x418	0x00000000	Interrupt Priority Register 6
NVIC_IPR7	0x41C	0x00000000	Interrupt Priority Register 7
CPUID	0xD00	0x410CC200	CPUID Base Register
ICSR	0xD04	0x00000000	Interrupt Control and State Register
AIRCR	0xD0C	0xFA050000	Application Interrupt and Reset Control Register
SCR	0xD10	0x00000000	System Control Register
CCR	0xD14	0x00000208	Configuration and Control Register
SHPR2	0xD1C	0x00000000	System Handler Priority Register 2
SHPR3	0xD20	0x00000000	System Handler Priority Register 3
SHCSR	0xD24	0x00000000	System Handler Control and State Register

13.2 Register details

13.2.1 SYST_CSR

SysTick Control and Status Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0	COUNTFLAG [16]
31 … 17	16

Bit-field table (15 … 0)

0	CLKSOURCE [2]	TICKINT [1]	ENABLE [0]
15 … 3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	ENABLE	read-write	Counter Enable value1 = #0 (Counter disabled.) value2 = #1 (Counter enabled.)
1	TICKINT	read-write	SysTick Exception Request value1 = #0 (Counting down to zero does not assert the SysTick exception request.) value2 = #1 (Counting down to zero to assert the SysTick exception request.)
2	CLKSOURCE	read-write	Clock Source value1 = #0 (External clock.) value2 = #1 (Processor clock.)
16	COUNTFLAG	read-write	Counter Flag
17-31, 3-15	0	read	Reserved

13.2.2 SYST_RVR

SysTick Reload Value Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0								RELOAD [23:16]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

RELOAD [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
23:0	RELOAD	read-write	Reload Value
24-31	0	read	Reserved

13.2.3 SYST_CVR

SysTick Current Value Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0								CURRENT [23:16]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

CURRENT [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
23:0	CURRENT	read-write	SysTick Counter Current Value
24-31	0	read	Reserved

13.2.4 SYST_CALIB

SysTick Calibration Value Register

Reset 0x40000147

Width 32

Bit-field table (31 … 16)

NOREF [31]	SKEW [30]	0	TENMS [23:16]
31	30	29 28 27 26 25 24	23 22 21 20 19 18 17 16

Bit-field table (15 … 0)

TENMS [15:0]
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit-fields

Bits	Field	Access	Description
23:0	TENMS	read-only	10 Milliseconds
30	SKEW	read-only	Clock Skew
31	NOREF	read-only	Reference Clock
24-29	0	read	Reserved

13.2.5 NVIC_ISER

Interrupt Set-enable Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

SETENA [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

SETENA [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:0	SETENA	read-write	Interrupt Node Set-enable value1 = #0 (Read: Interrupt node disabled. Write: No effect.) value2 = #1 (Read: Interrupt node enabled. Write: Enable interrupt node)

13.2.6 NVIC_ICER

IInterrupt Clear-enable Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

CLRENA [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

CLRENA [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:0	CLRENA	read-write	Interrupt Node Clear-enable value1 = #0 (Read: Interrupt node disabled. Write: No effect) value2 = #1 (Read: Interrupt node enabled. Write: Disable interrupt node.)

13.2.7 NVIC_ISPR

Interrupt Set-pending Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

SETPEND [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

SETPEND [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:0	SETPEND	read-write	Interrupt Node Set-pending value1 = #0 (Read: Interrupt node is not pending. Write: No effect) value2 = #1 (Read: Interrupt node is pending. Write: Change interrupt state to pending.)

13.2.8 NVIC_ICPR

Interrupt Clear-pending Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

CLRPEND [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

CLRPEND [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:0	CLRPEND	read-write	Interrupt Node Clear-pending value1 = #0 (Read: Interrupt node is not pending. Write: No effect.) value2 = #1 (Read: Interrupt node is pending. Write: Remove interrupt state from pending.)

13.2.9 NVIC_IPR0

Interrupt Priority Register 0

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PRI_3 [31:24]								PRI_2 [23:16]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PRI_1 [15:8]								PRI_0 [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	PRI_0	read-write	Priority, Byte Offset 0
15:8	PRI_1	read-write	Priority, Byte Offset 1
23:16	PRI_2	read-write	Priority, Byte Offset 2
31:24	PRI_3	read-write	Priority, Byte Offset 3

13.2.10 NVIC_IPR1

Interrupt Priority Register 1

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PRI_3 [31:24]								PRI_2 [23:16]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PRI_1 [15:8]								PRI_0 [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	PRI_0	read-write	Priority, Byte Offset 0
15:8	PRI_1	read-write	Priority, Byte Offset 1
23:16	PRI_2	read-write	Priority, Byte Offset 2
31:24	PRI_3	read-write	Priority, Byte Offset 3

13.2.11 NVIC_IPR2

Interrupt Priority Register 2

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PRI_3 [31:24]								PRI_2 [23:16]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PRI_1 [15:8]								PRI_0 [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	PRI_0	read-write	Priority, Byte Offset 0
15:8	PRI_1	read-write	Priority, Byte Offset 1
23:16	PRI_2	read-write	Priority, Byte Offset 2
31:24	PRI_3	read-write	Priority, Byte Offset 3

13.2.12 NVIC_IPR3

Interrupt Priority Register 3

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PRI_3 [31:24]								PRI_2 [23:16]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PRI_1 [15:8]								PRI_0 [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	PRI_0	read-write	Priority, Byte Offset 0
15:8	PRI_1	read-write	Priority, Byte Offset 1
23:16	PRI_2	read-write	Priority, Byte Offset 2
31:24	PRI_3	read-write	Priority, Byte Offset 3

13.2.13 NVIC_IPR4

Interrupt Priority Register 4

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PRI_3 [31:24]								PRI_2 [23:16]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PRI_1 [15:8]								PRI_0 [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	PRI_0	read-write	Priority, Byte Offset 0
15:8	PRI_1	read-write	Priority, Byte Offset 1
23:16	PRI_2	read-write	Priority, Byte Offset 2
31:24	PRI_3	read-write	Priority, Byte Offset 3

13.2.14 NVIC_IPR5

Interrupt Priority Register 5

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PRI_3 [31:24]								PRI_2 [23:16]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PRI_1 [15:8]								PRI_0 [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	PRI_0	read-write	Priority, Byte Offset 0
15:8	PRI_1	read-write	Priority, Byte Offset 1
23:16	PRI_2	read-write	Priority, Byte Offset 2
31:24	PRI_3	read-write	Priority, Byte Offset 3

13.2.15 NVIC_IPR6

Interrupt Priority Register 6

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PRI_3 [31:24]								PRI_2 [23:16]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PRI_1 [15:8]								PRI_0 [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	PRI_0	read-write	Priority, Byte Offset 0
15:8	PRI_1	read-write	Priority, Byte Offset 1
23:16	PRI_2	read-write	Priority, Byte Offset 2
31:24	PRI_3	read-write	Priority, Byte Offset 3

13.2.16 NVIC_IPR7

Interrupt Priority Register 7

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PRI_3 [31:24]								PRI_2 [23:16]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PRI_1 [15:8]								PRI_0 [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	PRI_0	read-write	Priority, Byte Offset 0
15:8	PRI_1	read-write	Priority, Byte Offset 1
23:16	PRI_2	read-write	Priority, Byte Offset 2
31:24	PRI_3	read-write	Priority, Byte Offset 3

13.2.17 CPUID

CPUID Base Register

Reset	0x410CC200
Width	32

Bit-field table (31 … 16)

Implementer [31:24]								Variant [23:20]				Architecture [19:16]			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PartNo [15:4]												Revision [3:0]			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
3:0	Revision	read-only	Revision Number value1 = 0x0 (Patch 0)
15:4	PartNo	read-only	Part Number of the Processor value1 = 0xC20 (Cortex-M0)
19:16	Architecture	read-only	Architecture value1 = 0xC (ARMv6-M)
23:20	Variant	read-only	Variant Number value1 = 0x0 (Revision 0)
31:24	Implementer	read-only	Implementer Code value1 = 0x41 (ARM)

13.2.18 ICSR

Interrupt Control and State Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0			PEND SVSET [28]	PEND SVCL R [27]	PEND STSET [26]	PEND STCLR [25]	0		ISRPE NDING [22]	0				VECTPENDING [17:16]	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

VECTPENDING [15:12]				0						VECTACTIVE [5:0]					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
5:0	VECTACTIVE	read-only	Active Exception Number value1 = 0x00 (Thread mode)
17:12	VECTPENDING	read-only	Pending Exception Number value1 = 0x0 (No pending exceptions)
22	ISRPENDING	read-only	Interrupt Pending Flag value1 = #0 (Interrupt not pending) value2 = #1 (Interrupt pending.)
25	PENDSTCLR	write-only	SysTick Exception Clear-pending value1 = #0 (No effect) value2 = #1 (removes the pending state from the SysTick exception.)
26	PENDSTSET	read-write	SysTick Exception Set-pending value1 = 0 (SysTick exception is not pending) value2 = 1 (SysTick exception is pending.)
27	PENDSVCLR	write-only	PendSV Clear Pending value1 = #0 (Do not clear.) value2 = #1 (Removes pending state from PendSV exception.)
28	PENDSVSET	read-write	PendSV Set Pending value1 = #0 (PendSV exception is not pending.) value2 = #1 (PendSV excepton is pending.)
29-31, 23-24	18-21, 6-11	read	Reserved

13.2.19 AIRCR

Application Interrupt and Reset Control Register

Reset	0xFA050000
Width	32

Bit-field table (31 … 16)

VECTKEY [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

ENDIANNESS [15]	0												SYSRESETREQ [2]	0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
2	SYSRESETREQ	write-only	System Reset Request value1 = #0 (No effect.) value2 = #1 (Requests a system level reset.)
15	ENDIANNESS	read-only	Data Endianness value1 = #0 (Little-endian)
31:16	VECTKEY	read-write	Register Key
3-14, 0-1	0	read	Reserved

13.2.20 SCR

System Control Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0											SEVONPEND [4]	0	SLEEPDEEP [2]	SLEEPONEXIT [1]	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
1	SLEEPONEXIT	read-write	Sleep-on-exit value1 = #0 (Do not sleep when returning to Thread mode.) value2 = #1 (Enter sleep, or deep sleep, on return from an ISR to Thread mode.)
2	SLEEPDEEP	read-write	Low Power Sleep Mode value1 = #0 (Sleep) value2 = #1 (Deep sleep)
4	SEVONPEND	read-write	Send Event on Pending bit value1 = #0 (Only enabled interrupts or events can wakeup the processor, disabled interrupts are excluded.) value2 = #1 (Enabled events and all interrupts, including disabled interrupts, can wakeup the processor.)
5-31, 3, 0	0	read	Reserved

13.2.21 CCR

Configuration and Control Register

Reset	0x00000208
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0						STKALIGN [9]	0					UNALIGN_TRP [3]	0		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
3	UNALIGN_TRP	read-only	Unaligned Access Traps
9	STKALIGN	read-only	Stack Alignment
10-31, 4-8, 0-2	0	read	Reserved

13.2.22 SHPR2

System Handler Priority Register 2

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PRI_11 [31:24]								0							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:24	PRI_11	read-write	Priority of System Handler 11
0-23	0	read	Reserved

13.2.23 SHPR3

System Handler Priority Register 3

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

PRI_15 [31:24]								PRI_14 [23:16]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
23:16	PRI_14	read-write	Priority of System Handler 14
31:24	PRI_15	read-write	Priority of System Handler 15
0-15	0	read	Reserved

13.2.24 SHCSR

System Handler Control and State Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															

Bit-field table (15 … 0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SVCALLPENDED [15]								0							

Bit-fields

Bits	Field	Access	Description
15	SVCALLPENDED	read-write	SVCall Pending bit value1 = #0 (SVCall is not pending.) value2 = #1 (SVCall is pending.)
16-31, 0-14	0	read	Reserved

14 Pseudo Random Number Generator Registers

PRNG Unit

14.1 Register overview

Instance	Base address
PRNG	0x48020000

Register name	Offset	Reset	Description
WORD	0x00	0x0000	PRNG Word Register
CHK	0x04	0x0000	PRNG Status Check Register
CTRL	0x0C	0x0000	PRNG Control Register

14.2 Register details

14.2.1 WORD

PRNG Word Register

Reset	0x0000
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

RDATA [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
15:0	RDATA	read-write	Random Data

14.2.2 CHK

PRNG Status Check Register

Reset	0x0000
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0															RDV [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	RDV	read-only	Random Data / Key Valid Flag value1 = #0 (New random data block is not yet ready to be read. In) this flag is set to #0 while loading is in progress.) value2 = #1 (Random data block is valid. In key loading mode this value indicates that the next partial key word can be written to PRNG_WORD.)
1-15	0	read	Reserved

14.2.3 CTRL

PRNG Control Register

Reset	0x0000
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0												KLD [3]	RDBS [2:1]		0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
2:1	RDBS	read-write	Random Data Block Size value1 = #00 (Reset state (no random data block size defined), value of PRNG_WORD is undefined.) value2 = #01 (8 bits in PRNG_WORD.RDATA[7:0]) value3 = #10 (16 bits in PRNG_WORD.RDATA[15:0])
3	KLD	read-write	Key Load Operation Mode value1 = #0 (Streaming mode (default)) value2 = #1 (Key loading mode)
4-15, 0	0	read	Reserved

15 Real Time Clock Registers

Real Time Clock

15.1 Register overview

Instance	Base address
RTC	0x40010A00

Register name	Offset	Reset	Description
ID	0x00	0x00A3C000	RTC Module ID Register
CTR	0x04	0x7FFF0000	RTC Control Register
RAWSTAT	0x08	0x00000000	RTC Raw Service Request Register
STSSR	0x0C	0x00000000	RTC Service Request Status Register
MSKSR	0x10	0x00000000	RTC Service Request Mask Register
CLRSR	0x14	0x00000000	RTC Clear Service Request Register
ATIM0	0x18	0x00000000	RTC Alarm Time Register 0
ATIM1	0x1C	0x00000000	RTC Alarm Time Register 1
TIM0	0x20	0x00000000	RTC Time Register 0
TIM1	0x24	0x00000000	RTC Time Register 1

15.2 Register details

15.2.1 ID

RTC Module ID Register

Reset	0x00A3C000
Width	32

Bit-field table (31 … 16)

MOD_NUMBER [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

MOD_TYPE [15:8]								MOD_REV [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	MOD_REV	read-only	Module Revision Number
15:8	MOD_TYPE	read-only	Module Type
31:16	MOD_NUMBER	read-only	Module Number Value

15.2.2 CTR

RTC Control Register

Reset	0x7FFF0000
Width	32

Bit-field table (31 … 16)

DIV [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0														SUS [1]	ENB [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	ENB	read-write	RTC Module Enable
1	SUS	read-write	Debug Suspend Control
31:16	DIV	read-write	Divider Value
2-15	0	read	Reserved

15.2.3 RAWSTAT

RTC Raw Service Request Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0							RAI [8]	0	RPYE [6]	RPMO [5]	0	RPDA [3]	RPHO [2]	RPMI [1]	RPSE [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	RPSE	read-only	Raw Periodic Seconds Service Request
1	RPMI	read-only	Raw Periodic Minutes Service Request
2	RPHO	read-only	Raw Periodic Hours Service Request
3	RPDA	read-only	Raw Periodic Days Service Request
5	RPMO	read-only	Raw Periodic Months Service Request
6	RPYE	read-only	Raw Periodic Years Service Request
8	RAI	read-only	Alarm Service Request
9-31, 7, 4	0	read	Reserved

15.2.4 STSSR

RTC Service Request Status Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0							SAI [8]	0	SPYE [6]	SPMO [5]	0	SPDA [3]	SPHO [2]	SPMI [1]	SPSE [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	SPSE	read-only	Periodic Seconds Service Request Status after masking
1	SPMI	read-only	Periodic Minutes Service Request Status after masking
2	SPHO	read-only	Periodic Hours Service Request Status after masking
3	SPDA	read-only	Periodic Days Service Request Status after masking
5	SPMO	read-only	Periodic Months Service Request Status after masking
6	SPYE	read-only	Periodic Years Service Request Status after masking
8	SAI	read-only	Alarm Service Request Status after masking
9-31, 7, 4	0	read	Reserved

15.2.5 MSKSR

RTC Service Request Mask Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0							MAI [8]	0	MPYE [6]	MPMO [5]	0	MPDA [3]	MPHO [2]	MPMI [1]	MPSE [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	MPSE	read-write	Periodic Seconds Interrupt Mask
1	MPMI	read-write	Periodic Minutes Interrupt Mask
2	MPHO	read-write	Periodic Hours Interrupt Mask
3	MPDA	read-write	Periodic Days Interrupt Mask
5	MPMO	read-write	Periodic Months Interrupt Mask
6	MPYE	read-write	Periodic Years Interrupt Mask
8	MAI	read-write	Alarm Interrupt Mask
9-31, 7, 4	0	read	Reserved

15.2.6 CLRSR

RTC Clear Service Request Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0							RAI [8]	0	RPYE [6]	RPMO [5]	0	RPDA [3]	RPHO [2]	RPMI [1]	RPSE [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	RPSE	write-only	Raw Periodic Seconds Interrupt Clear
1	RPMI	write-only	Raw Periodic Minutes Interrupt Clear
2	RPHO	write-only	Raw Periodic Hours Interrupt Clear
3	RPDA	write-only	Raw Periodic Days Interrupt Clear
5	RPMO	write-only	Raw Periodic Months Interrupt Clear
6	RPYE	write-only	Raw Periodic Years Interrupt Clear
8	RAI	write-only	Raw Alarm Interrupt Clear
9-31, 7, 4	0	read	Reserved

15.2.7 ATIM0

RTC Alarm Time Register 0

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0			ADA [28:24]					0			AHO [20:16]				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0			AMI [13:8]					0		ASE [5:0]					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
5:0	ASE	read-write	Alarm Seconds Compare Value
13:8	AMI	read-write	Alarm Minutes Compare Value
20:16	AHO	read-write	Alarm Hours Compare Value
28:24	ADA	read-write	Alarm Days Compare Value
29-31, 21-23, 14-15, 6-7		read	Reserved

15.2.8 ATIM1

RTC Alarm Time Register 1

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

AYE [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0				AMO [11:8]				0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
11:8	AMO	read-write	Alarm Month Compare Value
31:16	AYE	read-write	Alarm Year Compare Value
12-15, 0-7	0	read	Reserved

15.2.9 TIM0

RTC Time Register 0

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0			DA [28:24]					0			HO [20:16]				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0			MI [13:8]					0		SE [5:0]					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
5:0	SE	read-write	Seconds Time Value
13:8	MI	read-write	Minutes Time Value
20:16	HO	read-write	Hours Time Value
28:24	DA	read-write	Days Time Value
29-31, 21-23	14-15, 6-7	read	Reserved

15.2.10 TIM1

RTC Time Register 1

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

YE [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0				MO [11:8]				0					DAWE [2:0]		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
2:0	DAWE	read-write	Days of Week Time Value
11:8	MO	read-write	Month Time Value
31:16	YE	read-write	Year Time Value
12-15, 3-7	0	read	Reserved

16 Sample and Hold Sequencer Registers

Sample and Hold ADC Sequencer

16.1 Register overview

Instance	Base address
SHS0	0x48034000

Register name	Offset	Reset	Description
ID	0x08	0x0099C000	Module Identification Register
SHSCFG	0x40	0x00000000	SHS Configuration Register
STEPCFG	0x44	0x00000098	Stepper Configuration Register
TIMCFG0	0x80	0x00000001	Timing Configuration Register 0
TIMCFG1	0x84	0x00000001	Timing Configuration Register 1
CALCTR	0xBC	0x03100400	Calibration Control Register
CALGC0	0xC0	0x20002000	Gain Calibration Control Register 0
CALGC1	0xC4	0x20002000	Gain Calibration Control Register 1
CALOC0	0xE0	0x00000000	Offset Calibration Control Register 0
CALOC1	0xE4	0x00000000	Offset Calibration Control Register 1
GNCTR00	0x180	0x00000000	Gain Control Register 00
GNCTR10	0x190	0x00000000	Gain Control Register 10
LOOP	0x50	0x00000000	Loop Control Register

16.2 Register details

16.2.1 ID

Module Identification Register

Reset	0x0099C000
Width	32

Bit-field table (31 … 16)

MOD_NUMBER [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

MOD_TYPE [15:8]								MOD_REV [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	MOD_REV	read-only	Module Revision
15:8	MOD_TYPE	read-only	Module Type
31:16	MOD_NUMBER	read-only	Module Number

16.2.2 SHSCFG

SHS Configuration Register

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

STATE [31:28]				TC [27:24]				0						SP1 [17]	SP0 [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

SCWC [15]	ANRDY [14]	0	ANOFF [12]	AREF [11:10]		0						DIVS [3:0]			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
3:0	DIVS	read-write	Divider Factor for the SHS Clock value1 = #0000 (fSH = fCONV / 1) value2 = #0001 (fSH = fCONV / 2) value3 = #0111 (fSH = fCONV / 8)
11:10	AREF	read-write	Analog Calbration Reference Voltage Selection value1 = #00 (External reference, upper supply range) value3 = #10 (Internal reference, upper supply range) value4 = #11 (Internal reference, lower supply range)
12	ANOFF	read-write	Analog Converter Power Down Force value1 = #0 (Converter controlled by bitfields ANONS (digital control block)) value2 = #1 (Converter is permanently off)
14	ANRDY	read-only	Analog Converter Ready value1 = #0 (Converter is in power-down mode) value2 = #1 (Converter is operable)
15	SCWC	write-only	Write Control for SHS Configuration value1 = #0 (No write access to SHS configuration) value2 = #1 (Bitfields ANOFF, AREF, DIVS can be written)
16	SP0	read-only	Sample Pending on S&H Unit x value1 = #0 (No sample pending) value2 = #1 (S&H unit x has finished the sample phase)
17	SP1	read-only	Sample Pending on S&H Unit x value1 = #0 (No sample pending) value2 = #1 (S&H unit x has finished the sample phase)
27:24	TC	read-write	Test Control value1 = #1011 (Internal test functions enabled)
31:28	STATE	read-only	Current State of Sequencer value1 = #0000 (Idle) value2 = #0001 (Offset calibration active) value3 = #0010 (Gain calibration active) value4 = #0011 (Startup calibration active) value5 = #1000 (Stepper process active for S&H unit 0) value6 = #1001 (Stepper process active for S&H unit 1)
18-23, 13, 4-0		read	Reserved

16.2.3 STEPCFG

Stepper Configuration Register

Reset	0x00000098
Width	32

Bit-field table (31 … 16)

SEN7 [31]	KSEL7 [30:28]			SEN6 [27]	KSEL6 [26:24]			SEN5 [23]	KSEL5 [22:20]			SEN4 [19]	KSEL4 [18:16]		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

SEN3 [15]	KSEL3 [14:12]			SEN2 [11]	KSEL2 [10:8]			SEN1 [7]	KSEL1 [6:4]			SEN0 [3]	KSEL0 [2:0]		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
2:0	KSEL0	read-write	Kernel Select
3	SEN0	read-write	Step x Enable value1 = #0 (Off: This step is not part of the stepper sequence) value2 = #1 (Active: This step is executed during the sequence)
6:4	KSEL1	read-write	Kernel Select
7	SEN1	read-write	Step x Enable value1 = #0 (Off: This step is not part of the stepper sequence) value2 = #1 (Active: This step is executed during the sequence)
10:8	KSEL2	read-write	Kernel Select
11	SEN2	read-write	Step x Enable value1 = #0 (Off: This step is not part of the stepper sequence) value2 = #1 (Active: This step is executed during the sequence)
14:12	KSEL3	read-write	Kernel Select
15	SEN3	read-write	Step x Enable value1 = #0 (Off: This step is not part of the stepper sequence) value2 = #1 (Active: This step is executed during the sequence)
18:16	KSEL4	read-write	Kernel Select
19	SEN4	read-write	Step x Enable value1 = #0 (Off: This step is not part of the stepper sequence) value2 = #1 (Active: This step is executed during the sequence)
22:20	KSEL5	read-write	Kernel Select
23	SEN5	read-write	Step x Enable value1 = #0 (Off: This step is not part of the stepper sequence) value2 = #1 (Active: This step is executed during the sequence)
26:24	KSEL6	read-write	Kernel Select
27	SEN6	read-write	Step x Enable value1 = #0 (Off: This step is not part of the stepper sequence) value2 = #1 (Active: This step is executed during the sequence)
30:28	KSEL7	read-write	Kernel Select
31	SEN7	read-write	Step x Enable value1 = #0 (Off: This step is not part of the stepper sequence) value2 = #1 (Active: This step is executed during the sequence)

16.2.4 TIMCFG0

Timing Configuration Register 0

Reset	0x00000001
Width	32

Bit-field table (31 … 16)

0	TGEN [29:16]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0	SST [13:8]	FCRT [7:4]	0	AT [0]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	AT	read-write	Accelerated Timing value1 = #0 (Compatible timing: Result available after standard conversion time) value2 = #1 (Accelerated timing: Result available as soon as converted)
7:4	FCRT	read-write	Fast Compare Mode Response Time value1 = 0x0 (Result after tADCI x 2) value2 = 0xF (Result after tADCI x 32)
13:8	SST	read-write	Short Sample Time value1 = 0x00 (Compatible timing: Sample time is defined by DIVA and STC.) value2 = 0x01 (Sample time is tADC x 1) value3 = 0x3F (Sample time is tADC x 63)
29:16	TGEN	read-only	Timing Generator
30-31, 14-15	01-3	read	Reserved

16.2.5 TIMCFG1

Timing Configuration Register 1

Reset	0x00000001
Width	32

Bit-field table (31 … 16)

0	TGEN [29:16]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0	SST [13:8]	FCRT [7:4]	0	AT [0]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	AT	read-write	Accelerated Timing value1 = #0 (Compatible timing: Result available after standard conversion time) value2 = #1 (Accelerated timing: Result available as soon as converted)
7:4	FCRT	read-write	Fast Compare Mode Response Time value1 = 0x0 (Result after tADCI x 2) value2 = 0xF (Result after tADCI x 32)
13:8	SST	read-write	Short Sample Time value1 = 0x00 (Compatible timing: Sample time is defined by DIVA and STC.) value2 = 0x01 (Sample time is tADC x 1) value3 = 0x3F (Sample time is tADC x 63)
29:16	TGEN	read-only	Timing Generator
30-31, 14-15	01-3	read	Reserved

16.2.6 CALCTR

Calibration Control Register

Reset	0x03100400
Width	32

Bit-field table (31 … 16)

SUCAL [31]	0	CALMAX [29:24]						0	SUCALVAL [22:16]						
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0		CALGNSTC [13:8]						0							CALORD [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	CALORD	read-write	Calibration Order value1 = #0 (Do conversions then calibration) value2 = #1 (Do calibration then conversions)
13:8	CALGNSTC	read-write	Gain Calibration Sample Time Control
22:16	SUCALVAL	read-write	Startup Calibration Cycles
29:24	CALMAX	read-write	Calibration Maximum Timing
31	SUCAL	write-only	Start-Up Calibration value1 = #0 (No action) value2 = #1 (Initiate the start-up calibration phase (indication in bitfield SHSCFG.STATE))
30, 23, 14-15, 1-7	0	read	Reserved

16.2.7 CALGC0

Gain Calibration Control Register 0

Reset	0x20002000
Width	32

Bit-field table (31 … 16)

GNAWC [31]	0	CALGNVALA [29:16]														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	

Bit-field table (15 … 0)

GNSWC [15]	0	CALGNVALS [13:0]														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Bit-fields

Bits	Field	Access	Description
13:0	CALGNVALS	read-write	Gain Calibration Value, Standard Reference
15	GNSWC	write-only	Gain Calibration Write Control, Standard value1 = #0 (No write access to gain calibration parameter) value2 = #1 (CALGNVALS can be written)
29:16	CALGNVALA	read-write	Gain Calibration Value, Alternate Reference
31	GNAWC	write-only	Gain Calibration Write Control, Alternate value1 = #0 (No write access to gain calibration parameter) value2 = #1 (CALGNVALA can be written)
30, 14	0	read	Reserved

16.2.8 CALGC1

Gain Calibration Control Register 1

Reset	0x20002000
Width	32

Bit-field table (31 … 16)

GNAWC [31]	0	CALGNVALA [29:16]														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	

Bit-field table (15 … 0)

GNSWC [15]	0	CALGNVALS [13:0]														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Bit-fields

Bits	Field	Access	Description
13:0	CALGNVALS	read-write	Gain Calibration Value, Standard Reference
15	GNSWC	write-only	Gain Calibration Write Control, Standard value1 = #0 (No write access to gain calibration parameter) value2 = #1 (CALGNVALS can be written)
29:16	CALGNVALA	read-write	Gain Calibration Value, Alternate Reference
31	GNAWC	write-only	Gain Calibration Write Control, Alternate value1 = #0 (No write access to gain calibration parameter) value2 = #1 (CALGNVALA can be written)
30, 14	0	read	Reserved

16.2.9 CALOC0

Offset Calibration Control Register 0

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

DISCAL [31]	CALOFFVAL3 [30:24]							0	CALOFFVAL2 [22:16]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	

Bit-field table (15 … 0)

OFFWC [15]	CALOFFVAL1 [14:8]							0	CALOFFVAL0 [6:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Bit-fields

Bits	Field	Access	Description
6:0	CALOFFVAL0	read-write	Offset Calibration Value for Gain Level z
14:8	CALOFFVAL1	read-write	Offset Calibration Value for Gain Level z
15	OFFWC	write-only	Offset Calibration Write Control value1 = #0 (No write access to offset cal. parameters) value2 = #1 (CALOFFVALz can be written)
22:16	CALOFFVAL2	read-write	Offset Calibration Value for Gain Level z
30:24	CALOFFVAL3	read-write	Offset Calibration Value for Gain Level z
31	DISCAL	read-write	Disable Calibration value1 = #0 (Calibration enabled (offset and gain)) value2 = #1 (No calibration)
23, 7	0	read	Reserved

16.2.10 CALOC1

Offset Calibration Control Register 1

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

DISCAL [31]	CALOFFVAL3 [30:24]							0	CALOFFVAL2 [22:16]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	

Bit-field table (15 … 0)

OFFWC [15]	CALOFFVAL1 [14:8]							0	CALOFFVAL0 [6:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Bit-fields

Bits	Field	Access	Description
6:0	CALOFFVAL0	read-write	Offset Calibration Value for Gain Level z
14:8	CALOFFVAL1	read-write	Offset Calibration Value for Gain Level z
15	OFFWC	write-only	Offset Calibration Write Control value1 = #0 (No write access to offset cal. parameters) value2 = #1 (CALOFFVALz can be written)
22:16	CALOFFVAL2	read-write	Offset Calibration Value for Gain Level z
30:24	CALOFFVAL3	read-write	Offset Calibration Value for Gain Level z
31	DISCAL	read-write	Disable Calibration value1 = #0 (Calibration enabled (offset and gain)) value2 = #1 (No calibration)
23, 7	0	read	Reserved

16.2.11 GNCTR00

Gain Control Register 00

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

GAIN7 [31:28]				GAIN6 [27:24]				GAIN5 [23:20]				GAIN4 [19:16]			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

GAIN3 [15:12]				GAIN2 [11:8]				GAIN1 [7:4]				GAIN0 [3:0]			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
3:0	GAIN0	read-write	Gain Control 0 value1 = #0000 (Gain factor = 1) value2 = #0001 (Gain factor = 3) value3 = #0010 (Gain factor = 6) value4 = #0011 (Gain factor = 12)
7:4	GAIN1	read-write	Gain Control 1 value1 = #0000 (Gain factor = 1) value2 = #0001 (Gain factor = 3) value3 = #0010 (Gain factor = 6) value4 = #0011 (Gain factor = 12)
11:8	GAIN2	read-write	Gain Control 2 value1 = #0000 (Gain factor = 1) value2 = #0001 (Gain factor = 3) value3 = #0010 (Gain factor = 6) value4 = #0011 (Gain factor = 12)
15:12	GAIN3	read-write	Gain Control 3 value1 = #0000 (Gain factor = 1) value2 = #0001 (Gain factor = 3) value3 = #0010 (Gain factor = 6) value4 = #0011 (Gain factor = 12)
19:16	GAIN4	read-write	Gain Control 4 value1 = #0000 (Gain factor = 1) value2 = #0001 (Gain factor = 3) value3 = #0010 (Gain factor = 6) value4 = #0011 (Gain factor = 12)
23:20	GAIN5	read-write	Gain Control 5 value1 = #0000 (Gain factor = 1) value2 = #0001 (Gain factor = 3) value3 = #0010 (Gain factor = 6) value4 = #0011 (Gain factor = 12)
27:24	GAIN6	read-write	Gain Control 6 value1 = #0000 (Gain factor = 1) value2 = #0001 (Gain factor = 3) value3 = #0010 (Gain factor = 6) value4 = #0011 (Gain factor = 12)
31:28	GAIN7	read-write	Gain Control 7 value1 = #0000 (Gain factor = 1) value2 = #0001 (Gain factor = 3) value3 = #0010 (Gain factor = 6) value4 = #0011 (Gain factor = 12)

16.2.12 GNCTR10

Gain Control Register 10

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

GAIN7 [31:28]				GAIN6 [27:24]				GAIN5 [23:20]				GAIN4 [19:16]			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

GAIN3 [15:12]				GAIN2 [11:8]				GAIN1 [7:4]				GAIN0 [3:0]			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
3:0	GAIN0	read-write	Gain Control 0 value1 = #0000 (Gain factor = 1) value2 = #0001 (Gain factor = 3) value3 = #0010 (Gain factor = 6) value4 = #0011 (Gain factor = 12)
7:4	GAIN1	read-write	Gain Control 1 value1 = #0000 (Gain factor = 1) value2 = #0001 (Gain factor = 3) value3 = #0010 (Gain factor = 6) value4 = #0011 (Gain factor = 12)
11:8	GAIN2	read-write	Gain Control 2 value1 = #0000 (Gain factor = 1) value2 = #0001 (Gain factor = 3) value3 = #0010 (Gain factor = 6) value4 = #0011 (Gain factor = 12)
15:12	GAIN3	read-write	Gain Control 3 value1 = #0000 (Gain factor = 1) value2 = #0001 (Gain factor = 3) value3 = #0010 (Gain factor = 6) value4 = #0011 (Gain factor = 12)
19:16	GAIN4	read-write	Gain Control 4 value1 = #0000 (Gain factor = 1) value2 = #0001 (Gain factor = 3) value3 = #0010 (Gain factor = 6) value4 = #0011 (Gain factor = 12)
23:20	GAIN5	read-write	Gain Control 5 value1 = #0000 (Gain factor = 1) value2 = #0001 (Gain factor = 3) value3 = #0010 (Gain factor = 6) value4 = #0011 (Gain factor = 12)
27:24	GAIN6	read-write	Gain Control 6 value1 = #0000 (Gain factor = 1) value2 = #0001 (Gain factor = 3) value3 = #0010 (Gain factor = 6) value4 = #0011 (Gain factor = 12)
31:28	GAIN7	read-write	Gain Control 7 value1 = #0000 (Gain factor = 1) value2 = #0001 (Gain factor = 3) value3 = #0010 (Gain factor = 6) value4 = #0011 (Gain factor = 12)

16.2.13 LOOP

Loop Control Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

LPEN1 [31]	0						LPSH1 [24]	0				LPCH1 [20:16]				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	

Bit-field table (15 … 0)

LPEN0 [15]	0						LPSH0 [8]	0				LPCH0 [4:0]				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Bit-fields

Bits	Field	Access	Description
4:0	LPCH0	read-write	Loop y Channel
8	LPSH0	read-write	Loop y Sample&Hold Unit
15	LPEN0	read-write	Loop y Enable value1 = 0x0 (Off: standard operation) value2 = 0x1 (ON: sigma-delta-loop is active)
20:16	LPCH1	read-write	Loop y Channel
24	LPSH1	read-write	Loop y Sample&Hold Unit
31	LPEN1	read-write	Loop y Enable value1 = 0x0 (Off: standard operation) value2 = 0x1 (ON: sigma-delta-loop is active)
25-30, 21-23	09-14, 5-7	read	Reserved

17 System control unit – SCU Registers

System Control Unit

17.1 Register overview

Instance	Base address
SCU_ANALOG	0x40011000

Register name	Offset	Reset	Description
ANATSECTRL	0x24	0x0000	Temperature Sensor Control Register
ANATSEIH	0x30	0x0000	Temperature Sensor High Temperature Interrupt Register
ANATSEIL	0x34	0xFFFF	Temperature Sensor Low Temperature Interrupt Register
ANATSEMON	0x40	0x0000	Temperature Sensor Counter2 Monitor Register
ANAVDEL	0x50	0x001C	Voltage Detector Control Register
ANAOFFSET	0x6C	0x0040	DCO1 Offset Register
ANAOSCLPCTRL	0x8C	0x0003	OSC_LP Control Register
ANAOSCHPCTRL	0x90	0x0038	OSC_HP Control Register
ANASYNC1	0x78	0x0B72	DCO1 Sync Control Register 1
ANASYNC2	0x7C	0x0002	DCO1 Sync Control Register 2

17.2 Register details

17.2.1 ANATSECTRL

Temperature Sensor Control Register

Reset	0x0000
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0															TSE_EN [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	TSE_EN	read-write	Temperature sensor enable value1 = #0 (Temperature sensor is disabled) value2 = #1 (Temperature sensor is switched on)
1-15	0	read	Reserved

17.2.2 ANATSEIH

Temperature Sensor High Temperature Interrupt Register

Reset	0x0000
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

TSE_IH [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
15:0	TSE_IH	read-write	Counter value for high temperature interrupt

17.2.3 ANATSEIL

Temperature Sensor Low Temperature Interrupt Register

Reset	0xFFFF
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

TSE_IL [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
15:0	TSE_IL	read-write	Counter value for low temperature interrupt

17.2.4 ANATSEMON

Temperature Sensor Counter2 Monitor Register

Reset	0x0000
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

TSE_MON [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
15:0	TSE_MON	read-only	Result values; loaded by TSE_DONE

17.2.5 ANAVDEL

Voltage Detector Control Register

Reset	0x001C
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0											VDEL_EN [4]	VDEL_TIM_ADJ [3:2]		VDEL_SELECT [1:0]	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
1:0	VDEL_SELECT	read-write	VDEL Range Select value1 = #00 (2.25V) value2 = #01 (3.0V) value3 = #10 (4.4V)
3:2	VDEL_TIM_ADJ	read-write	VDEL Timing Setting value1 = #00 (typ 1us - slowest response time) value2 = #01 (typ 500n) value3 = #10 (typ 250n) value4 = #11 (no delay - fastest response time.)
4	VDEL_EN	read-write	VDEL unit Enable value1 = #0 (VDEL is disabled) value2 = #1 (VDEL is active)
5-15	0	read	Reserved

17.2.6 ANAOFFSET

DCO1 Offset Register

Reset	0x0040
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0									ADJL_OFFSET [6:0]						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
6:0	ADJL_OFFSET	read-write	ADJL Offset register value1 = 0x00 (- 3.xx%, typ.) value2 = 0x3F (DCO1 ADJL value is reduced by 1 step (DCO_ADJL - 1).) value3 = 0x40 (0, DCO_ADJL is not changed, default) value4 = 0x41 (DCO1 ADJL value is increased by 1 step (DCO_ADJL + 1)) value5 = 0x7F (+ 3.xx%, typ.)
7-15	0	read	Reserved

17.2.7 ANAOSCLPCTRL

OSC_LP Control Register

Reset	0x0003
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0														MODE [1:0]	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
1:0	MODE	read-write	OSC_LP Oscillator Mode value1 = #00 (Oscillator is enabled and in operation mode (OSC mode)) value2 = #01 (Oscillator is enabled, shaper is bypassed) value3 = #10 (Oscillator is in power down mode) value4 = #11 (Oscillator is in power down mode , Pad can be used in GPIO mode)
2-15	0	read	Reserved

17.2.8 ANAOSCHPCTRL

OSC_HP Control Register

Reset	0x0038
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0									HYSC TRL [6]	MODE [5:4]		GAINSEL [3:2]		SHBY [1]	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
1	SHBY	read-write	Shaper Bypass Mode value1 = #0 (The shaper is not bypassed) value2 = #1 (The shaper is bypassed)
3:2	GAINSEL	read-write	OSC_HP Oscillator Gain Selection value1 = #00 (Gain control is configured for frequencies from 4 MHz to y1 MHz) value2 = #01 (Gain control is configured for frequencies from 4 MHz to y2 MHz) value3 = #10 (Gain control is configured for frequencies from 4 MHz to 20 MHz)
5:4	MODE	read-write	OSC_HP Oscillator Mode value1 = #00 (Oscillator is enabled and in active power mode with shaper enabled (OSC mode)) value2 = #01 (Oscillator in power down mode with shaper enabled (External Clock Input Mode).) value3 = #10 (Oscillator is enabled with shaper disabled. No clock output is available unless the shaper is bypass (SHBY=1)) value4 = #11 (Oscillator is in power down mode with shaper disabled. Pad can be used in GPIO mode.)
6	HYSCTRL	read-write	Shaper Hystersis Mode value1 = #0 (External clock frequency < 20MHz.) value2 = #1 (External clock frequency > 20MHz)
7-15, 0	0	read	Reserved

17.2.9 ANASYNC1

DCO1 Sync Control Register 1

Reset 0x0B72

Width 16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

XTAL_SEL [15]	SYNC_DCO_EN [14]	SYNC_PRELOAD [13:0]													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
13:0	SYNC_PRELOAD	read-write	Counter target value, which defines the update cycle value1 = 0x1FFF (Longest integration time = best accuracy)
14	SYNC_DCO_EN	read-write	DCO1 synchronization feature enable value1 = #0 (No DCO1 synchronization via an external clock source. This option is used for the DCO1 calibration using the temperature sensor.) value2 = #1 (DCO1 gets synchronized via an external clock source.)
15	XTAL_SEL	read-write	Oscillator Source select value1 = #0 (OSC_LP is selected) value2 = #1 (OSC_HP is selected)

17.2.10 ANASYNC2

DCO1 Sync Control Register 2

Reset	0x0002
Width	16

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0			SYNC_READY [12]	0	PRESCALER [10:0]										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
10:0	PRESCALER	read-write	Prescaler value value1 = 0x000 (Bypass: Internal sync counter frequency = crystal frequency) value2 = 0x001 (DIV1: Internal sync counter feed freq. = crystal frequency/1) value3 = 0x002 (DIV2: Internal sync counter feed freq. = crystal frequency/2) value4 = 0x7FF (Maximum divider value (for best accuracy, but slowest response))
12	SYNC_READY	read-only	DCO1 frequency reached its target value value1 = #0 (Actual DCO1 frequency is out of targe) value2 = #1 (DCO1 is synchronized to the XTAL frequency)
13-15, 11	0	read	Reserved

18 System control unit – SCU_CLK Registers

System Control Unit

18.1 Register overview

Instance	Base address
SCU_CLK	0x40010300

Register name	Offset	Reset	Description
CLKCR	0x00	0x30000600	Clock Control Register
CLKCR1	0x1C	0x00000100	Clock Control Register 1
PWRSVCR	0x04	0x00000000	Power Save Control Register
CGATSTAT0	0x08	0x003F07FF	Peripheral 0 Clock Gating Status
CGATSET0	0x0C	0x00000000	Peripheral 0 Clock Gating Set
CGATCLR0	0x10	0x00000000	Peripheral 0 Clock Gating Clear
OSCCSR	0x14	0x00000000	Oscillator Control and Status Register

18.2 Register details

18.2.1 CLKCR

Clock Control Register

Reset 0x30000600

Width 32

Bit-field table (31 … 16)

VDDC 2HIGH [31]	VDDC 2LOW [30]	CNTADJ [29:20]										RTCCLKSEL [19:17]			PCLKS EL [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

IDIV [15:8]								FDIV [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	FDIV	read-write	Fractional Divider Selection, FDIV[7:0]
15:8	IDIV	read-write	Divider Selection value1 = 0x00 (Divider is bypassed.) value2 = 0x01 (1;) value3 = 0x02 (2;) value4 = 0x03 (3;) value5 = 0x04 (4;) value6 = 0xFE (254;) value7 = 0xFF (255;)
16	PCLKSEL	read-write	PCLK Clock Select value1 = #0 (PCLK = MCLK) value2 = #1 (PCLK = 2 x MCLK)
19:17	RTCCLKSEL	read-write	RTC Clock Select
29:20	CNTADJ	read-write	Counter Adjustment value1 = 0x000 (1 clock cycles of the DCO1, 48MHz clock) value2 = 0x001 (2 clock cycles of the DCO1, 48MHz clock) value3 = 0x002 (3 clock cycles of the DCO1, 48MHz clock) value4 = 0x003 (4 clock cycles of the DCO1, 48MHz clock) value5 = 0x004 (5 clock cycles of the DCO1, 48MHz clock) value6 = 0x300 (769 clock cycles of the DCO1, 48MHz clock) value7 = 0x3FE (1023 clock cycles of the DCO1, 48MHz clock) value8 = 0x3FF (1024 clock cycles of the DCO1, 48MHz clock)
30	VDDC2LOW	read-only	VDDC too low value1 = #0 (VDDC is not too low and the fractional divider input clock is running at the targeted frequency) value2 = #1 (VDDC is too low and the fractional divider input clock is not running at the targeted frequency)
31	VDDC2HIGH	read-only	VDDC too high value1 = #0 (VDDC is not too high) value2 = #1 (VDDC is too high)

18.2.2 CLKCR1

Clock Control Register 1

Reset	0x00000100
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0						DCLK SEL [9]	ADCC LKSEL [8]	0						FDIV [1:0]	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
1:0	FDIV	read-write	Fractional Divider Selection, FDIV[9:8]
8	ADCCLKSEL	read-write	ADC Converter Clock Select value1 = #0 (fCONV= 48MHz) value2 = #1 (fCONV= 32MHz)
9	DCLKSEL	read-write	Doubler Clock Source Select value1 = #0 (DCO1) value2 = #1 (External clock via OSC_HP)
10-31, 2-7	0	read	Reserved

18.2.3 PWRSVCR

Power Save Control Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0															FPD [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	FPD	read-write	Flash Power Down value1 = #0 (no effect) value2 = #1 (Flash power down when entering power save mode. Upon wake-up, CPU is able to fetch code from flash.)
1-31	0	read	Reserved

18.2.4 CGATSTAT0

Peripheral 0 Clock Gating Status

Reset 0x003F07FF

Width 32

Bit-field table (31 … 16)

0										MCAN 0 [21]	POSIF 1 [20]	0	USIC1 [18]	CCU41 [17]	CCU81 [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0					RTC [1 0]	WDT [9]	MATH [8]	POSIF 0 [7]	0		BCCU 0 [4]	USIC0 [3]	CCU40 [2]	CCU80 [1]	VADC [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	VADC	read-only	VADC and SHS Gating Status value1 = #0 (gating de-asserted) value2 = #1 (gating asserted)
1	CCU80	read-only	CCU80 Gating Status value1 = #0 (gating de-asserted) value2 = #1 (gating asserted)
2	CCU40	read-only	CCU40 Gating Status value1 = #0 (gating de-asserted) value2 = #1 (gating asserted)
3	USIC0	read-only	USIC0 Gating Status value1 = #0 (gating de-asserted) value2 = #1 (gating asserted)
4	BCCU0	read-only	BCCU0 Gating Status value1 = #0 (gating de-asserted) value2 = #1 (gating asserted)
7	POSIF0	read-only	POSIF0 Gating Status value1 = #0 (gating de-asserted) value2 = #1 (gating asserted)
8	MATH	read-only	MATH Gating Status value1 = #0 (gating de-asserted) value2 = #1 (gating asserted)
9	WDT	read-only	WDT Gating Status value1 = #0 (gating de-asserted) value2 = #1 (gating asserted)
10	RTC	read-only	RTC Gating Status value1 = #0 (gating de-asserted) value2 = #1 (gating asserted)
16	CCU81	read-only	CCU81 Gating Status value1 = #0 (gating de-asserted) value2 = #1 (gating asserted)
17	CCU41	read-only	CCU41 Gating Status value1 = #0 (gating de-asserted) value2 = #1 (gating asserted)
18	USIC1	read-only	USIC1 Gating Status value1 = #0 (gating de-asserted) value2 = #1 (gating asserted)
20	POSIF1	read-only	POSIF1 Gating Status value1 = #0 (gating de-asserted) value2 = #1 (gating asserted)
21	MCAN0	read-only	MultiCAN Gating Status value1 = #0 (gating de-asserted) value2 = #1 (gating asserted)
22-31, 19, 11-15, 5-6	0	read	Reserved

18.2.5 CGATSET0

Peripheral 0 Clock Gating Set

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0										MCAN 0 [21]	POSIF 1 [20]	0	USIC1 [18]	CCU41 [17]	CCU81 [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0					RTC [1 0]	WDT [9]	MATH [8]	POSIF 0 [7]	0		BCCU 0 [4]	USIC0 [3]	CCU40 [2]	CCU80 [1]	VADC [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	VADC	write-only	VADC and SHS Gating Set value1 = #0 (no effect) value2 = #1 (enable gating)
1	CCU80	write-only	CCU80 Gating Set value1 = #0 (no effect) value2 = #1 (enable gating)
2	CCU40	write-only	CCU40 Gating Set value1 = #0 (no effect) value2 = #1 (enable gating)
3	USIC0	write-only	USIC0 Gating Set value1 = #0 (no effect) value2 = #1 (enable gating)
4	BCCU0	write-only	BCCU0 Gating Set value1 = #0 (no effect) value2 = #1 (enable gating)
7	POSIF0	write-only	POSIF0 Gating Set value1 = #0 (no effect) value2 = #1 (enable gating)
8	MATH	write-only	MATH Gating Set value1 = #0 (no effect) value2 = #1 (enable gating)
9	WDT	write-only	WDT Gating Set value1 = #0 (no effect) value2 = #1 (enable gating)
10	RTC	write-only	RTC Gating Set value1 = #0 (no effect) value2 = #1 (enable gating)
16	CCU81	write-only	CCU81 Gating Set value1 = #0 (no effect) value2 = #1 (enable gating)
17	CCU41	write-only	CCU41 Gating Set value1 = #0 (no effect) value2 = #1 (enable gating)
18	USIC1	write-only	USIC1 Gating Set value1 = #0 (no effect) value2 = #1 (enable gating)
20	POSIF1	write-only	POSIF1 Gating Set value1 = #0 (no effect) value2 = #1 (enable gating)
21	MCAN0	write-only	MutliCAN Gating Set value1 = #0 (no effect) value2 = #1 (enable gating)
22-31, 19, 11-15, 5-6	10	read	Reserved

18.2.6 CGATCLR0

Peripheral 0 Clock Gating Clear

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0										MCAN 0 [21]	POSIF 1 [20]	0	USIC1 [18]	CCU41 [17]	CCU81 [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0					RTC [1 0]	WDT [9]	MATH [8]	POSIF 0 [7]	0		BCCU 0 [4]	USIC0 [3]	CCU40 [2]	CCU80 [1]	VADC [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	VADC	write-only	VADC and SHS Gating Clear value1 = #0 (no effect) value2 = #1 (disable gating)
1	CCU80	write-only	CCU80 Gating Clear value1 = #0 (no effect) value2 = #1 (disble gating)
2	CCU40	write-only	CCU40 Gating Clear value1 = #0 (no effect) value2 = #1 (disable gating)
3	USIC0	write-only	USIC0 Gating Clear value1 = #0 (no effect) value2 = #1 (disable gating)
4	BCCU0	write-only	BCCU0 Gating Clear value1 = #0 (no effect) value2 = #1 (disable gating)
7	POSIF0	write-only	POSIF0 Gating Clear value1 = #0 (no effect) value2 = #1 (disable gating)
8	MATH	write-only	MATH Gating Clear value1 = #0 (no effect) value2 = #1 (disable gating)
9	WDT	write-only	WDT Gating Clear value1 = #0 (no effect) value2 = #1 (disble gating)
10	RTC	write-only	RTC Gating Clear value1 = #0 (no effect) value2 = #1 (disable gating)
16	CCU81	write-only	CCU81 Gating Clear value1 = #0 (no effect) value2 = #1 (disable gating)
17	CCU41	write-only	CCU41 Gating Clear value1 = #0 (no effect) value2 = #1 (disable gating)
18	USIC1	write-only	USIC1 Gating Clear value1 = #0 (no effect) value2 = #1 (disable gating)
20	POSIF1	write-only	POSIF1 Gating Clear value1 = #0 (no effect) value2 = #1 (disable gating)
21	MCAN0	write-only	MutliCAN Gating Clear value1 = #0 (no effect) value2 = #1 (disable gating)
22-31, 19, 11-15, 5-6	10	read	Reserved

18.2.7 OSCCSR

Oscillator Control and Status Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0						XOWDEN [25]	XOWDRES [24]	0						OWDEN [17]	OWDRES [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0							DCO1PD [8]	0						OSC2H [1]	OSC2L [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	OSC2L	read-only	Oscillator Valid Low Status Bit value1 = #0 (The OSC frequency is usable) value2 = #1 (The OSC frequency is not usable. Frequency is too low.)
1	OSC2H	read-only	Oscillator Valid High Status Bit value1 = #0 (The OSC frequency is usable) value2 = #1 (The OSC frequency is not usable. Frequency is too high.)
8	DCO1PD	read-write	DCO1 Power down value1 = #0 (DCO1 is not power down) value2 = #1 (DCO1 power down.)
16	OWDRES	read-write	Oscillator Watchdog Reset value1 = #0 (The Oscillator Watchdog is not cleared and remains active) value2 = #1 (The Oscillator Watchdog is cleared and restarted. The OSC2L and OSC2H flag will be held in the last value until it is updated after 3 standby clock cycles.)
17	OWDEN	read-write	Oscillator Watchdog Enable value1 = #0 (The Oscillator Watchdog is disabled) value2 = #1 (The Oscillator Watchdog is enabled)
24	XOWDRES	read-write	XTAL Oscillator Watchdog Reset value1 = #0 (The Oscillator Watchdog is not cleared and remains active) value2 = #1 (The Oscillator Watchdog is cleared and restarted.)
25	XOWDEN	read-write	XTAL Oscillator Watchdog Enable value1 = #0 (The XTAL Oscillator Watchdog is disabled) value2 = #1 (The XTAL Oscillator Watchdog is enabled)
26-31, 18-23, 9-15, 2-7		read	Reserved

19 System control unit – SCU_GENERAL Registers

System Control Unit

19.1 Register overview

Instance	Base address
SCU_GENERAL	0x40010000

Register name	Offset	Reset	Description
DBGROMID	0x00	0x10204083	Debug System ROM ID Register
IDCHIP	0x04	0x00000000	Chip ID Register
ID	0x08	0x00F4C000	SCU Module ID Register
SSW0	0x14	0x00000000	SSW Register 0
PASSWD	0x24	0x00000007	Password Register
CCUCON	0x30	0x00000000	CCU Control Register
MIRRSTS	0x48	0x00000000	Mirror Update Status Register
PMTSR	0x54	0x00000000	Parity Memory Test Select Register
PFUCR	0x68	0x00000001	Prefetch Unit Control Register
INTCR0	0x6C	0x00000000	Interrupt Control Register 0
INTCR1	0x70	0x00000000	Interrupt Control Register 1
STSTAT	0x74	0x00000000	Startup Status Register

19.2 Register details

19.2.1 DBGROMID

Debug System ROM ID Register

Reset	0x10204083
Width	32

Bit-field table (31 … 16)

VERSION [31:28]				PARTNO [27:16]											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

PARTNO [15:12]				MANUFID [11:1]											0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
11:1	MANUFID	read-only	Manufactory Identity
27:12	PARTNO	read-only	Part Number
31:28	VERSION	read-only	Product version
0	0	read	Reserved

19.2.2 IDCHIP

Chip ID Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

IDCHIP [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

IDCHIP [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:0	IDCHIP	read-only	CHIP ID PSOC_C1 = 0x000C1XXX ('000C 1XXXH PSOC Control C1) TEMP_NEG40_85 = 0x000CXXX2 ('000C XXX2H temperature: -40C to 85C) TEMP_NEG40_105 = 0x000CXXX3 ('000C XXX3H temperature: -40C to 105C) TSSOP38 = 0x000CXX1X ('000C XX1XH TSSOP38 pin package) VQFN40 = 0x000CXX4X ('000C XX4XH VQFN40 pin package) VQFN48 = 0x000CXX8X ('000C XX8XH VQFN48 pin package) LQFP48 = 0x000CXXBX ('000C XXBXH LQFP-48 pin package)

19.2.3 ID

SCU Module ID Register

Reset	0x00F4C000
Width	32

Bit-field table (31 … 16)

MOD_NUMBER [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

MOD_TYPE [15:8]								MOD_REV [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	MOD_REV	read-only	Module Revision Number
15:8	MOD_TYPE	read-only	Module Type
31:16	MOD_NUMBER	read-only	Module Number Value

19.2.4 SSW0

SSW Register 0

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

DAT [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

DAT [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:0	DAT	read-write	SSW Data

19.2.5 PASSWD

Password Register

Reset	0x00000007
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0								PASS [7:3]					PROTS [2]	MODE [1:0]	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
1:0	MODE	read-write	Bit Protection Scheme Control Bits value1 = #00 (Scheme disabled - direct access to the protected bits is allowed.) value2 = #11 (Scheme enabled - the bit field PASS has to be written with the passwords to open and close the access to the protected bits. (Default))
2	PROTS	read-only	Bit Protection Signal Status Bit value1 = #0 (Software is able to write to all protected bits.) value2 = #1 (Software is unable to write to any of the protected bits.)
7:3	PASS	write-only	Password Bits value1 = #11000 (Enables writing of the bit field MODE.) value2 = #10011 (Opens access to writing of all protected bits.) value3 = #10101 (Closes access to writing of all protected bits.)
8-31	0	read	Reserved

19.2.6 CCUCON

CCU Control Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0						GSC81 [9]	GSC80 [8]	0						GSC41 [1]	GSC40 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	GSC40	read-write	Global Start Control CCU40
1	GSC41	read-write	Global Start Control CCU41
8	GSC80	read-write	Global Start Control CCU80
9	GSC81	read-write	Global Start Control CCU81
10-31, 2-7	0	read	Reserved

19.2.7 MIRRSTS

Mirror Update Status Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0											RTC_TIM1 [4]	RTC_TIM0 [3]	RTC_ATIM1 [2]	RTC_ATIM0 [1]	RTC_CTR [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	RTC_CTR	read-only	RTC CTR Mirror Register Update Status
1	RTC_ATIM0	read-only	RTC ATIM0 Mirror Register Update Status
2	RTC_ATIM1	read-only	RTC ATIM1 Mirror Register Update Status
3	RTC_TIM0	read-only	RTC TIM0 Mirror Register Update Status
4	RTC_TIM1	read-only	RTC TIM1 Mirror Register Update Status
5-31	0	read	Reserved

19.2.8 PMTSR

Parity Memory Test Select Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0															MTENS [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	MTENS	read-write	Parity Test Enable Control for 16kbytes SRAM value1 = #0 (standard operation) value2 = #1 (generate an inverted parity bit during a write operation)
1-31	0	read	Reserved

19.2.9 PFUCR

Prefetch Unit Control Register

Reset	0x00000001
Width	32

Bit-field table (31 … 16)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															

Bit-field table (15 … 0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															PFUBYP [0]

Bit-fields

Bits	Field	Access	Description
0	PFUBYP	read-write	Prefetch Unit (PFU) Bypass value1 = #0 (PFU not bypass) value2 = #1 (PFU bypass)
1-31	0	read	Reserved

19.2.10 INTCR0

Interrupt Control Register 0

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

INTSEL15 [31:30]		INTSEL14 [29:28]		INTSEL13 [27:26]		INTSEL12 [25:24]		INTSEL11 [23:22]		INTSEL10 [21:20]		INTSEL9 [19:18]		INTSEL8 [17:16]	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

INTSEL7 [15:14]		INTSEL6 [13:12]		INTSEL5 [11:10]		INTSEL4 [9:8]		INTSEL3 [7:6]		INTSEL2 [5:4]		INTSEL1 [3:2]		INTSEL0 [1:0]	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
1:0	INTSEL0	read-write	Interrupt Source Select for Node 0 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
3:2	INTSEL1	read-write	Interrupt Source Select for Node 1 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
5:4	INTSEL2	read-write	Interrupt Source Select for Node 2 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
7:6	INTSEL3	read-write	Interrupt Source Select for Node 3 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
9:8	INTSEL4	read-write	Interrupt Source Select for Node 4 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
11:10	INTSEL5	read-write	Interrupt Source Select for Node 5 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
13:12	INTSEL6	read-write	Interrupt Source Select for Node 6 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
15:14	INTSEL7	read-write	Interrupt Source Select for Node 7 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
17:16	INTSEL8	read-write	Interrupt Source Select for Node 8 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)

Bits	Field	Access	Description
19:18	INTSEL9	read-write	Interrupt Source Select for Node 9 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
21:20	INTSEL10	read-write	Interrupt Source Select for Node 10 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
23:22	INTSEL11	read-write	Interrupt Source Select for Node 11 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
25:24	INTSEL12	read-write	Interrupt Source Select for Node 12 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
27:26	INTSEL13	read-write	Interrupt Source Select for Node 13 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
29:28	INTSEL14	read-write	Interrupt Source Select for Node 14 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
31:30	INTSEL15	read-write	Interrupt Source Select for Node 15 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)

19.2.11 INTCR1

Interrupt Control Register 1

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

INTSEL31 [31:30]		INTSEL30 [29:28]		INTSEL29 [27:26]		INTSEL28 [25:24]		INTSEL27 [23:22]		INTSEL26 [21:20]		INTSEL25 [19:18]		INTSEL24 [17:16]	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

INTSEL23 [15:14]		INTSEL22 [13:12]		INTSEL21 [11:10]		INTSEL20 [9:8]		INTSEL19 [7:6]		INTSEL18 [5:4]		INTSEL17 [3:2]		INTSEL16 [1:0]	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
1:0	INTSEL16	read-write	Interrupt Source Select for Node 16 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
3:2	INTSEL17	read-write	Interrupt Source Select for Node 17 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
5:4	INTSEL18	read-write	Interrupt Source Select for Node 18 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
7:6	INTSEL19	read-write	Interrupt Source Select for Node 19 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
9:8	INTSEL20	read-write	Interrupt Source Select for Node 20 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
11:10	INTSEL21	read-write	Interrupt Source Select for Node 21 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
13:12	INTSEL22	read-write	Interrupt Source Select for Node 22 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
15:14	INTSEL23	read-write	Interrupt Source Select for Node 23 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
17:16	INTSEL24	read-write	Interrupt Source Select for Node 24 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)

Bits	Field	Access	Description
19:18	INTSEL25	read-write	Interrupt Source Select for Node 25 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
21:20	INTSEL26	read-write	Interrupt Source Select for Node 26 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
23:22	INTSEL27	read-write	Interrupt Source Select for Node 27 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
25:24	INTSEL28	read-write	Interrupt Source Select for Node 28 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
27:26	INTSEL29	read-write	Interrupt Source Select for Node 29 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
29:28	INTSEL30	read-write	Interrupt Source Select for Node 30 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)
31:30	INTSEL31	read-write	Interrupt Source Select for Node 31 value1 = #00 (Select source A) value2 = #01 (Select source B) value3 = #10 (Select source C) value4 = #11 (Select source A or B)

19.2.12 STSTAT

Startup Status Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0														HWCON [1:0]	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
1:0	HWCON	read-only	HW Configuration value1 = #00 (User productive mode (UPM)) value2 = #01 (ASC BSL) value3 = #10 (Alternate Boot Mode (ABM)) value4 = #11 (CAN BSL)
2-31	0	read	Reserved

20 System control unit – SCU_INTERRUPT Registers

System Control Unit

20.1 Register overview

Instance	Base address
SCU_INTERRUPT	0x40010038

Register name	Offset	Reset	Description
SRRAW	0x00	0x00000000	SCU Raw Service Request Status
SRMSK	0x04	0x00000000	SCU Service Request Mask
SRCLR	0x08	0x00000000	SCU Service Request Clear
SRSET	0x0C	0x00000000	SCU Service Request Set
SRRAW1	0x20	0x00000000	SCU Raw Service Request Status 1
SRMSK1	0x24	0x00000000	SCU Service Request Mask 1
SRCLR1	0x28	0x00000000	SCU Service Request Clear 1
SRSET1	0x2C	0x00000000	SCU Service Request Set 1

20.2 Register details

20.2.1 SRRAW

SCU Raw Service Request Status

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

TSE_LOW [31]	TSE_HIGH [30]	TSE_DONE [29]	RTC_TIM1 [28]	RTC_TIM0 [27]	RTC_ATIM1 [26]	RTC_ATIM0 [25]	RTC_CTR [24]	0	SBYCLKFI [22]	VCLIPI [21]	FLCMPLTI [20]	FLECC2I [19]	PEU0I [18]	PESRAMI [17]	LOCI [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

ORC7I [15]	ORC6I [14]	ORC5I [13]	ORC4I [12]	ORC3I [11]	ORC2I [10]	ORC1I [9]	ORC0I [8]	VDROPI [7]	ACMP2I [6]	ACMP1I [5]	ACMP0I [4]	VDDPI [3]	AI [2]	PI [1]	PRWARN [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	PRWARN	read-only	WDT pre-warning Event Status Before Masking
1	PI	read-only	RTC Raw Periodic Event Status Before Masking
2	AI	read-only	RTC Raw Alarm Event Status Before Masking
3	VDDPI	read-only	VDDP pre-warning Event Status Before Masking
4	ACMP0I	read-only	Analog Comparator 0 Event Status Before Masking
5	ACMP1I	read-only	Analog Comparator 1 Event Status Before Masking
6	ACMP2I	read-only	Analog Comparator 2 Event Status Before Masking
7	VDROPI	read-only	VDROP Event Status Before Masking
8	ORC0I	read-only	Out of Range Comparator X Event Status Before Masking
9	ORC1I	read-only	Out of Range Comparator X Event Status Before Masking
10	ORC2I	read-only	Out of Range Comparator X Event Status Before Masking
11	ORC3I	read-only	Out of Range Comparator X Event Status Before Masking
12	ORC4I	read-only	Out of Range Comparator X Event Status Before Masking
13	ORC5I	read-only	Out of Range Comparator X Event Status Before Masking
14	ORC6I	read-only	Out of Range Comparator X Event Status Before Masking
15	ORC7I	read-only	Out of Range Comparator X Event Status Before Masking
16	LOCI	read-only	Loss of DCO1 Clock Event Status Before Masking
17	PESRAMI	read-only	16kbytes SRAM Parity Error Event Status Before Masking
18	PEU0I	read-only	USIC0 SRAM Parity Error Event Status Before Masking
19	FLECC2I	read-only	Flash Double Bit ECC Event Status Before Masking
20	FLCMPLTI	read-only	Flash Operation Complete Event Status Before Masking
21	VCLIPI	read-only	VCLIP Event Status Before Masking
22	SBYCLKFI	read-only	Standby Clock Failure Event Status Before Masking
24	RTC_CTR	read-only	RTC CTR Mirror Register Update Status Before Masking
25	RTC_ATIM0	read-only	RTC ATIM0 Mirror Register Update Status Before Masking
26	RTC_ATIM1	read-only	RTC ATIM1 Mirror Register Update Status Before Masking
27	RTC_TIM0	read-only	RTC TIM0 Mirror Register Update Before Masking
28	RTC_TIM1	read-only	RTC TIM1 Mirror Register Update Status Before Masking
29	TSE_DONE	read-only	DTS Measurement Done Event Status Before Masking
30	TSE_HIGH	read-only	DTS Compare High Temperature Event Status Before Masking
31	TSE_LOW	read-only	DTS Compare Low Temperature Event Status Before Masking
23	0	read	Reserved

20.2.2 SRMSK

SCU Service Request Mask

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

TSE_LOW [31]	TSE_HIGH [30]	TSE_DONE [29]	RTC_TIM1 [28]	RTC_TIM0 [27]	RTC_ATIM1 [26]	RTC_ATIM0 [25]	RTC_CTR [24]	0	SBYCLKFI [22]	VCLIPI [21]	0	FLECC2I [19]	PEU0I [18]	PESRAMI [17]	LOCI [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

ORC7I [15]	ORC6I [14]	ORC5I [13]	ORC4I [12]	ORC3I [11]	ORC2I [10]	ORC1I [9]	ORC0I [8]	VDROPI [7]	ACMP2I [6]	ACMP1I [5]	ACMP0I [4]	VDDPI [3]	0	PRWARN [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	PRWARN	read-write	WDT pre-warning Interrupt Mask
3	VDDPI	read-write	VDDP pre-warning Interrupt Mask
4	ACMP0I	read-write	Analog Comparator 0 Interrupt Mask
5	ACMP1I	read-write	Analog Comparator 1 Interrupt Mask
6	ACMP2I	read-write	Analog Comparator 2 Interrupt Mask
7	VDROPI	read-write	VDROP Interrupt Mask
8	ORC0I	read-write	Out of Range Comparator X Interrupt Mask
9	ORC1I	read-write	Out of Range Comparator X Interrupt Mask
10	ORC2I	read-write	Out of Range Comparator X Interrupt Mask
11	ORC3I	read-write	Out of Range Comparator X Interrupt Mask
12	ORC4I	read-write	Out of Range Comparator X Interrupt Mask
13	ORC5I	read-write	Out of Range Comparator X Interrupt Mask
14	ORC6I	read-write	Out of Range Comparator X Interrupt Mask
15	ORC7I	read-write	Out of Range Comparator X Interrupt Mask
16	LOCI	read-write	Loss of DCO1 Clock Interrupt Mask
17	PESRAMI	read-write	16kbytes SRAM Parity Error Interrupt Mask
18	PEU0I	read-write	USIC0 SRAM Parity Error Interrupt Mask
19	FLECC2I	read-write	Flash Double Bit ECC Interrupt Mask
21	VCLIPI	read-write	VCLIP Interrupt Mask
22	SBYCLKFI	read-write	Standby Clock Failure Interrupt Mask
24	RTC_CTR	read-write	RTC CTR Mirror Register Update Mask
25	RTC_ATIM0	read-write	RTC ATIM0 Mirror Register Update Mask
26	RTC_ATIM1	read-write	RTC ATIM1 Mirror Register Update Mask
27	RTC_TIM0	read-write	RTC TIM0 Mirror Register Update Mask
28	RTC_TIM1	read-write	RTC TIM1 Mirror Register Update Mask
29	TSE_DONE	read-write	DTS Measurement Done Interrupt Mask
30	TSE_HIGH	read-write	DTS Compare High Temperature Interrupt Mask
31	TSE_LOW	read-write	DTS Compare Low Temperature Interrupt Mask
23, 20, 1-2	0	read	Reserved

20.2.3 SRCLR

SCU Service Request Clear

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

TSE_LOW [31]	TSE_HIGH [30]	TSE_DONE [29]	RTC_TIM1 [28]	RTC_TIM0 [27]	RTC_ATIM1 [26]	RTC_ATIM0 [25]	RTC_CTR [24]	0	SBYCLKFI [22]	VCLIPI [21]	FLCMPLTI [20]	FLECC2I [19]	PEU0I [18]	PESRAMI [17]	LOCI [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

ORC7I [15]	ORC6I [14]	ORC5I [13]	ORC4I [12]	ORC3I [11]	ORC2I [10]	ORC1I [9]	ORC0I [8]	VDROPI [7]	ACMP2I [6]	ACMP1I [5]	ACMP0I [4]	VDDPI [3]	AI [2]	PI [1]	PRWARN [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	PRWARN	write-only	WDT pre-warning Interrupt Clear
1	PI	write-only	RTC Periodic Interrupt Clear
2	AI	write-only	RTC Alarm Interrupt Clear
3	VDDPI	write-only	VDDP pre-warning Interrupt Clear
4	ACMP0I	write-only	Analog Comparator 0 Interrupt Clear
5	ACMP1I	write-only	Analog Comparator 1 Interrupt Clear
6	ACMP2I	write-only	Analog Comparator 2 Interrupt Clear
7	VDROPI	write-only	VDROP Interrupt Clear
8	ORC0I	write-only	Out of Range Comparator X Interrupt Clear
9	ORC1I	write-only	Out of Range Comparator X Interrupt Clear
10	ORC2I	write-only	Out of Range Comparator X Interrupt Clear
11	ORC3I	write-only	Out of Range Comparator X Interrupt Clear
12	ORC4I	write-only	Out of Range Comparator X Interrupt Clear
13	ORC5I	write-only	Out of Range Comparator X Interrupt Clear
14	ORC6I	write-only	Out of Range Comparator X Interrupt Clear
15	ORC7I	write-only	Out of Range Comparator X Interrupt Clear
16	LOCI	write-only	Loss of DCO1 Clock Interrupt Clear
17	PESRAMI	write-only	16kbytes SRAM Parity Error Interrupt Clear
18	PEU0I	write-only	USIC0 SRAM Parity Error Interrupt Clear
19	FLECC2I	write-only	Flash Double Bit ECC Interrupt Clear
20	FLCMPLTI	write-only	Flash Operation Complete Interrupt Clear
21	VCLIPI	write-only	VCLIP Interrupt Clear
22	SBYCLKFI	write-only	Standby Clock Failure Interrupt Clear
24	RTC_CTR	write-only	RTC CTR Mirror Register Update Clear
25	RTC_ATIM0	write-only	RTC ATIM0 Mirror Register Update Clear
26	RTC_ATIM1	write-only	RTC ATIM1 Mirror Register Update Clear
27	RTC_TIM0	write-only	RTC TIM0 Mirror Register Update Clear
28	RTC_TIM1	write-only	RTC TIM1 Mirror Register Update Clear
29	TSE_DONE	write-only	DTS Measurement Done Interrupt Clear
30	TSE_HIGH	write-only	DTS Compare High Temperature Interrupt Clear
31	TSE_LOW	write-only	DTS Compare Low Temperature Interrupt Clear
23	0	read	Reserved

20.2.4 SRSET

SCU Service Request Set

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

TSE_LOW [31]	TSE_HIGH [30]	TSE_DONE [29]	RTC_TIM1 [28]	RTC_TIM0 [27]	RTC_ATIM1 [26]	RTC_ATIM0 [25]	RTC_CTR [24]	0	SBYCLKFI [22]	VCLIPI [21]	FLCMPLTI [20]	FLECC2I [19]	PEU0I [18]	PESRAMI [17]	LOCI [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

ORC7I [15]	ORC6I [14]	ORC5I [13]	ORC4I [12]	ORC3I [11]	ORC2I [10]	ORC1I [9]	ORC0I [8]	VDROPI [7]	ACMP2I [6]	ACMP1I [5]	ACMP0I [4]	VDDPI [3]	AI [2]	PI [1]	PRWARN [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	PRWARN	write-only	WDT pre-warning Interrupt Set
1	PI	write-only	RTC Periodic Interrupt Set
2	AI	write-only	RTC Alarm Interrupt Set
3	VDDPI	write-only	VDDP pre-warning Interrupt Set
4	ACMP0I	write-only	Analog Comparator 0 Interrupt Set
5	ACMP1I	write-only	Analog Comparator 1 Interrupt Set
6	ACMP2I	write-only	Analog Comparator 2 Interrupt Set
7	VDROPI	write-only	VDROP Interrupt Set
8	ORC0I	write-only	Out of Range Comparator X Interrupt Set
9	ORC1I	write-only	Out of Range Comparator X Interrupt Set
10	ORC2I	write-only	Out of Range Comparator X Interrupt Set
11	ORC3I	write-only	Out of Range Comparator X Interrupt Set
12	ORC4I	write-only	Out of Range Comparator X Interrupt Set
13	ORC5I	write-only	Out of Range Comparator X Interrupt Set
14	ORC6I	write-only	Out of Range Comparator X Interrupt Set
15	ORC7I	write-only	Out of Range Comparator X Interrupt Set
16	LOCI	write-only	Loss of DCO1 Clock Interrupt Set
17	PESRAMI	write-only	16kbytes SRAM Parity Error Interrupt Set
18	PEU0I	write-only	USIC0 SRAM Parity Error Interrupt Set
19	FLECC2I	write-only	Flash Double Bit ECC Interrupt Set
20	FLCMPLTI	write-only	Flash Operation Complete Interrupt Set
21	VCLIPI	write-only	VCLIP Interrupt Set
22	SBYCLKFI	write-only	Standby Clock Failure Interrupt Set
24	RTC_CTR	write-only	RTC CTR Mirror Register Update Set
25	RTC_ATIM0	write-only	RTC ATIM0 Mirror Register Update Set
26	RTC_ATIM1	write-only	RTC ATIM1 Mirror Register Update Set
27	RTC_TIM0	write-only	RTC TIM0 Mirror Register Update Set
28	RTC_TIM1	write-only	RTC TIM1 Mirror Register Update Set
29	TSE_DONE	write-only	DTS Measurement Done Interrupt Set
30	TSE_HIGH	write-only	DTS Compare High Temperature Interrupt Set
31	TSE_LOW	write-only	DTS Compare Low Temperature Interrupt Set
23	0	read	Reserved

20.2.5 SRRAW1

SCU Raw Service Request Status 1

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0											DCO1 OFSI [4]	PEMCI [3]	PEU1I [2]	LOECI [1]	ACMP 3I [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	ACMP3I	read-only	Analog Comparator 3 Event Status Before Masking
1	LOECI	read-only	Loss of External OSC_HP Clock Event Status Before Masking
2	PEU1I	read-only	USIC1 SRAM Parity Error Event Status Before Masking
3	PEMCI	read-only	MultiCAN SRAM Parity Error Event Status Before Masking
4	DCO1OFSI	read-only	DCO1 Out of SYNC Event Status Before Masking
5-31	0	read	Reserved

20.2.6 SRMSK1

SCU Service Request Mask 1

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0											DCO1 OFSI [4]	PEMCI [3]	PEU1I [2]	LOECI [1]	ACMP 3I [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	ACMP3I	read-write	Analog Comparator 3 Interrupt Mask
1	LOECI	read-write	Loss of External OSC_HP Clock Interrupt Mask
2	PEU1I	read-write	USIC1 SRAM Parity Error Interrupt Mask
3	PEMCI	read-write	MultiCAN SRAM Parity Error Interrupt Mask
4	DCO1OFSI	read-write	DCO1 Out of SYNC Interrupt Mask
5-31	0	read	Reserved

20.2.7 SRCLR1

SCU Service Request Clear 1

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0											DCO1 OFSI [4]	PEMCI [3]	PEU1I [2]	LOECI [1]	ACMP 3I [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	ACMP3I	write-only	Analog Comparator 3 Interrupt Clear
1	LOECI	write-only	Loss of External OSC_HP Clock Interrupt Clear
2	PEU1I	write-only	USIC1 SRAM Parity Error Interrupt Clear
3	PEMCI	write-only	MultiCAN SRAM Parity Error Interrupt Clear
4	DCO1OFSI	write-only	DCO1 Out of SYNC Interrupt Clear
5-31	0	read	Reserved

20.2.8 SRSET1

SCU Service Request Set 1

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0											DCO1 OFSI [4]	PEMCI [3]	PEU1I [2]	LOECI [1]	ACMP 3I [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	ACMP3I	write-only	Analog Comparator 3 Interrupt Set
1	LOECI	write-only	Loss of External OSC_HP Clock Interrupt Set
2	PEU1I	write-only	USIC1 SRAM Parity Error Interrupt Set
3	PEMCI	write-only	MultiCAN SRAM Parity Error Interrupt Set
4	DCO1OFSI	write-only	DCO1 Out of SYNC Interrupt Set
5-31	0	read	Reserved

21 System control unit – SCU_POWER Registers

System Control Unit

21.1 Register overview

Instance	Base address
SCU_POWER	0x40010200

Register name	Offset	Reset	Description
VDESR	0x00	0x00000000	Voltage Detector Status Register

21.2 Register details

21.2.1 VDESR

Voltage Detector Status Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															

Bit-field table (15 … 0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0														VDDP PW [1]	VCLIP [0]

Bit-fields

Bits	Field	Access	Description
0	VCLIP	read-only	VCLIP Indication value1 = #0 (VCLIP is not active) value2 = #1 (VCLIP is active)
1	VDDPPW	read-only	VDDPPW Indication value1 = #0 (VDDP is above pre-warning threshold) value2 = #1 (VDDP is below pre-warningthreshold)
2-31	0	read	Reserved

22 System control unit – SCU_RESET Registers

System Control Unit

22.1 Register overview

Instance	Base address
SCU_RESET	0x40010400

Register name	Offset	Reset	Description
RSTSTAT	0x00	0x00000000	RCU Reset Status
RSTSET	0x04	0x00000000	RCU Reset Set Register
RSTCLR	0x08	0x00000000	RCU Reset Clear Register
RSTCON	0x0C	0x00000000	RCU Reset Control Register

22.2 Register details

22.2.1 RSTSTAT

RCU Reset Status

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0					LCKEN [10]	RSTSTAT [9:0]									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
9:0	RSTSTAT	read-only	Reset Status Information
10	LCKEN	read-only	Enable Lockup Status value1 = #0 (Reset by Lockup disabled) value2 = #1 (Reset by Lockup enabled)
11-31	0	read	Reserved

22.2.2 RSTSET

RCU Reset Set Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0					LCKEN [10]	0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
10	LCKEN	write-only	Enable Lockup Reset value1 = #0 (no effect) value2 = #1 (Enable reset when Lockup gets asserted)
11-31, 0-9	0	read	Reserved

22.2.3 RSTCLR

RCU Reset Clear Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0					LCKEN [10]	0									RSCLR [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	RSCLR	write-only	Clear Reset Status value1 = #0 (no effect) value2 = #1 (Clears field RSTSTAT.RSTSTAT)
10	LCKEN	write-only	Enable Lockup Reset value1 = #0 (no effect) value2 = #1 (Disable reset when Lockup gets asserted)
11-31, 1-9	0	read	Reserved

22.2.4 RSTCON

RCU Reset Control Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0	MRSTEN [16]
31 … 17	16

Bit-field table (15 … 0)

0	LOECRSTEN [6]	MPERSTEN [5]	U1PERSTEN [4]	U0PERSTEN [3]	SPERSTEN [2]	LOCRSTEN [1]	ECCRSTEN [0]
15 … 7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	ECCRSTEN	read-write	Enable ECC Error Reset value1 = #0 (No reset when ECC double bit error occur) value2 = #1 (Reset when ECC double bit error occur)
1	LOCRSTEN	read-write	Enable Loss of DCO1 Clock Reset value1 = #0 (No reset when loss of DCO1 clock occur) value2 = #1 (Reset when loss of DCO1 clock occur)
2	SPERSTEN	read-write	Enable 16kbytes SRAM Parity Error Reset value1 = #0 (No reset when SRAM parity error occur) value2 = #1 (Reset when SRAM parity error occur)
3	U0PERSTEN	read-write	Enable USIC0 SRAM Parity Error Reset value1 = #0 (No reset when USIC0 memory parity error occur) value2 = #1 (Reset when USIC0 memory parity error occur)
4	U1PERSTEN	read-write	Enable USIC01 SRAM Parity Error Reset value1 = #0 (No reset when USIC1 memory parity error occur) value2 = #1 (Reset when USIC1 memory parity error occur)
5	MPERSTEN	read-write	Enable MultiCAN+SRAM Parity Error Reset value1 = #0 (No reset when MultiCAN+ memory parity error occur) value2 = #1 (Reset when MultiCAN+ memory parity error occur)
6	LOECRSTEN	read-write	Enable Loss of External Clock Reset value1 = #0 (No reset when loss of external clock occur) value2 = #1 (Reset when loss of external clock occur)
16	MRSTEN	write-only	Enable Master Reset value1 = #0 (No effect) value2 = #1 (Triggered Master reset)
17-31, 7-15	0	read	Reserved

23 Universal Serial Interface Channel Registers

Universal Serial Interface Controller 0

23.1 Register overview

Instance	Base address
USIC0	0x48000008
USIC1	0x48004008
USIC0_CH0	0x48000000
USIC0_CH1	0x48000200
USIC1_CH0	0x48004000
USIC1_CH1	0x48004200

Register name	Offset	Reset	Description
ID	0x00	0x00AAC000	Module Identification Register

23.2 Register details

23.2.1 ID

Module Identification Register

Reset	0x00AAC000
Width	32

Bit-field table (31 … 16)

MOD_NUMBER [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

MOD_TYPE [15:8]								MOD_REV [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	MOD_REV	read-only	Module Revision Number
15:8	MOD_TYPE	read-only	Module Type
31:16	MOD_NUMBER	read-only	Module Number Value

24 Versatile Analog-to-Digital Converter Registers

Analog to Digital Converter

24.1 Register overview

Instance	Base address
VADC	0x48030000
VADC_G0	0x48030400
VADC_G1	0x48030800

Register name	Offset	Reset	Description
CLC	0x00	0x00000003	Clock Control Register
ID	0x08	0x00C5C000	Module Identification Register
OCS	0x28	0x00000000	OCDS Control and Status Register
GLOBCFG	0x80	0x0000000F	Global Configuration Register
ACCPROT0	0x88	0x00000000	Access Protection Register
ACCPROT1	0x8C	0x00000000	Access Protection Register
GLOBICLASS[%s]	0xA0	0x00000000	Input Class Register, Global
GLOBBOUND	0xB8	0x00000000	Global Boundary Select Register
GLOBEFLAG	0xE0	0x00000000	Global Event Flag Register
GLOBEVNP	0x140	0x00000000	Global Event Node Pointer Register
BRSSEL[%s]	0x180	0x00000000	Background Request Source Channel Select Register
BRSPND[%s]	0x1C0	0x00000000	Background Request Source Pending Register
BRSCTRL	0x200	0x00000000	Background Request Source Control Register
BRSMR	0x204	0x00000000	Background Request Source Mode Register
GLOBRCR	0x280	0x00000000	Global Result Control Register
GLOBRES	0x300	0x00000000	Global Result Register
GLOBRESD	0x380	0x00000000	Global Result Register, Debug
EMUXSEL	0x3F0	0x00000000	External Multiplexer Select Register

24.2 Register details

24.2.1 CLC

Clock Control Register

Reset	0x00000003
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0												EDIS [3]	0	DISS [1]	DISR [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	DISR	read-write	Module Disable Request Bit value1 = #0 (On request: enable the module clock) value2 = #1 (Off request: stop the module clock)
1	DISS	read-only	Module Disable Status Bit value1 = #0 (Module clock is enabled) value2 = #1 (Off: module is not clocked)
3	EDIS	read-write	Sleep Mode Enable Control value1 = #0 (Sleep mode request is enabled and functional) value2 = #1 (Module disregards the sleep mode control signal)
4-31, 2	0	read	Reserved

24.2.2 ID

Module Identification Register

Reset	0x00C5C000
Width	32

Bit-field table (31 … 16)

MOD_NUMBER [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

MOD_TYPE [15:8]								MOD_REV [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	MOD_REV	read-only	Module Revision
15:8	MOD_TYPE	read-only	Module Type
31:16	MOD_NUMBER	read-only	Module Number

24.2.3 OCS

OCDS Control and Status Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0		SUSSTA [29]	SUS_P [28]	SUS [27:24]				0							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0												TG_P [3]	TGB [2]	TGS [1:0]	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
1:0	TGS	read-write	Trigger Set for OTGB0/1 value1 = #00 (No Trigger Set output) value2 = #01 (Trigger Set 1: TS16_SSIG, input sample signals)
2	TGB	read-write	OTGB0/1 Bus Select value1 = #0 (Trigger Set is output on OTGB0) value2 = #1 (Trigger Set is output on OTGB1)
3	TG_P	write-only	TGS, TGB Write Protection
27:24	SUS	read-write	OCDS Suspend Control value1 = #0000 (Will not suspend) value2 = #0001 (Hard suspend: Clock is switched off immediately.) value3 = #0010 (Soft suspend mode 0: Stop conversions after the currently running one is completed and its result has been stored. No change for the arbiter.) value4 = #0011 (Soft suspend mode 1: Stop conversions after the currently running one is completed and its result has been stored. Stop arbiter after the current arbitration round.)
28	SUS_P	write-only	SUS Write Protection
29	SUSSTA	read-only	Suspend State value1 = #0 (Module is not (yet) suspended) value2 = #1 (Module is suspended)
30-31, 4-23	0	read	Reserved

24.2.4 GLOBCFG

Global Configuration Register

Reset 0x0000000F

Width 32

Bit-field table (31 … 16)

SUCAL [31]	0														DPCAL1 [17]	DPCAL0 [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	

Bit-field table (15 … 0)

DIVWC [15]	0					DIVD [9:8]		DCMSB [7]	0		DIVA [4:0]					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Bit-fields

Bits	Field	Access	Description
4:0	DIVA	read-write	Divider Factor for the Analog Internal Clock value1 = 0x00 (fADCI = fADC / 2) value2 = 0x01 (fADCI = fADC / 2) value3 = 0x02 (fADCI = fADC / 3) value4 = 0x1F (fADCI = fADC / 32)
7	DCMSB	read-write	Double Clock for the MSB Conversion value1 = #0 (1 clock cycle for the MSB (standard)) value2 = #1 (2 clock cycles for the MSB (fADCI > 20 MHz))
9:8	DIVD	read-write	Divider Factor for the Arbiter Clock value1 = #00 (fADCD = fADC) value2 = #01 (fADCD = fADC / 2) value3 = #10 (fADCD = fADC / 3) value4 = #11 (fADCD = fADC / 4)
15	DIVWC	write-only	Write Control for Divider Parameters value1 = #0 (No write access to divider parameters) value2 = #1 (Bitfields DIVA, DCMSB, DIVD can be written)
16	DPCAL0	read-write	Disable Post-Calibration value1 = #0 (Automatic post-calibration after each conversion of group x) value2 = #1 (No post-calibration)
17	DPCAL1	read-write	Disable Post-Calibration value1 = #0 (Automatic post-calibration after each conversion of group x) value2 = #1 (No post-calibration)
31	SUCAL	write-only	Start-Up Calibration value1 = #0 (No action) value2 = #1 (Initiate the start-up calibration phase (indication in bit GxARBCFG.CAL))
18-30, 10-14, 5-6		read	Reserved

24.2.5 ACCPROT0

Access Protection Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

APGC [31]	0														API1 [17]	API0 [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	

Bit-field table (15 … 0)

APEM [15]	0														APC1 [1]	APC0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Bit-fields

Bits	Field	Access	Description
0	APC0	read-write	Access Protection Channel Control, Group 0 - 1 value1 = #0 (Full access to registers) value2 = #1 (Write access to channel control registers is blocked)
1	APC1	read-write	Access Protection Channel Control, Group 0 - 1 value1 = #0 (Full access to registers) value2 = #1 (Write access to channel control registers is blocked)
15	APEM	read-write	Access Protection External Multiplexer value1 = #0 (Full access to registers) value2 = #1 (Write access to external multiplexer registers is blocked)
16	API0	read-write	Access Protection Initialization, Group 0 - 1 value1 = #0 (Full access to registers) value2 = #1 (Write access to initialization registers is blocked)
17	API1	read-write	Access Protection Initialization, Group 0 - 1 value1 = #0 (Full access to registers) value2 = #1 (Write access to initialization registers is blocked)
31	APGC	read-write	Access Protection Global Configuration value1 = #0 (Full access to register) value2 = #1 (Write access to global configuration register is blocked)
18-30, 2-14	0	read	Reserved

24.2.6 ACCPROT1

Access Protection Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0														APR1 [17]	APR0 [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

APTF [15]	0													APS1 [1]	APS0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	APS0	read-write	Access Protection Service Request, Group 0 - 1 value1 = #0 (Full access to registers) value2 = #1 (Write access to service request registers is blocked)
1	APS1	read-write	Access Protection Service Request, Group 0 - 1 value1 = #0 (Full access to registers) value2 = #1 (Write access to service request registers is blocked)
15	APTF	read-write	Access Protection Test Function value1 = #0 (Full access to register) value2 = #1 (Write access to test function register is blocked)
16	APR0	read-write	Access Protection Result Registers, Group 0 - 1 value1 = #0 (Full access to registers) value2 = #1 (Write access to result registers is blocked)
17	APR1	read-write	Access Protection Result Registers, Group 0 - 1 value1 = #0 (Full access to registers) value2 = #1 (Write access to result registers is blocked)
18-31, 2-14	0	read	Reserved

24.2.7 GLOBICLASS[%s]

Input Class Register, Global

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0					CME [26:24]			0			STCE [20:16]				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0					CMS [10:8]			0			STCS [4:0]				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
4:0	STCS	read-write	Sample Time Control for Standard Conversions
10:8	CMS	read-write	Conversion Mode for Standard Conversions value1 = #000 (12-bit conversion) value2 = #001 (10-bit conversion) value3 = #010 (8-bit conversion) value6 = #101 (10-bit fast compare mode)
20:16	STCE	read-write	Sample Time Control for EMUX Conversions
26:24	CME	read-write	Conversion Mode for EMUX Conversions value1 = #000 (12-bit conversion) value2 = #001 (10-bit conversion) value3 = #010 (8-bit conversion) value6 = #101 (10-bit fast compare mode)
27-31, 21-23	11-15, 5-7	read	Reserved

24.2.8 GLOBBOUND

Global Boundary Select Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0				BOUNDARY1 [27:16]											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0				BOUNDARY0 [11:0]											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
11:0	BOUNDARY0	read-write	Boundary Value 0 for Limit Checking
27:16	BOUNDARY1	read-write	Boundary Value 1 for Limit Checking
28-31, 12-15	0	read	Reserved

24.2.9 GLOBEFLAG

Global Event Flag Register

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

0							REVG LBCLR [24]	0							SEVG LBCLR [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0							REVG LB [8]	0							SEVG LB [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	SEVGLB	read-write	Source Event (Background) value1 = #0 (No source event) value2 = #1 (A source event has occurred)
8	REVGLB	read-write	Global Result Event value1 = #0 (No result event) value2 = #1 (New result was stored in register GLOBRES)
16	SEVGLBCLR	write-only	Clear Source Event (Background) value1 = #0 (No action) value2 = #1 (Clear the source event flag SEVGLB)
24	REVGLBCLR	write-only	Clear Global Result Event value1 = #0 (No action) value2 = #1 (Clear the result event flag REVGLB)
25-31, 17-23, 9-15, 1-7		read	Reserved

24.2.10 GLOBEVNP

Global Event Node Pointer Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0												REV0NP [19:16]			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0												SEV0NP [3:0]			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
3:0	SEV0NP	read-write	Service Request Node Pointer Backgr. Source value1 = #0000 (Select shared service request line 0 of common service request group 0) value2 = #0011 (Select shared service request line 3 of common service request group 0)
19:16	REV0NP	read-write	Service Request Node Pointer Global Result value1 = #0000 (Select shared service request line 0 of common service request group 0) value2 = #0011 (Select shared service request line 3 of common service request group 0)
20-31, 4-15	0	read	Reserved

24.2.11 BRSSEL[%s]

Background Request Source Channel Select Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0								CHSELG7 [7]	CHSELG6 [6]	CHSELG5 [5]	CHSELG4 [4]	CHSELG3 [3]	CHSELG2 [2]	CHSELG1 [1]	CHSELG0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	CHSELG0	read-write	Channel Selection Group x value1 = #0 (Ignore this channel) value2 = #1 (This channel is part of the scan sequence)
1	CHSELG1	read-write	Channel Selection Group x value1 = #0 (Ignore this channel) value2 = #1 (This channel is part of the scan sequence)
2	CHSELG2	read-write	Channel Selection Group x value1 = #0 (Ignore this channel) value2 = #1 (This channel is part of the scan sequence)
3	CHSELG3	read-write	Channel Selection Group x value1 = #0 (Ignore this channel) value2 = #1 (This channel is part of the scan sequence)
4	CHSELG4	read-write	Channel Selection Group x value1 = #0 (Ignore this channel) value2 = #1 (This channel is part of the scan sequence)
5	CHSELG5	read-write	Channel Selection Group x value1 = #0 (Ignore this channel) value2 = #1 (This channel is part of the scan sequence)
6	CHSELG6	read-write	Channel Selection Group x value1 = #0 (Ignore this channel) value2 = #1 (This channel is part of the scan sequence)
7	CHSELG7	read-write	Channel Selection Group x value1 = #0 (Ignore this channel) value2 = #1 (This channel is part of the scan sequence)
8-31	0	read	Reserved

24.2.12 BRSPND[%s]

Background Request Source Pending Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0								CHPN DG7 [7]	CHPN DG6 [6]	CHPN DG5 [5]	CHPN DG4 [4]	CHPN DG3 [3]	CHPN DG2 [2]	CHPN DG1 [1]	CHPN DG0 [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	CHPNDG0	read-write	Channels Pending Group x value1 = #0 (Ignore this channel) value2 = #1 (Request conversion of this channel)
1	CHPNDG1	read-write	Channels Pending Group x value1 = #0 (Ignore this channel) value2 = #1 (Request conversion of this channel)
2	CHPNDG2	read-write	Channels Pending Group x value1 = #0 (Ignore this channel) value2 = #1 (Request conversion of this channel)
3	CHPNDG3	read-write	Channels Pending Group x value1 = #0 (Ignore this channel) value2 = #1 (Request conversion of this channel)
4	CHPNDG4	read-write	Channels Pending Group x value1 = #0 (Ignore this channel) value2 = #1 (Request conversion of this channel)
5	CHPNDG5	read-write	Channels Pending Group x value1 = #0 (Ignore this channel) value2 = #1 (Request conversion of this channel)
6	CHPNDG6	read-write	Channels Pending Group x value1 = #0 (Ignore this channel) value2 = #1 (Request conversion of this channel)
7	CHPNDG7	read-write	Channels Pending Group x value1 = #0 (Ignore this channel) value2 = #1 (Request conversion of this channel)
8-31	0	read	Reserved

24.2.13 BRSCTRL

Background Request Source Control Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0								GTWC [23]	0		GTLVL [20]	GTSEL [19:16]			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

XTWC [15]	XTMODE [14:13]		XTLVL [12]	XTSEL [11:8]				0				SRCRESREG [3:0]			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
3:0	SRCRESREG	read-write	Source-specific Result Register value1 = #0000 (Use GxCHCTRy.RESREG to select a group result register) value2 = #0001 (Store result in group result register GxRES1) value3 = #1111 (Store result in group result register GxRES15)
11:8	XTSEL	read-write	External Trigger Input Selection
12	XTLVL	read-only	External Trigger Level
14:13	XTMODE	read-write	Trigger Operating Mode value1 = #00 (No external trigger) value2 = #01 (Trigger event upon a falling edge) value3 = #10 (Trigger event upon a rising edge) value4 = #11 (Trigger event upon any edge)
15	XTWC	write-only	Write Control for Trigger Configuration value1 = #0 (No write access to trigger configuration) value2 = #1 (Bitfields XTMODE and XTSEL can be written)
19:16	GTSEL	read-write	Gate Input Selection
20	GTLVL	read-only	Gate Input Level
23	GTWC	write-only	Write Control for Gate Configuration value1 = #0 (No write access to gate configuration) value2 = #1 (Bitfield GTSEL can be written)
24-31, 21-22	04-7	read	Reserved

24.2.14 BRSMR

Background Request Source Mode Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															RPTDIS [16]
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0						LDEV [9]	CLRPND [8]	REQGT [7]	0	LDM [5]	SCAN [4]	ENSI [3]	ENTR [2]	ENGT [1:0]	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
1:0	ENGT	read-write	Enable Gate value1 = #00 (No conversion requests are issued) value2 = #01 (Conversion requests are issued if at least one pending bit is set) value3 = #10 (Conversion requests are issued if at least one pending bit is set and REQGTx = 1.) value4 = #11 (Conversion requests are issued if at least one pending bit is set and REQGTx = 0.)
2	ENTR	read-write	Enable External Trigger value1 = #0 (External trigger disabled) value2 = #1 (The selected edge at the selected trigger input signal REQTR generates the load event)
3	ENSI	read-write	Enable Source Interrupt value1 = #0 (No request source interrupt) value2 = #1 (A request source interrupt is generated upon a request source event (last pending conversion is finished))
4	SCAN	read-write	Autoscan Enable value1 = #0 (No autoscan) value2 = #1 (Autoscan functionality enabled: a request source event automatically generates a load event)
5	LDM	read-write	Autoscan Source Load Event Mode value1 = #0 (Overwrite mode: Copy all bits from the select registers to the pending registers upon a load event) value2 = #1 (Combine mode: Set all pending bits that are set in the select registers upon a load event (logic OR))
7	REQGT	read-only	Request Gate Level value1 = #0 (The gate input is low) value2 = #1 (The gate input is high)
8	CLRPND	write-only	Clear Pending Bits value1 = #0 (No action) value2 = #1 (The bits in registers BRSPNDx are cleared)
9	LDEV	write-only	Generate Load Event value1 = #0 (No action) value2 = #1 (A load event is generated)
16	RPTDIS	read-write	Repeat Disable value1 = #0 (A cancelled conversion is repeated) value2 = #1 (A cancelled conversion is discarded)
17-31, 10-15	06	read	Reserved

24.2.15 GLOBRCR

Global Result Control Register

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

SRGEN [31]	0						WFR [24]	0				DRCTR [19:16]			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
19:16	DRCTR	read-write	Data Reduction Control value1 = #0000 (Data reduction disabled)
24	WFR	read-write	Wait-for-Read Mode Enable value1 = #0 (Overwrite mode) value2 = #1 (Wait-for-read mode enabled for this register)
31	SRGEN	read-write	Service Request Generation Enable value1 = #0 (No service request) value2 = #1 (Service request after a result event)
25-30, 20-23, 00-15		read	Reserved

24.2.16 GLOBRES

Global Result Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

VF [31]	FCR [30]	CRS [29:28]		EMUX [27:25]			CHNR [24:20]					GNR [19:16]			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

RESULT [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
15:0	RESULT	read-write	Result of most recent conversion
19:16	GNR	read-only	Group Number
24:20	CHNR	read-only	Channel Number
27:25	EMUX	read-only	External Multiplexer Setting
29:28	CRS	read-only	Converted Request Source
30	FCR	read-only	Fast Compare Result value1 = #0 (Signal level was below compare value) value2 = #1 (Signal level was above compare value)
31	VF	read-write	Valid Flag value1 = #0 (Read access: No new valid data available Write access: No effect) value2 = #1 (Read access: Bitfield RESULT contains valid data and has not yet been read, or bit FCR has been updated Write access: Clear this valid flag and the data reduction counter (overrides a hardware set action))

24.2.17 GLOBRESD

Global Result Register, Debug

Reset 0x00000000

Width 32

Bit-field table (31 … 16)

VF [31]	FCR [30]	CRS [29:28]		EMUX [27:25]			CHNR [24:20]					GNR [19:16]			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

RESULT [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
15:0	RESULT	read-write	Result of most recent conversion
19:16	GNR	read-only	Group Number
24:20	CHNR	read-only	Channel Number
27:25	EMUX	read-only	External Multiplexer Setting
29:28	CRS	read-only	Converted Request Source
30	FCR	read-only	Fast Compare Result value1 = #0 (Signal level was below compare value) value2 = #1 (Signal level was above compare value)
31	VF	read-write	Valid Flag value1 = #0 (Read access: No new valid data available Write access: No effect) value2 = #1 (Read access: Bitfield RESULT contains valid data and has not yet been read, or bit FCR has been updated Write access: Clear this valid flag and the data reduction counter (overrides a hardware set action))

24.2.18 EMUXSEL

External Multiplexer Select Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0								EMUXGRP1 [7:4]				EMUXGRP0 [3:0]			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
3:0	EMUXGRP0	read-write	External Multiplexer Group for Interface x
7:4	EMUXGRP1	read-write	External Multiplexer Group for Interface x
8-31	0	read	Reserved

25 Watch Dog Timer Registers

Watch Dog Timer

25.1 Register overview

Instance	Base address
WDT	0x40020000

Register name	Offset	Reset	Description
ID	0x00	0x00ADC000	WDT Module ID Register
CTR	0x04	0x00000000	WDT Control Register
SRV	0x08	0x00000000	WDT Service Register
TIM	0x0C	0x00000000	WDT Timer Register
WLB	0x10	0x00000000	WDT Window Lower Bound Register
WUB	0x14	0xFFFFFFFF	WDT Window Upper Bound Register
WDTSTS	0x18	0x00000000	WDT Status Register
WDTCLR	0x1C	0x00000000	WDT Clear Register

25.2 Register details

25.2.1 ID

WDT Module ID Register

Reset	0x00ADC000
Width	32

Bit-field table (31 … 16)

MOD_NUMBER [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

MOD_TYPE [15:8]								MOD_REV [7:0]							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
7:0	MOD_REV	read-only	Module Revision Number
15:8	MOD_TYPE	read-only	Module Type
31:16	MOD_NUMBER	read-only	Module Number Value

25.2.2 CTR

WDT Control Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

SPW [15:8]								0			DSP [4]	0		PRE [1]	ENB [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	ENB	read-write	Enable
1	PRE	read-write	Pre-warning
4	DSP	read-write	Debug Suspend
15:8	SPW	read-write	Service Indication Pulse Width
16-31, 5-7, 2[illegible]3		read	Reserved

25.2.3 SRV

WDT Service Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

SRV [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

SRV [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:0	SRV	write-only	Service

25.2.4 TIM

WDT Timer Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

TIM [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

TIM [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:0	TIM	read-only	Timer Value

25.2.5 WLB

WDT Window Lower Bound Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

WLB [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

WLB [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:0	WLB	read-write	Window Lower Bound

25.2.6 WUB

WDT Window Upper Bound Register

Reset	0xFFFFFFFF
Width	32

Bit-field table (31 … 16)

WUB [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

WUB [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
31:0	WUB	read-write	Window Upper Bound

25.2.7 WDTSTS

WDT Status Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0															ALMS [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	ALMS	read-only	Pre-warning Alarm
1-31	0	read	Reserved

25.2.8 WDTCLR

WDT Clear Register

Reset	0x00000000
Width	32

Bit-field table (31 … 16)

0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit-field table (15 … 0)

0															ALMC [0]
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit-fields

Bits	Field	Access	Description
0	ALMC	write-only	Pre-warning Alarm
1-31	0	read	Reserved

References

Datasheet

[1] Infineon Technologies AG: *002-42736 – PSOC™ Control C1 - PSC1M1x; Available online*

Architecture reference manual

[2] Infineon Technologies AG: *002-42735 – PSOC™ Control C1 architecture reference manual;* Available online

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