SupIRBuck™

HIGHLY INTEGRATED 10A SINGLE-INPUT VOLTAGE, SYNCHRONOUS BUCK REGULATOR

Features

- Greater than 96% Maximum Efficiency
- Single 16V Application
- Single 5V Application
- Wide Output Voltage Range: 0.6V to 0.9*Vin
- Continuous 10A Load Capability
- Programmable Switching Frequency up to 1.5MHz
- Internal Digital Soft-Start
- Enable Input with Voltage Monitoring Capability
- Hiccup Mode Over Current Protection
- Internal LDO
- External Synchronization
- Enhanced PreBias Start up
- External Reference for Margining Purposes
- Input for Tracking Applications
- Integrated MOSFET Drivers and Bootstrap Diode
- Operating Junction Temp: -40°C <Tj<125°C
- Thermal Shut Down
- Power Good Output with tracking capability
- Over Voltage Detection Feature
- Pin Compatible with 6A and 14A Versions
- Small Size 5mmx6mm PQFN, 0.9 mm Height
- Lead-free, Halogen-free and RoHS Compliant

Applications

- Netcom and Telecom Applications
- Data Center Applications
- Distributed Point of Load Power Architectures

Description

The IR3838 ***SupIRBuck™*** is an easy-to-use, fully integrated and highly efficient DC/DC regulator. The onboard PWM controller and MOSFETs make IR3838 a space-efficient solution, providing accurate power delivery for low output voltage applications.

IR3838 is a versatile regulator which offers programmability of switching frequency and current limit while operates in wide input and output voltage range.

The switching frequency is programmable from 250kHz to 1.5MHz for an optimum solution.

It also features important protection functions, such as Pre-Bias startup, hiccup current limit and thermal shutdown to give required system level security in the event of fault conditions.

IR3838 offers margining capability through Vref pin. During the margining operation, PGood tracks Vref via feedback to ensure correct status of the output voltage.

The internal LDO enables the device to operate from a single supply. This internal LDO can be bypassed when an external bias voltage is available.

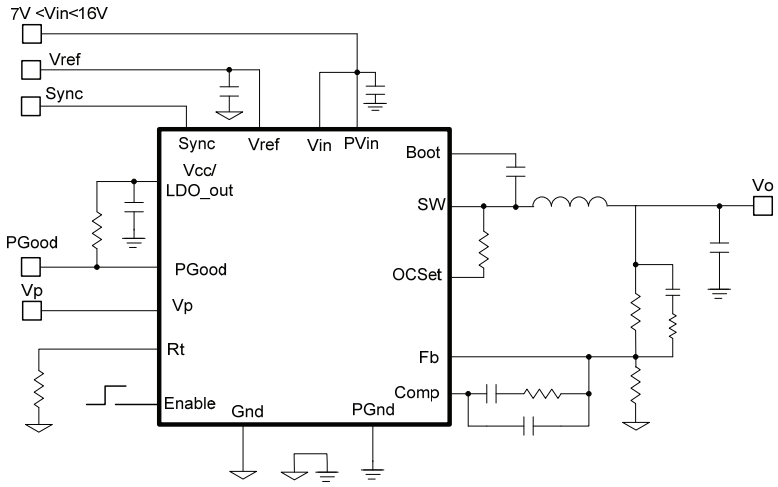


Fig. 1. Typical application diagram

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND unless otherwise specified)

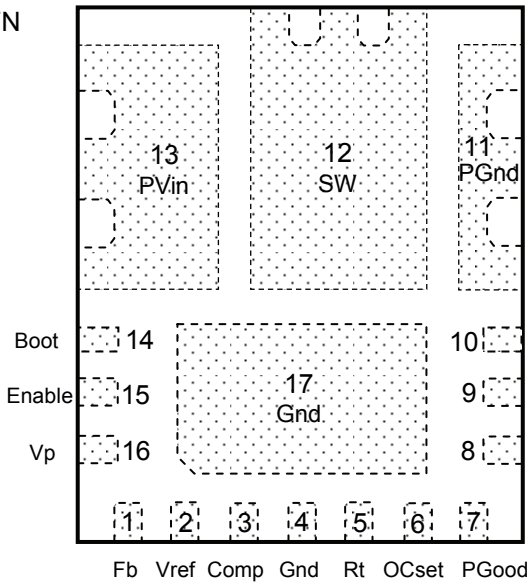
- PVin, Vin ..... -0.3V to 25V
- Vcc/LDO_out ..... -0.3V to 8V *(Note2)*
- Boot ..... -0.3V to 33V
- SW ..... -0.3V to 25V (DC), -4V to 25V (AC, 100ns)
- Boot to SW ..... -0.3V to Vcc+0.3V *(Note1)*
- OCset ..... -0.3V to 30V
- Input / output Pins ..... -0.3V to Vcc+0.3V *(Note1)*
- PGnd to Gnd ..... -0.3V to +0.3V
- Storage Temperature Range ..... -55°C To 150°C
- Junction Temperature Range ..... -40°C To 150°C *(Note2)*
- ESD Classification ..... JEDEC(2KV)
- Moisture sensitivity level..... JEDEC Level 2 @260 °C (*Note 5*)

Note1: *Must not exceed 8V*
Note2: *Vcc must not exceed 7.5V for Junction Temperature between -10°C and -40°C*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

Package Information

5mm x 6mm Power QFN
(Top View)



$\theta_{JA} = 35°C / W$

$\theta_{J\text{-}PCB} = 2°C / W$

ORDERING INFORMATION

PACKAGE DESIGNATOR	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER REEL
M	IR3838MTRPbF	17	4000
M	IR3838MTR1PbF	17	750

Block Diagram

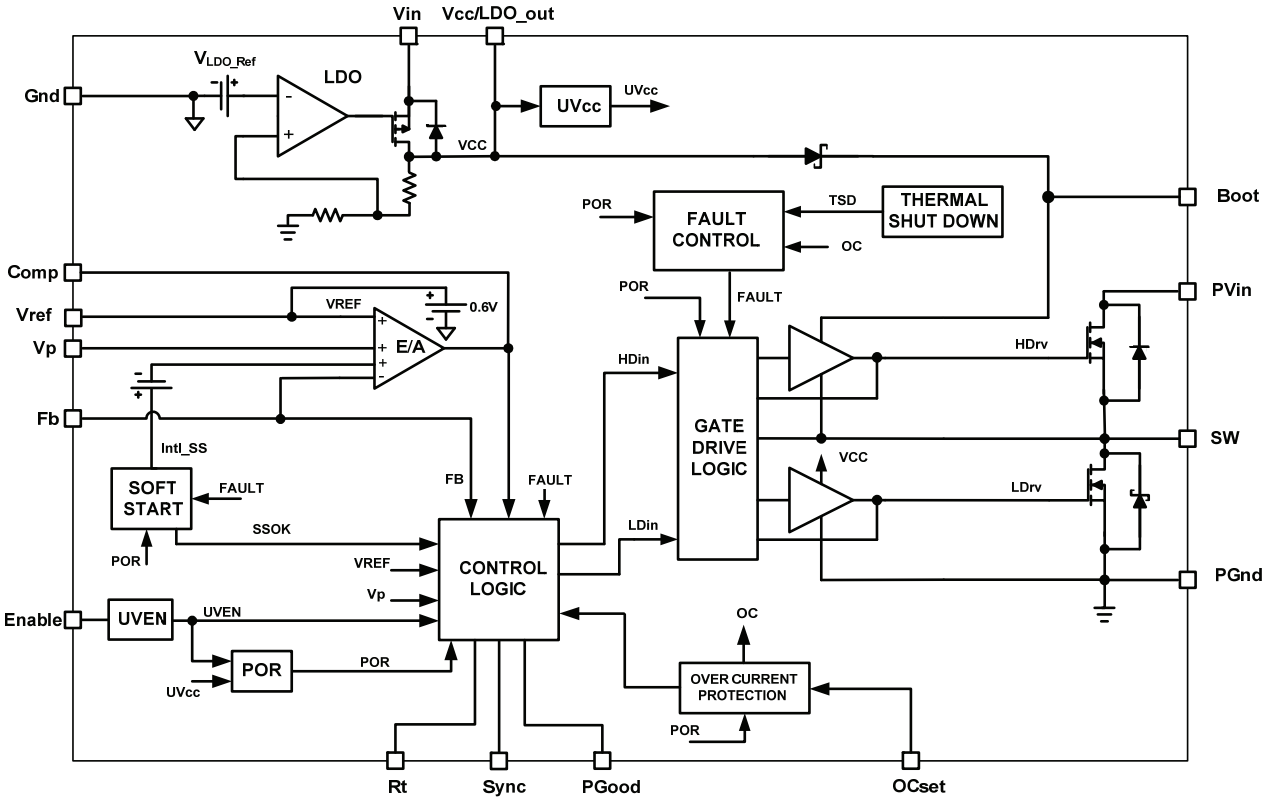


Fig. 2. Simplified block diagram of the IR3838

Pin Description

Pin	Name	Description
1	Fb	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator via resistor divider to set the output voltage and provide feedback to the error amplifier
2	Vref	External reference voltage, can be used for margining operation. A 100nF capacitor should be connected between this pin and Gnd.
3	Comp	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to Fb to provide loop compensation
4	Gnd	Signal ground for internal reference and control circuitry
5	Rt	Use an external resistor from this pin to Gnd to set the switching frequency
6	OCset	Current limit set point. A resistor from this pin to SW pin will set the current limit threshold
7	PGood	Power Good status pin. Output is open drain. Connect a pull up resistor from this pin to Vcc
8	Sync	External Synchronization, this pin is used to synchronize the device's switching with an external clock. It is recommended that the external Sync clock be set to 20% above the free-running frequency. If not used, this pin can be left floating.
9	Vin	Input voltage for Internal LDO. A 1.0µF capacitor should be connected between this pin and PGnd. If external supply is connected to Vcc/LDO_out pin, this pin should be left floating.
10	V_{CC} /LDO_out	Input Bias Voltage, output of internal LDO. Place a minimum 2.2µF cap from this pin to PGnd
11	PGnd	Power Ground. This pin serves as a separated ground for the MOSFET drivers and should be connected to the system's power ground plane.
12	SW	Switch node. This pin is connected to the output inductor
13	PVin	Input voltage for power stage
14	Boot	Supply voltage for high side driver, a 100nF capacitor should be connected between this pin and SW pin.
15	Enable	Enable pin to turn on and off the device, if this pin is connected to PVin pin through a resistor divider, input voltage UVLO can be implemented.
16	Vp	Input to error amplifier for tracking purposes
17	Gnd	Signal ground for internal reference and control circuitry

Recommended Operating Conditions

Symbol	Definition	Min	Max	Units
PVin	Input Voltage for power stage	1.5	16	V
Vin	Input Voltage for internal LDO *	7.0	16	
Vcc/LDO_out	Supply Voltage *	4.5	6.5	
Boot to SW	Supply Voltage	4.5	7.5	
V_o	Output Voltage	0.6	0.9*Vin	
I_o	Output Current	0	10	A
Fs	Switching Frequency	225	1650	kHz
T_j	Junction Temperature	-40	125	°C

* Vcc/LDO_out can be connected to an external regulated supply (≈ 5V). If so, the Vin input should be left unconnected.

Electrical Specifications

Unless otherwise specified, these specification apply over, 7.0V<V_{in}=PVin<16V, Vref=0.6V in 0°C<T_j< 125°C. Typical values are specified at T_a = 25°C.

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
POWER STAGE						
Power Losses	P_{loss}	V_{in}=12V, V_o=1.8V, I_o=10A, Fs=600kHz, L=0.6uH, *Note4*		2		W
Top Switch	$R_{ds(on)_Top}$	V_{Boot} -V_{sw} =5.0V, I_D=10A,Tj=25C		17.1	26	mΩ
Bottom Switch	$R_{ds(on)_Bot}$	V_{cc}=5.0V, I_D=10A		8.5	11	
Bootstrap Diode Forward Voltage		I(Boot)= 30mA	180	260	470	mV
SW leakage Current	Isw	SW=0V, Enable=0V			6	µA
		SW=0V, Enable=high, Vp=0V			14	
SUPPLY CURRENT						
V_{in} Supply Current (Standby)	$I_{in(Standby)}$	Enable low , No Switching,			400	µA
V_{in} Supply Current (Dyn)	$I_{in(Dyn)}$	Enable high, Fs=500kHz, Vin=12V		12		mA
INTERNAL REGULATOR (LDO)						
Output Voltage	IntVcc	Vin(min)=7.0V, Io=0-50mA, Cload=2.2uF	4.7	5.2	5.7	V
IntVcc Dropout	IntVcc_drop	Io=50mA, Cload=2.2uF		50	150	mV
Short Circuit Current	Ishort			70		mA
INTERNAL DIGITAL SOFT START						
Soft Start Clock Frequency	Clk(SS)	Note4	168	200	254	kHz
Soft Start Ramp Rate	Ramp(SS)			0.2		mV/us

Electrical Specifications (continued)

Unless otherwise specified, these specification apply over, 7.0V<V_{in}=PVin<16V, Vref=0.6V in 0°C<T_j< 125°C. Typical values are specified at T_a = 25°C.

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
Input Offset Voltage	Vos_Vp	Vfb-Vp, Vp=0.6V, Vref >2.0V	-1		+1	%
	Vos_Vref	Vfb-Vref, Vref=0.6V, Vp>2.0V	-1		1	
Input Bias Current	IFb(E/A)		-1		+1	µA
Input Bias Current	IVp(E/A)		-1		+1	µA
Sink Current	Isink(E/A)		0.40	0.85	1.2	mA
Source Current	Isource(E/A)		8	10	13	mA
Slew Rate	SR	*Note4*	7	12	20	V/µs
Gain-Bandwidth Product	GBWP	*Note4*	20	30	40	MHz
DC Gain	Gain	*Note4*	100	110	120	dB
Maximum Voltage	Vmax(E/A)		3.4	3.5	3.75	V
Minimum Voltage	Vmin(E/A)			150	220	mV
Common Mode Voltage			0		1.2	V
OSCILLATOR						
Rt Voltage			0.665	0.7	0.735	V
Frequency Range	F_S	Rt=59K	225	250	275	kHz
		Rt=28.7K	450	500	550	
		Rt=9.53K, Note4	1350	1500	1650	
Ramp Amplitude	Vramp	*Note4*		1.8		Vp-p
Ramp Offset	Ramp(os)	*Note4*		0.6		V
Min Pulse Width	Dmin(ctrl)	*Note4*			70	ns
Max Duty Cycle	Dmax	Fs=250kHz	91			%
Fixed Off Time		*Note4*			300	ns
Sync Frequency Range		20% above free running frequency	225		1650	kHz
Sync Pulse Duration			100	200		ns
Sync Level Threshold	Sync High		2			V
	Sync Low				0.6	
REFERENCE VOLTAGE						
Feedback Voltage	VFB	Vref pin floating, Vp=Vcc		0.6		V
Accuracy		0°C<Tj<125°C	-1.0		+1.0	%
		-40°C<Tj<125°C, Note3	-2.0		+2.0	
Vref margining voltage	Vref_marg		0.54		1.2	V
Sink Current	Isink_Vref	Vref=0.7V		19	25	µA
Source Current	Isource_Vref	Vref=0.5V		19	25	µA
Tracker Comparator Threshold	Tracker(upper)	Vref pulled up externally	1.35	1.5	1.6	V
	Tracker(lower)	Vref pulled up externally	1.05	1.2	1.3	
Tracker Comparator Hysteresis	Tracker_Hys	Vref pulled up externally	220	300	420	mV

Electrical Specifications (continued)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
FAULT PROTECTION						
OCSET Current	I_{OCSET}	Fs=250kHz	10.4	11.8	13.2	µA
		Fs=500kHz	21.5	24.4	27.3	
		Fs=1500kHz	68	77	86	
OC comp Offset Voltage	V_{OFFSET}	*Note4*	-6	0	+6	mV
SS off time	SS_Hiccup			4096		Cycles
Thermal Shutdown		*Note4*		140		°C
Thermal Hysteresis		*Note4*		20		
UNDER VOLTAGE LOCKOUT						
V_{CC}-Start-Threshold	V_{CC}_UVLO_Start	Vcc Rising Trip Level	4.06	4.26	4.46	V
V_{CC}-Stop-Threshold	V_{CC}_UVLO_Stop	Vcc Falling Trip Level	3.76	3.96	4.16	
Enable-Start-Threshold	Enable_UVLO_Start	Supply ramping up	1.14	1.2	1.36	V
Enable-Stop-Threshold	Enable_UVLO_Stop	Supply ramping down	0.75	0.85	0.95	
Enable leakage current	Ien	Enable=3.3V			10	µA
PGOOD						
Power Good upper Threshold	VPG(upper)	Fb Rising, Vref < 1.2V		115		%Vref
		Fb Rising, Vref > 1.5V		115		%Vp
Upper Threshold Delay	VPG(upper)_Dly	Fb Falling		256/Fs		s
Power Good lower Threshold	VPG(lower)	Fb Rising, Vref < 1.2V		85		%Vref
		Fb Rising, Vref > 1.5V		85		%Vp
Lower Threshold Delay	VPG(lower)_Dly	Fb Rising		256/Fs		s
Soft Start Delay Time	Tdelay(Delay)	Note4		10		ms
PGood Voltage Low	PG(voltage)	I_{Pgood}=-5mA			0.5	V
Tracker Comparator Upper Threshold	VPG(tracker_upper)	Vp Rising, Vref > 1.5V		0.5		V
Tracker Comparator Lower Threshold	VPG(tracker_lower)	Vp Falling, Vref > 1.5V		0.3		
Tracker Comparator Delay	Tdelay(tracker)	Vp Rising, Vref > 1.5V		256/Fs		s

***Note3*: Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.**

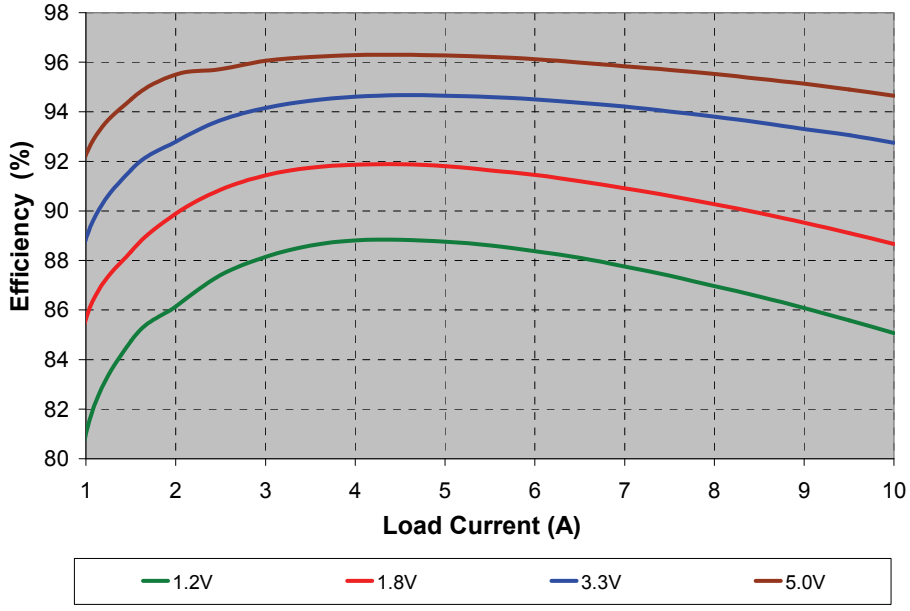
***Note4*: Guaranteed by design but not tested in production**

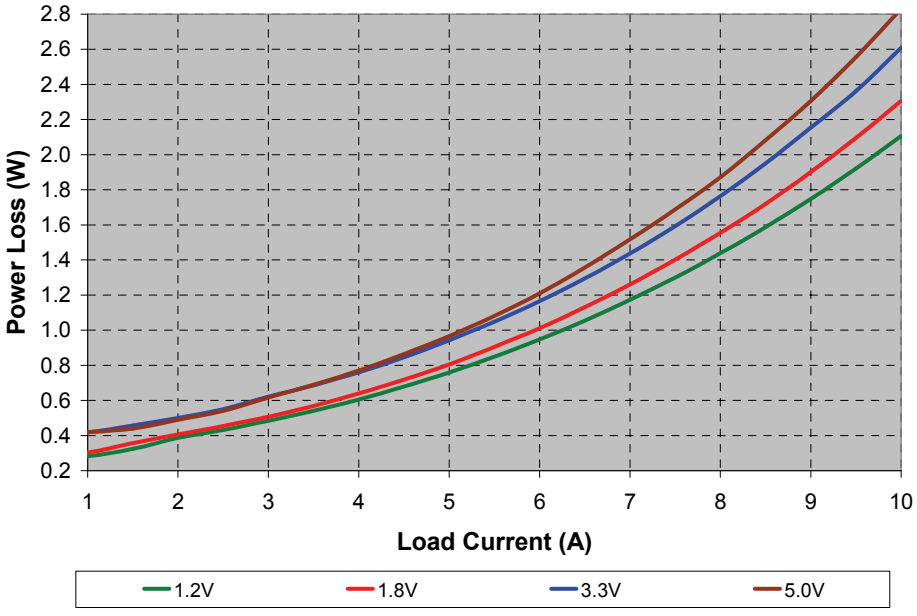
***Note5*: Upgrade to industrial/MSL2 level applies from date codes 1141 (marking explained on application note AN1132 page 2). Products with prior date code of 1141 are qualified with MSL3 for Consumer market.**

Typical Efficiency and Power Loss Curves
Vin=12V, Vcc=5V (external), Io=1A-10A, F_s=600kHz, Room Temperature, No Air Flow

The table below shows the inductors used for each of the output voltages in the efficiency measurement.

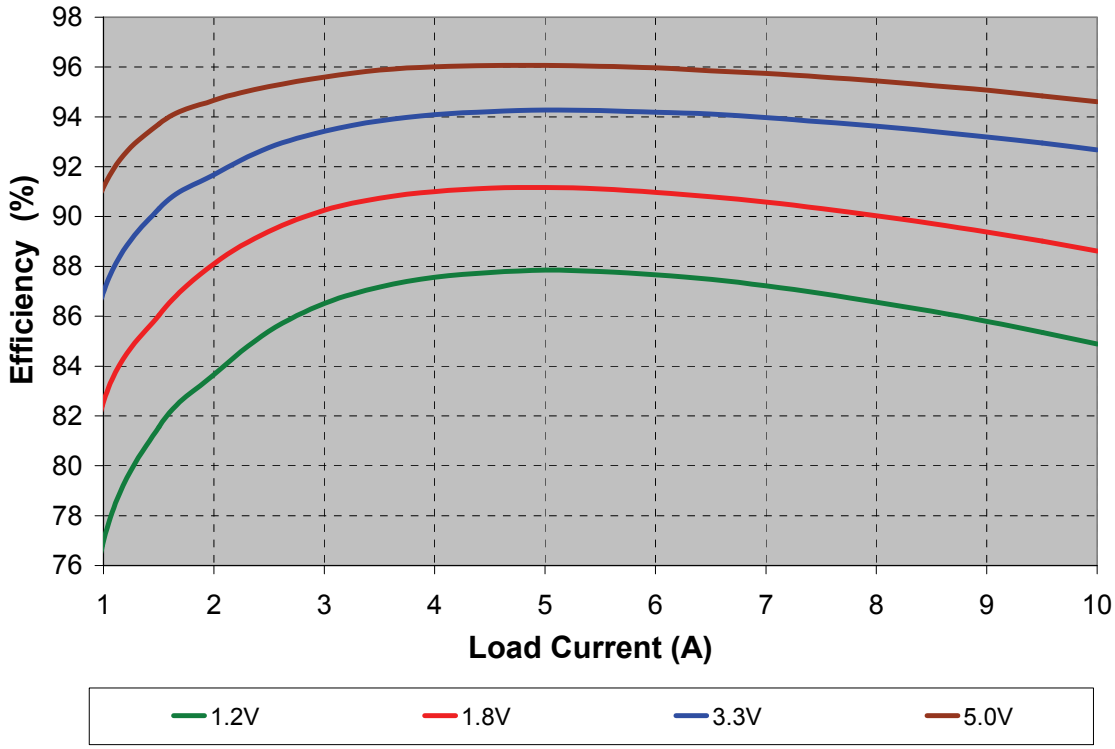
Vo [V]	L [µH]	MFR	P/N	DCR [mΩ]
1.2	0.51	Vitec	59PR9876N	0.29
1.8	0.72	Wurth Elek.	744 325 072	1.3
3.3	1.2	Wurth Elek.	744 325 120	1.8
5.0	1.2	Delta	MPL1055-1R2	2.9

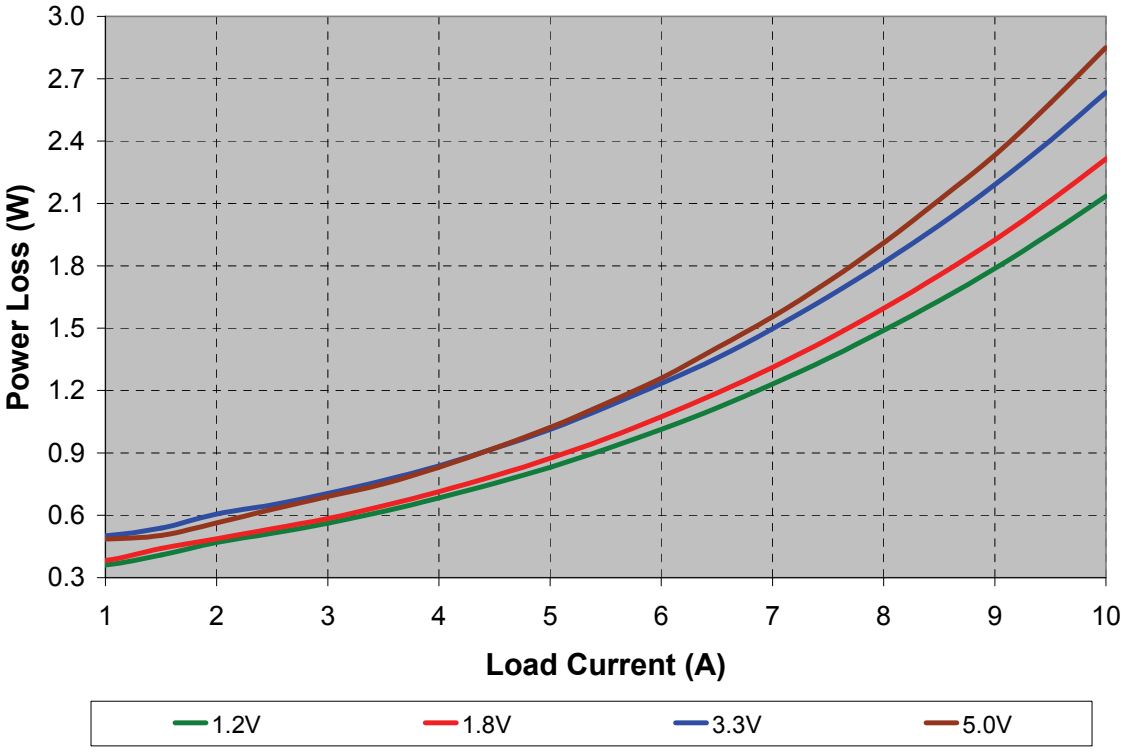




Typical Efficiency and Power Loss Curves
Vin=12V, Vcc/LDO_out=5.2V, Io=1A-10A, Fs=600kHz, Room Temperature, No Air Flow

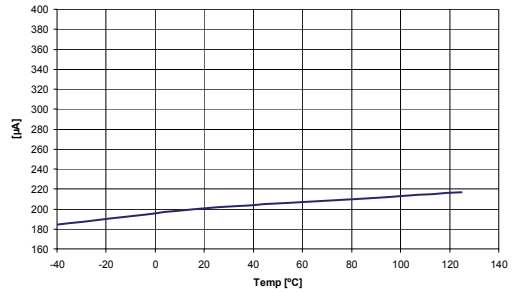
The same inductors as listed on the previous page have been used.



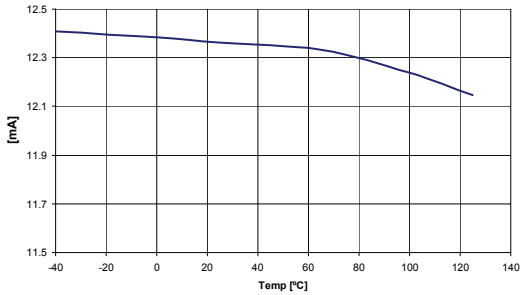


TYPICAL OPERATING CHARACTERISTICS (-40°C - 125°C), F_s=500 kHz

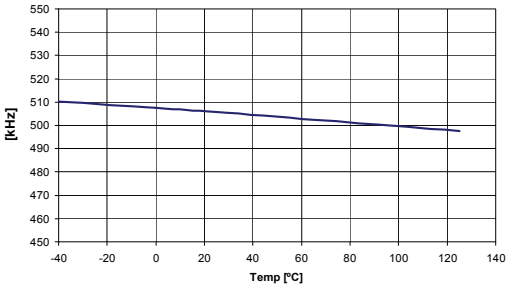
Iin(Standby)



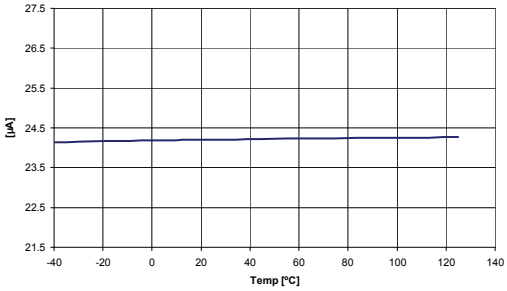
Iin(Dyn)



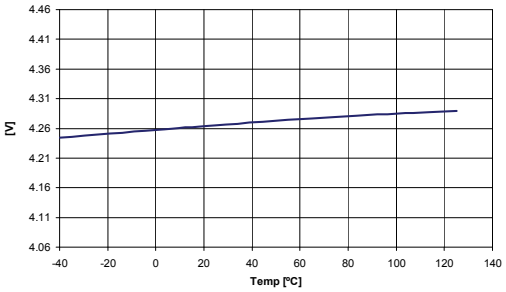
FREQUENCY



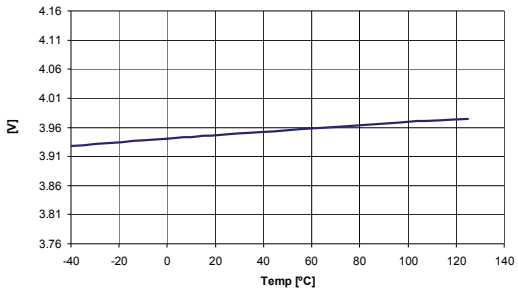
IOCSET(500kHz)



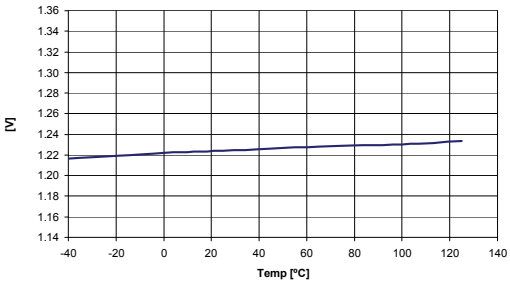
Vcc(UVLO) Start



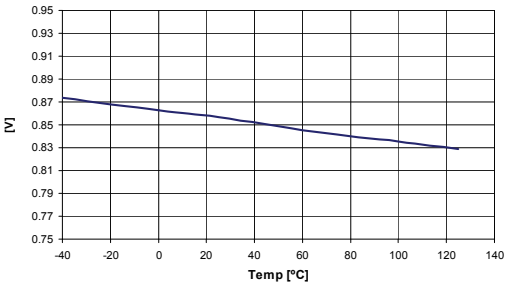
Vcc(UVLO) Stop



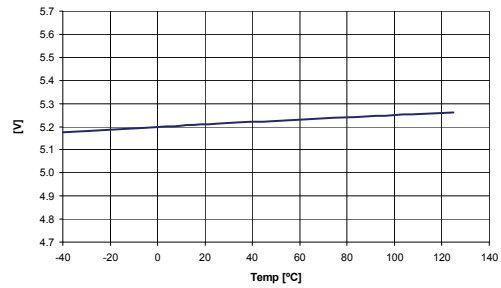
Enable(UVLO) Start



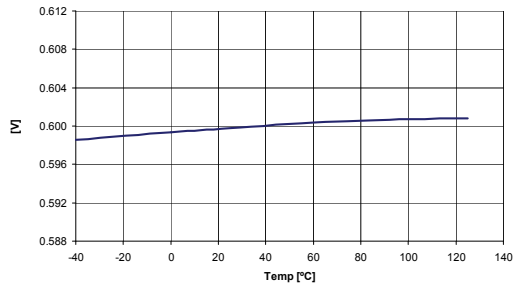
Enable(UVLO) Stop



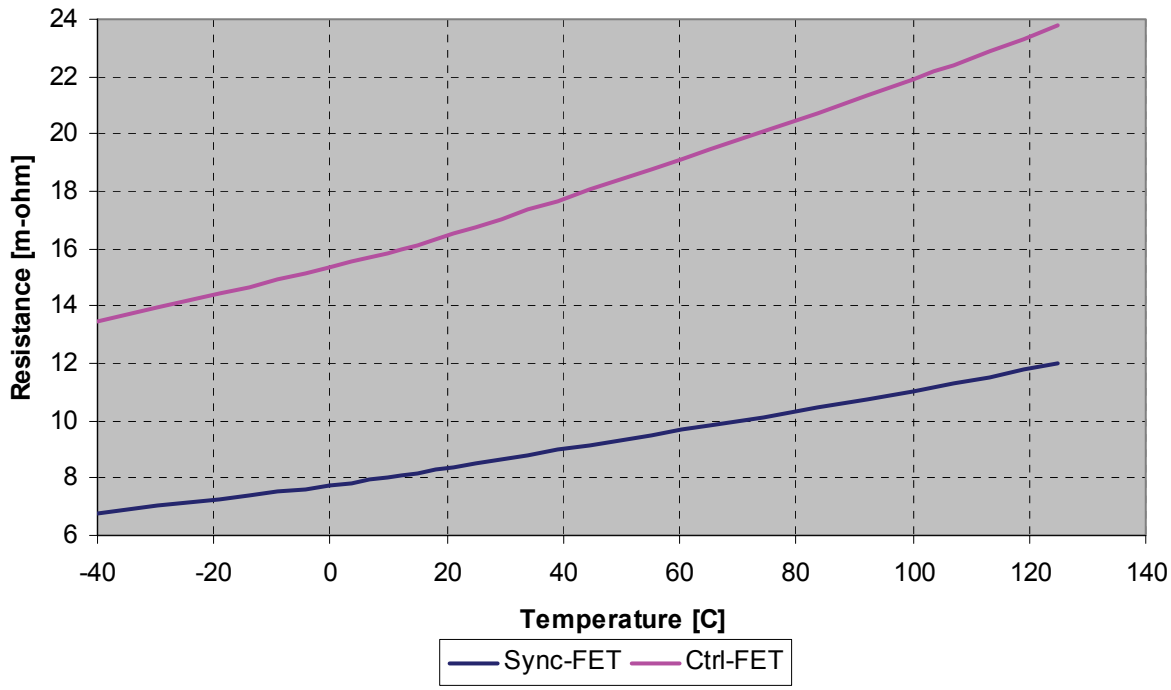
Vcc_LDO



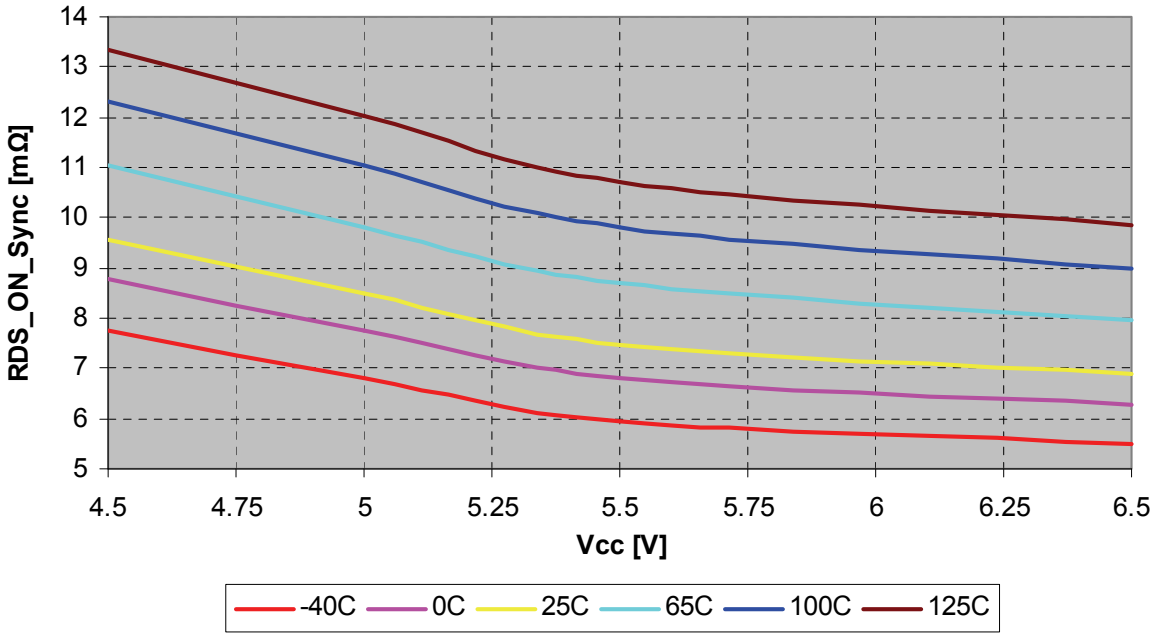
Vfb



Rdson of MOSFETs Over Temperature at Vcc=5V



Rdson of Sync-FET versus Vcc at different Temperatures



Circuit Description

THEORY OF OPERATION

Introduction

The IR3838 uses a PWM voltage mode control scheme with external compensation to provide good noise immunity and maximum flexibility in selecting inductor values and capacitor types.

The switching frequency is programmable from 250kHz to 1.5MHz and provides the capability of optimizing the design in terms of size and performance.

IR3838 provides precisely regulated output voltage programmed via two external resistors from 0.6V to 0.9*Vin.

The IR3838 operates with an internal bias supply voltage of 5.2V (LDO) which is connected to the Vcc/LDO_out pin. This allows operation with single supply. The IC can also be operated with an external supply from 4.5V to 6.5V, allowing an extended operating input voltage (PVin) range from 1.5V to 16V. For using the internal supply, the Vin pin should be connected to PVin pin. If an external supply is used, it should be connected to Vcc/LDO_out pin and the Vin pin should be left floating.

The device utilizes the on-resistance of the low side MOSFET (sync FET) as current sense element. This method enhances the converter's efficiency and reduces cost by eliminating the need for external current sense resistor.

IR3838 includes two low $R_{ds(on)}$ MOSFETs using IR's HEXFET technology. These are specifically designed for high efficiency applications.

Under-Voltage Lockout and POR

The under-voltage lockout circuit monitors the voltage of Vcc/Ldo pin and the Enable input. It assures that the MOSFET driver outputs remain in the off state whenever either of these two signals drop below the set thresholds. Normal operation resumes once Vcc/LDO and Enable rise above their thresholds.

The POR (Power On Ready) signal is generated when all these signals reach the valid logic level (see system block diagram). When the POR is asserted the soft start sequence starts (see soft start section).

Enable

The Enable features another level of flexibility for start up. The Enable has precise threshold which is internally monitored by Under-Voltage Lockout (UVLO) circuit. Therefore, the IR3838 will turn on only when the voltage at the Enable pin exceeds this threshold, typically, 1.2V.

If the input to the Enable pin is derived from the bus voltage by a suitably programmed resistive divider, it can be ensured that the IR3838 does not turn on until the bus voltage reaches the desired level (Fig. 3). Only after the bus voltage reaches or exceeds this level will the voltage at Enable pin exceed its threshold, thus enabling the IR3838. Therefore, in addition to being a logic input pin to enable the IR3838, the Enable feature, with its precise threshold, also allows the user to implement an Under-Voltage Lockout for the bus voltage (PVin). This is desirable particularly for high output voltage applications, where we might want the IR3838 to be disabled at least until PVin exceeds the desired output voltage level.

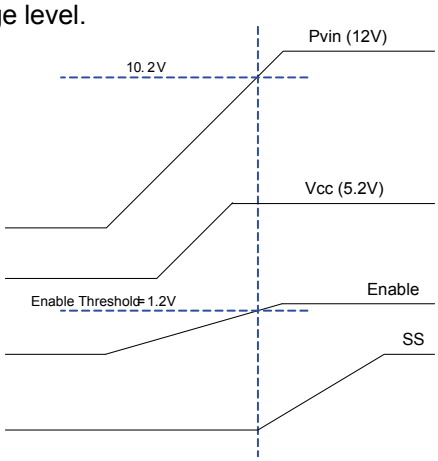


Fig. 3. Normal Start up, device turns on when the bus voltage reaches 10.2V

Figure 4a. shows the recommended start-up sequence for the normal (non-tracking, non-sequencing) operation of IR3838, when Enable is used as a logic input. In this operating mode Vref is left floating. Figure 4b. shows the recommended startup sequence for sequenced operation of IR3838 with Enable used as logic input. For this mode of operation, Vref is left floating. Figure 4c shows the recommended startup sequence for tracking operation of IR3838 with Enable used as logic input. For this mode of operation, Vref is connected to a voltage greater than 1.5V.

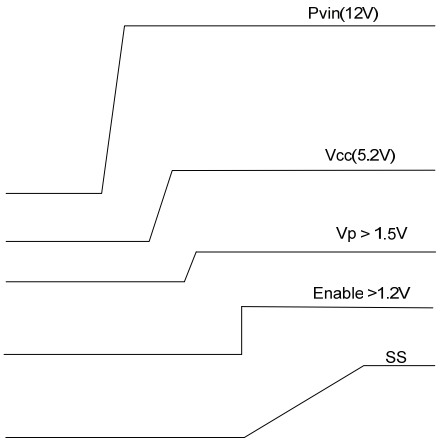


Fig. 4a. Recommended startup for Normal operation

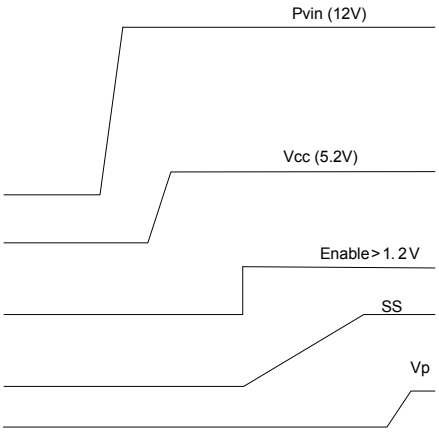


Fig. 4b. Recommended startup for sequencing operation (ratiometric or simultaneous)

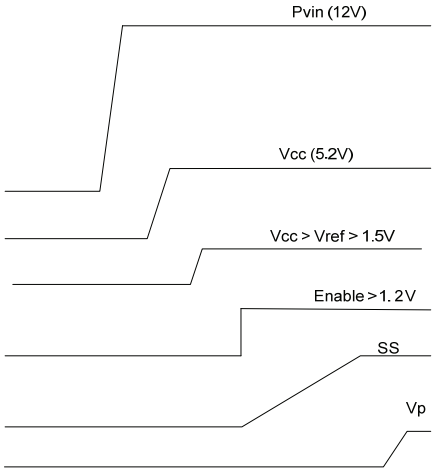


Fig. 4c. Recommended startup for memory tracking operation (Vtt-DDR)

Vref

This pin reflects the internal reference voltage which is used by the error amplifier to set the output voltage. In most operating conditions this pin is only connected to an external bypass capacitor and it is left floating. In tracking mode this pin should be connected to an external voltage greater than 1.5V and less than 7V. For margining applications, an external voltage source is connected to Vref pin and overrides the internal reference voltage. The external voltage source should have a low internal resistance (<100Ω) and be able to source and sink more than 25µA.

Pre-Bias Startup

IR3838 is able to start up into pre-charged output, which prevents oscillation and disturbances of the output voltage.

The output starts in asynchronous fashion and keeps the synchronous MOSFET (sync FET) off until the first gate signal for control MOSFET (control FET) is generated. Figure 5a shows a typical Pre-Bias condition at start up. The sync FET always starts with a narrow pulse width and gradually increases its duty cycle with a step of 25%, 50%, 75% and 100% until it reaches the steady state value. The number of these startup pulses for the sync FET is internally programmed. Figure 5b shows a series of 32, 16, 8 startup pulses.

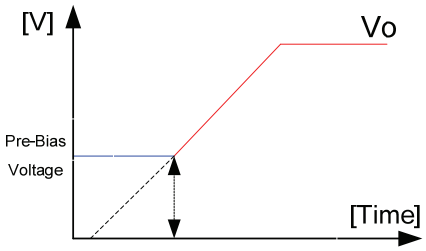


Fig. 5a. Pre-Bias startup

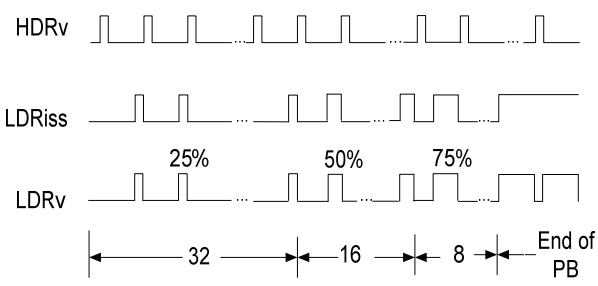


Fig. 5b. Pre-Bias startup pulses

Soft-Start

The IR3838 has a digital internal soft-start to control the output voltage rise and to limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Enable and Vcc rise above their UVLO thresholds and generate the Power On Ready (POR) signal. The internal SS signal linearly rises with the rate of 0.2mV / µs from 0V to 2V. Figure 6 shows the waveforms during soft start (also refer to figure 11). The normal start up time is fixed, and is equal to:

$$T_{start} = \frac{(1.3V - 0.7V)}{0.2mV/\mu s} = 3ms \quad \text{----------(1)}$$

During the soft start the OCP is enabled to protect the device for any short circuit and over current condition.

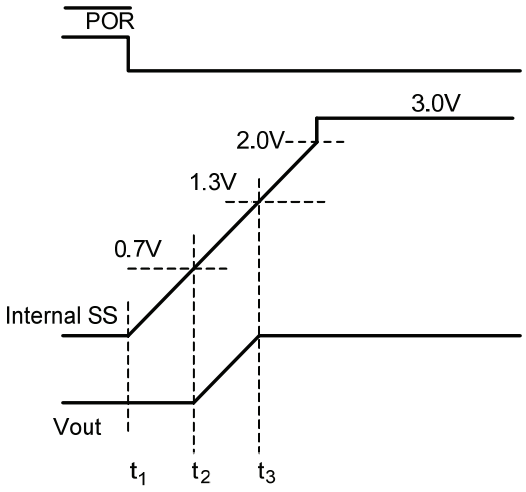


Fig. 6. Theoretical operation waveforms during soft-start (non tracking / non sequencing)

Operating Frequency

The switching frequency can be programmed between 250kHz – 1500kHz by connecting an external resistor from R_t pin to Gnd. Table 1 tabulates the oscillator frequency versus R_t.

Shutdown

The IR3838 can be shutdown by pulling the Enable pin below its 0.85 V threshold. This will tri-state both, the high side driver as well as the low side driver.

Table 1. Switching Frequency and I_{OCSet} vs. External Resistor (R_t)

R_t (kΩ)	F_s (kHz)	I_{ocset} (µA)
47.5	300	14.7
35.7	400	19.6
28.7	500	24.35
23.7	600	29.54
20.5	700	34.1
17.8	800	39.3
15.8	900	44.3
14.3	1000	48.95
12.7	1100	55.1
11.5	1200	60.85
10.7	1300	65.4
9.76	1400	71.7
9.31	1500	75.15

Over-Current Protection

The over current protection is performed by sensing current through the $R_{DS(on)}$ of the sync FET. This method enhances the converter's efficiency and reduces cost by eliminating a current sense resistor. As shown in figure 7, an external resistor (R_{OCSet}) is connected between OCSet pin and the switch node (SW) which sets the current limit set point.

An internal current source sources current (*IOCSet*) out of the *OCSet* pin. This current is a function of Rt and hence, of the free-running switching frequency.

$$I_{OCSet}(\mu A) = \frac{700}{R_t(k\Omega)} \text{.....(2)}$$

Table 1. shows *IOCSet* at different switching frequencies. The internal current source develops a voltage across R_{OCSet}. When the sync FET is turned on, the inductor current flows through Q2 and results in a voltage at OCSet which is given by:

$$V_{OCSet} = (I_{OCSet} * R_{OCSet}) - (R_{DS(on)} * I_L) \text{.....(3)}$$

An over current is detected if the OCSet pin goes below ground. However, to avoid false tripping , due to the noise generated when the sync FET is turned on, the OCP comparator is enabled about 200ns after sync-FET is turned on.

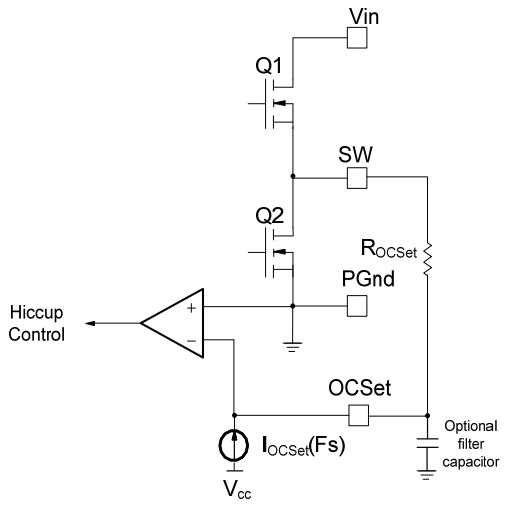


Fig. 7. Connection of over current sensing resistor

As mentioned earlier, an over current is detected if the OCSet pin goes below ground. Hence, at the current limit threshold, V_{OCset}=0. Then, for a current limit setting I_{Limit}, R_{OCSet} is calculated as follows:

$$R_{OCSet} = \frac{R_{DS(on)} * I_{Limit}}{I_{OCSet}} \quad \text{.....(4)}$$

An over-current detection trips the OCP comparator, latches OCP signal and cycles the soft start function in hiccup mode.

The hiccup is performed by making the internal SS signal equal to zero and counting the number of switching cycles. The Soft Start pin is held low until 4096 cycles have been completed. The OCP signal resets and the converter recovers. After every soft start cycle, the converter stays in this mode until the overload or short circuit is removed.
An optional 10pF-22pF filter capacitor can be connected from OCSet pin to PGnd. It is recommended to use this capacitor for very narrow duty cycle applications (pulse-width <150ns).

Thermal Shutdown
Temperature sensing is provided inside IR3838. The trip threshold is typically set to 140°C. When trip threshold is exceeded, thermal shutdown turns off both MOSFETs and resets the internal soft start.
Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20°C hysteresis in the thermal shutdown threshold.

External Synchronization
The IR3838 incorporates an internal circuit which enables synchronization of the internal oscillator (using rising edge) to an external clock. An external resistor from Rt pin to Gnd is still required to set the free-running frequency close to the Sync input frequency. This function is important to avoid sub-harmonic oscillations due to beat frequency for embedded systems when multiple POL (point of load) regulators are used. Applying the external signal to the Sync input changes the effective value of the ramp signal (Vramp/Vosc).

$$Vosc_1 = 1.8 \times f_{Free_Run} / f_{Sync} \quad \text{.....(5)}$$

Equation (5) shows that the effective amplitude of the ramp is reduced after the external Sync signal is applied. More difference between the frequency of the Sync and the free-running frequency results in more change in the effective amplitude of the ramp signal. Therefore, since the ramp amplitude takes part in calculating the loop-gain and bandwidth of the regulator, it is recommended to not use a Sync frequency which is much higher than the free-running frequency (or vice versa). In addition, the effective value of the ramp signal, given by equation (5), should be used when the compensator is designed for the regulator.
The pulse width of the external clock, which is applied to the sync, should be greater than 100ns and its high level should be greater than 2V, while its lower level is less than 0.6V. For more information refer to the Oscillator section in page-6. If this pin is left floating, the IC will run with the free running frequency set by the resistor Rt.

Output Voltage Tracking and Sequencing
The IR3838 can accommodate user programmable tracking and/or sequencing options using Vp, Vref, Enable, and Power Good pins. In the block diagram presented on page 3, the error-amplifier (E/A) has been depicted with three positive inputs. Ideally, the input with the lower voltage is used for regulating the output voltage and the other two inputs are ignored. In practice the voltage of the other two inputs should be about 200mV greater than the low-voltage input so that their effects can completely be ignored. For normal operation, Vp is tied to Vcc (1.5V < Vp < Vcc) and Vref is left floating (with a bypass capacitor).

Therefore, in normal operating condition, after Enable goes high the SS ramps up the output voltage until Vfb (voltage of feedback/Fb pin) reaches about 0.6V. Then Vref takes over and the output voltage is regulated (refer to Fig. 11).

Tracking-mode operation is achieved by connecting Vref to Vcc (1.5V<Vref<Vcc). Then, while Vp=0, Enable is taken above its threshold so that the soft start circuit generates internal SS signal. After the internal SS signal reaches the final value (refer to Fig. 4c) ramping up the Vp input will ramp up the output voltage. In tracking mode, Vfb always follows Vp which means Vout is always proportional to Vp voltage (typical for DDR/Vtt rail applications)

In sequencing mode of operation (simultaneous or ratiometric), Vref is left floating and Vp is kept to ground level until after SS signal reaches the final value. Then Vp is ramped up and Vfb follows Vp. When Vp>0.6V the error-amplifier switches to Vref and the output voltage is regulated with Vref.

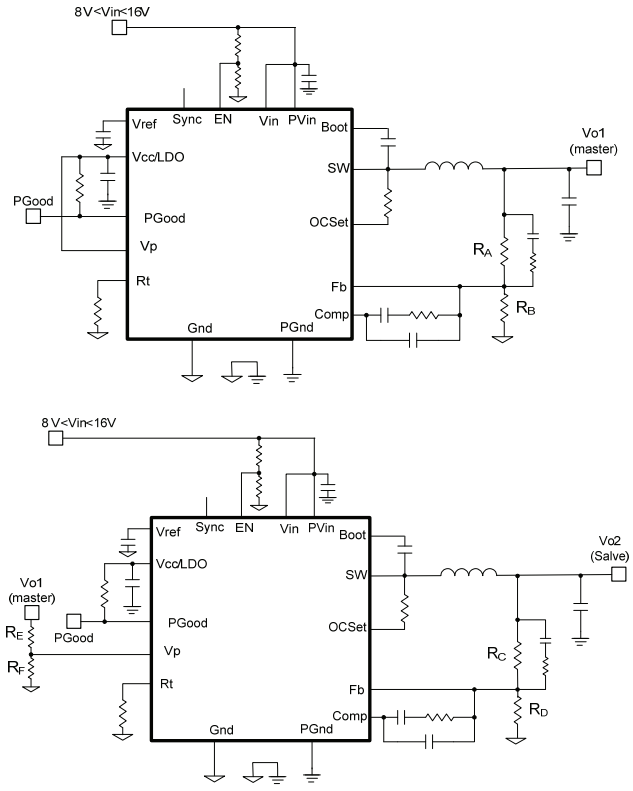


Fig. 8. Application Circuit for Simultaneous and ratiometric Sequencing

Tracking and sequencing operations can be implemented to be simultaneous or ratiometric (refer to figures 9 and 10). Figure 8 shows typical circuit configuration for sequencing operation. With this power-up configuration, the voltage at the Vp pin of the slave reaches 0.6V before the Fb pin of the master. If $\mathbf{R_E/R_F = R_C/R_D}$, simultaneous startup is achieved. That is, the output voltage of the slave follows that of the master until the voltage at the Vp pin of the slave reaches 0.6 V. After the voltage at the Vp pin of the slave exceeds 0.6V, the internal 0.6V reference of the slave dictates its output voltage. In reality the regulation gradually shifts from Vp to internal Vref. The circuit shown in Fig. 8 can also be used for simultaneous or ratiometric tracking operation if Vref of the slave is connected to Vcc. Table 2 on page 17 summarizes the required conditions to achieve simultaneous / ratiometric tracking or sequencing operations.

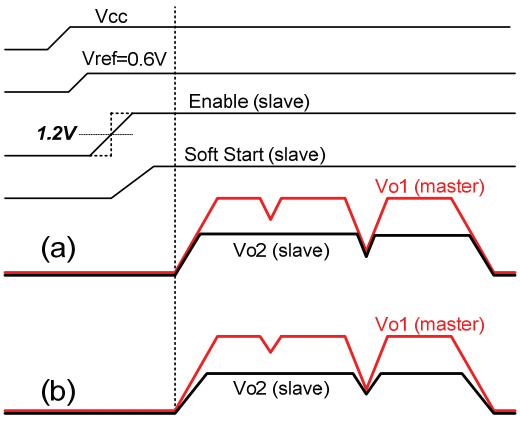


Fig. 9 Typical waveforms for sequencing mode of operation: (a) simultaneous, (b) ratiometric

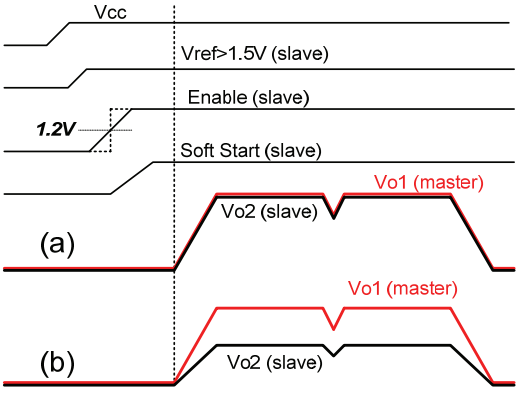


Fig. 10 Typical waveforms in tracking mode of operation: (a) simultaneous, (b) ratiometric

Power Good Output

The IC continually monitors the output voltage via Feedback (Fb pin). The feedback voltage is compared to a threshold. The threshold is set differently at different operating modes and the results of the comparison sets the PGood signal.

Figures 11, 12, and 13 show the timing diagram of the PGood signal at different operating modes.

The PGood pin is open drain and it needs to be externally pulled high. High state indicates that output is in regulation.

Table 2. The required conditions to achieve simultaneous / ratiometric tracking and sequencing operations with the circuit configuration of Fig. 8

Operating Mode	Vref (slave)	Vp	Required Condition
Normal (Non-Sequencing, Non-Tracking)	0.6V (Float)	> 1.5V	-
Simultaneous Sequencing	0.6V	Ramp up from 0V	$R_A/R_B > R_E/R_F = R_C/R_D$
Ratiometric Sequencing	0.6V	Ramp up from 0V	$R_A/R_B > R_E/R_F > R_C/R_D$
Simultaneous Tracking	> 1.5V	Ramp up from 0V	$R_E/R_F = R_C/R_D$
Ratiometric Tracking	> 1.5V	Ramp up from 0V	$R_E/R_F > R_C/R_D$

TIMING DIAGRAM OF PGOOD FUNCTIONS

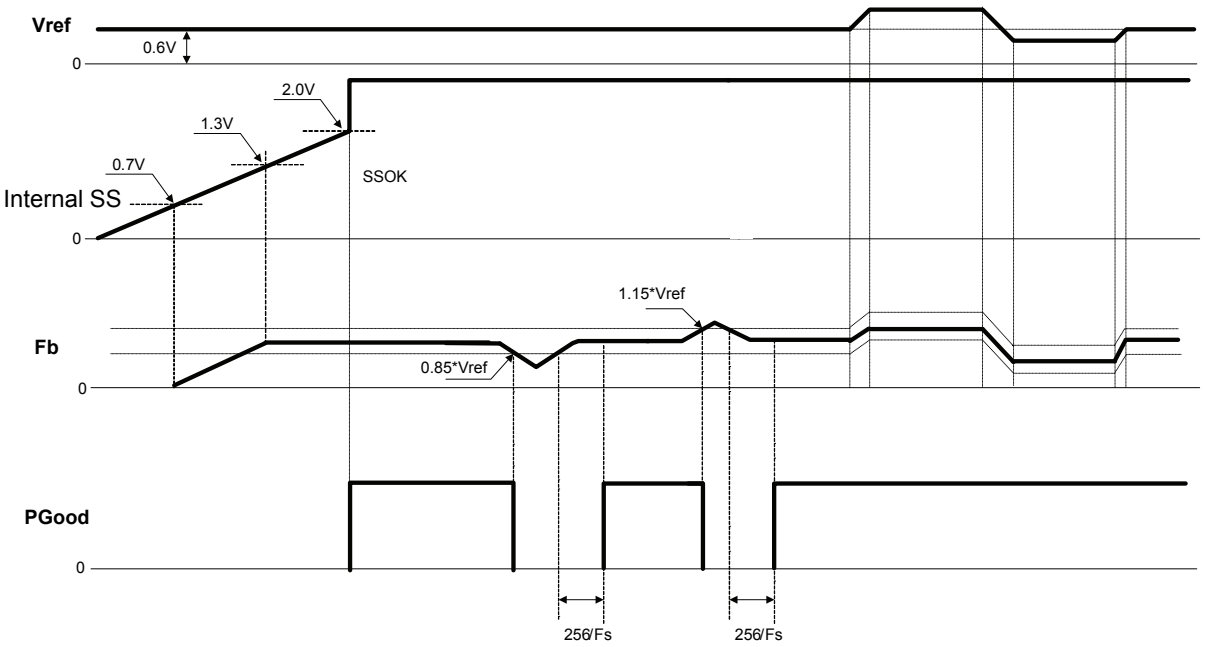


Fig.11 Non-sequence Startup and Vref Margin (Vp =Vcc)

TIMING DIAGRAM OF PGOOD FUNCTIONS

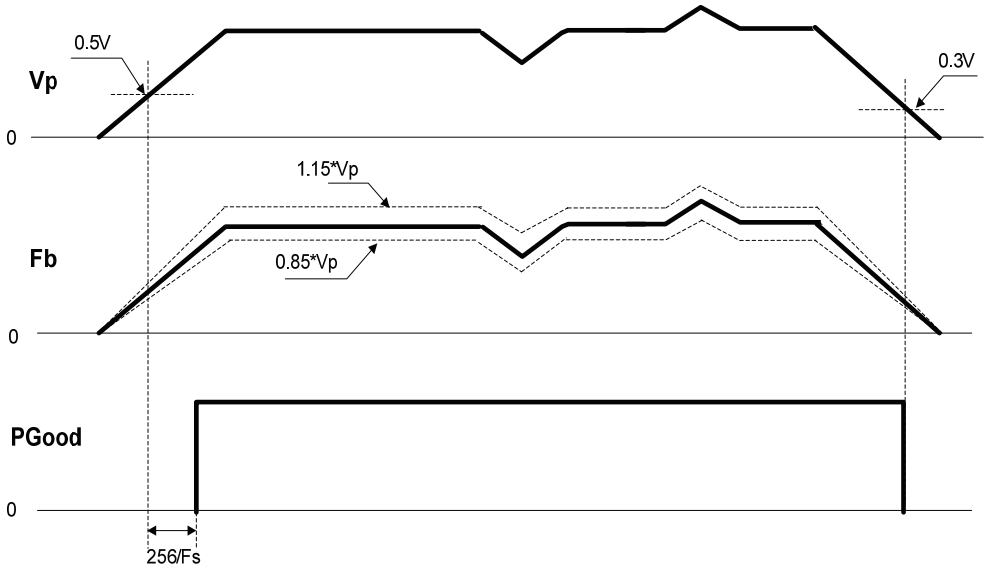


Fig.12 Vp Tracking (Vref >1.5V, SS=H)

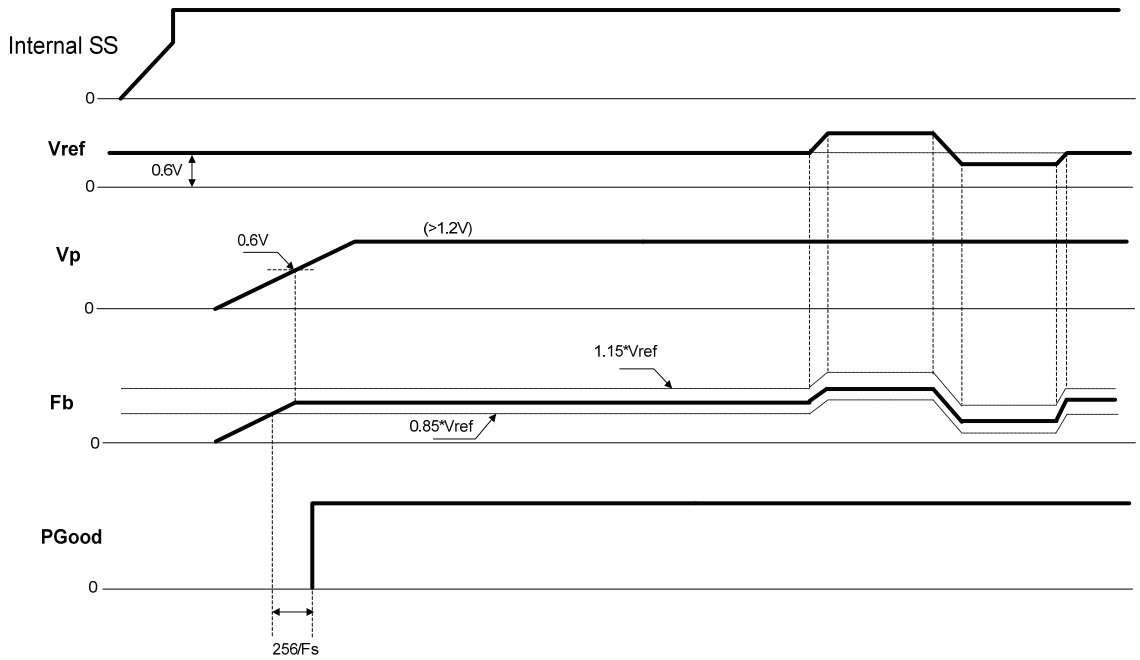


Fig.13 Vp Sequence and Vref Margin

Minimum on time Considerations

The minimum ON time is the shortest amount of time for which the Control FET may be reliably turned on, and this depends on the internal timing delays. For the IR3838, the typical minimum on-time is specified as 70 ns.
Any design or application using the IR3838 must ensure operation with a pulse width that is higher than this minimum on-time and preferably higher than 150 ns. This is necessary for the circuit to operate without jitter and pulse-skipping, which can cause high inductor current ripple and high output voltage ripple.

$$t_{on} = \frac{D}{F_s} = \frac{V_{out}}{V_{in} \times F_s}$$

In any application that uses the IR3838, the following condition must be satisfied:

$$t_{on(min)} \le t_{on}$$
$$\therefore t_{on(min)} \le \frac{V_{out}}{V_{in} \times F_s}$$
$$\therefore V_{in} \times F_s \le \frac{V_{out}}{t_{on(min)}}$$

The minimum output voltage is limited by the reference voltage and hence $V_{out(min)}$ = 0.6 V. Therefore, for $V_{out(min)}$ = 0.6 V,

$$\therefore V_{in} \times F_s \le \frac{V_{out(min)}}{t_{on(min)}}$$
$$\therefore V_{in} \times F_s \le \frac{0.6\ \text{V}}{150\ \text{ns}} = 4 \times 10^6\ \text{V/s}$$

Therefore, at the maximum recommended input voltage 16V and minimum output voltage, the converter should be designed at a switching frequency that does not exceed 250 kHz. Conversely, for operation at the maximum recommended operating frequency (1.65 MHz) and minimum output voltage (0.6V), The input voltage (PVin) should not exceed 2.42V, otherwise pulse skipping will happen.
At low output voltages (below 1V) specially at Vo=0.6V, it is recommended to design the compensator so that the bandwidth of the loop does not exceed 1/10 of the switching frequency.

Maximum Duty Ratio Considerations

A fixed off-time of 300 ns maximum is specified for the IR3838. This provides an upper limit on the operating duty ratio at any given switching frequency. Thus, the higher the switching frequency, the lower is the maximum duty ratio at which the IR3838 can operate. To allow some margin, the maximum operating duty ratio in any application using the IR3838 should still accommodate about 500 ns off-time. Fig 14. shows a plot of the maximum duty ratio v/s the switching frequency, with 300 ns off-time.

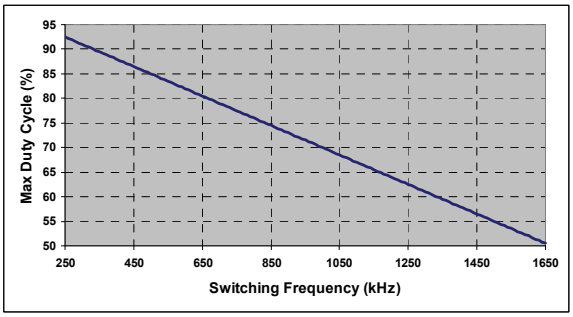


Fig. 14. Maximum duty cycle v/s switching frequency.

Application Information

Design Example:

The following example is a typical application for IR3838. The application circuit is shown on page 26.

$V_{in} = 12\,\text{V}\,(13.2\text{V max})$
$V_o = 1.8\,\text{V}$
$I_o = 10\,\text{A}$
$\Delta V_o \leq \pm 2\% \cdot V_o$ (*for 30% load transient*)
$F_s = 600\,\text{kHz}$

Enabling the IR3838

As explained earlier, the precise threshold of the Enable lends itself well to implementation of a UVLO for the Bus Voltage as shown in figure 15.

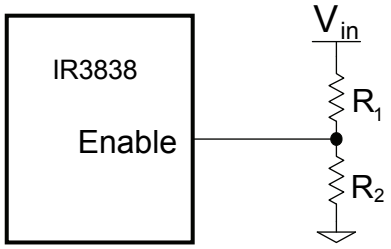


Fig. 15. Using Enable pin for UVLO implementation

For a typical Enable threshold of V_{EN} = 1.2 V

$$V_{in(min)} * \frac{R_2}{R_1 + R_2} = V_{EN} = 1.2 \quad \ldots\ldots\ldots (6)$$

$$R_2 = R_1 \frac{V_{EN}}{V_{in(\,min\,)} - V_{EN}} \quad \ldots\ldots\ldots (7)$$

For a $V_{in\ (min)}$=10.2V, R_1=49.9K and R_2=6.8k ohm is a good choice.

Programming the frequency

For F_s = 600 kHz, select R_t = 23.7 kΩ, using Table 1.

Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 0.6V. The divider ratio is set to provide 0.6V at the Fb pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_o = V_{ref} * \left(1 + \frac{R_8}{R_9}\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (8)$$

When an external resistor divider is connected to the output as shown in figure 16.
Equation (8) can be rewritten as:

$$R_9 = R_8 * \left(\frac{V_{ref}}{V_o - V_{ref}}\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (9)$$

For the calculated values of R8 and R9 see feedback compensation section.

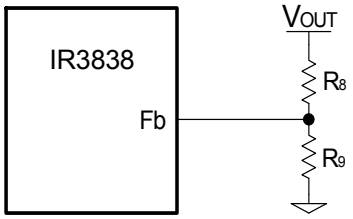


Fig. 16. Typical application of the IR3838 for programming the output voltage

Bootstrap Capacitor Selection

To drive the Control FET, it is necessary to supply a gate voltage at least 4V greater than the voltage at the SW pin, which is connected to the source of the Control FET . This is achieved by using a bootstrap configuration, which comprises the internal bootstrap diode and an external bootstrap capacitor (C6). The operation of the circuit is as follows: When the sync FET is turned on, the capacitor node connected to SW is pulled down to ground. The capacitor charges towards V_{cc} through the internal bootstrap diode (figure 17), which has a forward voltage drop V_D. The voltage V_c across the bootstrap capacitor C6 is approximately given as

$$V_c \cong V_{cc} - V_D \quad \ldots\ldots\ldots\ldots\ldots\ldots (10)$$

When the control FET turns on in the next cycle, the capacitor node connected to SW rises to the bus voltage V_{in}. However, if the value of C6 is appropriately chosen, the voltage V_c across C6 remains approximately unchanged and the voltage at the Boot pin becomes:

$$V_{Boot} \cong V_{in} + V_{cc} - V_D \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (11)$$

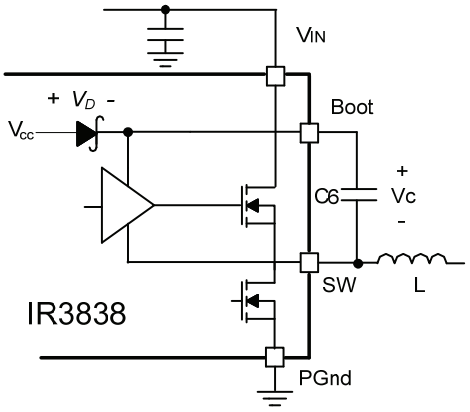


Fig. 17. Bootstrap circuit to generate Vc voltage

A bootstrap capacitor of value 0.1uF is suitable for most applications.

Input Capacitor Selection

The ripple current generated during the on time of the control FET should be provided by the input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_o * \sqrt{D*(1-D)} \quad \text{.....(12)}$$

$$D = \frac{V_o}{V_{in}} \quad \text{.....(13)}$$

Where:

D is the Duty Cycle

I_{RMS} is the RMS value of the input capacitor current.

Io is the output current.

For I_o=10A and D = 0.15, the I_{RMS} = 3.6A.

Ceramic capacitors are recommended due to their peak current capabilities. They also feature low ESR and ESL at higher frequency which enables better efficiency. For this application, it is advisable to have 3x10uF, 16V ceramic capacitors, ECJ-3YX1C106K from Panasonic. In addition to these, although not mandatory, a 1x330uF, 25V SMD capacitor EEV-FK1E331P may also be used as a bulk capacitor and is recommended if the input power supply is not located close to the converter.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value causes large ripple current, resulting in the smaller size, faster response to a load transient but poor efficiency and high output noise. Generally, the selection of the inductor value can be reduced to the desired maximum ripple current in the inductor (Δi) . The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for the desired operating ripple current can be determined using the following relation:

$$V_{in} - V_o = L * \frac{\Delta i}{\Delta t};\ \ \Delta t = D * \frac{1}{F_s}$$
$$L = (V_{in} - V_o) * \frac{V_o}{V_{in} * \Delta i * F_s} \quad \text{..... (14)}$$

Where:

V_{in} = Maximum input voltage

V_o = Output Voltage

Δi = Inductor ripple current

F_s = Switching frequency

Δt = Turn on time

D = Duty cycle

If $\Delta i \approx 42.5\%(I_o)$, then the output inductor is calculated to be 0.6µH. Select MPL104-0R6 from Delta (L=0.6µH) which provides a compact, low profile inductor suitable for this application.

Output Capacitor Selection

The voltage ripple and transient requirements determine the output capacitors type and values. The criteria is normally based on the value of the Effective Series Resistance (ESR). However the actual capacitance value and the Equivalent Series Inductance (ESL) are other contributing components. These components can be described as

$$\Delta V_o = \Delta V_{o(ESR)} + \Delta V_{o(ESL)} + \Delta V_{o(C)}$$
$$\Delta V_{o(ESR)} = \Delta I_L * ESR$$
$$\Delta V_{o(ESL)} = \left(\frac{V_{in} - V_o}{L}\right) * ESL$$
$$\Delta V_{o(C)} = \frac{\Delta I_L}{8 * C_o * F_s} \quad \text{.....(15)}$$

Where:

ΔV_o = output voltage ripple
ΔI_L = Inductor ripple current

Since the output capacitor has a major role in the overall performance of the converter and determines the result of transient response, selection of the capacitor is critical. The IR3838 can perform well with all types of capacitors.

As a rule, the capacitor must have low enough ESR to meet output ripple and load transient requirements.

The goal for this design is to meet the voltage ripple requirement in the smallest possible capacitor size. Therefore it is advisable to select ceramic capacitors due to their low ESR and ESL and small size. Five of Taiyo Yuden's JMK212BJ476MG-T (47uF, 6.3V, ≈3mΩ) capacitors is a good choice.

It is also recommended to use a 0.1µF ceramic capacitor at the output for high frequency filtering.

Feedback Compensation

The IR3838 is a voltage mode controller. The control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed-loop transfer function with the highest 0 dB crossing frequency and adequate phase margin (greater than 45º).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180º (see figure 18). The resonant frequency of the LC filter is expressed as follows:

$$F_{LC} = \frac{1}{2*\pi\sqrt{L_o * C_o}} \quad \text{.....(16)}$$

Figure 18 shows gain and phase of the LC filter. Since we already have 180º phase shift from the output filter alone, the system runs the risk of being unstable.

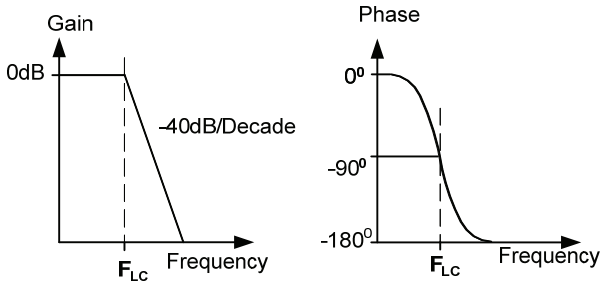


Fig. 18. Gain and Phase of LC filter

The IR3838 uses a voltage-type error amplifier with high-gain (110dB) and high-bandwidth (30MHz). The output of the amplifier is available for DC gain control and AC phase compensation.

The error amplifier can be compensated either in type II or type III compensation.

Local feedback with Type II compensation is shown in Fig. 19.

This method requires that the output capacitor should have enough ESR to satisfy stability requirements. If the output capacitor's ESR generates a zero at 5kHz to 50kHz, the zero generates acceptable phase margin and the Type II compensator can be used.

The ESR zero of the output capacitor is expressed as follows:

$$F_{ESR} = \frac{1}{2*\pi*ESR*C_o} \quad \text{.....(17)}$$

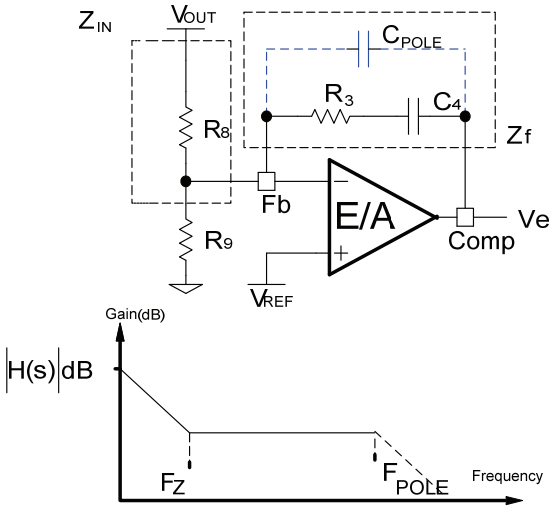


Fig. 19. Type II compensation network and its asymptotic gain plot

The transfer function (V_e/V_{out}) is given by:

$$\frac{V_e}{V_{out}} = H(s) = -\frac{Z_f}{Z_{IN}} = -\frac{1+sR_3C_4}{sR_8C_4} \quad \text{.....(18)}$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$\left| H(s) \right| = \frac{R_3}{R_8} \quad \text{.....(19)}$$

$$F_z = \frac{1}{2\pi * R_3 * C_4} \quad \text{.....(20)}$$

First select the desired zero-crossover frequency (F_o):

$$F_o > F_{ESR} \text{ and } F_o \le (1/5 \sim 1/10) * F_s \quad \text{.....(21)}$$

Use the following equation to calculate R3:

$$R_3 = \frac{V_{osc} * F_o * F_{ESR} * R_8}{V_{in} * F_{LC}^2} \quad \text{.....(22)}$$

Where:
V_{in} = Maximum Input Voltage
V_{osc} = Amplitude of the oscillator Ramp Voltage
F_o = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_8 = Feedback Resistor

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_z = 75\% F_{LC}$$

$$F_z = 0.75 * \frac{1}{2\pi\sqrt{L_o * C_o}} \quad \text{.....(23)}$$

Use equations (20), (21) and (22) to calculate C4.
One more capacitor is sometimes added in parallel with C4 and R3. This introduces one more pole which is mainly used to suppress the switching noise.

The additional pole is given by:

$$F_P = \frac{1}{2\pi * R_3 * \frac{C_4 * C_{POLE}}{C_4 + C_{POLE}}} \quad \text{.....(24)}$$

The pole sets to one half of the switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi * R_3 * F_s - \frac{1}{C_4}} \cong \frac{1}{\pi * R_3 * F_s} \quad \text{.....(25)}$$

For a general solution for unconditional stability for any type of output capacitors, and a wide range of ESR values, we should implement local feedback with a type III compensation network. The typically used compensation network for voltage-mode controller is shown in figure 20.

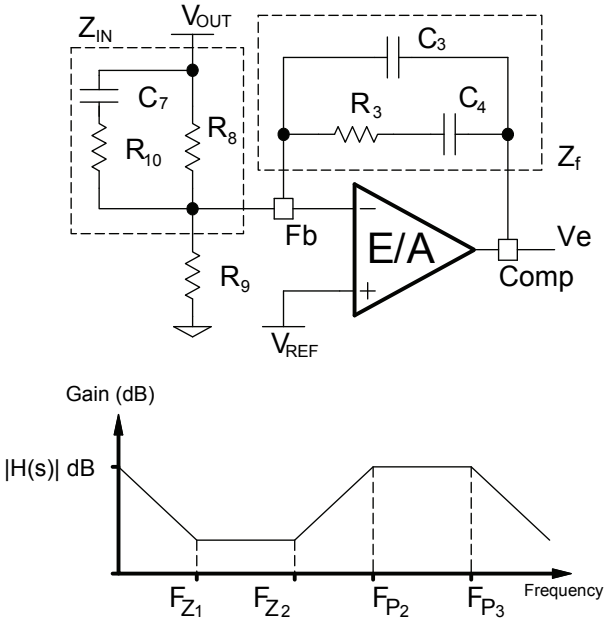


Fig.20. Type III Compensation network and its asymptotic gain plot

Again, the transfer function is given by:

$$\frac{V_e}{V_{out}} = H(s) = -\frac{Z_f}{Z_{IN}}$$

By replacing Z_{in} and Z_f according to figure 20, the transfer function can be expressed as:

$$H(s) = -\frac{(1+sR_3C_4)[1+sC_7(R_8+R_{10})]}{sR_8(C_4+C_3)\left[1+sR_3\left(\frac{C_4*C_3}{C_4+C_3}\right)\right](1+sR_{10}C_7)} \quad ....(26)$$

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0 \quad .....(27)$$

$$F_{P2} = \frac{1}{2\pi * R_{10} * C_7} \quad .....(28)$$

$$F_{P3} = \frac{1}{2\pi * R_3\left(\frac{C_4 * C_3}{C_4 + C_3}\right)} \cong \frac{1}{2\pi * R_3 * C_3} \quad .....(29)$$

$$F_{Z1} = \frac{1}{2\pi * R_3 * C_4} \quad .....(30)$$

$$F_{Z2} = \frac{1}{2\pi * C_7 * (R_8 + R_{10})} \cong \frac{1}{2\pi * C_7 * R_8} \quad .....(31)$$

Cross over frequency is expressed as:

$$F_o = R_3 * C_7 * \frac{V_{in}}{V_{osc}} * \frac{1}{2\pi * L_o * C_o} \quad .....(32)$$

Based on the frequency of the zero generated by the output capacitor and its ESR, relative to crossover frequency, the compensation type can be different. Table 3 shows the compensation types for relative locations of the crossover frequency.

Table 3. Different types of compensators

Compensator Type	F_{ESR} vs F_0	Typical Output Capacitor
Type II	$F_{LC} < F_{ESR} < F_0 < F_S/2$	Electrolytic
Type III	$F_{LC} < F_0 < F_{ESR}$	SP-Cap, Ceramic

The higher the crossover frequency is, the potentially faster the load transient response will be. However, the crossover frequency should be low enough to allow attenuation of switching noise. Typically, the control loop bandwidth or crossover frequency (F_o) is selected such that

$$F_o \le (1/5 \sim 1/10) * F_s$$

The DC gain should be large enough to provide high DC-regulation accuracy. The phase margin should be greater than 45° for overall stability.

For this design we have:
V_{in}=12V
V_o=1.8V
V_{osc}=1.8V
V_{ref}=0.6V
L_o=0.6µH
C_o=5x47µF, ESR≈3mΩ each

It must be noted here that the value of the capacitance used in the compensator design must be the small signal value. For instance, the small signal capacitance of the 47uF capacitor used in this design is 26uF at 1.8 V DC bias and 600 kHz frequency. It is this value that must be used for all computations related to the compensation. The small signal value may be obtained from the manufacturer's datasheets, design tools or SPICE models. Alternatively, they may also be inferred from measuring the power stage transfer function of the converter and measuring the double pole frequency F_{LC} and using equation (16) to compute the small signal C_o.

These result to:
F_{LC}=18 kHz
F_{ESR}=2.04 MHz
F_s/2=300 kHz

Select crossover frequency F_0=100 kHz
Since $F_{LC}<F_0<Fs/2<F_{ESR}$, Type III is selected to place the pole and zeros.

Detailed calculation of compensation Type III :

Desired Phase Margin $\Theta=70^{o}$

$$F_{Z2}=F_o\sqrt{\frac{1-sin\,\Theta}{1+sin\,\Theta}}=17.63\text{kHz}$$

$$F_{P2}=F_o\sqrt{\frac{1+sin\,\Theta}{1-sin\,\Theta}}=567.1\text{kHz}$$

Select $F_{Z1}=0.5*F_{Z2}=8.82$ kHz and

$$F_{P3}=0.5*F_s=300\text{ kHz}$$

Select $C_7=2.2\text{nF}$

Calculate R_3, C_3 and C_4 :

$$R_3=\frac{2\pi*F_o*L_o*C_o*V_{osc}}{C_7*V_{in}};R_3=3.34\text{ k}\Omega$$

Select $R_3=3.32\,\text{k}\Omega$

$$C_4=\frac{1}{2\pi*F_{Z1}*R_3};C_4=5.44\text{ nF},\text{ Select }C_4=5.6\text{ nF}$$

$$C_3=\frac{1}{2\pi*F_{P3}*R_3};C_3=159\,\text{pF},\text{ Select}\,C_3=150\,\text{pF}$$

Calculate R_{10}, R_8 and R_9 :

$$R_{10}=\frac{1}{2\pi*C_7*F_{P2}};\ R_{10}=128\,\Omega,\text{ Select}\,R_{10}=127\,\Omega$$

$$R_8=\frac{1}{2\pi*C_7*F_{Z2}}-R_{10};\ R_8=3.98\,\text{k}\Omega,$$

Select $R_8=4.02\,\text{k}\Omega$

$$R_9=\frac{V_{ref}}{V_o-V_{ref}}*R_8;R_9=2.01\text{k}\Omega\text{ Select}\,R_9=2\text{ k}\Omega$$

Programming the Current-Limit
The Current-Limit threshold can be set by connecting a resistor (R_{OCSet}) from the SW pin to the OCSet pin. The resistor can be calculated by using equation (4). This resistor (R_{OCSet}) must be placed close to the IC.
The $R_{DS(on)}$ has a positive temperature coefficient and it should be considered for the worst case operation (40% increase due to temperature has been considered in below).

$$I_{SET}=I_{L(critical)}=\frac{R_{OCSet}*I_{OCSet}}{R_{DS(on)}}\quad\text{.....(33)}$$

$R_{DS(on)}=8.5\ \text{m}\Omega*1.4=11.9\ \text{m}\Omega$
$I_{SET}\cong I_{o(LIM)}=10\text{ A}*1.5=15\text{ A}$
(50% over nominal output current)
$I_{OCSet}=29.54\ \mu\text{A}$ (at $F_s=600\,\text{kHz}$)
$R_{OCSet}=6.04\ \text{k}\Omega$ Select $R_{OCSet}=6.04\ \text{k}\Omega$

The optional filter capacitor from OCSet pin to PGnd has not been used for this design.

Setting the Power Good Threshold
In this design IR3838 is used in normal (non-tracking, non-sequencing) mode, therefore the PGood thresholds are internally set at 85% and 115% of Vref. At startup as soon as the internal soft start signal reaches 2V (Figure 11), and assuming Fb voltage follows Vref, the PGood is asserted. As long as the voltage at the Fb pin is between the thresholds (mentioned above), Enable is high, and no fault happens, the PGood remains high.

The PGood is an open drain output. Hence, it is necessary to use a pull up resistor, R_{PG}, from PGood pin to Vcc. The value of the pull-up resistor must be chosen such as to limit the current flowing into the PGood pin to less than 5mA when the output voltage is not in regulation. A typical value used is 10kΩ.

Vref Bypass Capacitor
A bypass capacitor of about 0.1uF is required to be placed between Vref and Gnd pins. This capacitor should be placed as close as possible to Vref pin.

Application Diagram:

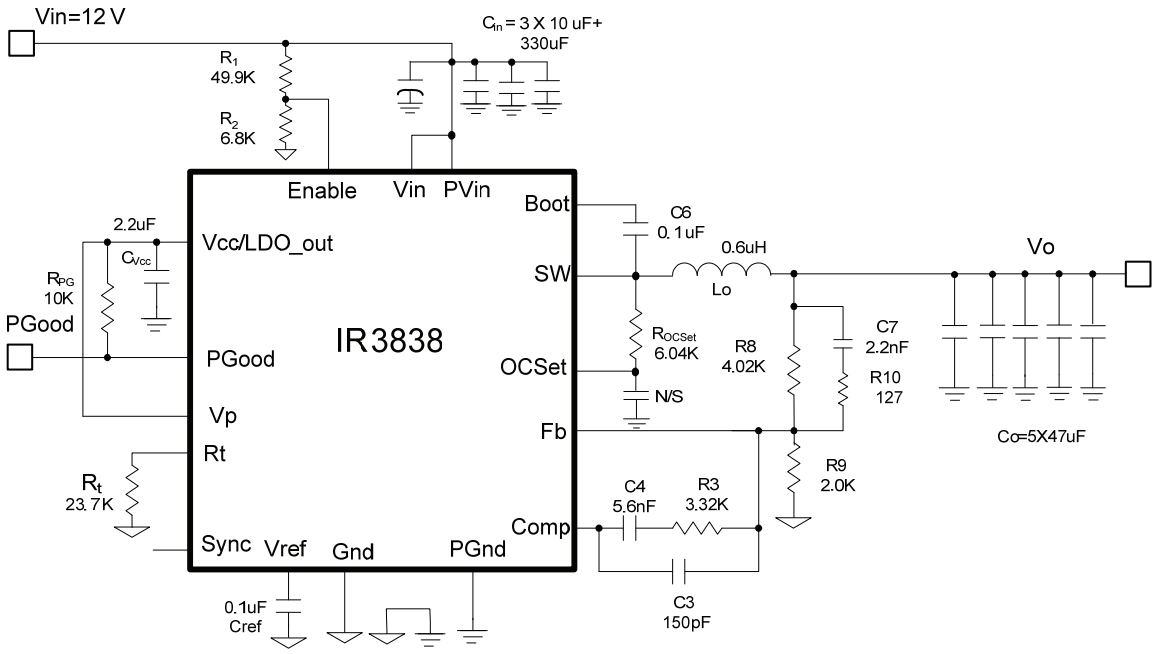


Fig. 21. Application circuit diagram for a 12V to 1.8 V, 10 A Point Of Load Converter

Suggested Bill of Materials for the application circuit:

Part Reference	Quantity	Value	Description	Manufacturer	Part Number
Cin	1	330uF	SMD Elecrolytic, Fsize, 25V, 20%	Panasonic	EEV-FK1E331P
	3	10uF	1206, 16V, X7R, 20%	Panasonic - ECG	ECJ-3YX1C106K
Lo	1	0.6uH	11.5x10x4mm, 20%, 1.5mΩ	Delta	MPL104-0R6
Co	5	47uF	Ceramic, 6.3V, 0805, X5R,20%	Taiyo Yuden	JMK212BJ476MG-T
R1	1	49.9K	Thick Film, 0603,1/10 W,1%	Rohm	MCR03EZPFX4992
R2	1	6.8K	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX6801
R_t	1	23.7k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX2372
R_{OCSet}	1	6.04k	Thick Film, 0603,1/10 W,1%	Rohm	MCR03EZPFX6041
R_{PG}	1	10K	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX1002
Cref	1	0.1uF	0603, 25V, X7R, 10%	Panasonic - ECG	ECJ-1VB1E104K
R3	1	3.32k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX3321
C3	1	150pF	50V, 0603, NPO, 5%	Panasonic- ECG	ECJ-1VC1H151J
C4	1	5.6nF	0603, 50V, X7R, 10%	Panasonic - ECG	ECJ-1VB1H562K
C6	1	0.1uF	0603, 25V, X7R, 10%	Panasonic - ECG	ECJ-1VB1E104K
R8	1	4.02K	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX4021
R9	1	2.0K	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX2001
R10	1	127	Thick Film, 0603,1/10W,1%	Panasonic - ECG	ERJ-3EKF1270V
C7	1	2200pF	0603, 50V, X7R, 10%	Panasonic - ECG	ECJ-1VB1H222K
CVcc	1	2.2uF	0603, 10V, X5R, 10%	Panasonic - ECG	ECJ-1VB1A225K
U1	1	IR3838	SupIRBuck, 10A, PQFN 5x6mm	International Rectifier	IR3838MPbF

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc/LDO=5.2V, Vo=1.8V, Io=0-10A, Room Temperature, No Air Flow

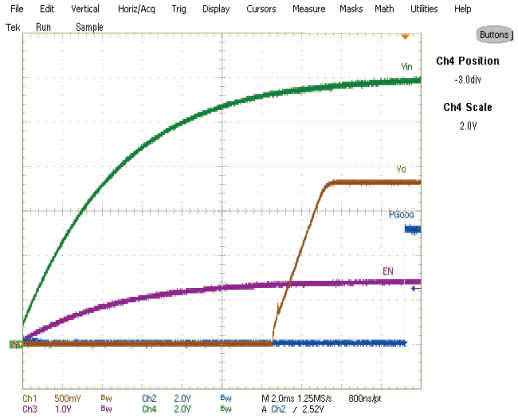


Fig. 22: Start up at 10A Load (Note 6)
Ch_1:V_{out} Ch_2:PGood Ch_3:EN Ch_4: V_{in}

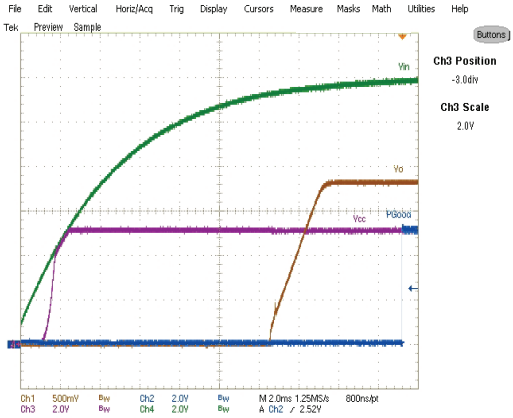


Fig. 23: Start up at 10A Load (Note 6)
Ch_1:V_{out} Ch_2:PGood Ch_3:Vcc Ch_4: V_{in}

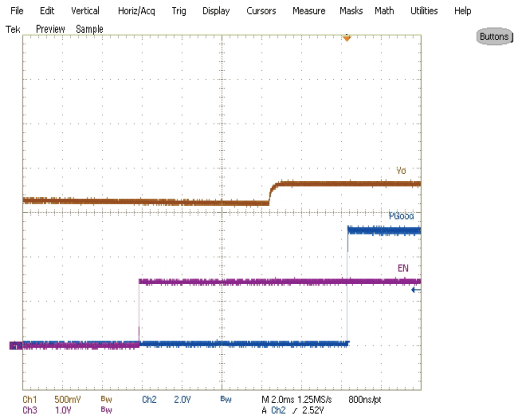


Fig. 24: Start up with 1.62V Prebias,
0A Load, Ch_1:V_{out} Ch_2: PGood Ch_3: EN

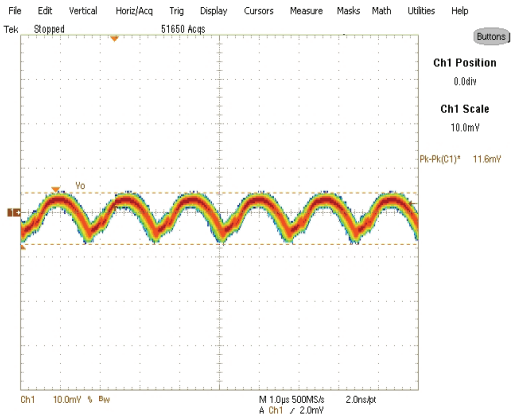


Fig. 25: Output Voltage Ripple,
10A load Ch_1: V_{out}

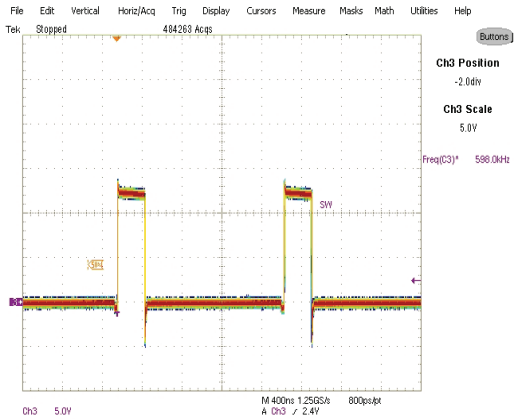


Fig. 26: Inductor node at 10A load
Ch_3:SW

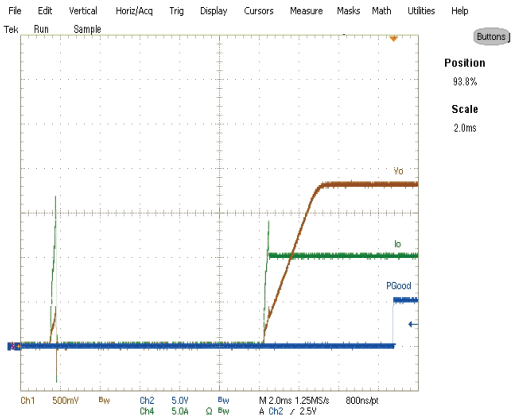


Fig. 27: Short (Hiccup) Recovery
Ch_1:V_{out}, Ch_2:PGood , Ch_4:Iout

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc/LDO=5.2V, Vo=1.8V, Room Temperature, No Air Flow

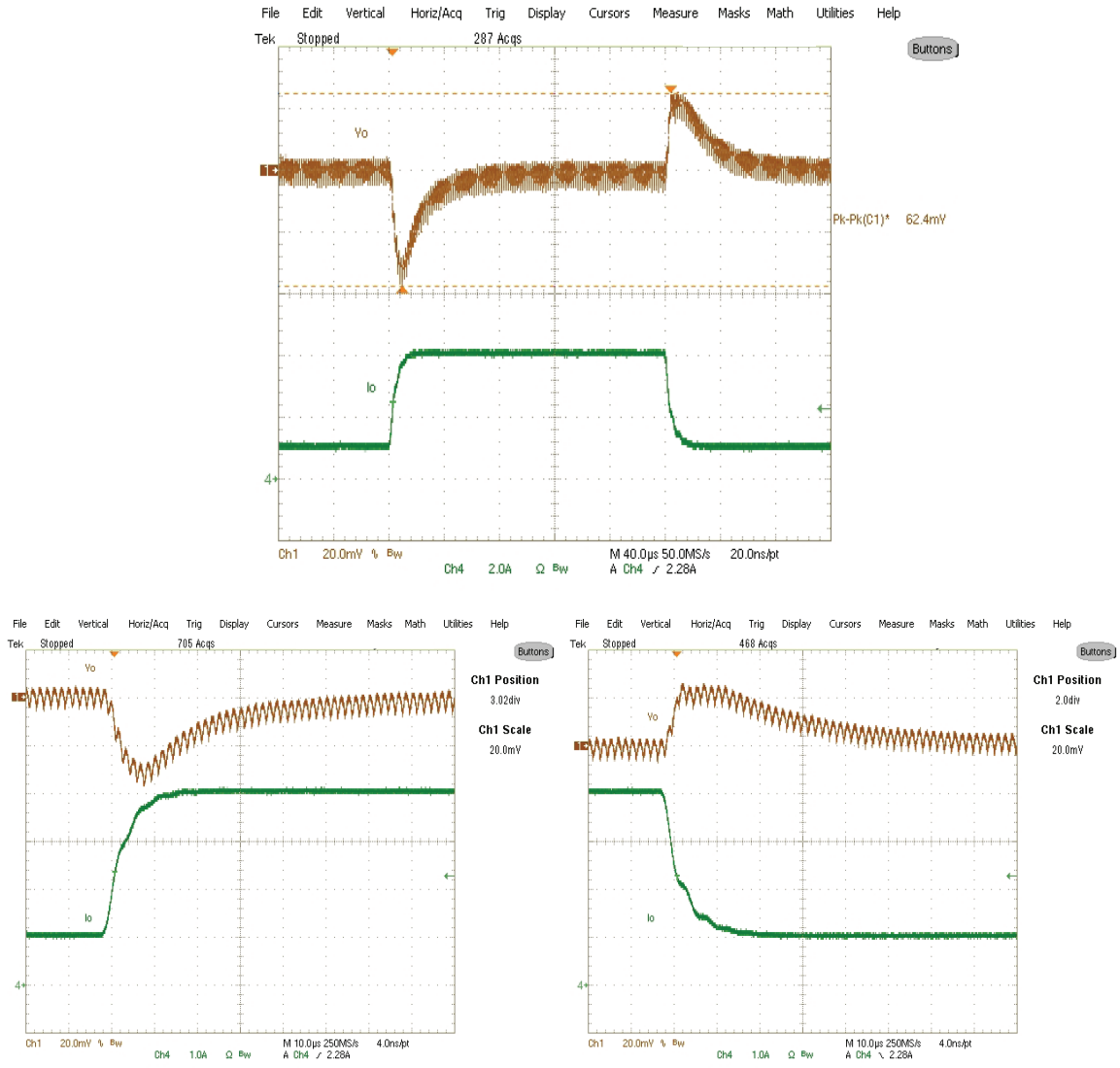


Fig. 28: Transient Response
1A-4A load (0.5A/us) Ch_1:V_{out}, Ch_4:I_o

Note6: Enable (EN) is tied to Vin via a resistor divider and triggered when Vin is exceeding above 10.2V.

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc/LDO=5.2V, Vo=1.8V, Io=0-10A, Room Temperature, No Air Flow

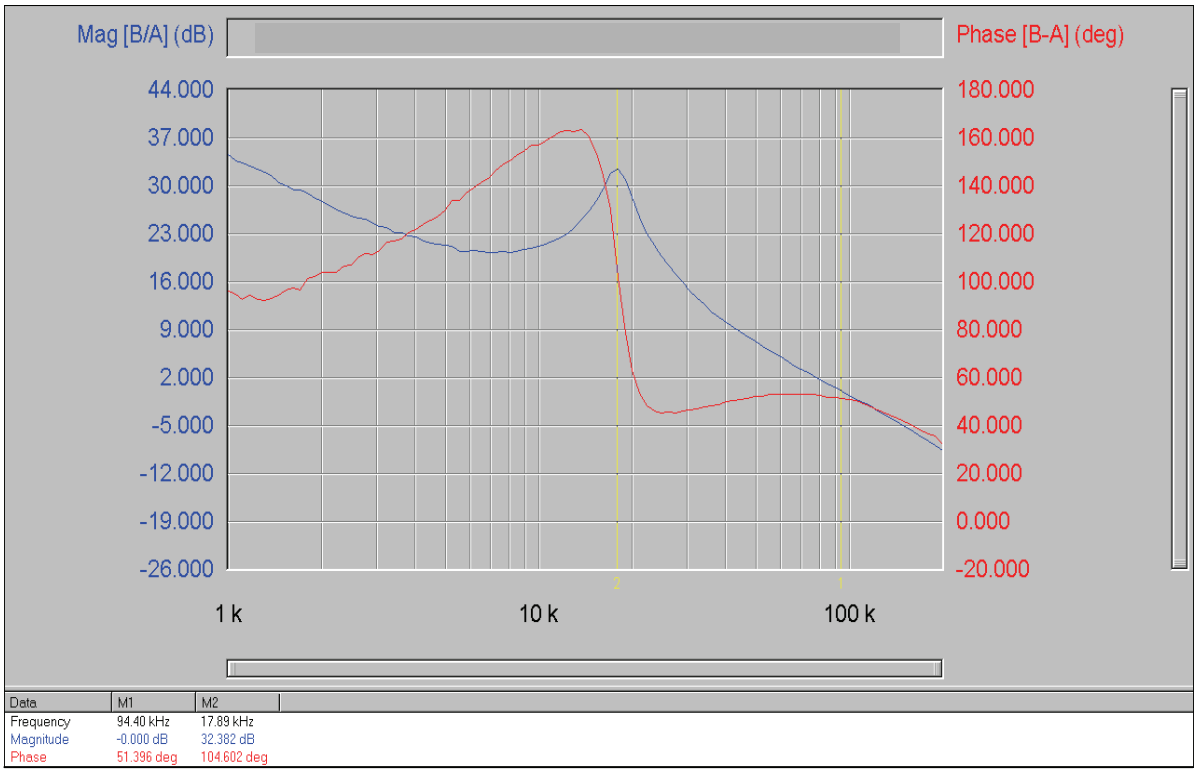


Fig.29: Bode Plot at 10A load shows a bandwidth of 94kHz and phase margin of 51 degrees

Layout Considerations

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Make all the connections for the power components in the top layer with wide, copper filled areas or polygons. In general, it is desirable to make proper use of power planes and polygons for power distribution and heat dissipation.

The inductor, output capacitors and the IR3838 should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place the input capacitor directly at the PVin pin of IR3838.

The feedback part of the system should be kept away from the inductor and other noise sources.

The critical bypass components such as capacitors for Vin, Vcc, Vref and Vp should be close to their respective pins. It is important to place the feedback components including feedback resistors and compensation components close to Fb and Comp pins.

The connection between the OCSet resistor and the SW pin should not share any trace with the connection between the bootstrap capacitor and the SW pin. Instead, it is recommended to use a Kelvin connection of the trace from the OCSet resistor and the trace from the bootstrap capacitor at the SW pin. Also, place the OCset resistor close to the device.

In a multilayer PCB use one layer as a power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point. It is recommended to place all the compensation parts over the analog ground plane in top layer.

The Power QFN is a thermally enhanced package. Based on thermal performance it is recommended to use at least a 4-layers PCB. To effectively remove heat from the device the exposed pad should be connected to the ground plane using vias. Figure 30 illustrates the implementation of the layout guidelines outlined above, on the IRDC3838 4 layer demoboard.

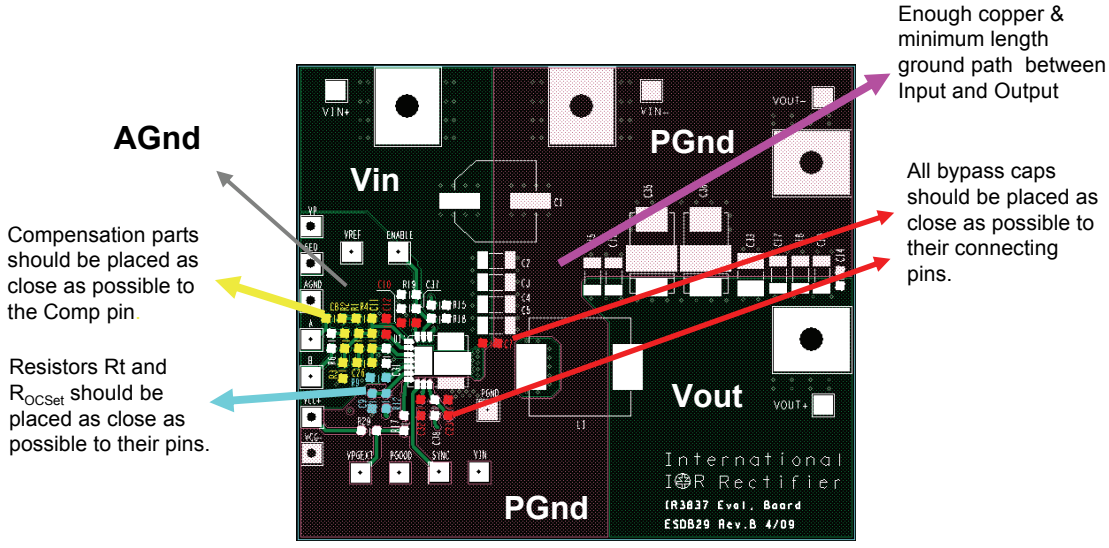


Fig. 30a. IRDC3838 Demoboard layout considerations – Top Layer

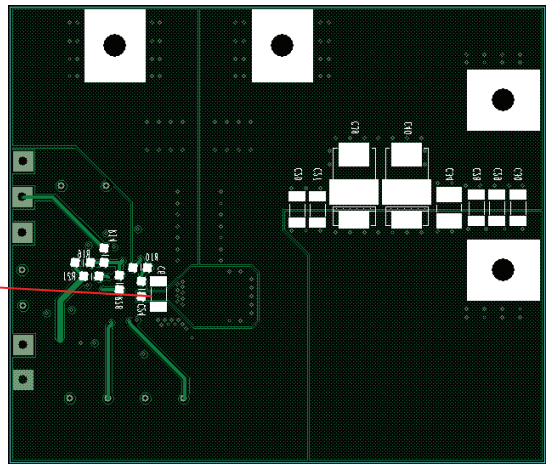


Fig. 30b. IRDC3838 demoboard layout considerations – Bottom Layer

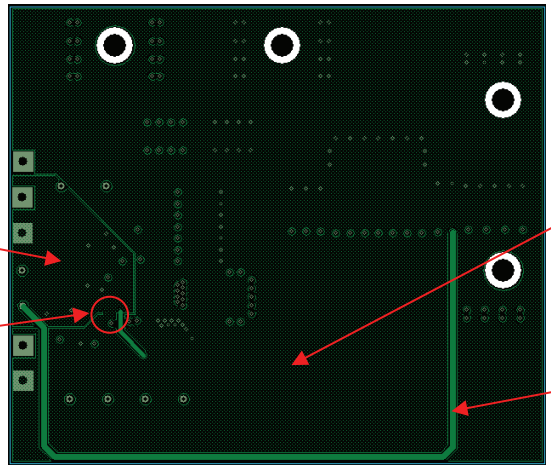


Fig. 30c. IRDC3838 demoboard layout considerations – Mid Layer 1

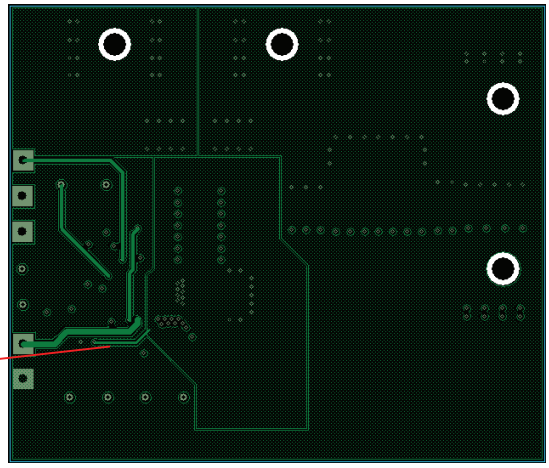
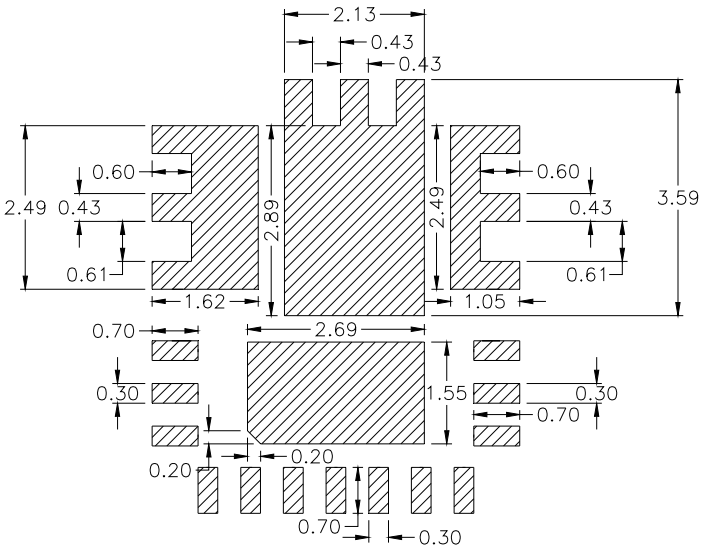


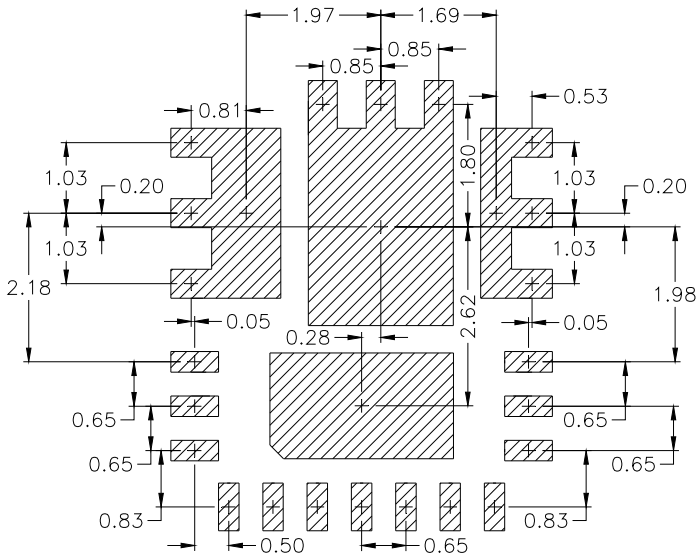
Fig. 30d. IRDC3838 demoboard layout considerations – Mid Layer 2

PCB Metal and Components Placement

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout as shown in following figures. PQFN devices should be placed to an accuracy of 0.050mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes. For further information, please refer to “SupIRBuck™ Multi-Chip Module (MCM) Power Quad Flat No-Lead (PQFN) Board Mounting Application Note.” (AN-1132)



PCB metal pad sizing (all dimensions in mm)



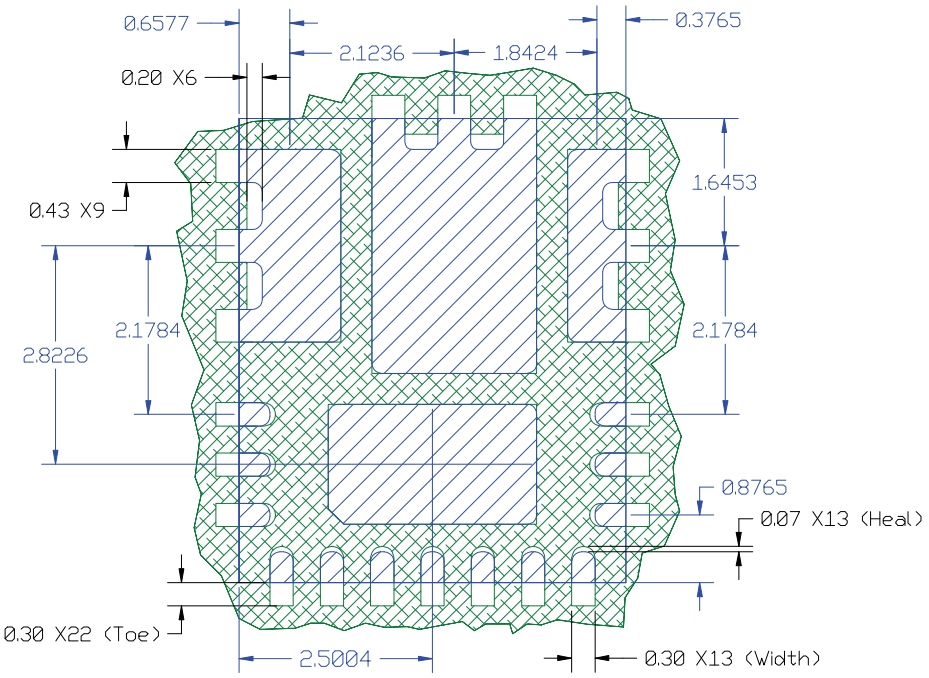
PCB metal pad spacing (all dimensions in mm)

Solder Resist

It is recommended that the lead lands are Non Solder Mask Defined (NSMD). The solder resist should be pulled away from the metal lead lands by a minimum of 0.025mm to ensure NSMD pads.

The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.05mm to accommodate solder resist mis-alignment.

Ensure that the solder resist in between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.



All Dimensions In mm
All Pads are Solder Mask Defined
Pad Center to Center dimensions

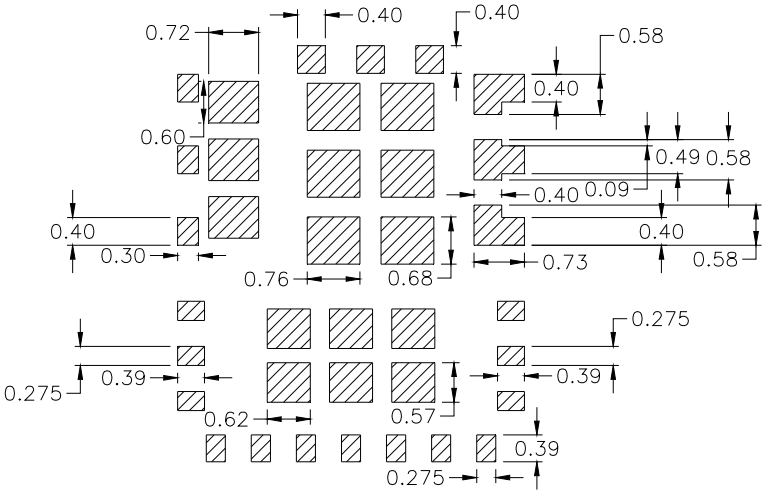
PCB Solder Resist

Component Pad

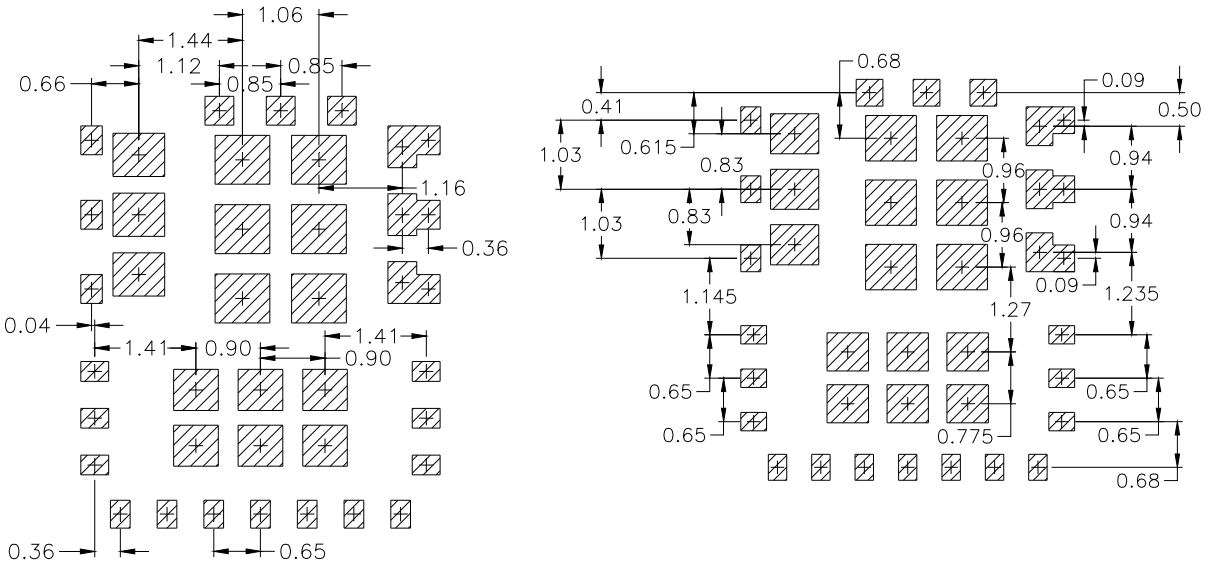
Stencil Design

Stencils for PQFN can be used with thicknesses of 0.100-0.250mm (0.004-0.010"). Stencils thinner than 0.100mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125mm-0.200mm (0.005-0.008"), with suitable reductions, give the best results.

Evaluations have shown that the best overall performance is achieved using the stencil design shown in following figure. This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.

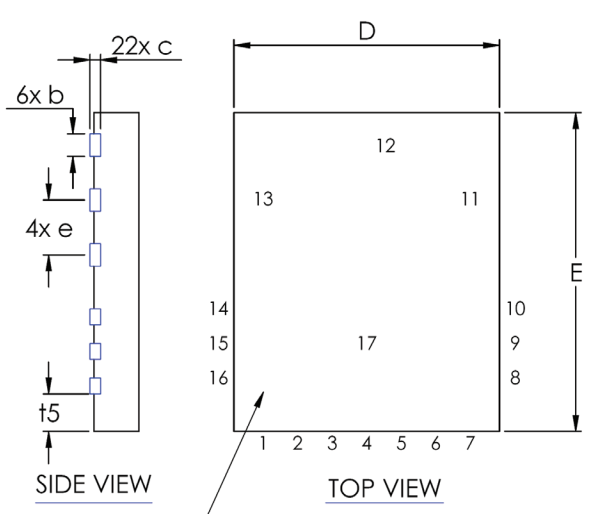


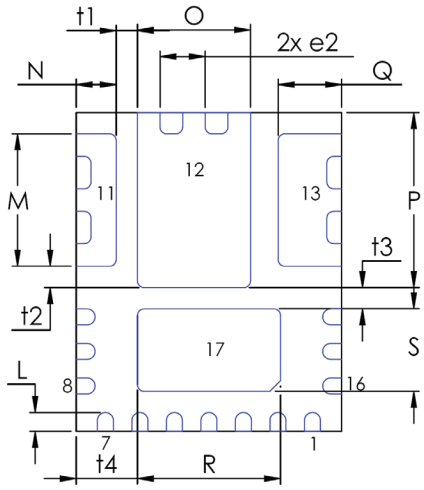
Stencil pad sizing (all dimensions in mm)

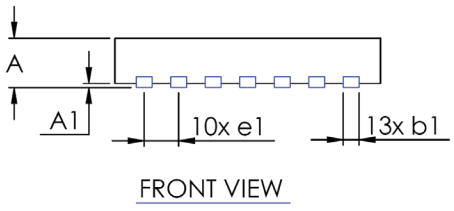


Stencil pad spacing (all dimensions in mm)

DIM	MILIMITERS		INCHES		DIM	MILIMITERS		INCHES	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	0.800	1.000	0.0315	0.0394	L	0.350	0.450	0.0138	0.0177
A1	0.000	0.050	0.0000	0.0020	M	2.441	2.541	0.0961	0.1000
b	0.375	0.475	0.1477	0.1871	N	0.703	0.803	0.0277	0.0316
b1	0.250	0.350	0.0098	0.1379	O	2.079	2.179	0.0819	0.0858
c	0.203 REF.		0.008 REF.		P	3.242	3.342	0.1276	0.1316
D	5.000 BASIC		1.969 BASIC		Q	1.265	1.365	0.0498	0.0537
E	6.000 BASIC		2.362 BASIC		R	2.644	2.744	0.1041	0.1080
e	1.033 BASIC		0.0407 BASIC		S	1.500	1.600	0.0591	0.0630
e1	0.650 BASIC		0.0256 BASIC		t1, t2, t3	0.401 BASIC		0.016 BACIS	
e2	0.852 BASIC		0.0335 BASIC		t4	1.153 BASIC		0.045 BASIC	
					t5	0.727 BASIC		0.0286 BASIC	







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This product has been designed and qualified for the Industrial market (*Note5*)
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