FEATURES

- Peak efficiency up to 94.0% at 1.2V
- Integrated driver, control MOSFET, synchronous MOSFET and Schottky diode
- Input voltage (VIN) operating range of 4.5V to 15V
- Separate LVCC and HVCC from 4.5V to 13.2V to optimize converter efficiency
- Output current capability of 45A DC
- Switching frequency up to 1.0MHz
- Programmable thermal flag threshold from 70°C to 150°C
- 5V VCC with under voltage lockout
- Low quiescent current
- Enable control
- Selectable regular 3.3V tri-state PWM logic or IR Active Tri-Level (ATL) PWM logic
- PCB footprint compatible with most IR3551 pins
- Efficient dual sided cooling
- Small 5mm x 6mm x 0.9mm PQFN package
- Lead free RoHS compliant package

APPLICATIONS

- Voltage Regulators for CPUs, GPUs, and DDR memory arrays
- High current, low profile DC-DC converters

DESCRIPTION

The IR3558 integrated PowIRstage® is a synchronous buck gate driver co-packed with a control MOSFET and a synchronous MOSFET with integrated Schottky diode. It is optimized internally for PCB layout, heat transfer and driver/MOSFET timing. Custom designed gate driver and MOSFET combination enables higher efficiency at lower output voltages required by cutting edge CPU, GPU and DDR memory designs.

Up to 1.0MHz switching frequency enables fast transient response, allowing miniaturization of output inductors as well as input and output capacitors while maintaining high efficiency. The IR3558's superior efficiency enables smallest size and lower solution cost. The IR3558 PCB footprint is compatible with most pins of the IR3551 (50A).

The IR3558 provides two selectable PWM logic modes, the 3.3V tri-state PWM logic or International Rectifier's Active Tri-Level™ (ATL) PWM logic. The ATL PWM logic eliminates a dedicated Body-Braking® pin and improves the transient response of the converter during load release.

The IR3558 provides a thermal flag output with programmable threshold from 70°C to 150°C, which makes it possible to adjust the thermal protection threshold based on the PCB layout and thermal distribution.

The IR3558 is optimized specifically for CPU core power delivery in server applications. The ability to meet the stringent requirements of the server market also makes the IR3558 ideally suited to powering GPU and DDR memory designs and other high current applications.

BASIC APPLICATION

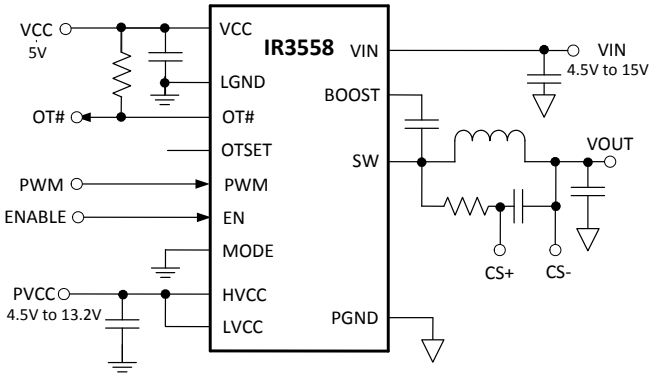


Figure 1: IR3558 Basic Application Circuit

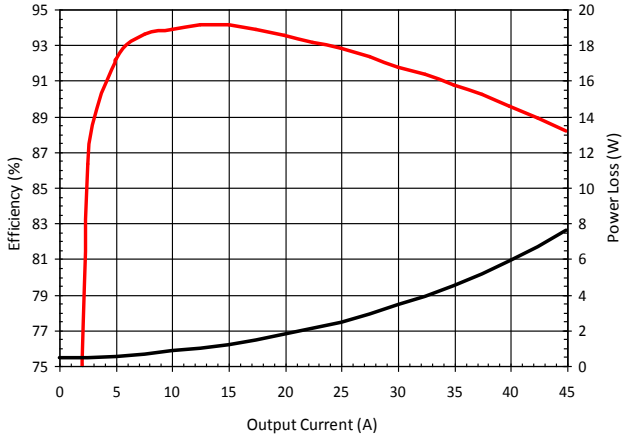


Figure 2: Typical IR3558 Efficiency & Power Loss (See Note 2 on Page 7)

PINOUT DIAGRAM

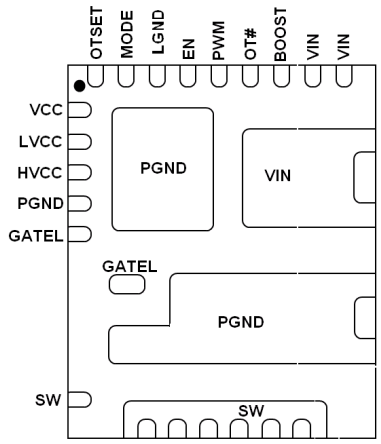


Figure 3: IR3558 Pin Diagram, Top View

ORDERING INFORMATION

Package	Tape & Reel Qty	Part Number
PQFN, 28 Lead 5mm x 6mm	4000	**IR3558MTRPBF**

TYPICAL APPLICATION DIAGRAM

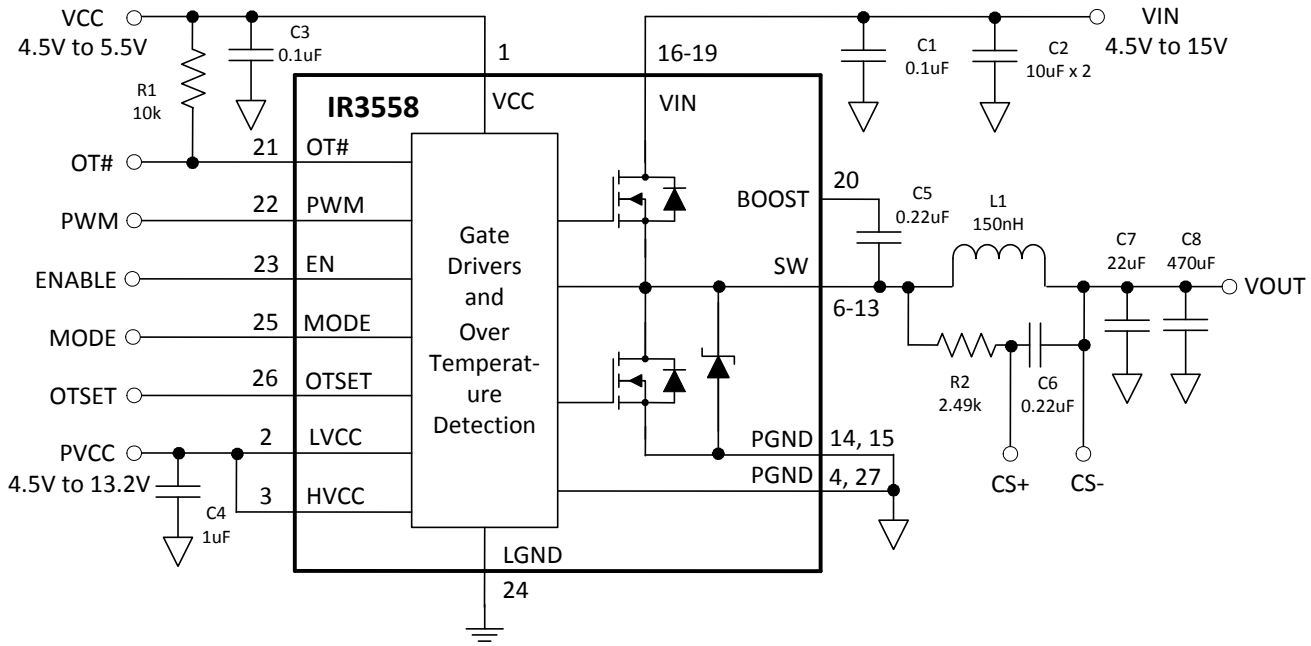


Figure 4: Application Circuit

FUNCTIONAL BLOCK DIAGRAM

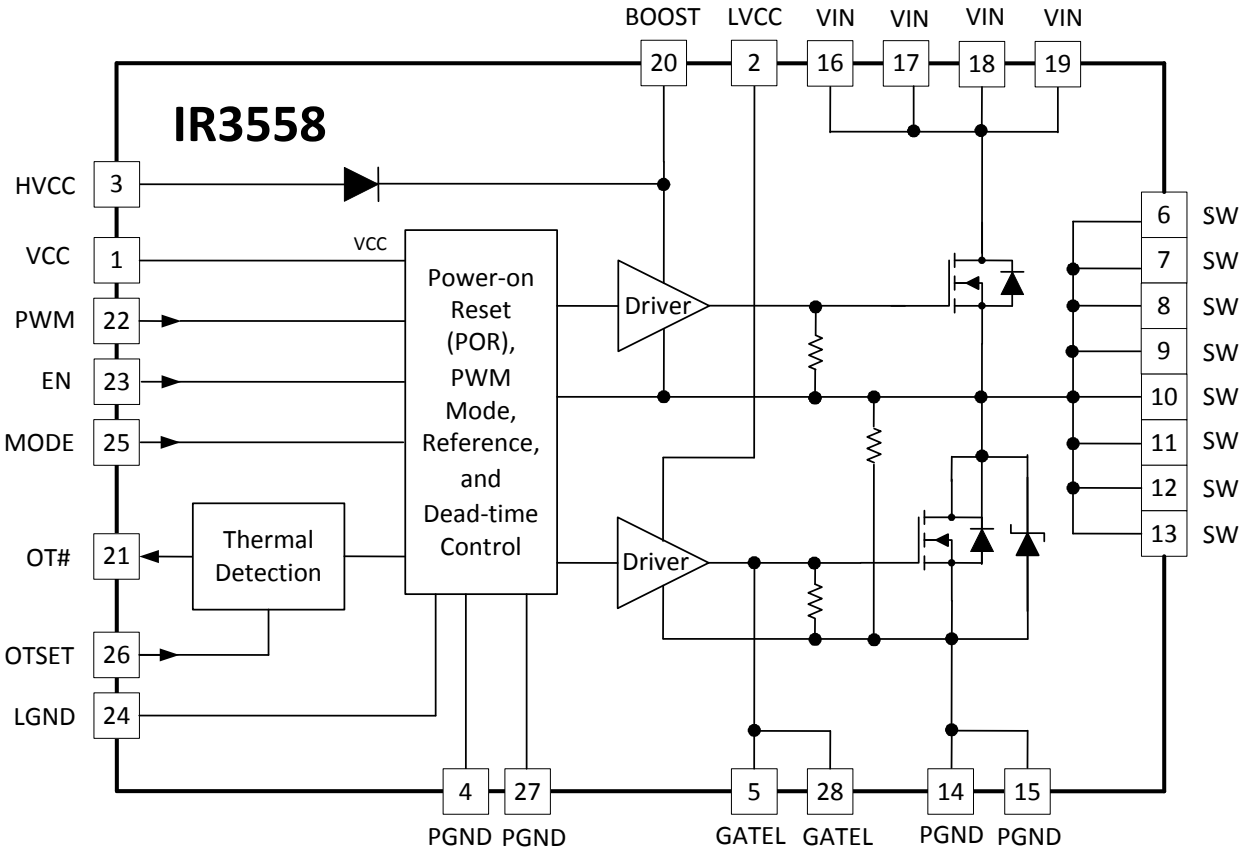


Figure 5: IR3558 Functional Block Diagram

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	VCC	Bias voltage for control logic. Connect VCC to a 5V supply. Connect a minimum 0.1uF capacitor between VCC and LGND.
2	LVCC	Supply voltage for the low-side driver. Connect LVCC to a 4.5V to 13.2V supply. Connect a minimum 0.1uF capacitor between LVCC and PGND (pin 4).
3	HVCC	Supply voltage for the high-side driver. Connect HVCC to a 4.5V to 13.2V supply. Connect a minimum 0.1uF capacitor between HVCC and PGND (pin 4).
4, 14, 15, 27	PGND	Power ground of low-side MOSFET driver and the synchronous MOSFET.
5, 28	GATEL	Low-side MOSFET driver pins that can be connected to a test point in order to observe the waveform.
6 – 13	SW	Switch node of synchronous buck converter.
16 – 19	VIN	High current input voltage connection. Recommended operating range is 4.5V to 15V. Connect at least two 10uF 1206 ceramic capacitors and a 0.1uF 0402 ceramic capacitor. Place the capacitors as close as possible to VIN pins and PGND pins (14-15). The 0.1uF 0402 capacitor should be on the same side of the PCB as the IR3558.
20	BOOST	Bootstrap capacitor connection. The bootstrap capacitor provides the charge to turn on the control MOSFET. Connect a minimum 0.22µF capacitor from BOOST to SW pin. Place the capacitor as close to BOOST pin as possible and minimize the parasitic inductance of the connection from the capacitor to SW pin. A 1Ω to 4Ω series resistor may be added to slow down the SW rising and limit the surge current into the bootstrap capacitor on start-up.
21	OT#	Open drain output of the phase fault circuits. Connect to an external pull-up resistor. Output is low when an over temperature condition inside the device is detected.
22	PWM	PWM control input. Connect this pin to the PWM output of a controller that outputs either a 3.3V tri-state PWM signal or a 1.8V International Rectifier's Active Tri-Level PWM signal.
23	EN	Enable control. 3.3V logic level input. Pulling this pin high to enable the device and grounding it to shut down both MOSFETs and enter low quiescent mode.
24	LGND	Signal ground. Driver control logic, analog circuits and IC substrate are referenced to this pin.
25	MODE	PWM mode selection. Grounding this pin to select the regular 3.3V tri-state PWM logic or connecting it to VCC to select International Rectifier's Active Tri-Level PWM logic.
26	OTSET	Over temperature set. The default is 150°C when this pin is floated. A resistor from this pin to ground programs the over temperature threshold from 70°C to 150°C. See "Over Temperature Threshold Set Resistor R_{OTSET}" Section for the resistor selection details.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PIN Number	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1	VCC	6.5V	-0.3V	NA	10mA
2	LVCC	15V	-0.3V	NA	1A for 100ns, 100mA DC
3	HVCC	15V	-0.3V	NA	1A for 100ns, 100mA DC
4, 27	PGND	0.3V	-0.3V	15mA	15mA
5, 28	GATEL	LVCC + 0.3V	-3V for 20ns, -0.3V DC	1A for 100ns, 200mA DC	1A for 100ns, 200mA DC
6-13	SW [2]	25V	-5V for 20ns, -0.3V DC	55A RMS	25A RMS
14, 15	PGND	NA	NA	25A RMS	55A RMS
16-19	VIN [2]	25V	-0.3V	5A RMS	20A RMS
20	BOOST [1]	35V	-0.3V	1A for 100ns, 100mA DC	5A for 100ns, 100mA DC
21	OT#	VCC + 0.3V	-0.3V	1mA	20mA
22	PWM	VCC + 0.3V	-0.3V	1mA	1mA
23	EN	VCC + 0.3V	-0.3V	1mA	1mA
24	LGND	0.3V	-0.3V	10mA	NA
25	MODE	VCC + 0.3V	-0.3V	1mA	1mA
26	OTSET	VCC + 0.3V	-0.3V	1mA	1mA

Note:
1. Maximum BOOST – SW = 15V.
2. Maximum VIN – SW = 25V.
3. All the maximum voltage ratings are referenced to PGND (Pins 14 and 15).

THERMAL INFORMATION	
Thermal Resistance, Junction to Top (θ_{JC_TOP})	18.2 °C/W
Thermal Resistance, Junction to PCB (pin 15) (θ_{JB})	2.6 °C/W
Thermal Resistance (θ_{JA})[1]	20.8 °C/W
Maximum Operating Junction Temperature	-40 to 150°C
Maximum Storage Temperature Range	-65°C to 150°C
ESD rating	HBM Class 1A JEDEC Standard
MSL Rating	3
Reflow Temperature	260°C

Note:
1. Thermal Resistance (θ_{JA}) is measured with the component mounted on a high effective thermal conductivity test board in free air. Refer to International Rectifier Application Note AN-994 for details.

ELECTRICAL SPECIFICATIONS

The electrical characteristics involve the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C.

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

PARAMETER	SYMBOL	MIN	MAX	UNIT
Recommended VIN Range	VIN	4.5	15	V
Recommended VCC Range	VCC	4.5	5.5	V
Recommended LVCC Range	LVCC	4.5	13.2	V
Recommended HVCC Range	HVCC	4.5	13.2	V
Recommended Switching Frequency	f_{SW}	200	1000	kHz
Recommended Operating Junction Temperature	T_J	-40	125	°C

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Efficiency						
PowIRstage Peak Efficiency	η	Note 2, Figure 2		94.0		%
		Note 3, Figure 8		93.0		%
PWM Tri-state Mode (Figure 6)						
PWM Input High Threshold	V_{PWM_HIGH}	PWM Tri-state to High	2.0	2.5	3.0	V
PWM Input Low Threshold	V_{PWM_LOW}	PWM Tri-state to Low	0.7	0.8	0.9	V
PWM Tri-state Float Voltage	V_{PWM_TRI}	PWM Floating	0.85	1.60	2.55	V
Hysteresis	V_{PWM_HYS}	Active to Tri-state or Tri-state to Active, Note 1		200		mV
Tri-state Hold OFF Time	T_{PWM_HOLD}	Note 1		80		ns
PWM Input Impedance	R_{PWM_SINK}		3.00	3.75	4.50	kΩ
Minimum Pulse Width	T_{PWM_MIN}	Note 1		40	60	ns
PWM Active Tri-Level (ATL) Mode (Figure 7)						
PWM Input High Threshold	V_{ATL_HIGH}		0.8	1.0	1.2	V
PWM Input High Threshold	V_{ATL_LOW}		0.65	0.8	0.95	V
PWM Tri-Level High Voltage	$V_{ATL_TRI_HIGH}$		2.1	2.5	2.9	V
PWM Tri-Level Low Voltage	$V_{ATL_TRI_LOW}$		2.00	2.30	2.42	V
PWM Input Current Low		V_{PWM} = 0V		-1.0	-1.5	mA
PWM Input Current High		V_{PWM} = 1.8V		-1.0	-1.5	mA
Enable Input – EN						
Input Voltage High	V_{N_H}		2.0			V
Input Voltage Low	V_{EN_L}				0.8	V
Input Current	I_{EN}	V(EN) = 5.5V		0.1	1	µA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Thermal Warning - OTSET Input and OT# Output						
Over Temperature High Threshold	OT	R_{OTSET} = open, Note 1		150		°C
Programmable Over Temperature High Threshold	OT	R_{OTSET} = 100kΩ, Note 1		125		°C
Over Temperature Hysteresis	OT_{HYS}	Note 1		-20		°C
OT# Sink Current			1.0	1.5		mA
OT# Output Low Voltage		1.5mA		0.4	1.0	V
Bootstrap Diode						
Forward Voltage	BD_{FV}	I(BOOST) = 30mA, LVCC = 6.8V	0.65	0.80	0.95	mV
VCC Under Voltage Lockout						
Start Threshold	V_{VCC_START}		3.5	3.8	4.1	V
Stop Threshold	V_{VCC_STOP}		3.2	3.5	3.8	V
Hysteresis	V_{VCC_HYS}		0.15	0.30	0.45	V
General						
VCC Supply Quiescent Current	I_{VCC}	V(VCC) = 5V, V(EN) =0V		1.5	2.5	mA
VCC Supply Current	I_{VCC_SW}	V(VCC) = 5V, V(EN) =5V		2.7	3.5	mA
LVCC Supply Quiescent Current	I_{LVCC}	V(LVCC) = 5V, V(EN) =0V		15	25	uA
		V(LVCC) = 7V, V(EN) =0V		20	30	uA
LVCC Supply Current	I_{LVCC_SW}	V(LVCC) = 5V, V(EN) =5V, fsw=400kHz		10	20	mA
		V(LVCC) = 7V, V(EN) =5V, fsw=400kHz		15	25	mA
HVCC Supply Quiescent Current	I_{BOOST}	V(HVCC) = 5V, V(EN) =0V		15	25	uA
		V(HVCC) = 7V, V(EN) =0V		20	30	uA
HVCC Supply Current	I_{BOOST_SW}	V(HVCC) =5V, V(EN) =5V, fsw=400kHz		5	10	mA
		V(HVCC) =7V, V(EN) =5V, fsw=400kHz		6.5	15	mA
VIN Supply Leakage Current	I_{VIN}	VIN = 20V, 125°C, V(PWM) = Tri-State			1	µA

Notes

1. Guaranteed by design but not tested in production
2. V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 300kHz, L=210nH (0.2mΩ), HVCC=LVCC=6.8V, C_{IN}=47uF x 4, C_{OUT} =470uF x3, 400LFM airflow, no heat sink, 25°C ambient temperature, and 8-layer PCB of 3.7" (L) x 2.6" (W). PWM controller loss and inductor loss are not included.
3. V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), HVCC=LVCC=7V, C_{IN}=47uF x 4, C_{OUT} =470uF x3, no airflow, no heat sink, 25°C ambient temperature, and 8-layer PCB of 3.7" (L) x 2.6" (W). PWM controller loss and inductor loss are not included.

TIMING DIAGRAMS

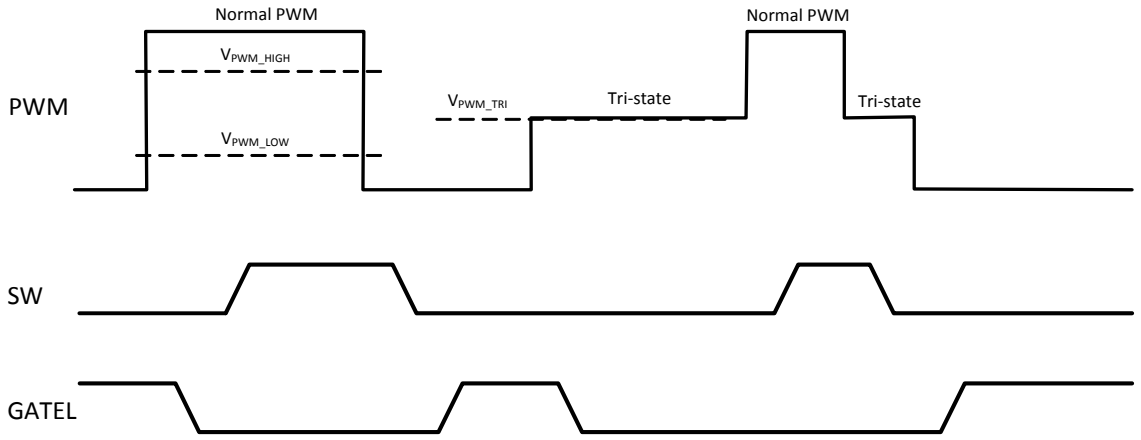


Figure 6: IR3558 Switching Waveforms in 3.3V Tri-state PWM Mode

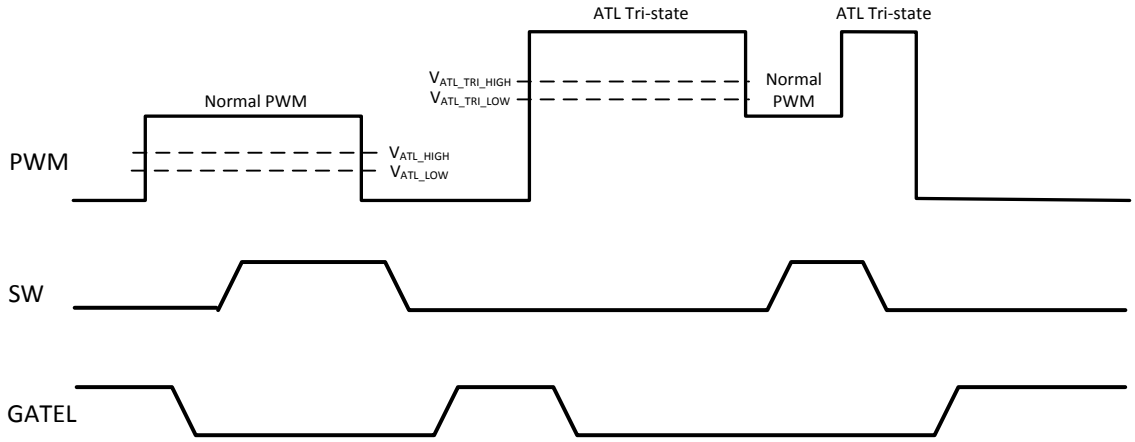


Figure 7: IR3558 Switching Waveforms in International Rectifier's Active Tri-Level® (ATL) PWM Mode

TYPICAL OPERATING CHARACTERISTICS

Circuit of Figure 32, V_{IN}=12V, V_{OUT}=1.2V, f_{SW}=400kHz, L=150nH (0.29mΩ), VCC=5V, HVCC=LVCC=7V, T_{AMB}=25°C, no heat sink, no air flow, 8-layer PCB board of 3.7" (L) x 2.6" (W), no PWM controller loss, no inductor loss, unless specified otherwise.

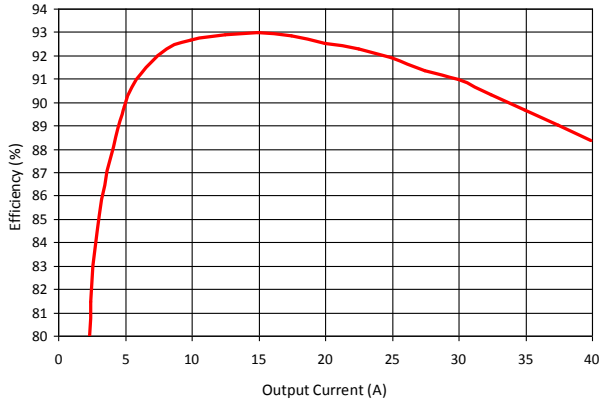


Figure 8: Typical IR3558 Efficiency

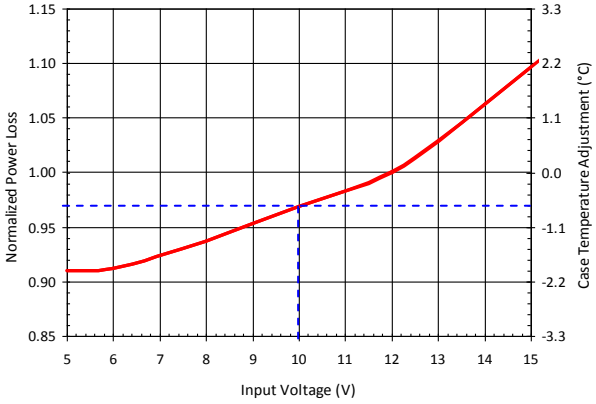


Figure 11: Normalized Power Loss vs. Input Voltage

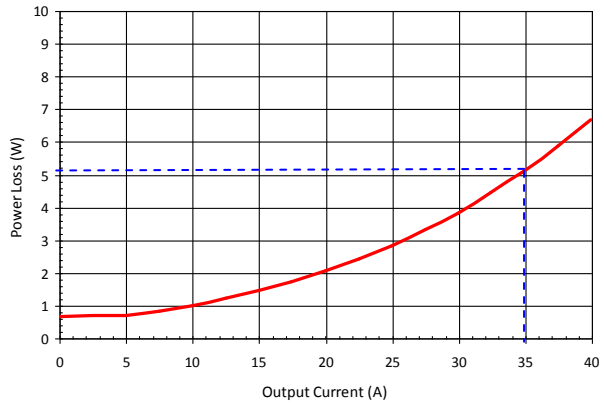


Figure 9: Typical IR3558 Power Loss

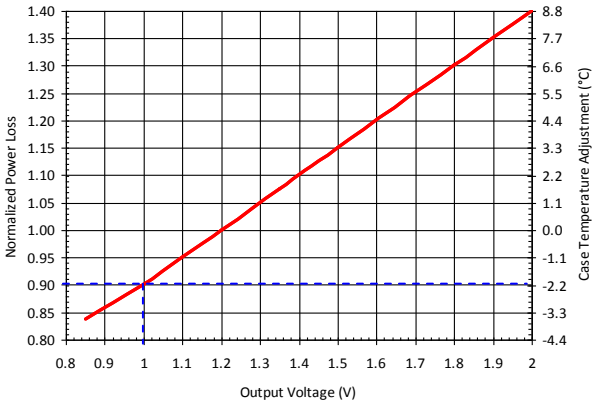


Figure 12: Normalized Power Loss vs. Output Voltage

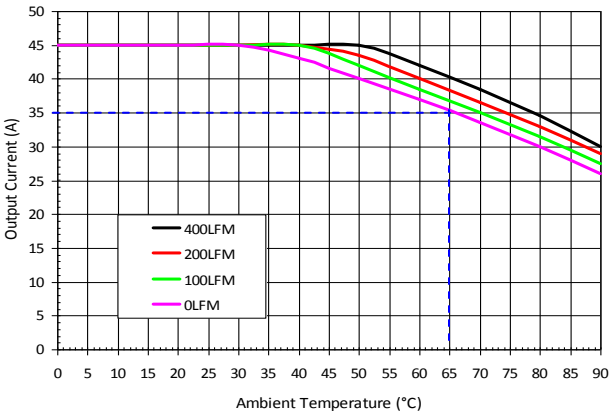


Figure 10: Safe Operating Area, T_{CASE} <= 125°C

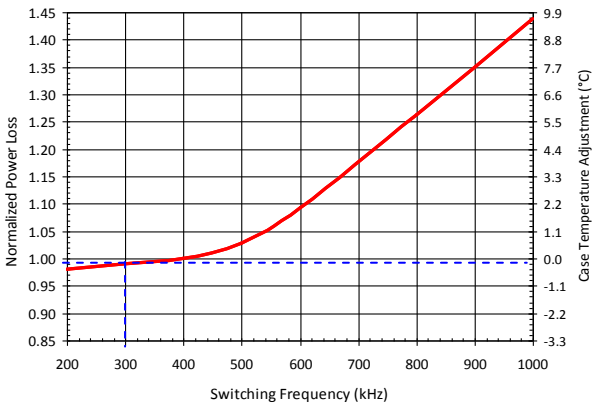


Figure 13: Normalized Power Loss vs. Switching Frequency

TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

Circuit of Figure 32, V_{IN}=12V, V_{OUT}=1.2V, f_{SW}=400kHz, L=150nH (0.29mΩ), VCC=5V, HVCC=LVCC=7V, T_{AMB}=25°C, no heat sink, no air flow, 8-layer PCB board of 3.7" (L) x 2.6" (W), no PWM controller loss, no inductor loss, unless specified otherwise.

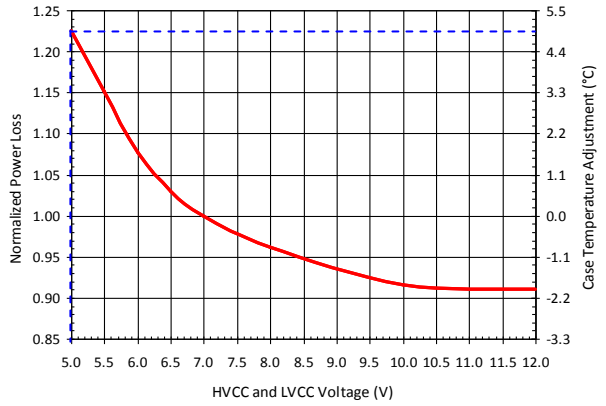


Figure 14: Normalized Power Loss vs. HVCC & LVCC Voltage

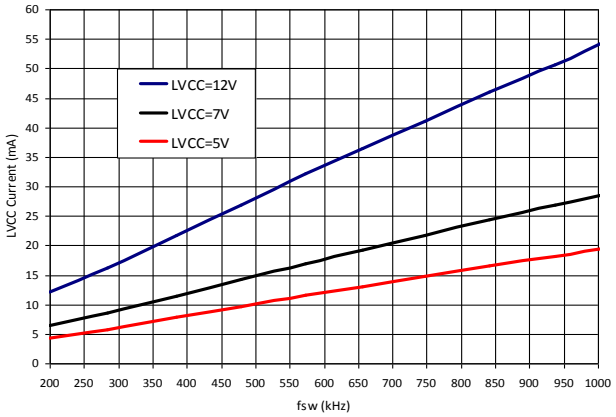


Figure 17: LVCC Current vs. Switching Frequency

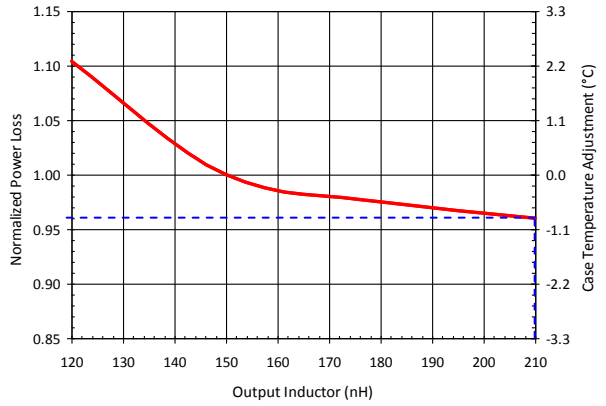


Figure 15: Power Loss vs. Output Inductor

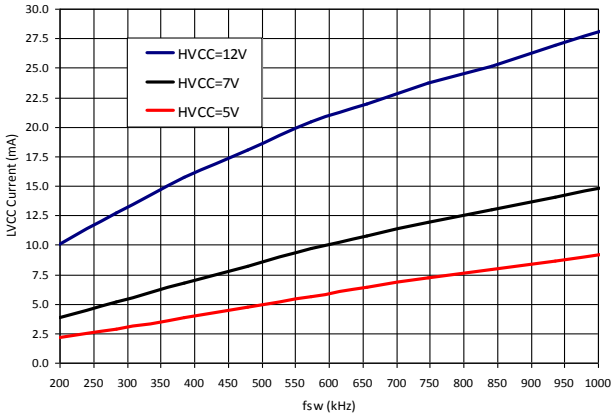


Figure 18: HVCC Current vs. Switching Frequency

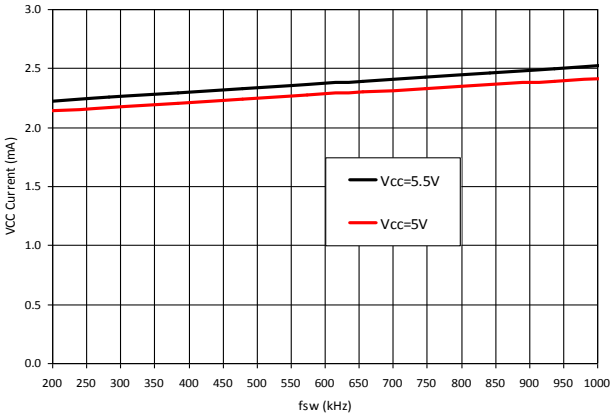


Figure 16: VCC Current vs. Switching Frequency

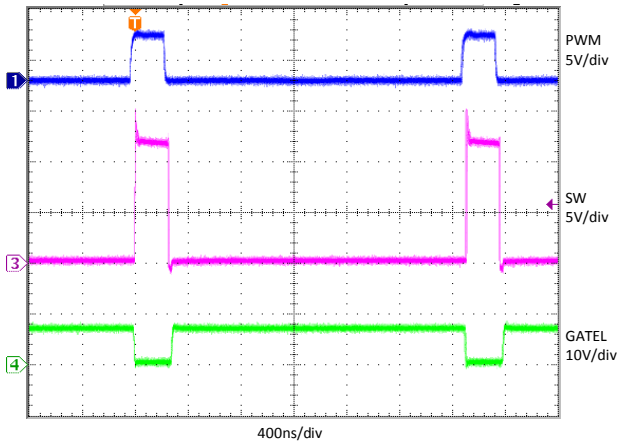


Figure 19: Switching Waveform in Tri-state Mode, I_{OUT} = 0A

TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

Circuit of Figure 32, V_{IN}=12V, V_{OUT}=1.2V, f_{SW}=400kHz, L=150nH (0.29mΩ), VCC=5V, HVCC=LVCC=7V, T_{AMB}=25°C, no heat sink, no air flow, 8-layer PCB board of 3.7" (L) x 2.6" (W), no PWM controller loss, no inductor loss, unless specified otherwise.

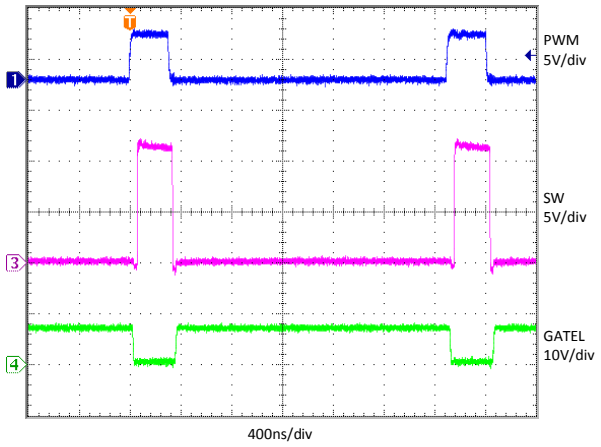


Figure 20: Switching Waveform in Tri-state Mode, I_{OUT} = 40A

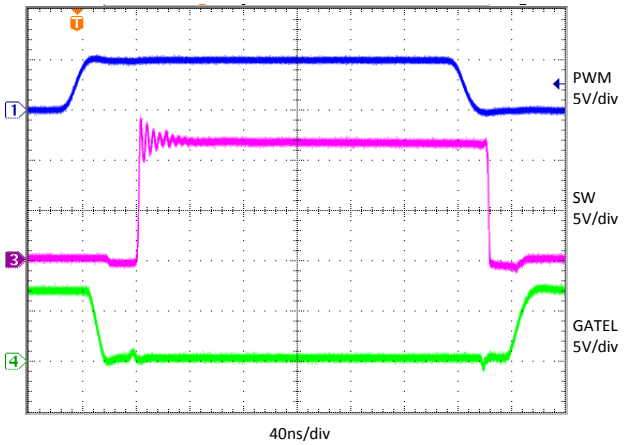


Figure 21: PWM to SW Delays in Tri-state Mode, I_{OUT} = 10A

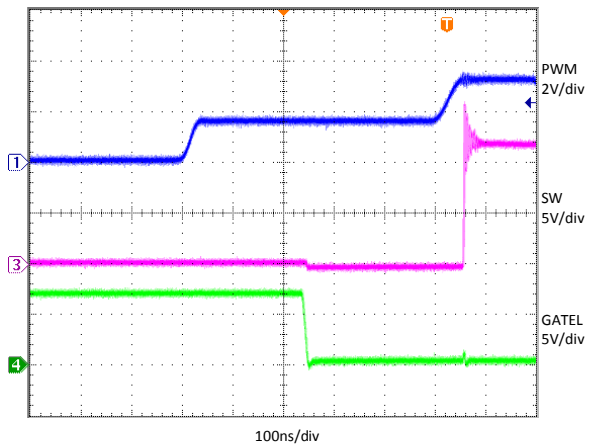


Figure 22: PWM Tri-state Delays in Tri-state Mode, I_{OUT} = 10A

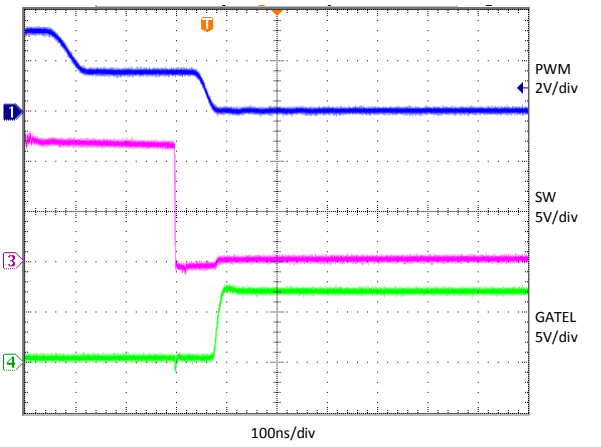


Figure 23: PWM Tri-state Delays in Tri-state Mode, I_{OUT} = 10A

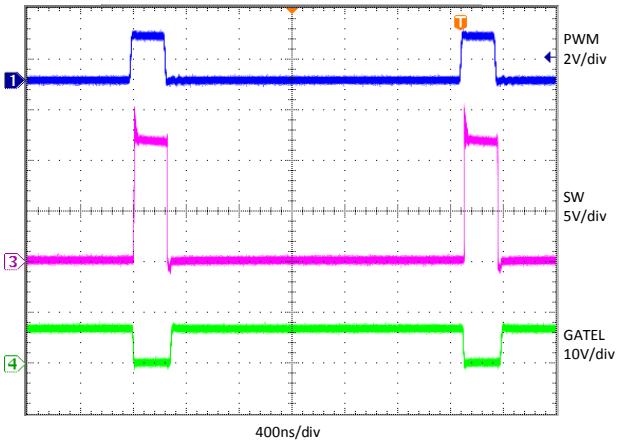


Figure 24: Switching Waveform in ATL Mode, I_{OUT} = 0A

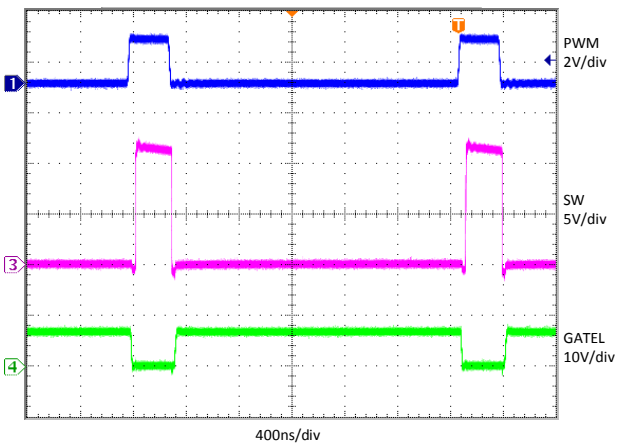


Figure 25: Switching Waveform in ATL Mode, I_{OUT} = 40A

TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

Circuit of Figure 32, V_{IN}=12V, V_{OUT}=1.2V, f_{SW}=400kHz, L=150nH (0.29mΩ), VCC=5V, HVCC=LVCC=7V, T_{AMB}=25°C, no heat sink, no air flow, 8-layer PCB board of 3.7" (L) x 2.6" (W), no PWM controller loss, no inductor loss, unless specified otherwise.

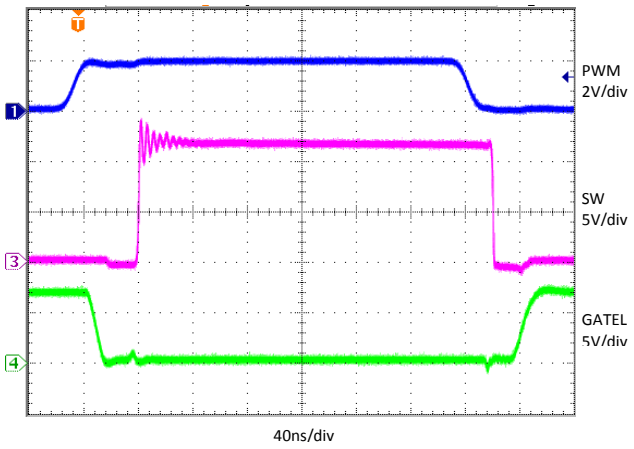


Figure 26: PWM to SW Delays in ATL Mode, I_{OUT} = 10A

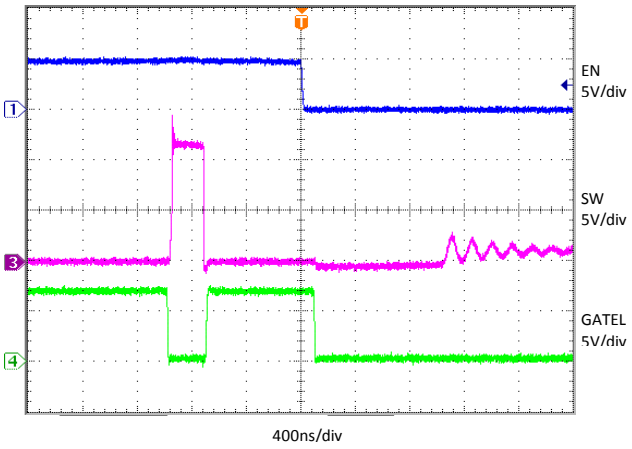


Figure 29: EN Disable Delay, I_{OUT} = 0A

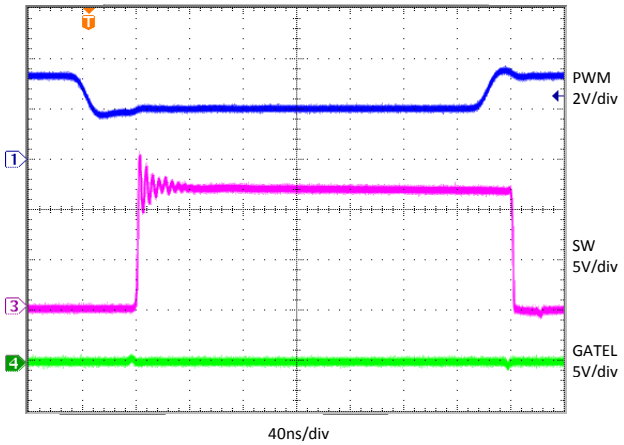


Figure 27: PWM Tri-state Delays in ATL Mode, I_{OUT} = 10A

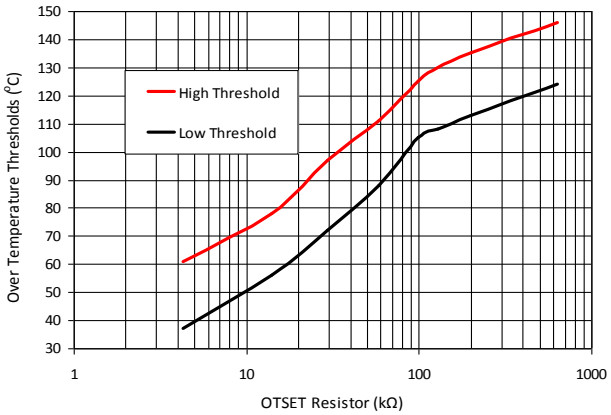


Figure 30: Over Temperature Threshold vs. OTSET Resistor

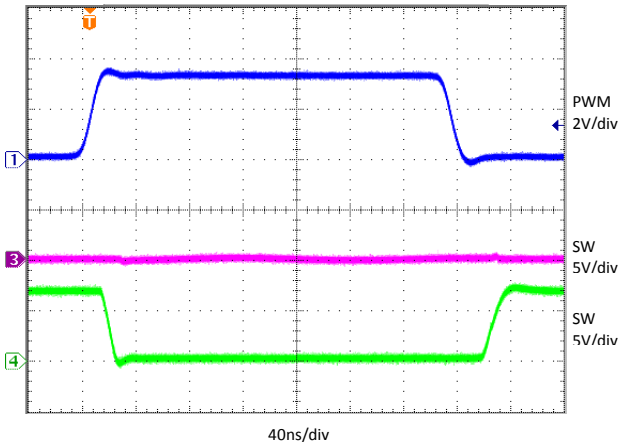


Figure 28: PWM Tri-state Delays in ATL Mode, I_{OUT} = 0A

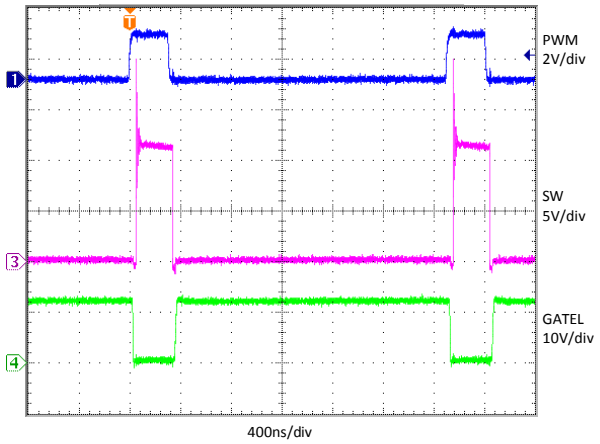


Figure 31: Switching Waveform, I_{OUT} = 40A, HVCC = LVCC = 12V

THEORY OF OPERATION

DESCRIPTION

The IR3558 PowIRstage® is a synchronous buck driver with co-packed MOSFETs with integrated Schottky diode, which provides system designers with ease of use and flexibility required in cutting edge CPU, GPU and DDR memory power delivery designs and other high-current low-profile applications.

The IR3558 is designed to work with a PWM controller. It accepts either regular 3.3V tri-state PWM signal or International Rectifier's Active Tri-Level (ATL) PWM signal, which is selectable by MODE pin.

The IR3558 provides Enable input to control the converter output and reduce quiesecent current.

The IR3558 provides a over temperature fault signal capable of detecting an over-temperature condition in the vicinity of the power stage. The over-temperature threshold is programmable from 70°C to 150°C.

PWM MODE SELECTION

The IR3558 features a MODE pin which allows operation with two different PWM signal levels. Grounding the MODE pin allows the IR3558 to accept a regular tri-state PWM with signal from 0V to 3.3V for low to high transitions. A PWM voltage level in the tri-state window of 0.85V and 2.55V for 80ns hold off time results in turning off both the control and synchronous MOSFETs. Floating MODE pin or connecting it to VCC enables the IR3558 to accept IR's proprietary ATL mode, in which the PWM voltage level is from 0V to 1.8V for low to high transitions. A PWM voltage level greater than the tri-state high threshold (2.5V typical) turns off both the control and synchronous MOSFETs.

REGULAR 3.3V PWM MODE

If MODE pin is grounded, the IR3558 accepts regular 3-level 3.3V PWM input signals. As shown in Figure 6, when PWM input is above V_{PWM_HIGH}, the synchronous MOSFET is turned off and the control MOSFET is turned on. When PWM input is below V_{PWM_LOW}, the control MOSFET is turned off and synchronous MOSFET is turned on. If PWM pin is floated, the built-in resistors pull the PWM pin into a tri-state region centered around 1.6V. Figures 19-23 show the PWM input and the corresponding SW and GATEL output of the IR3558.

ACTIVE TRI-LEVEL PWM MODE

When MODE pin is floating, the IR3558 accepts a unique tri-level PWM control signal provided by an IR digital PWM controller. As shown in Figure 7, the rising and falling edges of the PWM signal transition between 0V and 1.8V to switch both the control and synchronous MOSFETs during normal PWM operation. To turn both MOSFETs off simultaneously, the PWM signal crosses a tri-state voltage level higher than the $V_{ATL_TRI_HIGH}$ threshold (2.5V typical). This threshold based tri-state results in a very fast disable with only a small propagation delay. MOSFET switching resumes when the PWM signal falls below the $V_{ATL_TRI_LOW}$ threshold (2.3V typical) into the normal PWM operating voltage range. Figures 24-28 show the PWM input and the corresponding SW and GATEL output of the IR3558.

This fast tri-state operation eliminates the need for the PWM signal to dwell in the shutdown window, eliminating the delay time created by the PWM pull-up and pull-down resistors with the PWM trace routing capacitance. A dedicated Body-Braking® pin is not required, which simplifies the routing and layout.

One advantage of the ATL is the ability to quickly turn-off all synchronous MOSFETs during a load release event. This is known as Body-Braking® since all the load current is forced to flow momentarily through the body diodes of the MOSFETs, which discharges the inductor current faster and results in a much lower overshoot on the output voltage.

The IR3558 provides a 1mA typical pull-up current to drive the PWM input to the tri-state condition of 3.3V when the PWM controller output is in its high impedance state. The 1mA typical current is designed for driving worst case stray capacitances and transition the IR3558 into the tri-state condition rapidly to avoid a prolonged period of conduction of the control or synchronous MOSFET during faulty conditions. Once the PWM signal has been pulled up, the 1mA current is disabled to reduce power consumption.

ENABLE CONTROL

EN is a 3.3V logic input. Logic low disables PWM operation and places the power stage in tri-state, as shown in Figure 29. It also places the driver in a low power state with minimum quiescent current. Logic high enables the device.

INTEGRATED BOOTSTRAP DIODE

The bootstrap circuit is used to establish the gate voltage for the high-side driver. It consists of a diode and capacitor

connected between the SW and BOOST pins of the device. The bootstrap capacitor stores the charge and provides the voltage required to drive the internal control MOSFET gate.

The IR3558 features an integrated bootstrap diode to reduce external component count. This enables the IR3558 to be used effectively in cost and space sensitive designs. For ultra high efficiency designs, an external bootstrap diode in parallel with the integrated bootstrap diode is recommended.

A series resistor, 1Ω to 4Ω, may be added to slow down the SW rising and limit the surge current into the bootstrap capacitor on start-up.

ADJUSTABLE OVER TEMPERATURE THRESHOLD

In a single phase regulator, over temperature of the power stage can happen due to the over current, inductor saturation or other faulty conditions. In a multiphase voltage regulator, differences in temperature from phase to phase can occur due to current unbalance, mismatched thermal solutions, airflow, surrounding components or manufacturing errors and can often cause poor efficiency or even system failures if not monitored.

The IR3558 detects the die temperature of its internal MOSFET driver. The OTSET feature allows the user to adjust the over temperature threshold from 70°C to 150°C using a simple resistor between OTSET pin and ground. The equation defining the over temperature threshold, T_{OTSET} as a function of R_{OTSET} is:

$$T_{OTSET} = 150°C - 89°C * \frac{38k\Omega}{38k\Omega + R_{OTSET}}$$

Leaving the OTSET pin open will set the over temperature threshold at the default 150°C. Figure 30 shows the values of R_{OTSET} chosen as a function of the desired over temperature threshold.

The OT# flag is an open drain signal and is active low as the temperature of the IR3558 die exceeds the OTSET threshold. The OT# becomes high once the IR3558 temperature drops by the 20°C hysteresis. The OT# pin can be tied to a system level Enable to implement an over-temperature shutdown feature in a voltage regulator. To monitor all the phases in a multiphase system, tie the OT# of all IR3558 together and connect it to system Enable.

If OT# is not used it can be floated or connected to LGND.

ADJUSTABLE HVCC AND LVCC DRIVE VOLTAGES

HVCC and LVCC voltages can be independently adjusted to optimize high-side and low-side MOSFET efficiency respectively. Both voltage ranges are from 4.5V to 13.2V. Higher HVCC and LVCC gate drive voltages improve efficiency at heavy load but lower efficiency at light load. Higher HVCC voltage also causes undesirable higher switching node spike, as shown in Figure 31.

DESIGN PROCEDURES

POWER LOSS CALCULATION

The single-phase IR3558 efficiency and power loss measurement circuit is shown in Figure 32.

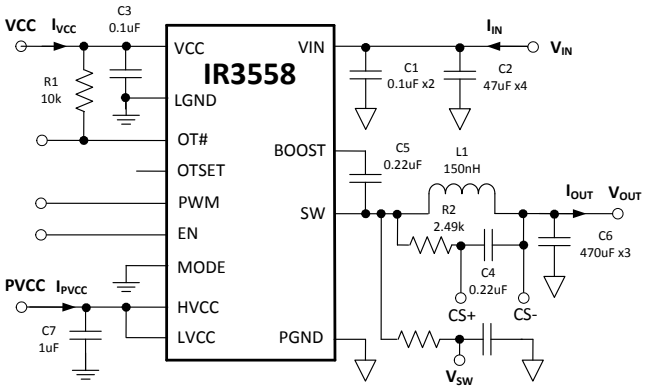


Figure 32: IR3558 Power Loss Measurement

The IR3558 power loss is determined by,

$$P_{LOSS} = V_{IN} \times I_{IN} + V_{CC} \times I_{VCC} + V_{PVCC} \times I_{PVCC} - V_{SW} \times I_{OUT}$$

Where both MOSFET loss and the driver loss are included, but the PWM controller and the inductor losses are not included.

Figure 8 shows the measured single-phase IR3558 efficiency under the default test conditions, V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), PVCC (HVCC/ LVCC) = 7V, $T_{AMBIENT}$ = 25°C, no heat sink, and no air flow.

The efficiency of an interleaved multiphase IR3558 converter is always higher than that of a single-phase under the same conditions due to the reduced input RMS current and more input/output capacitors.

The measured single-phase IR3558 power loss under the same conditions is provided in Figure 9.

If any of the application condition, i.e. input voltage, output voltage, switching frequency, PVCC (HVCC/LVCC) MOSFET driver voltage or inductance, is different from those of Figure 9, a set of normalized power loss curves should be used. Obtain the normalizing factors from Figures 11-15 for the new application conditions; multiply these factors by the power loss obtained from Figure 9 for the required load current.

As an example, the power loss calculation procedures under different conditions, V_{IN}=10V, V_{OUT}=1V, f_{SW} = 300kHz, L=210nH, PVCC (HVCC/LVCC) = 5V, I_{OUT}=35A, $T_{AMBIENT}$ = 25°C, no heat sink, and no air flow, are as follows.

1) Determine the power loss at 35A under the default test conditions of V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH, PVCC (HVCC/LVCC) = 7V, $T_{AMBIENT}$ = 25°C, no heat sink, and no air flow. It is 5.2W from Figure 9.

2) Determine the input voltage normalizing factor with V_{IN}=10V, which is 0.97 based on the dashed lines in Figure 11.

3) Determine the output voltage normalizing factor with V_{OUT}=1V, which is 0.90 based on the dashed lines in Figure 12.

4) Determine the switching frequency normalizing factor with f_{SW} = 300kHz, which is 0.99 based on the dashed lines in Figure 13.

5) Determine the MOSFET drive voltage normalizing factor with PVCC (HVCC/LVCC) = 5V, which is 1.22 based on the dashed lines in Figure 14.

6) Determine the inductance normalizing factor with L=210nH, which is 0.96 based on the dashed lines in Figure 15.

7) Multiply the power loss under the default conditions by the five normalizing factors to obtain the power loss under the new conditions, which is 5.2W x 0.97 x 0.90 x 0.99 x 1.22 x 0.96 = 5.3W.

SAFE OPERATING AREA

Figure 10 shows the IR3558 safe operating area with the case temperature controlled at or below 125°C. The test conditions are V_{IN}=12V, V_{OUT}=1.2V, f_{SW}=400kHz, L=150nH (0.29mΩ), HVCC=LVCC=7V, $T_{AMBIENT}$ = 0°C to 90°C, no heat sink, and Airflow = 0LFM / 100LFM / 200LFM / 400LFM.

If any of the application condition, i.e. input voltage, output voltage, switching frequency, HVCC/LVCC MOSFET driver voltage, or inductance is different from those of Figure 10, a set of IR3558 case temperature adjustment curves should be used. Obtain the temperature deltas from Figures 11-15 for the new application conditions; sum these deltas and then subtract from the IR3558 case temperature obtained from Figure 10 for the required load current.

The IR3558 safe operating area is obtained with the case temperature controlled at or below 125°C. If a lower case temperature is desired, reduce the highest ambient temperature by the same delta.

As an example, the highest ambient temperature calculation procedures for a different operating condition, V_{IN}=10V, V_{OUT}=1V, f_{SW} = 300kHz, L=210nH, PVCC (HVCC/LVCC) = 5V, I_{OUT}=35A, $T_{AMBIENT}$ = 25°C, no heat sink, and no air flow, are as follows.

8) From Figure 10, determine the highest ambient temperature at the required load current under the default conditions, which is 65°C at 35A with 0LFM airflow and the IR3558 case temperature of 125°C.

9) Determine the case temperature with V_{IN}=10V, which is -0.7° based on the dashed lines in Figure 11.

10) Determine the case temperature with V_{OUT}=1V, which is -2.2° based on the dashed lines in Figure 12.

11) Determine the case temperature with f_{SW} = 300kHz, which is -0.2° based on the dashed lines in Figure 13.

12) Determine the case temperature with PVCC (HVCC/LVCC) = 5V, which is +4.9° based on the dashed lines in Figure 14.

13) Determine the case temperature with L=210nH, which is -0.9° based on the dashed lines in Figure 15.

14) Sum the case temperature adjustment from 9) to 13), -0.7° -2.2° -0.2° +4.9° -0.9° = +0.9°. Deduct the delta from the highest ambient temperature in step 8), 65°C - (+0.9°C) = 64.1°C.

15) If the desired IR3558 case temperature is 105°C instead of 125°C, subtract 20°C (=125°C - 105°C) from the highest ambient temperature obtained from 14), i.e. 64.1°C - 20°C = 44.1°C.

OVER TEMPERATURE THRESHOLD SET RESISTOR R_{OTSET}

Decide the desired over temperature threshold, T_{OTSET}, based on the system requirement. Leaving the OTSET pin open will set the over temperature threshold at the 150°C. If the desired over temperature threshold is between 70°C and 150°C, use the following equation to calculate the OTSET resistor R_{OTSET}.

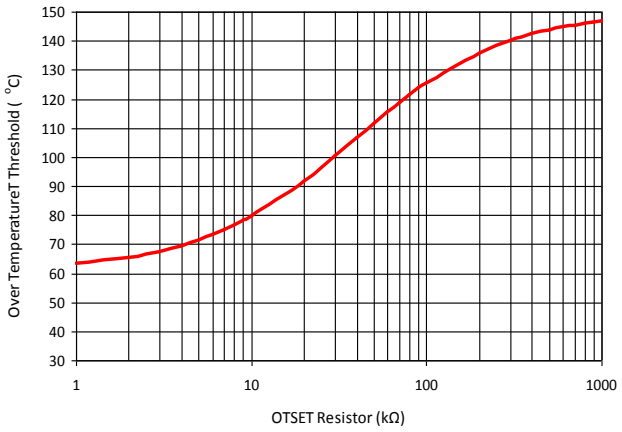


Figure 33: Over Temperature Threshold vs. ORSET Resistor

$$R_{OTSET} = \frac{38k\Omega * 89°C}{150°C - T_{OTSET}} - 38k\Omega$$

Figure 33 can also be used to determine the values of R_{OTSET}. A 1% or better resistor should be used for the best accuracy.

INPUT CAPACITORS C_{VIN}

At least two 10uF 1206 ceramic capacitors and one 0.1uF 0402 ceramic capacitor are recommended for decoupling the VIN to PGND connection. The 0.1uF 0402 capacitor should be on the same side of the PCB as the IR3558 and next to the VIN and PGND pins. Adding additional capacitance and use of capacitors with lower ESR and mounted with low inductance routing will improve efficiency and reduce overall system noise, especially in single-phase designs or during high current operation.

BOOTSTRAP CAPACITOR C_{BOOST}

A minimum of 0.22uF 0402 capacitor is required for the bootstrap circuit. A high temperature 0.22uF or greater value 0402 capacitor is recommended. It should be mounted on the same side of the PCB as the IR3558 and as close as possible to the BOOST pin. A low inductance routing of the SW pin connection to the other terminal of the bootstrap capacitor is strongly recommended.

A series resistor, 1Ω to 4Ω, may be added to slow down the SW rising and limit the surge current into the bootstrap capacitor on start-up.

VCC, HVCC AND LVCC DECOUPLING CAPACITORS C_{VCC}, C_{HVCC} AND C_{LVCC}

A 0.1uF ceramic decoupling capacitor is required at the VCC pin. A 0.1uF to 1uF ceramic decoupling capacitor is required at the HVCC or LVCC pin. They should be mounted on the same side of the PCB as the IR3558. The VCC capacitor should be as close as possible to the VCC and LGND. The HVCC and LVCC capacitors should be as close as possible to HVCC/LVCC and PGND (pin 4). Low inductance routing for the decoupling capacitors is strongly recommended.

MOUNTING OF HEAT SINKS

Care should be taken in the mounting of heat sinks so as not to short-circuit nearby components. The VCC and bootstrap capacitors are typically mounted on the same side of the PCB as the IR3558. The mounting height of these capacitors must be considered when selecting their package sizes.

HIGH OUTPUT VOLTAGE DESIGN CONSIDERATIONS

The IR3558 is capable of creating output voltages above the 3.3V recommended maximum output voltage as there are no restrictions inside the IR3558 on the duty cycle applied to the PWM pin. However the output current rating of the device will be reduced as the duty cycle increases. In very high duty cycle applications sufficient time must be provided for replenishment of the Bootstrap capacitor for the control MOSFET drive.

LAYOUT EXAMPLE

Contact International Rectifier for a layout example suitable for your specific application.

METAL AND COMPONENT PLACEMENT

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to prevent shorting.
- Lead land length should be equal to maximum part lead length +0.15 - 0.3 mm outboard extension and 0 to + 0.05mm inboard extension. The outboard extension ensures a large and visible toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width.
- Only 0.30mm diameter via shall be placed in the area of the power pad lands and connected to power planes to minimize the noise effect on the IC and to improve thermal performance.

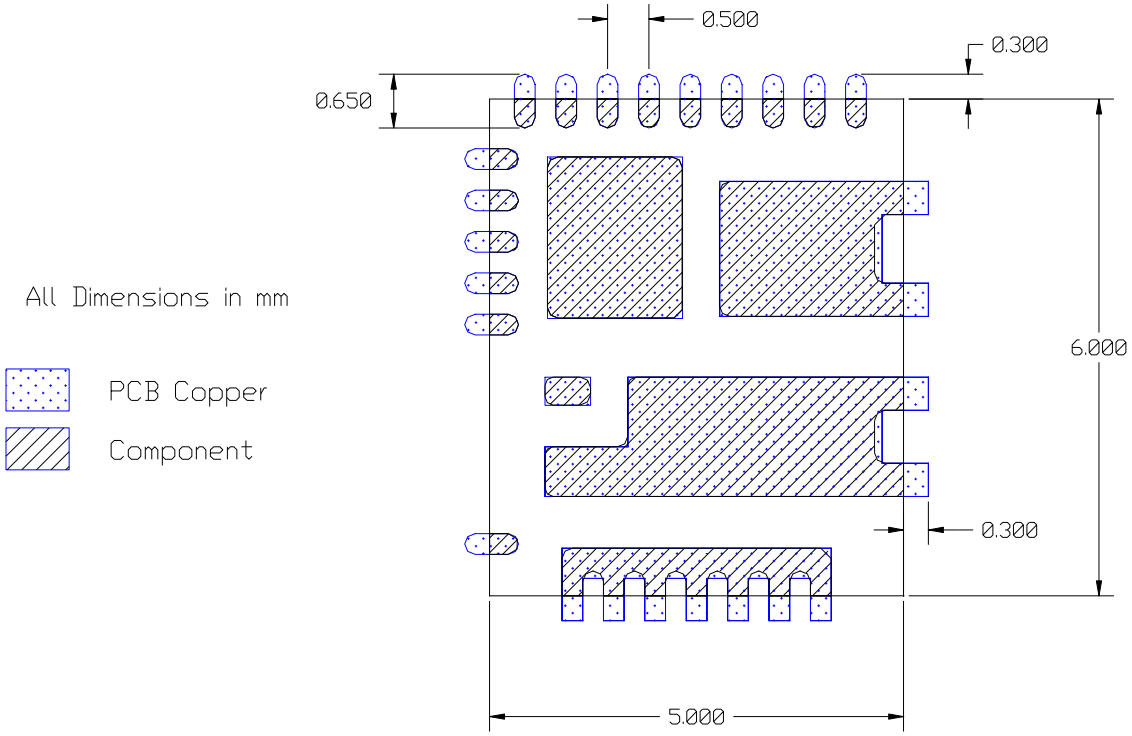


Figure 34: Metal and component placement

* Contact International Rectifier to receive an electronic PCB Library file in Cadence Allegro or CAD DXF/DWG format.

SOLDER RESIST

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist miss-alignment is a maximum of 0.05mm and it is recommended that the low power signal lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm typical.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The dimensions of power land pads, VIN, PGND, and SW, are Non Solder Mask Defined (NSMD). The equivalent PCB layout becomes Solder Mask Defined (SMD) after power shape routing.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

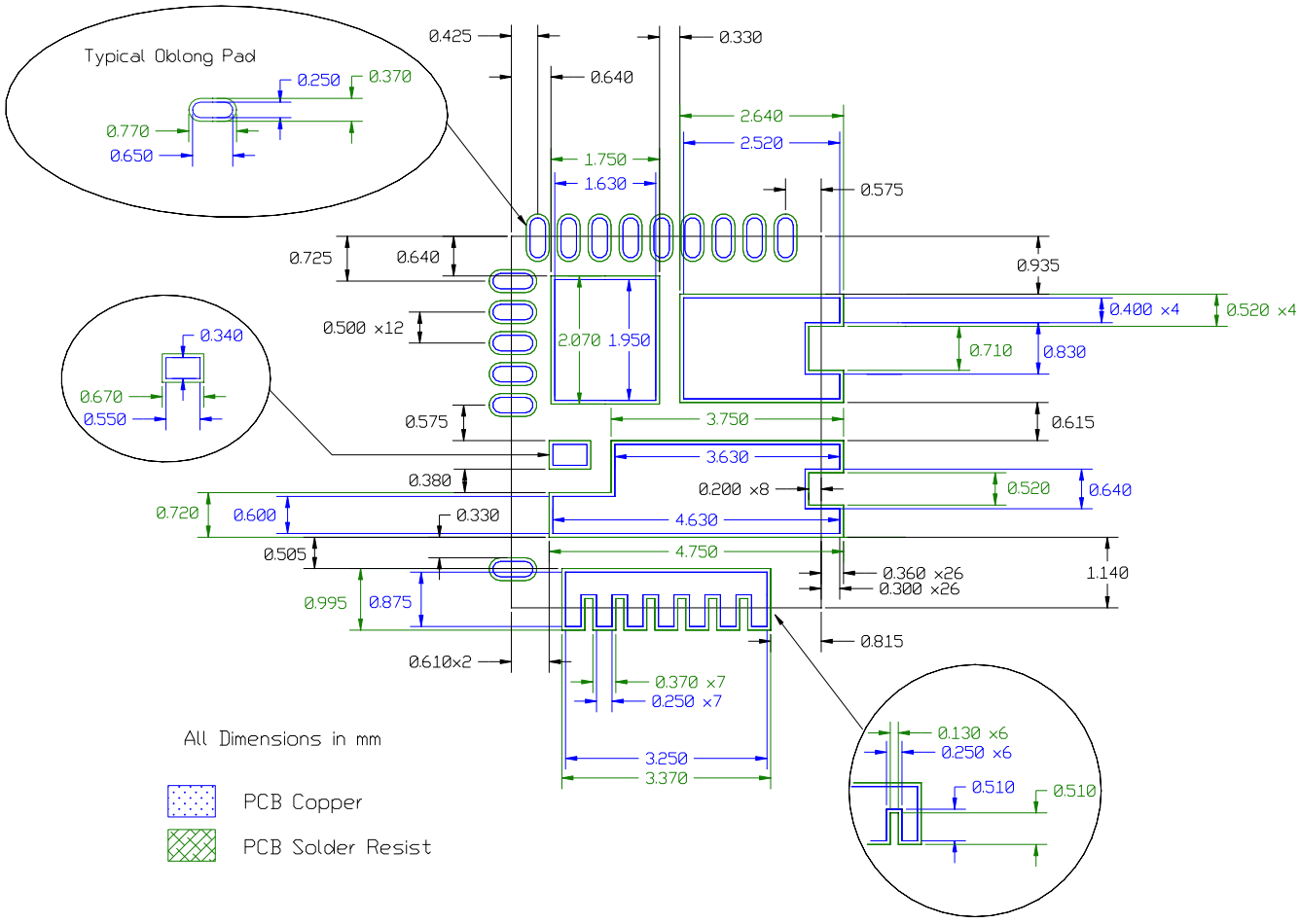


Figure 35: Solder resist

* Contact International Rectifier to receive an electronic PCB Library file in Cadence Allegro or CAD DXF/DWG format.

STENCIL DESIGN

- The stencil apertures for the lead lands should be approximately 65% to 75% of the area of the lead lands depending on stencil thickness. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The low power signal stencil lead land apertures should therefore be shortened in length to keep area ratio of 65% to 75% while centered on lead land.
- The power pads VIN, PGND and SW, land pad apertures should be approximately 65% to 75% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open. Solder paste on large pads is broken down into small sections with a minimum gap of 0.2mm between allowing for out-gassing during solder reflow.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.

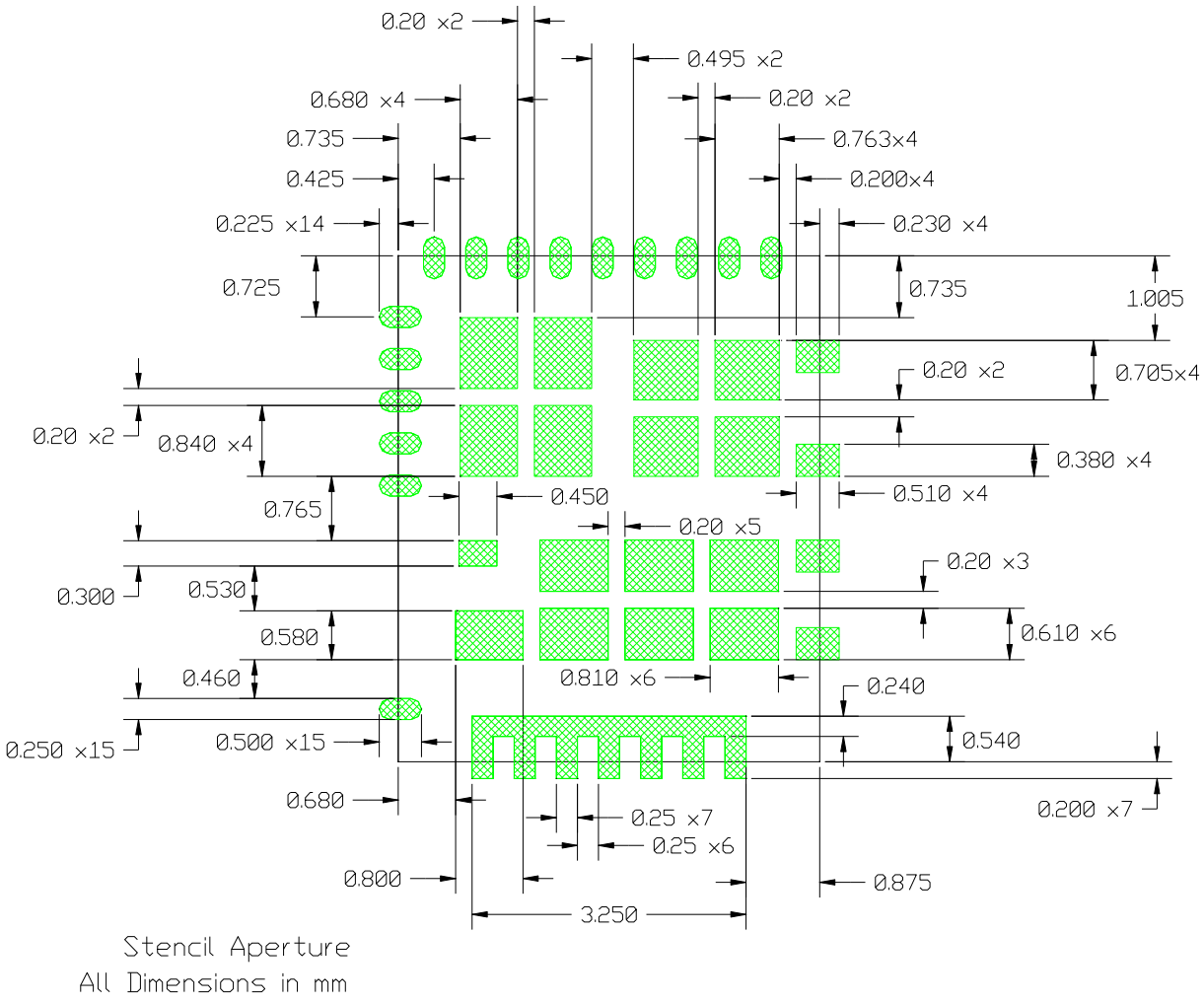


Figure 36: Stencil design

* Contact International Rectifier to receive an electronic PCB Library file in Cadence Allegro or CAD DXF/DWG format.

MARKING INFORMATION

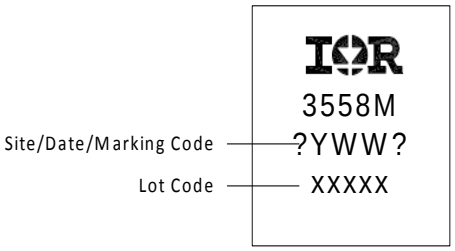
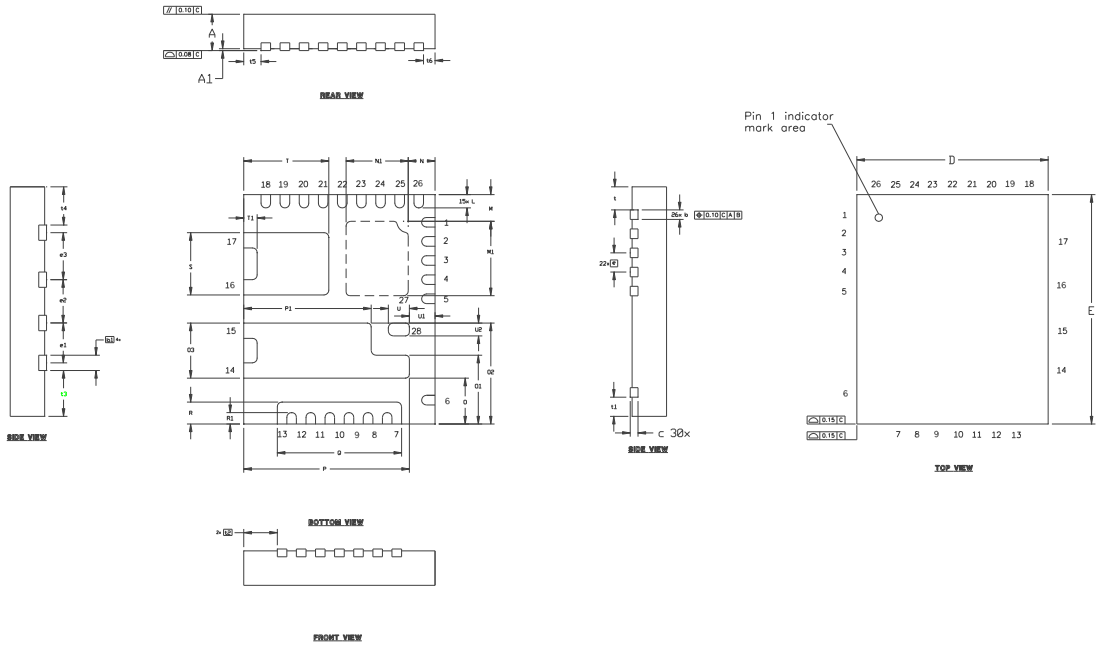


Figure 37: PQFN 5mm x 6mm

PACKAGE INFORMATION



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.800	1.000	.0315	.0394
A1	0.000	0.050	.0000	.0020
b	0.20	0.30	.0079	.0118
b1	0.350	0.450	.0138	.0177
c	0.203 REF.		.0080 REF.	
D	5.000 BASIC		.1969 BASIC	
E	6.000 BASIC		.2362 BASIC	
e	0.500 BASIC		.0197 BASIC	
e1	1.041 BASIC		.0410 BASIC	
e2	1.134 BASIC		.0446 BASIC	
e3	1.230 BASIC		.0484 BASIC	
t	0.600 BASIC		.0236 BASIC	
t1	0.500 BASIC		.0197 BASIC	
t2	0.875 BASIC		.0344 BASIC	
t3	1.200 BASIC		.0472 BASIC	
t4	0.996 BASIC		.0392 BASIC	
t5	0.450 BASIC		.0177 BASIC	
t6	0.300 BASIC		.0118 BASIC	

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
L	0.300	0.400	.0118	.0157
M	0.650	0.750	.0256	.0295
M1	1.896	1.996	.0747	.0786
N	0.650	0.750	.0256	.0296
N1	1.577	1.677	.0621	.0660
O	1.150	1.250	.0453	.0492
O1	1.750	1.850	.0689	.0728
O2	2.591	2.691	.1020	.1060
O3	1.391	1.491	.0548	.0587
P	4.281	4.381	.1685	.1725
P1	3.281	3.381	.1292	.1331
Q	3.200	3.300	.1260	.1299
R	0.525	0.625	.0207	.0246
R1	0.250	0.350	.0098	.0138
S	1.580	1.680	.0622	.0661
T	2.173	2.273	.0856	.0895
T1	0.300	0.400	.0118	.0157
U	0.500	0.600	.0197	.0236
U1	0.619	0.719	.0244	.0283
U2	0.287	0.387	.0130	.0152

Figure 38: PQFN 5mm x 6mm

Data and specifications subject to change without notice.
This product will be designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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