Power-Factor Controller (PFC) IC for High Power Factor and Active Harmonic Filter

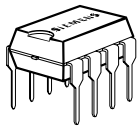
TDA 4862

Advanced Information

Bipolar IC

Features

- IC for sinusoidal line-current consumption
- Power factor approaching 1
- Controls boost converter as an active harmonics filter
- Internal start-up with low current consumption
- Zero current detector for discontinuous operation mode
- High current totem pole gate driver
- Trimmed ± 1.4% internal reference
- Undervoltage lock-out with hysteresis
- Very low start-up current consumption
- Pin compatible to world standard
- Fast overvoltage regulator
- Current sense input with internal low pass filter



PG-DIP-8-1



PG-DSO-8-1

	Type	Ordering Code	Package
▼	TDA 4862	Q67000-A8368	PG-DIP-8-1
▼	TDA 4862 G	Q67006-A8369	PG-DSO-8-1

▼ = New type

Description

The TDA 4862 is excellent convenient for designing a preconverter in ballasts and switched mode power supplies with sinusoidal line current consumption and a power factor approaching unity.

The TDA 4862 controls a boost converter as an active harmonics filter in a discontinuous mode (free oscillating triangular shaped current mode).

The TDA 4862 comprises an internal start-up timer, a high gain voltage amplifier, an one quadrant multiplier for approaching unity power factor, a zero current detector, PWM and logic circuitry, and totem pole MOSFET gate driver.

Protective features are: input undervoltage lockout with hysteresis, V_{CC} zener clamp, cycle-by-cycle current limiting, output voltage limiting for fast and slow load changes up to open circuit, and a sinking gate driver current activated whenever undervoltage mode occurs.

The output voltage of this preconverter is regulated with high accuracy. Therefore the device can be used for world-wide line voltages without switches.

The TDA 4862 is the improved version of the TDA 4817 with a pinout equivalent to world standard.

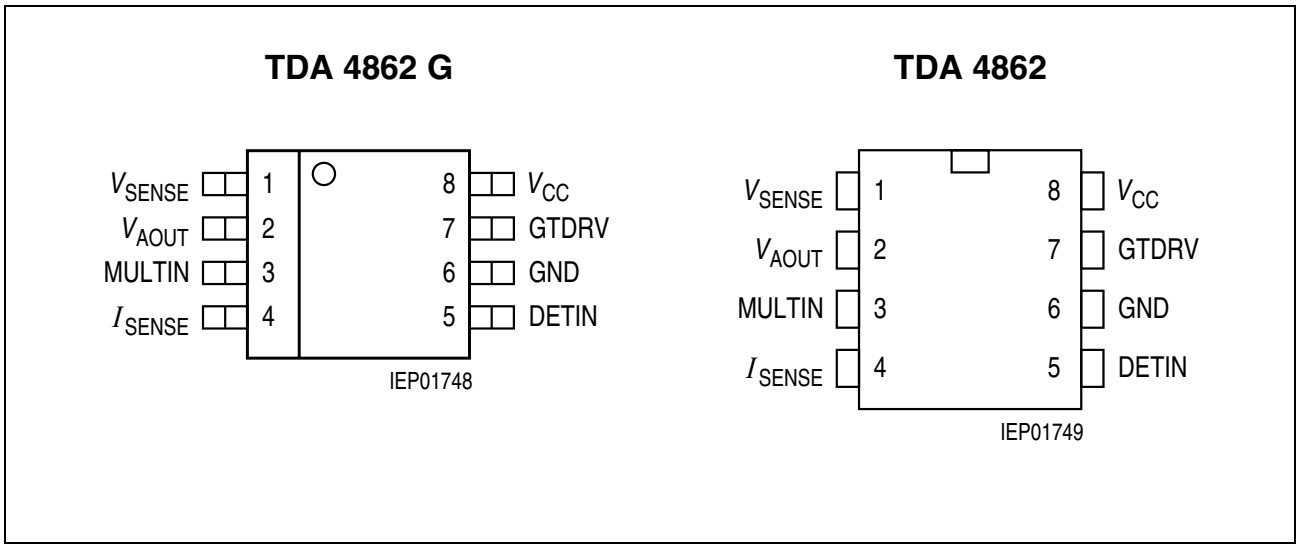


Figure 1 Pin Configuration (top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	V_{SENSE}	**Voltage Amplifier Inverting Input;** V_{SENSE} is connected via a resistive divider to the boost converter output. With a capacitor connected to V_{AOUT} it forms an integrator.
2	V_{AOUT}	**Voltage Amplifier Output;** V_{AOUT} is connected internally to the first multiplier input. To prevent overshoot the input voltage will be clamped at 5 V. During no load conditions output pulses are suppressed completely when V_{AOUT} falls below 2.2 V. If the current flowing into this pin is exceeding an internal defined margin the multiplier output voltage is reduced to prevent the MOSFET from overvoltage damage.
3	MULTIN	**Multiplier Input;** MULTIN is the second multiplier input and connected via a resistive divider to the rectifier output voltage.
4	I_{SENSE}	**Current Sense Minus;** I_{SENSE} is connected to a sense resistor controlling the MOSFET source current. The input is internally clamped at – 0.3 V to prevent negative input voltage interaction. An internal low pass filter suppresses voltage spikes when turning the MOSFET on.
5	DETIN	**Zero Current Detector Input;** DETIN is connected to an auxiliary winding monitoring the zero crossing of the inductor current.
6	GND	**Ground;** All voltages are measured with respect to GND. V_{CC} should be bypassed directly to GND with a 0.1 µF or larger ceramic capacitor.
7	GTDRV	**Gate Drive Output;** GTDRV is the output of a totem-pole circuitry for direct driving a MOSFET. A clamping network bypasses low state source current and high state sink current.
8	V_{CC}	**Positive Supply Voltage;** V_{CC} should be connected to a stable source slightly above the V_{CC} turn-ON threshold for normal operation. A 100 nF or lager ceramic capacitor connected to V_{CC} absorbs supply current spikes required to charge external MOSFET gate capacitances.

Functional Description

Introduction

Conventional electronic ballasts and switching power supplies are designed with a bridge rectifier and bulk capacitor. Their disadvantage is that the circuit draws power from the line when the instantaneous AC voltage exceeds the capacitor's voltage. This occurs near the line voltage peak and causes a high charge current spike with following characteristics: the apparent power is higher than the real power that means low power factor condition, the current spikes are non-sinusoidal with a high content of harmonics causing line noise, the rectified voltage depends on load condition and requires a large bulk capacitor, special efforts in noise suppression are necessary.

With the TDA 4862 preconverter a sinusoidal current is achieved which varies in direct instantaneous proportion to the input voltage half sine wave and means a power factor near 1. This is due to the appearance of almost any complex load like a resistive one at the AC line. The harmonic distortions are reduced and comply with the IEC555 standard.

Operating Description

The TDA 4862 contains a wide bandwidth voltage amplifier used in a feedback loop, an overvoltage regulator, an one quadrant multiplier with a wide linear operating range, a current sense comparator, zero current detector, a PWM and logic circuitry, a totem-pole MOSFET driver, an internal trimmed voltage reference, a restart timer and an undervoltage lockout circuitry. These functional blocks are described below.

Voltage Amplifier

The voltage amplifier is internally compensated and yields a gain bandwidth of 0.8 MHz and a phase margin of 80 degrees. The non-inverting input is biased at 2.5 V and is not pinned out. The inverting input is sensing the output voltage via a resitive devider. The voltage amplifier output V_{AOUT} and the inverting input V_{SENSE} are connected in a simplest way via an external capacitor. It forms an integrator which monitors the average output voltage over several line cycles. Typically the bandwidth is set below 20 Hz. In order to keep the output voltage constant the voltage amplifier output is connected to the multiplier input for regulation.

Overvoltage Regulator

Fast changes of the output voltage can't be regulated by the integrator formed with the voltage amplifier This occurs during initial start-up, sudden load removal, or output arcing and leads to a current peak at the voltage amplifier input while the voltage amplifier's differential input voltages remains zero. The peak current is flowing through the external capacitor into V_{AOUT}. Exceeding an internal defined margin causes a regulation circuitry to reduce the multiplier output voltage.

Functional Description (cont'd)

Multiplier

A one quadrant multiplier is the crucial circuitry that regulates the gate driver with respect of the DC output voltage and the AC haversine input voltage of the preregulator. Both inputs are designed for good linearity over a wide dynamic range, 0 V to 4.0 V for the MULTIN and 2.5 V to 4.0 V for the V_{AOUT}.

Current Sense Comparator and RS Latch

The multiplier output voltage is compared with the current sense voltage which represents the current through the MOSFET. The current sense comparator in addition with the logic ensures that only a single pulse appears at the drive output during a given cycle. The multiplier output and the current sense threshold are internally clamped at 1.3 V. So the gate drive MOSFET is protected against critical operating, as they occur during start up. To prevent the input from negative pulses a special protection circuitry is implemented. Switch-on current peaks are reduced by an internal RC-Filter.

Zero Current Detector

The zero current detector senses the inductor current via an auxiliary winding and ensures that the next on-time is initiated immediately when the inductor current has reached zero. This diminishes the reverse recovery losses of the boost converter diode. Output switch conduction is terminated when the voltage drop of the shunt resistor reaches the threshold level of the multiplier output. So the boost current waveform has a triangular shape and there are no deadtime gaps between the cycles. This leads to a continuous AC line current limiting the peak current to twice of the average current.

To prevent false tripping the zero current detector is designed as a Schmitt trigger with a hysteresis of 0.6 V. An internal 5 V clamp protects the input from overvoltage breakdown, a 0.6 V clamp prevents substrate injection. An external resistor must be used in series with the auxiliary winding to limit the current through the clamps.

Timer

A restart timer function was added to the IC to eliminate the need for an oscillator when used in stand-alone applications. The timer starts or restarts the TDA 4862 if the drive output has been off for more than 15 µs after the inductor current reaches zero.

Functional Description (cont'd)

Undervoltage Lockout

An undervoltage lockout circuitry enables the output stage when V_{CC} reaches the upper threshold V_{CC} and terminates the output stage when V_{CC} is falling below the lower threshold V_{CCL}. In the standby mode the supply current is typically 75 µA. An internal clamp has been added from V_{CC} to ground to protect the IC from an overvoltage condition. The external circuitry is created with a start-up resistor connected from V_{CC} to the input supply voltage and a storage capacitor from V_{CC} to ground. Bootstrap power supply is created with the previous mentioned auxiliary winding and a diode.

Output

The TDA 4862 totem pole output stage is MOSFET compatible. An internal protection circuitry is activated when V_{CC} is within the stand by mode and ensures that the MOSFET is turned-OFF. The totem pole output has been optimized to minimize cross conduction current during high speed operation. The addition of two 4 Ω resistors, one in series with the source output transistor and one in series with the sink output transistor, reduces the cross conduction current.

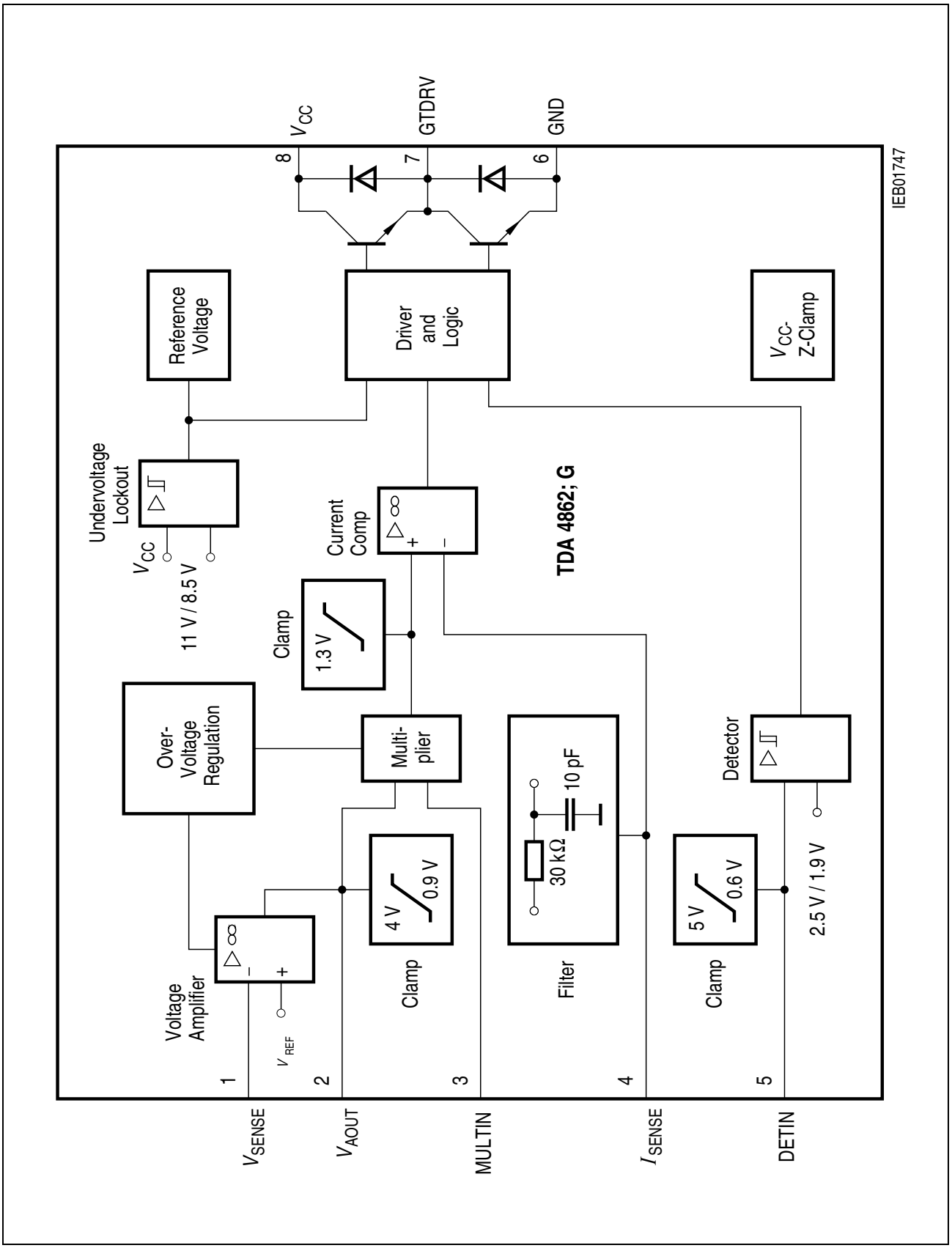


Figure 2 Block Diagram

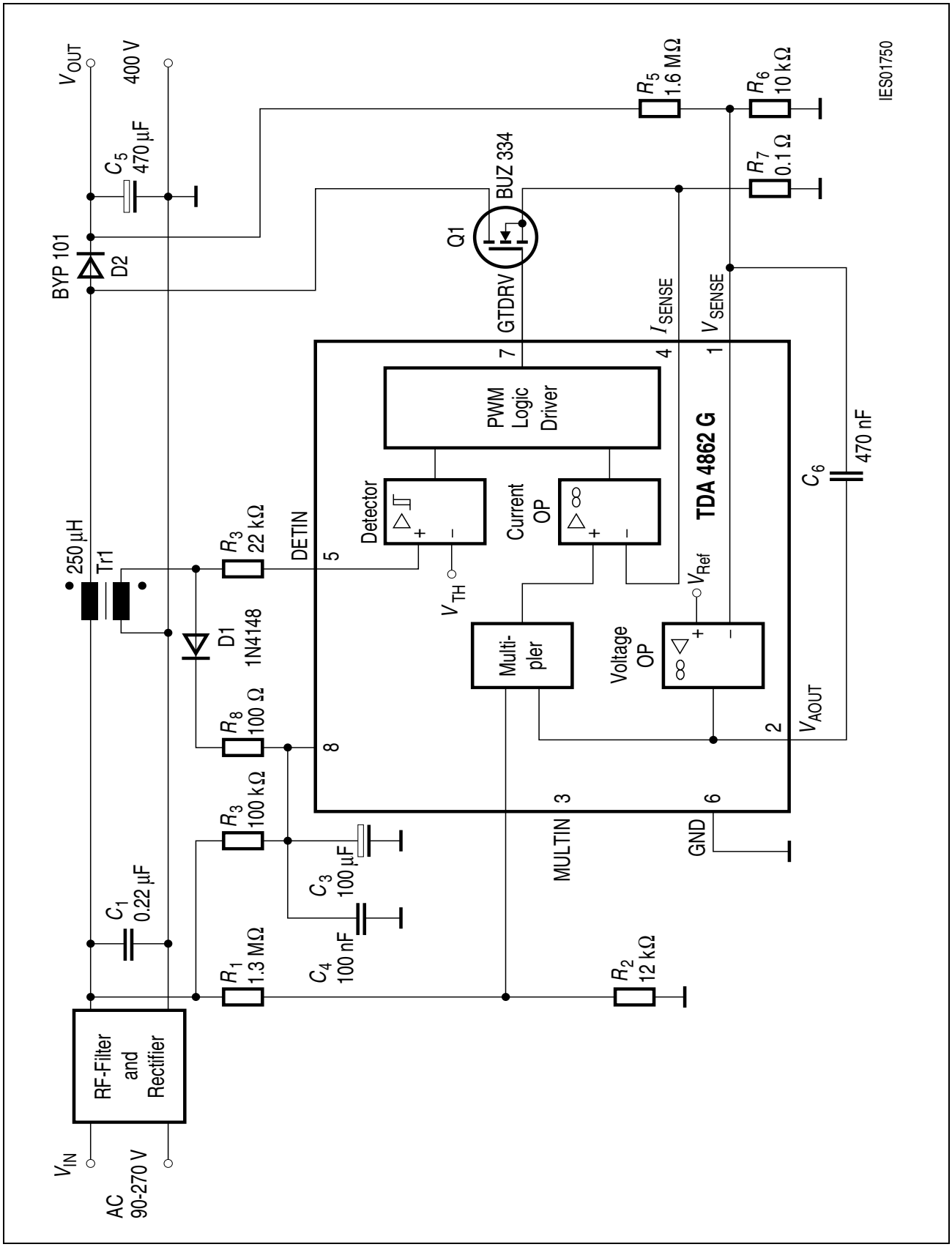


Figure 3 Application Circuit with TDA 4862; G

Absolute Maximum Ratings

Parameter			Symbol	Limit Values		Unit	Notes
				min.	max.		
Supply voltage at	V_{CC}	Pin 8	V_{CC}	– 0.3	–	V	–
supply + Z-current	V_{CC}-GND	Pin 8	I_{CCZ}	0	70	mA	observe P_{max}
Current into	GTDRV	Pin 7	I_{GTDRV}	– 400	500	mA	observe P_{max}
Clamping current into	GTDRV	Pin 7	I_{GTDCH}	–	100	mA	$V_{GTDRV} > V_{CC}$
Clamping current into	GTDRV	Pin 7	I_{GTDCL}	– 100	–	mA	$V_{GTDRV} < -0.3$ V
Voltage at	V_{SENSE}	Pin 1	V_{VSENSE}	– 0.3	17	V	–
Voltage at	V_{AOUT}	Pin 2	V_{VAOUT}	– 0.3	6	V	–
Voltage at	MULTIN	Pin 3	V_{MULTIN}	– 0.3	17	V	–
Voltage at	I_{SENSE}	Pin 4	V_{ISENSE}	– 10	17	V	–
Current into	DETIN	Pin 5	I_{DETINH}	–	50	mA	$V_{DETIN} > 6$ V
Current into	DETIN	Pin 5	I_{DETINL}	– 10	–	mA	$V_{DETIN} < 0.9$ V
Junction temperature			T_j	– 40	150	°C	–
Storage temperature			T_{stg}	– 50	150	°C	–
Thermal resistance system-air							
TDA 4862			R_{thSA}	–	100	K/W	PG-DIP-8-1
TDA 4862 G			R_{thSA}	–	180	K/W	PG-DSO-8-1

Operating Range

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	V_{CC}	V_{CCON}	V_Z	V	1)
Z-current	I_Z	0	50	mA	observe P_{max}
Junction temperature	T_j	– 40	150	°C	–
Voltage at I_{SENSE}	V_{ISENSE}	– 5	V_Z	V	–

1) V_{CCON} means V_{CCH} has been exceeded but the supply voltage is still above V_{CCL}. The device has switched from standby to active. For V_{CCH} and V_{CCL} values **see Electrical Characteristics**. If 0 V < V_{CC} < V_{CCON}, the device is in standby and output GTDRV is active low.

Electrical Characteristics

Unless otherwise stated, V_{CC} = 12 V, – 40 °C < T_j < 150 °C.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Overall						
Supply current, OFF	I_{CCL}	–	75	200	µA	0 V < V_{CC} < V_{CCH}
Supply current, ON	I_{CCH}	–	4	6	mA	Output low
Supply current, dynamic	I_{CCDY}	–	4.2	8	mA	f_{DETIN} = 50 kHz, C_{GTDRV} = 1 nF
V_{CC} turn-ON threshold	V_{CCH}	–	11	11.5	V	–
V_{CC} turn-OFF threshold	V_{CCL}	8.0	8.5	–	V	–
V_{CC} turn-ON/OFF hysteresis	V_{CCHY}	1.8	2.3	3.0	V	–
V_{CC} clamp	V_Z	15	17	19	V	I_{CCZ} = 50 mA
Voltage Amplifier						
Voltage feedback threshold	V_{FB}	2.465	2.5	2.535	V	T_j = 25 °C, Pin 1 to Pin 2
Voltage feedback threshold	V_{FB}	2.45	–	2.55	V	Pin 1 to Pin 2
Line regulation	ΔV_{FBL}	–	–	5	mV	V_{CC} = 10 V to 15 V
Input bias current	$I_{BVSENSE}$	– 1	–	–	µA	–
Open loop voltage gain[1)]	G_V	–	80	–	dB	–
Unity gain bandwidth[1)]	B_W	–	0.8	–	MHz	–
Phase margin[1)]	Φ_M	–	80	–	Degr	–
Inhibit threshold voltage	V_{VAOUTI}	–	2.2	–	V	–
Output current source	I_{VAOUTH}	–	– 12	–	mA	V_{VAOUT} = 0 V, V_{VSENSE} = 2.3 V
Output current sink	I_{VAOUTL}	–	4	–	mA	V_{VAOUT} = 4 V, V_{VSENSE} = 2.8 V

[1]not subject to production test - verified by characterization.

Electrical Characteristics (cont'd)

Unless otherwise stated, V_{CC} = 12 V, – 40 °C < T_j < 150 °C.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output voltage swing high state	V_{VAOUTH}	3.8	4.3	5.0	V	I_{VAOUT} = – 0.2 mA V_{VSENSE} = 2.3 V
Output voltage swing low state	V_{VAOUTL}	–	0.9	–	V	I_{VAOUT} = 0.5 A V_{VSENSE} = 2.8 V
Overvoltage Regulator						
Regulation current	I_{RVAOUT}	20	30	45	µA	V_{VAOUT} = V_{MULTIN} = 4 V, V_{ISENSE} = 0.5 V
Current Comparator						
Input bias current	$I_{BISENSE}$	– 1	–	–	µA	–
Input offset voltage	$V_{ISENSEO}$	–	25	–	mV	V_{MULTIN} = 0 V, V_{VAOUT} = 2.4 V
Max threshold voltage	$V_{ISENSEM}$	1.05	1.25	1.5	V	–
Delay to output[1)]	t_{PHL}	–	250	–	ns	–
)						
Detector						
Upper threshold voltage (V_{DETIN} increasing)	V_{DETINU}	–	2.5	2.75	V	–
Lower threshold voltage (V_{DETIN} decreasing)	V_{DETINL}	1.5	1.9	–	V	–
Hysteresis	$V_{DETINHY}$	–	0.6	–	V	–
Input current	I_{BDETIN}	– 1	–	–	µA	1.5 V < V_{DETIN} < 2.75 V
Input clamp voltage High state Low state	 $V_{DETINHC}$ $V_{DETINLC}$	 4 –	 5 0.6	 – 1	 V V	 I_{DETIN} = 5 mA I_{DETIN} = – 5 mA

[1)] not subject to production test - verified by characterization

Electrical Characteristics (cont'd)

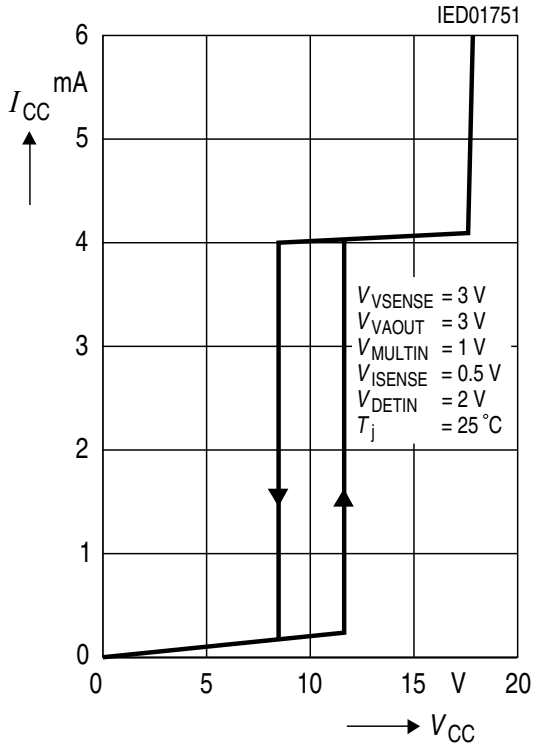
Unless otherwise stated, V_{CC} = 12 V, – 40 °C < T_j < 150 °C.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Multiplier						
Input bias current	$I_{BMULTIN}$	– 1	–	–	µA	–
Dynamic voltage range MULTIN V_{AOUT}	 V_{MULTIN} V_{VAOUT}	 0 to 3 V_{FB} to V_{FB} + 1	 0 to 4 V_{FB} to V_{FB} + 1.5	 – –	 V V	 V_{VAOUT} = 2.75 V V_{MULTIN} = 1.0 V
Multiplier gain [1]	K	0.45	0.65	0.85	1/V	V_{MULTIN} = 2 V V_{VAOUT} = V_{FB} + 1 V
Restart Timer						
Restart time delay	t_{DLY}	75	190	400	µs	–
Gate Driver						
Output voltage low state	V_{GTDRVL}	–	0.8 1.8	–	V V	I_{GTDRV} = 20 mA I_{GTDRV} = 200 mA
Output voltage high state	V_{GTDRVH}	–	9.4 8.7	–	V	I_{GTDRV} = – 20 mA I_{GTDRV} = – 200 mA
Output voltage active shut down	V_{GTDRVU}	–	2.0	2.6	V	I_{GTDRV} = 50 mA V_{CC} increasing: 0 < V_{CC} < V_{CCH}, V_{CC} decreasing: 0 < V_{CC} < V_{CCL}
Rise time [2]	t_r	–	100	–	–	C_{GTDRV} = 1 nF
Fall time [2]	t_f	–	40	–	–	C_{GTDRV} = 1 nF

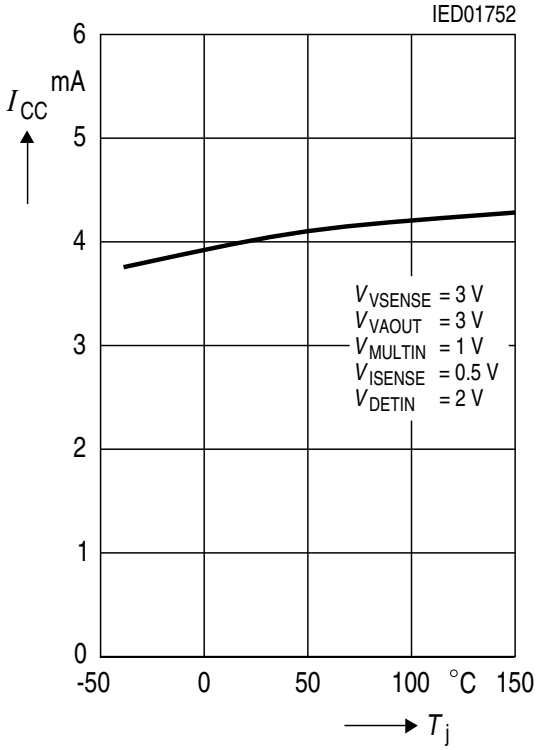
[1] $K = V_{ISENSE} / (V_{MULTIN} \times (V_{VAOUT} - V_{FB}))$

[2] not subject to production test - verified by design

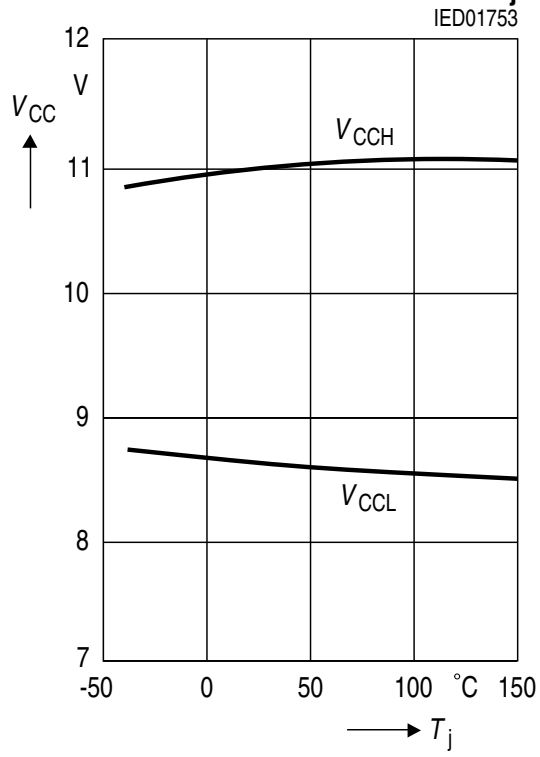
Supply Current I_{CC} versus Supply Voltage V_{CC}



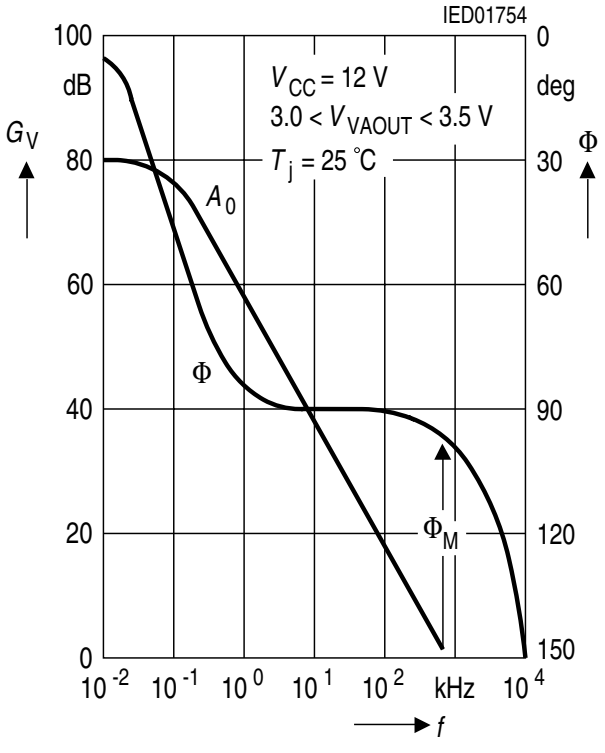
Supply Current I_{CC} versus Junction Temperature T_j



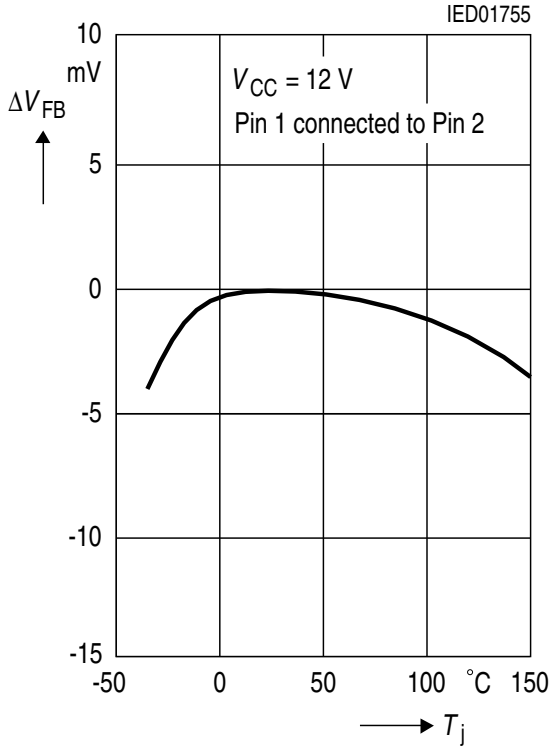
Turn-ON/-OFF Threshold Voltage V_{CC} versus Junction Temperature T_j



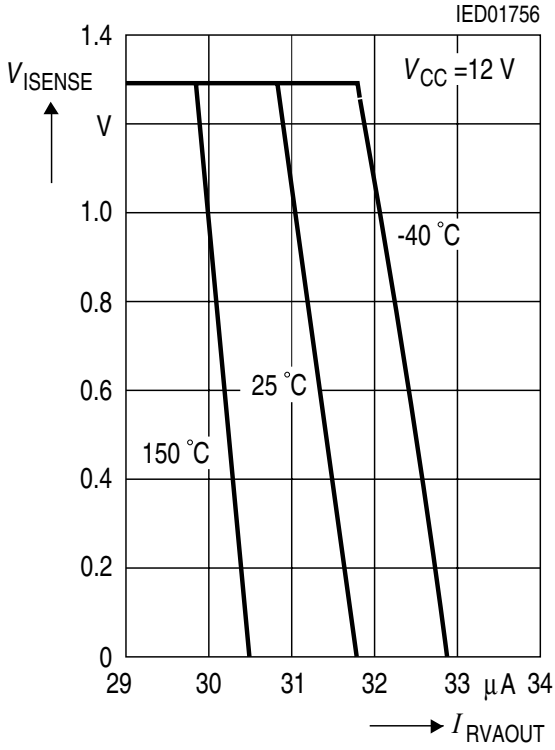
Open Loop Gain G_V and Phase Φ versus Frequency f



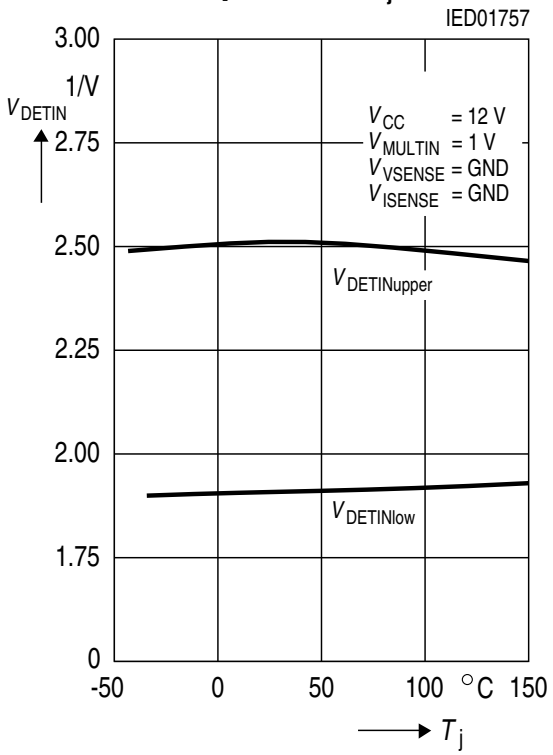
Threshold Voltage Change ΔV_{FB} versus Junction Temperature T_j



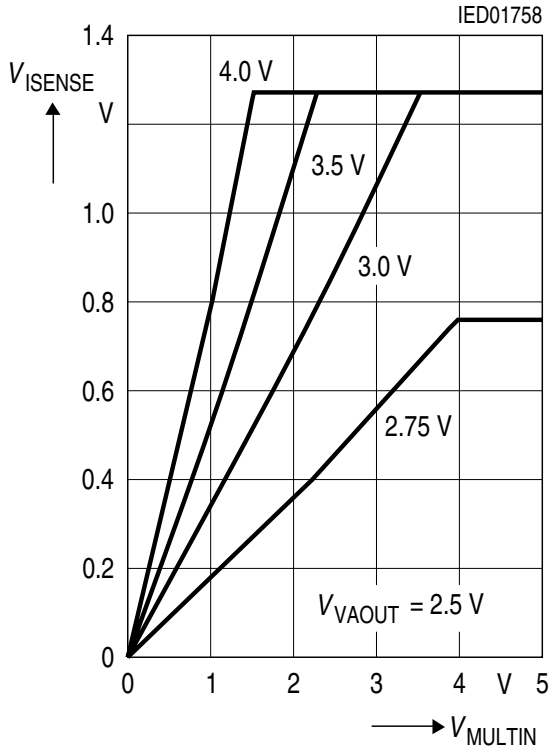
Threshold Voltage V_{ISENSE} versus Regulation Current I_{RVAOUT}



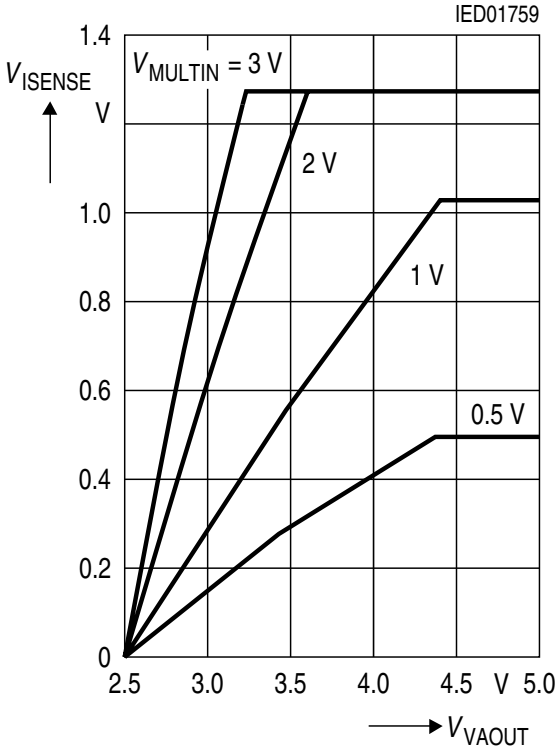
Threshold Voltage V_{DETIN} versus Junction Temperature T_j



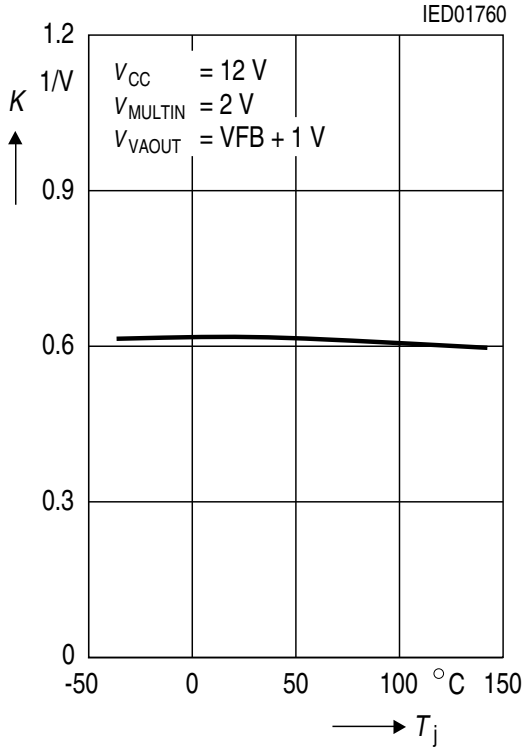
Current Sense Threshold V_{ISENSE} versus Multiplier Input V_{MULTIN}



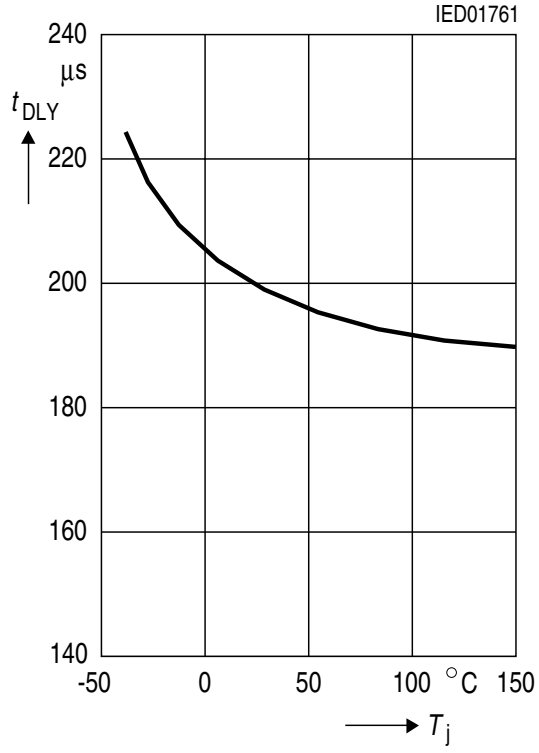
Current Sense Threshold V_{ISENSE} versus Voltage Amplifier Output V_{VAOUT}



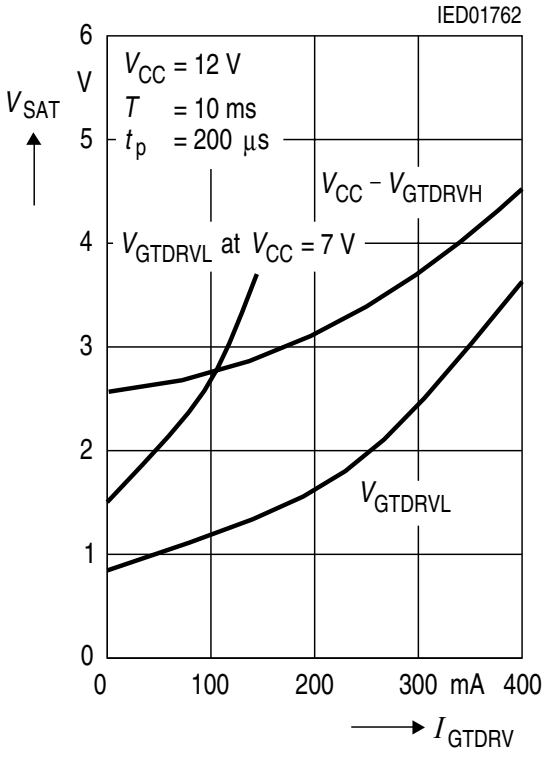
Multiplier Gain K versus Junction Temperature T_j



Restart Time Delay t_{DLY} versus Junction Temperature T_j

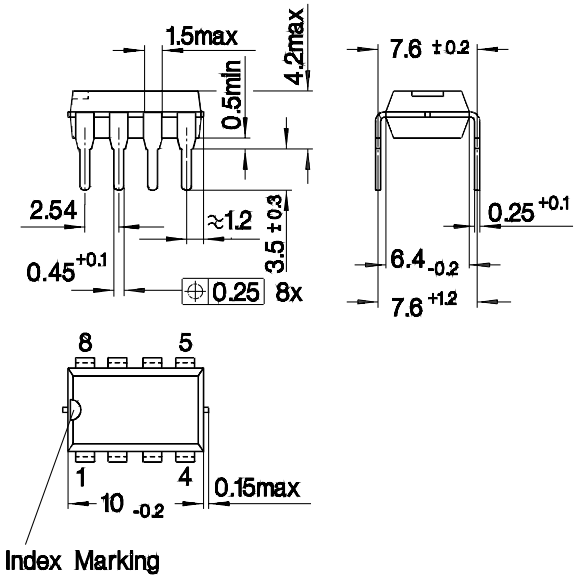


Output Voltage Low/High State V_{SAT} versus Load Current I_{GTDRV}



Package Outlines

Plastic Package, PG-DIP-8-1
(Plastic Dual In-line Package)

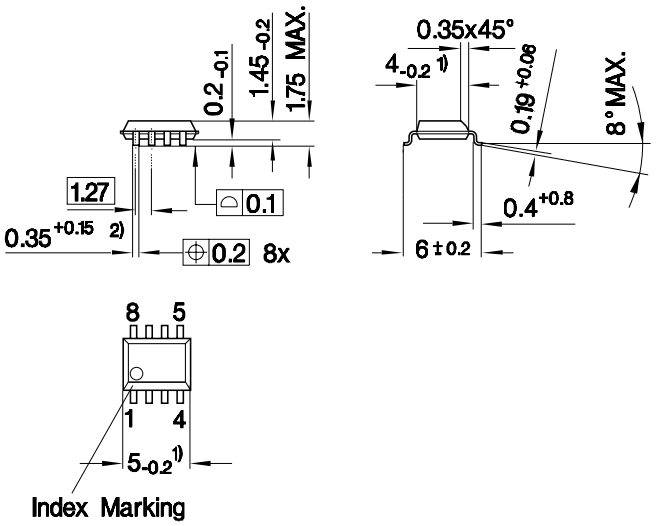


GPD05025

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

Dimensions in mm

Plastic Package, PG-DSO-8-1
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Lead width can be 0.61 max. in dambar area

GPS05121

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm

Revision History:	Current Version: 2005-02-17	
Previous Version:2003-05-01		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
1	1	Pb-free lead plating; RoHS compliant

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