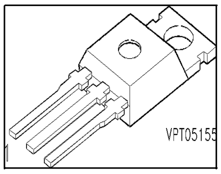
Cool MOS™ Power Transistor

V_{DS} @ T_{jmax}	650	V
$R_{DS(on)}$	3	Ω
I_D	1.8	A

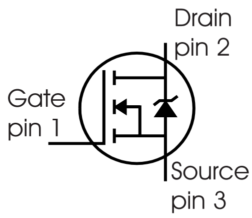
Feature

- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- Extreme dv/dt rated
- Ultra low effective capacitances
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[0)] for target applications

PG-TO220



Type	Package	Ordering Code	Marking
SPP02N60C3	PG-TO220	Q67040-S4392	02N60C3



Maximum Ratings

Parameter	Symbol	Value	Unit
Continuous drain current T_C = 25 °C T_C = 100 °C	I_D	 1.8 1.1	A
Pulsed drain current, t_p limited by T_{jmax}	$I_{D\ puls}$	5.4	
Avalanche energy, single pulse I_D = 1.35 A, V_{DD} = 50 V	E_{AS}	50	mJ
Avalanche energy, repetitive t_{AR} limited by T_{jmax}[1)] I_D = 1.8 A, V_{DD} = 50 V	E_{AR}	0.07	
Avalanche current, repetitive t_{AR} limited by T_{jmax}	I_{AR}	1.8	A
Gate source voltage static	V_{GS}	±20	V
Gate source voltage AC (f >1Hz)	V_{GS}	±30	
Power dissipation, T_C = 25°C	P_{tot}	25	W
Operating and storage temperature	T_j , T_{stg}	-55... +150	°C
Reverse diode dv/dt [6)]	dv/dt	15	V/ns

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain Source voltage slope V_{DS} = 480 V, I_D = 1.8 A, T_j = 125 °C	dv/dt	50	V/ns

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	-	-	5	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	62	
SMD version, device on PCB: @ min. footprint @ 6 cm^2 cooling area [2)]	R_{thJA}	 - -	 - 35	 62 -	
Soldering temperature, wavesoldering 1.6 mm (0.063 in.) from case for 10s [3)]	T_{sold}	-	-	260	°C

Electrical Characteristics, at Tj=25°C unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=0.25mA	600	-	-	V
Drain-Source avalanche breakdown voltage	$V_{(BR)DS}$	V_{GS}=0V, I_D=0.25A	-	700	-	
Gate threshold voltage	$V_{GS(th)}$	I_D=80µA, V_{GS}=V_{DS}	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	V_{DS}=600V, V_{GS}=0V, T_j=25°C, T_j=150°C	 - -	 0.5 -	 1 50	µA
Gate-source leakage current	I_{GSS}	V_{GS}=30V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=1.1A, T_j=25°C T_j=150°C	 - -	 2.7 7.3	 3 -	Ω
Gate input resistance	R_G	f=1MHz, open Drain	-	9	-	

Electrical Characteristics , at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Transconductance	g_{fs}	$V_{DS}≥2*I_D*R_{DS(on)max}$, I_D=1.1A	-	1.75	-	S
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	200	-	pF
Output capacitance	C_{oss}		-	90	-	
Reverse transfer capacitance	C_{rss}		-	4	-	
Effective output capacitance,[4] energy related	$C_{o(er)}$	V_{GS}=0V, V_{DS}=0V to 480V	-	8.1	-	pF
Effective output capacitance,[5] time related	$C_{o(tr)}$		-	15.7	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=350V, V_{GS}=0/10V, I_D=1.8A, R_G=50Ω	-	6	-	ns
Rise time	t_r		-	3	-	
Turn-off delay time	$t_{d(off)}$		-	68	70	
Fall time	t_f		-	12	30	

Gate Charge Characteristics

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Gate to source charge	Q_{gs}	V_{DD}=420V, I_D=1.8A	-	1.6	-	nC
Gate to drain charge	Q_{gd}		-	3.8	-	
Gate charge total	Q_g	V_{DD}=420V, I_D=1.8A, V_{GS}=0 to 10V	-	9.5	12.5	
Gate plateau voltage	$V_{(plateau)}$	V_{DD}=420V, I_D=1.8A	-	5.5	-	V

[0]J-STD20 and JESD22

[1]Repetitve avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR}*f$.

[2]Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical without blown air.

[3]Soldering temperature for TO-263: 220°C, reflow

[4]$C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

[5]$C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

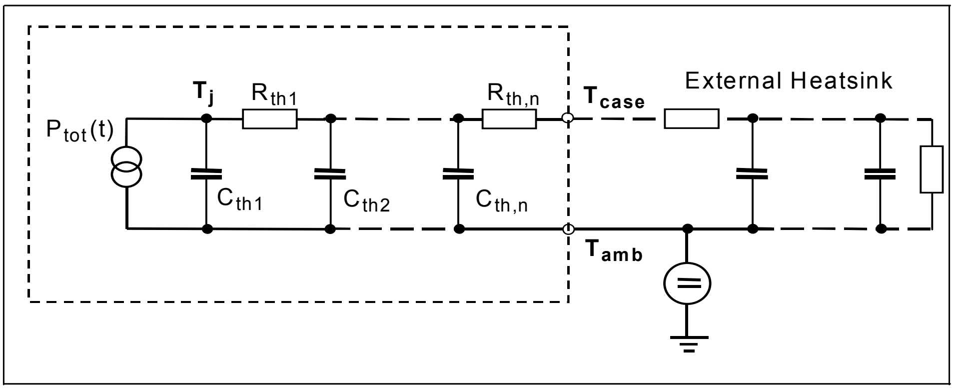
[6]I_{SD}<=I_D, di/dt<=400A/us, V_{DClink}=400V, V_{peak}<$V_{BR, DSS}$, T_j<$T_{j,max}$.
Identical low-side and high-side switch.

Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Inverse diode continuous forward current	I_S	T_C=25°C	-	-	1.8	A
Inverse diode direct current, pulsed	I_{SM}		-	-	5.4	
Inverse diode forward voltage	V_{SD}	V_{GS}=0V, I_F=I_S	-	1	1.2	V
Reverse recovery time	t_{rr}	V_R=420V, I_F=I_S ,	-	200	350	ns
Reverse recovery charge	Q_{rr}	di_F/dt=100A/µs	-	1.3	-	µC
Peak reverse recovery current	I_{rrm}		-	9	-	A
Peak rate of fall of reverse recovery current	di_{rr}/dt		-	-	200	A/µs

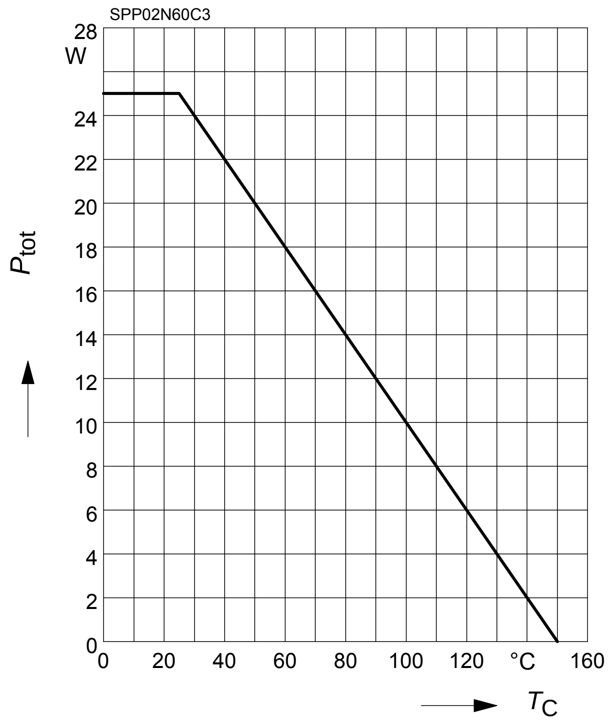
Typical Transient Thermal Characteristics

Symbol	Value	Unit	Symbol	Value	Unit
	typ.			typ.	
Thermal resistance			Thermal capacitance		
R_{th1}	0.1	K/W	C_{th1}	0.00002806	Ws/K
R_{th2}	0.184		C_{th2}	0.0001113	
R_{th3}	0.306		C_{th3}	0.0001679	
R_{th4}	1.207		C_{th4}	0.000547	
R_{th5}	0.974		C_{th5}	0.001388	
R_{th6}	0.251		C_{th6}	0.035	



1 Power dissipation

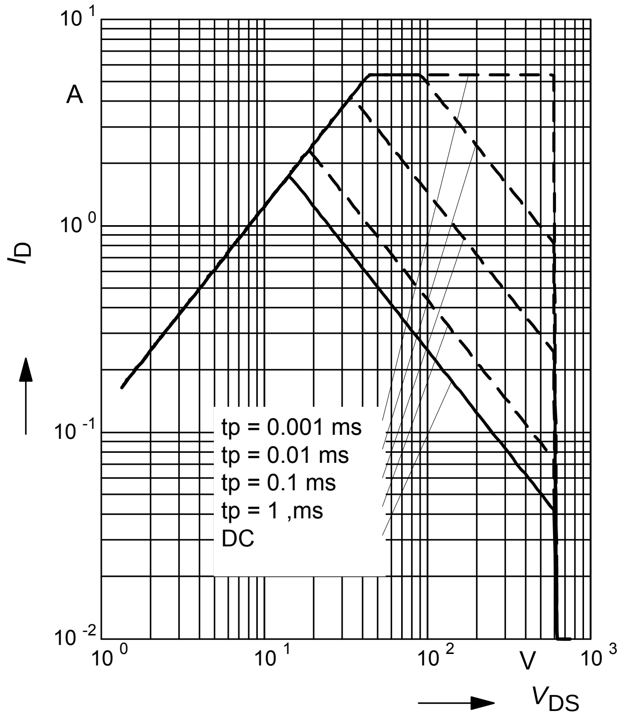
$P_{tot} = f(T_C)$



2 Safe operating area

$I_D = f(V_{DS})$

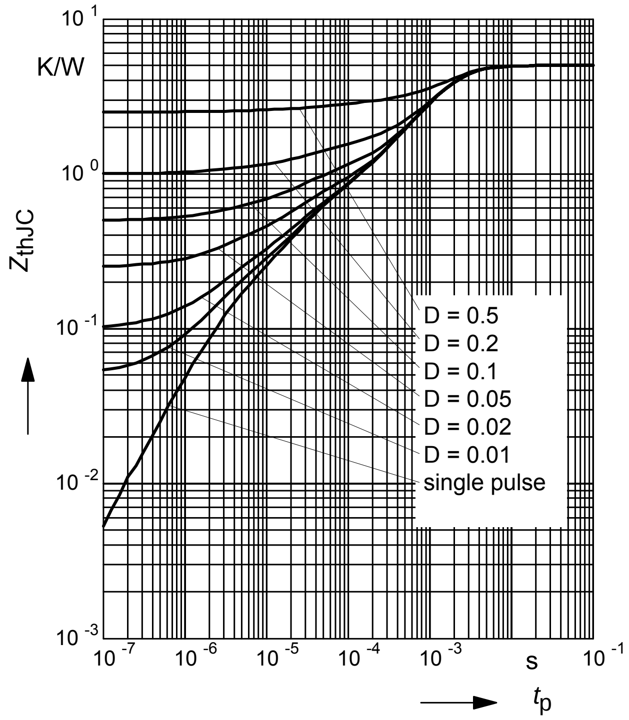
parameter : $D = 0$, T_C=25°C



3 Transient thermal impedance

$Z_{thJC} = f(t_p)$

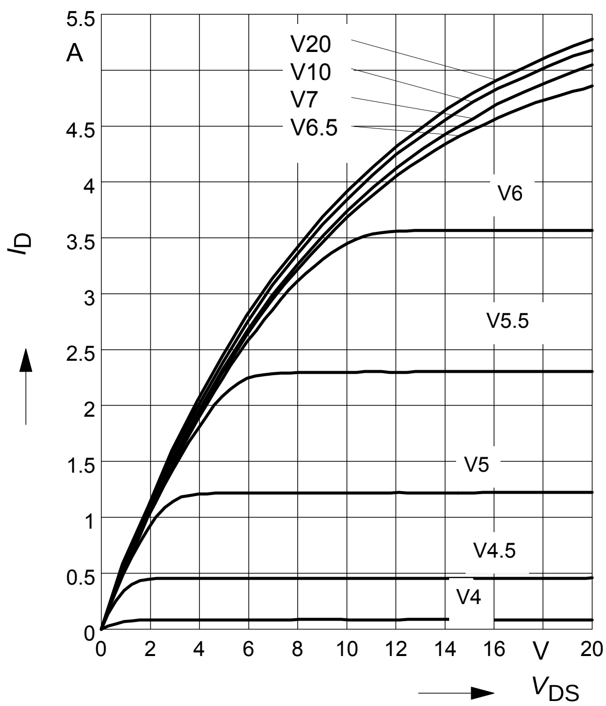
parameter: $D = t_p/T$



4 Typ. output characteristic

$I_D = f(V_{DS})$; T_j=25°C

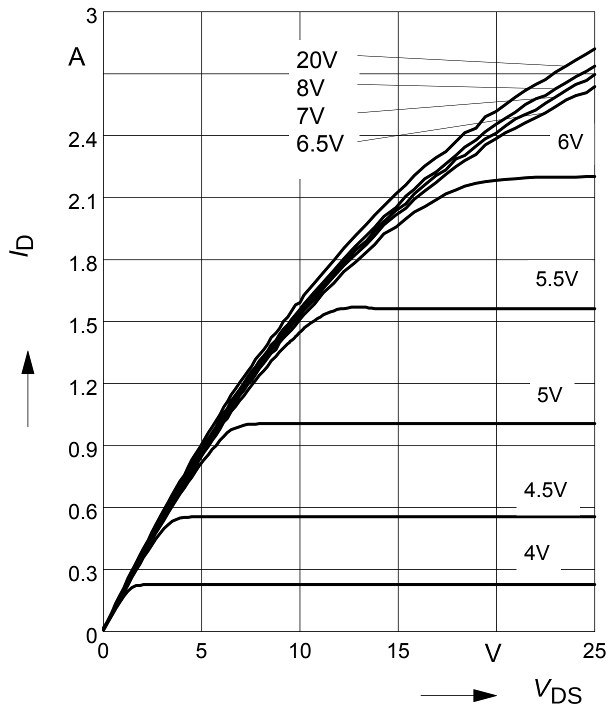
parameter: t_p = 10 µs, V_{GS}



5 Typ. output characteristic

$I_D = f(V_{DS})$; T_j=150°C

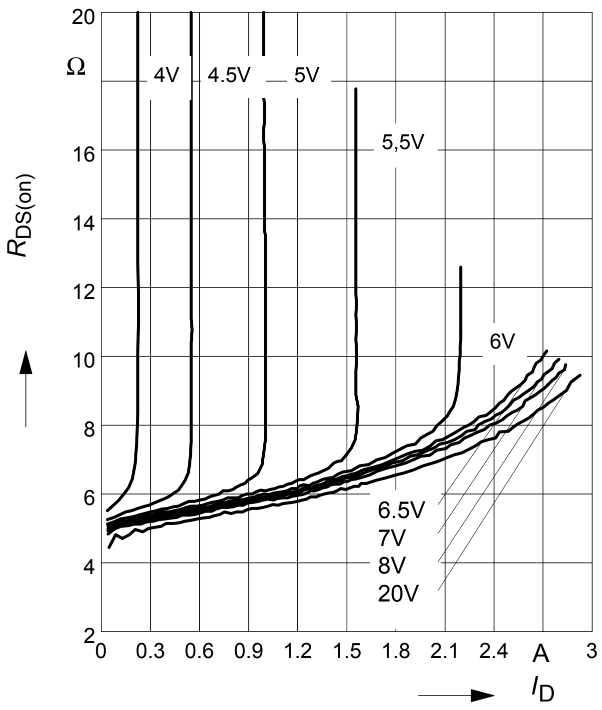
parameter: t_p = 10 µs, V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$

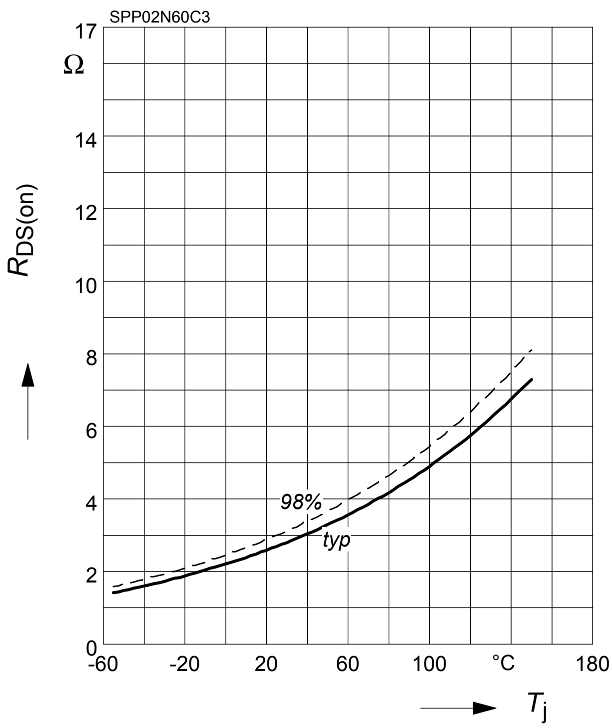
parameter: T_j=150°C, V_{GS}



7 Drain-source on-state resistance

$R_{DS(on)} = f(T_j)$

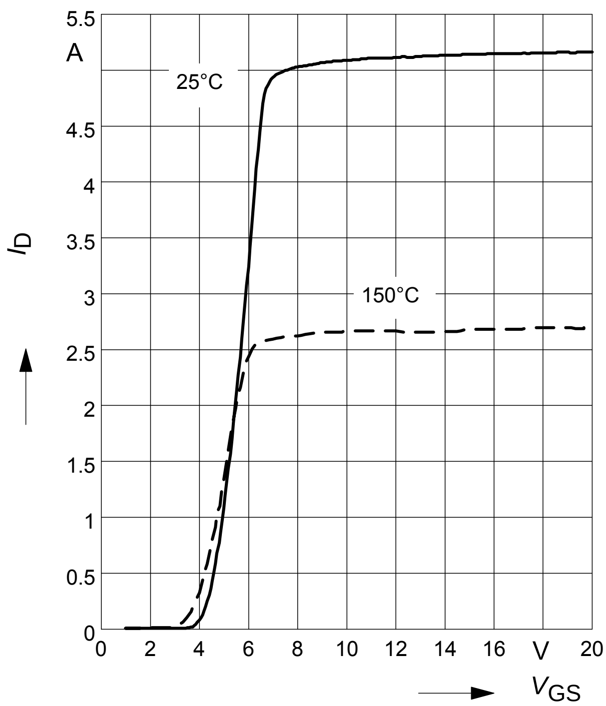
parameter : I_D = 1.1 A, V_{GS} = 10 V



8 Typ. transfer characteristics

$I_D= f(V_{GS})$; $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$

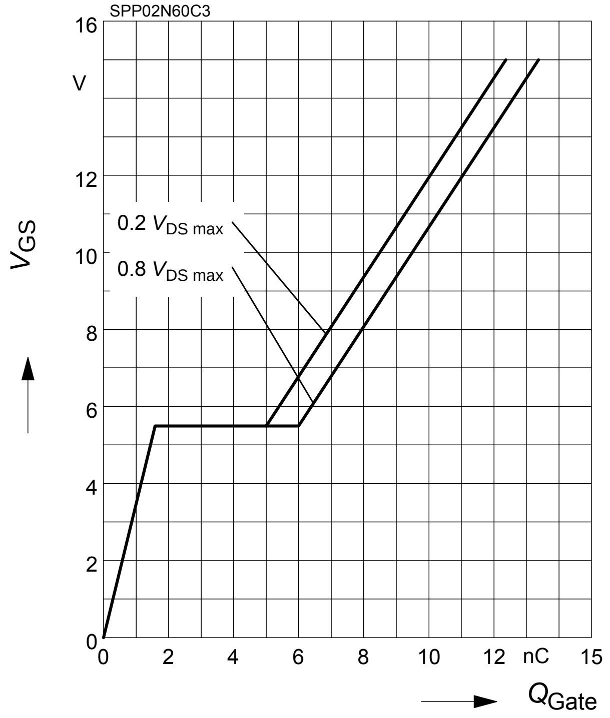
parameter: t_p = 10 µs



9 Typ. gate charge

$V_{GS} = f\ (Q_{Gate})$

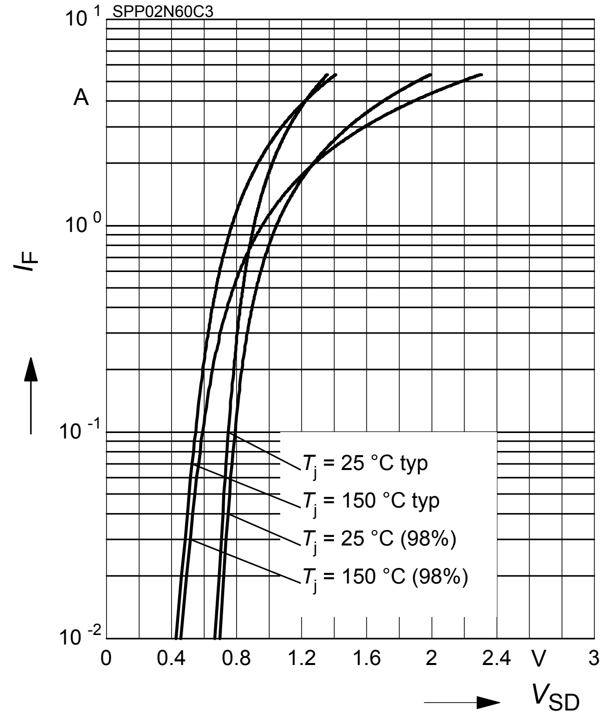
parameter: I_D = 1.8 A pulsed



10 Forward characteristics of body diode

$I_F = f\ (V_{SD})$

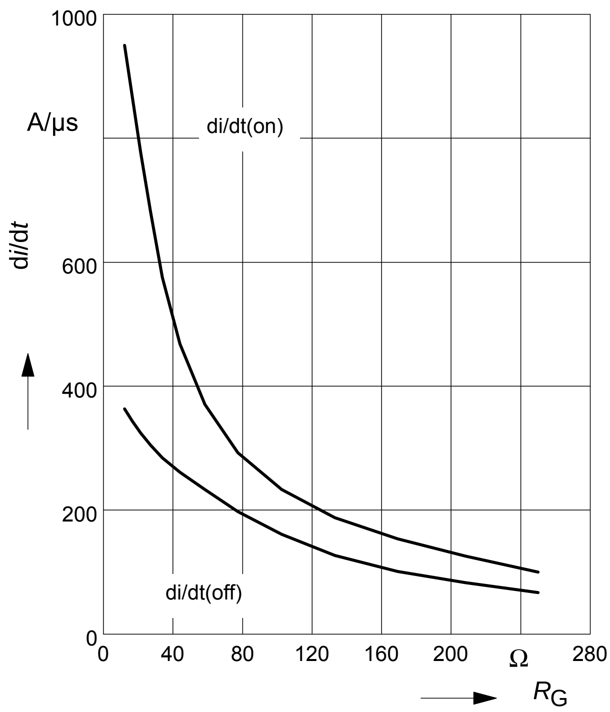
parameter: T_j , tp = 10 µs



11 Typ. drain current slope

di/dt = f(R_G), inductive load, T_j = 125°C

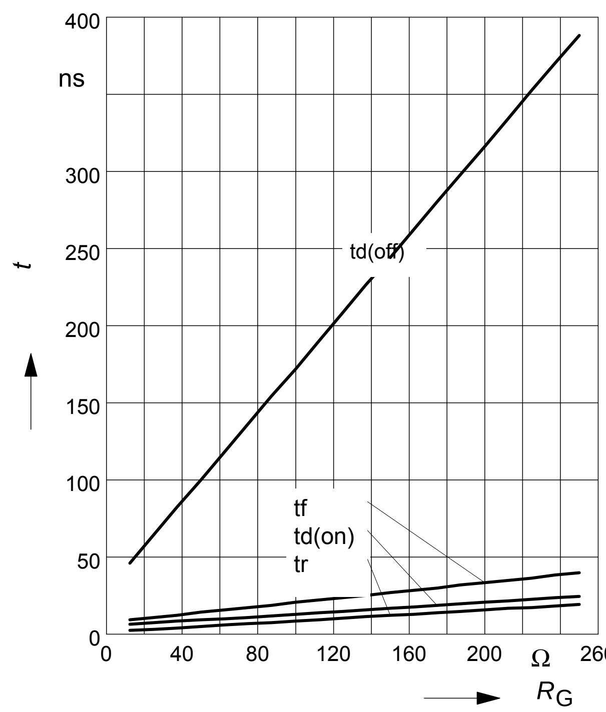
par.: V_{DS}=380V, V_{GS}=0/+13V, I_D=1.8A



12 Typ. switching time

$t = f\ (R_G)$, inductive load, T_j=125°C

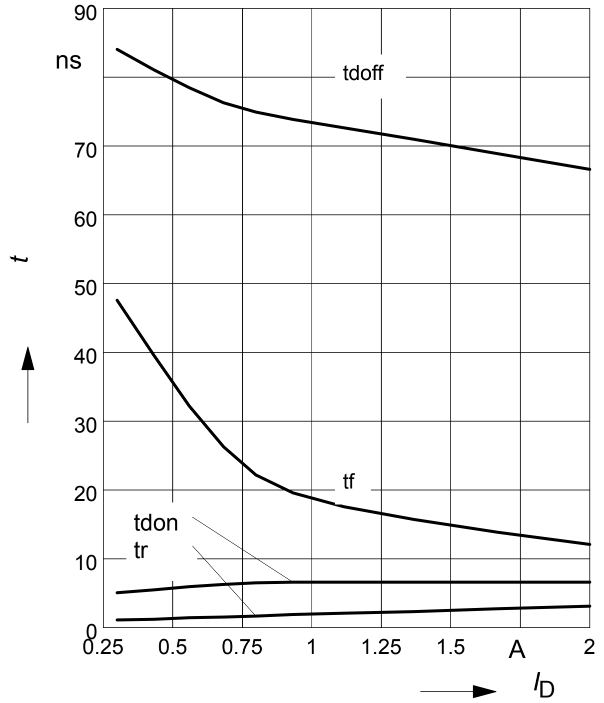
par.: V_{DS}=380V, V_{GS}=0/+13V, I_D=1.8 A



13 Typ. switching time

$t = f(I_D)$, inductive load, T_j=125°C

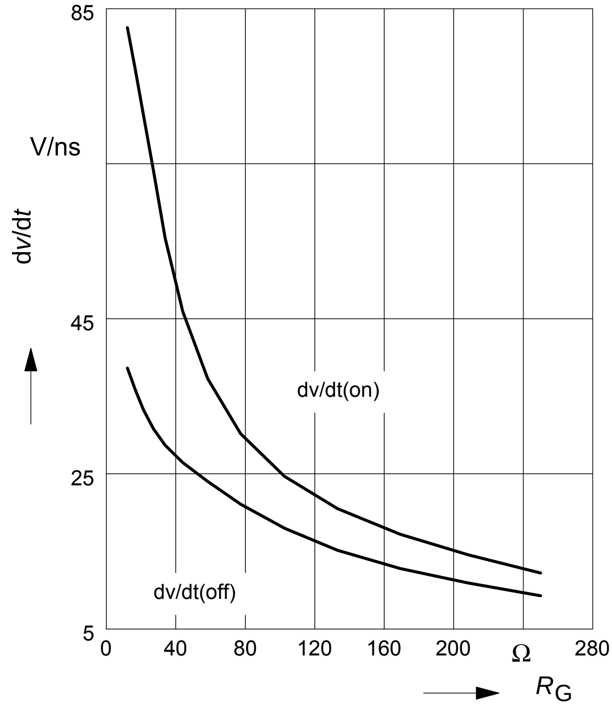
par.: V_{DS}=380V, V_{GS}=0/+13V, R_G=50Ω



14 Typ. drain source voltage slope

$dv/dt = f(R_G)$, inductive load, T_j = 125°C

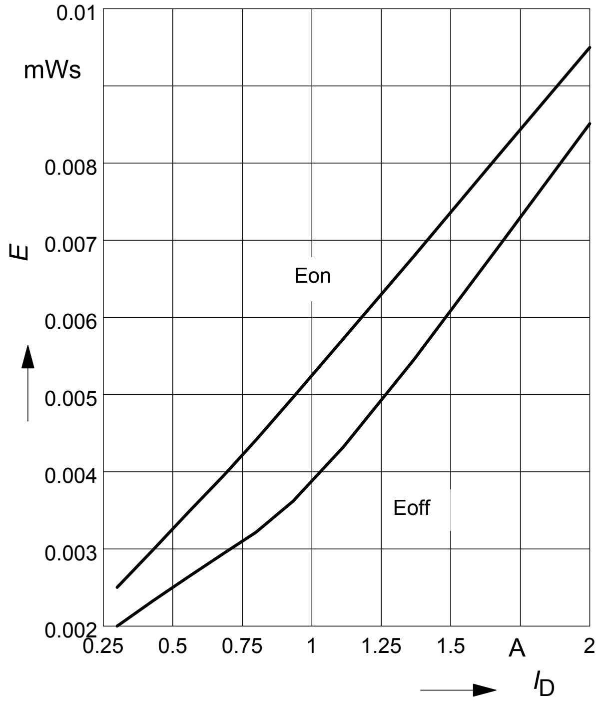
par.: V_{DS}=380V, V_{GS}=0/+13V, I_D=1.8A



15 Typ. switching losses

$E = f(I_D)$, inductive load, T_j=125°C

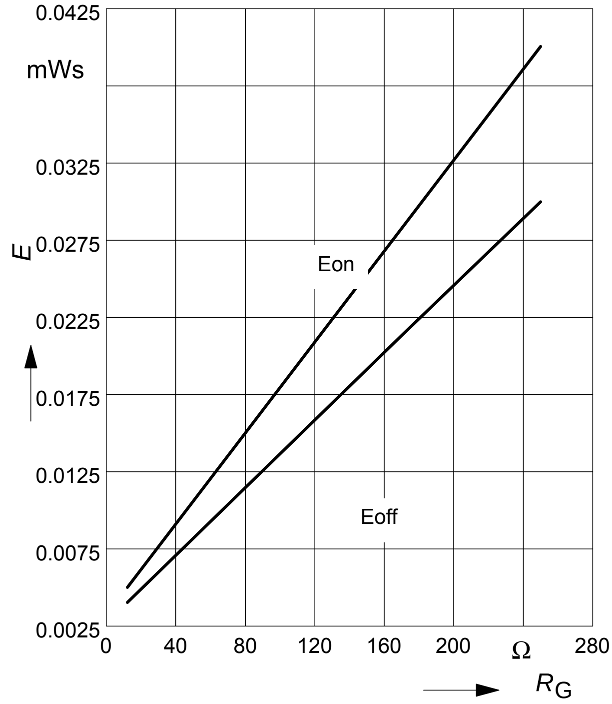
par.: V_{DS}=380V, V_{GS}=0/+13V, R_G=50Ω



16 Typ. switching losses

$E = f(R_G)$, inductive load, T_j=125°C

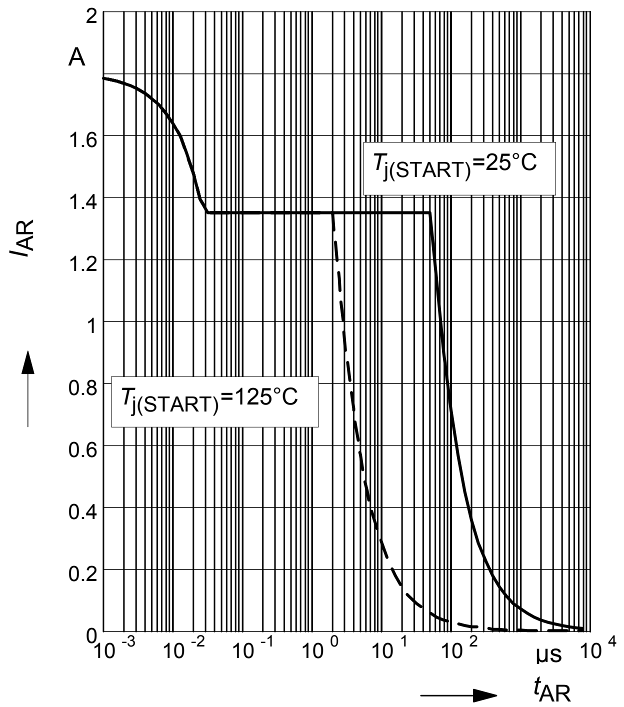
par.: V_{DS}=380V, V_{GS}=0/+13V, I_D=1.8A



17 Avalanche SOA

$I_{AR} = f(t_{AR})$

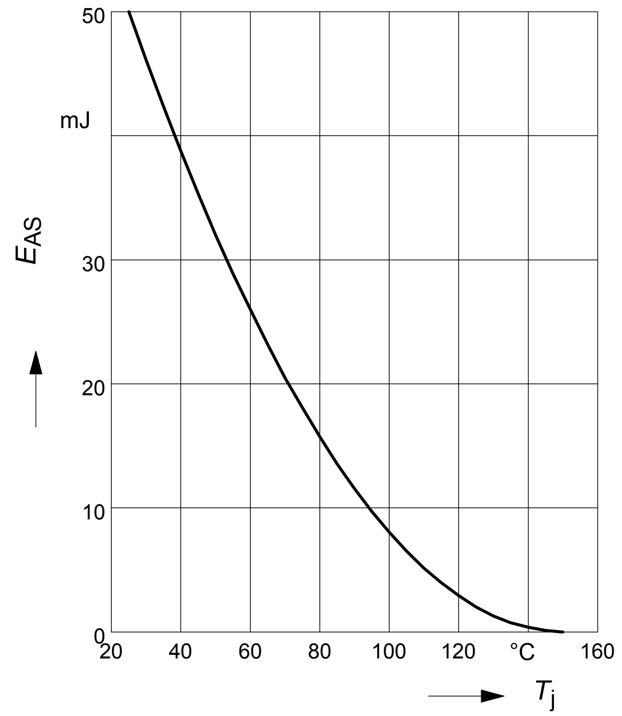
par.: $T_j \leq 150$ °C



18 Avalanche energy

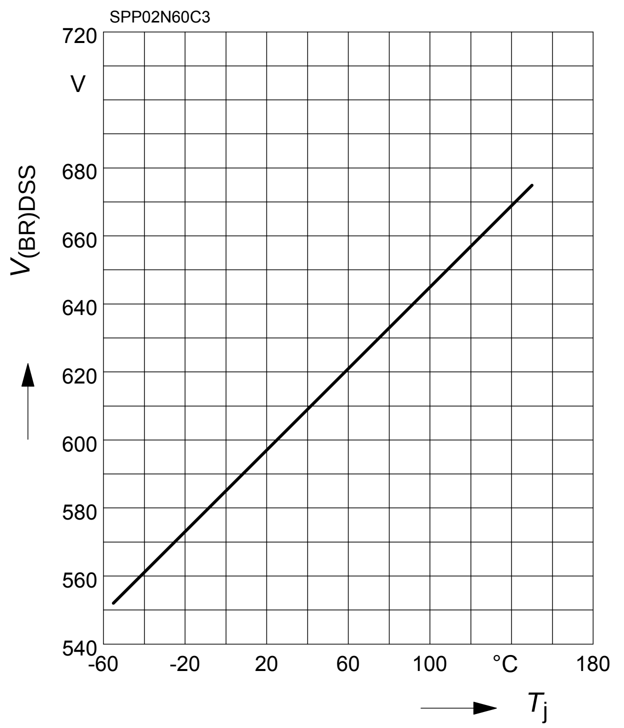
$E_{AS} = f(T_j)$

par.: I_D = 1.35 A, V_{DD} = 50 V



19 Drain-source breakdown voltage

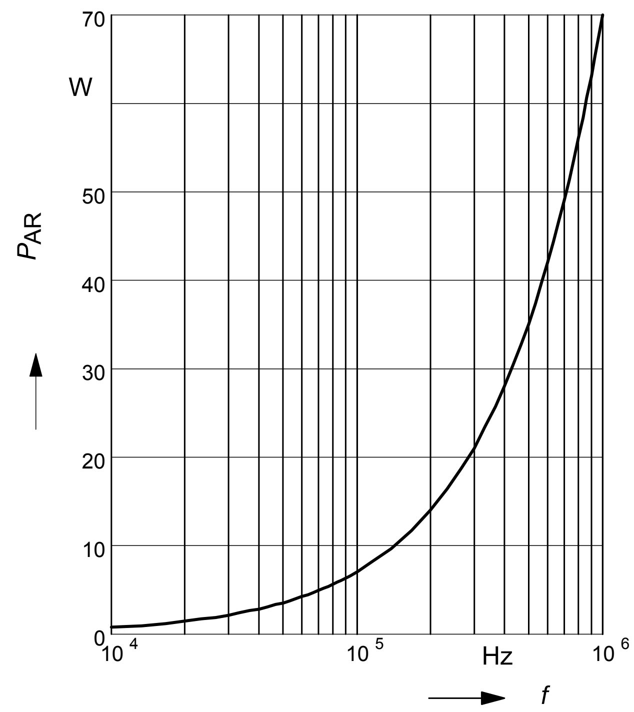
$V_{(BR)DSS} = f(T_j)$



20 Avalanche power losses

$P_{AR} = f(f)$

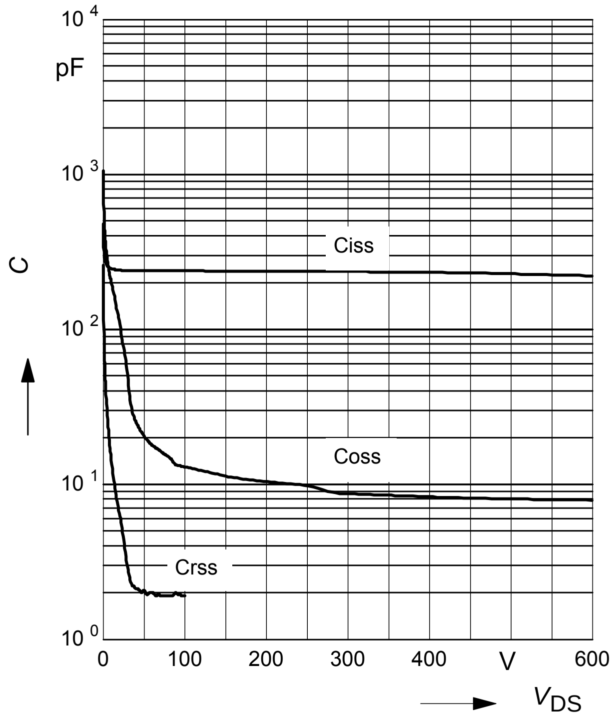
parameter: E_{AR}=0.07mJ



21 Typ. capacitances

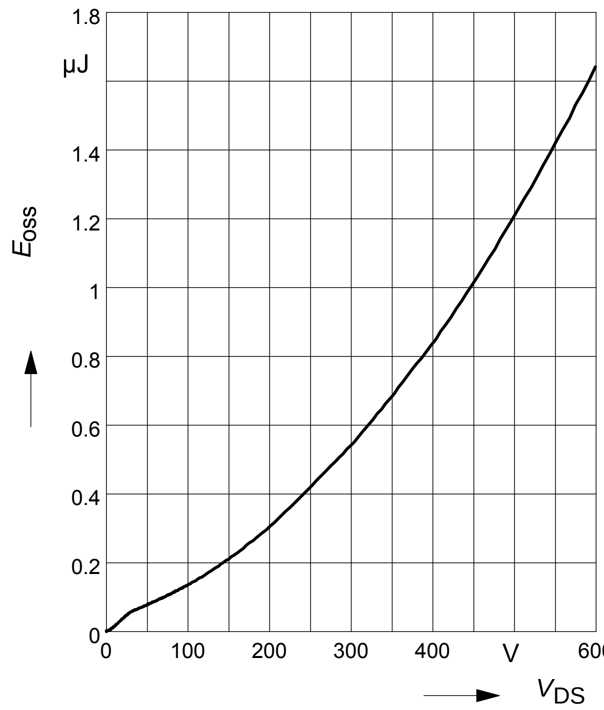
$C = f(V_{DS})$

parameter: V_{GS}=0V, f=1 MHz

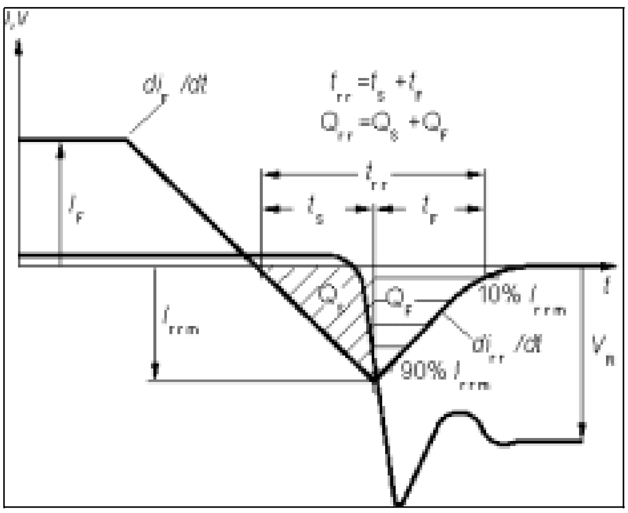


22 Typ. C_{oss} stored energy

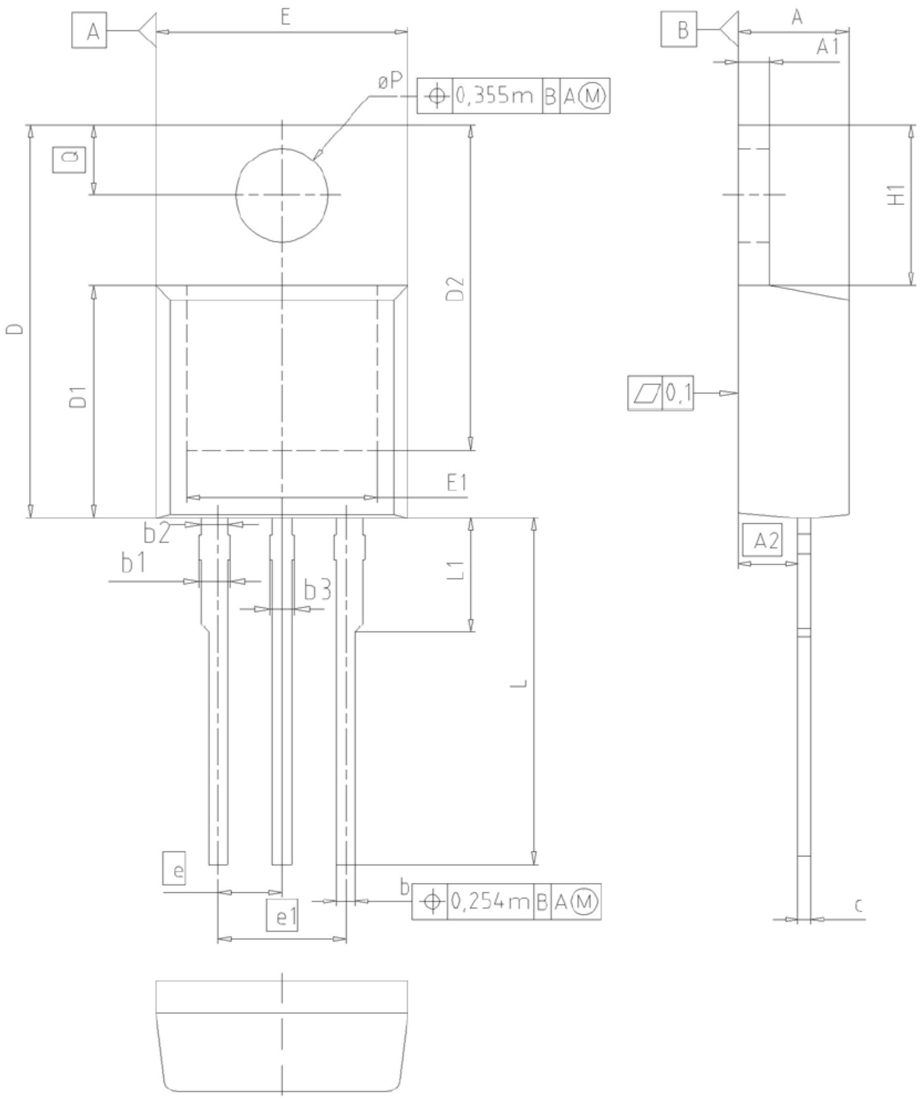
$E_{oss}=f(V_{DS})$



Definition of diodes switching characteristics



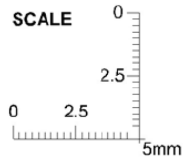
PG-TO220-3-1, PG-TO220-3-21 : Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

DOCUMENT NO.
Z8B00003318

SCALE



EUROPEAN PROJECTION

ISSUE DATE
23-08-2007

REVISION
05

Revision History

SPP02N60C3

Revision: 2017-05-18, Rev. 2.8

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.8	2017-05-18	typo correction in dv/dt diagram scaling

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Published by
Infineon Technologies AG
81726 München, Germany

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