# 16/32-Bit

Architecture

# XC2268I

16/32-Bit Single-Chip Microcontroller
with 32-Bit Performance
XC2000 Family Derivatives / Premium Line

## Data Sheet

V1.3 2014-07

Microcontrollers

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**XC2268I Data Sheet**
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| Page | Subjects (major changes since last revision) |
|---|---|
| 9 | Added XC2268I-136FxxLR to Basic Device Types |
| 10 | Moved XC2268I-136FxxL from Basic to Special Device Types |
| 128 | Added package type PG-LQFP-100-15 |

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**16/32-Bit Single-Chip Microcontroller with 32-Bit Performance**

**XC2268I (XC2000 Family)**

# 1 Summary of Features

For a quick overview and easy reference, the features of the XC2268I are summarized here.

- High-performance CPU with five-stage pipeline and MPU
  - 7.8 ns instruction cycle at 128 MHz CPU clock (single-cycle execution)
  - One-cycle 32-bit addition and subtraction with 40-bit result
  - One-cycle multiplication (16 × 16 bit)
  - Background division (32 / 16 bit) in 21 cycles
  - One-cycle multiply-and-accumulate (MAC) instructions
  - Enhanced Boolean bit manipulation facilities
  - Zero-cycle jump execution
  - Additional instructions to support HLL and operating systems
  - Register-based design with multiple variable register banks
  - Fast context switching support with two additional local register banks
  - 16 Kbytes of two-way set-associative Instruction Cache (ICache)
  - 16 Mbytes total linear address space for code and data
  - 1024 Bytes on-chip special function register area (C166 Family compatible)
  - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels providing 112 interrupt nodes
  - Selectable external inputs for interrupt generation and wake-up
  - Fastest sample-rate 7.8 ns
- Sixteen-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
  - 8 Kbytes on-chip stand-by RAM (SBRAM)
  - 2 Kbytes on-chip dual-port RAM (DPRAM)
  - 24 Kbytes on-chip data SRAM (DSRAM)
  - Up to 64 Kbytes on-chip program/data SRAM (PSRAM)
  - Up to 1 088 Kbytes on-chip program memory (Flash memory)
  - Memory content protection through Error Correction Code (ECC)
- On-Chip Peripheral Modules

  - Multi-functional general purpose timer unit with 5 timers
  - 16-channel general purpose capture/compare unit (CAPCOM2)
  - Up to four capture/compare units for flexible PWM signal generation (CCU6x)
  - Two synchronizable 12-bit A/D Converters with up to 24 channels, conversion time below 1 µs, optional data preprocessing (data reduction, range check), broken wire detection
  - Up to 10 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
  - On-chip MultiCAN interface (Rev. 2.0B active) with up to 256 message objects (Full CAN/Basic CAN) on up to 6 CAN nodes and gateway functionality
  - On-chip system timer and on-chip real time clock
- Up to 12 Mbytes external address space for code and data
  - Programmable external bus characteristics for different address ranges
  - Multiplexed or demultiplexed external address/data buses
  - Selectable address bus width
  - 16-bit or 8-bit data bus width
  - Five programmable chip-select signals
- Single power supply from 3.0 V to 5.5 V
- Power reduction and wake-up modes with flexible power management
- Programmable watchdog timer and oscillator watchdog
- Up to 75 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via Device Access Port (DAP) or JTAG interface
- 100-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

### Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the function set of the corresponding product type
- the temperature range:
  - SAF-…: -40°C to 85°C
  - SAH-…: -40°C to 110°C
  - SAK-…: -40°C to 125°C
- the package and the type of delivery.

For ordering codes for the XC2268I please contact your sales representative or local distributor.

This document describes several derivatives of the XC2268I group:

**Basic Device Types** are readily available and
**Special Device Types** are only available on request.

As this document refers to all of these derivatives, some descriptions may not apply to a specific product, in particular to the special device types.

For simplicity the term **XC2268I** is used for all derivatives throughout this document.

## 1.1 Basic Device Types

Basic device types are available and can be ordered through Infineon's direct and/or distribution channels.

**Table 1 Synopsis of XC2268I Basic Device Types**

| Derivative[1] | Flash Memory[2] | PSRAM DSRAM[3] | Capt./Comp. Modules | ADC[4] Chan. | Interfaces[4] |
|---|---|---|---|---|---|
| XC2268I-136FxxLR | 1 088 Kbytes | 64 Kbytes 24 Kbytes | CC2 CCU60/1/2/3 | 11 + 8 | 6 CAN Nodes 10 Serial Chan. |

1) xx is a placeholder for the available speed grade (in MHz).

2) Specific information about the on-chip Flash memory in **Table 3**.

3) All derivatives additionally provide 8 Kbytes SBRAM and 2 Kbytes DPRAM.

4) Specific information about the available channels in **Table 5**.
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

## 1.2 Special Device Types

Special device types are only available for high-volume applications on request.

**Table 2 Synopsis of XC2268I Special Device Types**

| Derivative[1)] | Flash Memory[2)] | PSRAM DSRAM[3)] | Capt./Comp. Modules | ADC[4)] Chan. | Interfaces[4)] |
|---|---|---|---|---|---|
| XC2268I-72FxxL | 576 Kbytes | 64 Kbytes<br>24 Kbytes | CC2<br>CCU60/1/2/3 | 11 + 8 | 6 CAN Nodes<br>10 Serial Chan. |
| XC2268I-104FxxL | 832 Kbytes | 64 Kbytes<br>24 Kbytes | CC2<br>CCU60/1/2/3 | 11 + 8 | 6 CAN Nodes<br>10 Serial Chan. |
| XC2268I-136FxxL | 1 088 Kbytes | 64 Kbytes<br>24 Kbytes | CC2<br>CCU60/1/2/3 | 11 + 8 | 6 CAN Nodes<br>10 Serial Chan. |

1) xx is a placeholder for the available speed grade (in MHz).

2) Specific information about the on-chip Flash memory in **Table 3**.

3) All derivatives additionally provide 8 Kbytes SBRAM and 2 Kbytes DPRAM.

4) Specific information about the available channels in **Table 5**.
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

## 1.3 Definition of Feature Variants

The XC2268I types are offered with several Flash memory sizes. **Table 3** describes the location of the available memory areas for each Flash memory size.

**Table 3 Flash Memory Allocation**

| Total Flash Size | Flash Area A[1)] | Flash Area B | Flash Area C |
|---|---|---|---|
| 1 088 Kbytes | $C0'0000_H$ … $C0'EFFF_H$ | $C1'0000_H$ … $D0'FFFF_H$ | n.a. |
| 832 Kbytes | $C0'0000_H$ … $C0'EFFF_H$ | $C1'0000_H$ … $CB'FFFF_H$ | $D0'0000_H$ … $D0'FFFF_H$ |
| 576 Kbytes | $C0'0000_H$ … $C0'EFFF_H$ | $C1'0000_H$ … $C7'FFFF_H$ | $D0'0000_H$ … $D0'FFFF_H$ |

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

**Table 4 Flash Memory Module Allocation (in Kbytes)**

| Total Flash Size | Flash 0[1)] | Flash 1 | Flash 2 | Flash 3 | Flash 4 |
|---|---|---|---|---|---|
| 1 088 Kbytes | 256 | 256 | 256 | 256 | 64 |
| 832 Kbytes | 256 | 256 | 256 | --- | 64 |
| 576 Kbytes | 256 | 256 | --- | --- | 64 |

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XC2268I types are offered with different interface options. **Table 5** lists the available channels for each option.

**Table 5 Interface Channel Association**

| Total Number | Available Channels |
|---|---|
| 11 ADC0 channels | CH0, CH2 … CH5, CH8 … CH11, CH13, CH15 |
| 8 ADC1 channels | CH0, CH2, CH4, CH5, CH6 (overlay: CH8 … CH11), CH12, CH13, CH14 |
| 6 CAN nodes | CAN0, CAN1, CAN2, CAN3, CAN4, CAN5<br>256 message objects |
| 10 serial channels | U0C0, U0C1, U1C0, U1C1, U2C0, U2C1, U3C0, U3C1, U4C0, U4C1 |

# 2 General Device Information

The XC2268I series (16/32-Bit Single-Chip Microcontroller with 32-Bit Performance) is a part of the Infineon XC2000 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 128 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

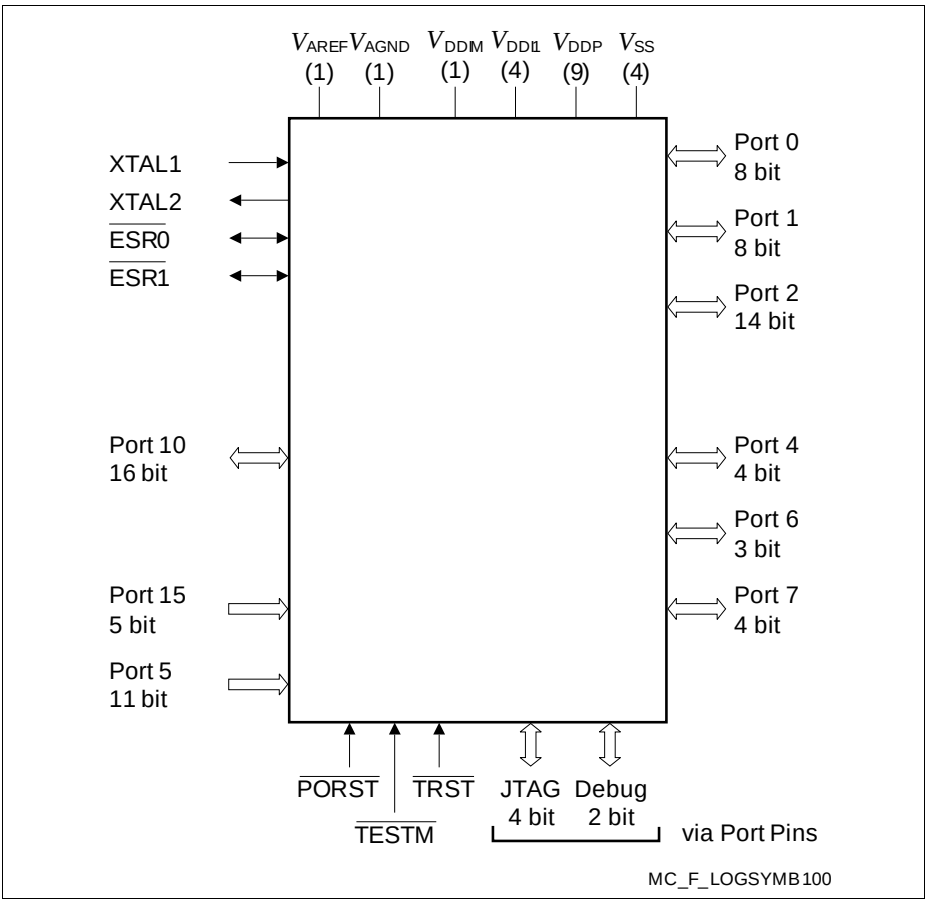


**Figure 1 XC2268I Logic Symbol**

## 2.1 Pin Configuration and Definition

The pins of the XC2268I are described in detail in **Table 6**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.

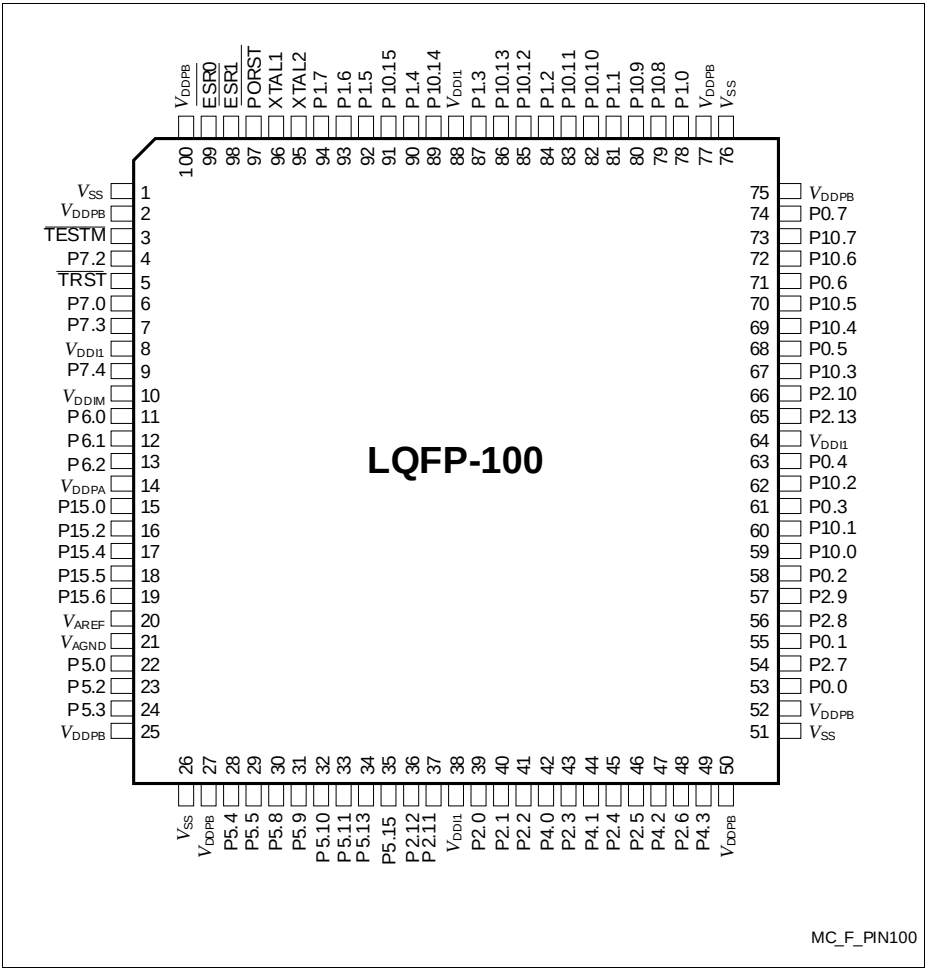


**Figure 2 XC2268I Pin Configuration (top view)**

### Key to Pin Definitions

- **Ctrl.**: The output signal for a port pin is selected by bit field PC in the associated register Px_IOCRy. Output O0 is selected by setting the respective bit field PC to $1x00_B$, output O1 is selected by $1x01_B$, etc.
  Output signal OH is controlled by hardware.
- **Type**: Indicates the pad type and its power supply domain (A, B, M, 1).
  - St: Standard pad
  - Sp: Special pad e.g. XTALx
  - DP: Double pad - can be used as standard or high speed pad
  - In: Input only pad
  - PS: Power supply pad

**Table 6 Pin Definitions and Functions**

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 3 | $\overline{\text{TESTM}}$ | I | In/B | **Testmode Enable**<br>Enables factory test modes, must be held HIGH for normal operation (connect to $V_{DDPB}$).<br>An internal pull-up device will hold this pin high when nothing is driving it. |
| 4 | P7.2 | O0 / I | St/B | **Bit 2 of Port 7, General Purpose Input/Output** |
| | EMUX0 | O1 | St/B | **External Analog MUX Control Output 0 (ADC1)** |
| | TxDC4 | O2 | St/B | **CAN Node 4 Transmit Data Output** |
| | TxDC5 | O3 | St/B | **CAN Node 5 Transmit Data Output** |
| | CCU62_CCPOS0A | I | St/B | **CCU62 Position Input 0** |
| | TDI_C | IH | St/B | **JTAG Test Data Input**<br>If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. |
| 5 | $\overline{\text{TRST}}$ | I | In/B | **Test-System Reset Input**<br>For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XC2268I's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system.<br>An internal pull-down device will hold this pin low when nothing is driving it. |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 6 | P7.0 | O0 / I | St/B | **Bit 0 of Port 7, General Purpose Input/Output** |
| | T3OUT | O1 | St/B | **GPT12E Timer T3 Toggle Latch Output** |
| | T6OUT | O2 | St/B | **GPT12E Timer T6 Toggle Latch Output** |
| | TDO_A | OH / IH | St/B | **JTAG Test Data Output / DAP1 Input/Output** If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it. |
| | ESR2_1 | I | St/B | **ESR2 Trigger Input 1** |
| | RxDC4B | I | St/B | **CAN Node 4 Receive Data Input** |
| | U4C1_DX0C | I | St/B | **USIC4 Channel 0 Receive Data Input** |
| 7 | P7.3 | O0 / I | St/B | **Bit 3 of Port 7, General Purpose Input/Output** |
| | EMUX1 | O1 | St/B | **External Analog MUX Control Output 1 (ADC1)** |
| | U0C1_DOUT | O2 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | U0C0_DOUT | O3 | St/B | **USIC0 Channel 0 Shift Data Output** |
| | CCU62_CCPOS1A | I | St/B | **CCU62 Position Input 1** |
| | TMS_C | IH | St/B | **JTAG Test Mode Selection Input** If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it. |
| | U0C1_DX0F | I | St/B | **USIC0 Channel 1 Shift Data Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 9 | P7.4 | O0 / I | St/B | **Bit 4 of Port 7, General Purpose Input/Output** |
| | EMUX2 | O1 | St/B | **External Analog MUX Control Output 2 (ADC1)** |
| | U0C1_DOUT | O2 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | U0C1_SCLKOUT | O3 | St/B | **USIC0 Channel 1 Shift Clock Output** |
| | CCU62_CCPOS2A | I | St/B | **CCU62 Position Input 2** |
| | TCK_C | IH | St/B | **DAP0/JTAG Clock Input**<br>If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.<br>If DAP pos. 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it. |
| | U0C0_DX0D | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | U0C1_DX1E | I | St/B | **USIC0 Channel 1 Shift Clock Input** |
| 11 | P6.0 | O0 / I | DA/A | **Bit 0 of Port 6, General Purpose Input/Output** |
| | EMUX0 | O1 | DA/A | **External Analog MUX Control Output 0 (ADC0)** |
| | TxDC2 | O2 | DA/A | **CAN Node 2 Transmit Data Output** |
| | $\overline{\text{BRKOUT}}$ | O3 | DA/A | **OCDS Break Signal Output** |
| | ADCx_REQGTyG | I | DA/A | **External Request Gate Input for ADC0/1** |
| | U1C1_DX0E | I | DA/A | **USIC1 Channel 1 Shift Data Input** |
| | ADC1_CH15 | I | DA/A | **Analog Input Channel 15 for ADC1** |
| 12 | P6.1 | O0 / I | DA/A | **Bit 1 of Port 6, General Purpose Input/Output** |
| | EMUX1 | O1 | DA/A | **External Analog MUX Control Output 1 (ADC0)** |
| | T3OUT | O2 | DA/A | **GPT12E Timer T3 Toggle Latch Output** |
| | U1C1_DOUT | O3 | DA/A | **USIC1 Channel 1 Shift Data Output** |
| | ADCx_REQTRyE | I | DA/A | **External Request Trigger Input for ADC0/1** |
| | RxDC2E | I | DA/A | **CAN Node 2 Receive Data Input** |
| | ESR1_6 | I | DA/A | **ESR1 Trigger Input 6** |
| | ADC1_CH14 | I | DA/A | **Analog Input Channel 14 for ADC1** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 13 | P6.2 | O0 / I | DA/A | **Bit 2 of Port 6, General Purpose Input/Output** |
| | EMUX2 | O1 | DA/A | **External Analog MUX Control Output 2 (ADC0)** |
| | T6OUT | O2 | DA/A | **GPT12E Timer T6 Toggle Latch Output** |
| | U1C1_SCLKOUT | O3 | DA/A | **USIC1 Channel 1 Shift Clock Output** |
| | U1C1_DX1C | I | DA/A | **USIC1 Channel 1 Shift Clock Input** |
| | ADC1_CH13 | I | DA/A | **Analog Input Channel 13 for ADC1** |
| 15 | P15.0 | I | In/A | **Bit 0 of Port 15, General Purpose Input** |
| | ADC1_CH0 | I | In/A | **Analog Input Channel 0 for ADC1** |
| 16 | P15.2 | I | In/A | **Bit 2 of Port 15, General Purpose Input** |
| | ADC1_CH2 | I | In/A | **Analog Input Channel 2 for ADC1** |
| | T5INA | I | In/A | **GPT12E Timer T5 Count/Gate Input** |
| 17 | P15.4 | I | In/A | **Bit 4 of Port 15, General Purpose Input** |
| | ADC1_CH4 | I | In/A | **Analog Input Channel 4 for ADC1** |
| | T6INA | I | In/A | **GPT12E Timer T6 Count/Gate Input** |
| 18 | P15.5 | I | In/A | **Bit 5 of Port 15, General Purpose Input** |
| | ADC1_CH5 | I | In/A | **Analog Input Channel 5 for ADC1** |
| | T6EUDA | I | In/A | **GPT12E Timer T6 External Up/Down Control Input** |
| 19 | P15.6 | I | In/A | **Bit 6 of Port 15, General Purpose Input** |
| | ADC1_CH6 | I | In/A | **Analog Input Channel 6 for ADC1** |
| 20 | $V_{AREF}$ | - | PS/A | **Reference Voltage for A/D Converters ADC0/1** |
| 21 | $V_{AGND}$ | - | PS/A | **Reference Ground for A/D Converters ADC0/1** |
| 22 | P5.0 | I | In/A | **Bit 0 of Port 5, General Purpose Input** |
| | ADC0_CH0 | I | In/A | **Analog Input Channel 0 for ADC0** |
| 23 | P5.2 | I | In/A | **Bit 2 of Port 5, General Purpose Input** |
| | ADC0_CH2 | I | In/A | **Analog Input Channel 2 for ADC0** |
| | TDI_A | I | In/A | **JTAG Test Data Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 24 | P5.3 | I | In/A | **Bit 3 of Port 5, General Purpose Input** |
| | ADC0_CH3 | I | In/A | **Analog Input Channel 3 for ADC0** |
| | T3INA | I | In/A | **GPT12E Timer T3 Count/Gate Input** |
| 28 | P5.4 | I | In/A | **Bit 4 of Port 5, General Purpose Input** |
| | ADC0_CH4 | I | In/A | **Analog Input Channel 4 for ADC0** |
| | CCU63_T12HRB | I | In/A | **External Run Control Input for T12 of CCU63** |
| | T3EUDA | I | In/A | **GPT12E Timer T3 External Up/Down Control Input** |
| | TMS_A | I | In/A | **JTAG Test Mode Selection Input** |
| 29 | P5.5 | I | In/A | **Bit 5 of Port 5, General Purpose Input** |
| | ADC0_CH5 | I | In/A | **Analog Input Channel 5 for ADC0** |
| | CCU60_T12HRB | I | In/A | **External Run Control Input for T12 of CCU60** |
| 30 | P5.8 | I | In/A | **Bit 8 of Port 5, General Purpose Input** |
| | ADC0_CH8 | I | In/A | **Analog Input Channel 8 for ADC0** |
| | ADC1_CH8 | I | In/A | **Analog Input Channel 8 for ADC1** |
| | CCU6x_T12HRC | I | In/A | **External Run Control Input for T12 of CCU60/1/2/3** |
| | CCU6x_T13HRC | I | In/A | **External Run Control Input for T13 of CCU60/1/2/3** |
| | U2C0_DX0F | I | In/A | **USIC2 Channel 0 Shift Data Input** |
| 31 | P5.9 | I | In/A | **Bit 9 of Port 5, General Purpose Input** |
| | ADC0_CH9 | I | In/A | **Analog Input Channel 9 for ADC0** |
| | ADC1_CH9 | I | In/A | **Analog Input Channel 9 for ADC1** |
| | CC2_T7IN | I | In/A | **CAPCOM2 Timer T7 Count Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 32 | P5.10 | I | In/A | **Bit 10 of Port 5, General Purpose Input** |
| | ADC0_CH10 | I | In/A | **Analog Input Channel 10 for ADC0** |
| | ADC1_CH10 | I | In/A | **Analog Input Channel 10 for ADC1** |
| | $\overline{\text{BRKIN_A}}$ | I | In/A | **OCDS Break Signal Input** |
| | U2C1_DX0F | I | In/A | **USIC2 Channel 1 Shift Data Input** |
| | CCU61_T13HRA | I | In/A | **External Run Control Input for T13 of CCU61** |
| 33 | P5.11 | I | In/A | **Bit 11 of Port 5, General Purpose Input** |
| | ADC0_CH11 | I | In/A | **Analog Input Channel 11 for ADC0** |
| | ADC1_CH11 | I | In/A | **Analog Input Channel 11 for ADC1** |
| 34 | P5.13 | I | In/A | **Bit 13 of Port 5, General Purpose Input** |
| | ADC0_CH13 | I | In/A | **Analog Input Channel 13 for ADC0** |
| | ERU_0B1 | I | St/B | **External Request Unit Channel 0 Input B1** |
| | CCU63_T13HRF | I | In/A | **External Run Control Input for T13 of CCU63** |
| 35 | P5.15 | I | In/A | **Bit 15 of Port 5, General Purpose Input** |
| | ADC0_CH15 | I | In/A | **Analog Input Channel 15 for ADC0** |
| | RxDC2F | I | In/A | **CAN Node 2 Receive Data Input** |
| 36 | P2.12 | O0 / I | St/B | **Bit 12 of Port 2, General Purpose Input/Output** |
| | U0C0_SELO4 | O1 | St/B | **USIC0 Channel 0 Select/Control 4 Output** |
| | U0C1_SELO3 | O2 | St/B | **USIC0 Channel 1 Select/Control 3 Output** |
| | TXDC2 | O3 | St/B | **CAN Node 2 Transmit Data Output** |
| | READY | IH | St/B | **External Bus Interface READY Input** |
| | U4C0_DX0A | I | St/B | **USIC4 Channel 0 Shift Data Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 37 | P2.11 | O0 / I | St/B | **Bit 11 of Port 2, General Purpose Input/Output** |
| | U0C0_SELO 2 | O1 | St/B | **USIC0 Channel 0 Select/Control 2 Output** |
| | U0C1_SELO 2 | O2 | St/B | **USIC0 Channel 1 Select/Control 2 Output** |
| | U3C1_DOUT | O3 | St/B | **USIC3 Channel 1 Shift Data Output** |
| | $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ | OH | St/B | **External Bus Interf. High-Byte Control Output** Can operate either as Byte High Enable ($\overline{\text{BHE}}$) or as Write strobe for High Byte ($\overline{\text{WRH}}$). |
| 39 | P2.0 | O0 / I | St/B | **Bit 0 of Port 2, General Purpose Input/Output** |
| | TxDC5 | O1 | St/B | **CAN Node 5 Transmit Data Output** |
| | CCU63_CC6 0 | O2 | St/B | **CCU63 Channel 0 Output** |
| | AD13 | OH / IH | St/B | **External Bus Interface Address/Data Line 13** |
| | RxDC0C | I | St/B | **CAN Node 0 Receive Data Input** |
| | CCU63_CC6 0INB | I | St/B | **CCU63 Channel 0 Input** |
| | T5INB | I | St/B | **GPT12E Timer T5 Count/Gate Input** |
| 40 | P2.1 | O0 / I | St/B | **Bit 1 of Port 2, General Purpose Input/Output** |
| | TxDC0 | O1 | St/B | **CAN Node 0 Transmit Data Output** |
| | CCU63_CC6 1 | O2 | St/B | **CCU63 Channel 1 Output** |
| | AD14 | OH / IH | St/B | **External Bus Interface Address/Data Line 14** |
| | RxDC5C | I | St/B | **CAN Node 5 Receive Data Input** |
| | CCU63_CC6 1INB | I | St/B | **CCU63 Channel 1 Input** |
| | T5EUDB | I | St/B | **GPT12E Timer T5 External Up/Down Control Input** |
| | ESR1_5 | I | St/B | **ESR1 Trigger Input 5** |
| | ERU_0A0 | I | St/B | **External Request Unit Channel 0 Input A0** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 41 | P2.2 | O0 / I | St/B | **Bit 2 of Port 2, General Purpose Input/Output** |
| | TxDC1 | O1 | St/B | **CAN Node 1 Transmit Data Output** |
| | CCU63_CC62 | O2 | St/B | **CCU63 Channel 2 Output** |
| | AD15 | OH / IH | St/B | **External Bus Interface Address/Data Line 15** |
| | CCU63_CC62INB | I | St/B | **CCU63 Channel 2 Input** |
| | ESR2_5 | I | St/B | **ESR2 Trigger Input 5** |
| | ERU_1A0 | I | St/B | **External Request Unit Channel 1 Input A0** |
| 42 | P4.0 | O0 / I | St/B | **Bit 0 of Port 4, General Purpose Input/Output** |
| | CC2_CC24 | O3 / I | St/B | **CAPCOM2 CC24IO Capture Inp./ Compare Out.** |
| | $\overline{CS0}$ | OH | St/B | **External Bus Interface Chip Select 0 Output** |
| 43 | P2.3 | O0 / I | St/B | **Bit 3 of Port 2, General Purpose Input/Output** |
| | U0C0_DOUT | O1 | St/B | **USIC0 Channel 0 Shift Data Output** |
| | CCU63_COUT63 | O2 | St/B | **CCU63 Channel 3 Output** |
| | CC2_CC16 | O3 / I | St/B | **CAPCOM2 CC16IO Capture Inp./ Compare Out.** |
| | A16 | OH | St/B | **External Bus Interface Address Line 16** |
| | ESR2_0 | I | St/B | **ESR2 Trigger Input 0** |
| | U0C0_DX0E | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | U0C1_DX0D | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| | RxDC0A | I | St/B | **CAN Node 0 Receive Data Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 44 | P4.1 | O0 / I | St/B | **Bit 1 of Port 4, General Purpose Input/Output** |
| | U3C0_SELO 3 | O1 | St/B | **USIC3 Channel Select/Control 3 Output** |
| | TxDC2 | O2 | St/B | **CAN Node 2 Transmit Data Output** |
| | CC2_CC25 | O3 / I | St/B | **CAPCOM2 CC25IO Capture Inp./ Compare Out.** |
| | $\overline{CS1}$ | OH | St/B | **External Bus Interface Chip Select 1 Output** |
| | CCU62_CCP OS0B | I | St/B | **CCU62 Position Input 0** |
| | T4EUDB | I | St/B | **GPT12E Timer T4 External Up/Down Control Input** |
| | ESR1_8 | I | St/B | **ESR1 Trigger Input 8** |
| 45 | P2.4 | O0 / I | St/B | **Bit 4 of Port 2, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | TxDC0 | O2 | St/B | **CAN Node 0 Transmit Data Output** |
| | CC2_CC17 | O3 / I | St/B | **CAPCOM2 CC17IO Capture Inp./ Compare Out.** |
| | A17 | OH | St/B | **External Bus Interface Address Line 17** |
| | ESR1_0 | I | St/B | **ESR1 Trigger Input 0** |
| | U0C0_DX0F | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | RxDC1A | I | St/B | **CAN Node 1 Receive Data Input** |
| 46 | P2.5 | O0 / I | St/B | **Bit 5 of Port 2, General Purpose Input/Output** |
| | U0C0_SCLK OUT | O1 | St/B | **USIC0 Channel 0 Shift Clock Output** |
| | TxDC0 | O2 | St/B | **CAN Node 0 Transmit Data Output** |
| | CC2_CC18 | O3 / I | St/B | **CAPCOM2 CC18IO Capture Inp./ Compare Out.** |
| | A18 | OH | St/B | **External Bus Interface Address Line 18** |
| | U0C0_DX1D | I | St/B | **USIC0 Channel 0 Shift Clock Input** |
| | ESR1_10 | I | St/B | **ESR1 Trigger Input 10** |
| | U3C1_DX0D | I | St/B | **USIC3 Channel 1 Shift Data Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 47 | P4.2 | O0 / I | St/B | **Bit 2 of Port 4, General Purpose Input/Output** |
| | U3C0_SCLKOUT | O1 | St/B | **USIC3 Channel 0 Shift Clock Output** |
| | TxDC2 | O2 | St/B | **CAN Node 2 Transmit Data Output** |
| | CC2_CC26 | O3 / I | St/B | **CAPCOM2 CC26IO Capture Inp./ Compare Out.** |
| | $\overline{CS2}$ | OH | St/B | **External Bus Interface Chip Select 2 Output** |
| | T2INA | I | St/B | **GPT12E Timer T2 Count/Gate Input** |
| | CCU62_CCPOS1B | I | St/B | **CCU62 Position Input 1** |
| | U3C0_DX1B | I | St/B | **USIC3 Channel 0 Shift Clock Input** |
| 48 | P2.6 | O0 / I | St/B | **Bit 6 of Port 2, General Purpose Input/Output** |
| | U0C0_SELO0 | O1 | St/B | **USIC0 Channel 0 Select/Control 0 Output** |
| | U0C1_SELO1 | O2 | St/B | **USIC0 Channel 1 Select/Control 1 Output** |
| | CC2_CC19 | O3 / I | St/B | **CAPCOM2 CC19IO Capture Inp./ Compare Out.** |
| | A19 | OH | St/B | **External Bus Interface Address Line 19** |
| | U0C0_DX2D | I | St/B | **USIC0 Channel 0 Shift Control Input** |
| | RxDC0D | I | St/B | **CAN Node 0 Receive Data Input** |
| | ESR2_6 | I | St/B | **ESR2 Trigger Input 6** |
| 49 | P4.3 | O0 / I | St/B | **Bit 3 of Port 4, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | CC2_CC27 | O3 / I | St/B | **CAPCOM2 CC27IO Capture Inp./ Compare Out.** |
| | $\overline{CS3}$ | OH | St/B | **External Bus Interface Chip Select 3 Output** |
| | RxDC2A | I | St/B | **CAN Node 2 Receive Data Input** |
| | T2EUDA | I | St/B | **GPT12E Timer T2 External Up/Down Control Input** |
| | CCU62_CCPOS2B | I | St/B | **CCU62 Position Input 2** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 53 | P0.0 | O0 / I | St/B | **Bit 0 of Port 0, General Purpose Input/Output** |
| | U1C0_DOUT | O1 | St/B | **USIC1 Channel 0 Shift Data Output** |
| | CCU61_CC60 | O3 | St/B | **CCU61 Channel 0 IOutput** |
| | A0 | OH | St/B | **External Bus Interface Address Line 0** |
| | U1C0_DX0A | I | St/B | **USIC1 Channel 0 Shift Data Input** |
| | CCU61_CC60INA | I | St/B | **CCU61 Channel 0 Input** |
| | ESR1_11 | I | St/B | **ESR1 Trigger Input 11** |
| 54 | P2.7 | O0 / I | St/B | **Bit 7 of Port 2, General Purpose Input/Output** |
| | U0C1_SELO0 | O1 | St/B | **USIC0 Channel 1 Select/Control 0 Output** |
| | U0C0_SELO1 | O2 | St/B | **USIC0 Channel 0 Select/Control 1 Output** |
| | CC2_CC20 | O3 / I | St/B | **CAPCOM2 CC20IO Capture Inp./ Compare Out.** |
| | A20 | OH | St/B | **External Bus Interface Address Line 20** |
| | U0C1_DX2C | I | St/B | **USIC0 Channel 1 Shift Control Input** |
| | RxDC1C | I | St/B | **CAN Node 1 Receive Data Input** |
| | ESR2_7 | I | St/B | **ESR2 Trigger Input 7** |
| | U4C0_DX0D | I | St/B | **USIC4 Channel 0 Shift Data Input** |
| 55 | P0.1 | O0 / I | St/B | **Bit 1 of Port 0, General Purpose Input/Output** |
| | U1C0_DOUT | O1 | St/B | **USIC1 Channel 0 Shift Data Output** |
| | TxDC0 | O2 | St/B | **CAN Node 0 Transmit Data Output** |
| | CCU61_CC61 | O3 | St/B | **CCU61 Channel 1 Output** |
| | A1 | OH | St/B | **External Bus Interface Address Line 1** |
| | U1C0_DX0B | I | St/B | **USIC1 Channel 0 Shift Data Input** |
| | CCU61_CC61INA | I | St/B | **CCU61 Channel 1 Input** |
| | U1C0_DX1A | I | St/B | **USIC1 Channel 0 Shift Clock Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 56 | P2.8 | O0 / I | DP/B | **Bit 8 of Port 2, General Purpose Input/Output** |
| | U0C1_SCLKOUT | O1 | DP/B | **USIC0 Channel 1 Shift Clock Output** |
| | EXTCLK | O2 | DP/B | **Programmable Clock Signal Output** [1] |
| | CC2_CC21 | O3 / I | DP/B | **CAPCOM2 CC21IO Capture Inp./ Compare Out.** |
| | A21 | OH | DP/B | **External Bus Interface Address Line 21** |
| | U0C1_DX1D | I | DP/B | **USIC0 Channel 1 Shift Clock Input** |
| 57 | P2.9 | O0 / I | St/B | **Bit 9 of Port 2, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | TxDC1 | O2 | St/B | **CAN Node 1 Transmit Data Output** |
| | CC2_CC22 | O3 / I | St/B | **CAPCOM2 CC22IO Capture Inp./ Compare Out.** |
| | A22 | OH | St/B | **External Bus Interface Address Line 22** |
| | CLKIN1 | I | St/B | **Clock Signal Input 1** |
| | TCK_A | IH | St/B | **DAP0/JTAG Clock Input**<br>If JTAG pos. A is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.<br>If DAP pos. 0 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it. |
| 58 | P0.2 | O0 / I | St/B | **Bit 2 of Port 0, General Purpose Input/Output** |
| | U1C0_SCLKOUT | O1 | St/B | **USIC1 Channel 0 Shift Clock Output** |
| | TxDC0 | O2 | St/B | **CAN Node 0 Transmit Data Output** |
| | CCU61_CC62 | O3 | St/B | **CCU61 Channel 2 Output** |
| | A2 | OH | St/B | **External Bus Interface Address Line 2** |
| | U1C0_DX1B | I | St/B | **USIC1 Channel 0 Shift Clock Input** |
| | CCU61_CC62INA | I | St/B | **CCU61 Channel 2 Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 59 | P10.0 | O0 / I | St/B | **Bit 0 of Port 10, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | CCU60_CC60 | O2 | St/B | **CCU60 Channel 0 Output** |
| | AD0 | OH / IH | St/B | **External Bus Interface Address/Data Line 0** |
| | CCU60_CC60INA | I | St/B | **CCU60 Channel 0 Input** |
| | ESR1_2 | I | St/B | **ESR1 Trigger Input 2** |
| | U0C0_DX0A | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | U0C1_DX0A | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| 60 | P10.1 | O0 / I | St/B | **Bit 1 of Port 10, General Purpose Input/Output** |
| | U0C0_DOUT | O1 | St/B | **USIC0 Channel 0 Shift Data Output** |
| | CCU60_CC61 | O2 | St/B | **CCU60 Channel 1 Output** |
| | AD1 | OH / IH | St/B | **External Bus Interface Address/Data Line 1** |
| | CCU60_CC61INA | I | St/B | **CCU60 Channel 1 Input** |
| | U0C0_DX1A | I | St/B | **USIC0 Channel 0 Shift Clock Input** |
| | U0C0_DX0B | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| 61 | P0.3 | O0 / I | St/B | **Bit 3 of Port 0, General Purpose Input/Output** |
| | U1C0_SELO0 | O1 | St/B | **USIC1 Channel 0 Select/Control 0 Output** |
| | U1C1_SELO1 | O2 | St/B | **USIC1 Channel 1 Select/Control 1 Output** |
| | CCU61_COUT60 | O3 | St/B | **CCU61 Channel 0 Output** |
| | A3 | OH | St/B | **External Bus Interface Address Line 3** |
| | U1C0_DX2A | I | St/B | **USIC1 Channel 0 Shift Control Input** |
| | RxDC0B | I | St/B | **CAN Node 0 Receive Data Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 62 | P10.2 | O0 / I | St/B | **Bit 2 of Port 10, General Purpose Input/Output** |
| | U0C0_SCLKOUT | O1 | St/B | **USIC0 Channel 0 Shift Clock Output** |
| | CCU60_CC62 | O2 | St/B | **CCU60 Channel 2 Output** |
| | U3C0_SELO1 | O3 | St/B | **USIC3 Channel 0 Select/Control 1 Output** |
| | AD2 | OH / IH | St/B | **External Bus Interface Address/Data Line 2** |
| | CCU60_CC62INA | I | St/B | **CCU60 Channel 2 Input** |
| | U0C0_DX1B | I | St/B | **USIC0 Channel 0 Shift Clock Input** |
| | U3C0_DX2B | I | St/B | **USIC3 Channel 0 Shift Control Input** |
| 63 | P0.4 | O0 / I | St/B | **Bit 4 of Port 0, General Purpose Input/Output** |
| | U1C1_SELO0 | O1 | St/B | **USIC1 Channel 1 Select/Control 0 Output** |
| | U1C0_SELO1 | O2 | St/B | **USIC1 Channel 0 Select/Control 1 Output** |
| | CCU61_COUT61 | O3 | St/B | **CCU61 Channel 1 Output** |
| | A4 | OH | St/B | **External Bus Interface Address Line 4** |
| | U1C1_DX2A | I | St/B | **USIC1 Channel 1 Shift Control Input** |
| | RxDC1B | I | St/B | **CAN Node 1 Receive Data Input** |
| | ESR2_8 | I | St/B | **ESR2 Trigger Input 8** |
| 65 | P2.13 | O0 / I | St/B | **Bit 13 of Port 2, General Purpose Input/Output** |
| | U2C1_SELO2 | O1 | St/B | **USIC2 Channel 1 Select/Control 2 Output** |
| | CCU63_COUT60 | O2 | St/B | **CCU63 Channel 0 Output** |
| | U4C0_DOUT | O3 | St/B | **USIC4 Channel 0 Shift Data Output** |
| | U4C0_DX0E | I | St/B | **USIC4 Channel 0 Shift Data Input** |
| | RxDC2D | I | St/B | **CAN Node 2 Receive Data Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 66 | P2.10 | O0 / I | St/B | **Bit 10 of Port 2, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | U0C0_SELO 3 | O2 | St/B | **USIC0 Channel 0 Select/Control 3 Output** |
| | CC2_CC23 | O3 / I | St/B | **CAPCOM2 CC23IO Capture Inp./ Compare Out.** |
| | A23 | OH | St/B | **External Bus Interface Address Line 23** |
| | U0C1_DX0E | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| | CAPINA | I | St/B | **GPT12E Register CAPREL Capture Input** |
| | U3C1_DX0A | I | St/B | **USIC3 Channel 1 Shift Data Input** |
| 67 | P10.3 | O0 / I | St/B | **Bit 3 of Port 10, General Purpose Input/Output** |
| | CCU60_COU T60 | O2 | St/B | **CCU60 Channel 0 Output** |
| | AD3 | OH / IH | St/B | **External Bus Interface Address/Data Line 3** |
| | U0C0_DX2A | I | St/B | **USIC0 Channel 0 Shift Control Input** |
| | U0C1_DX2A | I | St/B | **USIC0 Channel 1 Shift Control Input** |
| | U3C0_DX0A | I | St/B | **USIC3 Channel 0 Shift Data Input** |
| 68 | P0.5 | O0 / I | St/B | **Bit 5 of Port 0, General Purpose Input/Output** |
| | U1C1_SCLK OUT | O1 | St/B | **USIC1 Channel 1 Shift Clock Output** |
| | U1C0_SELO 2 | O2 | St/B | **USIC1 Channel 0 Select/Control 2 Output** |
| | CCU61_COU T62 | O3 | St/B | **CCU61 Channel 2 Output** |
| | A5 | OH | St/B | **External Bus Interface Address Line 5** |
| | U1C1_DX1A | I | St/B | **USIC1 Channel 1 Shift Clock Input** |
| | U1C0_DX1C | I | St/B | **USIC1 Channel 0 Shift Clock Input** |
| | RXDC3E | I | St/B | **CAN Node 3 Receive Data Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 69 | P10.4 | O0 / I | St/B | **Bit 4 of Port 10, General Purpose Input/Output** |
| | U0C0_SELO 3 | O1 | St/B | **USIC0 Channel 0 Select/Control 3 Output** |
| | CCU60_COU T61 | O2 | St/B | **CCU60 Channel 1 Output** |
| | U3C0_DOUT | O3 | St/B | **USIC3 Channel 0 Shift Data Output** |
| | AD4 | OH / IH | St/B | **External Bus Interface Address/Data Line 4** |
| | U0C0_DX2B | I | St/B | **USIC0 Channel 0 Shift Control Input** |
| | U0C1_DX2B | I | St/B | **USIC0 Channel 1 Shift Control Input** |
| | ESR1_9 | I | St/B | **ESR1 Trigger Input 9** |
| 70 | P10.5 | O0 / I | St/B | **Bit 5 of Port 10, General Purpose Input/Output** |
| | U0C1_SCLK OUT | O1 | St/B | **USIC0 Channel 1 Shift Clock Output** |
| | CCU60_COU T62 | O2 | St/B | **CCU60 Channel 2 Output** |
| | U2C0_DOUT | O3 | St/B | **USIC2 Channel 0 Shift Data Output** |
| | AD5 | OH / IH | St/B | **External Bus Interface Address/Data Line 5** |
| | U0C1_DX1B | I | St/B | **USIC0 Channel 1 Shift Clock Input** |
| 71 | P0.6 | O0 / I | St/B | **Bit 6 of Port 0, General Purpose Input/Output** |
| | U1C1_DOUT | O1 | St/B | **USIC1 Channel 1 Shift Data Output** |
| | TxDC1 | O2 | St/B | **CAN Node 1 Transmit Data Output** |
| | CCU61_COU T63 | O3 | St/B | **CCU61 Channel 3 Output** |
| | A6 | OH | St/B | **External Bus Interface Address Line 6** |
| | U1C1_DX0A | I | St/B | **USIC1 Channel 1 Shift Data Input** |
| | CCU61_CTR APA | I | St/B | **CCU61 Emergency Trap Input** |
| | U1C1_DX1B | I | St/B | **USIC1 Channel 1 Shift Clock Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 72 | P10.6 | O0 / I | St/B | **Bit 6 of Port 10, General Purpose Input/Output** |
| | U0C0_DOUT | O1 | St/B | **USIC0 Channel 0 Shift Data Output** |
| | TxDC4 | O2 | St/B | **CAN Node 4 Transmit Data Output** |
| | U1C0_SELO 0 | O3 | St/B | **USIC1 Channel 0 Select/Control 0 Output** |
| | AD6 | OH / IH | St/B | **External Bus Interface Address/Data Line 6** |
| | U0C0_DX0C | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | U1C0_DX2D | I | St/B | **USIC1 Channel 0 Shift Control Input** |
| | CCU60_CTR APA | I | St/B | **CCU60 Emergency Trap Input** |
| 73 | P10.7 | O0 / I | St/B | **Bit 7 of Port 10, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | CCU60_COU T63 | O2 | St/B | **CCU60 Channel 3 Output** |
| | CCU63_COU T61 | O3 | St/B | **CCU63 Channel 1 Output** |
| | AD7 | OH / IH | St/B | **External Bus Interface Address/Data Line 7** |
| | U0C1_DX0B | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| | CCU60_CCP OS0A | I | St/B | **CCU60 Position Input 0** |
| | RxDC4C | I | St/B | **CAN Node 4 Receive Data Input** |
| | T4INB | I | St/B | **GPT12E Timer T4 Count/Gate Input** |
| 74 | P0.7 | O0 / I | St/B | **Bit 7 of Port 0, General Purpose Input/Output** |
| | U1C1_DOUT | O1 | St/B | **USIC1 Channel 1 Shift Data Output** |
| | U1C0_SELO 3 | O2 | St/B | **USIC1 Channel 0 Select/Control 3 Output** |
| | TxDC3 | O3 | St/B | **CAN Node 3 Transmit Data Output** |
| | A7 | OH | St/B | **External Bus Interface Address Line 7** |
| | U1C1_DX0B | I | St/B | **USIC1 Channel 1 Shift Data Input** |
| | CCU61_CTR APB | I | St/B | **CCU61 Emergency Trap Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 78 | P1.0 | O0 / I | St/B | **Bit 0 of Port 1, General Purpose Input/Output** |
| | U1C0_MCLKOUT | O1 | St/B | **USIC1 Channel 0 Master Clock Output** |
| | U1C0_SELO4 | O2 | St/B | **USIC1 Channel 0 Select/Control 4 Output** |
| | A8 | OH | St/B | **External Bus Interface Address Line 8** |
| | ESR1_3 | I | St/B | **ESR1 Trigger Input 3** |
| | ERU_0B0 | I | St/B | **External Request Unit Channel 0 Input B0** |
| | CCU62_CTRAPB | I | St/B | **CCU62 Emergency Trap Input** |
| | T6INB | I | St/B | **GPT12E Timer T6 Count/Gate Input** |
| 79 | P10.8 | O0 / I | St/B | **Bit 8 of Port 10, General Purpose Input/Output** |
| | U0C0_MCLKOUT | O1 | St/B | **USIC0 Channel 0 Master Clock Output** |
| | U0C1_SELO0 | O2 | St/B | **USIC0 Channel 1 Select/Control 0 Output** |
| | U2C1_DOUT | O3 | St/B | **USIC2 Channel 1 Shift Data Output** |
| | AD8 | OH / IH | St/B | **External Bus Interface Address/Data Line 8** |
| | CCU60_CCPOS1A | I | St/B | **CCU60 Position Input 1** |
| | U0C0_DX1C | I | St/B | **USIC0 Channel 0 Shift Clock Input** |
| | $\overline{\text{BRKIN_B}}$ | I | St/B | **OCDS Break Signal Input** |
| | T3EUDB | I | St/B | **GPT12E Timer T3 External Up/Down Control Input** |
| | ESR2_11 | I | St/B | **ESR2 Trigger Input 11** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 80 | P10.9 | O0 / I | DP/B | **Bit 9 of Port 10, General Purpose Input/Output** |
| | U0C0_SELO 4 | O1 | DP/B | **USIC0 Channel 0 Select/Control 4 Output** |
| | U0C1_MCLK OUT | O2 | DP/B | **USIC0 Channel 1 Master Clock Output** |
| | AD9 | OH / IH | DP/B | **External Bus Interface Address/Data Line 9** |
| | CCU60_CCP OS2A | I | DP/B | **CCU60 Position Input 2** |
| | TCK_B | IH | DP/B | **DAP0/JTAG Clock Input**<br>If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.<br>If DAP pos. 1 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it. |
| | T3INB | I | DP/B | **GPT12E Timer T3 Count/Gate Input** |
| 81 | P1.1 | O0 / I | St/B | **Bit 1 of Port 1, General Purpose Input/Output** |
| | CCU62_COU T62 | O1 | St/B | **CCU62 Channel 2 Output** |
| | U1C0_SELO 5 | O2 | St/B | **USIC1 Channel 0 Select/Control 5 Output** |
| | U2C1_DOUT | O3 | St/B | **USIC2 Channel 1 Shift Data Output** |
| | A9 | OH | St/B | **External Bus Interface Address Line 9** |
| | ESR2_3 | I | St/B | **ESR2 Trigger Input 3** |
| | ERU_1B0 | I | St/B | **External Request Unit Channel 1 Input B0** |
| | U2C1_DX0C | I | St/B | **USIC2 Channel 1 Shift Data Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 82 | P10.10 | O0 / I | St/B | **Bit 10 of Port 10, General Purpose Input/Output** |
| | U0C0_SELO 0 | O1 | St/B | **USIC0 Channel 0 Select/Control 0 Output** |
| | CCU60_COU T63 | O2 | St/B | **CCU60 Channel 3 Output** |
| | AD10 | OH / IH | St/B | **External Bus Interface Address/Data Line 10** |
| | U0C0_DX2C | I | St/B | **USIC0 Channel 0 Shift Control Input** |
| | U0C1_DX1A | I | St/B | **USIC0 Channel 1 Shift Clock Input** |
| | TDI_B | IH | St/B | **JTAG Test Data Input**<br>If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. |
| 83 | P10.11 | O0 / I | St/B | **Bit 11 of Port 10, General Purpose Input/Output** |
| | U1C0_SCLK OUT | O1 | St/B | **USIC1 Channel 0 Shift Clock Output** |
| | $\overline{\text{BRKOUT}}$ | O2 | St/B | **OCDS Break Signal Output** |
| | U3C0_SELO 0 | O3 | St/B | **USIC3 Channel 0 Select/Control 0 Output** |
| | AD11 | OH / IH | St/B | **External Bus Interface Address/Data Line 11** |
| | U1C0_DX1D | I | St/B | **USIC1 Channel 0 Shift Clock Input** |
| | RxDC2B | I | St/B | **CAN Node 2 Receive Data Input** |
| | TMS_B | IH | St/B | **JTAG Test Mode Selection Input**<br>If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. |
| | U3C0_DX2A | I | St/B | **USIC3 Channel 0 Shift Control Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 84 | P1.2 | O0 / I | St/B | **Bit 2 of Port 1, General Purpose Input/Output** |
| | CCU62_CC62 | O1 | St/B | **CCU62 Channel 2 Output** |
| | U1C0_SELO6 | O2 | St/B | **USIC1 Channel 0 Select/Control 6 Output** |
| | U2C1_SCLKOUT | O3 | St/B | **USIC2 Channel 1 Shift Clock Output** |
| | A10 | OH | St/B | **External Bus Interface Address Line 10** |
| | ESR1_4 | I | St/B | **ESR1 Trigger Input 4** |
| | ERU_2A0 | I | St/B | **External Request Unit Channel 2 Input A0** |
| | CCU61_T12HRB | I | St/B | **External Run Control Input for T12 of CCU61** |
| | CCU62_CC62INA | I | St/B | **CCU62 Channel 2 Input** |
| | U2C1_DX0D | I | St/B | **USIC2 Channel 1 Shift Data Input** |
| | U2C1_DX1C | I | St/B | **USIC2 Channel 1 Shift Clock Input** |
| 85 | P10.12 | O0 / I | St/B | **Bit 12 of Port 10, General Purpose Input/Output** |
| | U1C0_DOUT | O1 | St/B | **USIC1 Channel 0 Shift Data Output** |
| | TxDC2 | O2 | St/B | **CAN Node 2 Transmit Data Output** |
| | CCU63_COUT62 | O3 | St/B | **CCU63 Channel 2 Output** |
| | TDO_B | OH / IH | St/B | **JTAG Test Data Output / DAP1 Input/Output** If DAP pos. 1 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it. |
| | AD12 | OH / IH | St/B | **External Bus Interface Address/Data Line 12** |
| | U1C0_DX0C | I | St/B | **USIC1 Channel 0 Shift Data Input** |
| | U1C0_DX1E | I | St/B | **USIC1 Channel 0 Shift Clock Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 86 | P10.13 | O0 / I | St/B | **Bit 13 of Port 10, General Purpose Input/Output** |
| | U1C0_DOUT | O1 | St/B | **USIC1 Channel 0 Shift Data Output** |
| | TxDC3 | O2 | St/B | **CAN Node 3 Transmit Data Output** |
| | U1C0_SELO 3 | O3 | St/B | **USIC1 Channel 0 Select/Control 3 Output** |
| | $\overline{WR}$/$\overline{WRL}$ | OH | St/B | **External Bus Interface Write Strobe Output** Active for each external write access, when $\overline{WR}$, active for ext. writes to the low byte, when $\overline{WRL}$. |
| | U1C0_DX0D | I | St/B | **USIC1 Channel 0 Shift Data Input** |
| 87 | P1.3 | O0 / I | St/B | **Bit 3 of Port 1, General Purpose Input/Output** |
| | CCU62_COU T63 | O1 | St/B | **CCU62 Channel 3 Output** |
| | U1C0_SELO 7 | O2 | St/B | **USIC1 Channel 0 Select/Control 7 Output** |
| | U2C0_SELO 4 | O3 | St/B | **USIC2 Channel 0 Select/Control 4 Output** |
| | A11 | OH | St/B | **External Bus Interface Address Line 11** |
| | ESR2_4 | I | St/B | **ESR2 Trigger Input 4** |
| | ERU_3A0 | I | St/B | **External Request Unit Channel 3 Input A0** |
| | CCU62_T12 HRB | I | St/B | **External Run Control Input for T12 of CCU62** |
| 89 | P10.14 | O0 / I | St/B | **Bit 14 of Port 10, General Purpose Input/Output** |
| | U1C0_SELO 1 | O1 | St/B | **USIC1 Channel 0 Select/Control 1 Output** |
| | U0C1_DOUT | O2 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | U3C0_SCLK OUT | O3 | St/B | **USIC3 Channel 0 Shift Clock Output** |
| | $\overline{RD}$ | OH | St/B | **External Bus Interface Read Strobe Output** |
| | ESR2_2 | I | St/B | **ESR2 Trigger Input 2** |
| | U0C1_DX0C | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| | RxDC3C | I | St/B | **CAN Node 3 Receive Data Input** |
| | U3C0_DX1A | I | St/B | **USIC3 Channel 0 Shift Clock Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 90 | P1.4 | O0 / I | St/B | **Bit 4 of Port 1, General Purpose Input/Output** |
| | CCU62_COUT61 | O1 | St/B | **CCU62 Channel 1 Output** |
| | U1C1_SELO4 | O2 | St/B | **USIC1 Channel 1 Select/Control 4 Output** |
| | U2C0_SELO5 | O3 | St/B | **USIC2 Channel 0 Select/Control 5 Output** |
| | A12 | OH | St/B | **External Bus Interface Address Line 12** |
| | U2C0_DX2B | I | St/B | **USIC2 Channel 0 Shift Control Input** |
| | RxDC5A | I | St/B | **CAN Node 5 Receive Data Input** |
| 91 | P10.15 | O0 / I | St/B | **Bit 15 of Port 10, General Purpose Input/Output** |
| | U1C0_SELO2 | O1 | St/B | **USIC1 Channel 0 Select/Control 2 Output** |
| | U0C1_DOUT | O2 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | U1C0_DOUT | O3 | St/B | **USIC1 Channel 0 Shift Data Output** |
| | ALE | OH | St/B | **External Bus Interf. Addr. Latch Enable Output** |
| | U0C1_DX1C | I | St/B | **USIC0 Channel 1 Shift Clock Input** |
| 92 | P1.5 | O0 / I | St/B | **Bit 5 of Port 1, General Purpose Input/Output** |
| | CCU62_COUT60 | O1 | St/B | **CCU62 Channel 0 Output** |
| | U1C1_SELO3 | O2 | St/B | **USIC1 Channel 1 Select/Control 3 Output** |
| | $\overline{\text{BRKOUT}}$ | O3 | St/B | **OCDS Break Signal Output** |
| | A13 | OH | St/B | **External Bus Interface Address Line 13** |
| | U2C0_DX0C | I | St/B | **USIC2 Channel 0 Shift Data Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 93 | P1.6 | O0 / I | St/B | **Bit 6 of Port 1, General Purpose Input/Output** |
| | CCU62_CC61 | O1 / I | St/B | **CCU62 Channel 1 Output** |
| | U1C1_SELO2 | O2 | St/B | **USIC1 Channel 1 Select/Control 2 Output** |
| | U2C0_DOUT | O3 | St/B | **USIC2 Channel 0 Shift Data Output** |
| | A14 | OH | St/B | **External Bus Interface Address Line 14** |
| | U2C0_DX0D | I | St/B | **USIC2 Channel 0 Shift Data Input** |
| | CCU62_CC61INA | I | St/B | **CCU62 Channel 1 Input** |
| | U4C1_DX0A | I | St/B | **USIC4 Channel 1 Shift Data Input** |
| 94 | P1.7 | O0 / I | St/B | **Bit 7 of Port 1, General Purpose Input/Output** |
| | CCU62_CC60 | O1 | St/B | **CCU62 Channel 0 Output** |
| | U1C1_MCLKOUT | O2 | St/B | **USIC1 Channel 1 Master Clock Output** |
| | U2C0_SCLKOUT | O3 | St/B | **USIC2 Channel 0 Shift Clock Output** |
| | A15 | OH | St/B | **External Bus Interface Address Line 15** |
| | U2C0_DX1C | I | St/B | **USIC2 Channel 0 Shift Clock Input** |
| | CCU62_CC60INA | I | St/B | **CCU62 Channel 0 Input** |
| | RxDC4E | I | St/B | **CAN Node 4 Receive Data Input** |
| 95 | XTAL2 | O | Sp/M | **Crystal Oscillator Amplifier Output** |
| 96 | XTAL1 | I | Sp/M | **Crystal Oscillator Amplifier Input**<br>To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Voltages on XTAL1 must comply to the core supply voltage $V_{DDIM}$. |
| | ESR2_9 | I | St/B | **ESR2 Trigger Input 9** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 97 | $\overline{\text{PORST}}$ | I | In/B | **Power On Reset Input**<br>A low level at this pin resets the XC2268I completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns.<br>An internal pull-up device will hold this pin high when nothing is driving it. |
| 98 | $\overline{\text{ESR1}}$ | O0 / I | St/B | **External Service Request 1**<br>After power-up, an internal weak pull-up device holds this pin high when nothing is driving it. |
| | RxDC0E | I | St/B | **CAN Node 0 Receive Data Input** |
| | U1C0_DX0F | I | St/B | **USIC1 Channel 0 Shift Data Input** |
| | U1C0_DX2C | I | St/B | **USIC1 Channel 0 Shift Control Input** |
| | U1C1_DX0C | I | St/B | **USIC1 Channel 1 Shift Data Input** |
| | U1C1_DX2B | I | St/B | **USIC1 Channel 1 Shift Control Input** |
| | U2C1_DX2C | I | St/B | **USIC2 Channel 1 Shift Control Input** |
| 99 | $\overline{\text{ESR0}}$ | O0 / I | St/B | **External Service Request 0**<br>After power-up, $\overline{\text{ESR0}}$ operates as open-drain bidirectional reset with a weak pull-up. |
| | U1C0_DX0E | I | St/B | **USIC1 Channel 0 Shift Data Input** |
| | U1C0_DX2B | I | St/B | **USIC1 Channel 0 Shift Control Input** |
| 10 | $V_{DDIM}$ | - | PS/M | **Digital Core Supply Voltage for Domain M**<br>Decouple with a ceramic capacitor, see Data Sheet for details. |
| 8, 38, 64, 88 | $V_{DDI1}$ | - | PS/1 | **Digital Core Supply Voltage for Domain 1**<br>Decouple with a ceramic capacitor, see Data Sheet for details.<br>All $V_{DDI1}$ pins must be connected to each other. |
| 14 | $V_{DDPA}$ | - | PS/A | **Digital Pad Supply Voltage for Domain A**<br>Connect decoupling capacitors to adjacent $V_{DDP}/V_{SS}$ pin pairs as close as possible to the pins.<br>*Note: The A/D Converters and ports P5, P6 and P15 are fed from supply voltage $V_{DDPA}$.* |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 2, 25, 27, 50, 52, 75, 77, 100 | $V_{DDPB}$ | - | PS/B | **Digital Pad Supply Voltage for Domain B**<br>Connect decoupling capacitors to adjacent $V_{DDP}/V_{SS}$ pin pairs as close as possible to the pins.<br>*Note: The on-chip voltage regulators and all ports except P5, P6 and P15 are fed from supply voltage $V_{DDPB}$.* |
| 1, 26, 51, 76 | $V_{SS}$ | - | PS/-- | **Digital Ground**<br>All $V_{SS}$ pins must be connected to the ground-line or ground-plane.<br>*Note: Also the exposed pad is connected internally to $V_{SS}$. To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground.*<br>*For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.* |

1) To generate the reference clock output for bus timing measurement, $f_{SYS}$ must be selected as source for EXTCLK and P2.8 must be selected as output pin. Also the high-speed clock pad must be enabled. This configuration is referred to as reference clock output signal CLKOUT.

## 2.2 Identification Registers

The identification registers describe the current version of the XC2268I and of its modules.

**Table 7 XC2268I Identification Registers**

| Short Name | Value | Address | Notes |
|---|---|---|---|
| SCU_IDMANUF | $1820_H$ | $00'F07E_H$ | |
| SCU_IDCHIP | $4801_H$ | $00'F07C_H$ | Step AA |
| SCU_IDMEM | $310F_H$ | $00'F07A_H$ | |
| SCU_IDPROG | $1313_H$ | $00'F078_H$ | |
| JTAG_ID | $101B'F083_H$ | --- | |

# 3 Functional Description

The architecture of the XC2268I combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources. This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XC2268I.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XC2268I.

## 3.1 Memory Subsystem and Organization

The memory space of the XC2268I is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

**Table 8 XC2268I Memory Map [1)]**

| Address Area | Start Loc. | End Loc. | Area Size[2)] | Notes |
|---|---|---|---|---|
| IMB register space | $FF'FF00_H$ | $FF'FFFF_H$ | 256 Bytes | |
| Reserved | $F0'0000_H$ | $FF'FEFF_H$ | < 1 Mbyte | Minus IMB registers |
| Reserved for EPSRAM | $E9'0000_H$ | $EF'FFFF_H$ | 448 Kbytes | Mirrors EPSRAM |
| Emulated PSRAM | $E8'0000_H$ | $E8'FFFF_H$ | up to 64 Kbytes | With Flash timing |
| Reserved for PSRAM | $E1'0000_H$ | $E7'FFFF_H$ | 448 Kbytes | Mirrors PSRAM |
| PSRAM | $E0'0000_H$ | $E0'FFFF_H$ | up to 64 Kbytes | Program SRAM |
| Reserved for Flash | $D1'0000_H$ | $DF'FFFF_H$ | 448 Kbytes | |
| Flash 4 | $D0'0000_H$ | $D0'FFFF_H$ | 64 Kbytes | |
| Flash 3 | $CC'0000_H$ | $CF'FFFF_H$ | 256 Kbytes | |
| Flash 2 | $C8'0000_H$ | $CB'FFFF_H$ | 256 Kbytes | |
| Flash 1 | $C4'0000_H$ | $C7'FFFF_H$ | 256 Kbytes | |
| Flash 0 | $C0'0000_H$ | $C3'FFFF_H$ | 256 Kbytes[3)] | Minus res. seg. |
| External memory area | $40'0000_H$ | $BF'FFFF_H$ | 8 Mbytes | |
| External IO area[4)] | $21'0000_H$ | $3F'FFFF_H$ | 1 984 Kbytes | |

**Table 8 XC2268I Memory Map** (cont'd)[1)]

| Address Area | Start Loc. | End Loc. | Area Size[2)] | Notes |
|---|---|---|---|---|
| MultiCAN alternate regs. | $20'8000_H$ | $20'AFFF_H$ | 12 Kbytes | Accessed via EBC |
| Reserved | $20'6800_H$ | $20'7FFF_H$ | 6 Kbytes | |
| MultiCAN registers | $20'0000_H$ | $20'3FFF_H$ | 16 Kbytes | Accessed via EBC |
| External memory area | $01'0000_H$ | $1F'FFFF_H$ | 1984 Kbytes | |
| SFR area | $00'FE00_H$ | $00'FFFF_H$ | 0.5 Kbytes | |
| Dualport RAM (DPRAM) | $00'F600_H$ | $00'FDFF_H$ | 2 Kbytes | |
| Reserved for DPRAM | $00'F200_H$ | $00'F5FF_H$ | 1 Kbytes | |
| ESFR area | $00'F000_H$ | $00'F1FF_H$ | 0.5 Kbytes | |
| XSFR area | $00'E000_H$ | $00'EFFF_H$ | 4 Kbytes | |
| Data SRAM (DSRAM) | $00'8000_H$ | $00'DFFF_H$ | 24 Kbytes | |
| External memory area | $00'0000_H$ | $00'7FFF_H$ | 32 Kbytes | |

1) Accesses to the shaded areas are reserved. In devices with external bus interface these accesses generate external bus accesses.

2) The areas marked with "<" are slightly smaller than indicated, see column "Notes".

3) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

4) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

This common memory space consists of 16 Mbytes organized as 256 segments of 64 Kbytes; each segment contains four data pages of 16 Kbytes. The entire memory space can be accessed bytewise or wordwise. Portions of the on-chip DPRAM and the register spaces (ESFR/SFR) additionally are directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls access to the program memories such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls access to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected to the high-speed system bus so that they can exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources. These include peripherals on the LXBus such as USIC or MultiCAN. The system bus allows concurrent two-way communication for maximum transfer performance.

**Up to 64 Kbytes of on-chip Program SRAM (PSRAM)** are provided to store user code or data. The PSRAM is accessed via the PMU and is optimized for code fetches. A section of the PSRAM with programmable size can be write-protected.

*Note: The actual size of the PSRAM depends on the quoted device type.*

**Up to 24 Kbytes of on-chip Data SRAM (DSRAM)** are used for storage of general user data. The DSRAM is accessed via a separate interface and is optimized for data access.

**2 Kbytes of on-chip Dual-Port RAM (DPRAM)** provide storage for user-defined variables, for the system stack, and for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, …, RL7, RH7) General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

**8 Kbytes of on-chip Stand-By SRAM (SBRAM)** provide storage for system-relevant user data that must be preserved while the major part of the device is powered down. The SBRAM is accessed via a specific interface and is powered in domain M.

**1024 bytes (2 × 512 bytes)** of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used to control and monitor functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XC2000 Family. In order to ensure upward compatibility they should either not be accessed or written with zeros.

In order to meet the requirements of designs where more memory is required than is available on chip, up to 12 Mbytes (approximately, see **Table 8**) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

**The on-chip Flash memory** stores code, constant data, and control data. The 1 088 Kbytes of on-chip Flash memory consist of 1 module of 64 Kbytes (preferably for data storage) and 4 modules of 256 Kbytes. Each module is organized in 4-Kbyte sectors.
The uppermost 4-Kbyte sector of segment 0 (located in Flash module 0) is used internally to store operation control parameters and protection information.

*Note: The actual size of the Flash memory depends on the chosen device type.*

Each sector can be separately write protected[1)], erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read access with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read access operations. Access to different Flash modules can be executed in parallel.
For Flash parameters, please see **Section 4.6**.

1) To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

### Memory Content Protection

The contents of on-chip memories can be protected against soft errors (induced e.g. by radiation) by activating the parity mechanism or the Error Correction Code (ECC).
The parity mechanism can detect a single-bit error and prevent the software from using incorrect data or executing incorrect instructions.
The ECC mechanism can detect and automatically correct single-bit errors. This supports the stable operation of the system.

It is strongly recommended to activate the ECC mechanism wherever possible because this dramatically increases the robustness of an application against such soft errors.

## 3.2 External Bus Controller

All external memory access operations are performed by a special on-chip External Bus Controller (EBC). The EBC also controls access to resources connected to the on-chip LXBus (MultiCAN and the USIC modules). The LXBus is an internal representation of the external bus that allows access to integrated peripherals and modules in the same way as to external components.

The EBC can be programmed either to Single Chip Mode, when no external memory is required, or to an external bus mode with the following selections[1]:

- Address Bus Width with a range of 0 … 24-bit
- Data Bus Width 8-bit or 16-bit
- Bus Operation Multiplexed or Demultiplexed

The bus interface uses Port 10 and Port 2 for addresses and data. In the demultiplexed bus modes, the lower addresses are output separately on Port 0 and Port 1. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines shall be assigned to Port 2.

External $\overline{CS}$ signals (address windows plus default) can be generated and output on Port 4 in order to save external glue logic. External modules can be directly connected to the common address/data bus and their individual select lines.

Important timing characteristics of the external bus interface are programmable (with registers TCONCSx/FCONCSx) to allow the user to adapt it to a wide range of different types of memories and external peripherals.
Access to very slow memories or modules with varying access times is supported by a special ‘Ready’ function. The active level of the control input signal is selectable.

In addition, up to four independent address windows may be defined (using registers ADDRSELx) to control access to resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these four address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is based on the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

## 3.3 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.

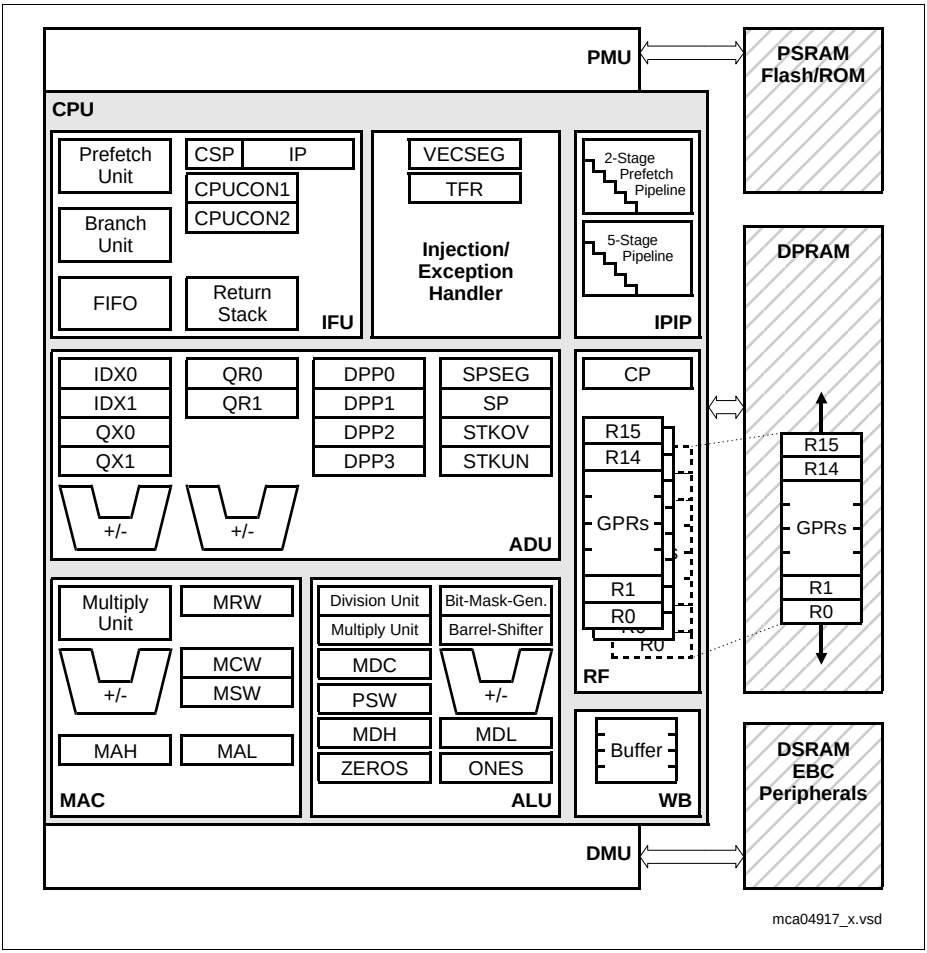


**Figure 3 CPU Block Diagram**

With this hardware most XC2268I instructions are executed in a single machine cycle of  ns @ -MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle, no matter how many bits are shifted. Also, multiplication and most MAC instructions execute in one cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast; for example, a 32-/16-bit division is started within 4 cycles while the remaining cycles are executed in the background. Another pipeline optimization, the branch target prediction, eliminates the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 word-wide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank accessed by the CPU at any time. The number of these register bank copies is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided for storage of temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area); it is accessed by the CPU with the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared with the stack pointer value during each stack access to detect stack overflow or underflow.

The high performance of the CPU hardware implementation can be best utilized by the programmer with the highly efficient XC2268I instruction set. This includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

## 3.4 Memory Protection Unit (MPU)

The XC2268I's Memory Protection Unit (MPU) protects user-specified memory areas from unauthorized read, write, or instruction fetch accesses. The MPU can protect the whole address space including the peripheral area. This completes established mechanisms such as the register security mechanism or stack overrun/underrun detection.

Four Protection Levels support flexible system programming where operating system, low level drivers, and applications run on separate levels. Each protection level permits different access restrictions for instructions and/or data.

Every access is checked (if the MPU is enabled) and an access violating the permission rules will be marked as invalid and leads to a protection trap.

A set of protection registers for each protection level specifies the address ranges and the access permissions. Applications requiring more than 4 protection levels can dynamically re-program the protection registers.

## 3.5 Memory Checker Module (MCHK)

The XC2268I's Memory Checker Module calculates a checksum (fractional polynomial division) on a block of data, often called Cyclic Redundancy Code (CRC). It is based on a 32-bit linear feedback shift register and may, therefore, also be used to generate pseudo-random numbers.

The Memory Checker Module is a 16-bit parallel input signature compression circuitry which enables error detection within a block of data stored in memory, registers, or communicated e.g. via serial communication lines. It reduces the probability of error masking due to repeated error patterns by calculating the signature of blocks of data.

The polynomial used for operation is configurable, so most of the commonly used polynomials may be used. Also, the block size for generating a CRC result is configurable via a local counter. An interrupt may be generated if testing the current data block reveals an error.

An autonomous CRC compare circuitry is included to enable redundant error detection, e.g. to enable higher safety integrity levels.

The Memory Checker Module provides enhanced fault detection (beyond parity or ECC) for data and instructions in volatile and non volatile memories. This is especially important for the safety and reliability of embedded systems.

## 3.6 Interrupt System

The architecture of the XC2268I supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Using a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed. With the PEC just one cycle is 'stolen' from the current CPU activity to perform the PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XC2268I has eight PEC channels, each with fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of 7/11[1)] CPU clocks, the XC2268I can react quickly to the occurrence of non-deterministic events.

### Interrupt Nodes and Source Selection

The interrupt system provides 112 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

### External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

### Trap Processing

The XC2268I provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called 'Hardware Traps'. A hardware trap causes an immediate system reaction similar to a standard interrupt service (branching

1) Depending if the jump cache is used or not.

to a dedicated vector table location). The occurrence of a hardware trap is also indicated by a single bit in the trap flag register (TFR). Unless another higher-priority trap service is in progress, a hardware trap will interrupt any ongoing program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Depending on the package option up to 3 External Service Request (ESR) pins are provided. The ESR unit processes their input values and allows to implement user controlled trap functions (System Requests SR0 and SR1). In this way reset, wakeup and power control can be efficiently realized.

Software interrupts are supported by the 'TRAP' instruction in combination with an individual trap (interrupt) number. Alternatively to emulate an interrupt by software a program can trigger interrupt requests by writing the Interrupt Request (IR) bit of an interrupt control register.

## 3.7 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system built into the XC2268I provides a broad range of debug and emulation features. User software running on the XC2268I can be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface. This either consists of the 2-pin Device Access Port (DAP) or of the JTAG port conforming to IEEE-1149. The debug interface can be completed with an optional break interface.

The debugger controls the OCDS with a set of dedicated registers accessible via the debug interface (DAP or JTAG). In addition the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported, as is the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing of data can be obtained via the debug interface, or via the external bus interface for increased performance.

Tracing of program execution is supported by the XC2000 Family emulation device. With this device the DAP can operate on clock rates of up to 20 MHz.

The DAP interface uses two interface signals, the JTAG interface uses four interface signals, to communicate with external circuitry. The debug interface can be amended with two optional break lines.

## 3.8 Capture/Compare Unit (CC2)

CAPCOM unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of one system clock cycle (eight cycles in staggered mode). The CAPCOM unit is typically used to handle high-speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), digital to analog (D/A) conversion, software timing, or time recording with respect to external events.

Two 16-bit timers with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, external count inputs allow event scheduling for the capture/compare registers relative to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer and programmed for capture or compare function.
All registers have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

**Table 9 Compare Modes**

| Compare Modes | Function |
|---|---|
| Mode 0 | Interrupt-only compare mode;<br>Several compare interrupts per timer period are possible |
| Mode 1 | Pin toggles on each compare match;<br>Several compare events per timer period are possible |

**Table 9 Compare Modes** (cont'd)

| Compare Modes | Function |
|---|---|
| Mode 2 | Interrupt-only compare mode;<br>Only one compare interrupt per timer period is generated |
| Mode 3 | Pin set '1' on match; pin reset '0' on compare timer overflow;<br>Only one compare event per timer period is generated |
| Double Register Mode | Two registers operate on one pin;<br>Pin toggles on each compare match;<br>Several compare events per timer period are possible |
| Single Event Mode | Generates single edges or pulses;<br>Can be used with any compare mode |

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.

## 3.9 Capture/Compare Units CCU6x

The XC2268I types feature the CCU60, CCU61, CCU62 and CCU63 unit(s).

CCU6 is a high-resolution capture and compare unit with application-specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

**Timer 12 Features**

- Three capture/compare channels, where each channel can be used either as a capture or as a compare channel.
- Supports generation of a three-phase PWM (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on a HW event (T12HR, for synchronization purposes)

**Timer 13 Features**

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period match and compare match
- Single-shot mode supported
- Automatic start on a HW event (T13HR, for synchronization purposes)

**Additional Features**

- Block commutation for brushless DC drives implemented
- Position detection via Hall sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC drives
- Output levels can be selected and adapted to the power stage

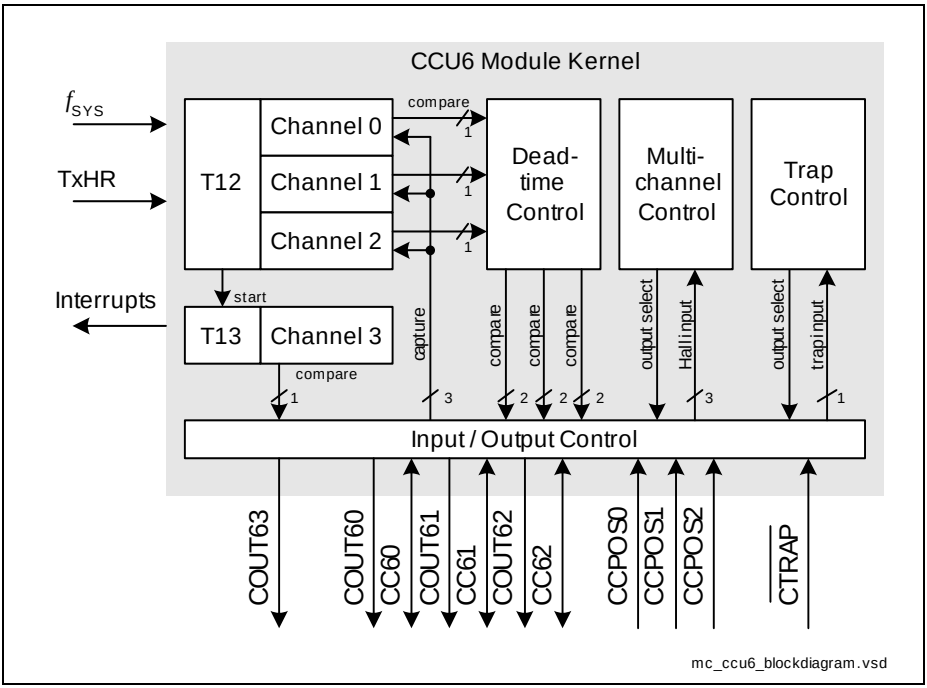


**Figure 4 CCU6 Block Diagram**

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

## 3.10 General Purpose Timer (GPT12E) Unit

The GPT12E unit is a very flexible multifunctional timer/counter structure which can be used for many different timing tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers organized in two separate modules, GPT1 and GPT2. Each timer in each module may either operate independently in a number of different modes or be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation: Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock and divided by a programmable prescaler. Counter Mode allows timer clocking in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes each timer has one associated port pin (TxIN) which serves as a gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The counting direction (up/down) for each timer can be programmed by software or altered dynamically by an external signal on a port pin (TxEUD), e.g. to facilitate position tracking.

In Incremental Interface Mode the GPT1 timers can be directly connected to the incremental position sensor signals A and B through their respective inputs TxIN and TxEUD. Direction and counting signals are internally derived from these two input signals, so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to the basic operating modes, T2 and T4 may be configured as reload or capture register for timer T3. A timer used as capture or reload register is stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at the associated input pin (TxIN). Timer T3 is reloaded with the contents of T2 or T4, triggered either by an external signal or a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be continuously generated without software intervention.

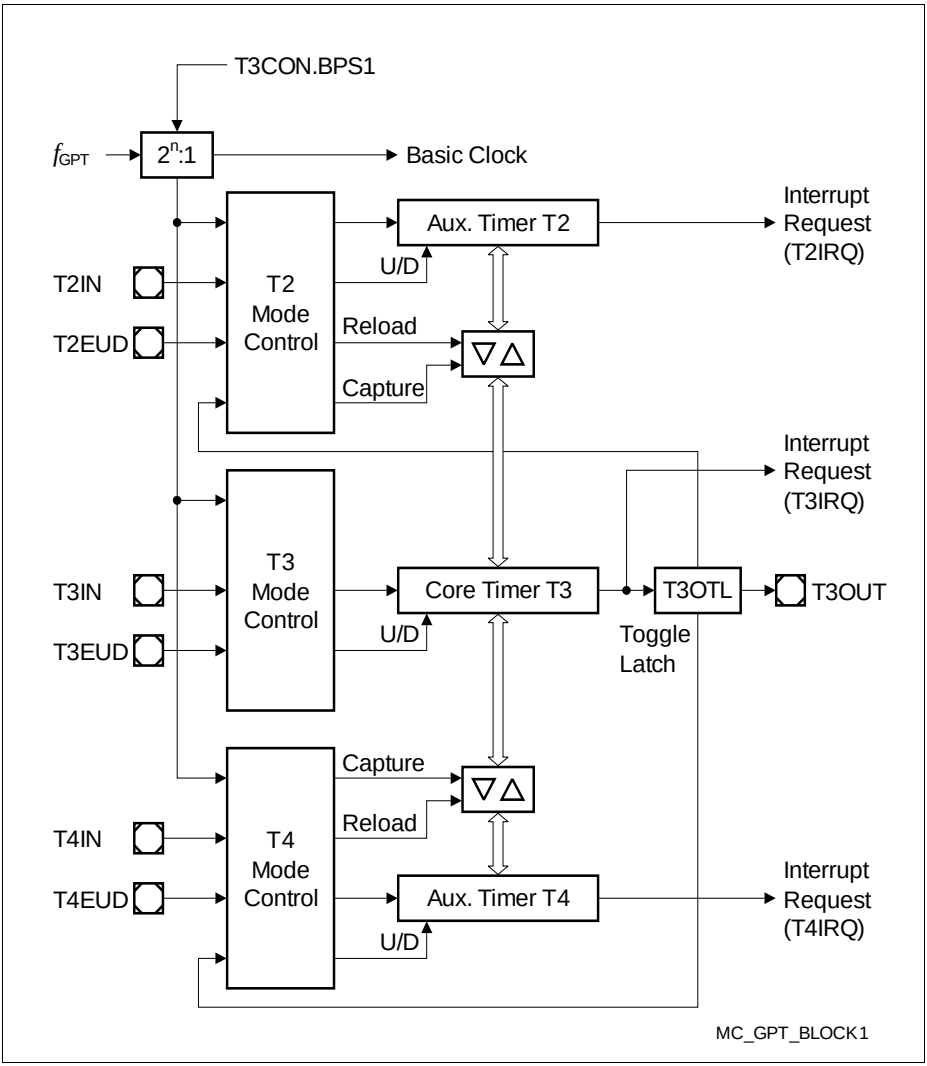


**Figure 5 Block Diagram of GPT1**

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD[1)]). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XC2268I to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

1) Exception: T5EUD is not connected to a pin.

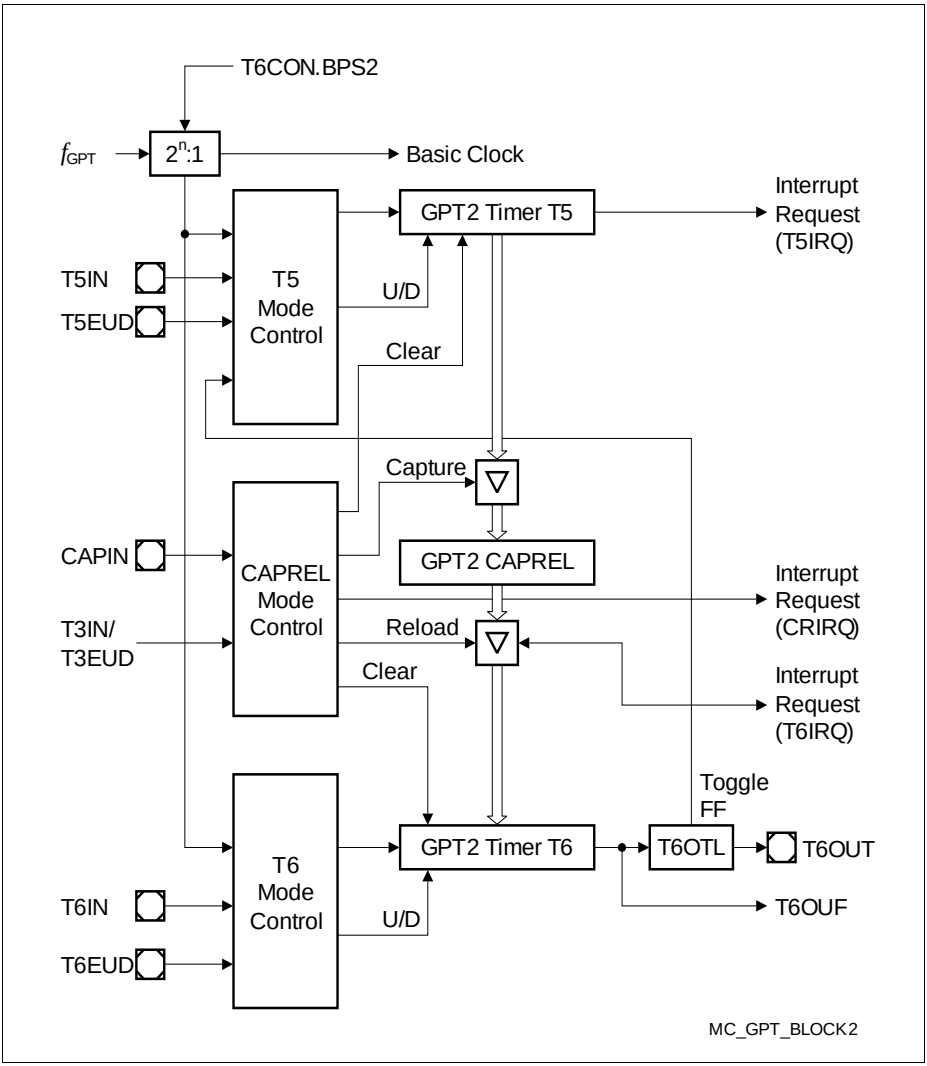


**Figure 6 Block Diagram of GPT2**

## 3.11 Real Time Clock

The Real Time Clock (RTC) module of the XC2268I can be clocked with a clock signal selected from internal sources or external sources (pins).

The RTC basically consists of a chain of divider blocks:

- Selectable 32:1 and 8:1 dividers (on - off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL) consisting of:
  - a reloadable 10-bit timer
  - a reloadable 6-bit timer
  - a reloadable 6-bit timer
  - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

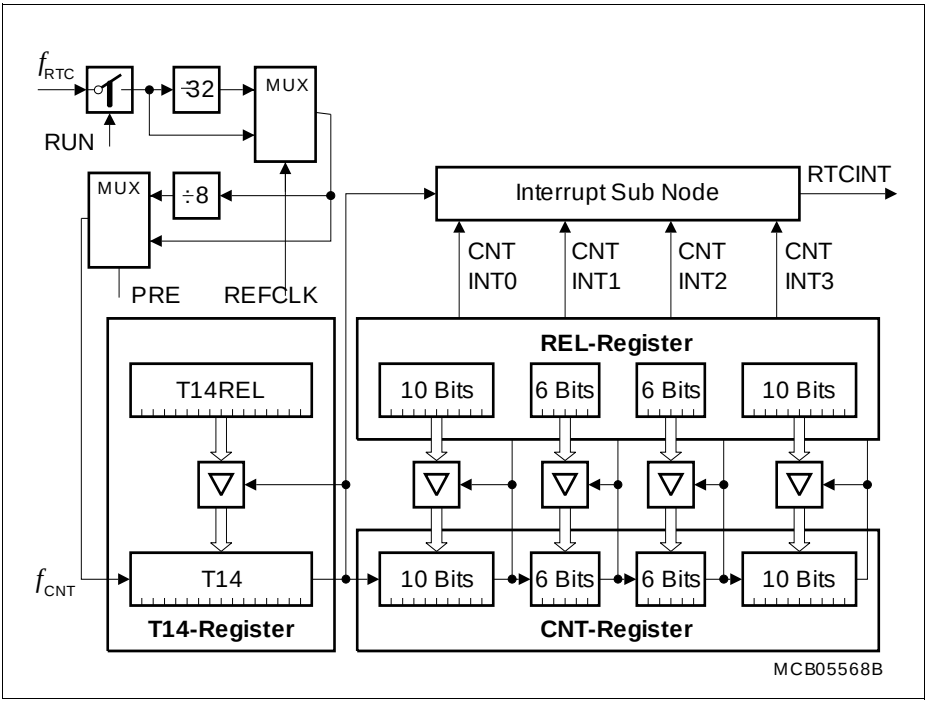


**Figure 7 RTC Block Diagram**

*Note: The registers associated with the RTC are only affected by a power reset.*

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time-based interrupt, to provide a system time tick independent of CPU frequency and other resources
- 48-bit timer for long-term measurements
- Alarm interrupt at a defined time

## 3.12 A/D Converters

For analog signal measurement, up to two 10-bit A/D converters (ADC0, ADC1) with 11 + 5 multiplexed input channels and a sample and hold circuit have been integrated on-chip. 4 inputs can be converted by both A/D converters. Conversions use the successive approximation method. The sample time (to charge the capacitors) and the conversion time are programmable so that they can be adjusted to the external circuit. The A/D converters can also operate in 8-bit conversion mode, further reducing the conversion time.

Several independent conversion result registers, selectable interrupt requests, and highly flexible conversion sequences provide a high degree of programmability to meet the application requirements. Both modules can be synchronized to allow parallel sampling of two input channels.

For applications that require more analog input channels, external analog multiplexers can be controlled automatically. For applications that require fewer analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converters of the XC2268I support two types of request sources which can be triggered by several internal and external events.

- Parallel requests are activated at the same time and then executed in a predefined sequence.
- Queued requests are executed in a user-defined sequence.

In addition, the conversion of a specific channel can be inserted into a running sequence without disturbing that sequence. All requests are arbitrated according to the priority level assigned to them.

Data reduction features reduce the number of required CPU access operations allowing the precise evaluation of analog inputs (high conversion rate) even at a low CPU speed. Result data can be reduced by limit checking or accumulation of results.

The Peripheral Event Controller (PEC) can be used to control the A/D converters or to automatically store conversion results to a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer. Each A/D converter contains eight result registers which can be concatenated to build a result FIFO. Wait-for-read mode can be enabled for each result register to prevent the loss of conversion data.

In order to decouple analog inputs from digital noise and to avoid input trigger noise, those pins used for analog input can be disconnected from the digital input stages. This can be selected for each pin separately with the Port x Digital Input Disable registers.

The Auto-Power-Down feature of the A/D converters minimizes the power consumption when no conversion is in progress.

Broken wire detection for each channel and a multiplexer test mode provide information to verify the proper operation of the analog signal sources (e.g. a sensor system).

## 3.13 Universal Serial Interface Channel Modules (USIC)

The XC2268I features the USIC modules USIC0, USIC1, USIC2, USIC3, USIC4. Each module provides two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.

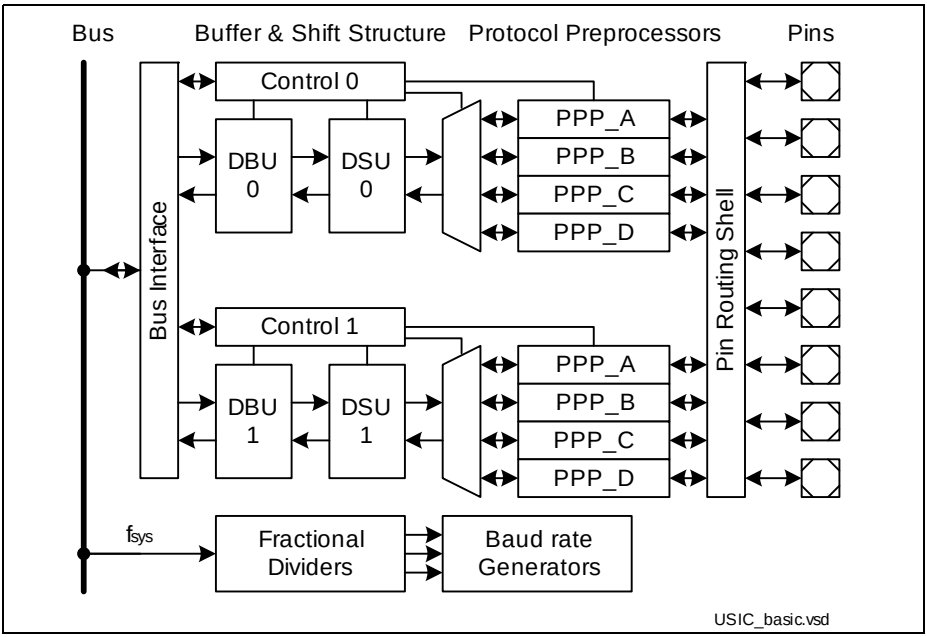


**Figure 8 General Structure of a USIC Module**

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)

### Target Protocols

Each USIC channel can receive and transmit data frames with a selectable data word width from 1 to 16 bits in each of the following protocols:

- **UART** (asynchronous serial channel)
  - module capability: maximum baud rate = $f_{SYS}$ / 4
  - data frame length programmable from 1 to 63 bits
  - MSB or LSB first
- **LIN** Support (Local Interconnect Network)
  - module capability: maximum baud rate = $f_{SYS}$ / 16
  - checksum generation under software control
  - baud rate detection possible by built-in capture event of baud rate generator
- **SSC/SPI** (synchronous serial channel with or without data buffer)
  - module capability: maximum baud rate = $f_{SYS}$ / 2, limited by loop delay
  - number of data bits programmable from 1 to 63, more with explicit stop condition
  - MSB or LSB first
  - optional control of slave select signals
- **IIC** (Inter-IC Bus)
  - supports baud rates of 100 kbit/s and 400 kbit/s
- **IIS** (Inter-IC Sound Bus)
  - module capability: maximum baud rate = $f_{SYS}$ / 2

*Note: Depending on the selected functions (such as digital filters, input synchronization stages, sample point adjustment, etc.), the maximum achievable baud rate can be limited. Please note that there may be additional delays, such as internal or external propagation delays and driver delays (e.g. for collision detection in UART mode, for IIC, etc.).*

## 3.14 MultiCAN Module

The MultiCAN module contains independently operating CAN nodes with Full-CAN functionality which are able to exchange Data and Remote Frames using a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

*Note: The number of CAN nodes and message objects depends on the selected device type.*

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to its own message object list and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

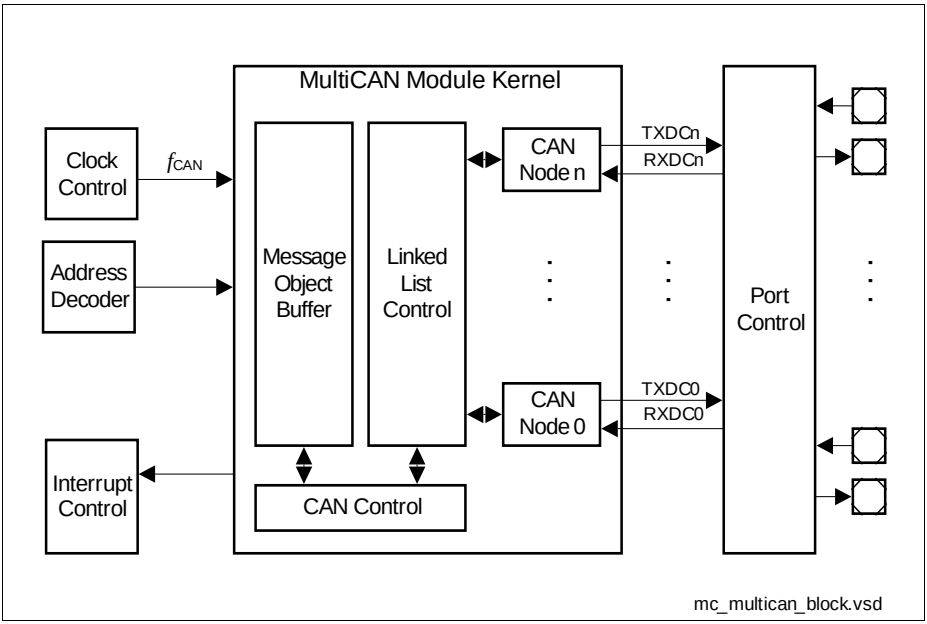


**Figure 9 Block Diagram of MultiCAN Module**

**MultiCAN Features**

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Independent CAN nodes
- Set of independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

## 3.15 System Timer

The System Timer consists of a programmable prescaler and two concatenated timers (10 bits and 6 bits). Both timers can generate interrupt requests. The clock source can be selected and the timers can also run during power reduction modes.

Therefore, the System Timer enables the software to maintain the current time for scheduling functions or for the implementation of a clock.

## 3.16 Watchdog Timer

The Watchdog Timer is one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after an application reset of the chip. It can be disabled and enabled at any time by executing the instructions DISWDT and ENWDT respectively. The software has to service the Watchdog Timer before it overflows. If this is not the case because of a hardware or software failure, the Watchdog Timer overflows, generating a prewarning interrupt and then a reset request.

The Watchdog Timer is a 16-bit timer clocked with the system clock divided by 16,384 or 256. The Watchdog Timer register is set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the Watchdog Timer is reloaded and the prescaler is cleared.

Time intervals between 3.2 µs and 13.4 s can be monitored (@ 80 MHz).

Time intervals between 2.0 µs and 8.39 s can be monitored (@ 128 MHz).

The default Watchdog Timer interval after power-up is 6.5 ms (@ 10 MHz).

## 3.17 Clock Generation

The Clock Generation Unit can generate the system clock signal $f_{SYS}$ for the XC2268I from a number of external or internal clock sources:

- External clock signals with pad voltage or core voltage levels
- External crystal or resonator using the on-chip oscillator
- On-chip clock source for operation without crystal/resonator
- Wake-up clock (ultra-low-power) to further reduce power consumption

The programmable on-chip PLL with multiple prescalers generates a clock signal for maximum system performance from standard crystals, a clock input signal, or from the on-chip clock source. See also **Section 4.7.2**.

The Oscillator Watchdog (OWD) generates an interrupt if the crystal oscillator frequency falls below a certain limit or stops completely. In this case, the system can be supplied with an emergency clock to enable operation even after an external clock failure.

All available clock signals can be output on one of two selectable pins.

## 3.18 Parallel Ports

The XC2268I provides up to 76 I/O lines which are organized into 7 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have alternate input or output functions associated with them. These alternate functions can be programmed to be assigned to various port pins to support the best utilization for a given application. For this reason, certain functions appear several times in **Table 10**.

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

**Table 10 Summary of the XC2268I's Ports**

| Port | Width | I/O | Connected Modules |
|---|---|---|---|
| P0 | 8 | I/O | EBC (A7...A0), CCU6, USIC, CAN |
| P1 | 8 | I/O | EBC (A15...A8), CCU6, USIC |
| P2 | 14 | I/O | EBC (READY, $\overline{\text{BHE}}$, A23...A16, AD15...AD13, D15...D13), CAN, CC2, GPT12E, USIC, DAP/JTAG |
| P4 | 4 | I/O | EBC ($\overline{\text{CS3}}$...$\overline{\text{CS0}}$), CC2, CAN, GPT12E, USIC |
| P5 | 11 | I | Analog Inputs, CCU6, DAP/JTAG, GPT12E, CAN |
| P6 | 3 | I/O | ADC, CAN, GPT12E |
| P7 | 5 | I/O | CAN, GPT12E, SCU, DAP/JTAG, CCU6, ADC, USIC |
| P10 | 16 | I/O | EBC (ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, AD12...AD0, D12...D0), CCU6, USIC, DAP/JTAG, CAN |
| P15 | 5 | I | Analog Inputs, GPT12E |

## 3.19 Power Management

The XC2268I provides the means to control the power it consumes either at a given time or averaged over a certain duration.
Three mechanisms can be used (and partly in parallel):

- **Supply Voltage Management** permits the temporary reduction of the supply voltage of major parts of the logic or even its complete disconnection. This drastically reduces the power consumed because it eliminates leakage current, particularly at high temperature.
  Several power reduction modes provide the best balance of power reduction and wake-up time.
- **Clock Generation Management** controls the frequency of internal and external clock signals. Clock signals for currently inactive parts of logic are disabled automatically. The user can drastically reduce the consumed power by reducing the XC2268I system clock frequency.
  External circuits can be controlled using the programmable frequency output EXTCLK.
- **Peripheral Management** permits temporary disabling of peripheral modules. Each peripheral can be disabled and enabled separately. The CPU can be switched off while the peripherals can continue to operate.

Wake-up from power reduction modes can be triggered either externally with signals generated by the external system, or internally by the on-chip wake-up timer. This supports intermittent operation of the XC2268I by generating cyclic wake-up signals. Full performance is available to quickly react to action requests while the intermittent sleep phases greatly reduce the average system power consumption.

*Note: When selecting the supply voltage and the clock source and generation method, the required parameters must be carefully written to the respective bit fields, to avoid unintended intermediate states. Recommended sequences are provided which ensure the intended operation of power supply system and clock system. Please refer to the Programmer's Guide.*

## 3.20 Instruction Set Summary

Table 11 lists the instructions of the XC2268I.
The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **"Instruction Set Manual"**.

This document also provides a detailed description of each instruction.

**Table 11 Instruction Set Summary**

| Mnemonic | Description | Bytes |
|---|---|---|
| ADD(B) | Add word (byte) operands | 2 / 4 |
| ADDC(B) | Add word (byte) operands with Carry | 2 / 4 |
| SUB(B) | Subtract word (byte) operands | 2 / 4 |
| SUBC(B) | Subtract word (byte) operands with Carry | 2 / 4 |
| MUL(U) | (Un)Signed multiply direct GPR by direct GPR (16- × 16-bit) | 2 |
| DIV(U) | (Un)Signed divide register MDL by direct GPR (16-/16-bit) | 2 |
| DIVL(U) | (Un)Signed long divide reg. MD by direct GPR (32-/16-bit) | 2 |
| CPL(B) | Complement direct word (byte) GPR | 2 |
| NEG(B) | Negate direct word (byte) GPR | 2 |
| AND(B) | Bitwise AND, (word/byte operands) | 2 / 4 |
| OR(B) | Bitwise OR, (word/byte operands) | 2 / 4 |
| XOR(B) | Bitwise exclusive OR, (word/byte operands) | 2 / 4 |
| BCLR/BSET | Clear/Set direct bit | 2 |
| BMOV(N) | Move (negated) direct bit to direct bit | 4 |
| BAND/BOR/BXOR | AND/OR/XOR direct bit with direct bit | 4 |
| BCMP | Compare direct bit to direct bit | 4 |
| BFLDH/BFLDL | Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data | 4 |
| CMP(B) | Compare word (byte) operands | 2 / 4 |
| CMPD1/2 | Compare word data to GPR and decrement GPR by 1/2 | 2 / 4 |
| CMPI1/2 | Compare word data to GPR and increment GPR by 1/2 | 2 / 4 |
| PRIOR | Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR | 2 |
| SHL/SHR | Shift left/right direct word GPR | 2 |

**Table 11 Instruction Set Summary** (cont'd)

| Mnemonic | Description | Bytes |
|---|---|---|
| ROL/ROR | Rotate left/right direct word GPR | 2 |
| ASHR | Arithmetic (sign bit) shift right direct word GPR | 2 |
| MOV(B) | Move word (byte) data | 2 / 4 |
| MOVBS/Z | Move byte operand to word op. with sign/zero extension | 2 / 4 |
| JMPA/I/R | Jump absolute/indirect/relative if condition is met | 4 |
| JMPS | Jump absolute to a code segment | 4 |
| JB(C) | Jump relative if direct bit is set (and clear bit) | 4 |
| JNB(S) | Jump relative if direct bit is not set (and set bit) | 4 |
| CALLA/I/R | Call absolute/indirect/relative subroutine if condition is met | 4 |
| CALLS | Call absolute subroutine in any code segment | 4 |
| PCALL | Push direct word register onto system stack and call absolute subroutine | 4 |
| TRAP | Call interrupt service routine via immediate trap number | 2 |
| PUSH/POP | Push/pop direct word register onto/from system stack | 2 |
| SCXT | Push direct word register onto system stack and update register with word operand | 4 |
| RET(P) | Return from intra-segment subroutine (and pop direct word register from system stack) | 2 |
| RETS | Return from inter-segment subroutine | 2 |
| RETI | Return from interrupt service subroutine | 2 |
| SBRK | Software Break | 2 |
| SRST | Software Reset | 4 |
| IDLE | Enter Idle Mode | 4 |
| PWRDN | Unused instruction[1)] | 4 |
| SRVWDT | Service Watchdog Timer | 4 |
| DISWDT/ENWDT | Disable/Enable Watchdog Timer | 4 |
| EINIT | End-of-Initialization Register Lock | 4 |
| ATOMIC | Begin ATOMIC sequence | 2 |
| EXTR | Begin EXTended Register sequence | 2 |
| EXTP(R) | Begin EXTended Page (and Register) sequence | 2 / 4 |
| EXTS(R) | Begin EXTended Segment (and Register) sequence | 2 / 4 |

**Table 11 Instruction Set Summary** (cont'd)

| Mnemonic | Description | Bytes |
|---|---|---|
| NOP | Null operation | 2 |
| CoMUL/CoMAC | Multiply (and accumulate) | 4 |
| CoADD/CoSUB | Add/Subtract | 4 |
| Co(A)SHR | (Arithmetic) Shift right | 4 |
| CoSHL | Shift left | 4 |
| CoLOAD/STORE | Load accumulator/Store MAC register | 4 |
| CoCMP | Compare | 4 |
| CoMAX/MIN | Maximum/Minimum | 4 |
| CoABS/CoRND | Absolute value/Round accumulator | 4 |
| CoMOV | Data move | 4 |
| CoNEG/NOP | Negate accumulator/Null operation | 4 |

1) The Enter Power Down Mode instruction is not used in the XC2268I, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

# 4 Electrical Parameters

The operating range for the XC2268I is defined by its electrical parameters. For proper operation the specified limits must be respected when integrating the device in its target environment.

## 4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

### 4.1.1 Absolut Maximum Rating Conditions

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on $V_{DDP}$ pins with respect to ground ($V_{SS}$) must not exceed the values defined by the absolute maximum ratings.

**Table 12 Absolute Maximum Rating Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output current on a pin when high value is driven | $I_{OH}$ SR | -30 | – | – | mA | |
| Output current on a pin when low value is driven | $I_{OL}$ SR | – | – | 30 | mA | |
| Overload current | $I_{OV}$ SR | -10 | – | 10 | mA | 1) |
| Absolute sum of overload currents | $\Sigma\lvert I_{OV}\rvert$ SR | – | – | 100 | mA | 1) |
| Junction Temperature | $T_J$ SR | -40 | – | 150 | °C | |
| Storage Temperature | $T_{ST}$ SR | -65 | – | 150 | °C | |
| Digital supply voltage for IO pads and voltage regulators | $V_{DDP}$ SR | -0.5 | – | 6.0 | V | |
| Voltage on any pin with respect to ground (Vss) | $V_{IN}$ SR | -0.5 | – | $V_{DDP}$ + 0.5 | V | $V_{IN} \le V_{DDP(max)}$ |

1) Overload condition occurs if the input voltage $V_{IN}$ is out of the absolute maximum rating range. In this case the current must be limited to the listed values by design measures.

### 4.1.2 Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XC2268I. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

*Note: Typical parameter values refer to room temperature and nominal supply voltage, minimum/maximum parameter values also include conditions of minimum/maximum temperature and minimum/maximum supply voltage. Additional details are described where applicable.*

**Table 13 Operating Conditions**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Voltage Regulator Buffer Capacitance for DMP_M | $C_{EVRM}$ SR | 1.0 | – | 4.7 | µF | 1) |
| Voltage Regulator Buffer Capacitance for DMP_1 | $C_{EVR1}$ SR | 0.68 | – | 2.2 | µF | 1)2) |
| External Load Capacitance | $C_L$ SR | – | 20[3)] | – | pF | pin out driver= default 4) |
| System frequency | $f_{SYS}$ SR | – | – | 128 | MHz | 5) |
| Overload current for analog inputs[6)] | $I_{OVA}$ SR | -2 | – | 5 | mA | not subject to production test |
| Overload current for digital inputs[6)] | $I_{OVD}$ SR | -5 | – | 5 | mA | not subject to production test |
| Overload current coupling factor for analog inputs[7)] | $K_{OVA}$ CC | – | $2.5 \times 10^{-4}$ | $1.5 \times 10^{-3}$ | - | $I_{OV} < 0$ mA; not subject to production test |
| | | – | $1.0 \times 10^{-6}$ | $1.0 \times 10^{-4}$ | - | $I_{OV} > 0$ mA; not subject to production test |
| Overload current coupling factor for digital I/O pins | $K_{OVD}$ CC | – | $1.0 \times 10^{-2}$ | $3.0 \times 10^{-2}$ | | $I_{OV} < 0$ mA; not subject to production test |
| | | – | $1.0 \times 10^{-4}$ | $5.0 \times 10^{-3}$ | | $I_{OV} > 0$ mA; not subject to production test |

**Table 13 Operating Conditions** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Absolute sum of overload currents | $\Sigma\|I_{OV}\|$ SR | – | – | 50 | mA | not subject to production test |
| Digital core supply voltage for domain M[8)] | $V_{DDIM}$ CC | – | 1.5 | – | | |
| Digital core supply voltage for domain 1[8)] | $V_{DDI1}$ CC | – | 1.5 | – | | |
| Digital supply voltage for IO pads and voltage regulators | $V_{DDP}$ SR | 3.0 | – | 5.5 | V | Operation |
| | | 3.1 | – | – | V | Power up[9)] |
| Digital ground voltage | $V_{SS}$ SR | – | 0 | – | V | |

1) To ensure the stability of the voltage regulators the EVRs must be buffered with ceramic capacitors. Separate buffer capacitors with the recomended values shall be connected as close as possible to each $V_{DDIM}$ and $V_{DDI1}$ pin to keep the resistance of the board tracks below 2 Ω. Connect all $V_{DDI1}$ pins together. The minimum capacitance value is required for proper operation under all conditions (e.g. temperature). Higher values slightly increase the startup time.

2) Use one Capacitor for each pin.

3) This is the reference load. For bigger capacitive loads, use the derating factors listed in the PAD properties section.

4) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability ($C_L$).

5) The operating frequency range may be reduced for specific device types. This is indicated in the device designation (...FxxL). 80 MHz devices are marked ...F80L.

6) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{IHmax}$ ($I_{OV} > 0$) or $V_{OV} < V_{ILmin}$ (($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed 50 mA. The supply voltages must remain within the specified limits. Proper operation under overload conditions depends on the application. Overload conditions must not occur on pin XTAL1 (powered by $V_{DDIM}$).

7) An overload current ($I_{OV}$) through a pin injects a certain error current ($I_{INJ}$) into the adjacent pins. This error current adds to the respective pins leakage current ($I_{OZ}$). The amount of error current depends on the overload current and is defined by the overload coupling factor $K_{OV}$. The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it.The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \ K_{OV})$. The additional error current may distort the input voltage on analog inputs.

8) Value is controlled by on-chip regulator

9) To ensure a stable power up sequence, the external supply voltage must reach or exceed a level of 3.1 V during power up for at least 0.5 ms.
For normal operation the complete specified voltage range is available.

### 4.1.3 Voltage Range Definition

The XC2268I timing depends on the supply voltage. If such a dependency exists the timing values are given for 2 voltage areas commonly used. The voltage areas are defined in the following tables.

**Table 14 Upper Voltage Range Definition**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Digital supply voltage for IO pads and voltage regulators | $V_{DDP}$ SR | 4.5 | 5 | 5.5 | V | $f_{SYS} \leq 100$ MHz |
| | | 4.75 | 5 | 5.25 | V | $f_{SYS} \leq 128$ MHz |

**Table 15 Lower Voltage Range Definition**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Digital supply voltage for IO pads and voltage regulators | $V_{DDP}$ SR | 3.0 | 3.3 | 4.5 | V | |

### 4.1.4 Pad Timing Definition

If not otherwise noted, all timing parameters are tested and are valid for the corresponding output pins operating in strong driver, fast edge mode.
See also **“Pad Properties” on Page 107**.

### 4.1.5 Parameter Interpretation

The parameters listed in the following include both the characteristics of the XC2268I and its demands on the system. To aid in correctly interpreting the parameters when evaluating them for a design, they are marked accordingly in the column “Symbol”:

**CC** (**C**ontroller **C**haracteristics):
The logic of the XC2268I provides signals with the specified characteristics.

**SR** (**S**ystem **R**equirement):
The external system must provide signals with the specified characteristics to the XC2268I.

## 4.2 DC Parameters

These parameters are static or average values that may be exceeded during switching transitions (e.g. output current).

Leakage current is strongly dependent on the operating temperature and the voltage level at the respective pin. The maximum values in the following tables apply under worst case conditions, i.e. maximum temperature and an input level equal to the supply voltage.
The value for the leakage current in an application can be determined by using the respective leakage derating formula (see tables) with values from that application.

The pads of the XC2268I are designed to operate in various driver modes. The DC parameter specifications refer to the pad current limits specified in **Section 4.6.4**.

### Supply Voltage Restrictions

The XC2268I can operate within a wide supply voltage range from 3.0 V to 5.5 V. However, during operation this supply voltage must remain within 10 percent of the selected nominal supply voltage. It cannot vary across the full operating voltage range.

Because of the supply voltage restriction and because electrical behavior depends on the supply voltage, the parameters are specified separately for the upper and the lower voltage range.

During operation, the supply voltages may only change with a maximum speed of dV/dt < 1 V/ms.

During power-on sequences, the supply voltages may only change with a maximum speed of dV/dt < 5 V/µs, i.e. the target supply voltage may be reached earliest after approx. 1 µs.

*Note: To limit the speed of supply voltage changes, the employment of external buffer capacitors at pins $V_{DDPA}$/$V_{DDPB}$ is recommended.*

### Pullup/Pulldown Device Behavior

Most pins of the XC2268I feature pullup or pulldown devices. For some special pins these are fixed; for the port pins they can be selected by the application.

The specified current values indicate how to load the respective pin depending on the intended signal level. **Figure 10** shows the current paths.

The shaded resistors shown in the figure may be required to compensate system pull currents that do not match the given limit values.

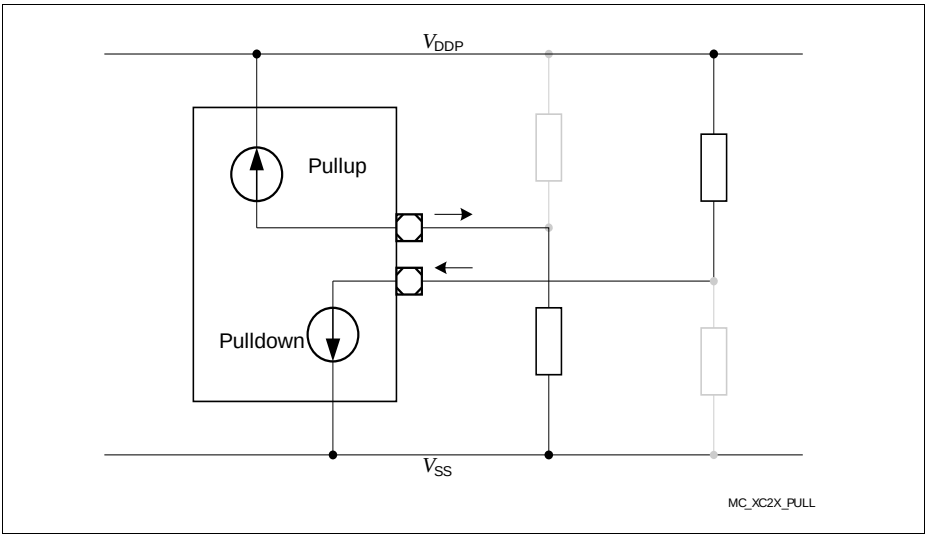


**Figure 10 Pullup/Pulldown Current Definition**

### 4.2.1 DC Parameters for Upper Voltage Area

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current $I_{OV}$.

*Note: Operating Conditions apply.*

**Table 16** is valid under the following conditions:
$V_{DDP} \geq 4.5$ V; $V_{DDPtyp} = 5$ V; $V_{DDP} \leq 5.5$ V

**Table 16 DC Characteristics for Upper Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Pin capacitance (digital inputs/outputs). To be doubled for double bond pins.[1)] | $C_{IO}$ CC | – | – | 10 | pF | not subject to production test |
| Input Hysteresis[2)] | HYS CC | 0.11 x $V_{DDP}$ | – | – | V | $R_S$ = 0 Ω |
| Absolute input leakage current on pins of analog ports[3)] | $\|I_{OZ1}\|$ CC | – | 10 | 200 | nA | $V_{IN} > 0$ V; $V_{IN} < V_{DDP}$ |
| Absolute input leakage current for all other pins. To be doubled for double bond pins.[3)1)4)] | $\|I_{OZ2}\|$ CC | – | 0.2 | 5 | µA | $T_J \leq 110$ °C; $V_{IN} < V_{DDP}$; $V_{IN} > V_{SS}$ |
| | | – | 0.2 | 15 | µA | $T_J \leq 150$ °C; $V_{IN} < V_{DDP}$; $V_{IN} > V_{SS}$ |
| Pull Level Force Current[5)] | $\|I_{PLF}\|$ SR | 250 | – | – | µA | [6)] |
| Pull Level Keep Current[7)] | $\|I_{PLK}\|$ SR | – | – | 30 | µA | [6)] |
| Input high voltage (all except XTAL1) | $V_{IH}$ SR | 0.7 x $V_{DDP}$ | – | $V_{DDP}$ + 0.3 | V | |
| Input low voltage (all except XTAL1) | $V_{IL}$ SR | -0.3 | – | 0.3 x $V_{DDP}$ | V | |
| Output High voltage[8)] | $V_{OH}$ CC | $V_{DDP}$ - 1.0 | – | – | V | $I_{OH} \geq I_{OHmax}$ |
| | | $V_{DDP}$ - 0.4 | – | – | V | $I_{OH} \geq I_{OHnom}$[9)] |

**Table 16 DC Characteristics for Upper Voltage Range** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output Low Voltage[8] | $V_{OL}$ CC | – | – | 1.0 | V | $I_{OL} \le I_{OLmax}$ |
| | | – | – | 0.4 | V | $I_{OL} \le I_{OLnom}$ [9] |

1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{IN} < V_{SS}$) or supply ripple ($V_{IN} > V_{DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current ($I_{INJ}$) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor $K_{OV}$.

4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature ($T_J$ = junction temperature [°C]): $I_{OZ} = 0.05 \times e^{(1.5 + 0.028 \times TJ>)}$ [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = $V_{DDP}$ - $V_{PIN}$ [V]): $I_{OZ} = I_{OZtempmax}$ - (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.

5) Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \le V_{ILmax}$ for a pullup; $V_{PIN} \ge V_{IHmin}$ for a pulldown.

6) These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.

7) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \ge V_{IHmin}$ for a pullup; $V_{PIN} \le V_{ILmax}$ for a pulldown.

8) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.

9) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL}$->$V_{SS}$, $V_{OH}$->$V_{DDP}$). However, only the levels for nominal output currents are verified.

### 4.2.2 DC Parameters for Lower Voltage Area

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current $I_{OV}$.

*Note: Operating Conditions apply.*

**Table 17** is valid under the following conditions:
$V_{DDP} \geq 3.0$ V; $V_{DDPtyp} = 3.3$ V; $V_{DDP} \leq 4.5$ V

**Table 17 DC Characteristics for Lower Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Pin capacitance (digital inputs/outputs). To be doubled for double bond pins.[1)] | $C_{IO}$ CC | – | – | 10 | pF | not subject to production test |
| Input Hysteresis[2)] | HYS CC | 0.07 x $V_{DDP}$ | – | – | V | $R_S$ = 0 Ω |
| Absolute input leakage current on pins of analog ports[3)] | $\|I_{OZ1}\|$ CC | – | 10 | 200 | nA | $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$ |
| Absolute input leakage current for all other pins. To be doubled for double bond pins.[3)1)4)] | $\|I_{OZ2}\|$ CC | – | 0.2 | 2.5 | µA | $T_J \leq 110$ °C; $V_{IN} < V_{DDP}$; $V_{IN} > V_{SS}$ |
| | | – | 0.2 | 8 | µA | $T_J \leq 150$ °C; $V_{IN} < V_{DDP}$; $V_{IN} > V_{SS}$ |
| Pull Level Force Current[5)] | $\|I_{PLF}\|$ SR | 150 | – | – | | [6)] |
| Pull Level Keep Current[7)] | $\|I_{PLK}\|$ SR | – | – | 10 | µA | [6)] |
| Input high voltage (all except XTAL1) | $V_{IH}$ SR | 0.7 x $V_{DDP}$ | – | $V_{DDP}$ + 0.3 | V | |
| Input low voltage (all except XTAL1) | $V_{IL}$ SR | -0.3 | – | 0.3 x $V_{DDP}$ | V | |
| Output High voltage[8)] | $V_{OH}$ CC | $V_{DDP}$ - 1.0 | – | – | V | $I_{OH} \geq I_{OHmax}$ |
| | | $V_{DDP}$ - 0.4 | – | – | V | $I_{OH} \geq I_{OHnom}$[9)] |

**Table 17 DC Characteristics for Lower Voltage Range** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output Low Voltage[8)] | $V_{OL}$ CC | – | – | 1.0 | V | $I_{OL} \le I_{OLmax}$ |
| | | – | – | 0.4 | V | $I_{OL} \le I_{OLnom}$ [10)] |

1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{IN} < V_{SS}$) or supply ripple ($V_{IN} > V_{DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current ($I_{INJ}$) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor $K_{OV}$.

4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature ($T_J$ = junction temperature [°C]): $I_{OZ} = 0.05 \times e^{(1.5 + 0.028 \times TJ>)}$ [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = $V_{DDP}$ - $V_{PIN}$ [V]): $I_{OZ} = I_{OZtempmax}$ - (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.

5) Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} <= V_{IL}$ for a pullup; $V_{PIN} >= V_{IH}$ for a pulldown.

6) These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.

7) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} >= V_{IH}$ for a pullup; $V_{PIN} <= V_{IL}$ for a pulldown.

8) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.

9) As a rule, with decreasing output current the output levels approach the respective supply level (VOL->VSS, VOH->VDDP). However, only the levels for nominal output currents are verified.

10) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL}$->$V_{SS}$, $V_{OH}$->$V_{DDP}$). However, only the levels for nominal output currents are verified.

### 4.2.3 Power Consumption

The power consumed by the XC2268I depends on several factors such as supply voltage, operating frequency, active circuits, and operating temperature. The power consumption specified here consists of two components:

- The switching current $I_S$ depends on the device activity
- The leakage current $I_{LK}$ depends on the device temperature

To determine the actual power consumption, always both components, switching current $I_S$ and leakage current $I_{LK}$ must be added:

$I_{DDP} = I_S + I_{LK}$.

*Note: The power consumption values are not subject to production test. They are verified by design/characterization.*
*To determine the total power consumption for dimensioning the external power supply, also the pad driver currents must be considered.*

The given power consumption parameters and their values refer to specific operating conditions:

- **Active mode**:
  Regular operation, i.e. peripherals are active, code execution out of Flash.
- **Stopover mode**:
  Crystal oscillator and PLL stopped, Flash switched off, clock in domain DMP_1 stopped.
- **Standby mode**:
  Voltage domain DMP_1 switched off completely, power supply control switched off. Voltage domain DMP_M is supplied by the ultra low power embedded voltage regulator (ULPEVR). The standard regulator (EVR_M) is switched off.

*Note: The maximum values cover the complete specified operating range of all manufactured devices.*
*The typical values refer to average devices under typical conditions, such as nominal supply voltage, room temperature, application-oriented activity.*
*After a power reset, the decoupling capacitors for $V_{DDIM}$ and $V_{DDI1}$ are charged with the maximum possible current.*

For additional information, please refer to **Section 5.2, Thermal Considerations**.

*Note: Operating Conditions apply.*

**Table 18 Switching Power Consumption**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Power supply current (active) with all peripherals active and EVVRs on | $I_{SACT}$ CC | – | 10 + 1.0 x $f_{SYS}$ 1) | 15 + 1.5 x $f_{SYS}$ 1) | mA | 2)3) |
| Power supply current in standby mode 4) | $I_{SSB}$ CC | – | 130 | 150 | µA | Upper voltage range |
| | | – | 100 | 110 | µA | Lower voltage range |
| Power supply current in stopover mode, EVVRs on | $I_{SSO}$ CC | – | 1.6 | 4 | mA | |

1) $f_{SYS}$ in MHz.

2) The pad supply voltage pins ($V_{DDPB}$) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers input stages are switched.
In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to 3 + 1.0 x $f_{SYS}$.

3) Please consider the additional conditions described in section "Active Mode Power Supply Current".

4) These values are valid if the voltage validation circuits for $V_{DDPB}$ (SWD) and $V_{DDIM}$ (PVC_M) are off. Leaving SWD and PVC_M active adds another 90 µA.

### Active Mode Power Supply Current

The actual power supply current in active mode not only depends on the system frequency but also on the configuration of the XC2268I's subsystem.

Besides the power consumed by the device logic the power supply pins also provide the current that flows through the pin output drivers.
A small current is consumed because the drivers' input stages are switched.

The IO power domains can be supplied separately. Power domain A ($V_{DDPA}$) supplies the A/D converters and Port 6. Power domain B ($V_{DDPB}$) supplies the on-chip EVVRs and all other ports.
During operation domain A draws a maximum current of 1.5 mA for each active A/D converter module from $V_{DDPA}$.

In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to (3 + 1.0×$f_{SYS}$) mA.

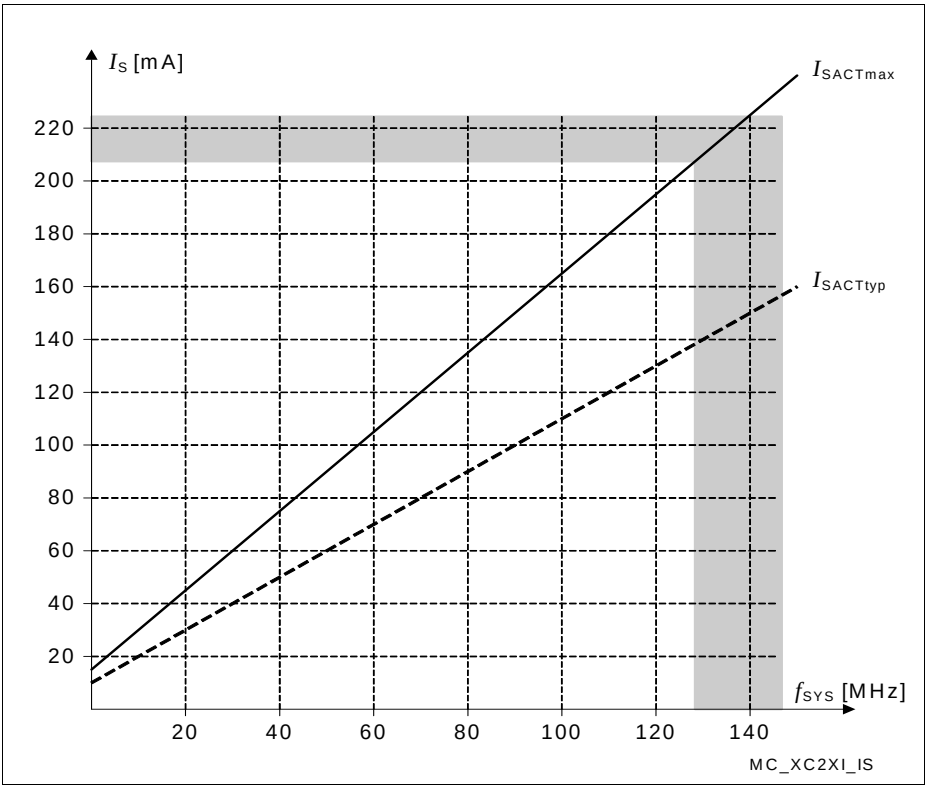


**Figure 11 Supply Current in Active Mode as a Function of Frequency**

*Note: Operating Conditions apply.*

**Table 19 Leakage Power Consumption**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Leakage supply current (DMP_1 off)[1] | $I_{LK0}$ CC | – | 20 | 35 | µA | $T_J$= 25 °C[2] |
| | | – | 115 | 330 | µA | $T_J$= 85 °C[2] |
| | | – | 270 | 880 | µA | $T_J$= 125 °C[2] |
| | | – | 420 | 1 450 | µA | $T_J$= 150 °C[2] |
| Leakage supply current (DMP_1 powered)[1] | $I_{LK1}$ CC | – | 0.03 | 0.05 | mA | $T_J$= 25 °C[2] |
| | | – | 0.7 | 1.7 | mA | $T_J$= 85 °C[2] |
| | | – | 3.0 | 8.3 | mA | $T_J$= 125 °C[2] |
| | | – | 6.4 | 18.5 | mA | $T_J$= 150 °C[2] |

1) The supply current caused by leakage depends mainly on the junction temperature and the supply voltage. The temperature difference between the junction temperature $T_J$ and the ambient temperature $T_A$ must be taken into account. As this fraction of the supply current does not depend on device activity, it must be added to other power consumption values.

2) All inputs (including pins configured as inputs) are set at 0 V to 0.1 V or at $V_{DDP}$ - 0.1 V to $V_{DDP}$ and all outputs (including pins configured as outputs) are disconnected.

*Note: A fraction of the leakage current flows through domain DMP_A (pin $V_{DDPA}$). This current can be calculated as* 7 000 $\times e^{-\alpha}$, with $\alpha$ = 5 000 / (273 + 1.3$\times T_J$). For $T_J$ = 150°C, this results in a current of 160 $\mu$A.

The leakage power consumption can be calculated according to the following formula:

$I_{LK0}$ = 500 000 + $e^{-\alpha}$, with $\alpha$ = 3 000 / (273 + B$\times T_J$) must be tagged “PWR_Management”

Parameter B must be replaced by

- 1.0 for typical values
- 1.6 for maximum values

$I_{LK1}$ = 580 000 + $e^{-\alpha}$, with $\alpha$ = 5 000 / (273 + B$\times T_J$)

Parameter B must be replaced by

- 1.1 for typical values
- 1.4 for maximum values

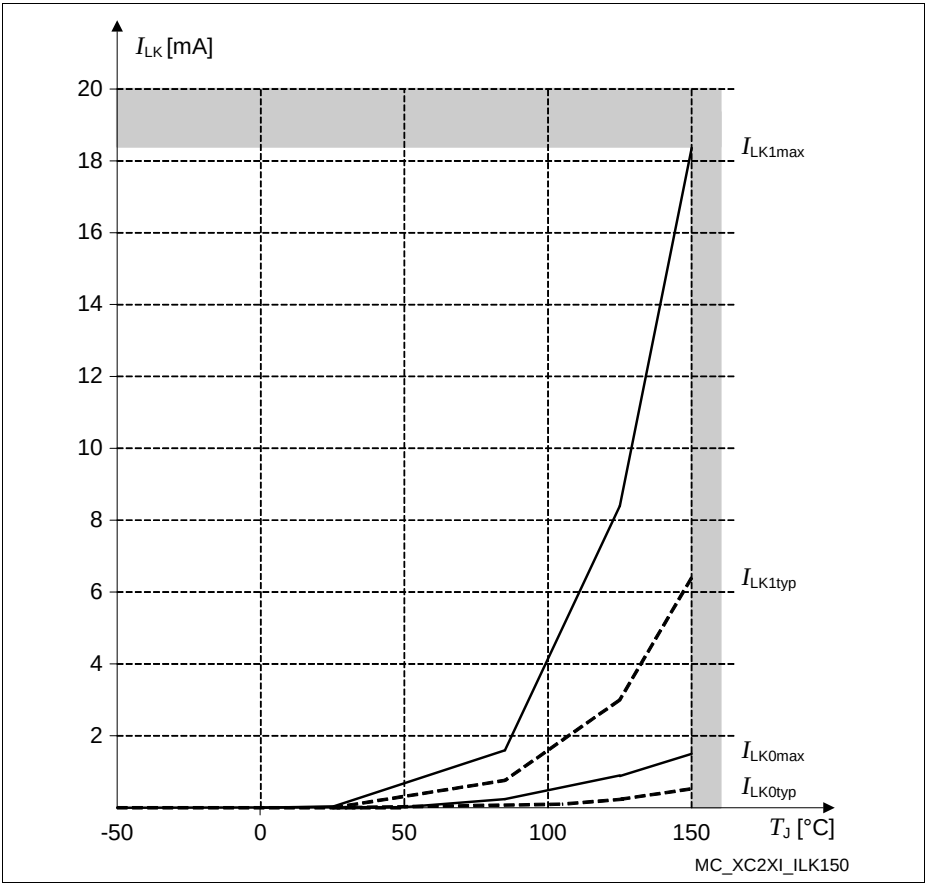


**Figure 12 Leakage Supply Current as a Function of Temperature**

## 4.3 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance.

*Note: Operating Conditions apply.*

**Table 20 ADC Parameters for All Voltage Ranges**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Switched capacitance at an analog input | $C_{AINSW}$ CC | – | 9 | 20 | pF | not subject to production test [1] |
| Total capacitance at an analog input | $C_{AINT}$ CC | – | 20 | 30 | pF | not subject to production test [1] |
| Switched capacitance at the reference input | $C_{AREFSW}$ CC | – | 15 | 30 | pF | not subject to production test [1] |
| Total capacitance at the reference input | $C_{AREFT}$ CC | – | 20 | 40 | pF | not subject to production test [1] |
| Broken wire detection delay against VAGND[2] | $t_{BWG}$ CC | – | – | 50 | [3] | |
| Broken wire detection delay against VAREF[2] | $t_{BWR}$ CC | – | – | 50 | [4] | |
| Conversion time for 8-bit result[2] | $t_{c8}$ CC | (10 + STC) x $t_{ADCI}$ + 2 x $t_{SYS}$ | | | | |
| Conversion time for 10-bit result[2] | $t_{c10}$ CC | (12 + STC) x $t_{ADCI}$ + 2 x $t_{SYS}$ | | | | |
| Conversion time for 12-bit result[2] | $t_{c12}$ CC | (16 + STC) x $t_{ADCI}$ + 2 x $t_{SYS}$ | | | | |
| Analog reference ground | $V_{AGND}$ SR | $V_{SS}$ - 0.05 | – | 1.5 | V | |
| Analog input voltage range | $V_{AIN}$ SR | $V_{AGND}$ | – | $V_{AREF}$ | V | [5] |
| Analog reference voltage | $V_{AREF}$ SR | $V_{AGND}$ + 1.0 | – | $V_{DDPA}$ + 0.05 | V | |

1) These parameter values cover the complete operating range. Under relaxed operating conditions (room temperature, nominal supply voltage) the typical values can be used for calculation.

2) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result. Values for the basic clock $t_{ADCI}$ depend on programming.

3) The broken wire detection delay against $V_{AGND}$ is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 500 µs. Result below 10% ($66_H$).

4) The broken wire detection delay against $V_{AREF}$ is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 10 µs. This function is influenced by leakage current, in particular at high temperature. Result above 80% ($332_H$).

5) $V_{AIN}$ may exceed $V_{AGND}$ or $V_{AREF}$ up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

**Table 21 ADC Parameters for Upper Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input resistance of the selected analog channel | $R_{AIN}$ CC | – | 0.9 | 1.5 | kΩ | not subject to production test 1) |
| Input resistance of the reference input | $R_{AREF}$ CC | – | 0.5 | 1 | kΩ | not subject to production test 1) |
| Differential Non-Linearity Error 2)3)4)5) | $\lvert EA_{DNL}\rvert$ CC | – | 1.5 | 3.0 | LSB | not subject to production test |
| Gain Error 2)3)4)5) | $\lvert EA_{GAIN}\rvert$ CC | – | 0.5 | 3.5 | LSB | not subject to production test |
| Integral Non-Linearity 2)3)4)5) | $\lvert EA_{INL}\rvert$ CC | – | 1.5 | 3.0 | LSB | not subject to production test |
| Offset Error 2)3)4)5) | $\lvert EA_{OFF}\rvert$ CC | – | 1.0 | 4.0 | LSB | not subject to production test |
| Total Unadjusted Error 3)4) | \|TUE\| CC | – | 2.5 | 4 | LSB | 6) |
| Analog clock frequency | $f_{ADCI}$ SR | 2 | – | 20 | MHz | Std. reference input ($V_{AREF}$) |
| | | 2 | – | 17.5 | MHz | Alt. reference input (CH0) |
| Wakeup time from analog powerdown, fast mode | $t_{WAF}$ CC | – | – | 7 | µs | |
| Wakeup time from analog powerdown, slow mode | $t_{WAS}$ CC | – | – | 11.5 | µs | |

1) These parameter values cover the complete operating range. Under relaxed operating conditions (room temperature, nominal supply voltage) the typical values can be used for calculation.
2) The sum of DNL/INL/GAIN/OFF errors does not exceed the related TUE total unadjusted error.
3) If a reduced analog reference voltage between 1 V and $V_{DDPA}$ / 2 is used, there is an additional decrease of the ADC speed and accuracy.
4) If the analog reference voltage is below $V_{DDPA}$ but still in the range of $V_{DDPA}$ / 2 and $V_{DDPA}$, the ADC errors increase. Reducing the reference voltage by a factor k (k < 1) increases TUE, DNL, INL, Gain and Offset errors by a factor 1/k.
5) If the analog reference voltage is above $V_{DDPA}$, the ADC errors increase.
6) TUE is based on 12-bit conversions.
TUE is tested at $V_{AREF}$ = $V_{DDPA}$ = 5.0 V, $V_{AGND}$ = 0 V. It is verified by design for all other voltages within the defined voltage range. The specified TUE is valid only if the absolute sum of input overload currents on analog port pins (see $I_{OV}$ specification) does not exceed 10 mA, and if $V_{AREF}$ and $V_{AGND}$ remain stable during the measurement time.

**Table 22 ADC Parameters for Lower Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input resistance of the selected analog channel | $R_{AIN}$ CC | – | 1.4 | 2.5 | kΩ | not subject to production test 1) |
| Input resistance of the reference input | $R_{AREF}$ CC | – | 0.8 | 1.7 | kΩ | not subject to production test 1) |
| Differential Non-Linearity Error 2)3)4)5) | $\|EA_{DNL}\|$ CC | – | 1.5 | 3.0 | LSB | not subject to production test |
| Gain Error 2)3)4)5) | $\|EA_{GAIN}\|$ CC | – | 0.5 | 3.5 | LSB | not subject to production test |
| Integral Non-Linearity 2)3)4)5) | $\|EA_{INL}\|$ CC | – | 1.5 | 3.0 | LSB | not subject to production test |
| Offset Error 2)3)4)5) | $\|EA_{OFF}\|$ CC | – | 1.0 | 4.0 | LSB | not subject to production test |
| Total Unadjusted Error 3)4) | \|TUE\| CC | – | 2.5 | 4 | LSB | 6) |
| Analog clock frequency | $f_{ADCI}$ SR | 2 | – | 16.7 | MHz | Std. reference input ($V_{AREF}$) |
| | | 2 | – | 12.1 | MHz | Alt. reference input (CH0) |

**Table 22 ADC Parameters for Lower Voltage Range** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Wakeup time from analog powerdown, fast mode | $t_{WAF}$ CC | – | – | 8.5 | µs | |
| Wakeup time from analog powerdown, slow mode | $t_{WAS}$ CC | – | – | 15 | µs | |

1) These parameter values cover the complete operating range. Under relaxed operating conditions (room temperature, nominal supply voltage) the typical values can be used for calculation.
2) The sum of DNL/INL/GAIN/OFF errors does not exceed the related TUE total unadjusted error.
3) If a reduced analog reference voltage between 1 V and $V_{DDPA}$ / 2 is used, there is an additional decrease of the ADC speed and accuracy.
4) If the analog reference voltage is below $V_{DDPA}$ but still in the range of $V_{DDPA}$ / 2 and $V_{DDPA}$, the ADC errors increase. Reducing the reference voltage by a factor k (k < 1) increases TUE, DNL, INL, Gain and Offset errors by a factor 1/k.
5) If the analog reference voltage is above $V_{DDPA}$, the ADC errors increase.
6) TUE is based on 12-bit conversions.
TUE is tested at $V_{AREF}$ = $V_{DDPA}$ = 3.3 V, $V_{AGND}$ = 0 V. It is verified by design for all other voltages within the defined voltage range. The specified TUE is valid only if the absolute sum of input overload currents on analog port pins (see $I_{OV}$ specification) does not exceed 10 mA, and if $V_{AREF}$ and $V_{AGND}$ remain stable during the measurement time.

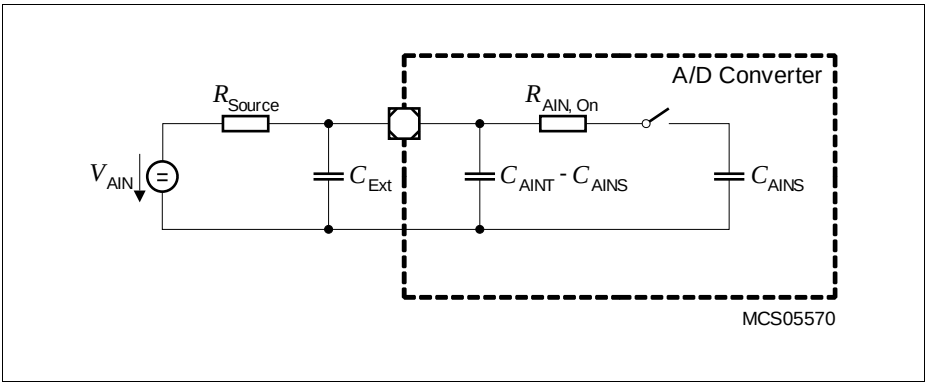


**Figure 13 Equivalent Circuitry for Analog Inputs**

Sample time and conversion time of the XC2268I's A/D converters are programmable. The timing above can be calculated using **Table 23**.
The limit values for $f_{ADCI}$ must not be exceeded when selecting the prescaler value.

**Table 23 A/D Converter Computation Table**

| GLOBCTR.5-0 (DIVA) | A/D Converter Analog Clock $f_{ADCI}$ | | INPCRx.7-0 (STC) | Sample Time[1] $t_S$ |
|---|---|---|---|---|
| $000000_B$ | $f_{SYS}$ | | $00_H$ | $t_{ADCI} \times 2$ |
| $000001_B$ | $f_{SYS}$ / 2 | | $01_H$ | $t_{ADCI} \times 3$ |
| $000010_B$ | $f_{SYS}$ / 3 | | $02_H$ | $t_{ADCI} \times 4$ |
| : | $f_{SYS}$ / (DIVA+1) | | : | $t_{ADCI} \times$ (STC+2) |
| $111110_B$ | $f_{SYS}$ / 63 | | $FE_H$ | $t_{ADCI} \times 256$ |
| $111111_B$ | $f_{SYS}$ / 64 | | $FF_H$ | $t_{ADCI} \times 257$ |

1) The selected sample time is doubled if broken wire detection is active (due to the presampling phase).

**Converter Timing Example A:**

Assumptions: $f_{SYS}$ = 128 MHz (i.e. $t_{SYS}$ = 7.8 ns), DIVA = $06_H$, STC = $00_H$
Analog clock $f_{ADCI}$ = $f_{SYS}$ / 7 = 18.3 MHz, i.e. $t_{ADCI}$ = 54.7 ns
Sample time $t_S$ = $t_{ADCI} \times 2$ = 109.4 ns

**Conversion 12-bit:**

$t_{C10}$ = $16 \times t_{ADCI} + 2 \times t_{SYS}$ = $16 \times 54.7$ ns + $2 \times 7.8$ ns = 0.891 µs

**Conversion 10-bit:**

$t_{C8}$ = $12 \times t_{ADCI} + 2 \times t_{SYS}$ = $12 \times 54.7$ ns + $2 \times 7.8$ ns = 0.672 µs

**Converter Timing Example B:**

Assumptions: $f_{SYS}$ = 40 MHz (i.e. $t_{SYS}$ = 25 ns), DIVA = $02_H$, STC = $03_H$
Analog clock $f_{ADCI}$ = $f_{SYS}$ / 3 = 13.3 MHz, i.e. $t_{ADCI}$ = 75 ns
Sample time $t_S$ = $t_{ADCI} \times 5$ = 375 ns

**Conversion 12-bit:**

$t_{C10}$ = $19 \times t_{ADCI} + 2 \times t_{SYS}$ = $19 \times 75$ ns + $2 \times 25$ ns = 1.475 µs

**Conversion 10-bit:**

$t_{C8}$ = $15 \times t_{ADCI} + 2 \times t_{SYS}$ = $15 \times 75$ ns + $2 \times 25$ ns = 1.175 µs

## 4.4 System Parameters

The following parameters specify several aspects which are important when integrating the XC2268I into an application system.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

*Note: Operating Conditions apply.*

**Table 24 Various System Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Short-term deviation of internal clock source frequency[1] | $\Delta f_{INT}$ CC | -1 | – | 1 | % | $\Delta T_J \leq 10$ °C |
| Internal clock source frequency | $f_{INT}$ CC | 4.8 | 5.0 | 5.2 | MHz | |
| Wakeup clock source frequency[2] | $f_{WU}$ CC | 400 | – | 700 | kHz | FREQSEL= 00 |
| | | 210 | – | 390 | kHz | FREQSEL= 01 |
| | | 140 | – | 260 | kHz | FREQSEL= 10 |
| | | 110 | – | 200 | kHz | FREQSEL= 11 |
| Startup time from power-on with code execution from Flash | $t_{SPO}$ CC | 1.9 | 2.5 | 3.7 | ms | $f_{WU}$ = 500 kHz |
| Startup time from standby mode with code execution from Flash | $t_{SSB}$ CC | 3.1 | 4.0 | 5.2 | ms | $f_{WU}$ = 140 kHz |
| | | 1.9 | 2.4 | 3.6 | ms | $f_{WU}$ = 500 kHz |
| Startup time from stopover mode with code execution from PSRAM | $t_{SSO}$ CC | 11 / $f_{WU}$[3] | – | 12 / $f_{WU}$[3] | µs | |
| Core voltage (PVC) supervision level | $V_{PVC}$ CC | $V_{LV}$ - 0.03 | $V_{LV}$ | $V_{LV}$ + 0.07[4] | V | [5] |
| Supply watchdog (SWD) supervision level | $V_{SWD}$ CC | $V_{LV}$ - 0.10[6] | $V_{LV}$ | $V_{LV}$ + 0.15 | V | Lower voltage range[5] |
| | | $V_{LV}$ - 0.15 | $V_{LV}$ | $V_{LV}$ + 0.15 | V | Upper voltage range[5] |

1) The short-term frequency deviation refers to a timeframe of a few hours and is measured relative to the current frequency at the beginning of the respective timeframe. This parameter is useful to determine a time span for re-triggering a LIN synchronization.
2) This parameter is tested for the fastest and the slowest selection. The medium selections are not subject to production test - verified by design/characterization
3) $f_{WU}$ in MHz
4) This value includes a hysteresis of approximately 50 mV for rising voltage.
5) $V_{LV}$ = selected PVC/SWD voltage level
6) The limit $V_{LV}$ - 0.10 V is valid for the OK1 level. The limit for the OK2 level is $V_{LV}$ - 0.15 V.

### Conditions for $t_{SPO}$ Timing Measurement

The time required for the transition from **Power-On** to **Base** mode is called $t_{SPO}$. It is measured under the following conditions:

Precondition: The pad supply is valid, i.e. $V_{DDPB}$ is above 3.0 V and remains above 3.0 V even though the XC2268I is starting up. See also $V_{DDPB}$ requirements in **Table 13**.

Start condition: Power-on reset is removed ($\overline{\text{PORST}}$ = 1).

End condition: External pin toggle caused by first user instruction executed from FLASH after startup.

### Conditions for $t_{SSB}$ Timing Measurement

The time required for the transition from **Standby** to **Base** mode is called $t_{SSB}$. It is measured under the following conditions:

Precondition: The **Standby** mode has been entered using the procedure defined in the Programmer's Guide.

Start condition: Pin toggle on $\overline{\text{ESR}}$ pin triggering the startup sequence.

End condition: External pin toggle caused by first user instruction executed from FLASH after startup.

### Conditions for $t_{SSO}$ Timing Measurement

The time required for the transition from **Stopover** to **Stopover Waked-Up** mode is called $t_{SSO}$. It is measured under the following conditions:

Precondition: The **Stopover** mode has been entered using the procedure defined in the Programmer's Guide.

Start condition: Pin toggle on $\overline{\text{ESR}}$ pin triggering the startup sequence.

End condition: External pin toggle caused by first user instruction executed from PSRAM after startup.

### Coding of bit fields LEVxV in SWD Configuration Registers

After power-on the supply watch dog is preconfigured to operate in the lower voltage range.

**Table 25 Coding of bit fields LEVxV in Register SWDCON0**

| Code | Voltage Level | Notes[1)] |
|---|---|---|
| $0000_B$ | - | out of valid operation range |
| $0001_B$ | 3.0 V | LEV1V: reset request |
| $0010_B$ - $0101_B$ | 3.1 V- 3.4 V | step width is 0.1 V |
| $0110_B$ | 3.6 V | |
| $0111_B$ | 4.0 V | |
| $1000_B$ | 4.2 V | |
| $1001_B$ | 4.5 V | LEV2V: no request |
| $1010_B$ - $1110_B$ | 4.6 V - 5.0 V | step width is 0.1 V |
| $1111_B$ | 5.5 V | |

1) The indicated default levels for LEV1V and LEV2V are selected automatically after a power-on reset.

### Coding of bit fields LEVxV in PVC Configuration Registers

The core voltages are controlled internally to the nominal value of 1.5 V; a variation of ±10 % is allowed. These operation conditions limit the possible PVC monitoring values to the predefined reset values shown in **Table 26**.

**Table 26 Coding of bit fields LEVxV in Registers PVCyCONz**

| Code | Voltage Level | Notes[1)] |
|---|---|---|
| $000_B$-$011_B$ | - | out of valid operation range |
| $100_B$ | 1.35 V | LEV1V: reset request |
| $101_B$ | 1.45 V | LEV2V: interrupt request[2)] |
| $110_B$ - $111_B$ | - | out of valid operation range |

1) The indicated default levels for LEV1V and LEV2V are selected automatically after a power-on reset.

2) Due to variations of the tolerance of both the Embedded Voltage Regulators (EVR) and the PVC levels, this interrupt can be triggered inadvertently, even though the core voltage is within the normal range. It is, therefore, recommended not to use this warning level.

## 4.5 Flash Memory Parameters

The XC2268I is delivered with all Flash sectors erased and with no protection installed.

The data retention time of the XC2268I's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

*Note: Operating Conditions apply.*

**Table 27 Flash Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Parallel Flash module program/erase limit depending on Flash read activity | $N_{PP}$ SR | – | – | 5[1)] | | $N_{FL_RD} \leq 1$ |
| | | – | – | 1[2)] | | $N_{FL_RD} > 1$ |
| Flash erase endurance for security pages | $N_{SEC}$ SR | 10 | – | – | cycles | $t_{RET} \geq$ 20 years |
| Flash wait states[3)] | $N_{WSFLASH}$ SR | 1 | – | – | | $f_{SYS} \leq$ 8 MHz |
| | | 2 | – | – | | $f_{SYS} \leq$ 13 MHz |
| | | 3 | – | – | | $f_{SYS} \leq$ 17 MHz |
| | | 4 | – | – | | $f_{SYS} >$ 17 MHz |
| Flash wait state extension[4)] | $N_{WSFLE}$ SR | 0 | – | – | | $f_{SYS} \leq$ 80 MHz |
| | | 1 | – | – | | $f_{SYS} >$ 80 MHz; $f_{SYS} \leq$ 128 MHz |
| Erase time per sector/page | $t_{ER}$ CC | – | 7[5)] | 8.0 | ms | |
| Programming time per page | $t_{PR}$ CC | – | 3[5)] | 3.5 | ms | |
| Data retention time | $t_{RET}$ CC | 20 | – | – | years | $N_{Er} \leq$ 1 000 cycles |
| Drain disturb limit | $N_{DD}$ SR | 32 | – | – | cycles | |

**Table 27 Flash Parameters** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Number of erase cycles | $N_{ER}$ SR | – | – | 15 000 | cycles | $t_{RET}$ ≥ 5 years; Valid when using Flash module 4 for data storage. |
| | | – | – | 1 000 | cycles | $t_{RET}$ ≥ 20 years |

1) All Flash module(s) can be erased/programmed while code is executed and/or data is read from only one Flash module or from PSRAM. The Flash module that delivers code/data can, of course, not be erased/programmed.
2) Flash module 4 can be erased/programmed while code is executed and/or data is read from any other Flash module.
3) Value of IMB_IMBCTRL.WSFLASH.
4) Value of IMB_IMBCTRL.WSFLE.
Set bit STMEM0.SFAR = 1 before selecting a system frequency above 80 MHz to avoid an inadvertent waitstate violation after an application reset (caused by the default setting).
5) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticably only at extremely low system clock frequencies.

Access to the XC2268I Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

Flash access via the cacheable Flash address space requires one additional waitstate in case of a cache miss, while the cache access (in case of a cache hit) requires no waitstate at all.

## 4.6 AC Parameters

These parameters describe the dynamic behavior of the XC2268I.

### 4.6.1 Testing Waveforms

These values are used for characterization and production testing (except pin XTAL1).

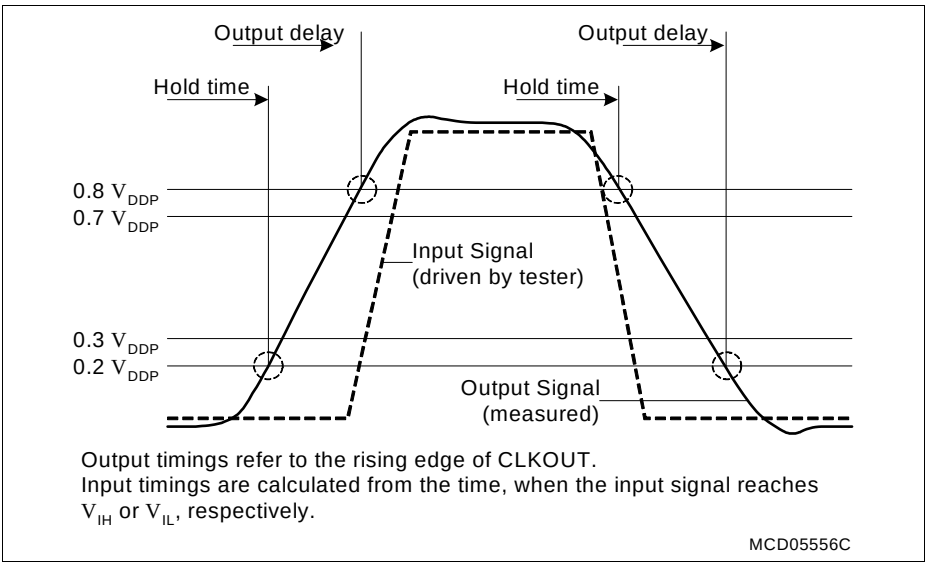


**Figure 14 Input Output Waveforms**

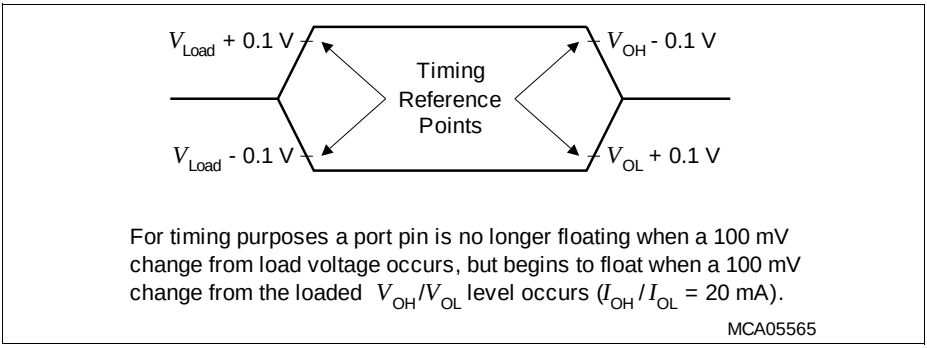


**Figure 15 Floating Waveforms**

### 4.6.2 Definition of Internal Timing

The internal operation of the XC2268I is controlled by the internal system clock $f_{SYS}$.

Because the system clock signal $f_{SYS}$ can be generated from a number of internal and external sources using different mechanisms, the duration of the system clock periods (TCSs) and their variation (as well as the derived external timing) depend on the mechanism used to generate $f_{SYS}$. This must be considered when calculating the timing for the XC2268I.

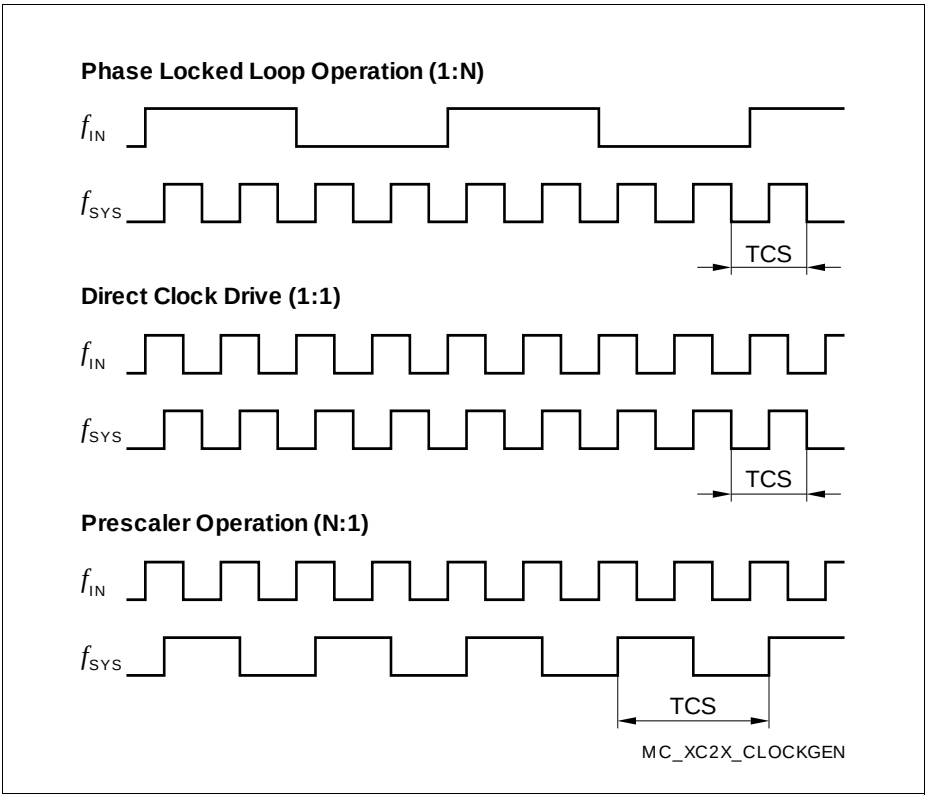


**Figure 16 Generation Mechanisms for the System Clock**

*Note: The example of PLL operation shown in **Figure 16** uses a PLL factor of 1:4; the example of prescaler operation uses a divider factor of 2:1.*

The specification of the external timing (AC Characteristics) depends on the period of the system clock (TCS).

**Direct Drive**

When direct drive operation is selected (SYSCON0.CLKSEL = $11_B$), the system clock is derived directly from the input clock signal CLKIN1:

$f_{SYS} = f_{IN}$.

The frequency of $f_{SYS}$ is the same as the frequency of $f_{IN}$. In this case the high and low times of $f_{SYS}$ are determined by the duty cycle of the input clock $f_{IN}$.

Selecting Bypass Operation from the XTAL1[1)] input and using a divider factor of 1 results in a similar configuration.

**Prescaler Operation**

When prescaler operation is selected (SYSCON0.CLKSEL = $10_B$, PLLCON0.VCOBY = $1_B$), the system clock is derived either from the crystal oscillator (input clock signal XTAL1) or from the internal clock source through the output prescaler K1 (= K1DIV+1):

$f_{SYS} = f_{OSC}$ / K1.

If a divider factor of 1 is selected, the frequency of $f_{SYS}$ equals the frequency of $f_{OSC}$. In this case the high and low times of $f_{SYS}$ are determined by the duty cycle of the input clock $f_{OSC}$ (external or internal).

The lowest system clock frequency results from selecting the maximum value for the divider factor K1:

$f_{SYS} = f_{OSC}$ / 1024.

### 4.6.2.1 Phase Locked Loop (PLL)

When PLL operation is selected (SYSCON0.CLKSEL = $10_B$, PLLCON0.VCOBY = $0_B$), the on-chip phase locked loop is enabled and provides the system clock. The PLL multiplies the input frequency by the factor **F** ($f_{SYS} = f_{IN} \times$ **F**).
**F** is calculated from the input divider P (= PDIV+1), the multiplication factor N (= NDIV+1), and the output divider K2 (= K2DIV+1):
(**F** = N / (P $\times$ K2)).

The input clock can be derived either from an external source at XTAL1 or from the on-chip clock source.

The PLL circuit synchronizes the system clock to the input clock. This synchronization is performed smoothly so that the system clock frequency does not change abruptly.

Adjustment to the input clock continuously changes the frequency of $f_{SYS}$ so that it is locked to $f_{IN}$. The slight variation causes a jitter of $f_{SYS}$ which in turn affects the duration of individual TCSs.

1) Voltages on XTAL1 must comply to the core supply voltage $V_{DDIM}$.

The timing in the AC Characteristics refers to TCSs. Timing must be calculated using the minimum TCS possible under the given circumstances.
The actual minimum value for TCS depends on the jitter of the PLL. Because the PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or oscillator), the accumulated jitter is limited. This means that the relative deviation for periods of more than one TCS is lower than for a single TCS (see formulas and **Figure 17**).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler K2 to generate the system clock signal $f_{SYS}$. The number of VCO cycles is K2 × **T**, where **T** is the number of consecutive $f_{SYS}$ cycles (TCS).

The maximum accumulated jitter (long-term jitter) $D_{Tmax}$ is defined by:

**$D_{Tmax}$ [ns] =** $\pm(220 / (K2 \times f_{SYS}) + 4.3)$

This maximum value is applicable, if either the number of clock cycles T > ($f_{SYS}$ / 1.2) or the prescaler value K2 > 17.

In all other cases for a timeframe of **T** × TCS the accumulated jitter $D_T$ is determined by:

**$D_T$ [ns] =** $D_{Tmax} \times [(1 - 0.058 \times K2) \times (T - 1) / (0.83 \times f_{SYS} - 1) + 0.058 \times K2]$

$f_{SYS}$ in [MHz] in all formulas.

Example, for a period of 3 TCSs @ 33 MHz and K2 = 4:

$D_{max} = \pm(220 / (4 \times 33) + 4.3) = 5.97$ ns (Not applicable directly in this case!)

$D_3 = 5.97 \times [(1 - 0.058 \times 4) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 4]$
$= 5.97 \times [0.768 \times 2 / 26.39 + 0.232]$
$= 1.7$ ns

Example, for a period of 3 TCSs @ 33 MHz and K2 = 2:

$D_{max} = \pm(220 / (2 \times 33) + 4.3) = 7.63$ ns (Not applicable directly in this case!)

$D_3 = 7.63 \times [(1 - 0.058 \times 2) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 2]$
$= 7.63 \times [0.884 \times 2 / 26.39 + 0.116]$
$= 1.4$ ns

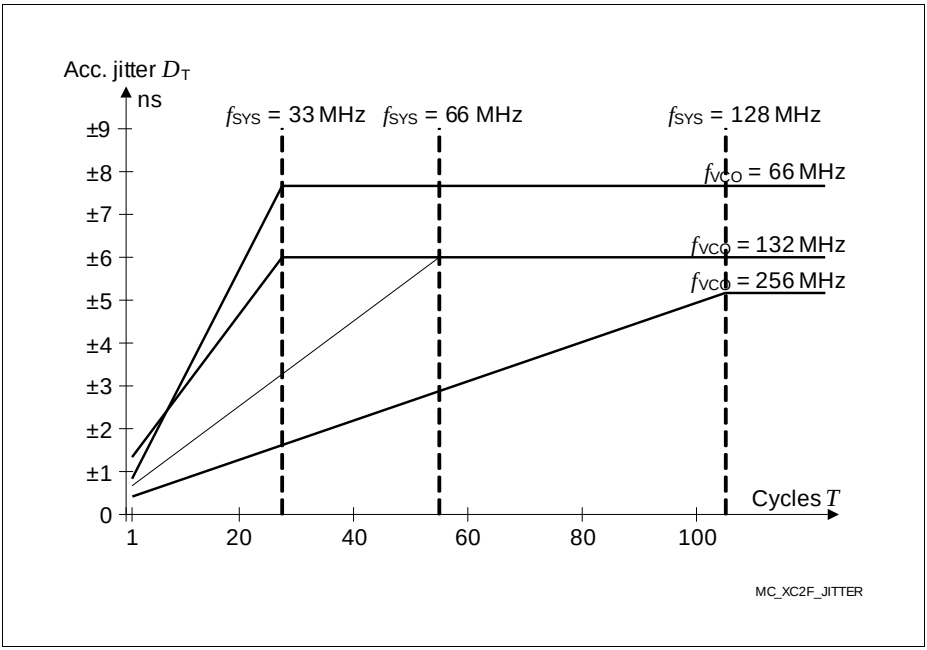


**Figure 17 Approximated Accumulated PLL Jitter**

*Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L$ = 20 pF.*
*The maximum peak-to-peak noise on the pad supply voltage (measured between $V_{DDPB}$ pin 100 and $V_{SS}$ pin 1) is limited to a peak-to-peak voltage of $V_{PP}$ = 50 mV. This can be achieved by appropriate blocking of the supply voltage as close as possible to the supply pins and using PCB supply and ground planes.*

### PLL Frequency Band Selection

Different frequency bands can be selected for the VCO so that the operation of the PLL can be adjusted to a wide range of input and output frequencies:

**Table 28 System PLL Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| VCO output frequency (VCO controlled) | $f_{VCO}$ CC | 50 | – | 110 | MHz | VCOSEL = $00_B$ |
| | | 100 | – | 200 | MHz | VCOSEL = $01_B$ |
| | | 200 | – | 280 | MHz | VCOSEL = $10_B$ |
| VCO output frequency (VCO free-running) | $f_{VCO}$ CC | 10 | – | 40 | MHz | VCOSEL = $00_B$ |
| | | 20 | – | 80 | MHz | VCOSEL = $01_B$ |
| | | 40 | – | 160 | MHz | VCOSEL = $10_B$ |

### 4.6.2.2 Wakeup Clock

When wakeup operation is selected (SYSCON0.CLKSEL = $00_B$), the system clock is derived from the low-frequency wakeup clock source:

$f_{SYS} = f_{WU}$.

In this mode, a basic functionality can be maintained without requiring an external clock source and while minimizing the power consumption.

### 4.6.2.3 Selecting and Changing the Operating Frequency

When selecting a clock source and the clock generation method, the required parameters must be carefully written to the respective bitfields, to avoid unintended intermediate states.

Many applications change the frequency of the system clock ($f_{SYS}$) during operation in order to optimize system performance and power consumption. Changing the operating frequency also changes the switching currents, which influences the power supply.

To ensure proper operation of the on-chip EVRs while they generate the core voltage, the operating frequency shall only be changed in certain steps. This prevents overshoots and undershoots of the supply voltage.

To avoid the indicated problems, recommended sequences are provided which ensure the intended operation of the clock system interacting with the power system.
Please refer to the Programmer’s Guide.

### 4.6.3 External Clock Input Parameters

These parameters specify the external clock generation for the XC2268I. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2
- By supplying an **external clock signal**
  - This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain)

If connected to CLKIN1, the input signal must reach the defined input levels $V_{IL}$ and $V_{IH}$. If connected to XTAL1, a minimum amplitude $V_{AX1}$ (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

*Note: The given clock timing parameters ($t_1$ … $t_4$) are only valid for an external clock input signal.*

*Note: Operating Conditions apply.*

**Table 29 External Clock Input Characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Oscillator frequency | $f_{OSC}$ SR | 4 | – | 40 | MHz | Input = clock signal |
| | | 4 | – | 20 | MHz | Input = crystal or ceramic resonator[1)] |
| XTAL1 input current absolute value | $\|I_{IL}\|$ CC | – | – | 20 | µA | |
| Input clock high time | $t_1$ SR | 6 | – | – | ns | |
| Input clock low time | $t_2$ SR | 6 | – | – | ns | |
| Input clock rise time | $t_3$ SR | – | – | 8 | ns | |
| Input clock fall time | $t_4$ SR | – | – | 8 | ns | |
| Input voltage amplitude on XTAL1[2)] | $V_{AX1}$ SR | 0.3 x $V_{DDIM}$ | – | – | V | 4 to 16 MHz |
| | | 0.4 x $V_{DDIM}$ | – | – | V | 16 to 25 MHz |
| | | 0.5 x $V_{DDIM}$ | – | – | V | 25 to 40 MHz |
| Input voltage range limits for signal on XTAL1 | $V_{IX1}$ SR | -1.7 + $V_{DDIM}$ | – | 1.7 | V | [3)] |

1) For frequencies above 16 MHz, it is mandatory to measure the oscillation allowance. Please refer to the general note below.
2) The amplitude voltage $V_{AX1}$ refers to the offset voltage $V_{OFF}$. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by $V_{IX1}$.
3) Overload conditions must not occur on pin XTAL1.

*Note: For crystal or ceramic resonator operation, it is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for oscillator operation.*
*The manufacturers of crystals and ceramic resonators offer an oscillator evaluation service. This evaluation checks the crystal/resonator specification limits to ensure a reliable oscillator operation.*

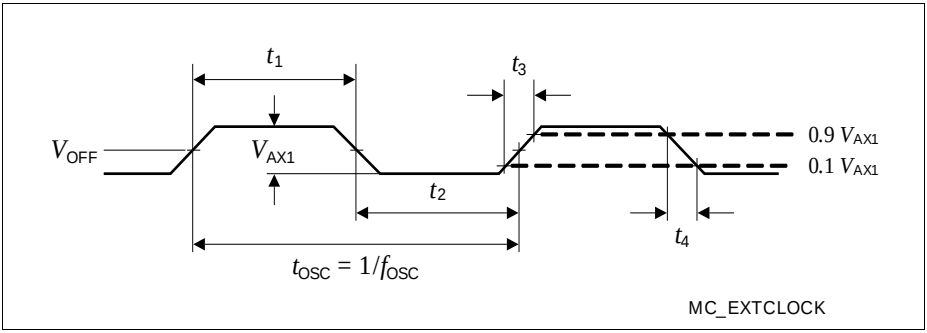


**Figure 18 External Clock Drive XTAL1**

### 4.6.4 Pad Properties

The output pad drivers of the XC2268I can operate in several user-selectable modes. Strong driver mode allows controlling external components requiring higher currents such as power bridges or LEDs. Reducing the driving power of an output pad reduces electromagnetic emissions (EME). In strong driver mode, selecting a slower edge reduces EME.

The dynamic behavior, i.e. the rise time and fall time, depends on the applied external capacitance that must be charged and discharged. Timing values are given for a capacitance of 20 pF, unless otherwise noted.

In general, the performance of a pad driver depends on the available supply voltage $V_{DDP}$. Therefore the following tables list the pad parameters for the upper voltage range and the lower voltage range, respectively.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

*Note: Operating Conditions apply.*

**Table 30** is valid under the following conditions:
$V_{DDP} \geq 4.5$ V; $V_{DDPtyp} = 5$ V; $V_{DDP} \leq 5.5$ V; $C_L \geq 20$ pF; $C_L \leq 100$ pF;

**Table 30 Standard Pad Parameters for Upper Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Maximum output driver current (absolute value)[1] | $I_{Omax}$ CC | – | – | 10 | mA | Strong driver |
| | | – | – | 4.0 | mA | Medium driver |
| | | – | – | 0.5 | mA | Weak driver |
| Nominal output driver current (absolute value) | $I_{Onom}$ CC | – | – | 2.5 | mA | Strong driver |
| | | – | – | 1.0 | mA | Medium driver |
| | | – | – | 0.1 | mA | Weak driver |
| Rise and Fall times (10% - 90%) | $t_{RF}$ CC | – | – | 4.2 + 0.14 x $C_L$ | ns | Strong driver; Sharp edge |
| | | – | – | 11.6 + 0.22 x $C_L$ | ns | Strong driver; Medium edge |
| | | – | – | 20.6 + 0.22 x $C_L$ | ns | Strong driver; Slow edge |
| | | – | – | 23 + 0.6 x $C_L$ | ns | Medium driver |
| | | – | – | 212 + 1.9 x $C_L$ | ns | Weak driver |

1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction ($\Sigma I_{OL}$ and $\Sigma I_{OH}$) must remain below 50 mA.

**Table 31** is valid under the following conditions:
$V_{DDP} \geq 3.0$ V; $V_{DDPtyp} = 3.3$ V; $V_{DDP} \leq 4.5$ V; $C_L \geq 20$ pF; $C_L \leq 100$ pF;

**Table 31 Standard Pad Parameters for Lower Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Maximum output driver current (absolute value)[1] | $I_{Omax}$ CC | – | – | 10 | mA | Strong driver |
| | | – | – | 2.5 | mA | Medium driver |
| | | – | – | 0.5 | mA | Weak driver |
| Nominal output driver current (absolute value) | $I_{Onom}$ CC | – | – | 2.5 | mA | Strong driver |
| | | – | – | 1.0 | mA | Medium driver |
| | | – | – | 0.1 | mA | Weak driver |
| Rise and Fall times (10% - 90%) | $t_{RF}$ CC | – | – | 6.2 + 0.24 x $C_L$ | ns | Strong driver; Sharp edge |
| | | – | – | 24 + 0.3 x $C_L$ | ns | Strong driver; Medium edge |
| | | – | – | 34 + 0.3 x $C_L$ | ns | Strong driver; Slow edge |
| | | – | – | 37 + 0.65 x $C_L$ | ns | Medium driver |
| | | – | – | 500 + 2.5 x $C_L$ | ns | Weak driver |

1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction ($\Sigma I_{OL}$ and $\Sigma I_{OH}$) must remain below 50 mA.

### 4.6.5 External Bus Timing

The following parameters specify the behavior of the XC2268I bus interface.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

*Note: Operating Conditions apply.*

**Bus Interface Performance Limits**

The output frequency at the bus interface pins is limited by the performance of the output drivers. The fast clock driver (used for CLKOUT) can drive 80-MHz signals, the standard drivers can drive 40-MHz signals
Therefore, the speed of the EBC must be limited, either by limiting the system frequency to $f_{SYS} \leq 80$ MHz or by adding waitstates so that signal transitions have a minimum distance of 12.5 ns.
For a description of the bus protocol and the programming of its variable timing parameters, please refer to the User's Manual.

**Table 32 EBC Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| CLKOUT Cycle Time[1)] | $t_5$ CC | – | 1 / $f_{SYS}$ | – | ns | |
| CLKOUT high time | $t_6$ CC | 2 | – | – | | |
| CLKOUT low time | $t_7$ CC | 2 | – | – | | |
| CLKOUT rise time | $t_8$ CC | – | – | 3 | ns | |
| CLKOUT fall time | $t_9$ CC | – | – | 3 | | |

1) The CLKOUT cycle time is influenced by PLL jitter. For longer periods the relative deviation decreases (see PLL deviation formula).

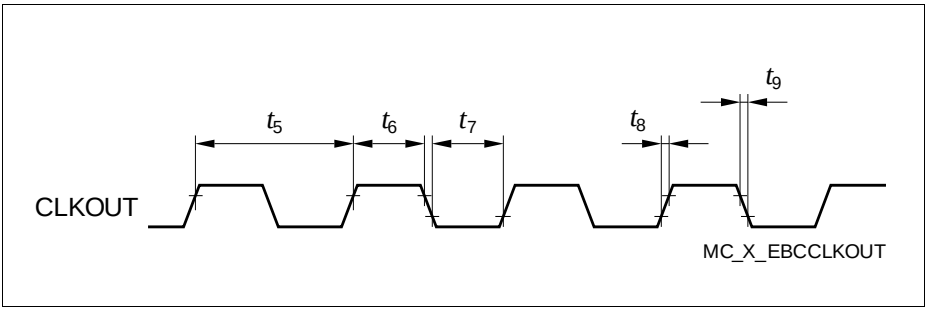


**Figure 19 CLKOUT Signal Timing**

*Note: The term CLKOUT refers to the reference clock output signal which is generated by selecting $f_{SYS}$ as the source signal for the clock output signal EXTCLK on pin P2.8 and by enabling the high-speed clock driver on this pin.*

### Variable Memory Cycles

External bus cycles of the XC2268I are executed in five consecutive cycle phases (AB, C, D, E, F). The duration of each cycle phase is programmable (via the TCONCSx registers) to adapt the external bus cycles to the respective external module (memory, peripheral, etc.).

The duration of the access phase can optionally be controlled by the external module using the READY handshake input.

This table provides a summary of the phases and the ranges for their length.

**Table 33 Programmable Bus Cycle Phases (see timing diagrams)**

| Bus Cycle Phase | Parameter | Valid Values | Unit |
|---|---|---|---|
| Address setup phase, the standard duration of this phase (1 … 2 TCS) can be extended by 0 … 3 TCS if the address window is changed | tpAB | 1 … 2 (5) | TCS |
| Command delay phase | tpC | 0 … 3 | TCS |
| Write Data setup/MUX Tristate phase | tpD | 0 … 1 | TCS |
| Access phase | tpE | 1 … 32 | TCS |
| Address/Write Data hold phase | tpF | 0 … 3 | TCS |

*Note: The bandwidth of a parameter (from minimum to maximum value) covers the whole operating range (temperature, voltage) as well as process variations. Within a given device, however, this bandwidth is smaller than the specified range. This is also due to interdependencies between certain parameters. Some of these interdependencies are described in additional notes (see standard timing).*

*Note: Operating Conditions apply; $C_L$ = 20 pF.*

**Table 34 EBC External Bus Timing for Upper Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output valid delay for $\overline{RD}$, $\overline{WR}$(L/H) | $t_{10}$ CC | – | 7 | 13 | ns | |
| Output valid delay for $\overline{BHE}$, ALE | $t_{11}$ CC | – | 7 | 14 | ns | |
| Address output valid delay for A23 ... A0 | $t_{12}$ CC | – | 8 | 14 | ns | |
| Address output valid delay for AD15 ... AD0 (MUX mode) | $t_{13}$ CC | – | 8 | 15 | ns | |
| Output valid delay for $\overline{CS}$ | $t_{14}$ CC | – | 7 | 13 | ns | |
| Data output valid delay for AD15 ... AD0 (write data, MUX mode) | $t_{15}$ CC | – | 8 | 15 | ns | |
| Data output valid delay for D15 ... D0 (write data, DEMUX mode) | $t_{16}$ CC | – | 8 | 15 | ns | |
| Output hold time for $\overline{RD}$, $\overline{WR}$(L/H) | $t_{20}$ CC | -2 | 6 | 8 | ns | |
| Output hold time for $\overline{BHE}$, ALE | $t_{21}$ CC | -2 | 6 | 10 | ns | |
| Address output hold time for AD15 ... AD0 | $t_{23}$ CC | -3 | 6 | 8 | ns | |
| Output hold time for $\overline{CS}$ | $t_{24}$ CC | -3 | 6 | 11 | ns | |
| Data output hold time for D15 ... D0 and AD15 ... AD0 | $t_{25}$ CC | -3 | 6 | 8 | ns | |
| Input setup time for READY, D15 ... D0, AD15 ... AD0 | $t_{30}$ SR | 25 | 15 | – | ns | |
| Input hold time READY, D15 ... D0, AD15 ... AD0[1)] | $t_{31}$ SR | 0 | -7 | – | ns | |

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.

**Table 35 EBC External Bus Timing for Lower Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output valid delay for $\overline{RD}$, $\overline{WR}$(L/$\overline{H}$) | $t_{10}$ CC | – | 11 | 20 | ns | |
| Output valid delay for $\overline{BHE}$, ALE | $t_{11}$ CC | – | 10 | 21 | ns | |
| Address output valid delay for A23 ... A0 | $t_{12}$ CC | – | 11 | 22 | ns | |
| Address output valid delay for AD15 ... AD0 (MUX mode) | $t_{13}$ CC | – | 10 | 22 | ns | |
| Output valid delay for $\overline{CS}$ | $t_{14}$ CC | – | 10 | 13 | ns | |
| Data output valid delay for AD15 ... AD0 (write data, MUX mode) | $t_{15}$ CC | – | 10 | 22 | ns | |
| Data output valid delay for D15 ... D0 (write data, DEMUX mode) | $t_{16}$ CC | – | 10 | 22 | ns | |
| Output hold time for $\overline{RD}$, $\overline{WR}$(L/$\overline{H}$) | $t_{20}$ CC | -2 | 8 | 10 | ns | |
| Output hold time for $\overline{BHE}$, ALE | $t_{21}$ CC | -2 | 8 | 10 | ns | |
| Address output hold time for AD15 ... AD0 | $t_{23}$ CC | -3 | 8 | 10 | ns | |
| Output hold time for $\overline{CS}$ | $t_{24}$ CC | -3 | 8 | 11 | ns | |
| Data output hold time for D15 ... D0 and AD15 ... AD0 | $t_{25}$ CC | -3 | 8 | 10 | ns | |
| Input setup time for READY, D15 ... D0, AD15 ... AD0 | $t_{30}$ SR | 29 | 17 | – | ns | |
| Input hold time READY, D15 ... D0, AD15 ... AD0[1)] | $t_{31}$ SR | 0 | -9 | – | ns | |

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of $\overline{RD}$. Address changes before the end of $\overline{RD}$ have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of $\overline{RD}$.

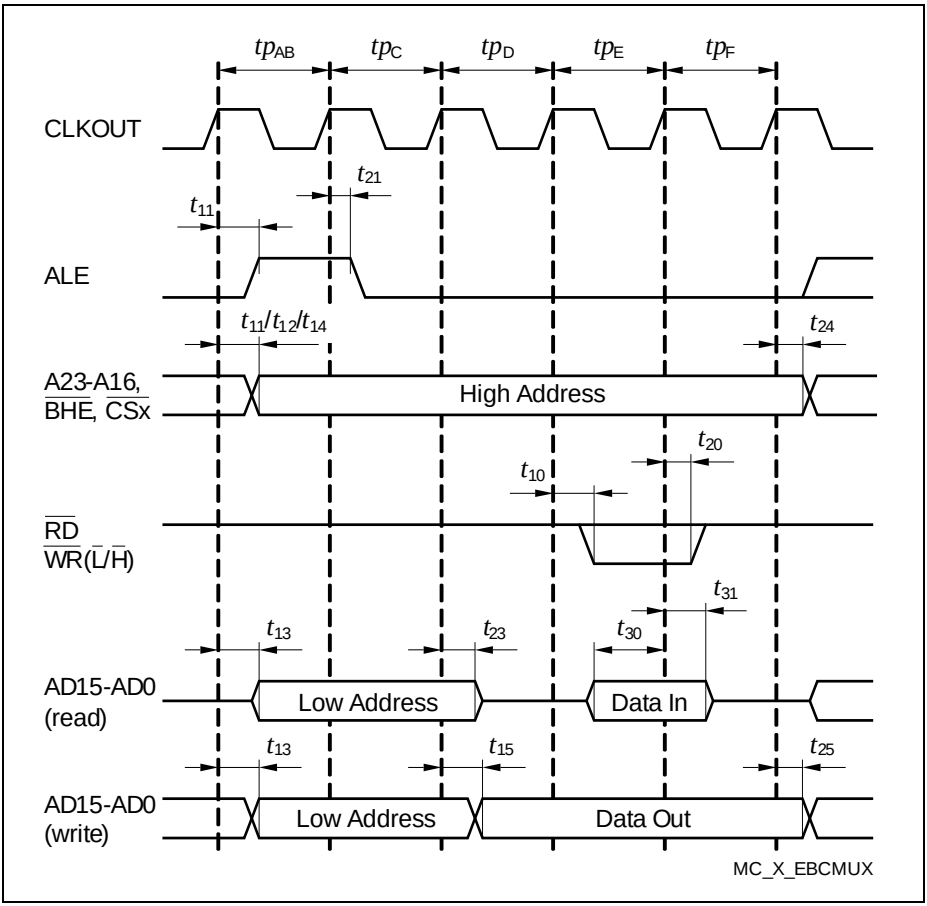


**Figure 20 Multiplexed Bus Cycle**

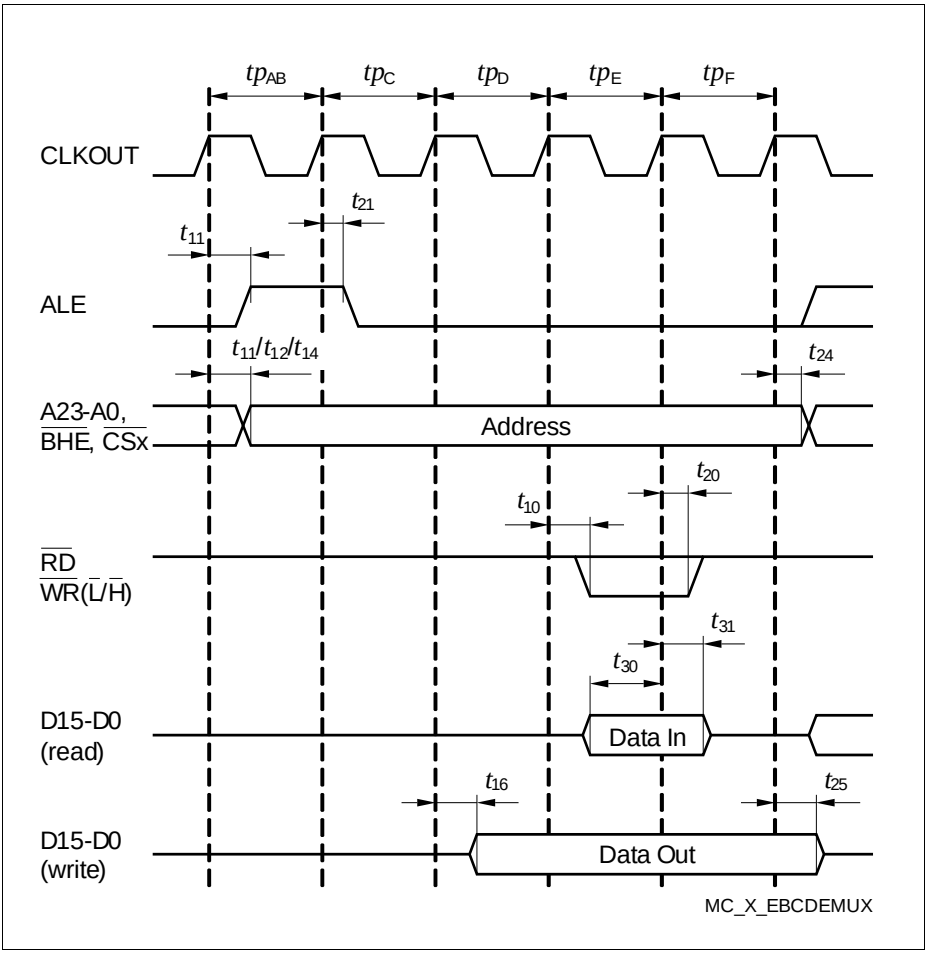


**Figure 21 Demultiplexed Bus Cycle**

### 4.6.5.1 Bus Cycle Control with the READY Input

The duration of an external bus cycle can be controlled by the external circuit using the READY input signal. The polarity of this input signal can be selected.

Synchronous READY permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

An asynchronous READY signal puts no timing constraints on the input signal but incurs a minimum of one waitstate due to the additional synchronization stage. The minimum duration of an asynchronous READY signal for safe synchronization is one CLKOUT period plus the input setup time.

An active READY signal can be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{RD}$ or $\overline{WR}$).

If the next bus cycle is controlled by READY, an active READY signal must be disabled before the first valid sample point in the next bus cycle. This sample point depends on the programmed phases of the next cycle.

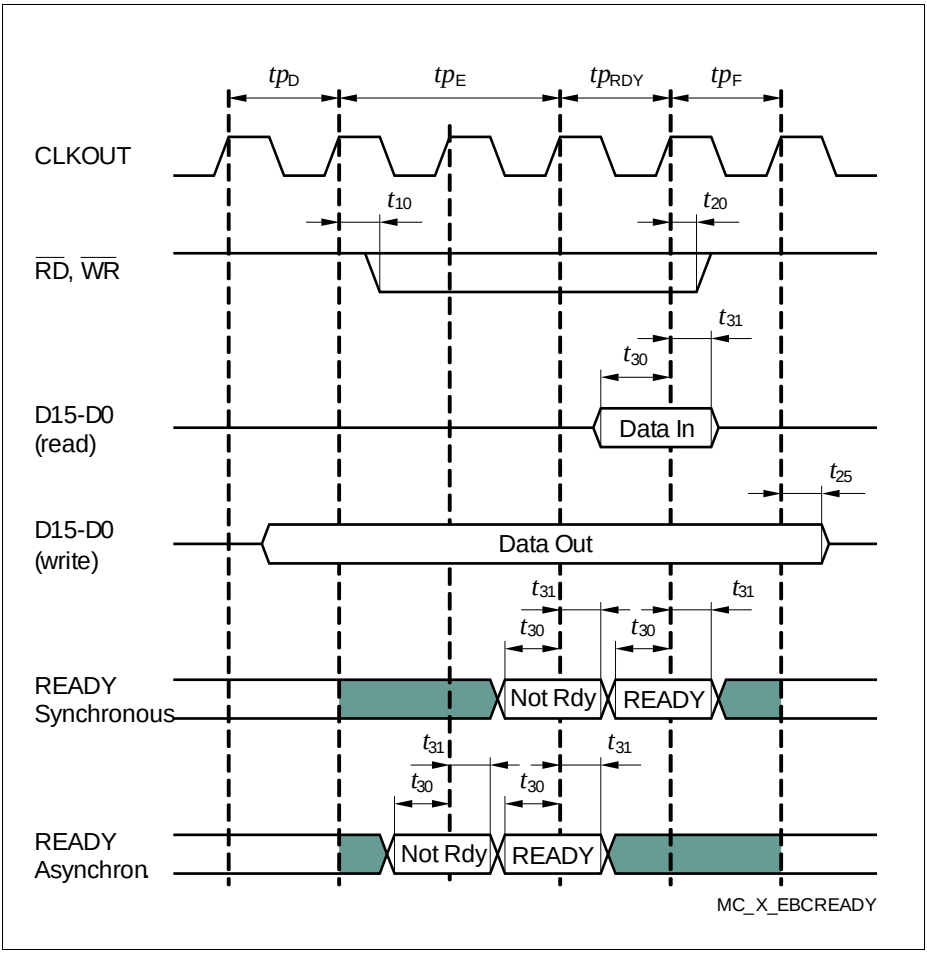


**Figure 22 READY Timing**

*Note: If the READY input is sampled inactive at the indicated sampling point (“Not Rdy”) a READY-controlled waitstate is inserted (tpRDY),*
*sampling the READY input active at the indicated sampling point (“Ready”) terminates the currently running bus cycle.*
*Note the different sampling points for synchronous and asynchronous READY.*
*This example uses one mandatory waitstate (see tpE) before the READY input value is used.*

### 4.6.6 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

*Note: Operating Conditions apply; $C_L$ = 20 pF.*

**Table 36 USIC SSC Master Mode Timing for Upper Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Slave select output SELO active to first SCLKOUT transmit edge | $t_1$ CC | $t_{SYS}$ - 8 [1] | – | – | ns | |
| Slave select output SELO inactive after last SCLKOUT receive edge | $t_2$ CC | $t_{SYS}$ - 6 [1] | – | – | ns | |
| Data output DOUT valid time | $t_3$ CC | -6 | – | 9 | ns | |
| Receive data input setup time to SCLKOUT receive edge | $t_4$ SR | 31 | – | – | ns | |
| Data input DX0 hold time from SCLKOUT receive edge | $t_5$ SR | -4 | – | – | ns | |

1) $t_{SYS} = 1 / f_{SYS}$

**Table 37 USIC SSC Master Mode Timing for Lower Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Slave select output SELO active to first SCLKOUT transmit edge | $t_1$ CC | $t_{SYS}$ - 10 [1] | – | – | ns | |
| Slave select output SELO inactive after last SCLKOUT receive edge | $t_2$ CC | $t_{SYS}$ - 9 [1] | – | – | ns | |
| Data output DOUT valid time | $t_3$ CC | -7 | – | 11 | ns | |

**Table 37 USIC SSC Master Mode Timing for Lower Voltage Range** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Receive data input setup time to SCLKOUT receive edge | $t_4$ SR | 40 | – | – | ns | |
| Data input DX0 hold time from SCLKOUT receive edge | $t_5$ SR | -5 | – | – | ns | |

1) $t_{SYS} = 1 / f_{SYS}$

**Table 38 USIC SSC Slave Mode Timing for Upper Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Select input DX2 setup to first clock input DX1 transmit edge[1)] | $t_{10}$ SR | 7 | – | – | ns | |
| Select input DX2 hold after last clock input DX1 receive edge[1)] | $t_{11}$ SR | 7 | – | – | ns | |
| Receive data input setup time to shift clock receive edge[1)] | $t_{12}$ SR | 7 | – | – | ns | |
| Data input DX0 hold time from clock input DX1 receive edge[1)] | $t_{13}$ SR | 5 | – | – | ns | |
| Data output DOUT valid time | $t_{14}$ CC | 7 | – | 33 | ns | |

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

**Table 39 USIC SSC Slave Mode Timing for Lower Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Select input DX2 setup to first clock input DX1 transmit edge[1)] | $t_{10}$ SR | 7 | – | – | ns | |
| Select input DX2 hold after last clock input DX1 receive edge[1)] | $t_{11}$ SR | 7 | – | – | ns | |
| Receive data input setup time to shift clock receive edge[1)] | $t_{12}$ SR | 7 | – | – | ns | |
| Data input DX0 hold time from clock input DX1 receive edge[1)] | $t_{13}$ SR | 5 | – | – | ns | |
| Data output DOUT valid time | $t_{14}$ CC | 8 | – | 41 | ns | |

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

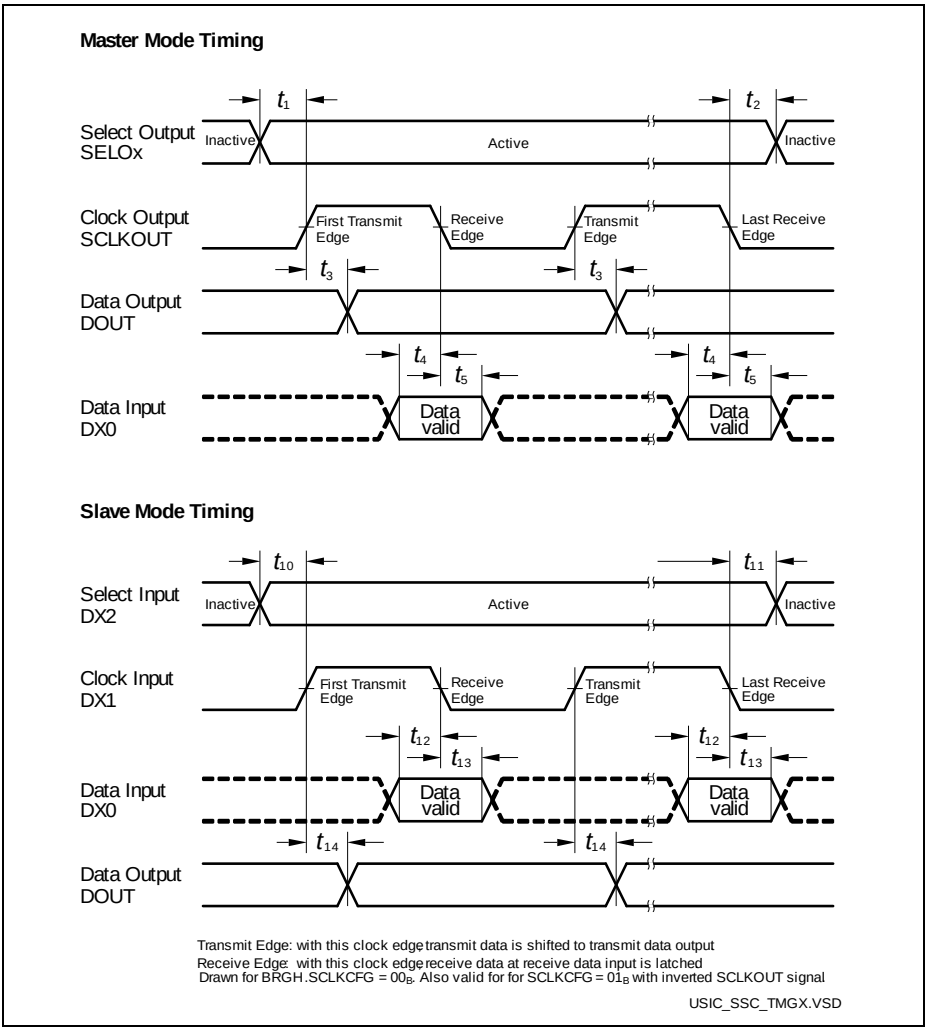


**Figure 23 USIC - SSC Master/Slave Mode Timing**

*Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.*

### 4.6.7 Debug Interface Timing

The debugger can communicate with the XC2268I either via the 2-pin DAP interface or via the standard JTAG interface.

#### Debug via DAP

The following parameters are applicable for communication through the DAP debug interface.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

*Note: Operating Conditions apply; $C_L$= 20 pF.*

**Table 40 DAP Interface Timing for Upper Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| DAP0 clock period | $t_{11}$ SR | 25[1)] | – | – | ns | |
| DAP0 high time | $t_{12}$ SR | 8 | – | – | ns | |
| DAP0 low time | $t_{13}$ SR | 8 | – | – | ns | |
| DAP0 clock rise time | $t_{14}$ SR | – | – | 4 | ns | |
| DAP0 clock fall time | $t_{15}$ SR | – | – | 4 | ns | |
| DAP1 setup to DAP0 rising edge | $t_{16}$ SR | 6 | – | – | ns | pad_type= standard |
| DAP1 hold after DAP0 rising edge | $t_{17}$ SR | 6 | – | – | ns | pad_type= standard |
| DAP1 valid per DAP0 clock period[2)] | $t_{19}$ CC | 17 | 20 | – | ns | pad_type= standard |

1) The debug interface cannot operate faster than the overall system, therefore $t_{11} \geq t_{SYS}$.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

**Table 41 DAP Interface Timing for Lower Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| DAP0 clock period | $t_{11}$ SR | 25[1] | – | – | ns | |
| DAP0 high time | $t_{12}$ SR | 8 | – | – | ns | |
| DAP0 low time | $t_{13}$ SR | 8 | – | – | ns | |
| DAP0 clock rise time | $t_{14}$ SR | – | – | 4 | ns | |
| DAP0 clock fall time | $t_{15}$ SR | – | – | 4 | ns | |
| DAP1 setup to DAP0 rising edge | $t_{16}$ SR | 6 | – | – | ns | pad_type= standard |
| DAP1 hold after DAP0 rising edge | $t_{17}$ SR | 6 | – | – | ns | pad_type= standard |
| DAP1 valid per DAP0 clock period[2] | $t_{19}$ CC | 12 | 17 | – | ns | pad_type= standard |

1) The debug interface cannot operate faster than the overall system, therefore $t_{11} \geq t_{SYS}$.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

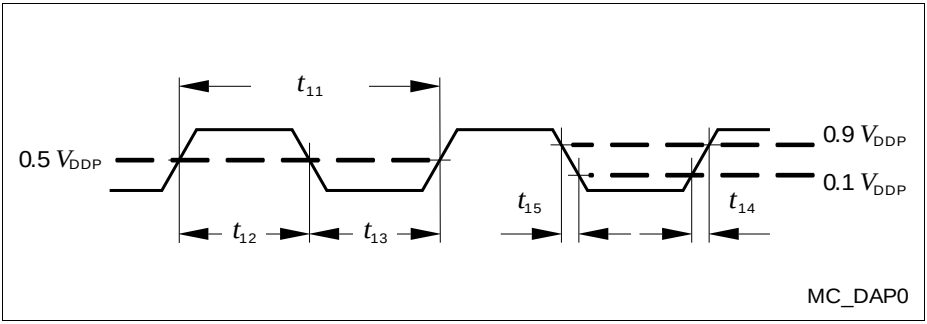


**Figure 24 Test Clock Timing (DAP0)**

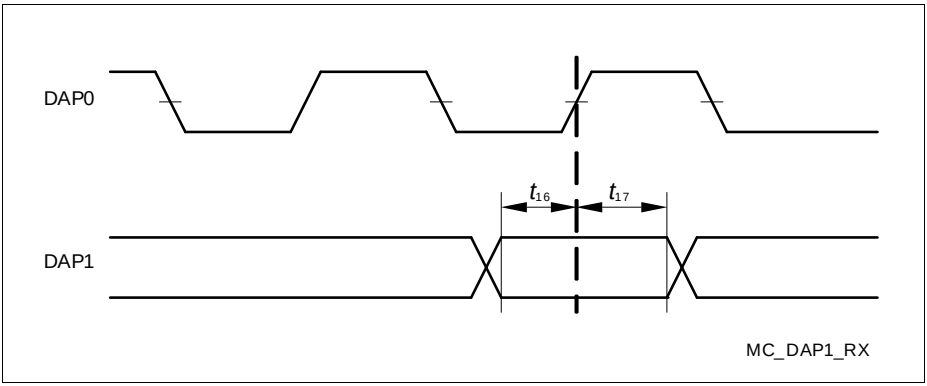


**Figure 25 DAP Timing Host to Device**

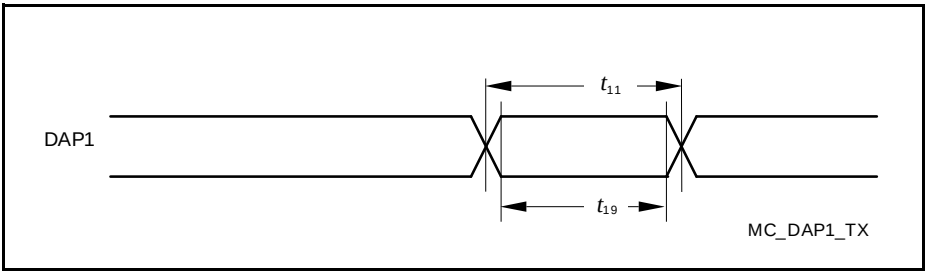


**Figure 26 DAP Timing Device to Host**

*Note: The transmission timing is determined by the receiving debugger by evaluating the sync-request synchronization pattern telegram.*

### Debug via JTAG

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

*Note: Operating Conditions apply; $C_L$= 20 pF.*

**Table 42 Interface Timing for Upper Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| TCK clock period | $t_1$ SR | 50[1] | – | – | ns | [2] |
| TCK high time | $t_2$ SR | 16 | – | – | ns | |
| TCK low time | $t_3$ SR | 16 | – | – | ns | |
| TCK clock rise time | $t_4$ SR | – | – | 8 | ns | |
| TCK clock fall time | $t_5$ SR | – | – | 8 | ns | |
| TDI/TMS setup to TCK rising edge | $t_6$ SR | 6 | – | – | ns | |
| TDI/TMS hold after TCK rising edge | $t_7$ SR | 6 | – | – | ns | |
| TDO valid from TCK falling edge (propagation delay)[3] | $t_8$ CC | – | 25 | 29 | ns | |
| TDO high impedance to valid output from TCK falling edge[4][3] | $t_9$ CC | – | 25 | 29 | ns | |
| TDO valid output to high impedance from TCK falling edge[3] | $t_{10}$ CC | – | 25 | 29 | ns | |
| TDO hold after TCK falling edge[3] | $t_{18}$ CC | 5 | – | – | ns | |

1) The debug interface cannot operate faster than the overall system, therefore $t_1 \geq t_{SYS}$.

2) Under typical conditions, the interface can operate at transfer rates up to 20 MHz.

3) The falling edge on TCK is used to generate the TDO timing.

4) The setup time for TDO is given implicitly by the TCK cycle time.

**Table 43 Interface Timing for Lower Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| TCK clock period | $t_1$ SR | 50[1] | – | – | ns | |
| TCK high time | $t_2$ SR | 16 | – | – | ns | |
| TCK low time | $t_3$ SR | 16 | – | – | ns | |
| TCK clock rise time | $t_4$ SR | – | – | 8 | ns | |
| TCK clock fall time | $t_5$ SR | – | – | 8 | ns | |
| TDI/TMS setup to TCK rising edge | $t_6$ SR | 6 | – | – | ns | |
| TDI/TMS hold after TCK rising edge | $t_7$ SR | 6 | – | – | ns | |
| TDO valid from TCK falling edge (propagation delay)[2] | $t_8$ CC | – | 32 | 36 | ns | |
| TDO high impedance to valid output from TCK falling edge[3][2] | $t_9$ CC | – | 32 | 36 | ns | |
| TDO valid output to high impedance from TCK falling edge[2] | $t_{10}$ CC | – | 32 | 36 | ns | |
| TDO hold after TCK falling edge[2] | $t_{18}$ CC | 5 | – | – | ns | |

1) The debug interface cannot operate faster than the overall system, therefore $t_1 \geq t_{SYS}$.

2) The falling edge on TCK is used to generate the TDO timing.

3) The setup time for TDO is given implicitly by the TCK cycle time.

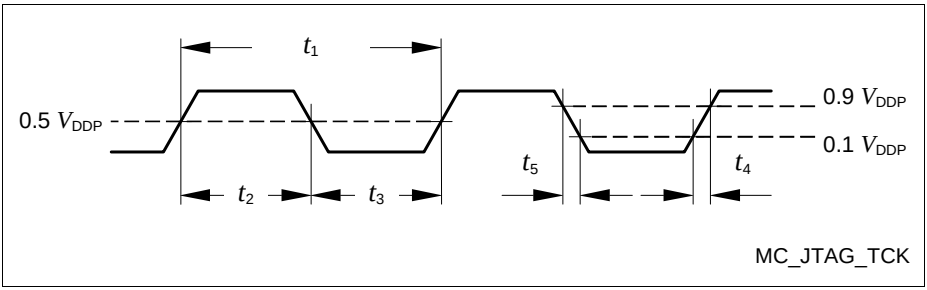


**Figure 27 Test Clock Timing (TCK)**

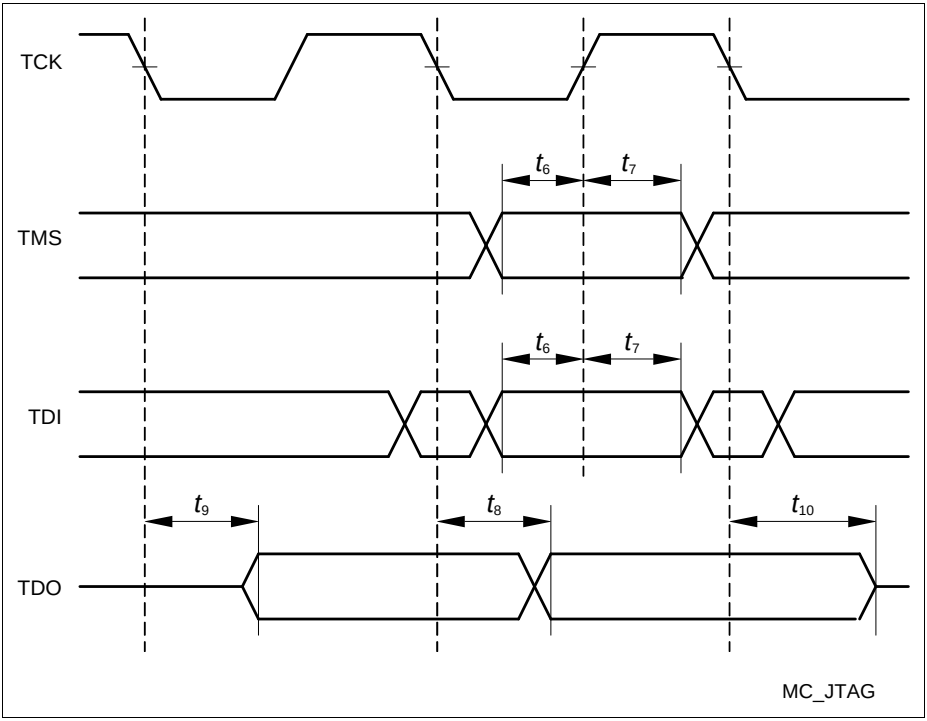


**Figure 28 JTAG Timing**

# 5 Package and Reliability

The XC2000 Family devices use the package type PG-LQFP (Plastic Green - Low Profile Quad Flat Package). The following specifications must be regarded to ensure proper integration of the XC2268I in its target environment.

## 5.1 Packaging

These parameters specify the packaging rather than the silicon.

**Table 44 Package Parameters (PG-LQFP-100-8/-15)**

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Exposed Pad Dimension | Ex × Ey | – | 7.5 × 7.5 | mm | – |
| Thermal resistance Junction-Ambient | $R_{\Theta JA}$ | – | 23 | K/W | 4-layer, pad soldered[1)] |

1) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad soldered to the board.
Using this device without the exposed pad soldered or on boards without thermal vias is not recommended.

*Note: To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground, independent of the thermal requirements.*
*Board layout examples are given in an application note.*

### Usage in High-Performance Applications

The XC2268I can deliver a high performance to the system. In some cases additional measures are required to remove the heat from the device.

This may be necessary if the XC2268I is supplied with $V_{DDP}$ = 5 V and is operated at a high system frequency in a hot environment.

Applications with $V_{DDP}$ = 3.3 V usually require no extra measures.

### Package Compatibility Considerations

The XC2268I is a member of the XC2000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Pad (if present) may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

## Package Outlines

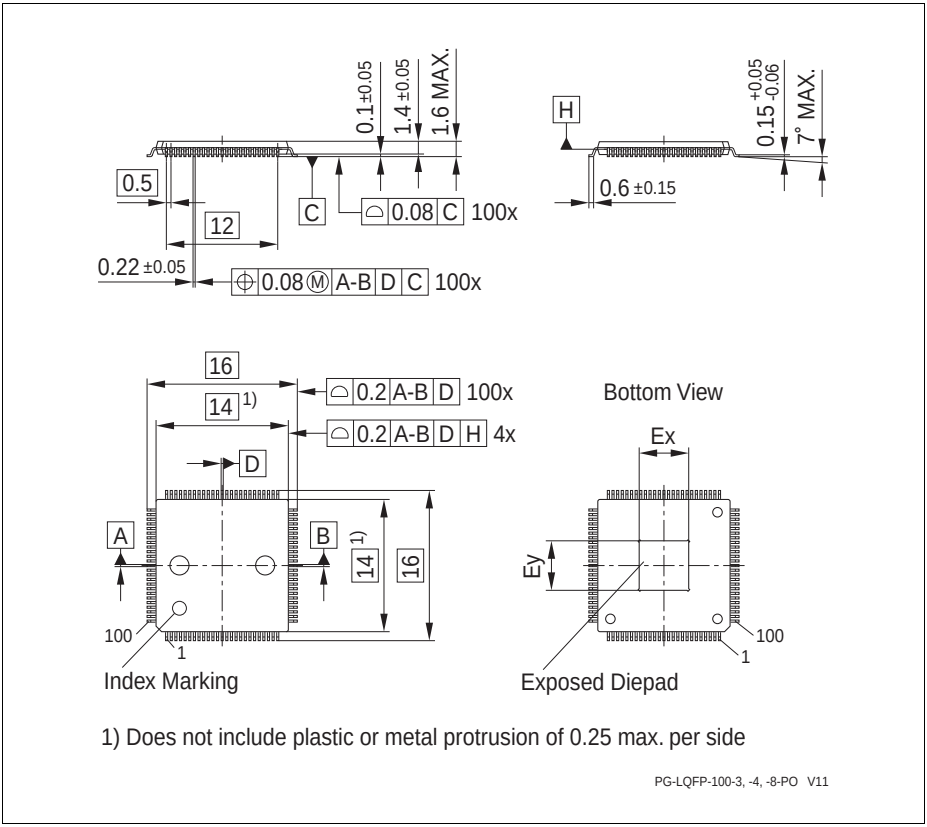


**Figure 29 PG-LQFP-100-8/-15** (Plastic Green Thin Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages**

## 5.2 Thermal Considerations

When operating the XC2268I in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by
$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers ($P_{IODYN}$) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce $V_{DDP}$, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

## 5.3 Quality Declarations

The operation lifetime of the XC2268I depends on the applied temperature profile in the application. For a typical example, please refer to **Table 46**; for other profiles, please contact your Infineon counterpart to calculate the specific lifetime within your application.

**Table 45 Quality Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operation lifetime | $t_{OP}$ CC | – | – | 20 | a | See **Table 46** and **Table 47** |
| ESD susceptibility according to Human Body Model (HBM) | $V_{HBM}$ SR | – | – | 2 000 | V | AEC-Q100-002 |
| ESD susceptibility according to Charged Device Model (CDM) | $V_{CDM}$ SR | – | – | 500 | V | JESD22-C101 |
| | | – | – | 750 | V | Corner Pins, JESD22-C101 |
| Moisture sensitivity level | MSL CC | – | – | 3 | – | JEDEC J-STD-020C |

**Table 46 Typical Usage Temperature Profile**

| Operating Time (Sum = 20 years) | Operating Temperat. | Notes |
|---|---|---|
| 1 200 h | $T_J$ = 150°C | Normal operation |
| 3 600 h | $T_J$ = 125°C | Normal operation |
| 7 200 h | $T_J$ = 110°C | Normal operation |
| 12 000 h | $T_J$ = 100°C | Normal operation |
| 7 × 21 600 h | $T_J$ = 0…10°C, …, 60…70°C | Power reduction |

**Table 47 Long Time Storage Temperature Profile**

| Operating Time (Sum = 20 years) | Operating Temperat. | Notes |
|---|---|---|
| 2 000 h | $T_J$ = 150°C | Normal operation |
| 16 000 h | $T_J$ = 125°C | Normal operation |
| 6 000 h | $T_J$ = 110°C | Normal operation |
| 151 200 h | $T_J \leq$ 150°C | No operation |

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