128Mb (16MB)/256Mb (32MB) Multiplexed MIRRORBIT™ Flash

16-bit data bus, 1.8V

General description

The Infineon S29VS256/128R and S29XS256/128R are MIRRORBIT™ flash products fabricated on 65-nm process technology. These burst mode flash devices are capable of performing simultaneous read and write operations with zero latency on two separate banks using multiplexed data and address pins. These products can operate up to 108 MHz and use a single V_{CC} of 1.7 V to 1.95 V that makes them ideal for the demanding wireless applications of today that require higher density, better performance, and lowered power consumption. The S29VS256/128R operates in ADM mode, while the S29XS256/128R can operate in the AADM mode.

Features

- Single 1.8 V supply for read/program/erase (1.70–1.95 V)
- 65-nm MIRRORBIT™ technology
- Address and data interface options
  - Address and data multiplexed for reduced I/O count (ADM) S29VS-R
  - Address-high, address-low, data multiplexed for minimum I/O count (AADM) S29XS-R
- Simultaneous read/write operation
- 32-word write buffer
- Bank architecture
  - Eight-bank
- Four 32-KB sectors at the top or bottom of memory array 255/127 of 128-KB sectors
- Programmable linear (8/16-word) with wrap around and continuous burst read modes
- Secured silicon sector region consisting of 128 words each for factory and customer
- 10-year data retention (typical)
- Cycling endurance: 100,000 cycles per sector (typical)
- RDY output indicates data available to system
- Command set compatible with JEDEC (42.4) standard
- Hardware sector protection via V_{PP} pin
- Handshaking by monitoring RDY
- Offered packages
  - 44-ball FBGA (6.2 mm × 7.7 mm × 1.0 mm)
- Low V_{CC} write inhibit
- Write operation status bits indicate program and erase operation completion
- Suspend and Resume commands for program and erase operations
- Asynchronous program operation, independent of burst control register settings
- V_{PP} input pin to reduce factory programming time
- Support for common flash interface (CFI)

Performance characteristics

Read access times	
Speed option (MHz)	108
Max. synch. latency, ns ($t_{IA)}$	72.34
Max. synch. burst access, ns ($t_{BACC)}$	6.75
Max. asynch. access time, ns (t_{ACC})	80
Max OE# access time, ns (t_{OE})	15

Current consumption (Typical values)	
Continuous burst read @ 108 MHz	32 mA
Simultaneous operation @ 108 MHz	71 mA
Program/erase	30 mA
Standby mode	30 µA

Typical program and erase times	
Single word programming	170 µs
Effective write buffer programming (V_{CC}) Per Word	14.1 µs
Effective write buffer programming (V_{PP}) Per Word	9 µs
Sector erase (16 Kword sector)	350 ms
Sector erase (64 Kword sector)	800 ms

Block diagram

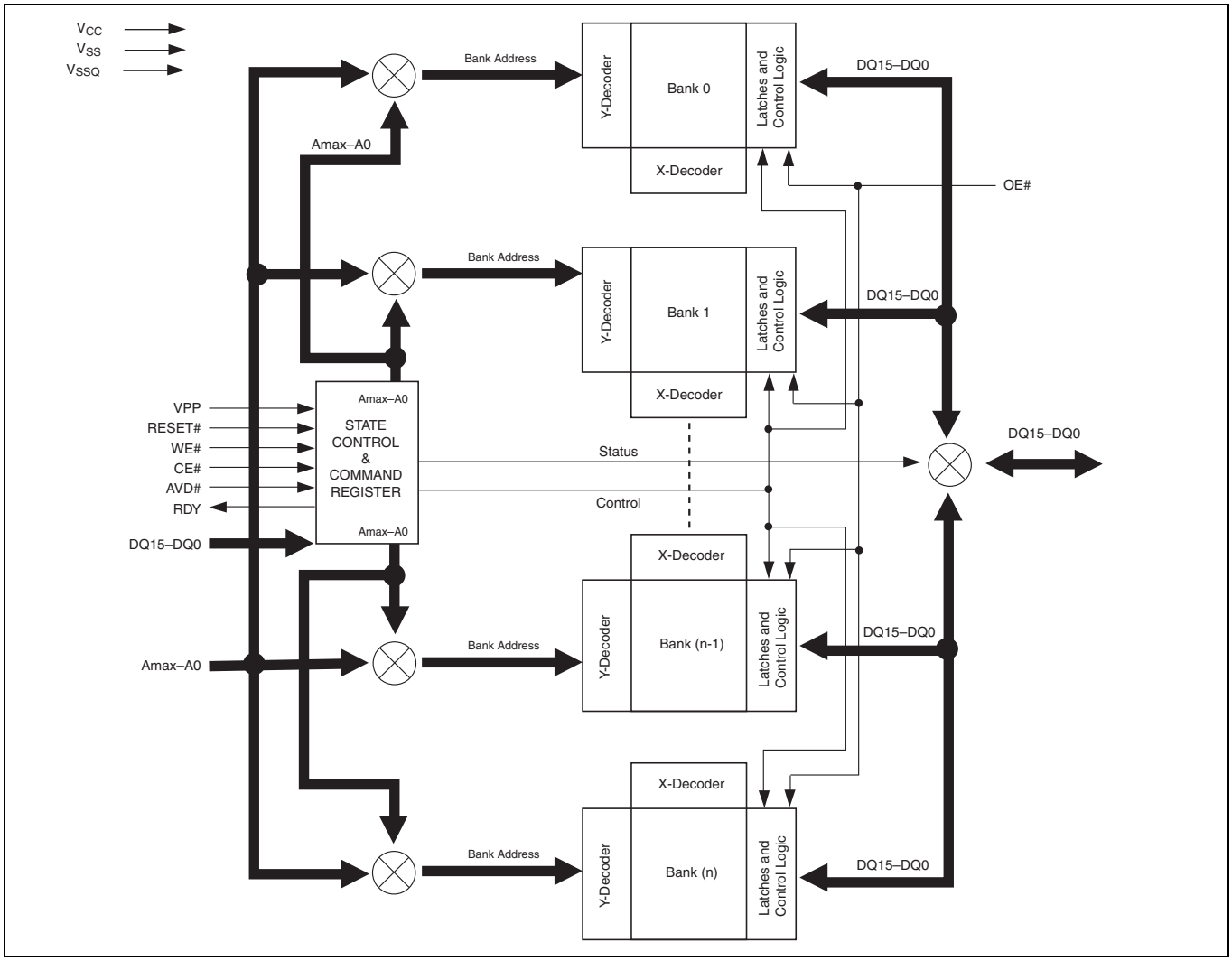

Figure 1 Simultaneous operation circuit

Notes
1. Amax = A23 for S29VS/XS256R, A22 for S29VS/XS128R.
2. Bank(n) = 8 (S29VS/XS256/128R).

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1 Input/output descriptions and logic symbol

Table 1 identifies the input and output package connections provided on the device.

Table 1 Input/output descriptions

Symbol	Type	Description
Amax – A16		Higher order address lines. Amax = A23 for VS256R, A22 for VS128R. On the XS256R and XS128R, these inputs can be left unconnected in AADM mode.
A/DQ15 – A/DQ0	I/O	Multiplexed address/data input/output
CE#	Input	Flash Chip Enable. Asynchronous relative to CLK.
OE#	Input	Output Enable. Asynchronous relative to CLK for the Burst mode.
WE#	Input	Write Enable
V_{CC}	Supply	Device Power Supply
V_{CCQ}	Supply	Input/Output Power Supply (must be ramped simultaneously with V_{CC})
V_{SS}	I/O	Ground
V_{SSQ}	I/O	Input/Output Ground
NC	No Connect	No Connected internally
RDY	Output	Ready. Indicates when valid burst data is ready to be read
CLK	Input	The first rising edge of CLK in conjunction with AVD# low latches address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access
AVD#	Input	Address Valid input. Indicates to device that the valid address is present on the address inputs (address bits A15 – A0 are multiplexed, address bits Amax – A16 are address only). V_{IL} = for asynchronous mode, indicates valid address; for burst mode, cause staring address to be latched on rising edge of CLK. V_{IH} = device ignores address inputs
RESET#	Input	Hardware Reset. Low = Device resets and returns to reading array data.
V_{PP}	Input	Accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.
RFU	Reserved	Reserved for future use

2 Product overview

The S29VS/XS-R family is 1.8-V only, simultaneous read/write, burst-mode, flash devices. These devices have a 16-bit (word) wide data bus. All read accesses provide 16-bits of data on each bus transfer cycle. All writes take 16-bits of data from each bus transfer cycle.

Table 2 Product overview

Device	Mb	MB	Mwords	Banks	MB/bank
S29VS128R/S29XS128R	128	16	8	8	2
S29VS256R/S29XS256R	256	32	16	8	4

The flash memory array is divided into banks. A bank is the address range within which one program, or erase operation may be in progress at the same time as one read operation is in progress in any other bank of the memory. This multiple bank structure enables simultaneous read and write (SRW) so that code may be executed or data read from one bank while a group of data is programmed, or erased as a background task in one other bank.

Each bank is divided into sectors. A sector is the minimum address range of data which can be erased to an all Ones state. Most of the sectors are 128 KB each. Depending on the option ordered, either the top-4 sectors or the bottom-4 sectors are 32 KB each. These are called boot sectors because they are often used for holding boot code or parameters that need to be protected or erased separately from other data in the flash array.

Programming is done via a 64 Byte write buffer. It is possible to program from one to 32 words (64 bytes) in each programming operation.

The S29VS/XS family is capable of continuous, synchronous (burst) read or linear read (8- or 16-word aligned group) with wrap around. A wrapped burst begins at the initial location and continues to the end of an 8, or 16-word aligned group then “wraps-around” to continue at the beginning of the 8, or 16-word aligned group. The burst completes with the last word before the initial location. Word wrap around burst is generally used for processor cache line fill.

3 Address space maps

There are five address spaces within each device:

- A non-volatile flash memory array used for storage of data that may be randomly accessed by asynchronous or burst read operations.
- A read only memory array used for factory programmed permanent device characteristics information. This area contains the device identification (ID) and common flash interface (CFI) information.
- A One time programmable (OTP) non-volatile flash array used for factory programmed permanent data, and customer programmable permanent data. This is called the secure silicon region (SSR).
- An OTP location used to permanently protect the SSR. This is call the SSR Lock.
- A volatile register used to configure device behavior options. This is called the Configuration Register.

The main flash memory array is the primary and default address space but, it may be partially overlaid by the other four address spaces with one alternate address space available at any one time. The location where the alternate address space is overlaid is defined by the address provided in the command that enables each overlay. The portion of the command address that is sufficient to select a sector is used to select the sector that is overlaid by an alternate address space overlay (ASO).

Any address range, within the overlaid sector, not defined by an overlay address map, is reserved for future use. All read accesses outside of an address map within the selected sector, return non-valid data. The locations will display actively driven data but the meaning of whatever ones or zeros appear are not defined.

There are three operation modes for each bank that determine what portions of the address space are readable at any given time:

- Read mode
- Embedded algorithm (EA) mode
- Address space overlay (ASO) mode

Each bank of the device can be in any operation mode but, only one bank can be in EA or ASO mode at any one time.

In read mode, a flash memory array bank may be directly read by asynchronous or burst accesses from the host system bus. The control unit (CU) puts all banks in read mode during power-on, a hardware reset, after a command reset, or after a bank is returned to read mode from EA mode.

In EA mode the flash memory array data in a bank is stable but undefined, and effectively unavailable for read access from the host system. While in EA mode the bank is used by the CU in the execution of commands. Typical EA mode operations are programming or erasing of data in the flash array. All other banks are available for read access while the one bank is in EA mode. This ability to read from one bank while another bank is used in the execution of a command is called simultaneous read and write (SRW) and allows for continued operation of the system via the reading of data or execution of code from other banks while one bank is programming or erasing data as a relatively long time frame background task.

In ASO mode, one of the overlay address spaces are overlaid in a bank (entered). That bank is in ASO mode and no other bank may be in EA or ASO mode. All EA activity must be completed before entering any ASO mode. A command for entering an EA or ASO mode while another bank is in EA or ASO mode will be ignored.

While an ASO mode is active (entered) in a bank, a read for Flash array data to any other bank is allowed. ASO mode selects a specific sector for the overlaid address space. Other sectors in the ASO bank still provide flash array data and may be read during ASO mode.

The ASOs are functionally tied to the lowest address bank. The commands used to overlay (enter) these areas must select a sector address within the lowest address bank.

While SSR Lock, SSR, or Configuration Register is overlaid only the SSR Lock, SSR, or Configuration Register respectively may be programmed in the overlaid sector. While any of these ASO areas are being programmed the ASO bank switches to EA mode. The ID/CFI and factory portion of the SSR ASO is not customer programmable.

The address nomenclature used in this document is a shorthand form that shows addresses are formed from a concatenation of high order bits, sufficient to select a sector address (SA), with low order bits to select a location within the sector. When in read mode and reading from the flash array the entire address is used to select a specific word for asynchronous read or the starting word address of a burst read. When writing a command, the address bits between SA and the command specified least significant bits must be zero to allow for future extension of an overlay address map.

3.1 Data address and quantity nomenclature

A bit is a single one or zero data value. A byte is a group of 8 bits aligned on an 8-bit boundary. A word is a group of 16-bits aligned on a 16-bit boundary.

Throughout this document **quantities of data are generally expressed in terms of byte units**. Example: most sectors have 128 Kilo Bytes of data and is written as 128 KBytes or 128 KB. **Addresses are also expressed in byte units**. A 128 KB sector has an address range from 00000h to 1FFFFh Byte locations. Byte units are used because most host systems and software for these systems use byte resolution addresses. Software and hardware developers most often calculate code and data sizes in terms of bytes, so this is more familiar terminology than describing data sizes in bits or words. In general, data units will not be abbreviated if possible so that full unit names of Byte, Word, or bit are used. However, there may be cases where capital B is used for byte units and lower case b is used for bit units, in situations where space is limited such as in table column headers.

In some cases data quantities will also be expressed in word or bit units in addition to the quantity shown in bytes. This may be done as an aid to readers familiar with prior device generation documentation which often provided only word or bit unit values. Word units may also be used to emphasize that, in the memory devices described in this documentation, data is always exchanged with the host system in word units. Each bus cycle transfer of read or write data on the host system bus is a transfer 16-bits of data. A read bus cycle is always a 16-bit wide transfer of data to the host system whether the host system chooses to look at all the bits or not. A write bus cycle is always a transfer of 16-bits to the memory device and the device will store all 16-bits to a register. In the case of a program operation all 16-bits of each word to be programmed will be stored in the flash array.

Because data is always transferred in word units, the memory devices being discussed use only the address signals from the system necessary to select words. The host system byte address uses system address a0 to select bytes and a1 to select words. Flash memories with word wide data paths have traditionally started their address signal numbering with A0 being the selector for words because a byte select input is not needed. So, system address a-maximum to a1 are connected to flash A-maximum to A0 (the documentation convention here is to use lower case for system address signal numbering and upper case for flash address signals). In prior generation Flash documentation, address values used in commands to the flash were documented from the viewpoint of the Flash device - the bit pattern appearing on flash address inputs A10 to A0. However, most software is written with addresses expressed in bytes. This means the address patterns shown in Flash command tables have traditionally been shifted by one bit to express them as byte address values in Flash control programs. Example: a prior generation flash datasheet would show a command write of data value xxA0h to address 555h; this is an address pattern of 10101010101b on flash address inputs A10 to A0; but software would define this as a byte address value of AAAh since the least significant address bit is not used by the flash); which is 101010101010b on system address bus a11 to a0. Because system a11 to a1 is connected to flash A10 to A0 the flash word address of 555h and the system byte address of AAAh provides the same bit pattern on the same address inputs. Because all address values are being documented as system byte addresses, that are more familiar to software writers, the command tables have addresses that are shifted from those shown in prior generation devices.

3.2 Flash memory array

The non-volatile flash memory array is organized as shown in the following tables. Devices are factory configured to have either all uniform size sectors or four smaller sectors at either the top of the device.

Table 3 System versus flash view of address

System address signals	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0
System byte address hex	A				A				A			
Binary pattern	1	0	1	0	1	0	1	0	1	0	1	0
Flash word address hex	5			5				5				
Flash address signals	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	

Table 4 S29VS/XS256R sector and memory address map (Top boot)

Bank size (Mb)	Sector count	Sector size (KB)	Bank	Sector range	Address range (Word)	Address range (Byte)	Notes
32	224	128	0	SA000-SA031	000000h–1FFFFFh	000000h–3FFFFFh	Sector starting address – Sector ending address
			1	SA032–SA063	⋮	⋮	
			2	SA064–SA095	⋮	⋮	
			3	SA096–SA127	⋮	⋮	
			4	SA128–SA159	⋮	⋮	
			5	SA160–SA191	⋮	⋮	
			6	SA192–SA223	⋮	⋮	
	31	128	7	SA224–SA254	E00000h–FEFFFFh	1C00000h–1FDFFFFh	
	4	32		SA255	FF0000h–FF3FFFh	1FE0000h–1FE7FFFh	
				SA256	FF4000h-FF7FFFh	1FE8000h-1FEFFFFh	
				SA257	FF8000h–FFBFFFh	1FF0000h–1FF7FFFh	
				SA258	FFC000h–FFFFFFh	1FF8000h–1FFFFFFh	

Note

All tables have been condensed to show sector-related information for an entire device on a single page. Sectors and their address ranges that are not explicitly listed (such as SA008–SA009) have sector starting and ending addresses that form the same pattern as all other sectors of that size. For example, all 128 KB sectors have the byte address pattern x000000h–x1FFFFh.

Table 5 S29VS/XS256R sector and memory address map (Bottom boot)

Bank size (Mb)	Sector count	Sector size (KB)	Bank	Sector range	Address range (Word)	Address range (Byte)	Notes
32	4	32	0	SA000	000000h–003FFFh	000000h–007FFFh	Sector starting address – Sector ending address
				SA001	004000h–007FFFh	008000h–00FFFFh	
				SA002	008000h–00BFFFh	010000h–017FFFh	
				SA003	00C000h–00FFFFh	018000h–01FFFFh	
	31	128		SA004–SA034	010000h–1FFFFFh	020000h–3FFFFFh	
	224	128	1	SA035–SA066	⋮	⋮	
			2	SA067–SA098	⋮	⋮	
			3	SA099–SA130	⋮	⋮	
			4	SA131–SA162	⋮	⋮	
			5	SA163–SA194	⋮	⋮	
			6	SA195–SA226	⋮	⋮	
			7	SA227–SA258	E00000h–FFFFFFh	1C00000h–1FFFFFFh	

Note
All tables have been condensed to show sector-related information for an entire device on a single page. Sectors and their address ranges that are not explicitly listed (such as SA008–SA009) have sector starting and ending addresses that form the same pattern as all other sectors of that size. For example, all 128 KB sectors have the byte address pattern x000000h–x1FFFFh.

Table 6 S29VS/XS128R sector and memory address map (Top boot)

Bank size (Mb)	Sector count	Sector size (KB)	Bank	Sector range	Address range (Word)	Address range (Byte)	Notes
16	112	128	0	SA000-SA015	000000h–0FFFFFh	000000h–1FFFFFh	Sector starting address – Sector ending address
			1	SA016–SA031	⋮	⋮	
			2	SA032–SA047	⋮	⋮	
			3	SA048–SA063	⋮	⋮	
			4	SA064–SA079	⋮	⋮	
			5	SA080–SA095	⋮	⋮	
			6	SA096–SA111	⋮	⋮	
	15	128	7	SA112–SA126	700000h–7EFFFFh	E00000h–FDFFFFh	
	4	32		SA127	7F0000h–7F3FFFh	FE0000h–FE7FFFh	
				SA128	7F4000h-7F7FFFh	FE8000h-FEFFFFh	
				SA129	7F8000h–7FBFFFh	FF0000h–FF7FFFh	
				SA130	7FC000h–7FFFFFh	FF8000h–FFFFFFh	

Note
All tables have been condensed to show sector-related information for an entire device on a single page. Sectors and their address ranges that are not explicitly listed (such as SA008–SA009) have sector starting and ending addresses that form the same pattern as all other sectors of that size. For example, all 128 KB sectors have the byte address pattern x000000h–x1FFFFh.

Table 7 S29VS/XS128R sector and memory address map (Bottom boot)

Bank size (Mb)	Sector count	Sector size (KB)	Bank	Sector range	Address range (word)	Address range (byte)	Notes
16	4	32	0	SA000	000000h–003FFFh	000000h–007FFFh	Sector starting address – Sector ending address
				SA001	004000h–007FFFh	008000h–00FFFFh	
				SA002	008000h–00BFFFh	010000h–017FFFh	
				SA003	00C000h–00FFFFh	018000h–01FFFFh	
	15	128		SA004–SA018	010000h–0FFFFFh	020000h–1FFFFFh	
	112	128	1	SA019–SA034	⋮	⋮	
			2	SA035–SA050	⋮	⋮	
			3	SA051–SA066	⋮	⋮	
			4	SA067–SA082	⋮	⋮	
			5	SA083–SA098	⋮	⋮	
			6	SA099–SA114	⋮	⋮	
			7	SA115–SA130	700000h–7FFFFFh	E00000h–FFFFFFh	

Note
All tables have been condensed to show sector-related information for an entire device on a single page. Sectors and their address ranges that are not explicitly listed (such as SA008–SA009) have sector starting and ending addresses that form the same pattern as all other sectors of that size. For example, all 128 KB sectors have the byte address pattern x000000h–x1FFFFh.

3.3 Address/data interface

There are two options for connection to the address and data buses.

- Address and data multiplexed (ADM) mode. On the S29VS-R devices, the upper address is supplied on separate signal inputs and the lower 16-bits of address are multiplexed with 16-bit data on the A/DQ15 to A/DQ0 I/Os.
- Address-high, address-low, and data multiplexed (AADM) mode. On the S29XS-R devices, the upper and lower address are multiplexed with 16-bit data on the A/DQ15 to A/D0 signal I/Os.

The two options allow use with the traditional address/data multiplexed NOR interface (S29NS family), or an address multiplexed/data multiplexed interface with the lowest signal count.

3.3.1 ADM interface (S29VS256R and S29VS128R)

A number of processors use ADM interface as a way to reduce pin count. The system permanently connects the upper address bits (A[MAX:16] to the device. When AVD# is LOW it connects A[15:0] to DQ[15:0]. The address is latched on the rising edge of AVD#. When AVD# is HIGH, the system connects the data bus to DQ[15:0]. This results in 16-pin savings from the traditional Address and Data in Parallel (ADP) interface.

3.3.2 AADM interface (S29XS256R and S29XS128R)

Signal input and output (I/O) connections on a high complexity component such as an Application Specific Integrated Circuit (ASIC) are a limited resource. Reducing signal count on any interface of the ASIC allows for either more features or lower package cost. The memory interface described in this section is intended to reduce the I/O signal count associated with the Flash memory interface with an ASIC.

The interface is called Address-High, Address-Low, and Data Multiplexed (AADM) because all address and data information is time multiplexed on a single 16-bit wide bus. This interface is electrically compatible with existing ADM 16-bit wide random access static memory interfaces but uses fewer address signals. In that sense AADM is a signal count subset of existing static memory interfaces. This interface can be implemented in existing memory controller designs, as an additional mode, with minimal changes. No new I/O technology is needed and existing memory interfaces can continue to be supported while the electronics industry adopts this new interface. ASIC designers can reuse the existing memory address signals above A15 for other functions when an AADM memory is in use.

By breaking up the memory address in to two time slots the address is naturally extended to be a 32-bit word address. But, using two bus cycles to transfer the address increases initial access latency by increasing the time address is using the bus. However, many memory accesses are to locations in memory nearby the previous access. Very often it is not necessary to provide both cycles of address. This interface stores the high half of address in the memory so that if the high half of address does not change from the previous access, only the low half of address needs to be sent on the bus. If a new upper address is not captured at the beginning of an access the last captured value of the upper address is used. This allows accesses within the same 128-KB address range to provide only the lower address as part of each access.

In AADM mode two signal rising edges are needed to capture the upper and lower address portions in asynchronous mode or two signal combinations over two clocks is needed in synchronous mode. In asynchronous mode the upper address is captured by an AVD# rising edge when OE# is Low; the lower address is captured on the rising edge of AVD# with OE# High. In synchronous mode the upper address is captured at the rising clock edge when AVD# and OE# are Low; the lower address is captured at the rising edge of clock when AVD# is Low and OE# is High.

CE# going High at any time during the access or OE# returning High after RDY is first asserted High during an access, terminates the read access and causes the address/data bus direction to switch back to input mode. The address/data bus direction switches from input to output mode only after an Address-Low capture when AVD# is Low and OE# is High. This prevents the assertion of OE# during Address-High capture from causing a bus conflict between the host address and memory data signals. Note, in burst mode, this implies at least one cycle of CE# or OE# High before an Address-high for a new access may be placed on the bus so that there is time for the memory to recognize the end of the previous access, stop driving data outputs, and ignore OE# so that assertion of OE# with the new Address-high does not create a bus conflict with a new address being driven on the bus. At high bus frequencies more than one cycle may be need in order to allow time for data outputs to stop driving and new address to be driven (bus turn around time).

During a write access, the address/data bus direction is always in the input mode.

The upper address is set to Zero or all Ones, for bottom or top boot respectively, during a Hardware Reset, operate in ADM mode during the early phase of boot code execution where only a single address cycle would be issued with the lower 16 bit of the address reaching the memory in AADM mode. The default high order address bits will direct the early boot accesses to the 128 KB at the boot end of the device. Note that in AADM interface mode this effectively requires that one of the boot sectors is selected for any address overlay mode because in the initial phase of AADM mode operation the host memory controller may only issue the low order address thus limiting the early boot time address space to the 128 KB at the boot end of the device.

3.3.3 Default access mode

Upon power-up or hardware reset, the device defaults to the Asynchronous Access mode.

3.4 Bus operations

Table 8 describes the required state of each input signal for each bus operation.

Table 8 Device bus operations

Operation	CE#	OE#	WE#	CLK	AVD#	A28-A16	A/DQ 15-A/DQ0	RESET#
Standby and reset								
Standby (CE# deselect)	H	X	X	X	X	X	High-Z	H
Hardware reset	X	X	X	X	X	X	High-Z	L
Asynchronous mode operations								
Asynchronous address latch (S29VS256R and S29VS128R)	L	H	X	X	↑	Addr In	Addr In	H
Asynchronous upper address latch (S29XS256R and S29XS128R only)	L	L	H	X	↑	X	Addr In	H
Asynchronous lower address latch (S29XS256R and S29XS128R only)	L	H	X	X	↑	X	Addr In	H
Asynchronous read	L	L	H	X	H	X	Data output valid	H
Asynchronous write latched data	L	H	↑	X	H	X	Data input valid	H
Synchronous mode operations								
Latch starting burst address by CLK - ADM mode	L	H	H	↑	L	Addr In	Addr In	H
Latch upper starting burst address by CLK (S29XS256R and S29XS128R only)	L	L	H	↑	L	X	Addr In	H
Latch lower starting burst address by CLK (S29XS256R and S29XS128R only)	L	H	H	↑	L	X	Addr In	H
Burst read and advance to next address [3]	L	L	H	↑	H	X	Data output valid	H
Terminate current burst cycle	↑	X	X	X	X	X	High-Z	H

Legend:

L = Logic 0, H = Logic 1, X = can be either V_{IL} or V_{IH}. ↑ = rising edge.

Note

3. Data is delivered by a read operation only after the burst initial wait state count has been satisfied.

3.5 Device ID and CFI (ID-CFI)

There are two traditional methods for systems to identify the type of flash memory installed in the system. One has been traditionally been called Autoselect and is now referred to as device identification (ID). A command is used to enable an address space overlay where up to 16 word locations can be read to get JEDEC manufacturer identification (ID), device ID, and some configuration and protection status information from the Flash memory. The system can use the manufacturer and device IDs to select the appropriate driver software to use with the Flash device. The other method is called Common Flash Interface (CFI). It also uses a command to enable an address space overlay where an extendable table of standard information about how the Flash memory is organized and behaves can be read. With this method the driver software does not have to be written with the specifics of each possible memory device in mind. Instead the driver software is written in a more general way to handle many different devices but adjusts the driver behavior based on the information in the CFI table stored in the Flash memory. Traditionally these two address spaces have used separate commands and were separate overlays. However, the mapping of these two address spaces are non-overlapping and so can be combined in to a single address space and appear together in a single overlay. Either of the traditional commands used to access (enter) the Autoselect (ID) or CFI overlay will cause the now combined ID-CFI address map to appear.

A write at any sector address, in bank zero, having the least significant byte address value of AAh, with xx98h or xx90h data, switches the addressed sector to an overlay of the ID-CFI address map. These are called ID-CFI Enter commands and are only valid when written to the specified bank when it is in read mode. The ID-CFI address map appears within, and replaces flash array data of, the selected sector address range. The ID-CFI enter commands use the same address and data values used on previous generation memories to access the JEDEC manufacturer ID (Autoselect) and common flash interface (CFI) information, respectively. While the ID-CFI address space is overlaid, any write with xxF0h data to the device will remove the overlay and return the selected sector to showing flash memory array data. Thus, the ID-CFI address space and commands are backward compatible with standard memory discovery algorithms.

Within the ID-CFI address map there are two subsections:

Table 9 ID-CFI address map overview

Byte address	Description	Size allocated (Bytes)	Read/write
(SA) + 00000h to 0001Fh	JEDEC ID (traditional Autoselect values)	32	Read only
(SA) + 00020h to 000BEh	CFI data structure	159	Read only

For the complete address map, see tables in **“Device ID and common flash memory interface address map”** on page 65.

3.5.1 JEDEC device ID

The Joint Electron Device Engineering Council (JEDEC) standard JEP106T defines a method for reading the manufacturer ID and device ID of a compliant memory. This information is primarily intended for programming equipment to automatically match a device with the corresponding programming algorithm.

The JEDEC ID information is structured to work with any memory data bus width e.g., x8, x16, x32. The code values are always byte wide but are located at bus width address boundaries such that incrementing the device address inputs will read successive byte, word, or double word locations with the codes always located in the least significant byte location of the data bus. Because the data bus is word wide each code byte is located in the lower half of each word location and the high order byte is always zero.

3.5.2 Common flash memory interface

The common flash interface (CFI) specification defines a standardized data structure that may be read from a flash memory device, which allows vendor-specified software algorithms to be used for entire families of devices. The data structure contains information for system configuration such as various electrical and timing parameters, and special functions supported by the device. Software support can then be device-independent, JEDEC ID-independent, and forward-and-backward-compatible for the specified flash device families.

The system can read CFI information at the addresses within the selected sector as shown in **"Device ID and common flash memory interface address map"** on page 65.

Like the JEDEC device ID information, CFI information is structured to work with any memory data bus width e.g., x8, x16, x32. The code values are always byte wide but are located at data bus width address boundaries such that incrementing the device address reads successive byte, word, or double word locations with the codes always located in the least significant byte location of the data bus. Because the data bus is word wide each code byte is located in the lower half of each word location and the high order byte is always zero.

For further information, please refer to the Infineon CFI Version 1.4 (or later) specification and the Infineon CFI publication 100 (see also JEDEC publications JEP137-A and JESD68.01). Please contact JEDEC (**www.jedec.org**) for their standards and the Infineon CFI publications may be found at the Infineon website (See **Common flash interface version 1.4 vendor specific extensions** application note at the time of this document's publication).

3.5.3 Secured silicon region

The secured silicon region provides an extra flash memory area that can be programmed once and permanently protected from further changes. The secured silicon region is 512 bytes in length. It consists of 256 bytes for factory data and 256 bytes for customer-secured data.

The secured silicon region (SSR) is overlaid in the sector address specified by the SSR enter command.

Table 10 Secured silicon region

Byte address range	Secure silicon region	Size
(SA) + 0000h to 00FFh	Factory	256 Bytes
(SA) + 0100h to 01FFh	Customer	256 Bytes

3.5.4 Configuration Register

The Configuration Register Enter command is only valid when written to a bank that is in read mode. The configuration register mode address map appears within, and replaces flash array data of, the selected sector address range. The meaning of the configuration register bits is defined in the configuration register operation description. In configuration register mode, a write of 00F0h to any address will return the sector to Read mode.

4 Device operations

This section describes the read and write bus operations, program, erase, simultaneous read/write, handshaking, and reset features of the flash devices.

The address space of the flash memory array is divided into banks. There are three operation modes for each bank:

- Read mode
- Embedded algorithm (EA) mode
- Address space overlay (ASO) mode

Each bank of the device can be in any operation mode but, only one bank can be in EA or ASO mode at any one time.

In read mode a flash memory array bank may be read by simply selecting the memory, supplying the address, and taking read data when it is ready. This is done by asynchronous or burst accesses from the host system bus. The CU puts all banks in read mode during power-on, a hardware reset, after a command reset, or after a bank is returned to read mode from EA mode.

During a burst read access valid read data is indicated by the RDY signal being High. When RDY is Low burst read data is not valid and wait states must be added. The use of the RDY signal to indicate when valid data is transferred on the system data bus is called handshaking or flow control.

EA and ASO modes are initiated by writing specific address and data patterns into command registers (see **Table 57**). The command registers do not occupy any memory locations; they are loaded by write bus cycles with the address and data information needed to execute a command. The contents of the registers serve as input to the control unit (CU) and the CU dictates the function of the device. Writing incorrect address and data values or writing them in an improper sequence may place the device in an unknown state, in which case the system must write the reset command to return all banks to read mode.

The flash memory array data in a bank that is in EA mode, is stable but undefined, and effectively unavailable for read access from the host system. While in EA mode the bank is used by the CU in the execution of commands. Typical command operations are programming or erasing of data in the flash array. All other banks are available for read access while the one bank is in EA mode. This ability to read from one bank while another bank is used in the execution of a command is called simultaneous read and write (SRW) and allows for continued operation of the system via the reading of data or code from other banks while one bank is programming or erasing data as a relatively long time frame background task. Only a status register read command can be used in a bank in EA mode to retrieve the EA status.

While any one of the overlay address spaces are overlaid in a bank (entered) that bank is in ASO mode and no other bank may be in EA or ASO mode. All EA activity must be completed or suspended before entering any ASO mode. A command for entering an EA or ASO mode while another bank is in EA or ASO mode will be ignored.

While an ASO mode is active (entered) in a bank, a read for flash array data to any other bank is allowed. ASO mode selects a specific sector for the overlaid address space. Other sectors in the ASO bank still provide flash array data and may be read during ASO mode.

While SSR Lock, SSR, or Configuration Register is overlaid only the SSR Lock, SSR, or Configuration Register respectively may be programmed in the overlaid sector. While any of these ASO areas are being programmed the ASO bank switches to EA mode. The ID/CFI and factory portion of the SSR ASO is not customer programmable. An attempt to program in these areas will fail.

4.1 Asynchronous read

The device defaults to reading array data asynchronously after device power-up or hardware reset. The device is in the asynchronous mode when bit 15 of the Configuration Register is set to '1'. To read data from the memory array, the system must first assert CE# and AVD# to V_{IL} with WE# at V_{IH} and a valid address.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable CE# to valid data at the outputs. See **"AC characteristics–Asynchronous read" on page 50**. Any input on CLK is ignored while in asynchronous mode.

4.1.1 S29VS-R ADM access

With CE# at V_{IL}, WE# at V_{IH}, and OE# at V_{IH}, the system presents the address to the device and drives AVD# to V_{IL}. AVD# is kept at V_{IL} for at least t_{AVDP} ns. The address is latched on the rising edge of AVD#.

4.1.2 S29XS-R AADM access

With CE# at V_{IL}, WE# at V_{IH}, and OE# at V_{IL}, the system presents the upper address bits to DQ and drives AVD# to V_{IL}. The upper address bits are latched when AVD# transitions to V_{IH}. The system then drives AVD# to V_{IL} again, with OE# at V_{IH} and the lower address bits on the DQ signals. The lower address bits are latched on the next rising edge of AVD#.

4.2 Synchronous (Burst) read mode and Configuration Register

The device is capable of continuous sequential burst operation and linear burst operation of a preset length.

In order to use synchronous (burst) read mode the configuration register bit 15 must be set to 0.

Prior to entering burst mode, the system should determine how many wait states are needed for the initial word of each burst access, what mode of burst operation is desired, how the RDY signal transitions with valid data, and output drive strength. The system would then write the configuration register command sequence. See **"Configuration Register"** on page 23 for further details.

When the appropriate number of Wait States have occurred, data is output after the **rising edge** of the CLK. Subsequent words are output t_{BACC} after the rising edge of each successive clock cycle, which automatically increments the internal address counter. RDY indicates the initial latency and any subsequent waits.

4.2.1 S29VS-R ADM access

To burst read data from the memory array in ADM mode, the system must assert CE# to V_{IL}, and provide a valid address while driving AVD# to V_{IL} for one cycle. OE# must remain at V_{IH} during the one cycle that AVD# is at V_{IL}. The data appears on A/DQ15 -A/DQ0 when CE# remains at V_{IL}, after OE# is driven to V_{IL} and the synchronous access times are satisfied. The next data in the burst sequence is read on each clock cycle that OE# and CE# remain at V_{IL}.

OE# does not terminate a burst access if it rises to V_{IH} during a burst access. The outputs will go to high impedance but the burst access will continue until terminated by CE# going to V_{IH}, or AVD# returns to V_{IL} with a new address to initiate a another burst access.

4.2.2 S29XS-R AADM access

To burst read data from the memory array in AADM mode, the system must assert CE# to V_{IL}, OE# must be driven to V_{IL} with AVD# for one cycle while the upper address is valid. The rising edge of CLK when OE# and AVD# are at V_{IL} captures the upper 16-bits of address. The rising edge of CLK when OE# is at V_{IH} and AVD# is at V_{IL} latches the lower 16-bits of address. The data appears on A/DQ15 -A/DQ0 when CE# remains at V_{IL}, after OE# is driven to V_{IL} and the synchronous access times are satisfied. The next data in the burst sequence is read on each clock cycle that OE# and CE# remain at V_{IL}.

Once OE# returns to V_{IH} during a burst read the OE# no longer enables the outputs until after AVD# is at V_{IL} with OE# at V_{IH} - which signals that address-low has been captured for the next burst access. This is so that OE# at V_{IL} may be used in conjunction with AVD# at V_{IL} to indicate address-high on the A/DQ signals without enabling the A/DQ outputs, thus avoiding data output contention with Address-high.

The device has a fixed internal address boundary that occurs every 256 Bytes (128 words). A boundary crossing latency of one or two additional wait states may be required. The device also reads data in 16 byte (8 word) aligned and length groups. When the initial address is not aligned at the beginning of a 16 byte boundary, additional wait states may be needed when crossing the first 16 byte boundary. The number of additional wait states depends on the clock frequency and starting address location.

Table 11 through **Table 19** provide the latency for initial and boundary crossing wait state operation (note that ws = wait state).

Table 11 Initial wait state vs. frequency

Wait state	Frequency (Maximum MHz)
3	27
4	40
5	54
6	66
7	80
8	95
9	104
10	120

Note
The default initial wait state delay after power on or reset is 13 wait states.

Table 12 Address latency for 10 -13 wait states

Word	Initial wait	Subsequent clock cycles after initial wait states									
0	10 -13 wait states	D0	D1	D2	D3	D4	D5	D6	D7	+2 ws [4]	D8
1		D1	D2	D3	D4	D5	D6	D7	1 ws	+2 ws	D8
2		D2	D3	D4	D5	D6	D7	1 ws	1 ws	+2 ws	D8
3		D3	D4	D5	D6	D7	1 ws	1 ws	1 ws	+2 ws	D8
4		D4	D5	D6	D7	1 ws	1 ws	1 ws	1 ws	+2 ws	D8
5		D5	D6	D7	1 ws	1 ws	1 ws	1 ws	1 ws	+2 ws	D8
6		D6	D7	1 ws	1 ws	1 ws	1 ws	1 ws	1 ws	+2 ws	D8
7		D7	1 ws	1 ws	1 ws	1 ws	1 ws	1 ws	1 ws	+2 ws	D8

Table 13 Address latency for 9 wait states

Word	Initial wait	Subsequent clock cycles after initial wait states									
0	9 wait states	D0	D1	D2	D3	D4	D5	D6	D7	+1 ws [4]	D8
1		D1	D2	D3	D4	D5	D6	D7	1 ws	+1 ws	D8
2		D2	D3	D4	D5	D6	D7	1 ws	1 ws	+1 ws	D8
3		D3	D4	D5	D6	D7	1 ws	1 ws	1 ws	+1 ws	D8
4		D4	D5	D6	D7	1 ws	1 ws	1 ws	1 ws	+1 ws	D8
5		D5	D6	D7	1 ws	1 ws	1 ws	1 ws	1 ws	+1 ws	D8
6		D6	D7	1 ws	1 ws	1 ws	1 ws	1 ws	1 ws	+1 ws	D8
7		D7	1 ws	1 ws	1 ws	1 ws	1 ws	1 ws	1 ws	+1 ws	D8

Note
4. This column applies to the 256 byte boundary only.

Table 14 Address latency for 8 wait states

Word	Initial wait	Subsequent clock cycles after initial wait states								
0	8 wait states	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	1 ws	D8
2		D2	D3	D4	D5	D6	D7	1 ws	1 ws	D8
3		D3	D4	D5	D6	D7	1 ws	1 ws	1 ws	D8
4		D4	D5	D6	D7	1 ws	1 ws	1 ws	1 ws	D8
5		D5	D6	D7	1 ws	1 ws	1 ws	1 ws	1 ws	D8
6		D6	D7	1 ws	1 ws	1 ws	1 ws	1 ws	1 ws	D8
7		D7	1 ws	1 ws	1 ws	1 ws	1 ws	1 ws	1 ws	D8

Table 15 Address latency for 7 wait states

Word	Initial wait	Subsequent clock cycles after initial wait states								
0	7 wait states	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	D4	D5	D6	D7	1 ws	D8	D9
3		D3	D4	D5	D6	D7	1 ws	1 ws	D8	D9
4		D4	D5	D6	D7	1 ws	1 ws	1 ws	D8	D9
5		D5	D6	D7	1 ws	1 ws	1 ws	1 ws	D8	D9
6		D6	D7	1 ws	1 ws	1 ws	1 ws	1 ws	D8	D9
7		D7	1 ws	1 ws	1 ws	1 ws	1 ws	1 ws	D8	D9

Table 16 Address latency for 6 wait states

Word	Initial wait	Subsequent clock cycles after initial wait states								
0	6 wait states	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	D4	D5	D6	D7	D8	D9	D10
3		D3	D4	D5	D6	D7	1 ws	D8	D9	D10
4		D4	D5	D6	D7	1 ws	1 ws	D8	D9	D10
5		D5	D6	D7	1 ws	1 ws	1 ws	D8	D9	D10
6		D6	D7	1 ws	1 ws	1 ws	1 ws	D8	D9	D10
7		D7	1 ws	1 ws	1 ws	1 ws	1 ws	D8	D9	D10

Table 17 Address latency for 5 wait states

Word	Initial wait	Subsequent clock cycles after initial wait states								
0	5 wait states	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	D4	D5	D6	D7	D8	D9	D10
3		D3	D4	D5	D6	D7	D8	D9	D10	D11
4		D4	D5	D6	D7	1 ws	D8	D9	D10	D11
5		D5	D6	D7	1 ws	1 ws	D8	D9	D10	D11
6		D6	D7	1 ws	1 ws	1 ws	D8	D9	D10	D11
7		D7	1 ws	1 ws	1 ws	1 ws	D8	D9	D10	D11

Table 18 Address latency for 4 wait states

Word	Initial wait	Subsequent clock cycles after initial wait states								
0	4 wait states	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	D4	D5	D6	D7	D8	D9	D10
3		D3	D4	D5	D6	D7	D8	D9	D10	D11
4		D4	D5	D6	D7	D8	D9	D10	D11	D12
5		D5	D6	D7	1 ws	D8	D9	D10	D11	D12
6		D6	D7	1 ws	1 ws	D8	D9	D10	D11	D12
7		D7	1 ws	1 ws	1 ws	D8	D9	D10	D11	D12

Table 19 Address latency for 3 wait states

Word	Initial wait	Subsequent clock cycles after initial wait states								
0	3 wait states	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	D4	D5	D6	D7	D8	D9	D10
3		D3	D4	D5	D6	D7	D8	D9	D10	D11
4		D4	D5	D6	D7	D8	D9	D10	D11	D12
5		D5	D6	D7	D8	D9	D10	D11	D12	D13
6		D6	D7	1 ws	D8	D9	D10	D11	D12	D13
7		D7	1 ws	1 ws	D8	D9	D10	D11	D12	D13

4.2.3 Continuous burst

The device continues to output sequential burst data from the memory array, wrapping around to address 0000000h after it reaches the highest addressable memory location, until the system drives CE# high, RESET# low, or AVD# low in conjunction with a new address. See **Table 8**.

If the host system crosses a bank boundary while reading in burst mode, and the subsequent bank is not programming or erasing, an address boundary crossing latency might be required. If the host system crosses the bank boundary while the subsequent bank is programming or erasing, continuous burst halts (RDY will be disabled and data will continue to be driven).

4.2.4 8-, 16-word linear burst with wrap around

Table 20 Burst address groups

Mode	Group size	Group byte address ranges
8-word	16 bytes	0-Fh, 10-1Fh, 20-2Fh,...
16-word	32 bytes	0-1Fh, 20-3Fh, 30-4Fh,...

The remaining two modes are fixed length linear burst with wrap around, in which a fixed number of words are read from consecutive addresses. In each of these modes, the burst addresses read are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode (see **Table 20**).

As an example: if the starting address in the 8-word mode is system byte address 3Ch, the address range to be read would be byte address 30-3Fh, and the burst sequence would be 3C-3E-30-32-34-36-38-3Ah. The burst sequence begins with the starting address written to the device, wraps back to the first address in the selected group, and outputs a maximum of 8 words. No additional wait states will be required within the 8-word burst. The 8th word will continue to be driven until the burst operation is aborted (CE# goes to V_{IH}, a new address is latched in for a new burst operation, or a hardware reset). In a similar fashion, the 16-word Linear Wrap modes begin their burst sequence on the starting address written to the device, and then wrap back to the first address in the selected address group. Additional wait states could be added the first time the device crosses from one to the other group of 8 words in a 16-word burst. The number will depend on the starting address and the wait state set within the configuration register. Note that in these two burst read modes the address pointer does not cross the boundary that occurs every 128 words; thus, no 128-word address boundary crossing wait states are inserted for linear burst with wrap.

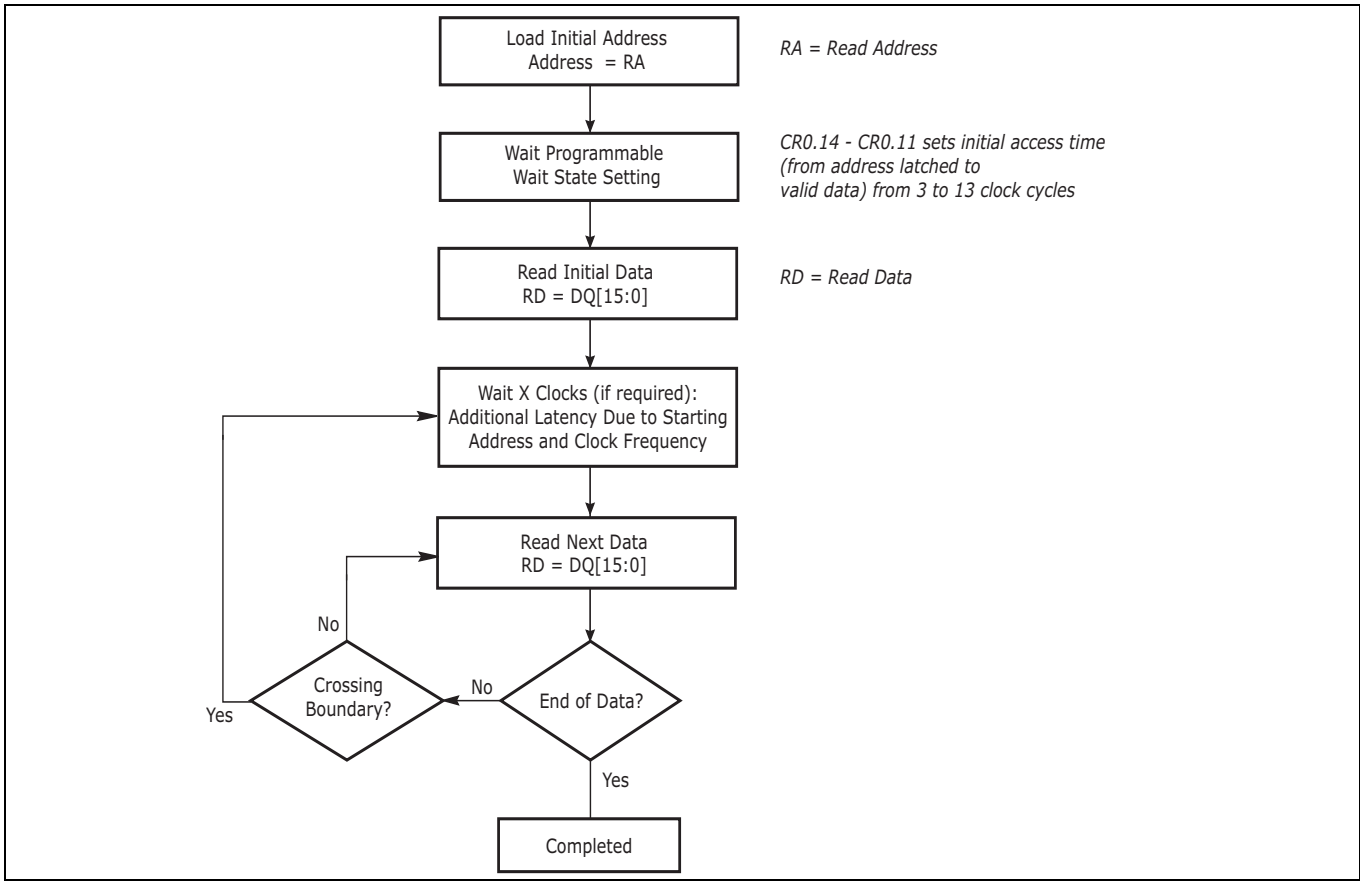


Figure 2 Synchronous read

4.2.5 Configuration Register

Configuration register (CR) sets various operational parameters associated with burst mode. Upon power-up or hardware reset, the device defaults to the idle state, and the configuration register settings are in their default state. The host system should determine the proper settings for the configuration register, and then execute the Set Configuration Register command sequence, before attempting burst operations. The Configuration Register can also be read using a command sequence (see **Table 57**). The table below describes the register settings and indicates the default state of each bit after power-on or a hardware reset. The configuration register bits are not affected by a command reset.

Table 21 Configuration Register

CR bit	Function	Settings (Binary)
CR.15	Device read mode	0 = Synchronous read mode
		1 = Asynchronous read mode (Default)
CR.14 CR.13 CR.12 CR.11	Programmable read wait states	0000 = Reserved
		0001 = Initial data is valid on the 3rd rising CLK edge after addresses are latched
		0010 = Initial data is valid on the 4th rising CLK edge after addresses are latched
		0011 = Initial data is valid on the 5th rising CLK edge after addresses are latched
		. . .
		1011 = 13th (Default)
		1100 = Reserved
		1101 = Reserved
		1110 = Reserved
		1111 = Reserved
CR.10	RDY polarity	0 = RDY signal is active low
		1 = RDY signal is active high (Default)
CR.9	Reserved	0 = Reserved
		1 = Reserved (Default)
CR.8	RDY timing	0 = RDY active one clock cycle before data
		1 = RDY active with data (Default)
CR.7	Output drive strength	0 = Full drive = Current driver strength (Default)
		1 = Half drive
CR.6	Reserved	0 = Reserved
		1 = Reserved (Default)
CR.5	Reserved	0 = Reserved (Default)
		1 = Reserved
CR.4	Reserved	0 = Reserved (Default)
		1 = Reserved
CR.3	Reserved	0 = Reserved
		1 = Reserved (Default)

Table 21 Configuration Register *(continued)*

CR bit	Function	Settings (Binary)
CR.2 CR.1 CR.0	Burst Length	000 = Continuous (Default)
		010 = 8-Word (16-Byte) linear burst with wrap around
		011 = 16-Word (32-Byte) linear burst with wrap around
		(All other bit settings are reserved)

4.2.5.1 Device read mode

Configuration Register bit 15 (CR.15) controls whether read accesses via the bus interface are in asynchronous or burst mode. Asynchronous mode is the default after power-on or hardware reset. Write accesses are always conducted with asynchronous mode timing, independent of the read mode.

4.2.5.2 Wait states

Configuration Register bits 14 to 11 (CR.[14..11]) define the number of delay cycles after the AVD# Low cycle that captures the initial address until the cycle that read data is valid. The bits from 14 to 11 are in most to least significant order. The random address access at the beginning of each read burst takes longer than the subsequent read cycles. The memory bus interface must be told how many cycles to wait before driving valid data then advancing to the next data word. The number of initial wait cycles will vary with the memory clock rate. The number of wait states is found in the wait state table information above. The minimum number of wait cycles is three. The maximum is 13. The default after power-on or hardware reset is 13 cycles.

When the appropriate number of Wait States have occurred, data is output after the rising edge of the CLK. Subsequent words are output t_{BACC} after the rising edge of each successive clock cycle, which automatically increments the internal address counter.

4.2.5.3 RDY polarity

Configuration Register bit 10 (CR.10) controls whether the RDY signal indicates valid data when High or when Low. When this bit is zero the RDY signal indicates data is valid when the signal is Low. When this bit is one the RDY signal indicates data is valid when the signal is High. The default for this bit is set to one after power-on or a hardware reset.

4.2.5.4 RDY timing

Configuration Register bit 8 (CR.8) controls whether the RDY signal indicates valid data on the same cycle that data is valid or one cycle before data is valid. When this bit is zero the RDY signal indicates data is valid in the same cycle the data is valid. When this bit is one the RDY signal indicates data is valid one cycle before data is valid. The default for this bit is set to one after power-on or a hardware reset.

4.2.5.5 Output drive strength

Configuration Register bit 7 (CR.7) controls whether the data outputs drive with full or half strength. When this bit is zero the data outputs drive with full strength. When this bit is one the data outputs drive with half strength. The default for this bit is cleared to zero after power-on or a hardware reset.

4.2.5.6 Burst length

Configuration Register bits 2 to 0 (CR.[2..0]) define the length of burst read accesses. The bits from 2 to 0 are in most to least significant order. See the register table for code meaning and default value.

4.3 Status Register

The status of program and erase operations is provided by a status register. A status register read command is written followed by a read of the status register for each access of the status register information. The Clear Status Register command will reset the status register. The status register can be read in synchronous or asynchronous mode.

Table 22 Status Register reset state [5, 6, 7, 8]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device Ready Bit. Overall status	Erase Suspend Status Bit	Erase Status Bit	Program Status Bit	RFU	Program Suspend Status Bit	Sector Lock Status Bit	Bank Status Bit
DRB 1 at Reset	ESSB 0 at Reset	ESB 0 at Reset	PSB 0 at Reset	RFU 0 at Reset	PSSB 0 at Reset	SLSB 0 at Reset	BSB 0 at Reset

Table 23 Status Register - Bit 7 [9, 10]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device Ready Bit. Overall status	Erase Suspend Status Bit	Erase Status Bit	Program Status Bit	RFU	Program Suspend Status Bit	Sector Lock Status Bit	Bank Status Bit
DRB	ESSB	ESB	PSB	RFU	PSSB	SLSB	BSB
0 Device busy programming or erasing	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	VALID
1 Device ready	VALID	VALID	VALID	VALID	VALID	VALID	VALID

Table 24 Status Register - Bit 6 [11, 12]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device Ready Bit. Overall status	Erase Suspend Status Bit	Erase Status Bit	Program Status Bit	RFU	Program Suspend Status Bit	Sector Lock Status Bit	Bank Status Bit
DRB	ESSB	ESB	PSB	RFU	PSSB	SLSB	BSB
1 Bits 6:1 only valid when Bit 7 = 1	0 No Erase in Suspension	X	X	X	X	X	X
1 Bit 6:1 only valid when Bit 7 = 1	1 Erase in Suspension	X	X	X	X	X	X

Notes
5. Status bits higher than Bit 7 are undefined.
6. Bit 7 reflects the device status.
7. If the device is busy, Bit 0 is used to check whether the addressed bank is busy or some other bank is busy.
8. All the other bits reflect the status of the device.
9. Bit 7 is set when there is no erase or program operation in progress in the device.
10. Bits 1 through 6 are valid if and only if Bit 7 is set.
11. Upon issuing the “Erase Suspend” command, the user must continue to read status until DRB becomes 1 before accessing another sector within the same bank.
12. Cleared by “Erase Resume” command.

Table 25 Status Register - Bit 5 [13, 14]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device Ready Bit. Overall status	Erase Suspend Status Bit	Erase Status Bit	Program Status Bit	RFU	Program Suspend Status Bit	Sector Lock Status Bit	Bank Status Bit
DRB	ESSB	ESB	PSB	RFU	PSSB	SLSB	BSB
1 Bits 6:1 only valid when Bit 7 = 1	X	0 Erase successful	X	X	X	X	X
1 Bit 6:1 only valid when Bit 7 = 1	X	1 Erase error	X	X	X	X	X

Table 26 Status Register - Bit 4 [14, 15]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device Ready Bit. Overall status	Erase Suspend Status Bit	Erase Status Bit	Program Status Bit	RFU	Program Suspend Status Bit	Sector Lock Status Bit	Bank Status Bit
DRB	ESSB	ESB	PSB	RFU	PSSB	SLSB	BSB
1 Bits 6:1 only valid when Bit 7 = 1	X	X	0 Program successful	X	X	X	X
1 Bit 6:1 only valid when Bit 7 = 1	X	X	1 Program fail	X	X	X	X

Table 27 Status Register - Bit 3 [14, 16]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device Ready Bit. Overall status	Erase Suspend Status Bit	Erase Status Bit	Program Status Bit	RFU	Program Suspend Status Bit	Sector Lock Status Bit	Bank Status Bit
DRB	ESSB	ESB	PSB	RFU	PSSB	SLSB	BSB
1 Bits 6:1 only valid when Bit 7 = 1	X	X	X	X	X	X	X

Notes
13. ESB bit reflects “success” or “failure” of the most recent erase operation.
14. Cleared by “Clear Status Register” command as well as by hardware reset.
15. PSB bit reflects “success” or “failure” of the most recent program operation.
16. This Register is reserved for future use.

Table 28 Status Register - Bit 2 [17, 18]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device Ready Bit. Overall status	Erase Suspend Status Bit	Erase Status Bit	Program Status Bit	RFU	Program Suspend Status Bit	Sector Lock Status Bit	Bank Status Bit
DRB	ESSB	ESB	PSB	RFU	PSSB	SLSB	BSB
1 Bits 6:1 only valid when Bit 7 = 1	X	X	X	X	0 No Program in suspension	X	X
1 Bit 6:1 only valid when Bit 7 = 1	X	X	X	X	1 Program in suspension	X	X

Table 29 Status Register - Bit 1 [19, 20, 21]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device Ready Bit. Overall status	Erase Suspend Status Bit	Erase Status Bit	Program Status Bit	RFU	Program Suspend Status Bit	Sector Lock Status Bit	Bank Status Bit
DRB	ESSB	ESB	PSB	RFU	PSSB	SLSB	BSB
1 Bits 6:1 only valid when Bit 7 = 1	X	X	X	X	X	0 Sector not locked during operation	X
1 Bit 6:1 only valid when Bit 7 = 1	X	X	X	X	X	1 Sector locked error	X

Notes
17. Upon issuing the “Program Suspend” command, the user must continue to read status until DRB becomes 1 before accessing another sector within the same bank.
18. Cleared by “Program Resume” command.
19. SLSB indicates that a program or erase operation failed to program or erase because the sector was locked or the operation was attempted on the protected Secure Silicon Region.
20. SLSB reflects the status of the most recent program or erase operation.
21. SLSB is cleared by “Clear Status Register” or by hardware reset.

Table 30 Status Register - Bit 0 [22]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device Ready Bit. Overall status	Erase Suspend Status Bit	Erase Status Bit	Program Status Bit	RFU	Program Suspend Status Bit	Sector Lock Status Bit	Bank Status Bit
DRB	ESSB	ESB	PSB	RFU	PSSB	SLSB	BSB
0 Bits 6:1 only valid when Bit 7 = 1	X	X	X	X	X	X	0 Program or Erase op. in addressed Bank
0 Bits 6:1 only valid when Bit 7 = 1	X	X	X	X	X	X	1 Program or Erase op. in other Bank
1 Bit 6:1 only valid when Bit 7 = 1	X	X	X	X	X	X	0 No active Program or Erase op.
1 Bit 6:1 only valid when Bit 7 = 1	X	X	X	X	X	X	1 invalid

4.4 Blank Check

The Blank Check command will confirm if the selected sector is erased.

The Blank Check command does not allow for reads to the array during the Blank Check. Reads to the array while this command is executing will return unknown data.

- Blank Check is only functional in Asynchronous Read mode (Configuration Register - CR [15] = 1).
- To initiate a Blank Check on Sector X, write 33h to address 555h in Sector X. while the device is in the Idle state (not during program suspend, not during erase suspend, ...).
- The Blank Check command may not be written while the device is actively programming or erasing. Blank Check does not support simultaneous operations.
- Use the Status Register read to confirm if the device is still busy and when compete if the sector is blank or not.
- Bit 5 of the Status Register will be cleared to zero if the sector is erased and set to one if not erased.
- Bit 7 and Bit 0 of the Status Register will show if the device is performing a Blank Check (similar to an erase operation).
- As soon as any bit is found to not be erased, the device will halt the operation and report the results.
- Once the Blank Check is completed, the device will to return to the Idle State.

Note
22.BSB is used to check if a program or erase operation in progress in the current bank.

4.5 Simultaneous read/write

The simultaneous read/write feature allows the host system to read data from one bank of memory while programming or erasing another bank of memory. An erase operation may also be suspended to read from or program another location within the same bank (note: programming to the sector being erased is not allowed). **Figure 18** shows how read and write cycles may be initiated for simultaneous operation with zero latency. Refer to the **"DC characteristics"** on page 44 table for read-while-program and read-while-erase current specification.

4.6 Writing commands/command sequences

The device accepts asynchronous write bus operations. During an asynchronous write bus operation, the system must drive CE# and WE# to V_{IL} and OE# to V_{IH} when providing an address and data. While an address is valid, AVD# must be driven to V_{IL}. Addresses are latched on the rising edge of AVD#, data is latched on the rising edge of WE#.

All writes to the memory are single word length and follow asynchronous timing. However, it is allowed to leave the host and memory interfaces in synchronous mode as long as the host synchronous timing for a single word synchronous write can meet the timing requirements of the memory device write cycle. Generally a synchronous write would include Clock toggling during the write but, it is also allowed for Clock to be at V_{IL} during the write.

If the device is in the synchronous read mode (CR.15 = 0), the addresses are latched on the rising edge of CLK when AVD# is at V_{IL}, while data is latched on the rising edge of WE#. If CLK is held at V_{IL}, addresses are latched on the rising edge of AVD#. CLK should not be held at V_{IH} when writing commands while the device is in Synchronous Read Mode. See the **Table 8** for the signal combinations that define each phase of a write bus operation to the device. Each write is a command or part of a command sequence to the device. The address provided in each write operation may be a bit pattern used to help identify the write as a command to the device. The upper portion of the address may also select the bank or sector in which the command operation is to be performed. A *bank address* (BA) is the set of address bits required to uniquely select a bank. Similarly, a *sector address* (SA) is the address bits required to uniquely select a sector. The data in each write identifies the command operation to be performed or supplies information needed to perform the operation. See **Table 57** for a listing of the commands accepted by the device. I_{CC2} in **"DC characteristics"** on page 44 represents the active current specification for an Embedded Algorithm operation.

4.7 Program/erase operations

- When the embedded program algorithm is complete, the device returns to the calling routing (erase suspend, SSR lock, secure silicon region, or idle state).
- The system can determine the status of the program operation by reading the Status Register. Refer to **"Status Register"** on page 25 for information on these status bits.
- A *0* cannot be programmed back to a *1*. A succeeding read shows that the data is still *0.* Only erase operations can convert a *0* to a *1*

old data	0011
new data	0101
results	0001

- Any commands written to the device during the Embedded Program Algorithm are ignored except the Program Suspend, and Status Read command. Any commands written to the device during the Embedded Erase Algorithm are ignored except Erase Suspend and Status Read command. Reading from a bank that is not programming or erasing is allowed.
- A hardware reset immediately terminates the program/erase operation and the program command sequence should be reinitiated once the device has returned to the idle state, to ensure data integrity.

4.7.1 Write Buffer Programming

Write Buffer Programming allows the system to write 1 to 64 bytes in one programming operation. The Write Buffer Programming command sequence is initiated by first writing the Write Buffer Load command written at the Sector Address + 555h in which programming occurs. Next, the system writes the number of *word locations minus 1* at the Sector Address + 2AAh. This tells the device how many write buffer addresses are loaded with data and therefore when to expect the *Program Buffer to Flash* confirm command. The Sector Address must match during the Write Buffer Load command and during the Write Word Count command and the Sector must be unlocked or the operation will abort and return to the initiating state.

The write buffer is used to program data within a 64 byte page aligned on a 64 byte boundary. Thus, a full page Write Buffer programming operation must be aligned on a page boundary. Programming operations of less than a full page may start on any word boundary but may not cross a page boundary.

The system then writes the starting address/data combination. This starting address is the first address/data pair to be programmed, and selects the *write-buffer-page* address. The Sector address must match the Write Buffer Load Sector Address or the operation will abort and return to the initiating state. All subsequent address/data pairs must be in sequential order. All write buffer addresses must be within the same page. If the system attempts to load data outside this range, the operation aborts after the Write to Buffer command is executed and the device will indicate a Program Fail in the Status Register at bit location 4 (PSB). A “Clear Status Register” must be issued to clear the PSB status bit.

The counter decrements for each data load operation.

Once the specified number of write buffer locations have been loaded, the system must then write the *Program Buffer to Flash* command at the Sector Address + 555h. The device then *goes busy*. The Embedded Program algorithm automatically programs and verifies the data for the correct data pattern. The system is not required to provide any controls or timings during these operations. If the incorrect number of write buffer locations have been loaded and the *Program Buffer to Flash* command is issued, the Status Register will indicate a program fail at bit location 4 (PSB). A “Clear Status Register” must be issued to clear the PSB status bit.

The write-buffer *embedded* programming operation can be suspended using the Program Suspend command. When the Embedded Program algorithm is complete, the device then returns to Erase Suspend, SSR Lock, Secure Silicon Region, or Idle state. The system can determine the status of the program operation by reading the Status Register. Refer to **“Status Register”** on page 25 for information on these status bits.

The Write Buffer Programming Sequence can be Aborted in the following ways:

- Load a value greater than the buffer size during the Number of Locations step.
- Write an address that is outside the Page of the Starting Address during the write buffer data loading stage of the operation.

The Write Buffer Programming Sequence can be stopped and reset by the following: Hardware Reset or Power cycle.

4.7.1.1 Software functions and sample code

Table 31 Write Buffer Program

Cycle	Description	Operation	Byte address	Word Address	Data
1	Write Buffer Load Command	Write	Sector Address + AAAh	Sector Address + 555h	0025h
2	Write Word Count	Write	Sector Address + 555h	Sector Address + 2AA	Word Count (N–1)h
Number of words (N) loaded into the write buffer can be from 1 to 32 words.					
3 to 34	Load Buffer Word N	Write	Program Address, Word N		Word N
Last	Write Buffer to Flash	Write	Sector Address + AAAh	Sector Address + 555h	0029h

The following is a C source code example of using the write buffer program function. Refer to the *Infineon Low Level Driver User's Guide* (available on **www.infineon.com**) for general information on Infineon Flash memory software development guidelines.

```
/* Example: Write Buffer Programming Command            */
/* NOTES: Write buffer programming limited to 32 words. */
/*        All addresses to be written to the flash in   */
/*        one operation must be within the same flash   */
/*        page. A flash page begins at addresses        */
/*        evenly divisible by 0x20.                     */
  UINT16 *src = source_of_data;              /* address of source data          */
  UINT16 *dst = destination_of_data;         /* flash destination address       */
  UINT16 wc   = words_to_program -1;         /* word count (minus 1)            */
*( (UINT16 *)sector_address + 0x555 )    = 0x0025;  /* write write buffer load command */
  *( (UINT16 *)sector_address + 0x2AA)    = wc;      /* write word count (minus 1)     */
do{
  *dst = *src; /* ALL dst MUST BE SAME PAGE */ /* write source data to destination */
  dst++;                                     /* increment destination pointer    */
  src++;                                     /* increment source pointer         */
  wc--;                                      /* decrement word count             */
  }while ( wc >= 0 ); /* do it again                        */

*( (UINT16 *)sector_address + 0x555)    = 0x0029;   /* write confirm command         */
  /* poll for completion */
```

Notes

23. Base = Base Address.
24. Last = Last cycle of write buffer program operation; depending on number of words written, the total number of cycles may be from 6 to 37.
25. For maximum efficiency, it is recommended that the write buffer be loaded with the highest number of words (N words) possible.

4.7.2 Program Suspend/Program Resume commands

The Program Suspend command allows the system to interrupt an embedded programming operation or a *Write to Buffer* programming operation so that data can read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the programming operation within t_{PSL} (program suspend latency) and updates the status bits. Addresses are *don't-cares* when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector and page. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend.

After the Program Resume command is written, the device reverts to programming and the status bits are updated. The system can determine the status of the program operation by reading the Status Register, just as in the standard program operation. See **"Status Register"** on page 25 for more information.

The system must write the Program Resume command to exit the Program Suspend mode and continue the programming operation. Further writes of the Program Resume command are ignored. Another Program Suspend command can be written after the device has resumed programming.

4.7.2.1 Software functions and sample code

Table 32 Program Suspend

Cycle	Operation	Byte address	Word address	Data
1	Write	Bank address	Bank address	0051h

The following is a C source code example of using the program suspend function. Refer to the *Infineon Low Level Driver User's Guide* (available on **www.infineon.com**) for general information on Infineon Flash memory software development guidelines.

```
/* Example: Program suspend command */
  *( (UINT16 *)bank_addr + 0x000 ) = 0x0051;   /* write suspend command          */
```

Table 33 Program Resume

Cycle	Operation	Byte Address	Word Address	Data
1	Write	Sector Address + 000h	Sector Address + 000h	0050h

The following is a C source code example of using the program resume function. Refer to the *Infineon Low Level Driver User's Guide* (available on **www.infineon.com**) for general information on Infineon Flash memory software development guidelines.

```
/* Example: Program resume command */
  *( (UINT16 *)sector_address + 0x000 ) = 0x0050;   /* write resume command          */
```

4.7.3 Sector Erase

The sector erase function erases one sector in the memory array (see **Table 57**). The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. After a successful sector erase, all locations within the erased sector contain FFFFh. The system is not required to provide any controls or timings during these operations. Sector Erase requires two commands. Each of the Sector Addresses must match, the lower addresses must be correct, and the sector must be unlocked previously by executing the Sector Unlock command and must not be locked by the Sector Lock Range command.

When the embedded erase algorithm is complete, the bank returns to idle state and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing banks. The system can determine the status of the erase operation by reading the Status Register. See **"Status Register"** on page 25 for information on these status bits.

Once the sector erase operation has begun, only reading from outside the erase bank, read of Status Register, and the Erase Suspend command are valid. All other commands are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the sector erase command sequence must be reinitiated once the device has returned to idle state, to ensure data integrity.

See **"Program/erase operations"** on page 29 for parameters and timing diagrams.

4.7.3.1 Software functions and sample code

Table 34 Sector Erase

Cycle	Description	Operation	Byte address	Word address	Data
1	Setup command	Write	Sector Address + AAAh	Sector Address + 555h	0080h
2	Sector Erase command	Write	Sector Address + 555h	Sector Address + 2AA	0030h

The following is a C source code example of using the sector erase function. Refer to the *Infineon Low Level Driver User's Guide* (available on **www.infineon.com**) for general information on Infineon Flash memory software development guidelines.

```
/* Example: Sector Erase Command */
*( (UINT16 *)sector_address + 0x555 ) = 0x0080;   /* write setup command           */
*( (UINT16 *)sector_address + 0x2AA)   = 0x0030;   /* write sector erase command    */
```

4.7.4 Chip Erase

The chip erase function erases the complete memory array. (See **Table 57**). The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. After a successful chip erase, all locations within the device contain FFFFh. The system is not required to provide any controls or timings during these operations. Chip Erase requires 2 commands. Each of the Sector Addresses must match, the lower addresses must be correct, and Sector 0 must be unlocked previously by executing the Sector Unlock command. If any sector has been locked by the Sector Lock Range command, the Chip Erase command will not start.

When the embedded erase algorithm is complete, the device returns to idle state and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can not read data from the device. The system can determine the status of the erase operation by reading the Status Register. See **"Status Register"** on page 25 for information on these status bits.

Once the chip erase operation has begun, only a Status Read, Hardware RESET or Power cycle are valid. All other commands are ignored. However, note that a Hardware Reset or Power Cycle immediately terminates the erase operation. If that occurs, the chip erase command sequence must be reinitiated once the device has returned to idle state, to ensure data integrity.

See **"Program/erase operations"** on page 29 for parameters and timing diagrams.

4.7.4.1 Software functions and sample code

Table 35 Chip Erase

Cycle	Description	Operation	Byte address	Word address	Data
1	Setup command	Write	Base + AAAh	Base + 555h	0080h
2	Chip Erase command	Write	Base + 555h	Base + 2AA	0010h

The following is a C source code example of using the chip erase function. Refer to the *Infineon Low Level Driver User's Guide* (available on **www.infineon.com**) for general information on Infineon Flash memory software development guidelines.

```
/* Example: Chip Erase Command */
/* Note: Cannot be suspended   */
*( (UINT16 *)base_addr + 0x555 ) = 0x0080;    /* write setup command             */
*( (UINT16 *)base_addr + 0x2AA ) = 0x0010;    /* write chip erase command        */
```

4.7.5 Erase Suspend/Erase Resume commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, the device. This command is valid only during the sector erase operation. The Erase Suspend command is ignored if written during the chip erase operation.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of t_{ESL} (erase suspend latency) to suspend the erase operation and update the status bits.

After the erase operation has been suspended, the bank enters the erase-suspend mode. The system can read data from or program data to the device. Reading at any address within erase-suspended sectors produces undetermined data. The system can read the Status Register to determine if a sector is actively erasing or is erase-suspended. Refer to **"Status Register"** on page 25 for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend mode. The system can determine the status of the program operation by reading the Status Register, just as in the standard program operation.

To resume the sector erase operation, the system must write the Erase Resume command. The device will revert to erasing and the status bits will be updated. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

4.7.5.1 Software functions and sample code

Table 36 Erase Suspend

Cycle	Operation	Byte address	Word address	Data
1	Write	Bank address	Bank address	00B0h

The following is a C source code example of using the erase suspend function. Refer to the *Infineon Low Level Driver User's Guide* (available on **www.infineon.com**) for general information on Infineon Flash memory software development guidelines.

```
/* Example: Erase suspend command */
  *( (UINT16 *)bank_addr + 0x000 ) = 0x00B0;   /* write suspend command          */
```

Table 37 Erase Resume

Cycle	Operation	Byte address	Word address	Data
1	Write	Sector Address + 000h	Sector Address + 000h	0030h

The following is a C source code example of using the erase resume function. Refer to the *Infineon Low Level Driver User's Guide* (available on **www.infineon.com**) for general information on Infineon Flash memory software development guidelines.

```
/* Example: Erase resume command */
  *( (UINT16 *)sector_address + 0x000 ) = 0x0030;   /* write resume command          */
   /* The flash needs adequate time in the resume state */
```

4.7.6 Accelerated program/sector erase

Accelerated write buffer programming, and sector erase operations are enabled through the V_{PP} function. This method is faster than the standard chip program and sector erase command sequences.

The accelerated write buffer program and sector erase functions must not be used more than 50 times per sector. In addition, accelerated write buffer program and sector erase should be performed at room temperature (30°C ±10°C).

If the system asserts V_{HH} on V_{PP}, the device automatically uses the higher voltage on the input to reduce the time required for program and erase operations. Removing V_{HH} from the V_{PP} input, upon completion of the embedded program or erase operation, returns the device to normal operation.

- Simultaneous operations are not supported while V_{PP} is at V_{HH}. The V_{PP} pin must not be at V_{HH} for operations other than accelerated write buffer programming, accelerated sector erase, and status register read or device damage may result.
- The V_{PP} pin must not be left floating or unconnected; inconsistent behavior of the device may result.
- There is a minimum of 100 ms required between accelerated write buffer programming and a subsequent accelerated sector erase.

4.8 Handshaking

The handshaking feature allows the host system to detect when data is ready to be read by simply monitoring the RDY (Ready) pin, which is a dedicated output controlled by CE#.

When CE# input is Low, the RDY output signal is actively driven. When both of the CE# inputs are High the RDY output is high-impedance. When CE# input and OE# input is Low, the A/DQ15-A/DQ0 output signals are actively driven. When both of the CE# inputs are High, or the OE# input is High, the A/DQ15-A/DQ0 outputs are high-impedance.

When the device is operated in synchronous mode, and OE# is low (active), the initial word of burst data becomes available after the rising edge of the RDY. CR.8 in the Configuration Register allows the host to specify whether RDY is active at the same time that data is ready, or one cycle before data is ready (see **Table 21**).

When the device is operated in asynchronous mode, RDY will be high when CE# is low (active).

4.9 Hardware reset

The RESET# input provides a hardware method of resetting the device to idle state. When RESET# is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, resets the configuration register, and ignores all read/write commands for the duration of the reset operation. The device also resets the internal state machine to idle state. Hardware Reset clears the AADM upper address register to zero.

To ensure data integrity the operation that was interrupted should be reinitiated once the device is ready to accept another command sequence.

When RESET# is held at V_{SS}, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL}, but not at V_{SS}, the standby current is greater.

See **Figure 14** for timing diagrams.

4.10 Software reset

Software reset is part of the command set (see **Table 57**) that also returns the device to idle state and must be used for the following conditions:

1. Exit ID/CFI mode
2. Exit Secure Silicon Region mode
3. Exit Configuration Register mode
4. Exit SSR Lock mode

Reset commands are ignored once programming/erasure has begun until the operation is complete.

4.10.1 Software functions and sample code

Table 38 Reset

Cycle	Operation	Byte address	Word address	Data
Reset command	Write	Base + xxxh	Base + xxxh	00F0h

Note

Base = Base address.

The following is a C source code example of using the reset function. Refer to the *Infineon Low Level Driver User's Guide* (available on **www.infineon.com**) for general information on Infineon Flash memory software development guidelines.

```
/* Example: Reset (software reset of Flash state machine) */
  *( (UINT16 *)base_addr + 0x000 ) = 0x00F0;
```

5 Sector protection/unprotection

The sector protection/unprotection feature disables or enables programming or erase operations in one or multiple sectors and can be implemented through software and/or hardware methods, which are independent of each other. This section describes the various methods of protecting data stored in the memory array.

5.1 Sector Lock/Unlock command

The Sector Lock/Unlock command sequence allows the system to protect all sectors from accidental writes or, unprotect one sector to allow programming or erasing of the sector. When the device is first powered up, all sectors are unlocked. To lock all sectors (enter protected mode), a Sector Lock/Unlock command must be issued to any Sector Address. Once this command is issued, only one sector at a time can be unlocked until power is cycled. To unlock a sector, the system must write the Sector Lock/Unlock command sequence. Two cycles are first written: addresses are x555h and x2AAh, and data is 60h. During the third cycle, the sector address (SLA) and unlock command (60h) are written, while specifying with address A6 whether that sector should be locked (A6 = V_{IL}) or unlocked (A6 = V_{IH}).

A Program or Erase operation will check the unlocked Sector Address only at the beginning of the Program or Erase operation. It is not necessary to keep the sector being Programmed or Erased unlocked during the operation. The system can change the unlocked Sector after programming or erasing the sector has begun. An Erase Resume or Program Resume command does not check the value of the unlocked Sector.

If A6 is set to V_{IL},then all sectors in the array will be locked. Only one sector at a time can be unlocked.

If a Sector Lock/Unlock command is issued to a sector that is protected by the Sector Lock Range command, all sectors in the part will be locked.

5.2 Sector Lock Range command

This command allows a range of sectors to be protected from program or erase (locked) until a hardware reset or power is removed from the device. Once this command is issued, all sectors are protected and the Sector Lock/Unlock command is ignored for the selected range of sectors. Sectors outside of the selected range must be unlocked one sector at a time using the Sector Unlock command in order to be erased/programmed.

Two cycles are first written: addresses are x555h and x2AAh, and data is 60h. During the third cycle, the sector address (SLA) and load sector address command (61h) is written. This cycle sets the lower sector address of the range. During the fourth cycle, the sector address (SLA) and load sector address command (61h) is written. This cycle sets the upper sector address of the range. The addresses reference a large sector address range (128 KB). If a sector address matches the location of the four small sectors, all of the small sectors will be protected as a group. The sectors selected by the lower and upper address, as well as all sectors between these sectors, are protected from program and erase until a hardware reset or power is removed. If the lower and upper sector addresses are for the same sector then only that one sector is locked. Flash address input A6 (system byte address bit a7) during both address cycles must be zero (A6 = V_{IL}) for the addresses to be accepted as valid.

If the first sector address cycle contains an address which is higher than the second sector address cycle, then the command sequence will be invalid. If A6 is set to one (A6 = V_{IH}) on either address cycle, the command sequence will disable subsequent Sector Lock Range commands.

A valid Sector Lock Range command sequence is accepted only once after a Hardware Reset or initial power up. Additional Sector Lock Range commands will be ignored.

If a Sector Unlock command tries to unlock a Sector within the Sector Lock Range, the Sector will remain in locked state. Similarly, if a Sector that is currently unlocked by the Sector Unlock command is overlapped by a subsequent Sector Lock Range, that sector will be locked and program erase operations to that region will be ignored.

This command is generally used by trusted boot code. After power on reset boot code has the option to check for any need to update sectors before locking them for the remainder of power on time. Once boot code is satisfied with the content of sectors to be protected the Sector Lock Range command is used to lock sectors against any program or erase during normal system operation. This adds an extra layer of protection for critical data that must be protected against accidental or malicious corruption. Yet, maintains flexibility for trusted boot code to perform occasional updates of the data. It is important to issue the Sector Lock Range command even if no sectors are to be protected so that sectors that should remain available for update cannot be later locked by accidental or malicious code behavior.

5.3 Hardware data protection methods

There are additional hardware methods by which intended or accidental erasure of any sectors can be prevented via hardware means. The following subsections describes these methods:

5.3.1 V_{PP} method

Once V_{PP} input is set to V_{IL}, all program and erase functions are disabled and hence all Sectors (including the Secure Silicon Region) are protected.

5.3.2 Low V_{CC} write inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down.

The command register and all internal program/erase circuits are disabled. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

5.3.3 Write pulse glitch protection

Noise pulses of less than 3 ns (typical) on OE#, WE#, or CE# do not initiate a write cycle.

5.3.4 Power-up write inhibit

If CE# = RESET# = V_{IL} and OE# = V_{IH} during power up, the device does not accept write commands. The internal state machine is automatically reset to the idle state on power-up.

5.4 SSR Lock

The SSR Lock consists of two bits. The customer secure silicon region protection bit is bit 0. The factory secure silicon region protection bit is bit 1. All other bits in this register return “1.” If the customer secure silicon region protection bit is set to “0,” the customer secure silicon region is protected and can not be programmed. If this bit is set to “1,” the customer secure silicon region is available for programming. Once this area has been programmed, the SSR Lock bit 0 should be programmed to “0.”

5.5 Secure silicon region

The secure silicon region provides an extra flash memory region that may be programmed once and permanently protected from further programming or erase.

- Reads can be performed in the asynchronous or synchronous mode.
- Sector address supplied during the Secure Silicon Entry command selects the flash memory array sector that is overlaid by the secure silicon region address map.
- Continuous burst mode reads within secure silicon region wrap from address FFh back to address 00h.
- Reads outside of the overlaid sector return memory array data.
- The secure silicon region is not accessible when the device is executing an embedded algorithm (nor during Program Suspend, Erase Suspend, or while another AOS is active).
- See the secure silicon address map for address range of this area.

5.5.1 Factory secure silicon region

The factory secure silicon region is always protected when shipped from the factory and has the factory SSR Lock Bit (bit 1) permanently set to a zero. This prevents cloning of a factory locked part and ensures the security of the ESN and customer code once the product is shipped to the field.

5.5.2 Customer secure silicon region

The customer secure silicon region is typically shipped unprotected, Customer SSR Lock Bit (bit 0) set to a one, allowing customers to utilize that sector in any manner they choose.

- The customer secure silicon region can be read any number of times, but each word CL can be programmed only once and the region locked only once. The customer secure silicon region lock must be used with caution as once locked, there is no procedure available for unlocking the customer secure silicon region area and none of the bits in the customer secure silicon region memory space can be modified in any way. The customer indicator bit is located in the SSR Lock at bit location 0.
- Once the Customer Secure Silicon Region area is protected, any further attempts to program in the area will fail with status indicating the area being programmed is protected.

5.5.3 Secure Silicon Region Entry and Exit command sequences

The system can access the secure silicon region region by issuing the one-cycle Enter Secure Silicon Region Entry command sequence from the IDLE State. The device continues to have access to the secure silicon region region until the system issues the Exit Secure Silicon Region command sequence, performs a Hardware RESET, or until power is removed from the device.

See **Table 57** for Secure Silicon Region command definitions for address and data requirements for both command sequences.

The Secure Silicon Region Entry command allows the following commands to be executed:

- Read customer and factory secure silicon regions
- Program the customer secure silicon region
- Read data out of all sectors not re-mapped to secure silicon region
- Secure Silicon Region Exit

5.5.3.1 Software functions and sample code

The following are C functions and source code examples of using the Secured Silicon Sector Entry, Program, and Exit commands. Refer to the *Infineon Low Level Driver User's Guide* (available on **www.infineon.com**) for general information on Infineon Flash memory software development guidelines.

Table 39 Secured Silicon Region Entry

Cycle	Operation	Byte address	Word address	Data
Entry Cycle	Write	Sector Address + AAAh	Sector Address + 555h	0088h

```
/* Example: SecSi Sector Entry Command */
*( (UINT16 *)sector_address + 0x555 ) = 0x0088;   /* write Secsi Sector Entry Cmd    */
```

Table 40 Secured silicon region program

Cycle	Operation	Byte address	Word address	Data
Program Setup	Write	Sector Address + AAAh	Sector Address + 555h	0025h
Write Word Count	Write	Sector Address + 555h	Sector Address + 2AA	Word Count (N–1)h
Number of words (N) loaded into the write buffer can be from 1 to 32 words.				
Load Buffer Word N	Write	Program Address, Word N		Word N
Write Buffer to Flash	Write	Sector Address + AAAh	Sector Address + 555h	0029h

```
/* Once in the SecSi Sector mode, you program */
/* words using the programming algorithm.     */
```

Table 41 Secured Silicon Region Exit

Cycle	Operation	Byte address	Word address	Data
Exit Cycle	Write	Base address	Base address	00F0h

```
/* Example: SecSi Sector Exit Command */
*( (UINT16 *)base_addr + 0x000 ) = 0x00F0;   /* write SecSi Sector Exit cycle */
```

6 Power conservation modes

6.1 Standby mode

In the standby mode current consumption is greatly reduced, and the outputs (A/DQ15-A/DQ0) are placed in the high impedance state, independent of the OE# input. The device enters the CMOS standby mode when the CE# and RESET# inputs are both held at $V_{CC} \pm 0.2$ V. The device requires standard access time (t_{CE} or t_{IA}) for read access, before it is ready to read data. If the device is deselected during erasure or programming, the device draws active current until the operation is completed. I_{CC3} in **"DC characteristics"** on page 44 represents the standby current specification

6.2 Automatic sleep mode

The automatic sleep mode minimizes Flash device energy consumption while in asynchronous mode and while the device is not in a suspended state. The device automatically enables this mode when addresses remain stable for t_{ACC} + 20 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings (t_{ACC} or t_{PACC}) provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. While in synchronous mode, the automatic sleep mode is disabled. I_{CC6} in **"DC characteristics"** on page 44 represents the automatic sleep mode current specification.

6.3 Output Disable (OE#)

When the OE# input is at V_{IH}, output (A/DQ15-A/DQ0) from the device is disabled and placed in the high impedance state. RDY is not controlled by OE#.

7 Electrical specifications

7.1 Absolute maximum ratings

Table 42 Absolute maximum ratings

Parameter	Value
Storage temperature plastic packages	–65°C to +150°C
Ambient temperature with power applied	–65°C to +125°C
Voltage with respect to ground: All Inputs and I/Os except as noted below [26]	–0.5 V to VIO + 0.5 V
V_{CC} [26]	–0.5 V to +2.5 V
V_{IO}	–0.5 V to +2.5 V
V_{PP} [27]	–0.5 V to +9.5 V
Output short circuit current [28]	100 mA

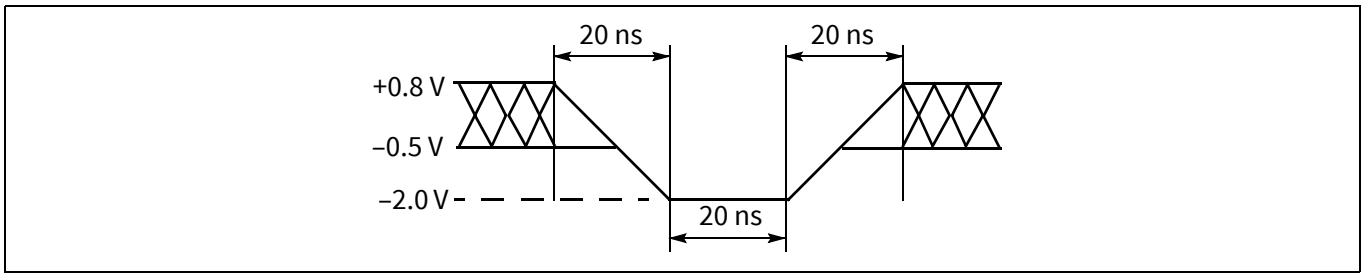


Figure 3 Maximum negative overshoot waveform

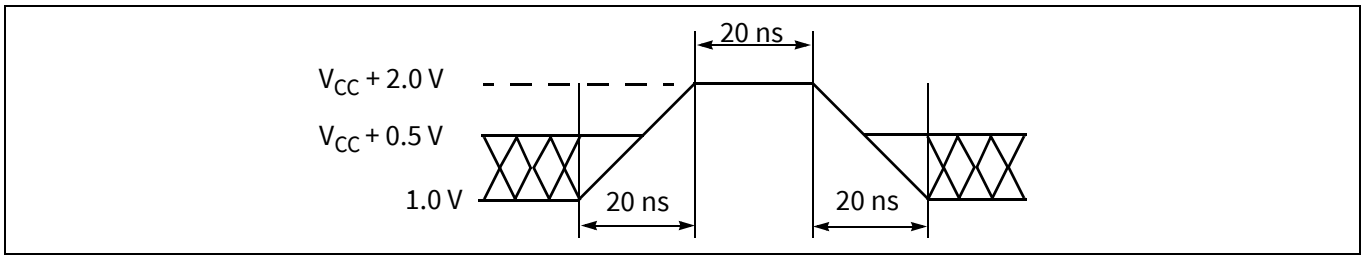


Figure 4 Maximum positive overshoot waveform

Notes

26. Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, inputs or I/Os may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See **Figure 3**. Maximum DC voltage on input or I/Os is V_{CC} + 0.5 V. During voltage transitions outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See **Figure 4**.
27. Minimum DC input voltage on pin V_{PP} is -0.5V. During voltage transitions, V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See **Figure 3**. Maximum DC voltage on pin V_{PP} is +9.5 V, which may overshoot to 10.5 V for periods up to 20 ns.
28. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
29. Stresses above those listed under "**Absolute maximum ratings**" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Operating ranges

Table 43 Operating ranges

Parameter	Operating ranges [30]
Wireless (W) devices	
Ambient temperature (T_A)	–25°C to +85°C
Industrial (I) devices	
Ambient temperature (T_A) (Refer to publication number S29VS_XS-R_SP for industrial temperature specific differences)	–40°C to +85°C
Supply voltages	
V_{CC} supply voltages	+1.70 V to +1.95 V
V_{IO} supply voltages	+1.70 V to +1.95 V
	$V_{CC(min)} \geq V_{IO(min)}$ - 200 mV

7.3 DC characteristics

7.3.1 CMOS compatible

Table 44 CMOS compatible

Parameter	Description	Test conditions [31, 32]		Min	Typ	Max	Unit
I_{LI}	Input load current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$max				±1	µA
I_{LO}	Output leakage current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$max				±1	µA
I_{CCB}	V_{CC} active burst read current	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 8	83 MHz		35	38	mA
			104 MHz 108 MHz		39	44	mA
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 16	83 MHz		28	30	mA
			104 MHz 108 MHz		32	36	mA
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = Continuous	83 MHz		28	30	mA
			104 MHz 108 MHz		32	36	mA
I_{IO1}	V_{IO} non-active output	OE# = V_{IH}, RDY = Tri-state			20	30	µA
I_{IO2}	V_{IO} standby	CE# = RESET# = V_{CC} ± 0.2V			2	3	µA
I_{CC1}	V_{CC} active asynchronous read current	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}	10 MHz		40	60	mA
			5 MHz		20	40	mA
			1 MHz		10	20	mA
I_{CC2}	V_{CC} active write current [33, 34]	CE# = V_{IL}, OE# = V_{IH}, $V_{PP} = V_{IH}$	V_{PP}		1	5	µA
			V_{CC}		30	40	mA

Notes
30. Operating ranges define those limits between which the functionality of the device is guaranteed.
31. Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.
32. $V_{CC} = V_{IO}$
33. I_{CC} active while embedded erase or embedded program is in progress.
34. Effect of status register polling during write not included.

Table 44 CMOS compatible *(continued)*

Parameter	Description	Test conditions [31, 32]		Min	Typ	Max	Unit
I_{CC3}	V_{CC} standby current	CE# = RESET# = V_{CC} ± 0.2 V	V_{PP}		1	5	µA
			V_{CC}		30	40	µA
I_{CC4}	V_{CC} reset current	RESET# = V_{IL}, CLK = V_{IL}			150	250	µA
I_{CC5}	V_{CC} active current (Read while write) (Continuous burst) [35]	CE# = V_{IL}, OE# = V_{IH}, V_{PP} = V_{IH}	83 MHz		65	70	mA
			104 MHz 108 MHz		71	76	
I_{CC6}	V_{CC} sleep current [36]	CE# = V_{IL}, OE# = V_{IH}			20	40	µA
I_{PP}	Accelerated program current [37]	CE# = V_{IL}, OE# = V_{IH}, V_{PP} = 9.5 V	V_{PP}		7	10	mA
			V_{CC}		25	28	mA
V_{IL}	Input low voltage	V_{IO} = 1.8 V		–0.2		0.4	V
V_{IH}	Input high voltage	V_{IO} = 1.8 V		V_{IO} – 0.4		V_{IO} + 0.4	
V_{OL}	Output low voltage	I_{OL} = 100 µA, V_{CC} = $V_{CC\ min}$ = V_{IO}				0.1	V
V_{OH}	Output high voltage	I_{OH} = –100 µA, V_{CC} = $V_{CC\ min}$ = V_{IO}		V_{IO} – 0.1			V
V_{HH}	Voltage for accelerated program			8.5		9.5	V
V_{LKO}	Low V_{CC} lock-out voltage			1.0		1.1	V

7.4 Capacitance

Table 45 Capacitance

Symbol	Description	Test conditions [38, 39]		Min.	Typ.	Max.	Unit
C_{IN}	Input capacitance (Address, CE#, OE#, WE#, AVD#, WE#, CLK, RESET#)	V_{IN} = 0	Single die	2.0	4.5	6.0	pF
			Dual die	4.0	9.0	12.0	pF
C_{OUT}	Output capacitance (DQ, RDY)	V_{OUT} = 0	Single die	2.0	4.5	6.0	pF
			Dual die	4.0	9.0	12.0	pF

Notes
35. I_{CC5} applies while reading the status register during program and erase operations.
36. Device enters automatic sleep mode when addresses are stable for t_{ACC} + 20 ns. Typical sleep mode current is equal to I_{CC3}.
37. Total current during accelerated programming is the sum of V_{PP} and V_{CC} currents.
38. Test conditions T_A = 25°C, f = 1.0 MHz
39. Sampled, not 100% tested.

7.5 AC test conditions

Table 46 AC test conditions

Parameter		Operating range
Input level		0.0 to V_{IO}
Input comparison level		$V_{IO}/2$
Output data comparison level		$V_{IO}/2$
Load capacitance (C_L)		30 pF
Transition time (t_T) (input rise and fall times)	83 MHz	2.50 ns
	104 MHz	1.85 ns
	108 MHz	1.85 ns
Transition time (t_T) (CLK input rise and fall times)	83 MHz	2.50 ns
	104 MHz	1.85 ns
	108 MHz	1.85 ns

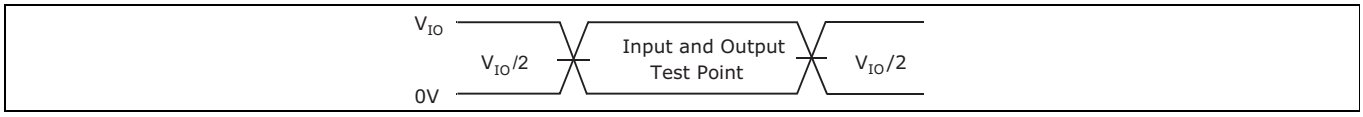


Figure 5 Input pulse and test point

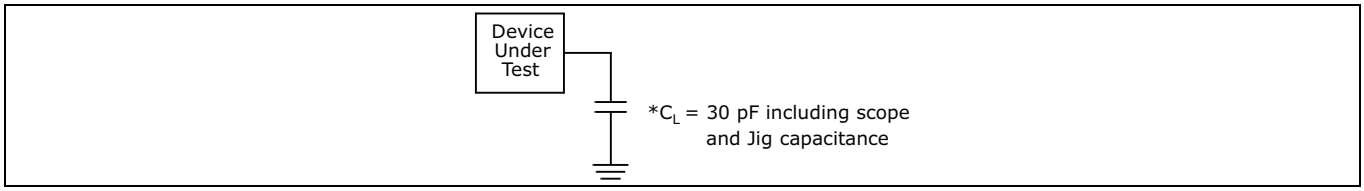
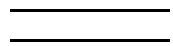
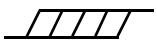
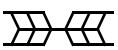


Figure 6 Output load

7.6 Key to switching waveforms

Table 47 Waveforms

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't care, any change permitted	Changing, state unknown
	Does not apply	Center line is high impedance state (High-Z)

7.7 V_{CC} power-up and power down

During power-up or power-down, V_{CC} must always be greater than or equal to V_{IO} ($V_{CC} \geq V_{IO}$).

The device ignores all inputs until a time delay of t_{VCS} has elapsed after the moment that V_{CC} and V_{IO} both rise above, and stay above the minimum V_{CC} and V_{IO} thresholds. During t_{VCS}, the device is performing power-on reset operations.

During power-down or voltage drops below V_{CC} Lockout maximum (V_{LKO}), the V_{CC} and V_{IO} voltages must drop below V_{CC} Reset (V_{RST}) minimum for a period of t_{PD} for the part to initialize correctly when V_{CC} and V_{IO} again rise to their operating ranges. If during a voltage drop the V_{CC} stays above V_{LKO} maximum, the part will stay initialized and will work correctly when V_{CC} is again above V_{CC} minimum. If the part locks up from improper initialization, a hardware reset can be used to initialize the part correctly.

Normal precautions must be ensured for supply decoupling to stabilize the V_{CC} and V_{IO} power supplies. Each device in a system should have the V_{CC} and V_{IO} power supplies decoupled by a suitable capacitor close to the package connections (this capacitor is generally in the order of 0.1 µF). At no time should V_{IO} be greater then 200 mV above V_{CC} ($V_{CC} \geq V_{IO}$ - 200 mV).

Table 48 Power-up and power down [40, 41, 42, 43]

Parameter	Description	Test setup	Value	Unit
t_{VCS}	V_{CC} setup time [44]	Min	300	µs
t_{VIOS}	V_{IO} setup time	Min	300	µs
t_{RH}	Time between RESET# (high) and CE# (low)	Min	200	ns
V_{RST}	V_{CC} and V_{IO} Low voltage needed to ensure initialization will occur	Min	0.7	V
t_{PD}	Duration of $V_{CC} \leq V_{RST\ (min)}$ [44]	Min	10	µs

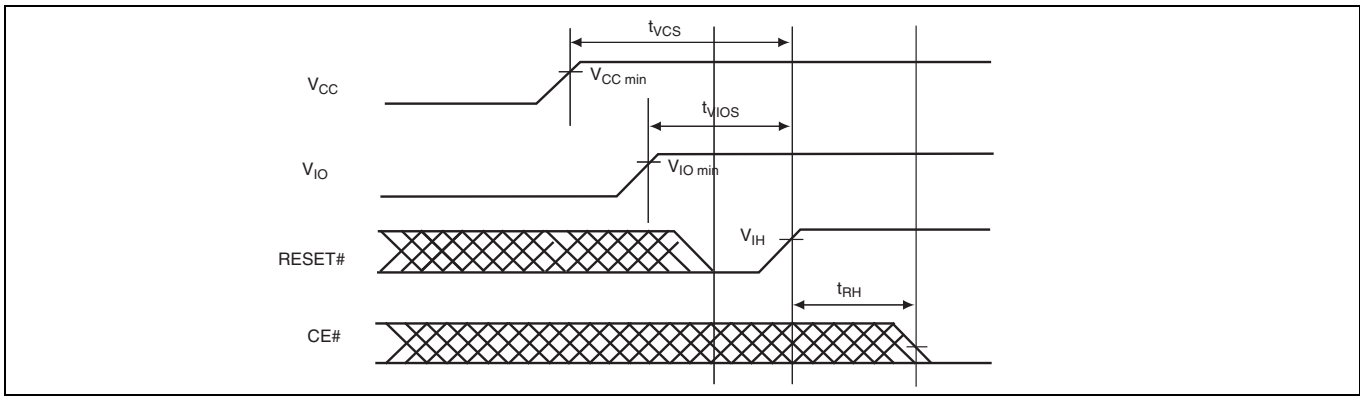


Figure 7 V_{CC} power-up diagram

Notes
40.RESET# must be high after V_{CC} and V_{IO} are higher than V_{CC} minimum.
41.$V_{CC} \geq V_{IO}$ – 200 mV during power-up.
42.V_{CC} and V_{IO} ramp rate could be non-linear.
43.V_{CC} and V_{IO} are recommended to be ramped up simultaneously.
44.Not 100% tested.

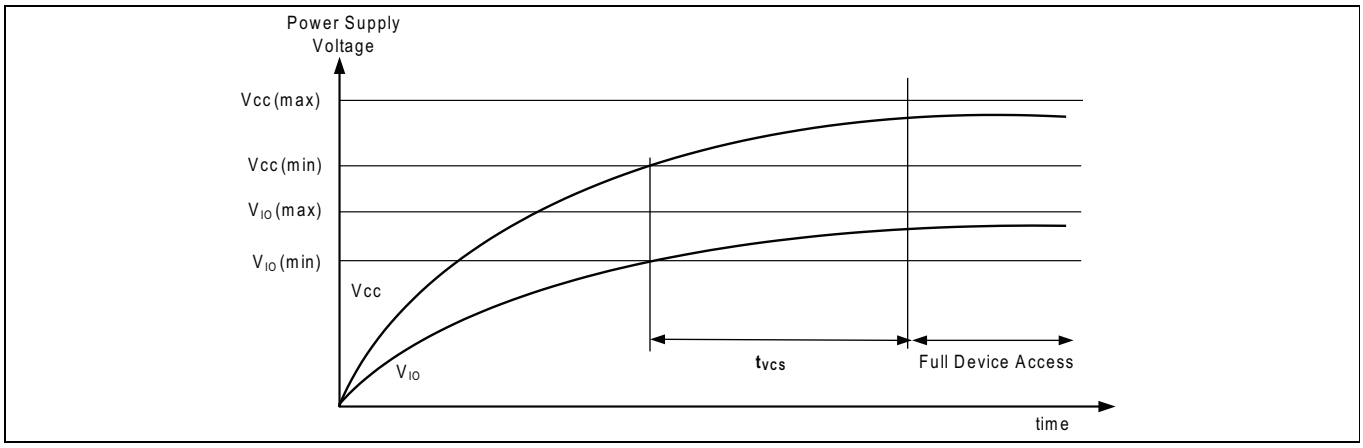


Figure 8 Power-up

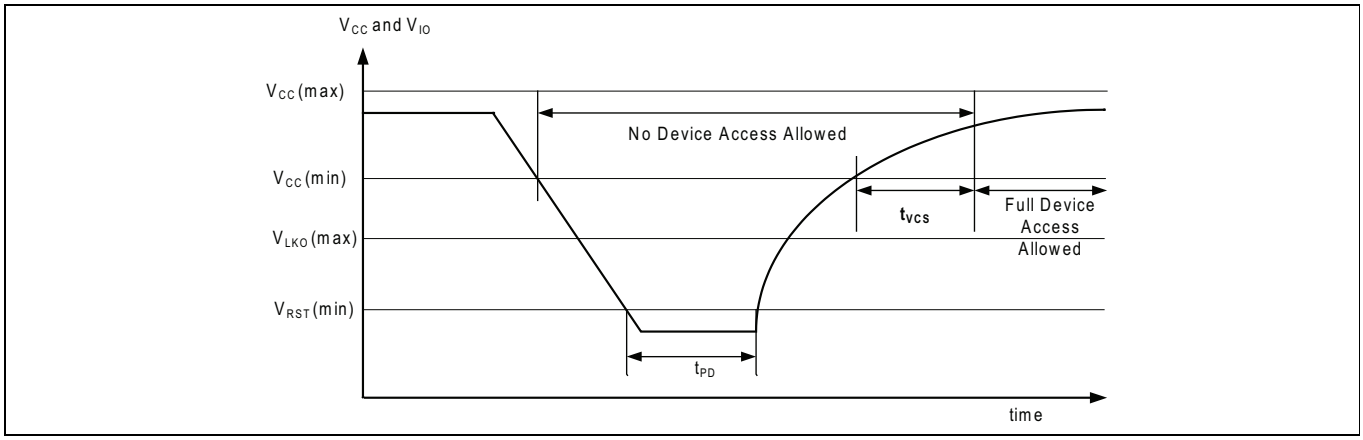


Figure 9 V_{CC} power-down and voltage drop

7.8 CLK characterization

Table 49 CLK characterization

Parameter	Description		108 MHz	Unit
f_{CLK}	CLK frequency	Max	108	MHz
		Min	DC [45]	
t_{CLK}	CLK period	Min	9.26	ns
t_{CL}/t_{CH}	CLK low/high time	Min	0.40 t_{CLK}	ns

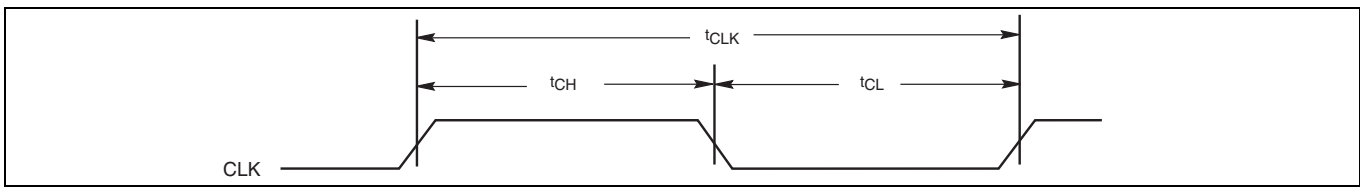


Figure 10 CLK characterization

Note
45. DC for operations other than continuous and 16 word (32-byte) synchronous burst read. See **"AC characteristics"** on page 49 table.

7.9 AC characteristics

7.9.1 AC characteristics–Synchronous burst read

Table 50 AC characteristics–Synchronous burst read

Parameter [46]	Symbol		83 MHz	104 MHz	108 MHz	Unit
Clock frequency	CLK	Min	DC (0) for operations other than continuous and 32 byte synchronous burst. 120 in 32 byte burst 1000 in continuous burst			KHz
Clock cycle	t_{CLK}	Min	12	9.6	9.26	ns
CLK rise time	t_{CLKR}	Max	2.5	1.92	1.852	ns
CLK fall time	t_{CLKF}					
CLK high or low time	$t_{CLKH/L}$	Min	5	4	3.86	ns
Internal access time	t_{IA}	Max	75		72.34	ns
Burst access time valid clock to output delay	t_{BACC}	Max	9	7.6	6.75	ns
AVD# setup time to CLK	t_{AVDS}	Min	4		3.38	ns
AVD# hold time from CLK	t_{AVDH}	Min	3		2.89	ns
Address setup time to CLK	t_{ACS}	Min	4		2.89	ns
Address hold time from CLK	t_{ACH}	Min	5		4.82	ns
Data hold time from next clock cycle	t_{BDH}	Min	3	2	2	ns
Output enable to data	t_{OE}	Max	15			ns
CE# disable to output High-Z [47]	t_{CEZ}	Max	10			ns
OE# disable to output High-Z [47]	t_{OEZ}	Max	10			ns
CE# setup time to CLK	t_{CES}	Min	4		3.38	ns
CLK to RDY valid	t_{RACC}	Max	9	7.6	6.75	ns
CE# low to RDY valid	t_{CR}	Max	10			ns
AVD# pulse width	t_{AVDP}	Min	6			ns

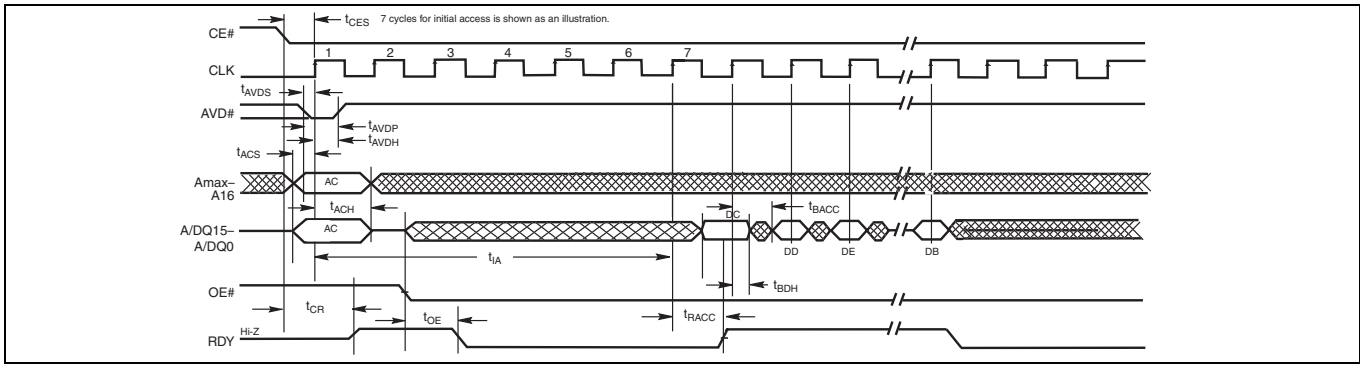


Figure 11 Synchronous read mode - ADM interface

Notes

46.Not 100% tested.

47.If OE# is disabled before CE# is disabled, the output goes to High-Z by t_{OEZ}.
If CE# is disabled before OE# is disabled, the output goes to High-Z by t_{CEZ}.
If CE# and OE# are disabled at the same time, the output goes to High-Z by t_{OEZ}.

48.AVD cannot be low for two subsequent CLK cycles.

7.9.2 AC characteristics–Asynchronous read

Table 51 AC characteristics–Asynchronous read

Parameter	Symbol	Min	Max	Unit
Access time from CE# low	t_{CE}	–	80	ns
Asynchronous access time from address valid	t_{ACC}	–	80	
Read cycle time	t_{RC}	80	–	
AVD# low time	t_{AVDP}	6	–	
Address setup to rising edge of AVD#	t_{AAVDS}	4	–	
Address hold from rising edge of AVD#	t_{AAVDH}	3.5	–	
Output enable to output valid	t_{OE}	–	15	
CE# setup to AVD# falling edge	t_{CAS}	0	–	
CE# disable to output and RDY High-Z [49]	t_{CEZ}	–	10	
OE# disable to output High-Z [49]	t_{OEZ}	–	10	
AVD# High to OE# Low	t_{AVDO}	4	–	
CE# low to RDY valid	t_{CR}	–	10	
WE# disable to AVD# enable	t_{WEA}	9.6	–	
WE# disable to OE# enable	t_{OEH}	4	–	

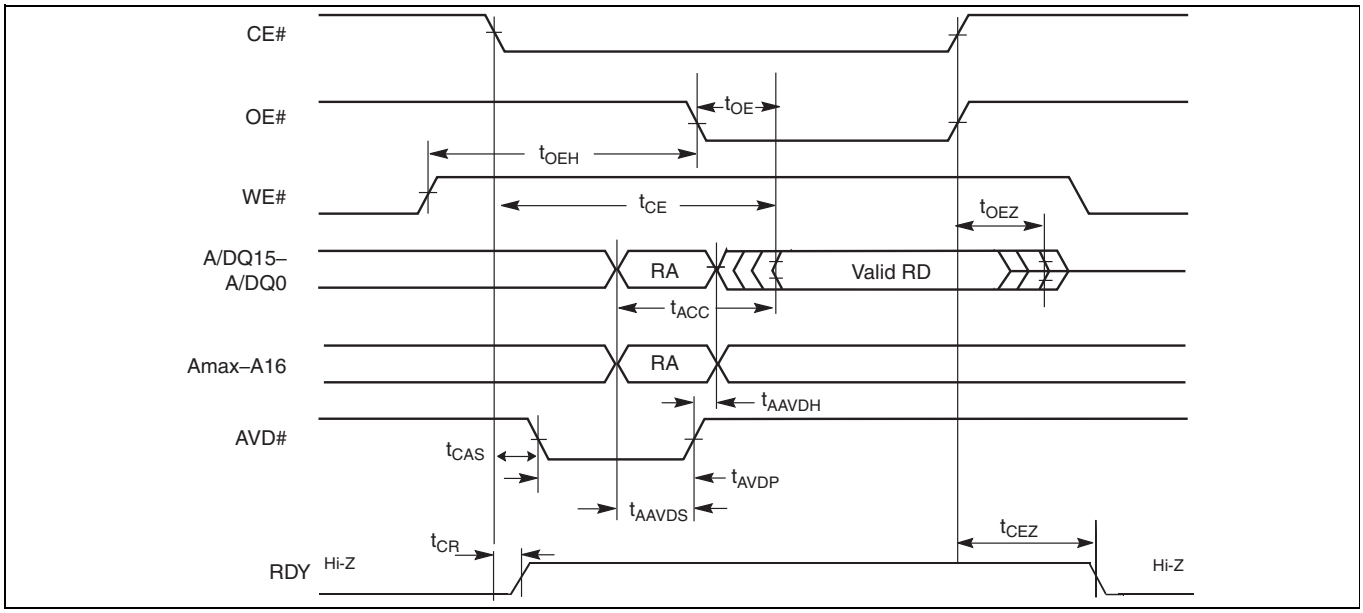


Figure 12 Asynchronous mode read - ADM interface [51, 52]

Notes

49. Not 100% tested.
50. If OE# is disabled before CE# is disabled, the output goes to High-Z by t_{OEZ}.
    If CE# is disabled before OE# is disabled, the output goes to High-Z by t_{CEZ}.
    If CE# and OE# are disabled at the same time, the output goes to High-Z by t_{OEZ}.
51. AVD# Transition occurs after CE# is driven to low and valid address transition occurs before AVD# is driven to Low.
52. VA = Valid read address, RD = Read data.If CE# and OE# are disabled at the same time, the output goes to High-Z by t_{OEZ}.

7.9.3 AC characteristics–Erase/program timing

Table 52 AC characteristics–Erase/program timing

Parameter	Symbol	Min	Typ	Max	Unit
WE# cycle time [53]	t_{WC}	60	–	–	ns
AVD# low pulse width	t_{AVDP}	6	–	–	ns
Address setup to rising edge of AVD#	t_{AAVDS}	4	–	–	ns
Address hold from rising edge of AVD#	t_{AAVDH}	3.5	–	–	ns
Read recovery time before write	t_{GHWL}	0	–	–	ns
Data setup to rising edge of WE#	t_{DS}	20	–	–	ns
Data hold from rising edge of WE#	t_{DH}	0	–	–	ns
CE# setup to falling edge of WE#	t_{CS}	4	–	–	ns
CE# hold from rising edge of WE#	t_{CH}	0	–	–	ns
WE# pulse width	t_{WP}	25	–	–	ns
WE# pulse width high	t_{WPH}	20	–	–	ns
Latency between read and write operations	t_{SRW}	0	–	–	ns
AVD# disable to WE# disable	t_{VLWH}	23.5	–	–	ns
WE# disable to AVD# enable	t_{WEA}	9.6	–	–	ns
CE# low to RDY valid	t_{CR}	–	–	10	ns
CE# disable to output High-Z	t_{CEZ}	–	–	10	ns
OE# disable to WE# enable	t_{WEH}	4	–	–	ns
Erase suspend latency	t_{ESL}	–	–	30	µs
Program suspend latency	t_{PSL}	–	–	30	µs
Erase resume to erases suspend	t_{ERS}	30	–	–	µs
Program resume to program suspend	t_{PRS}	30	–	–	µs

Note
53.Sampled, not 100% tested.

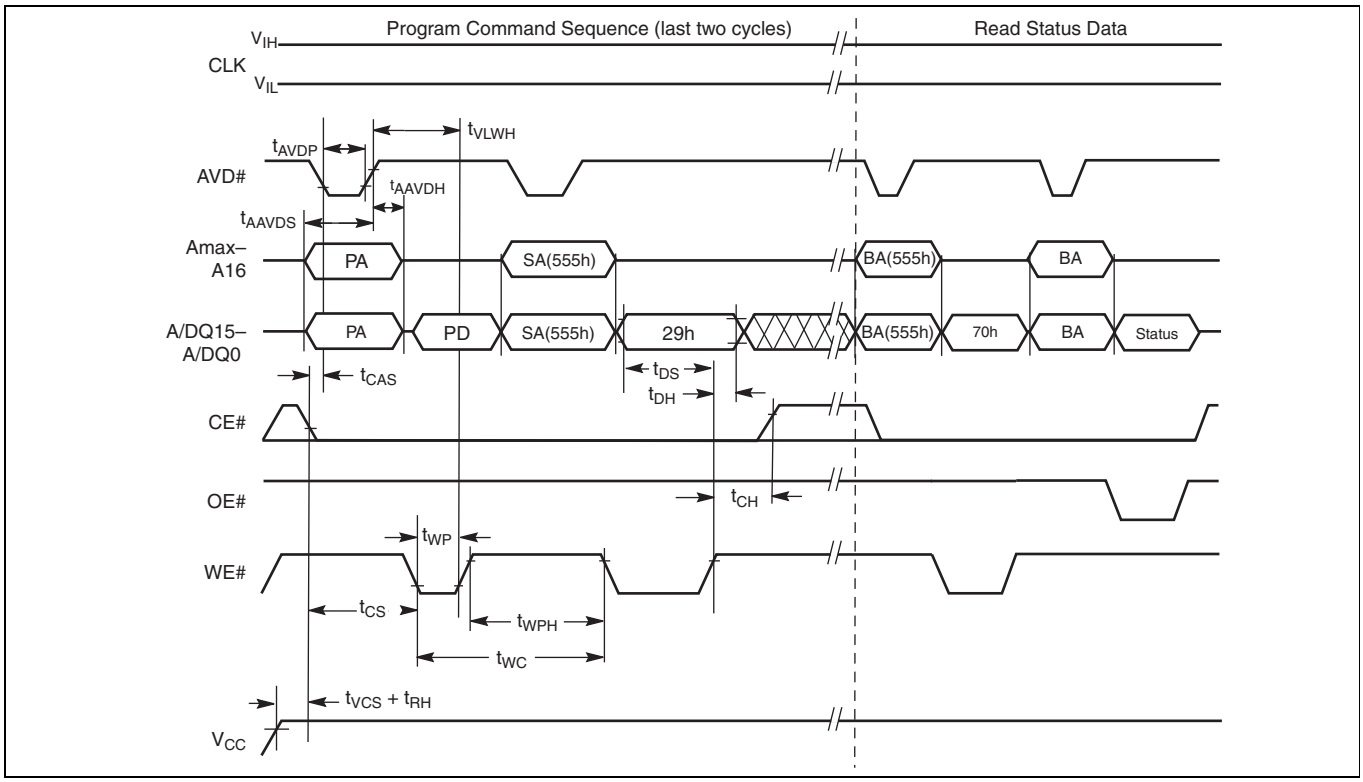


Figure 13 Asynchronous program operation timings - ADM interface

7.9.4 Hardware reset (Reset#)

Table 53 Warm-reset

Parameter		Description		All speed options	Unit
JEDEC	Std				
	t_{RP}	RESET# pulse width	Min	50	ns
	t_{RH}	Reset high time before read	Min	200	ns
	t_{RPH}	RESET# low to CE# low	Min	10	us

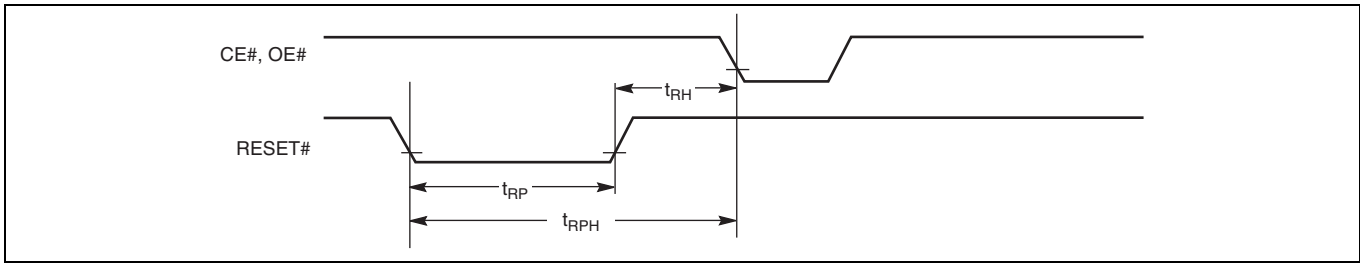


Figure 14 Reset timings

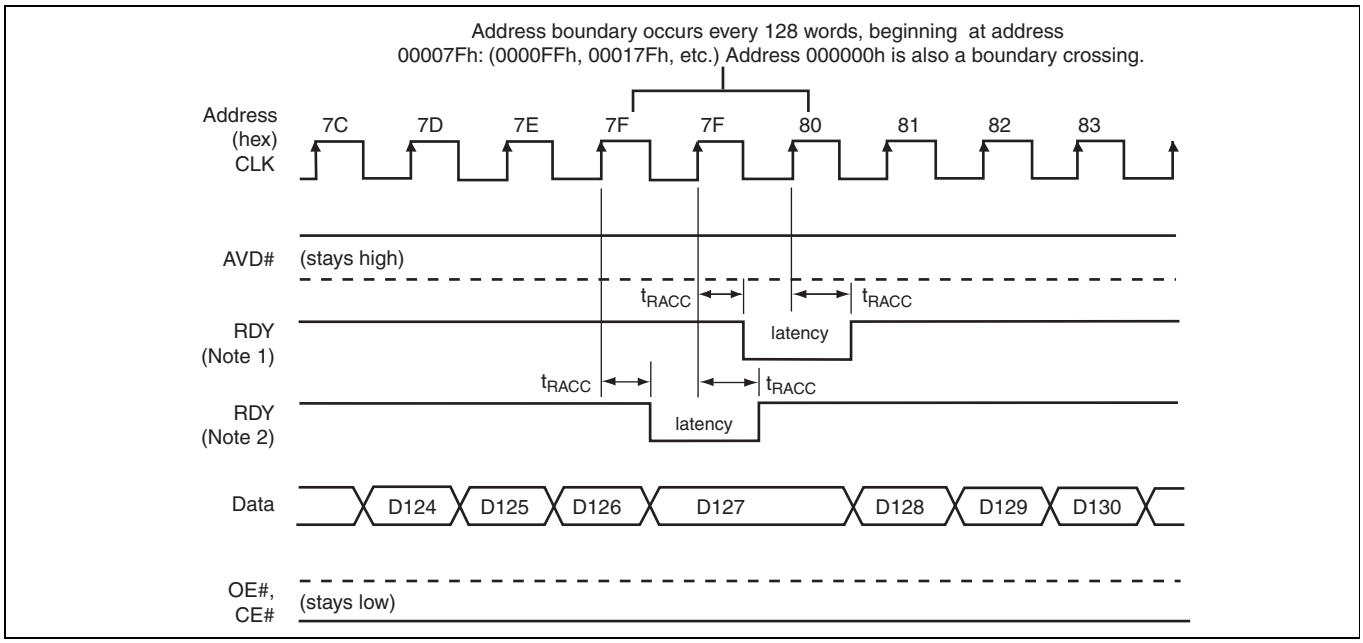


Figure 15 Latency with boundary crossing [54, 55, 56]

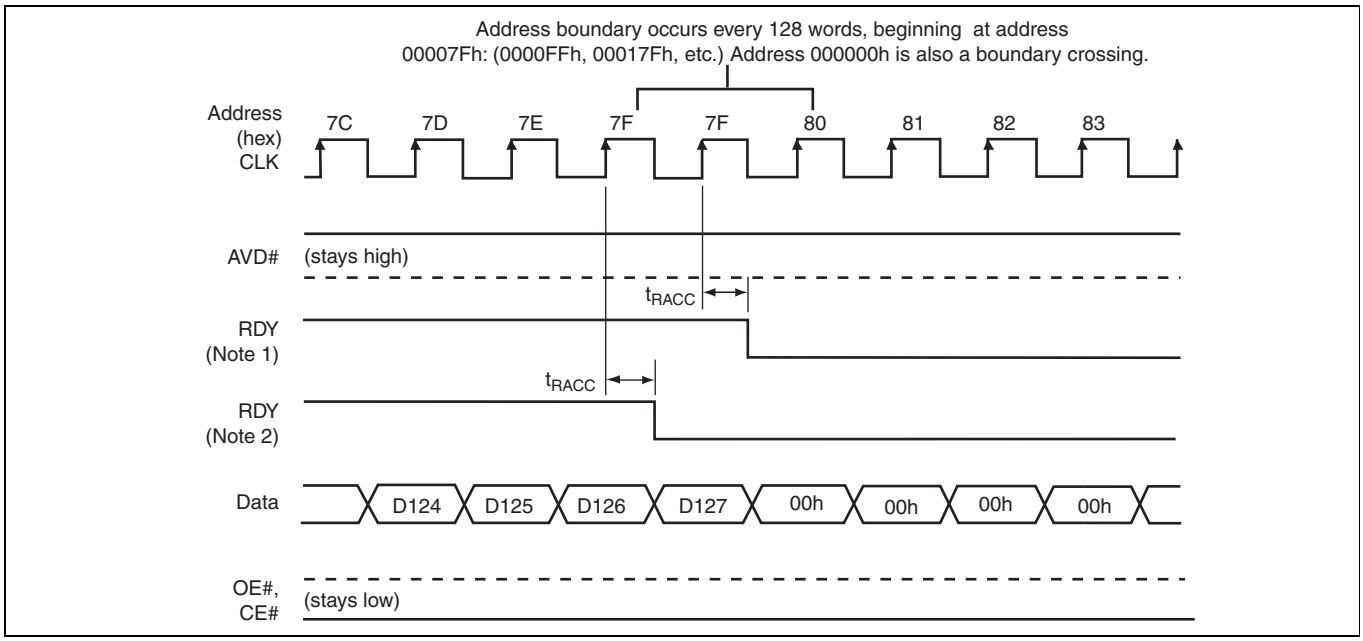


Figure 16 Latency with boundary crossing into bank performing embedded operation [54, 55, 57]

Notes
54.RDY active with data (CR.8 = 1 in the Configuration Register).
55.RDY active one clock cycle before data (CR.8 = 0 in the Configuration Register).
56.Figure shows the device not crossing a bank in the process of performing an erase or program.
57.Figure shows the device crossing a bank in the process of performing an erase or program.

7.9.5 Wait state Configuration Register setup

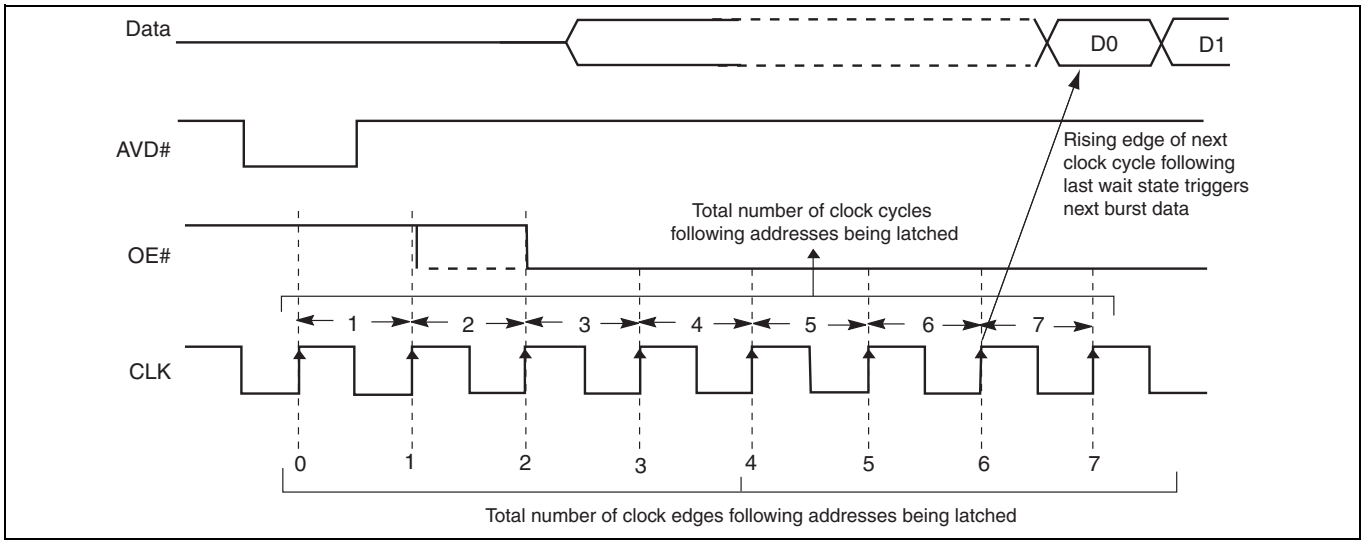


Figure 17 Example of programmable wait states

Table 54 Wait state Configuration Register setup

Configuration Register	Programmable Wait States			
CR.14 CR.13 CR.12 CR.11	0000 =	initial data is valid on the	Reserved	rising CLK edge after addresses are latched
	0001 =		3rd	
	0010 =		4th	
	0011 =		5th	
	0100 =		6th	
	0101 =		7th	
	0110 =		8th	
	0111 =		9th	
	1000 =		10th	
	. . .		. . .	
	1011 =		13th	
	1100 =	Reserved		
	1111 =			

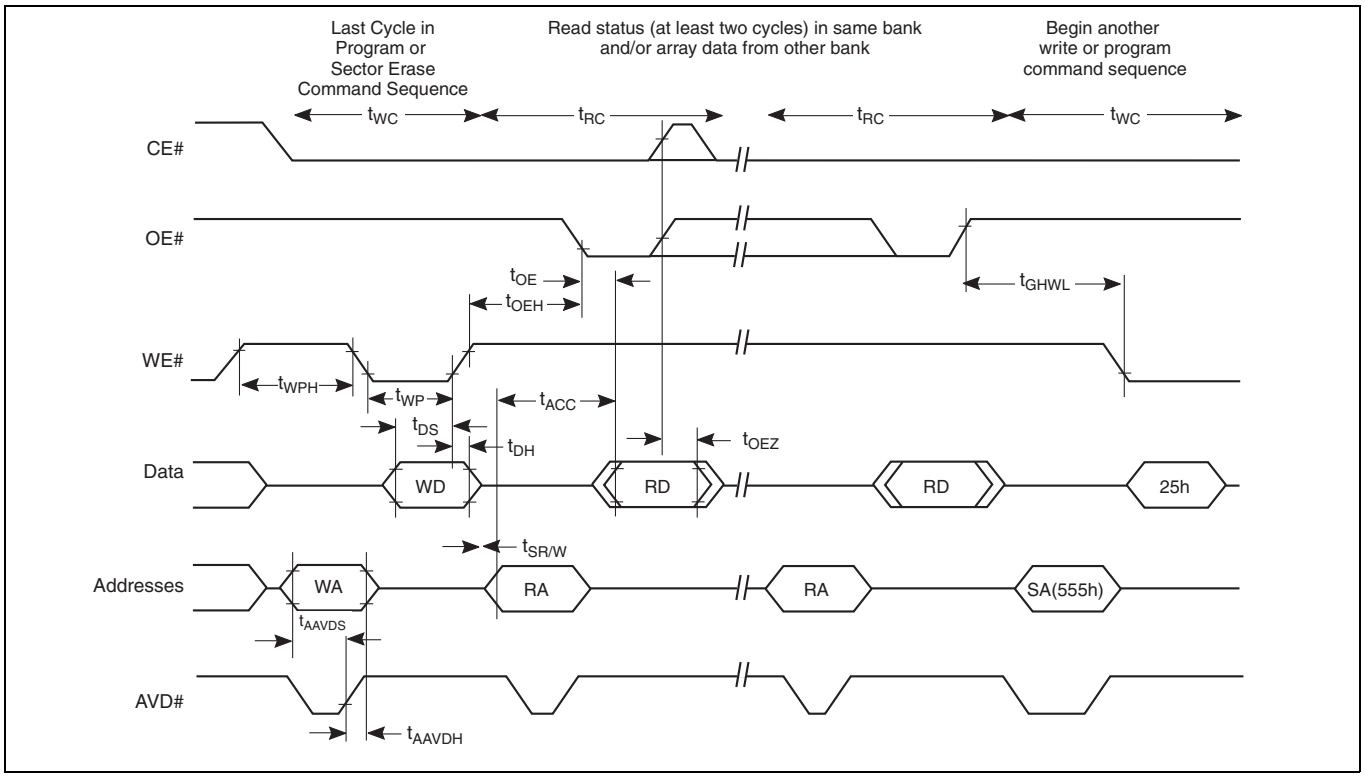


Figure 18 Back-to-back read/write cycle timings - ADM interface [58]

Note

58. Breakpoints in waveforms indicate that system may alternately read array data from the non-busy bank while checking the status of the program or erase operation in the busy bank. The system should read status twice to ensure valid information.

7.9.6 Erase and programming performance

Table 55 Erase and programming performance

Parameter			Typ [59]	Max [60]	Unit	Comments
Sector erase time [64]	128 KB	V_{CC}	0.8/1.3	3.5/5.5	s	[61]
	32 KB	V_{CC}	0.35/0.6	2.0/3.5		
	128 KB	V_{PP}	0.8/1.3	3.5/5.5		
	32 KB	V_{PP}	0.35/0.6	2.0/3.5		
Chip erase time [64], [65]		V_{CC}	78/126 (128 Mb) 155/251 (256 Mb)	200/325 (128 Mb) 400/650 (256 Mb)		
		V_{PP}	78/126 (128 Mb) 155/251 (256 Mb)	154/250 (128 Mb) 308/500 (256 Mb)		
Single word program time (using program buffer)		V_{CC}	170	800	µs	Excludes system level overhead [62]
Effective word programming time using program write buffer		V_{CC}	14.1	94		
		V_{PP}	9	48		
Total 32-word buffer programming time		V_{CC}	450	3000		
		V_{PP}	288	1540		
Chip programming time (using 32 word buffer)		V_{CC}	118 (128 Mb) 236 (256 Mb)	157 (128 Mb) 315 (256 Mb)	s	Excludes system level overhead [62]
		V_{PP}	76 (128 Mb) 151 (256 Mb)	80 (128 Mb) 160 (256 Mb)		
Erase suspend/erase resume (t_{ESL})				30	µs	
Program suspend/program resume (t_{PSL})				30	µs	
Blank check				1	ms	

Notes

59. Typical program and erase times assume the following conditions: 25°C, 1.8 V V_{CC}, 10,000 cycles. Additionally, programming typically assumes a checkerboard pattern.
60. Under worst case conditions of –25°C, V_{CC} = 1.70 V, 100,000 cycles.
61. In the pre-programming step of the embedded erase algorithm, all words are programmed to 00h before erasure.
62. System-level overhead is the time required to execute the bus-cycle sequence for the program command. See **Table 57** for further information on command definitions.
63. The device has a minimum erase and program cycle endurance of 10,000 cycles.
64. The first value excludes pre-programming time, while the second value is inclusive of pre-programming time for the FFFFh pattern, with status polling rate as 400 ns.
65. The erase time is calculated from the time of issuing erase command to the completion of erase operation (indicated by status register).

8 Ordering information

The ordering part number is formed by a valid combination of the following:

S29VS
S29XS **256** **R** **XX** **B** **H** **W** **00** **0**

Packing type
0 = Tray[66]
3 = 13" Tape and reel

Model number
00 = Top
01 = Bottom

Temperature range
W = Wireless (— 25°C to +85°C)

Package material
H = Halogen-free, Lead (Pb)-free

Package type
B = Very thin fine-pitch BGA

Speed option (Burst frequency)
0S = 83 MHz
AA = 104 MHz
AB = 108 MHz

Technology
T = 65-nm MIRRORBIT™ technology

Density
256 = 256 Mb
512 = 512 Mb

Device family
S29VS = 1.8 V-only simultaneous read/write, burst-mode address and data multiplexed flash memory
S29XS = 1.8 V-only simultaneous read/write, burst-mode address low, address high and data multiplexed flash memory

Notes
66.Type 0 is standard. Specify other options as required.

8.1 Valid combinations

Valid combination list configurations are planned to be supported in volume for this device. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 56 Valid combinations

S29VS-R valid combinations [67, 68]				Model Numbers	Package type [68]
Base ordering part number	Speed option	Package type, material, and temperature range	Packing type		
S29VS256R	0S, AA, AB	BHW [69]	0, 3 67	00, 01	6.2 mm x 7.7 mm, 44-ball
S29VS128R					
S29XS256R					
S29XS128R					

Notes
67. Type 0 is standard. Specify other options as required.
68. BGA package marking omits leading S29 and packing type designator from ordering part number.
69. Industrial temperature range is also available. For device specification differences, please refer to the specification supplement with publication number S29VS_XS-R_SP.

9 Package diagrams

This section shows the I/O designations and package specifications for the S29VS-R/S29XS-R.

9.1 Special handling instructions for FBGA package

Special handling is required for flash memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

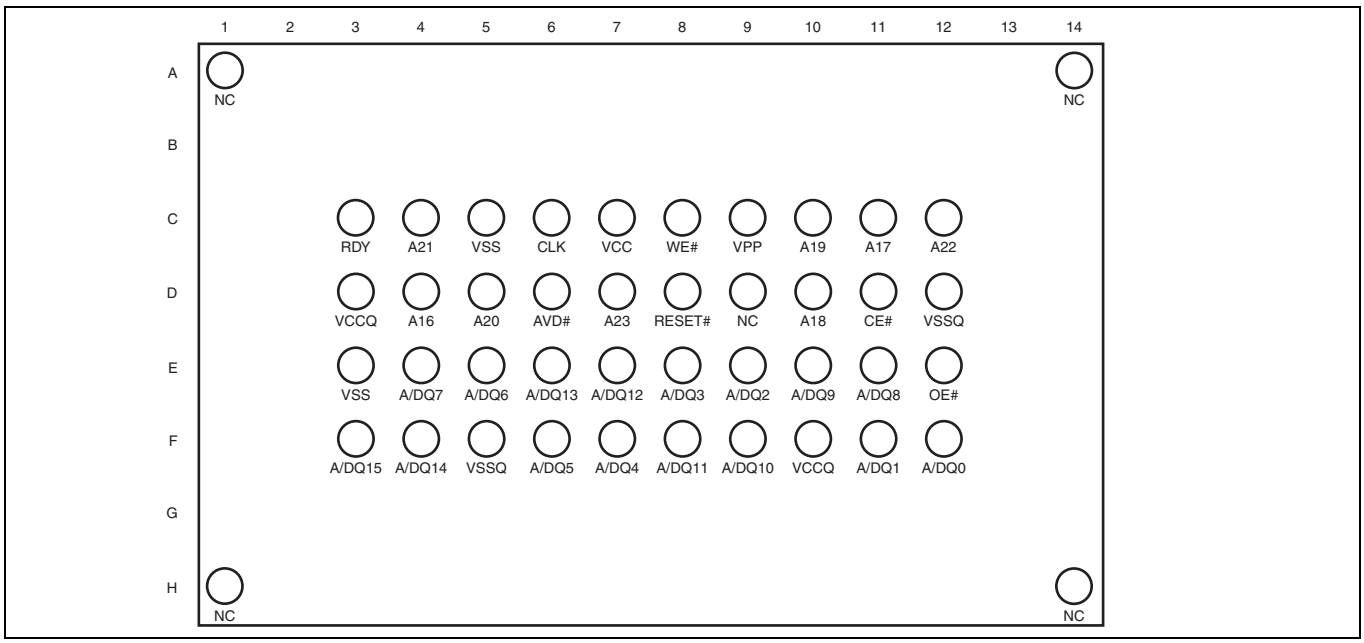
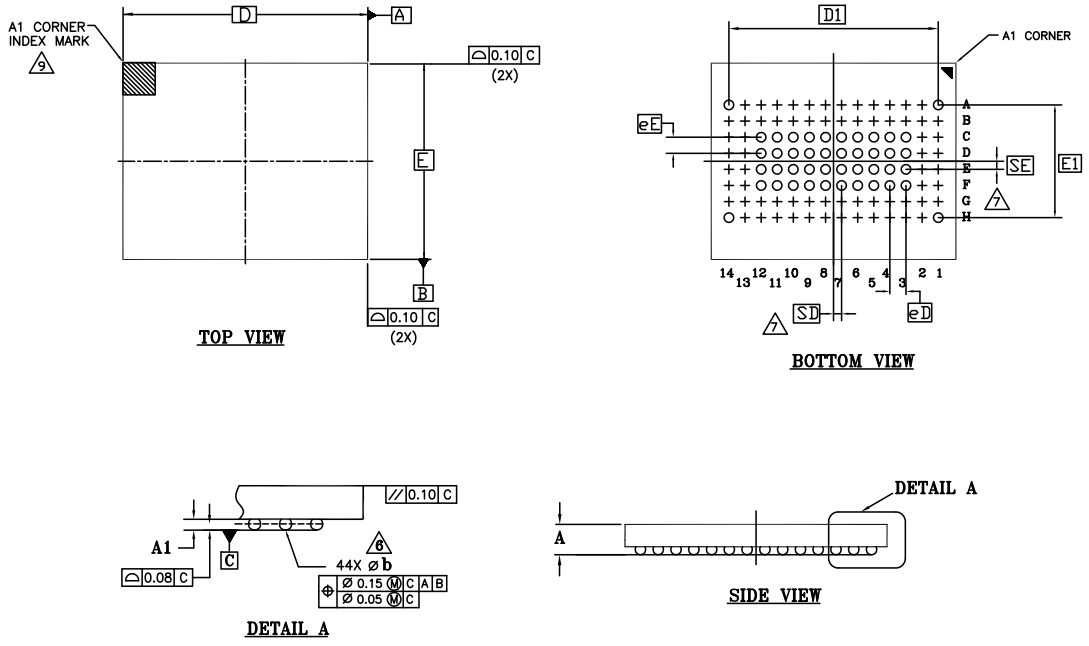


Figure 19 44-ball very thin fine-pitch ball grid array, top view, balls facing down [70, 71]

Notes
70.Ball D7 is NC for S29VS128R.
71.Balls D7, C12, C4, D5, C10, D10, C11, D4 are NC for S29XS256R and S29XS128R.



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.18	-	-
D	7.70 BSC		
E	6.20 BSC		
D1	6.50 BSC		
E1	3.50 BSC		
MD	14		
ME	8		
n	44		
Ø b	0.25	0.30	0.35
eD	0.50 BSC		
eE	0.50 BSC		
SD	0.25 BSC		
SE	0.25 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. JEDEC SPECIFICATION NO. REF. : N/A

002-24745 **

Figure 20 VDJ044—44-ball very thin fine-pitch ball grid array, 7.7 × 6.2 × 1.0 mm

10 References

The following document contains information relating to the S29VS-R/S29XS-R devices. Click on the title or go to **www.infineon.com**, or request a copy from your sales office.

- **AN98522 - X-ray inspection considerations for surface-mounted flash ICs**

11 Appendix

This section contains information relating to software control or interfacing with the flash device.

11.1 Command definitions

All values are in hexadecimal. The S29VS-R family of devices are 16-bit word address oriented. Most system address buses, regardless of data bus size, are byte oriented. It is common practice for system designers to shift the address buses. That is, flash address A0 is connected to system address A1, etc. To accommodate the system designers, addresses are listed in both word address and byte address where applicable. The flash address (word) is listed above the system address (byte).

Table 57 Command definitions

Command sequence	Cycles	Bus cycles [72, 73, 74, 75]							
		First		Second		Third		Fourth	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read		RA	RD						
Reset	1	X	F0						
Write Buffer Load [79]	3-34	(SA) 555 (SA) AAA	25	(SA) 2AA (SA) 554	WC	(SA) PA [82]	PD	PA [83]	PD
Buffer to Flash	1	(SA) 555 (SA) AAA	29						
Chip Erase	2	(SA) 555 (SA) AAA	80	(SA) 2AA (SA) 554	10				
Sector Erase	2	(SA) 555 (SA) AAA	80	(SA) 2AA (SA) 554	30				
Read Status Register	2	(SA) 555 (SA) AAA	70	(SA)	RR				
Clear Status Register	1	(SA) 555 (SA) AAA	71						
Program Suspend [76]	1	XXX	51						
Program Resume [76]	1	(SA) 000	50						

Notes

72. See **"Device operations"** on page 17 for description of bus operations.
73. Except for the following, all bus cycles are write cycle: read cycle during Read, ID/CFI Read (Manufacturing ID, Device ID, Indicator Bits), Configuration Register read, Secure Silicon Region Read, SSR Lock Read, and 2nd cycle of Status Register Read.
74. Data bits DQ15–DQ8 are don't care in command sequences, except for RD, PD, and WD.
75. Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.
76. The Program Resume command is valid only during the Program Suspend mode/state.
77. The Erase Resume command is valid only during the Erase Suspend mode/state.
78. Command is valid when all banks are ready to read array data.
79. The total number of cycles in the command sequence is determined by the number of words written to the write buffer.
80. V_{PP} must be at V_{HH} during the entire operation of this command.
81. Entry commands are needed to enter a specific mode to enable instructions only available within that mode.
82. Must be the lowest word address of the words being programmed within the 32 word write buffer page. This is not necessarily the lowest address of the page. Data words are loaded into the write page buffer in sequential order from lowest to highest address.
83. Subsequent addresses must fall within the same Sector and Page as the initial starting address.
84. Blank Check is only functional in Asynchronous Read mode (Configuration Register - CR [15] = 1).

Table 57 Command definitions *(continued)*

Command sequence		Cycles	Bus cycles [72, 73, 74, 75]							
			First		Second		Third		Fourth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data
Erase Suspend [77]		1	XXX	B0						
Erase Resume [77]		1	(SA) 000	30						
Blank Check [84]		1	(SA) 555 (SA) AAA	33						
Sector Lock/Unlock		3	555 AAA	60	2AA 554	60	SLA	60		
Sector Lock Range		4	555 AAA	60	2AA 554	60	SLA	61	SLA	61
ID/CFI command definitions										
ID/CFI	ID/CFI Entry [78, 81]	1	(SA) X55 (SA) XAA	90 or 98						
	ID/CFI Read	1	(SA) RA	data						
	ID/CFI Exit	1	XXX	FO						
Configuration command definitions										
Configuration Register	Configuration Register Entry [78, 81]	1	(SA) 555 (SA) AAA	D0						
	Write Buffer Load	3	(SA) 555 (SA) AAA	25	(SA) 2AA (SA) 554	0	(SA) X00	PD		
	Buffer to Flash (Configuration Register)	1	(SA) 555 (SA) AAA	29						
	Configuration Register Read	1	(SA) X00	RR						
	Configuration Register Exit	1	XXX	FO						

Notes

72. See **"Device operations"** on page 17 for description of bus operations.
73. Except for the following, all bus cycles are write cycle: read cycle during Read, ID/CFI Read (Manufacturing ID, Device ID, Indicator Bits), Configuration Register read, Secure Silicon Region Read, SSR Lock Read, and 2nd cycle of Status Register Read.
74. Data bits DQ15–DQ8 are don't care in command sequences, except for RD, PD, and WD.
75. Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.
76. The Program Resume command is valid only during the Program Suspend mode/state.
77. The Erase Resume command is valid only during the Erase Suspend mode/state.
78. Command is valid when all banks are ready to read array data.
79. The total number of cycles in the command sequence is determined by the number of words written to the write buffer.
80. V_{PP} must be at V_{HH} during the entire operation of this command.
81. Entry commands are needed to enter a specific mode to enable instructions only available within that mode.
82. Must be the lowest word address of the words being programmed within the 32 word write buffer page. This is not necessarily the lowest address of the page. Data words are loaded into the write page buffer in sequential order from lowest to highest address.
83. Subsequent addresses must fall within the same Sector and Page as the initial starting address.
84. Blank Check is only functional in Asynchronous Read mode (Configuration Register - CR [15] = 1).

Table 57 Command definitions *(continued)*

Command sequence		Cycles	Bus cycles [72, 73, 74, 75]							
			First		Second		Third		Fourth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data
SSR Lock command definitions										
SSR Lock	SSR Lock Entry [78, 81]	1	(SA) 555 (SA) AAA	40						
	Write Buffer Load [79]	3	(SA) 555 (SA) AAA	25	(SA) 2AA (SA) 554	0	(SA) 00	PD		
	Buffer to Flash	1	(SA) 555 (SA) AAA	29						
	SSR Lock Read	1	(SA) XXX	RR						
	SSR Lock Exit	1	XXX	F0						
Secure Silicon Region command definitions										
Secure Silicon Region	Secure Silicon Region Entry [78, 81]	1	(SA) 555 (SA) AAA	88						
	Write Buffer Load [79]	3-34	(SA) 555 (SA) AAA	25	(SA) 2AA (SA) 554	WC	(SA) PA	PD	(SA) PA	PD
	Buffer to Flash	1	(SA) 555 (SA) AAA	29						
	Secure Silicon Region Read	1	(SA) RA	RD						
	Secure Silicon Region Exit	1	XXX	F0						

Notes

72. See **"Device operations"** on page 17 for description of bus operations.
73. Except for the following, all bus cycles are write cycle: read cycle during Read, ID/CFI Read (Manufacturing ID, Device ID, Indicator Bits), Configuration Register read, Secure Silicon Region Read, SSR Lock Read, and 2nd cycle of Status Register Read.
74. Data bits DQ15–DQ8 are don't care in command sequences, except for RD, PD, and WD.
75. Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.
76. The Program Resume command is valid only during the Program Suspend mode/state.
77. The Erase Resume command is valid only during the Erase Suspend mode/state.
78. Command is valid when all banks are ready to read array data.
79. The total number of cycles in the command sequence is determined by the number of words written to the write buffer.
80. V_{PP} must be at V_{HH} during the entire operation of this command.
81. Entry commands are needed to enter a specific mode to enable instructions only available within that mode.
82. Must be the lowest word address of the words being programmed within the 32 word write buffer page. This is not necessarily the lowest address of the page. Data words are loaded into the write page buffer in sequential order from lowest to highest address.
83. Subsequent addresses must fall within the same Sector and Page as the initial starting address.
84. Blank Check is only functional in Asynchronous Read mode (Configuration Register - CR [15] = 1).

Legend:

- X = Don't care
- RA = Address of the location to be read.
- RD = Read Data from location RA during read operation.

- RR = Read Register value
- PA = Address of the memory location to be programmed.
- PD = Data to be programmed at location PA.
- BA = Address bits sufficient to select a bank
- SA = Address bits sufficient to select a sector
- SLA = Sector Lock Address
- WBL = Write Buffer Location. Address must be within the same write buffer page as PA.
- WC = Word Count. Number of write buffer locations to load minus 1.

11.2 Device ID and common flash memory interface address map

The Device ID fields occupy the first 32 bytes of address space followed by the common flash interface data structure. The common flash interface (CFI) specification defines a standardized data structure containing device specific parameter, structure, and feature set information, which allows vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and back-ward-compatible for the specified flash device families. Flash driver software can be standardized for long-term compatibility.

This device enters the ID/CFI mode when the system writes the ID/CFI Query command, 90h or 98h, to address (SA)55h any time all banks are in read mode (the CU is in Idle State). The system can then read ID and CFI information at the addresses, within the selected sector, given in the following tables. To terminate reading ID/CFI, the system must write the reset command.

Table 58 ID/CFI data

	Word offset address	Byte offset address	DATA		Description
			VS256R/XS256R	VS128R/XS128R	
Device identification	(SA) + 00h	(SA) + 00h	0001h		Infineon manufacturer ID
	(SA) + 01h	(SA) + 02h	007Eh (Top/Bottom)	007Eh (Top/Bottom)	Device ID, Word 1 Extended ID address code. Indicates an extended two byte device ID is located at byte address 1Ch and 1Eh.
	(SA) + 02h	(SA) + 04h	Reserved		Reserved
	(SA) + 03h	(SA) + 06h	Reserved		Reserved
	(SA) + 04h	(SA) + 08h	Reserved		Reserved
	(SA) + 05h	(SA) + 0Ah	Reserved		Reserved
	(SA) + 06h	(SA) + 0Ch	0010h		ID Version
	(SA) + 07h	(SA) + 0Eh	DQ15 - DQ8 = Reserved DQ7 - Factory Lock Bit: 1 = Locked; 0 = Not Locked DQ6 - Customer Lock Bit: 1 = Locked; 0 = Not locked DQ5 - DQ0 = Reserved		Indicator bits
	(SA) + 08h	(SA) + 10h	Reserved		Reserved
	(SA) + 09h	(SA) + 12h	Reserved		Reserved
	(SA) + 0Ah	(SA) + 14h	Reserved		Reserved
	(SA) + 0Bh	(SA) + 16h	Reserved		Reserved

Table 58 ID/CFI data *(continued)*

	Word offset address	Byte offset address	DATA		Description
			VS256R/XS256R	VS128R/XS128R	
Device identification	(SA) + 0Ch	(SA) + 18h	05h Bit 0 - Status Register support 1 = Status Register supported 0 = Status Register not supported Bit 1 - DQ polling support 1 = DQ bits polling supported 0 = DQ bits polling not supported Bit 3-2 - Command set support 11 = Reserved 10 = Reserved 01 = Reduced command set 00 = Old command set Bit 4- F - Reserved		Lower software bits
	(SA) + 0Dh	(SA) + 1Ah	Reserved		Upper software bits Reserved
	(SA) + 0Eh	(SA) + 1Ch	0064h/Top; 0066h/Bottom	0063h/Top; 0065h/Bottom	High order device ID, Word 2
	(SA) + 0Fh	(SA) + 1Eh	0001h (Top/Bottom)	0001h (Top/Bottom)	Low order device ID, Word 3
Common flash interface	**CFI query identification string**				
	(SA) + 10h	(SA) + 20h	0051h		Query Unique ASCII string “QRY”
	(SA) + 11h	(SA) + 22h	0052h		
	(SA) + 12h	(SA) + 24h	0059h		
	(SA) + 13h	(SA) + 26h	0002h		Primary algorithm command set (Infineon = 0002h)
	(SA) + 14h	(SA) + 28h	0000h		
	(SA) + 15h	(SA) + 2Ah	0040h		Address for primary extended table
	(SA) + 16h	(SA) + 2Ch	0000h		
	(SA) + 17h	(SA) + 2Eh	0000h		Alternate algorithm command set (00h = none exists)
	(SA) + 18h	(SA) + 30h	0000h		
	(SA) + 19h	(SA) + 32h	0000h		Address for secondary algorithm extended query table (00h = none exists)
	(SA) + 1Ah	(SA) + 34h	0000h		
	System interface string				
	(SA) + 1Bh	(SA) + 36h	0017h		V_{CC} logic supply minimum program/erase or write voltage D7-D4: Volt D3-D0: 100 millivolt
	(SA) + 1Ch	(SA) + 38h	0019h		V_{CC} logic supply maximum program/erase or write voltage D7-D4: Volt D3-D0: 100 millivolt
	(SA) + 1Dh	(SA) + 3Ah	0085h		V_{PP} [Programming] supply minimum program/erase voltage (00h = no V_{PP} pin present)

Table 58 ID/CFI data *(continued)*

	Word offset address	Byte offset address	DATA		Description
			VS256R/XS256R	VS128R/XS128R	
Common flash interface	(SA) + 1Eh	(SA) + 3Ch	0095h		V_{PP} [Programming] supply maximum program/erase voltage (00h = no V_{PP} pin present)
	(SA) + 1Fh	(SA) + 3Eh	0008h		Typical word programming time per single word 2^N µs (e.g., < or = 32 µs)
	(SA) + 20h	(SA) + 40h	0009h		Typical Program Time for programming the complete buffer 2^N µs (e.g., < or = 256 µs) (00h = not supported)
	(SA) + 21h	(SA) + 42h	000Ah		Typical time for sector erase 2^N ms
	(SA) + 22h	(SA) + 44h	0012h	0011h	Typical time for full chip erase 2^N µs (00h = not supported)
	(SA) + 23h	(SA) + 46h	0003h		Max. program time per single word [2^N times typical value]
	(SA) + 24h	(SA) + 48h	0003h		Max. program time using buffer [2^N times typical value]
	(SA) + 25h	(SA) + 4Ah	0003h		Max. time for sector erase [2^N times typical value]
	(SA) + 26h	(SA) + 4Ch	0003h		Max. time for full chip erase [2^N times typical value] (00h = not supported)
	Device geometry definition				
	(SA) + 27h	(SA) + 4Eh	0019h	0018h	Device size = 2^N byte
	(SA) + 28h	(SA) + 50h	0001h		Flash device interface 0h = x8 1h = x16 2h = x8/x16 3h = x32 [lower byte]
	(SA) + 29h	(SA) + 52h	0000h		[upper byte] (00h = not supported)
	(SA) + 2Ah	(SA) + 54h	0006h		Max. number of bytes in multi-byte buffer write = 2^N [lower byte]
	(SA) + 2Bh	(SA) + 56h	0000h		[upper byte] (00h = not supported)
	(SA) + 2Ch	(SA) + 58h	0002h		Number of erase block regions within device (Number of regions within the device containing one or more contiguous erase blocks of the same size)
	(SA) + 2Dh	(SA) + 5Ah	00FEh (Top boot) 0003h (Bottom boot)	007Eh (Top boot) 0003h (Bottom boot)	Erase block region 1 information [lower byte] - Number of erase sectors of identical size within the erase block region. 00h = 1 sector; 01h = 2 sectors 02h = 3 sectors 03h = 4 sectors
	(SA) + 2Eh	(SA) + 5Ch	0000h		[upper byte]

Table 58 ID/CFI data *(continued)*

	Word offset address	Byte offset address	DATA		Description
			VS256R/XS256R	VS128R/XS128R	
Common flash interface	(SA) + 2Fh	(SA) + 5Eh	0000h (Top boot)		[lower byte] - Sector size in bytes divided by 256 (n [bytes]h = sector size / 256)
			0080h (Bottom boot)		
	(SA) + 30h	(SA) + 60h	0002h (Top boot)		[upper byte]
			0000h (Bottom boot)		
	(SA) + 31h	(SA) + 62h	0003h (Top boot)	0003h (Top boot)	Erase block region 2 Information
			00FEh (Bottom boot)	007Eh (Bottom boot)	
	(SA) + 32h	(SA) + 64h	0000h		[upper byte]
	(SA) + 33h	(SA) + 66h	0080h (Top boot)		[lower byte] - Sector size in bytes divided by 256 (n [bytes]h = sector size / 256)
			0000h (Bottom boot)		
	(SA) + 34h	(SA) + 68h	0000h (Top boot)		[upper byte]
			0002h (Bottom boot)		
	Primary algorithm-Specific extended query				
	(SA) + 40h	(SA) + 80h	0050h		Query unique ASCII string “PRI”
	(SA) + 41h	(SA) + 82h	0052h		
	(SA) + 42h	(SA) + 84h	0049h		
	(SA) + 43h	(SA) + 86h	0031h		Major CFI version number, ASCII
	(SA) + 44h	(SA) + 88h	0034h		Minor CFI version number, ASCII
	(SA) + 45h	(SA) + 8Ah	0020h		Address sensitive unlock (Bits 1-0): 00b = Required 01b = Not required Process technology (Bits 5-2) 0011b = 130-nm floating-gate technology 0100b = 110-nm MIRRORBIT™ technology 0101b = 90-nm floating-gate technology 0110b = 90-nm MIRRORBIT™ technology 1000b = 65-nm MIRRORBIT™ technology
	(SA) + 46h	(SA) + 8Ch	0002h		Erase suspend 0= Not supported 1 = To read only 2 = To read and write
	(SA) + 47h	(SA) + 8Eh	0001h		Sector protection per group 0 = not Supported X = number of sectors in per group
	(SA) + 48h	(SA) + 90h	0000h		Sector temporary unprotect 00h = Not supported 01h = Supported
	(SA) + 49h	(SA) + 92h	0009h		Sector protect/unprotect scheme 08h = Advanced sector protection 09h = Single-sector lock + Sector lock range

Table 58 ID/CFI data *(continued)*

	Word offset address	Byte offset address	DATA		Description
			VS256R/XS256R	VS128R/XS128R	
Common Flash Interface	(SA) + 4Ah	(SA) + 94h	00E0h	0070h	Simultaneous operations Number of sectors in all banks except boot bank
	(SA) + 4Bh	(SA) + 96h	0001h		Burst mode type 00h = Not supported 01h = Supported
	(SA) + 4Ch	(SA) + 98h	0000h		Page mode type 00h = Not supported 01h = 4-word page 02h = 8-word page 04h = 16-word page
	(SA) + 4Dh	(SA) + 9Ah	0085h		V_{PP} (Acceleration) supply minimum 00h = Not supported D7-D4: Volt D3-D0: 100 millivolt
	(SA) + 4Eh	(SA) + 9Ch	0095h		V_{PP} (Acceleration) supply maximum 00h = Not supported D7-D4: Volt D3-D0: 100 millivolt
	(SA) + 4Fh	(SA) + 9Eh	03h (Top boot) 02h (Bottom boot)		Top/bottom sector flag 00h = Uniform 01h = Dual boot 02h = Bottom boot 03h = Top boot
	(SA) + 50h	(SA) + A0h	0001h		Program suspend 00h = Not supported 01h= Supported
	(SA) + 51h	(SA) + A2h	0000h		Unlock bypass 00h = Not supported 01h = Supported
	(SA) + 52h	(SA) + A4h	0008h		Secure silicon region (Customer SSR Area) Size 2^N bytes
	(SA) + 53h	(SA) + A6h	000Eh		Hardware reset ow time-out until reset is completed during an embedded algorithm - Maximum 2^N ns (e.g., 10 µs => n = E)
	(SA) + 54h	(SA) + A8h	000Eh		Hardware reset low time-out until reset is completed not during an embedded algorithm - Maximum 2^N ns (e.g., 10 µs => n = E)
	(SA) + 55h	(SA) + AAh	0005h		Erase suspend time-out maximum 2^N µs
	(SA) + 56h	(SA) + ACh	0005h		Program suspend time-out maximum 2^N µs
	(SA) + 57h	(SA) + AEh	0008h		Bank organization: X= Number of banks

Table 58 ID/CFI data *(continued)*

	Word offset address	Byte offset address	DATA		Description
			VS256R/XS256R	VS128R/XS128R	
Common flash interface	(SA) + 58h	(SA) + B0h	0020h (Top boot)	0010h (Top boot)	Bank 0 region information. X= Number of sectors in bank
			0023h (Bottom boot)	0013h (Bottom boot)	
	(SA) + 59h	(SA) + B2h	0020h	0010h	Bank 1 region information. X= Number of sectors in bank
	(SA) + 5Ah	(SA) + B4h	0020h	0010h	Bank 2 region information. X= Number of sectors in bank
	(SA) + 5Bh	(SA) + B6h	0020h	0010h	Bank 3 region information. X= Number of sectors in bank
	(SA) + 5Ch	(SA) + B8h	0020h	0010h	Bank 4 region information. X= Number of sectors in bank
	(SA) + 5Dh	(SA) + BAh	0020h	0010h	Bank 5 region information. X= Number of sectors in bank
	(SA) + 5Eh	(SA) + BCh	0020h	0010h	Bank 6 region information. X= Number of sectors in bank
	(SA) + 5Fh	(SA) + BEh	0020h (Bottom boot)	0010h (Bottom boot)	Bank 7 region information. X= Number of sectors in bank
			0023h (Top boot)	0013h (Top boot)	

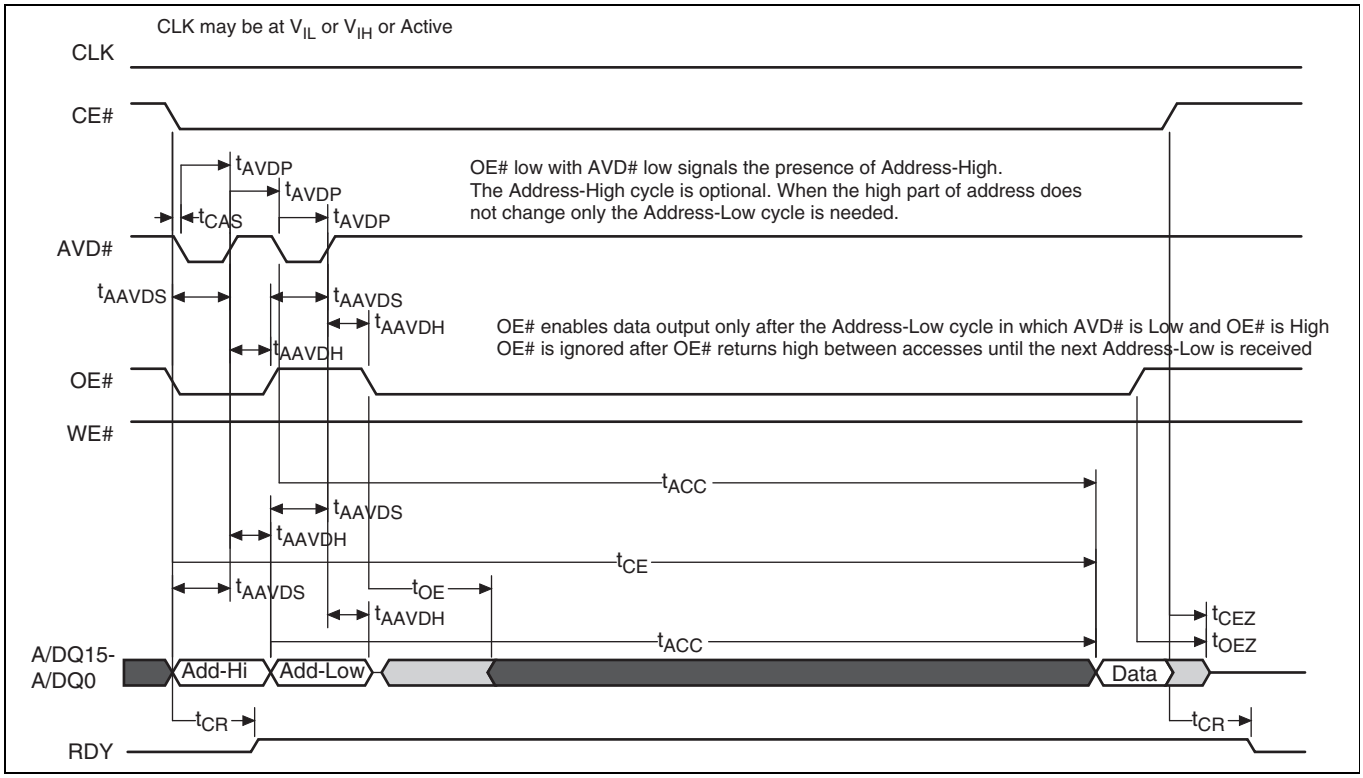


Figure 21 Asynchronous read - AADM interface

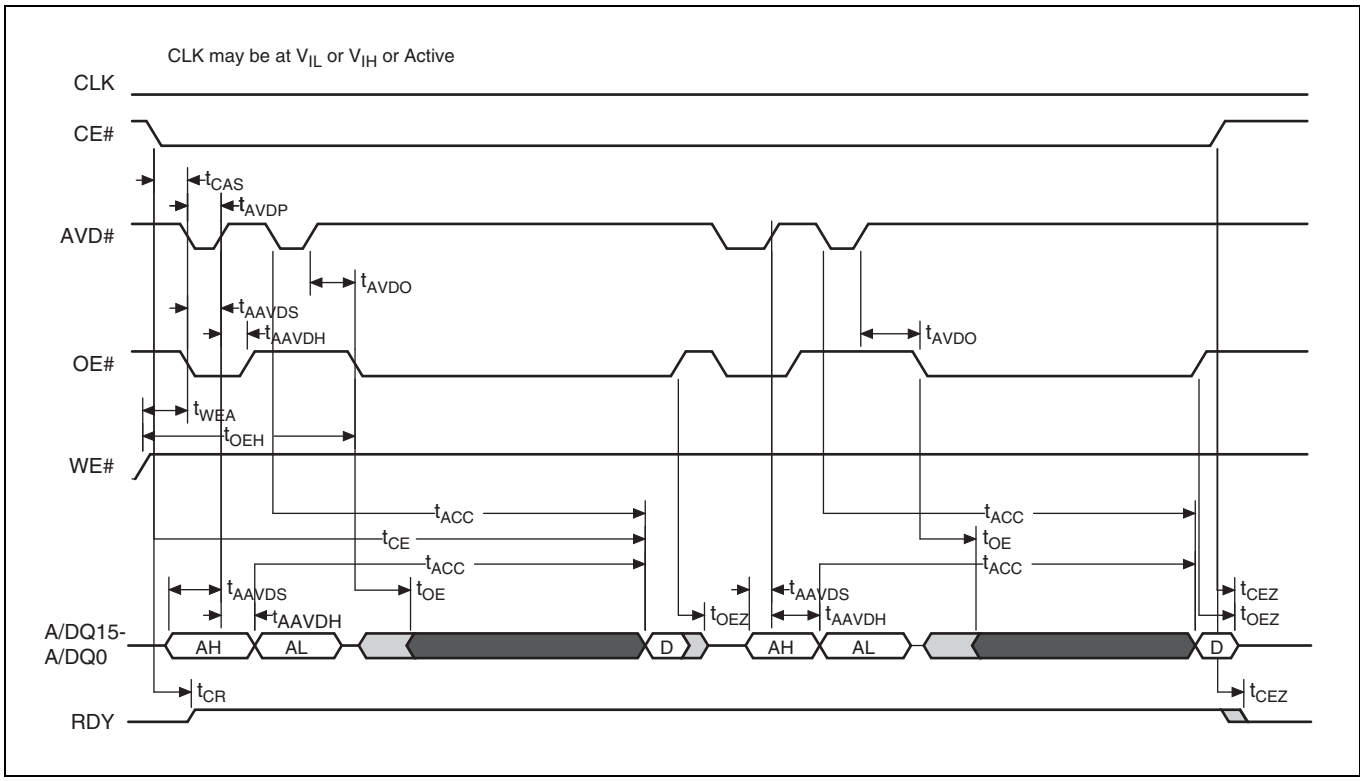


Figure 22 Asynchronous read followed by read - AADM interface

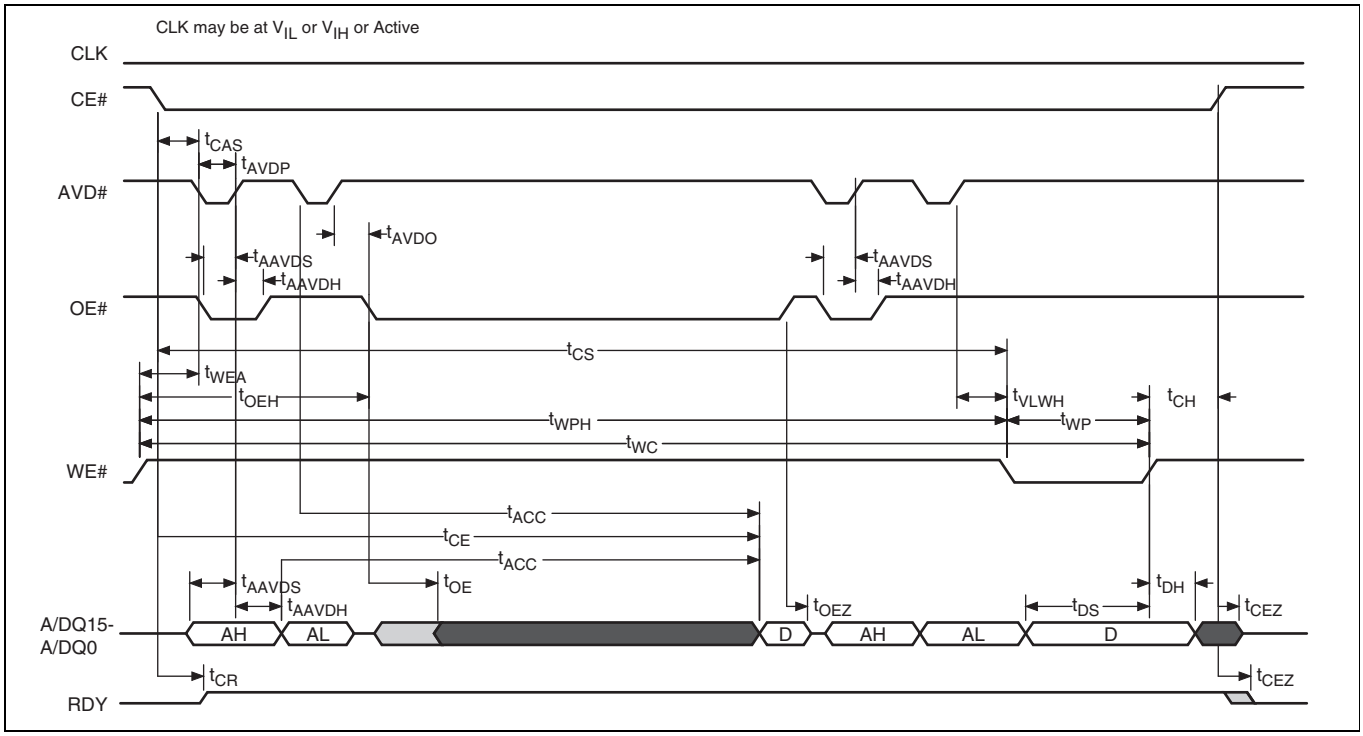


Figure 23 Asynchronous read followed by write - AADM interface

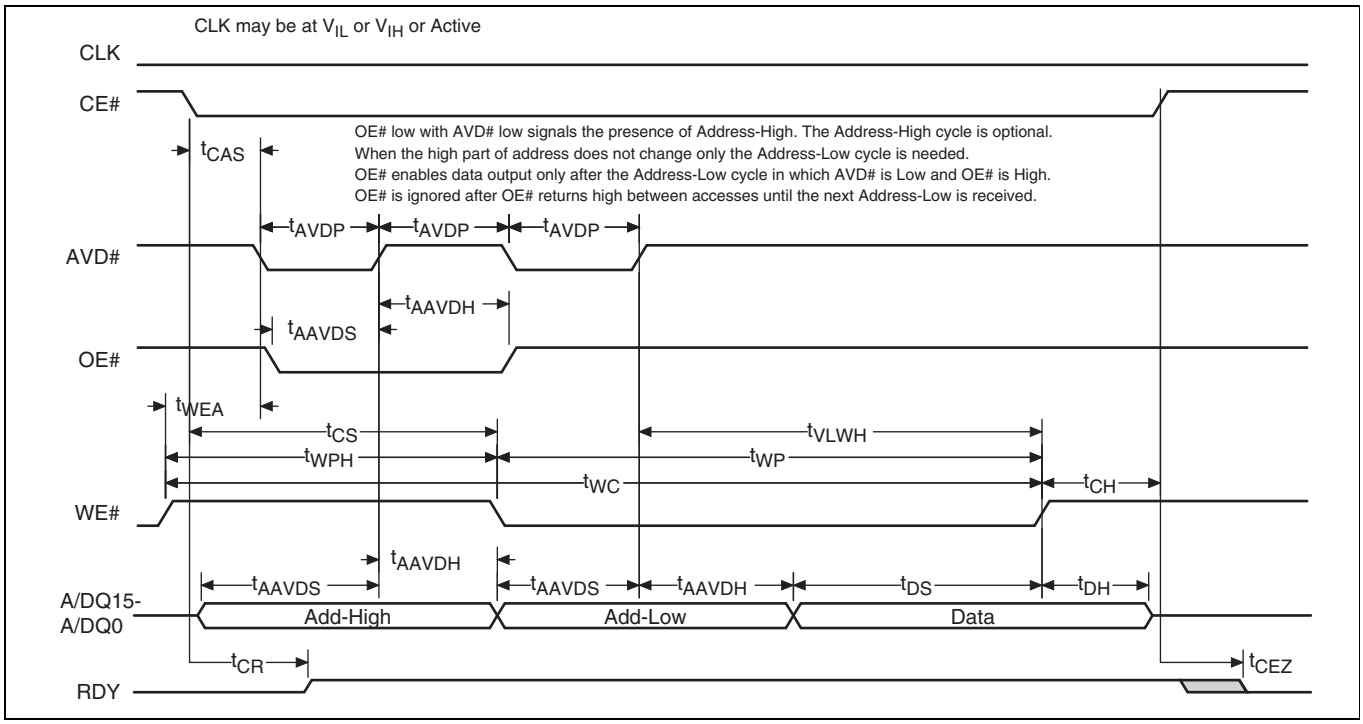


Figure 24 Asynchronous write - AADM interface

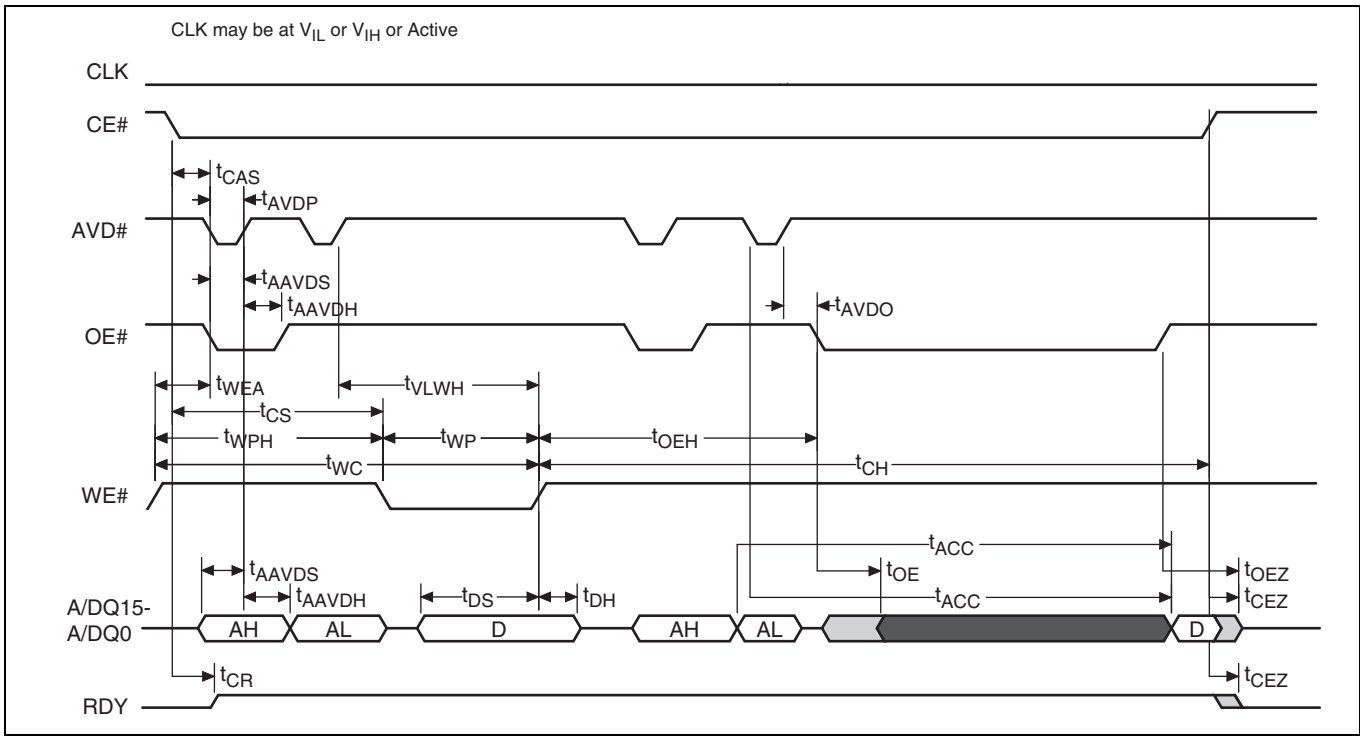


Figure 25 Asynchronous write followed by read - AADM interface

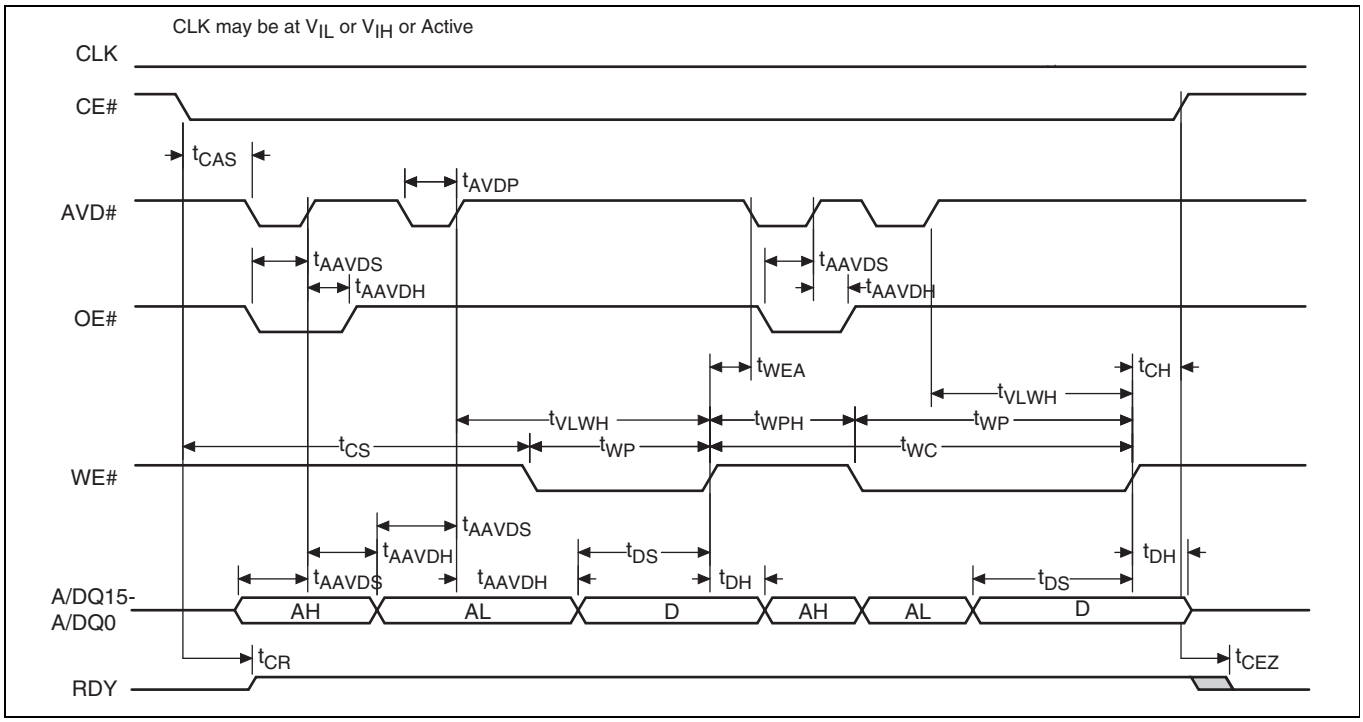


Figure 26 Asynchronous write followed by write - AADM interface

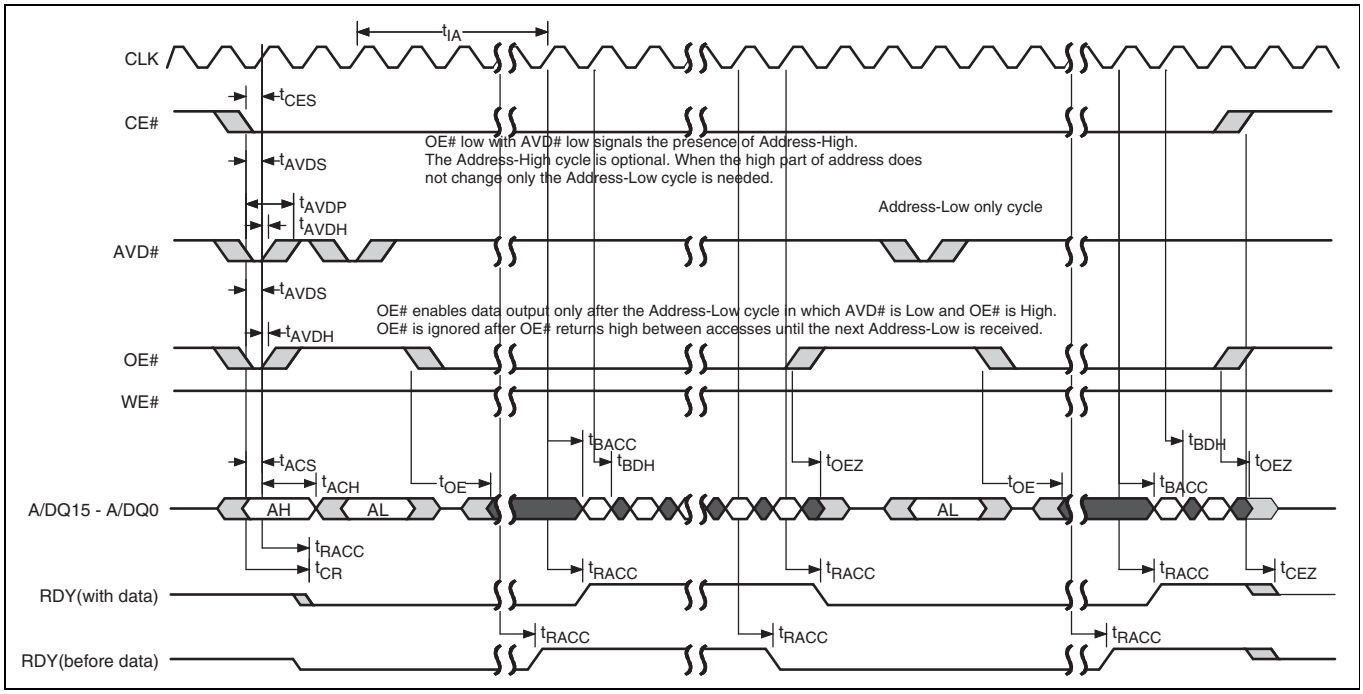


Figure 27 Synchronous read wrapped burst address low only - AADM interface

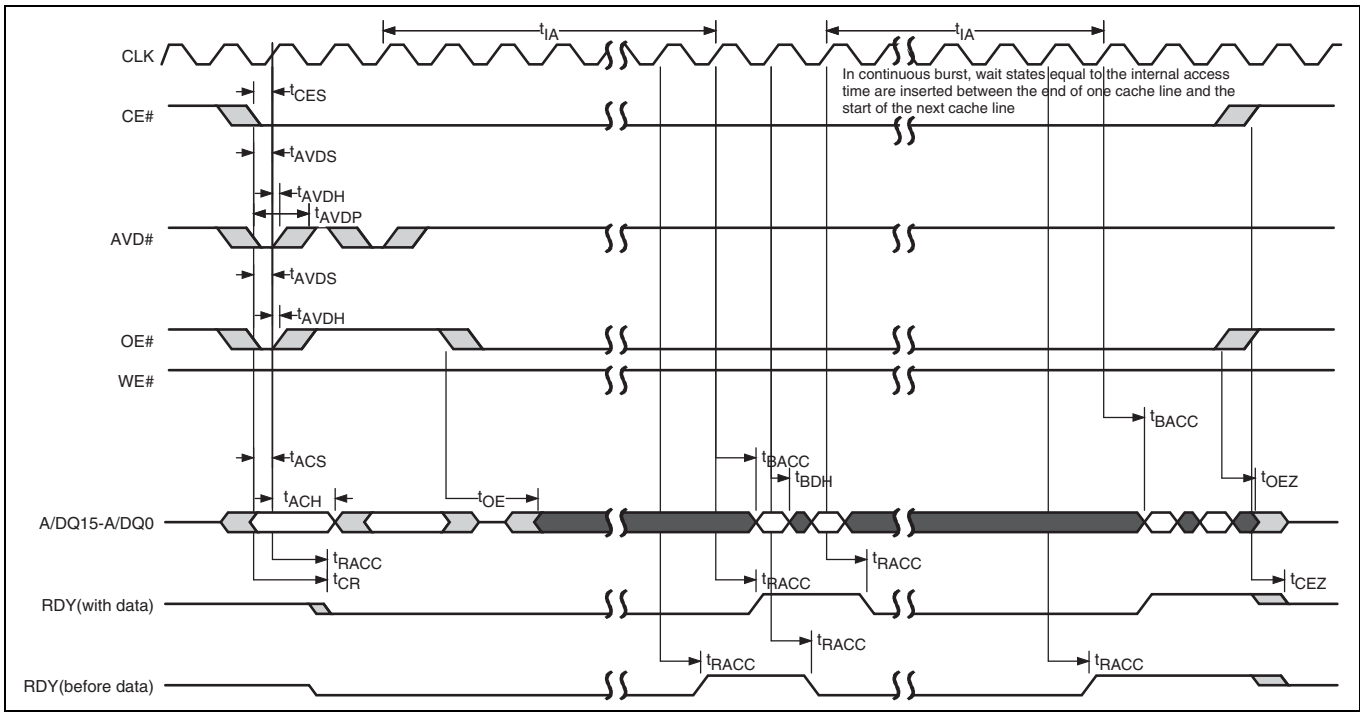


Figure 28 Synchronous read continuous burst - AADM interface

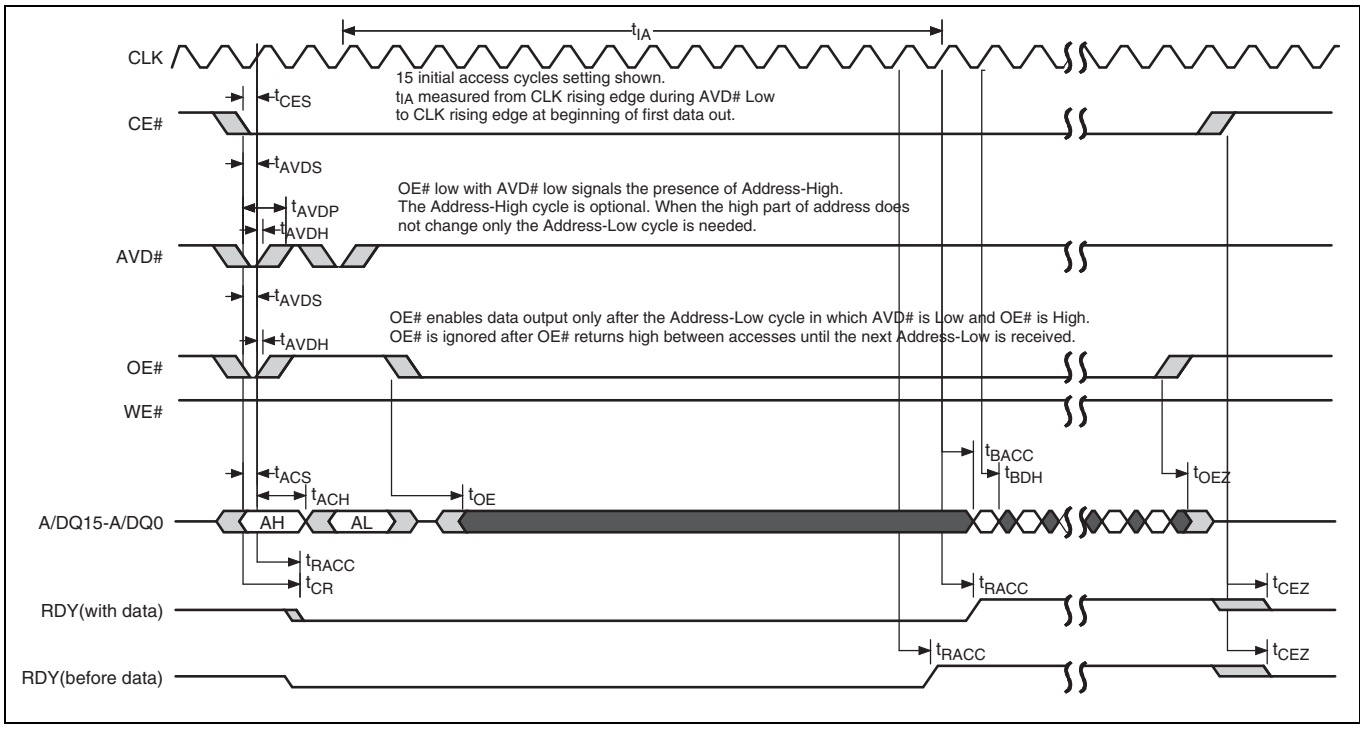


Figure 29 Synchronous read wrapped burst - AADM interface

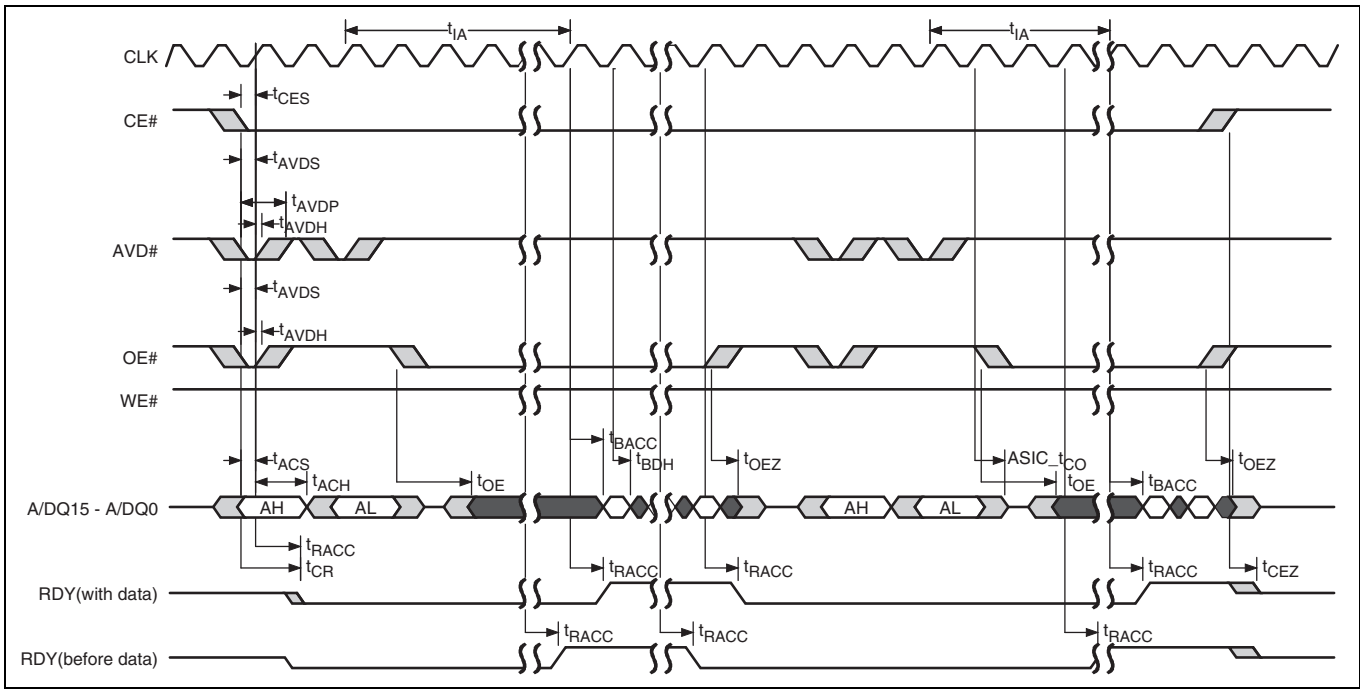


Figure 30 Synchronous read followed by read burst - AADM interface

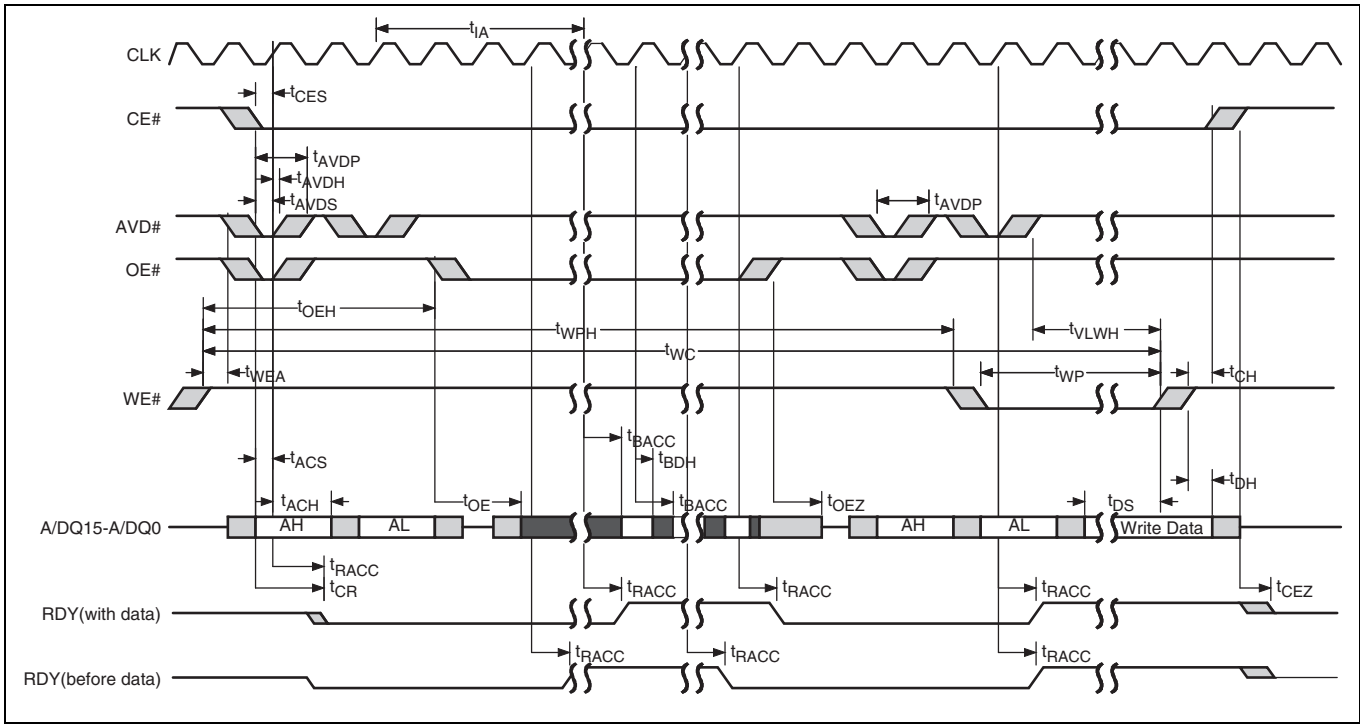


Figure 31 Synchronous read followed by write - AADM interface

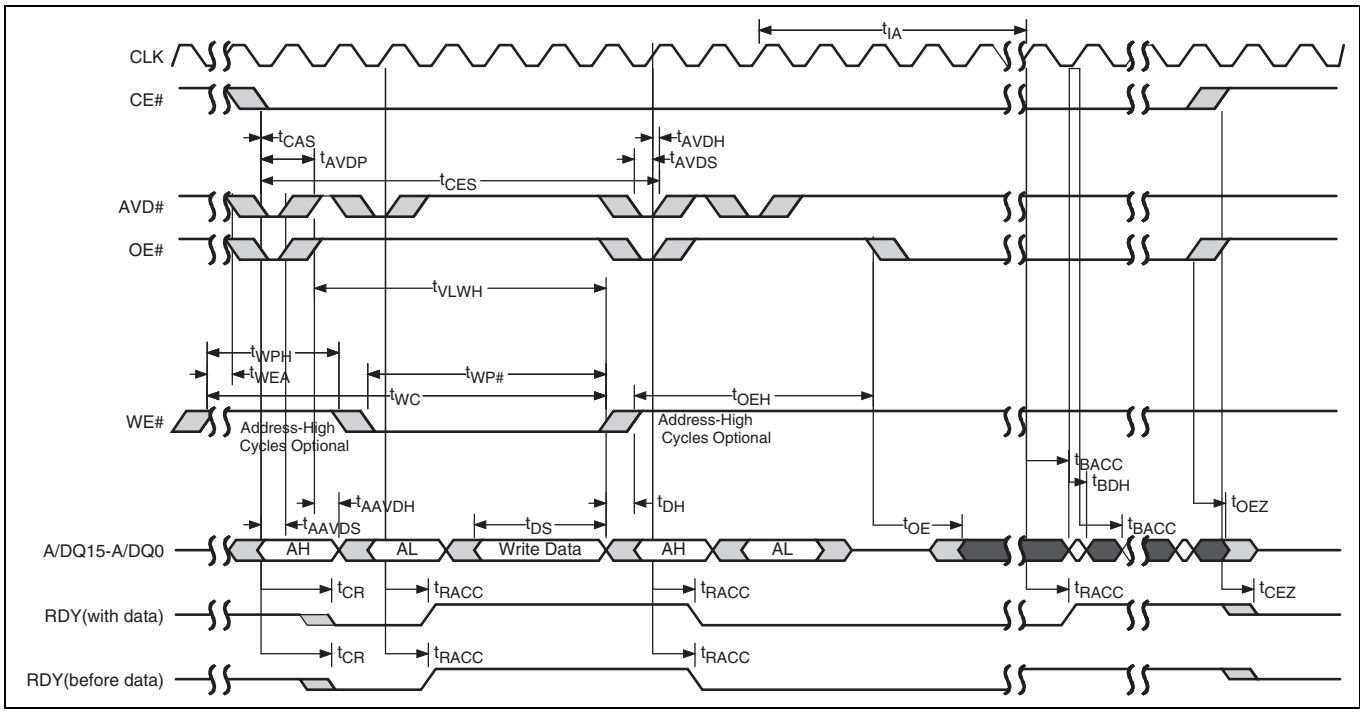


Figure 32 Synchronous write followed by read burst - AADM interface

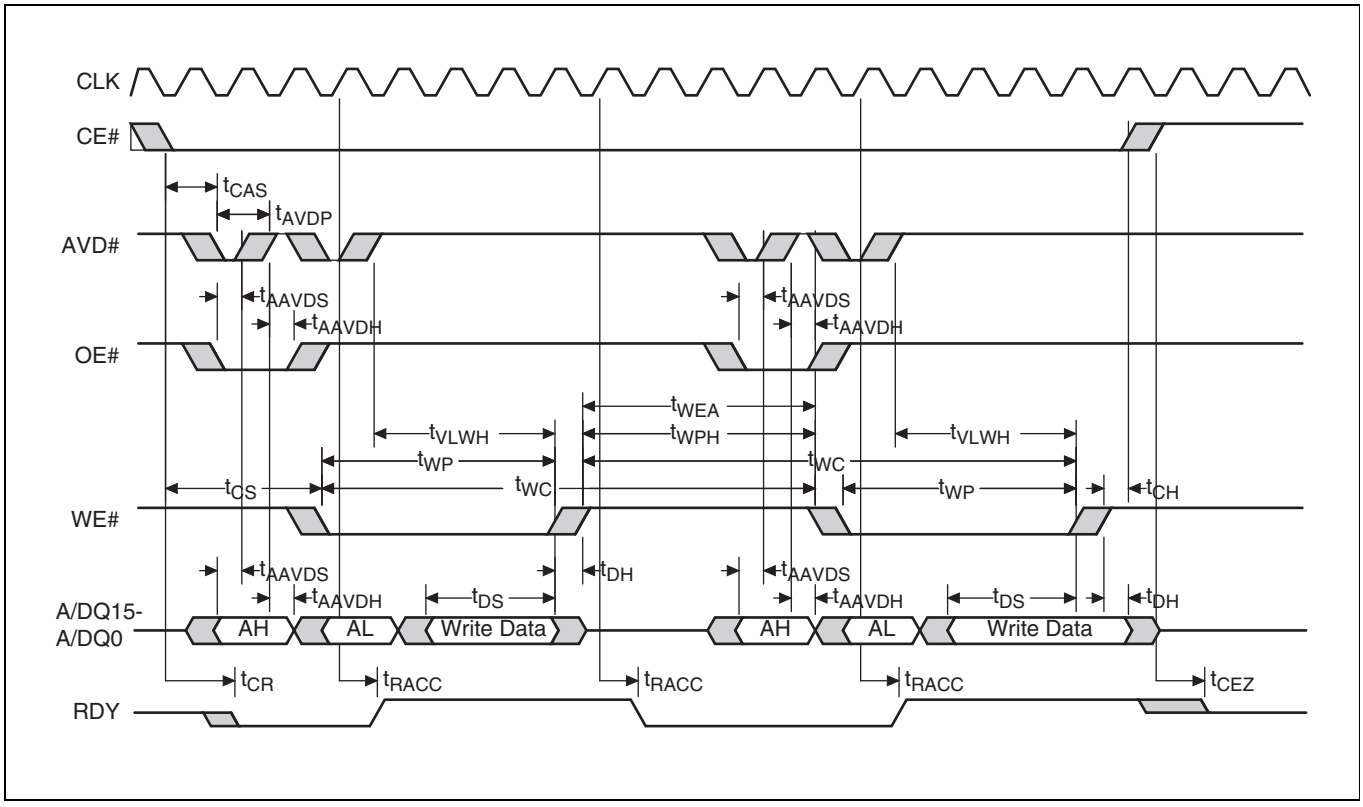


Figure 33 Synchronous write followed by write - AADM interface

Revision history

Document version	Date of release	Description of changes
**	2008-05-15	Initial release
*A	2008-08-01	**DC Characteristics** Changed some values in the CMOS Compatible table **Device ID and Common Flash Memory Interface Address Map** Changed some values in the ID/CFI Data table **Memory Address Map** Added memory address map
*B	2008-09-12	**Physical Dimensions/Connection Diagrams** Updated ball positions
*C	2009-03-10	**Blank Check Command** Functional in Asynchronous Read Mode only **DC Characteristics** Changed some ICCB values **Global** Added 108 MHz; removed 66 MHz
*D	2010-05-26	**Global** Modified document title **Features** Clarified some points **Ordering Information and Valid Combinations** Added Industrial Temperature range option **Address/Data Interface** Corrected typo **Device Bus Operations Table** Corrected A/DQ15-A/DQ0 column information for Asynchronous Read **Asynchronous Read** Clarified asynchronous read operation. **S29XS-R AADM Access** Clarified asynchronous AADM read access. **S29VS-R ADM Access** Standardized logic Low and High descriptions to VIL and VIH. Clarified wait states required by initial access and internal boundary crossings. **S29XS-R AADM Access** Standardized logic Low and High descriptions to VIL and VIH. Clarified wait states required by initial access and internal boundary crossings. **Writing Commands/Command Sequences** Clarified device behavior. **Program/Erase Operations** Removed redundant information. **Sector Lock Range Command** Clarified Sector Lock Range behavior **Figure Synchronous Read Mode** Added “ADM Interface” label **Figure Asynchronous Mode Read** Added “ADM Interface” label **Figure Asynchronous Program Operation Timings** Added “ADM Interface” label **Figure Back-to-Back Read/Write Cycle Timings** Added “ADM Interface” label **Figure Latency with Boundary Crossing** Corrected CR8 setting in Notes 1 and 2

Revision history

Document version	Date of release	Description of changes
*D (Cont.)	2010-05-26	**Figure Latency with Boundary Crossing into Bank Performing Embedded Operation** Corrected CR8 setting in Notes 1 and 2 **Figures Asynchronous Read - AADM Interface to Asynchronous Write Followed By Write - AADM Interface** Clarified CLK waveform behavior **Figure Synchronous Write Followed By Read Burst - AADM Interface** Corrected Figure title **ADM Interface (S29VS256R and S29VS128R)** Clarified traditional interface **Table Wait State vs. Frequency** Modified title and added note **Table Address Latency for 10–13 Wait States** Added note **Table Address Latency for 9 Wait States** Added note **Figure Synchronous Read** Removed note 1 **CLK Characterization** Removed note 2 **Erase and Programming Performance** Corrected note 2
*E	2010-07-22	**DC Characteristics** Changed ICC Read test conditions to OE#=H with relevant values **Performance Characteristics** Updated tables **Erase and Programming Performance** Changed typical programming times
*F	2010-11-18	**Erase and Programming Performance** Changed maximum chip erase times **ID/CFI Data** Corrected Data and Description for Word Offset 03h, 55h, 56h Corrected Data for Word Offset 1Dh, 1Eh, 52h
*G	2012-07-30	**Command Definitions** Corrected number of cycles for Write Buffer Load
*H	2015-12-17	Changed status from Advance to Final. Updated to the template.
*I	2017-02-16	Updated **"Electrical specifications"** on page 43: Updated **"V_{CC} power-up and power down"** on page 47: Added description. Added V_{RST}, t_{PD} parameters and their corresponding details in the table. Added **Figure 8** and **Figure 9**. Updated to new template.
*J	2017-11-15	Updated Logo and Copyright.
*K	2018-08-09	Updated to new template. Completing Sunset Review.

Revision history

Document version	Date of release	Description of changes
*L	2019-05-27	Updated **Package diagrams**: Updated **Special handling instructions for FBGA package**: Updated **Figure 20**: Removed existing spec. Added spec 002-24745 **. Updated to new template. Completing Sunset Review.
*M	2022-06-17	Updated **Table 9** Migrated to Infineon template

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