

DirectFET™ dual P-Channel Power MOSFET ②

Typical values (unless otherwise specified)

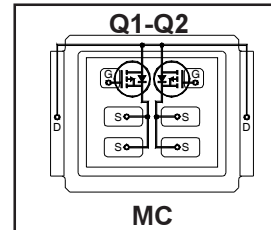
V_{DSS}	V_{GS}	$R_{DS(on)}$		$R_{DS(on)}$	
-30V max	±20V max	5.3mΩ@-10V		9.0mΩ@-4.5V	
$Q_{g\ tot}$	Q_{gd}	Q_{gs2}	Q_{rr}	Q_{oss}	$V_{gs(th)}$
32nC	15nC	3.2nC	62nC	23nC	-1.8V

Applications

- Isolation Switch for Input Power or Battery Application

Features and Benefits

- Environmentally Friendly Product
- RoHs Compliant Containing no Lead, no Bromide and no Halogen
- Dual Common-Drain P-Channel MOSFETs Provides High Level of Integration and Very Low $R_{DS(on)}$



Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details)①

SQ	SX	ST		MQ	MX	MT	MP	MC		
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Description

The IRF9395MTRPbF combines the latest HEXFET® P-Channel Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of a SO-8 and only 0.6 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRF9395MTRPbF	DirectFET Medium Can	Tape and Reel	4800	"TR" suffix
IRF9395MTR1PbF	DirectFET Medium Can	Tape and Reel	1000	"TR1" suffix EOL notice # 264

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	-30	V
V_{GS}	Gate-to-Source Voltage	±20	V
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ③	-14	A
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ③	-11	A
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ④	-75	A
I_{DM}	Pulsed Drain Current ⑤	-110	A

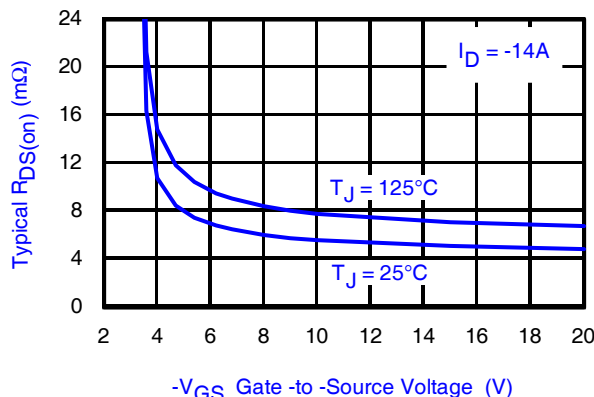


Fig 1. Typical On-Resistance vs. Gate Voltage

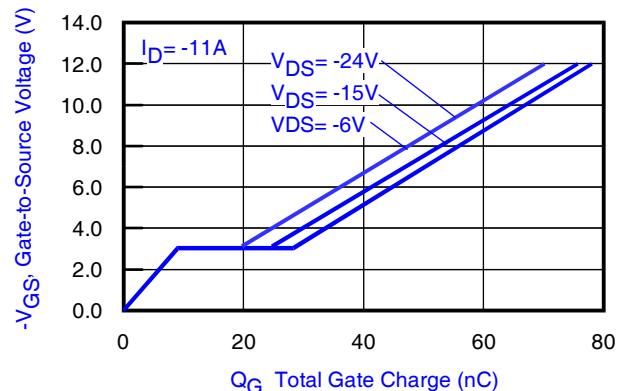


Fig 2. Typical Total Gate Charge vs. Gate-to-Source Voltage

Notes:

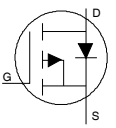
- Click on this section to link to the appropriate technical paper.
- Click on this section to link to the DirectFET Website.
- Surface mounted on 1 in. square Cu board, steady state.

- T_C measured with thermocouple mounted to top (Drain) of part.
- Repetitive rating; pulse width limited by max. junction temperature.

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-30	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.012	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = -1.0\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	5.3	7.0	$\text{m}\Omega$	$V_{GS} = -10V, I_D = -14A$ ⑥
		—	9.0	11.9		$V_{GS} = -4.5V, I_D = -11A$ ⑥
$V_{GS(th)}$	Gate Threshold Voltage	-1.3	-1.8	-2.4	V	$V_{DS} = V_{GS}, I_D = -50\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-6.1	—	$\text{mV}/^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	-1.0	μA	$V_{DS} = -24V, V_{GS} = 0V$
		—	—	-150		$V_{DS} = -24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$
g_{fs}	Forward Transconductance	40	—	—	S	$V_{DS} = -15V, I_D = -11A$
Q_g	Total Gate Charge	—	64	—	nC	$V_{DS} = -15V, V_{GS} = -10V, I_D = -11A$ $V_{DS} = -15V$ $V_{GS} = -4.5V$ $I_D = -11A$ See Fig.15
Q_g	Total Gate Charge	—	32	—		
Q_{gs1}	Pre- V_{th} Gate-to-Source Charge	—	6.5	—		
Q_{gs2}	Post - V_{th} Gate-to-Source Charge	—	3.2	—		
Q_{gd}	Gate-to-Drain Charge	—	15	—		
Q_{godr}	Gate Charge Overdrive	—	7.3	—		
Q_{sw}	Switch charge ($Q_{gs2} + Q_{gd}$)	—	18.2	—		
Q_{oss}	Output Charge	—	23	—	nC	$V_{DS} = -16V, V_{GS} = 0V$
R_G	Gate Resistance	—	15	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	$V_{DD} = -15V, V_{GS} = -4.5V$ ⑥ $I_D = -11A$ $R_G = 1.8\Omega$ See Fig.17
t_r	Rise Time	—	142	—		
$t_{d(off)}$	Turn-Off Delay Time	—	76	—		
t_f	Fall Time	—	121	—		
C_{iss}	Input Capacitance	—	3241	—	pF	$V_{GS} = 0V$ $V_{DS} = -15V$ $f = 1.0\text{KHz}$
C_{oss}	Output Capacitance	—	820	—		
C_{rss}	Reverse Transfer Capacitance	—	466	—		

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-57	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ⑤	—	—	-110		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}, I_S = -11A, V_{GS} = 0V$ ⑥
t_{rr}	Reverse Recovery Time	—	43	65	ns	$T_J = 25^\circ\text{C}, I_F = -11A, V_{DD} = -15V$
Q_{rr}	Reverse Recovery Charge	—	62	93	nC	$di/dt = 260A/\mu s$ ⑥

Notes:

 ⑤ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

Absolute Maximum Ratings

	Parameter	Max.	Units
P_D @ $T_A = 25^\circ\text{C}$	Power Dissipation ③	2.1	W
P_D @ $T_A = 70^\circ\text{C}$	Power Dissipation ③	1.3	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation ④	57	
T_P	Peak Soldering Temperature	270	$^\circ\text{C}$
T_J	Operating Junction and	-40 to + 150	
T_{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③	—	60	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient ⑦	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑧	20	—	
$R_{\theta JC}$	Junction-to-Case ④,⑨	—	2.2	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	1.0	—	
	Linear Derating Factor ③	0.02		W/ $^\circ\text{C}$

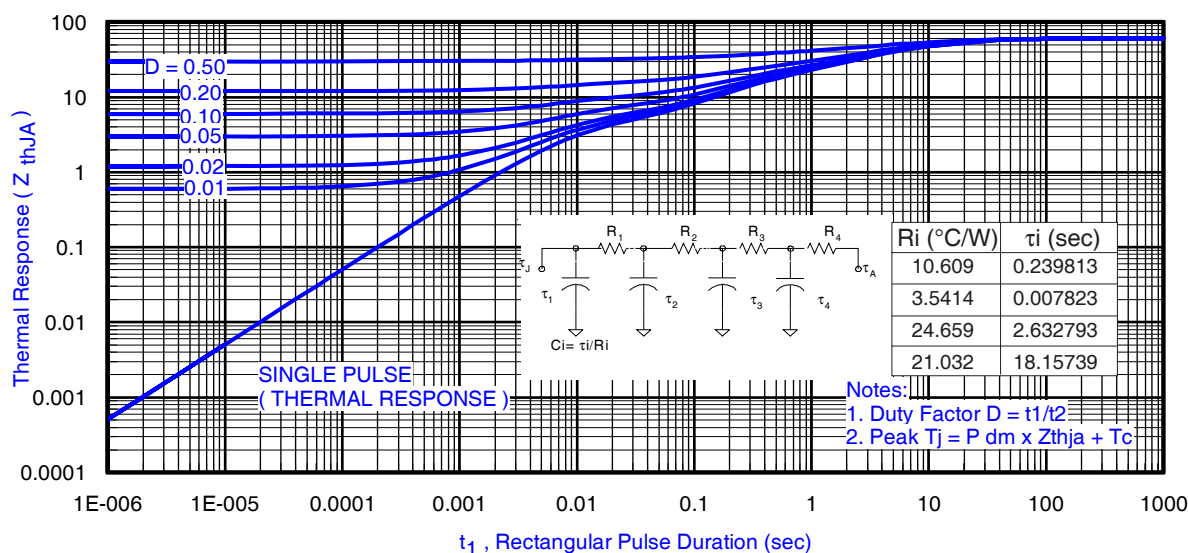
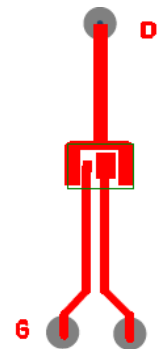
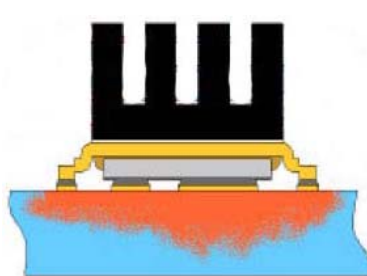
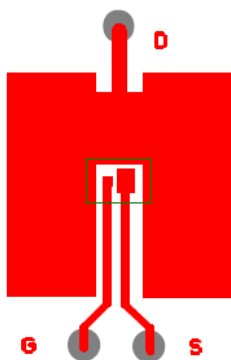


Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient ①

Notes:

- ⑦ Used double sided cooling, mounting pad with large heatsink.
 ⑧ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.

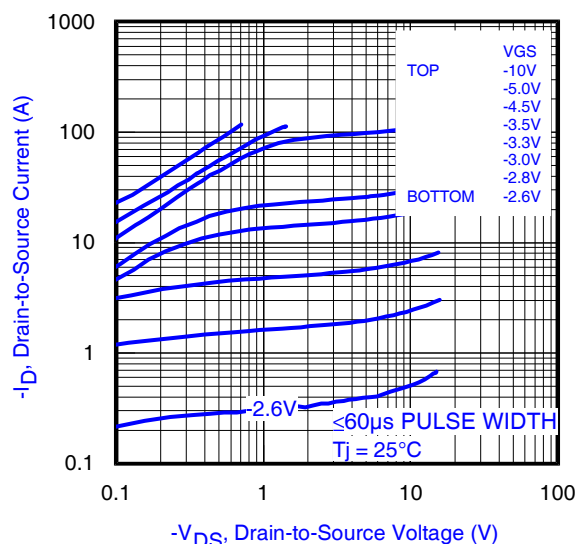
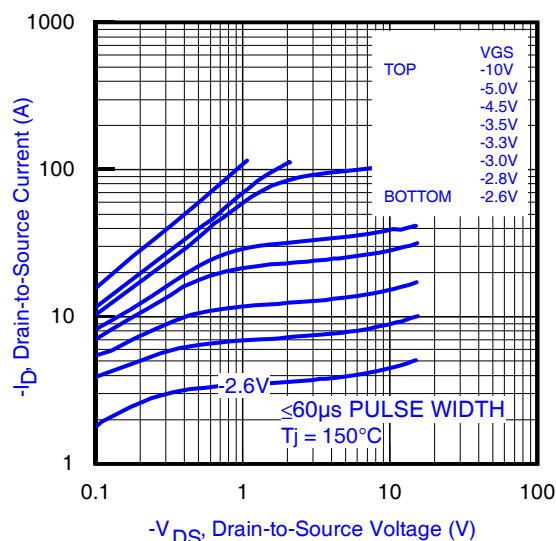
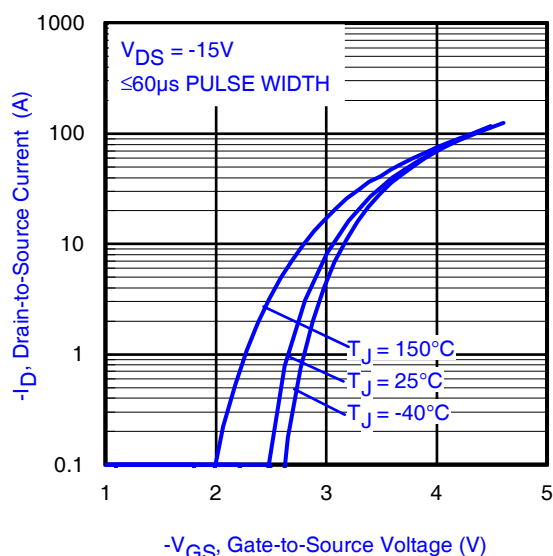
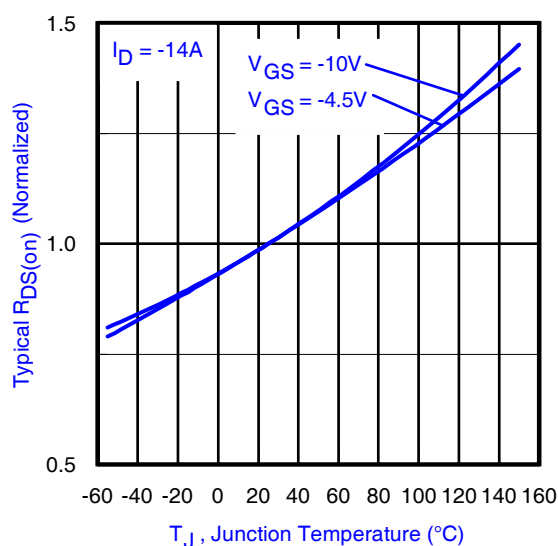
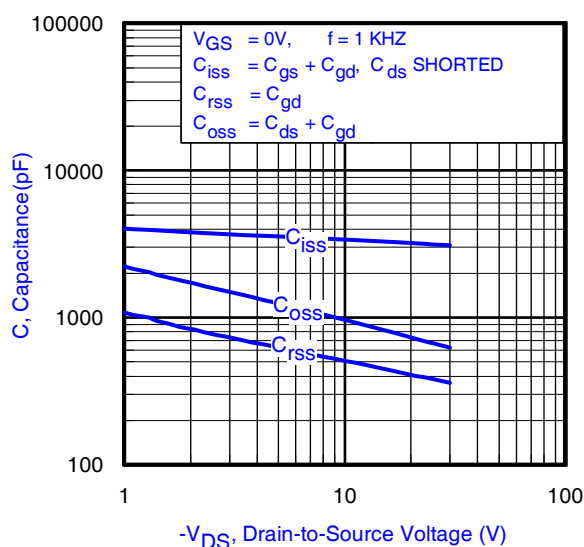
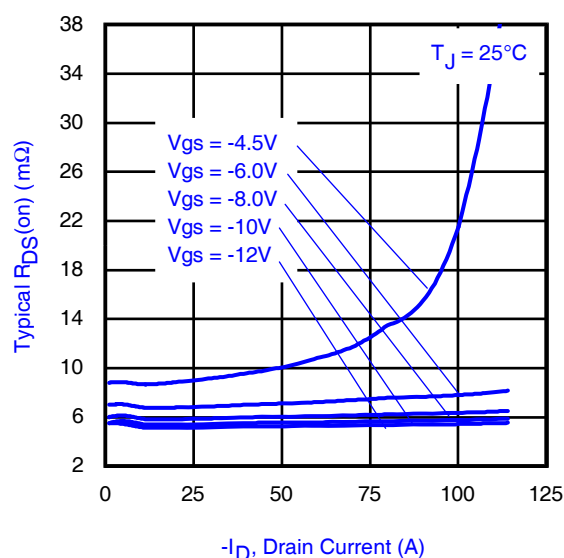
⑨ R_θ is measured at T_J of approximately 90°C .

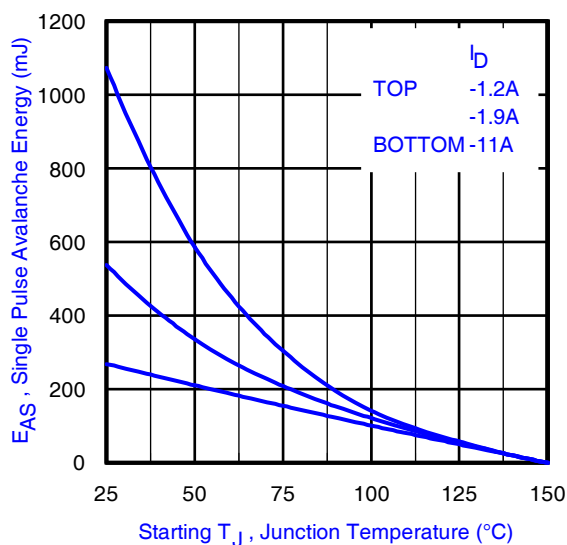
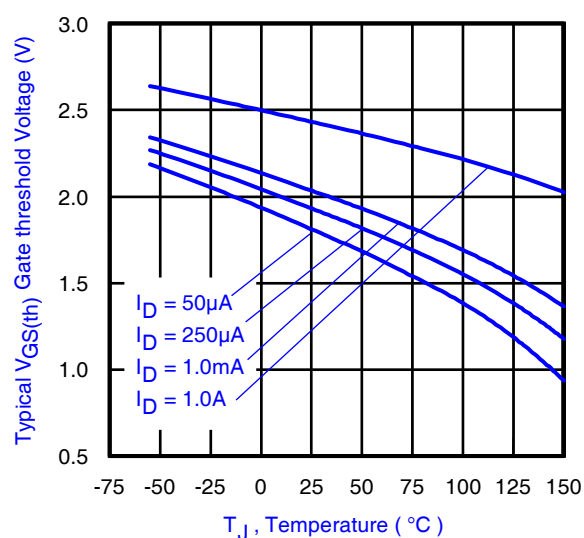
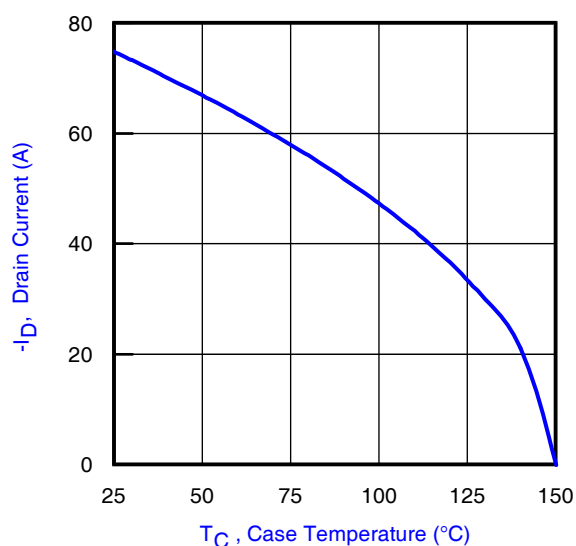
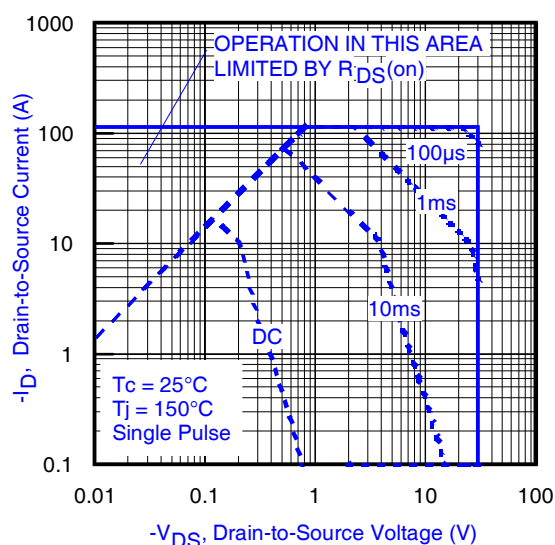
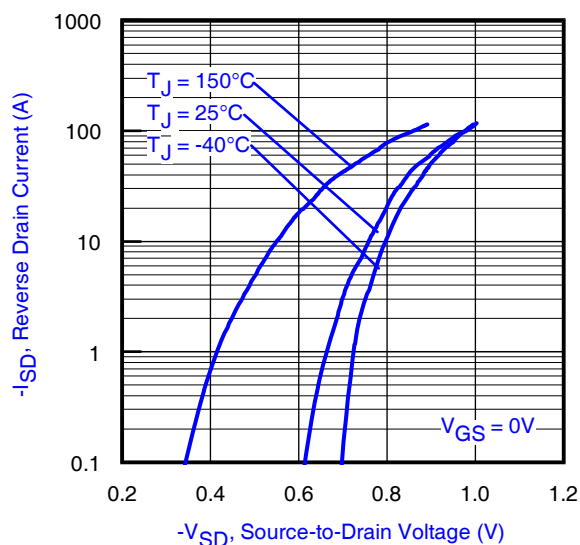


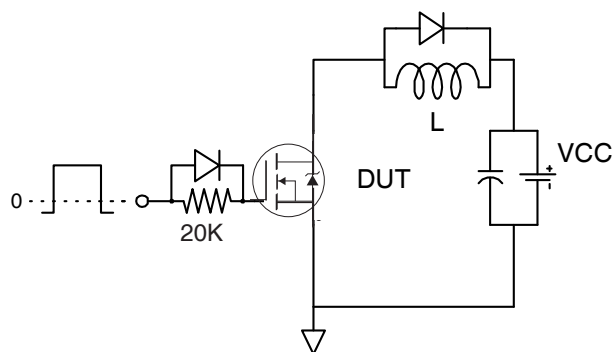
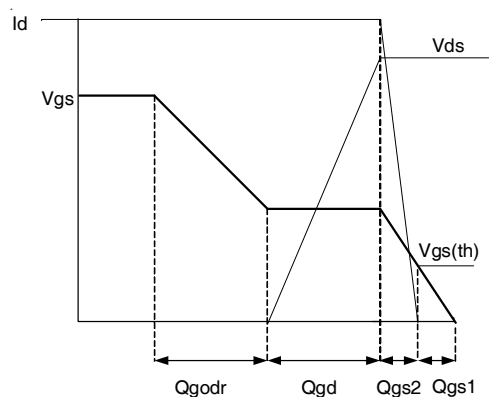
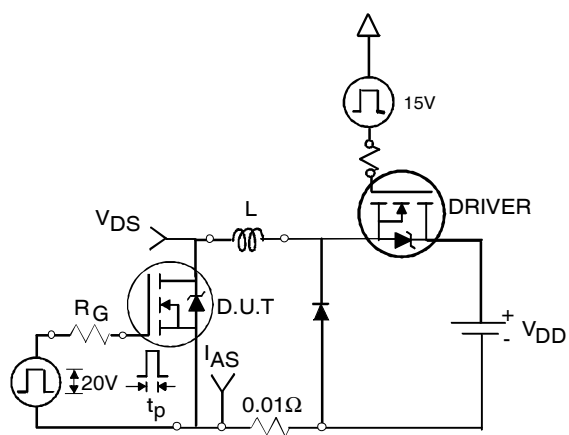
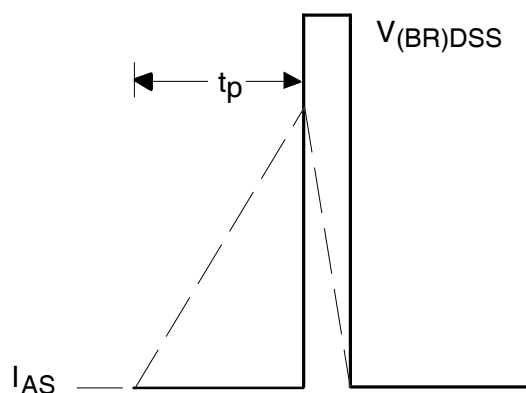
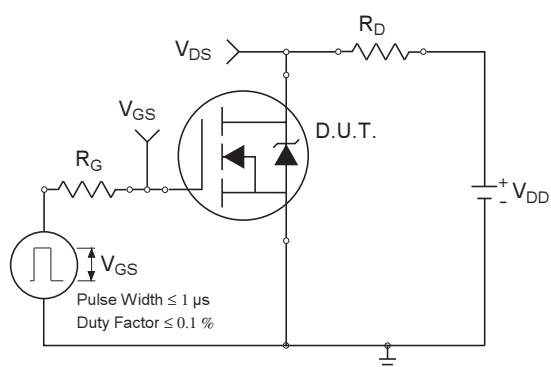
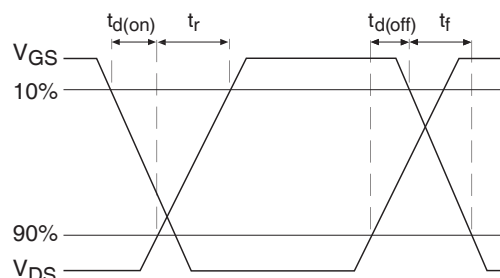
③ Surface mounted on 1 in. square Cu board (still air).

⑧ Mounted to a PCB with small clip heatsink (still air)

⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)


Fig 4. Typical Output Characteristics

Fig 5. Typical Output Characteristics

Fig 6. Typical Transfer Characteristics

Fig 7. Normalized On-Resistance vs. Temperature

Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

Fig 9. Typical On-Resistance vs. Drain Current and Gate Voltage




Fig 15a. Gate Charge Test Circuit

Fig 15b. Gate Charge Waveform

Fig 16a. Unclamped Inductive Test Circuit

Fig 16b. Unclamped Inductive Waveforms

Fig 17a. Switching Time Test Circuit

Fig 17b. Switching Time Waveforms

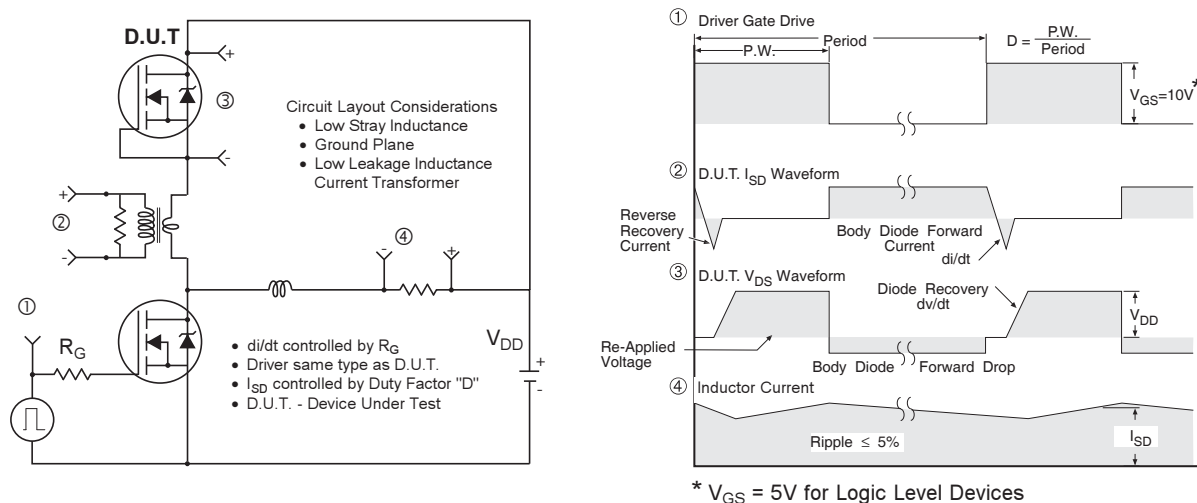
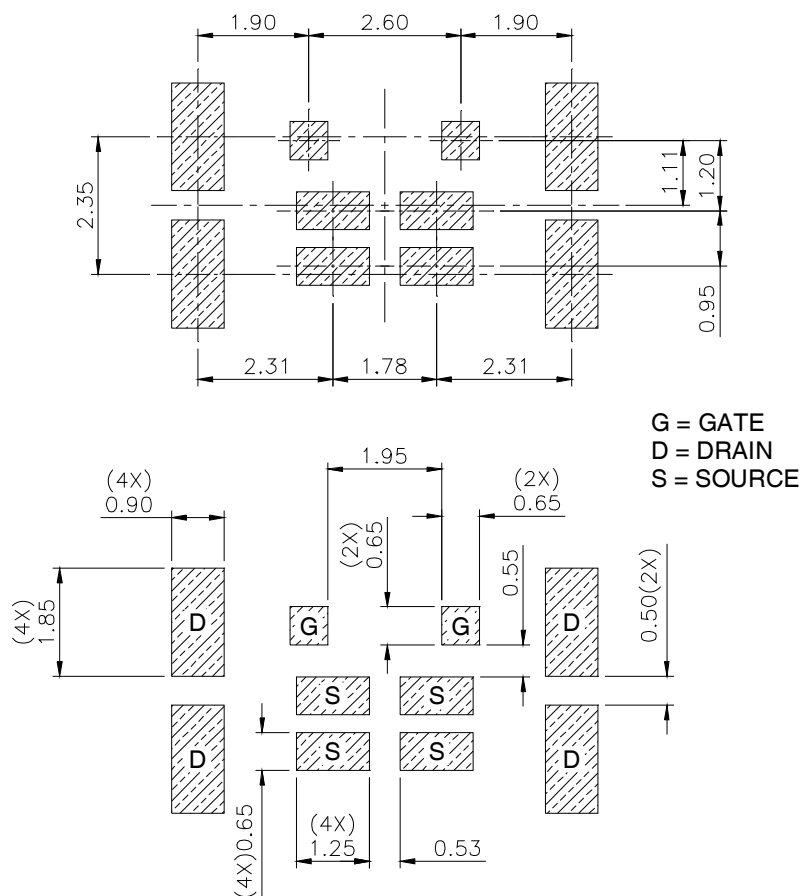


Fig 18. Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs

DirectFET™ Board Footprint, MC Outline (Medium Size Can, C-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET.

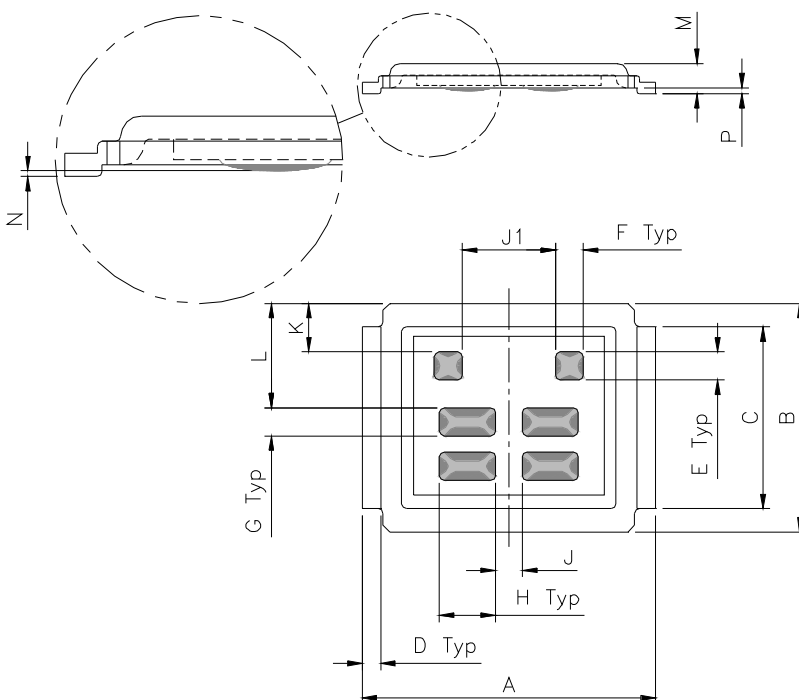
This includes all recommendations for stencil and substrate designs.



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

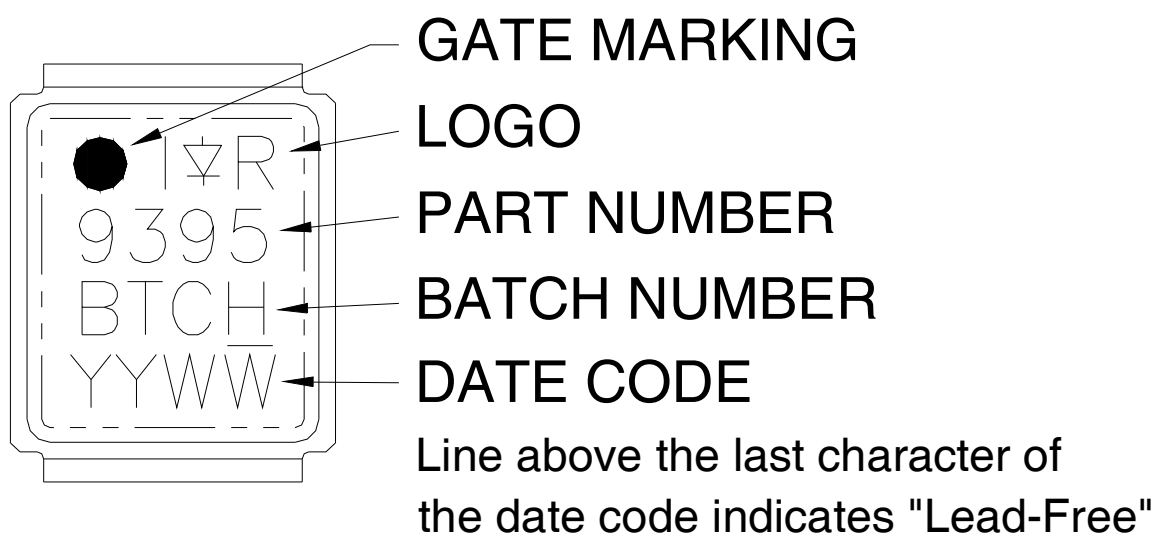
DirectFET™ Outline Dimension, MC Outline (Medium Size Can, C-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



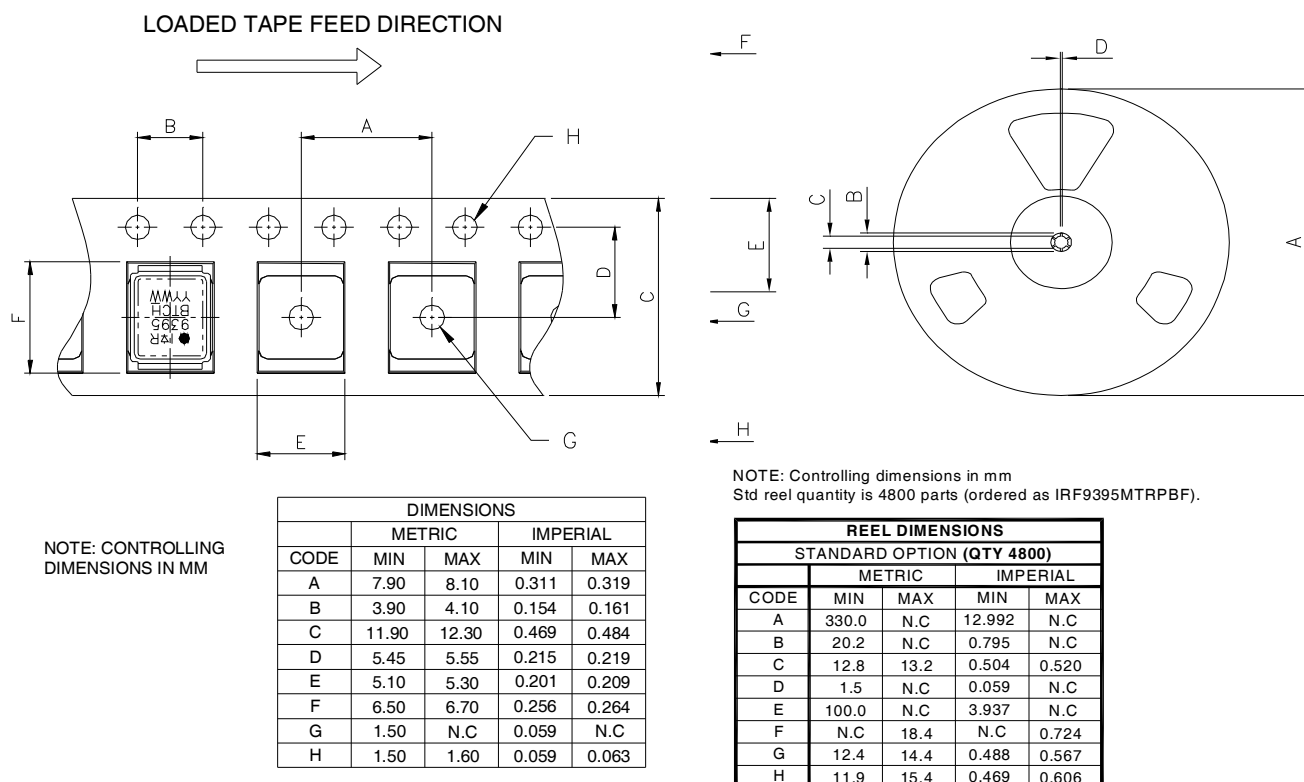
DIMENSIONS				
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.201
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.58	0.62	0.023	0.024
F	0.58	0.62	0.023	0.024
G	0.58	0.62	0.023	0.024
H	1.18	1.22	0.047	0.048
J	0.56	0.60	0.022	0.023
J1	1.98	2.02	0.078	0.079
K	1.02	1.06	0.040	0.041
L	2.22	2.26	0.088	0.089
M	0.59	0.70	0.023	0.028
N	0.03	0.08	0.001	0.003
P	0.08	0.17	0.003	0.007

DirectFET™ Part Marking



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

DirectFET™ Tape & Reel Dimension (Showing component orientation).



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Qualification Information†

Qualification level	Industrial†	
	(per JEDEC JESD47F†† guidelines)	
Moisture Sensitivity Level	DirectFET	MSL1 (per JEDEC J-STD-020D††)
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
10/25/2013	- Updated Qualification level from "Consumer" to "Industrial" on page 9 - Updated data sheet with new IR corporate template
2/24/2014	Updated ordering information to reflect the End-Of-life (EOL) of the mini-reel option (EOL notice #264)

International
 Rectifier

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To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>

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