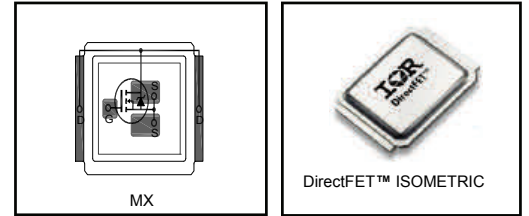


HEXFET® Power MOSFET plus Schottky Diode^②
Typical values (unless otherwise specified)

- [RoHs Compliant Containing No Lead and Bromide](#) ^②
- Integrated Monolithic Schottky Diode
- Low Profile (<0.7 mm)
- [Dual Sided Cooling Compatible](#) ^①
- Low Package Inductance
- Optimized for High Frequency Switching
- Ideal for CPU Core DC-DC Converters
- Optimized for Sync. FET socket of Sync. Buck Converter
- Low Conduction and Switching Losses
- [Compatible with existing Surface Mount Techniques](#) ^①
- 100% Rg tested
- Footprint compatible to DirectFET

V _{DSS}		V _{GS}		R _{DS(on)}		R _{DS(on)}	
25V min		±16V max		0.8mΩ @ 10V		1.2mΩ @ 4.5V	
Q _{g tot}	Q _{gd}	Q _{gs2}	Q _{rr}	Q _{oss}	V _{gs(th)}		
45nC	15nC	5.5nC	75nC	48nC	1.6V		



[Applicable DirectFET™ Outline and Substrate Outline \(see p.7,8 for details\)](#) ^①

SQ	SX	ST		MQ	MX	MT	MP			
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Description

The IRF6898MPbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of a SO-8 and only 0.7 mm profile. The DirectFET™ package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques. Application note [AN-1035](#) is followed regarding the manufacturing methods and processes. The DirectFET™ package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

The IRF6894MPbF balances industry leading on-state resistance while minimizing gate charge along with low gate resistance to reduce both conduction and switching losses. This part contains an integrated Schottky diode to reduce the Qrr of the body drain diode further reducing the losses in a Synchronous Buck circuit. The reduced losses make this product ideal for high frequency/high efficiency DC-DC converters that power high current loads such as the latest generation of microprocessors. The IRF6898MPbF has been optimized for parameters that are critical in synchronous buck converter's Sync FET sockets.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF6898MPbF	DirectFET® Medium Can	Tape and Reel	4800	IRF6898MTRPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
V _{DS}	Drain-to-Source Voltage	25	V
V _{GS}	Gate-to-Source Voltage	±16	
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited) ^④	40	A
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited) ^④	32	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited) ^③	214	
I _{DM}	Pulsed Drain Current ^⑤	320	
E _{AS}	Single Pulse Avalanche Energy ^⑥	537	mJ
I _{AR}	Avalanche Current ^⑥	32	A

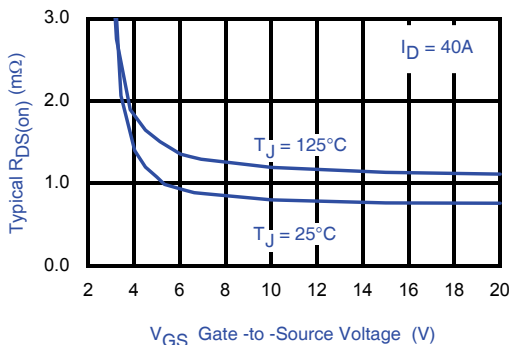


Fig 1. Typical On-Resistance vs. Gate Voltage

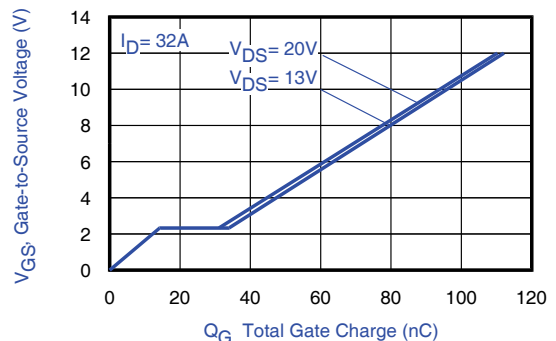


Fig 2. Typical Total Gate Charge vs. Gate-to-Source Voltage

Notes

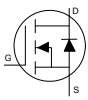
- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET™ Website.
- ③ Surface mounted on 1 in. square Cu board, steady state.

- ④ TC measured with thermocouple mounted to top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑥ Starting T_J = 25°C, L = 1.1mH, R_G = 50Ω, I_{AS} = 32A.

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	25	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.02	—	V/°C	I _D = 10mA (25°C-125°C)
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	0.8	1.1	mΩ	V _{GS} = 10V, I _D = 40A ⑦
		—	1.2	1.6		V _{GS} = 4.5V, I _D = 32A ⑦
V _{GS(th)}	Gate Threshold Voltage	1.1	1.6	2.1	V	V _{DS} = V _{GS} , I _D = 100μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Temp. Coefficient	—	-4.1	—	mV/°C	V _{DS} = V _{GS} , I _D = 10mA
I _{DSS}	Drain-to-Source Leakage Current	—	—	500	μA	V _{DS} = 20 V, V _{GS} = 0V
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -16V
g _{fs}	Forward Transconductance	188	—	—	S	V _{DS} = 13V, I _D = 32A
Q _g	Total Gate Charge	—	45	68	nC	V _{DS} = 13V V _{GS} = 4.5V I _D = 32A See Fig 15
Q _{gs1}	Pre- V _{th} Gate-to-Source Charge	—	11	—		
Q _{gs2}	Post- V _{th} Gate-to-Source Charge	—	5.5	—		
Q _{gd}	Gate-to-Drain Charge	—	15	—		
Q _{godr}	Gate Charge Overdrive	—	13.5	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	20.5	—		
Q _{oss}	Output Charge	—	48	—	nC	V _{DS} = 16V, V _{GS} = 0V
R _G	Gate Resistance	—	0.2	—	Ω	
t _{d(on)}	Turn-On Delay Time	—	21	—	ns	V _{DD} = 13V, V _{GS} = 4.5V ⑦ I _D = 32A R _G = 1.8Ω See Fig 17
t _r	Rise Time	—	55	—		
t _{d(off)}	Turn-Off Delay Time	—	28	—		
t _f	Fall Time	—	16	—		
C _{iss}	Input Capacitance	—	5630	—	pF	V _{GS} = 0V V _{DS} = 13V f = 1.0MHz
C _{oss}	Output Capacitance	—	1770	—		
C _{rss}	Reverse Transfer Capacitance	—	400	—		

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	40	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ⑤	—	—	320		
V _{SD}	Diode Forward Voltage	—	—	0.75	V	T _J = 25°C, I _S = 32A, V _{GS} = 0V ⑦
t _{rr}	Reverse Recovery Time	—	34	51	ns	T _J = 25°C, I _F = 32A
Q _{rr}	Reverse Recovery Charge	—	75	112	nC	di/dt = 320A/μs ⑦

Notes:

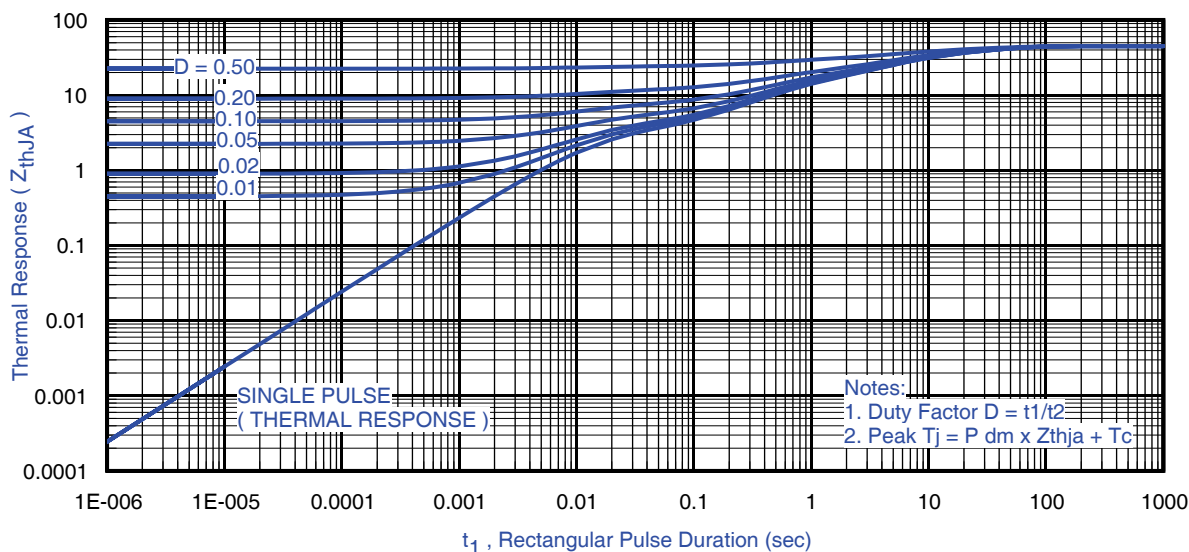
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑦ Pulse width ≤ 400μs; duty cycle ≤ 2%.

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation ③④	2.8	W
$P_D @ T_A = 70^\circ\text{C}$	Power Dissipation ③④	1.8	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ④	78	
T_P	Peak Soldering Temperature	270	$^\circ\text{C}$
T_J	Operating Junction and	-40 to + 150	
T_{STG}	Storage Temperature Range		

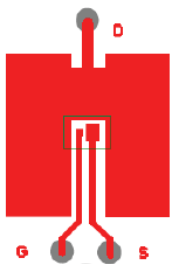
Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③	—	45	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient ⑧	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑨	20	—	
$R_{\theta JC}$	Junction-to-Can ④⑩	—	1.6	
$R_{\theta JA-PCB}$	Junction-to-PCB Mounted	1.0	—	
	Linear Derating Factor ③	0.022		$\text{W}/^\circ\text{C}$

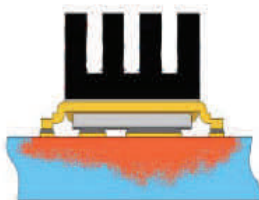

Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient③
Notes:

- ③ Surface mounted on 1 in. square Cu board, steady state.
- ④ T_C measured with thermocouple incontact with top (Drain) of part.

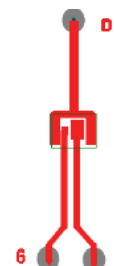
- ⑧ Used double sided cooling, mounting pad with large heatsink.
- ⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑩ R_{θ} is measured at T_J of approximately 90°C .



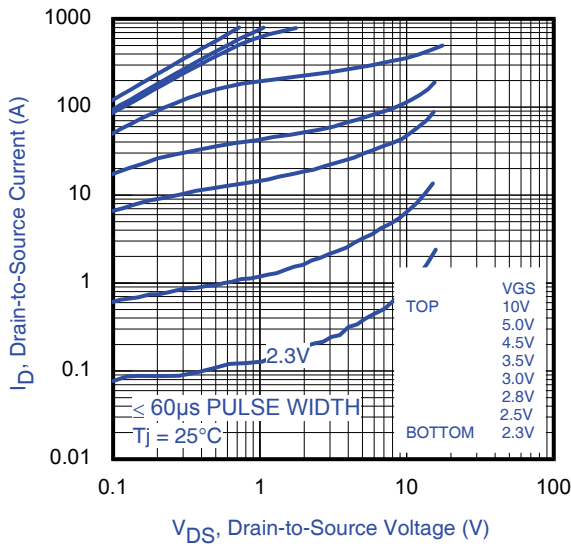
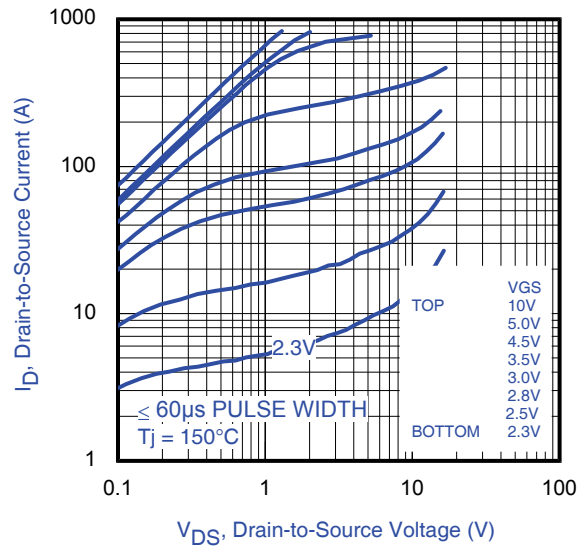
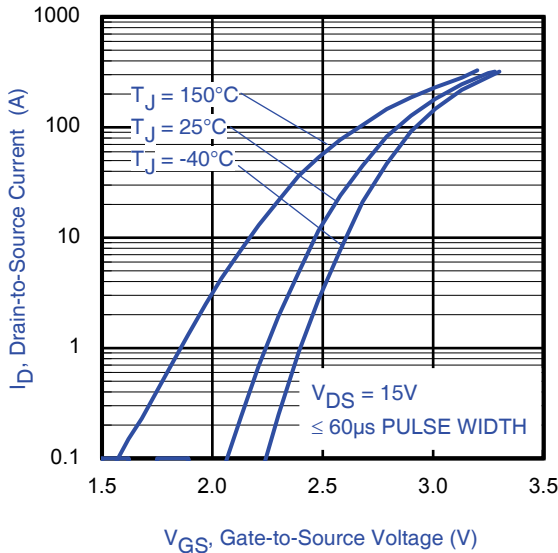
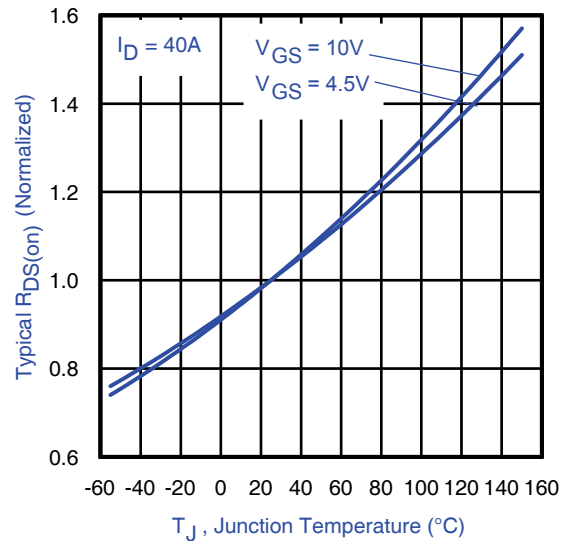
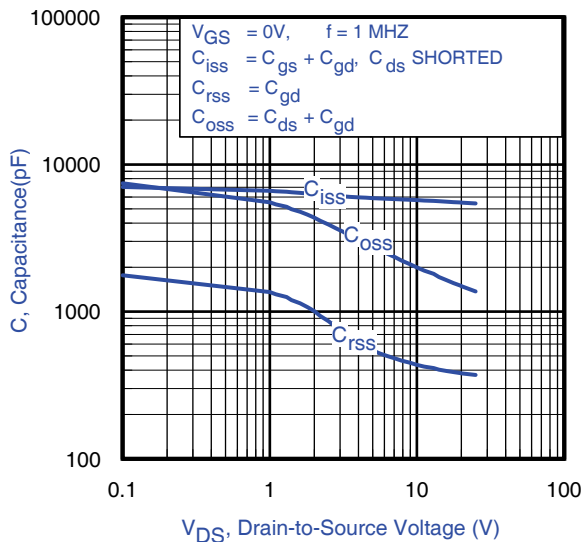
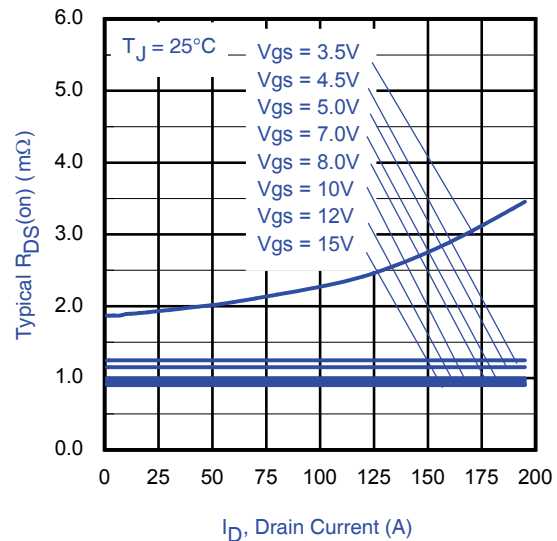
③ Surface mounted on 1 in. square Cu board (still air).



⑨ Mounted to a PCB with small clip heatsink (still air)



⑧ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)


Fig 4. Typical Output Characteristics

Fig 5. Typical Output Characteristics

Fig 6. Typical Transfer Characteristics

Fig 7. Normalized On-Resistance vs. Temperature

Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

Fig 9. Typical On-Resistance vs. Drain Current and Gate Voltage

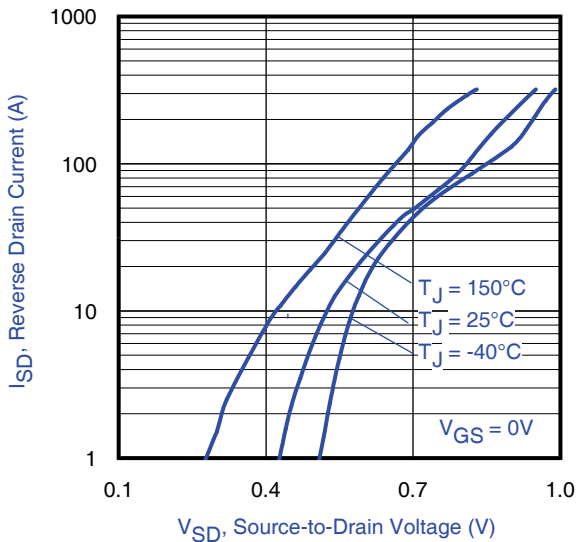


Fig 10. Typical Source-Drain Diode Forward Voltage

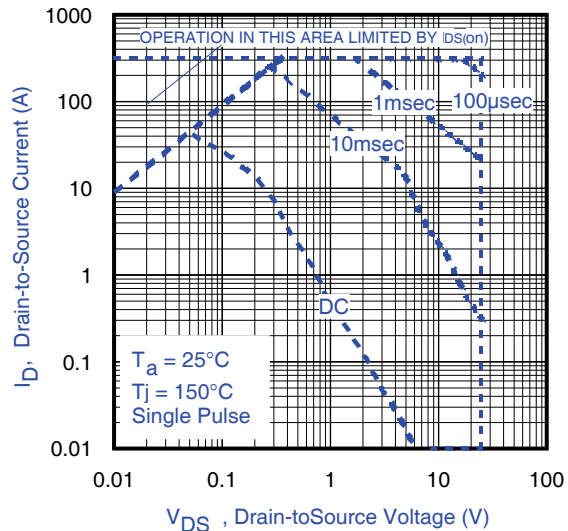


Fig 11. Maximum Safe Operating Area

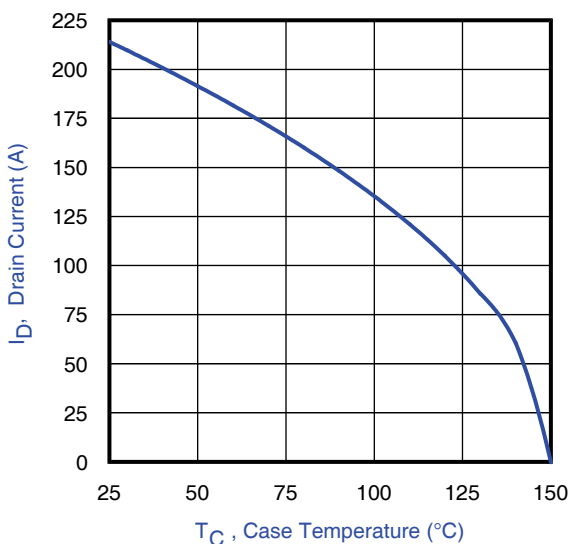


Fig 12. Maximum Drain Current vs. Case Temperature

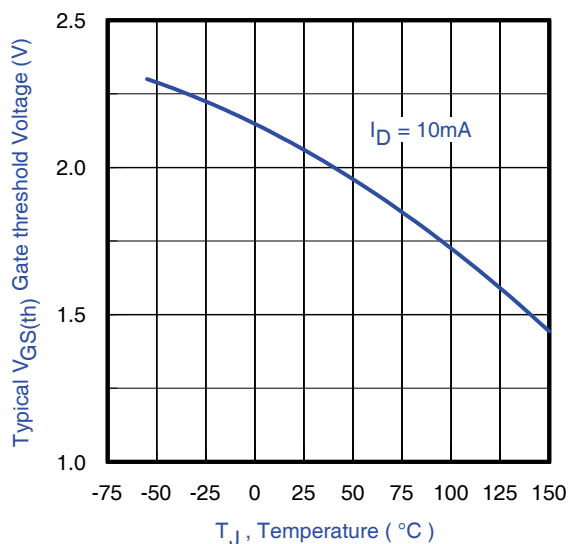


Fig 13. Typical Threshold Voltage vs. Junction Temperature

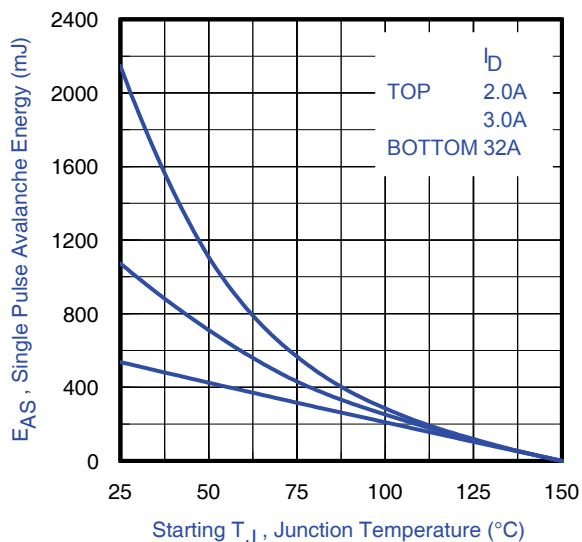


Fig 14. Maximum Avalanche Energy vs. Drain Current

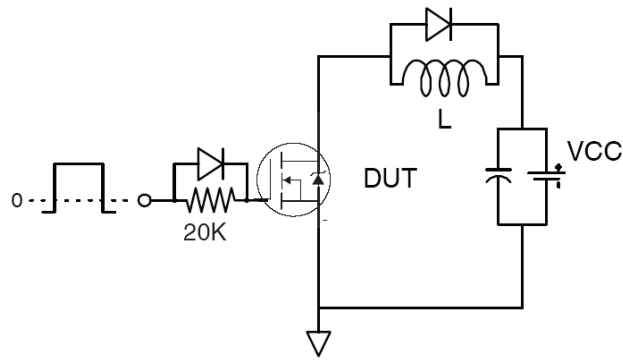


Fig 15a. Gate Charge Test Circuit

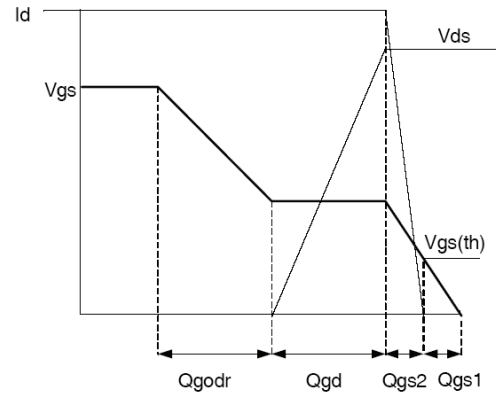


Fig 15b. Gate Charge Waveform

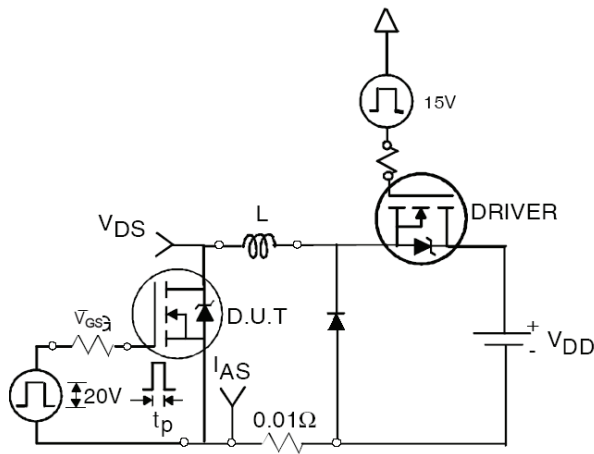


Fig 16a. Unclamped Inductive Test Circuit

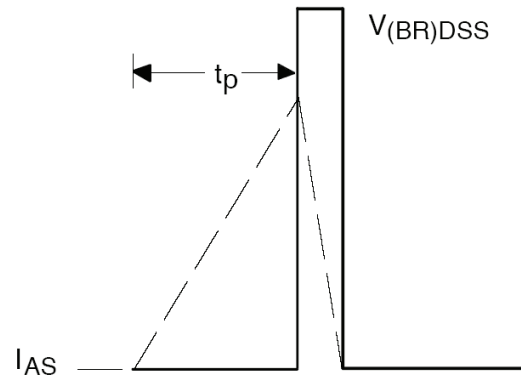


Fig 16b. Unclamped Inductive Waveforms

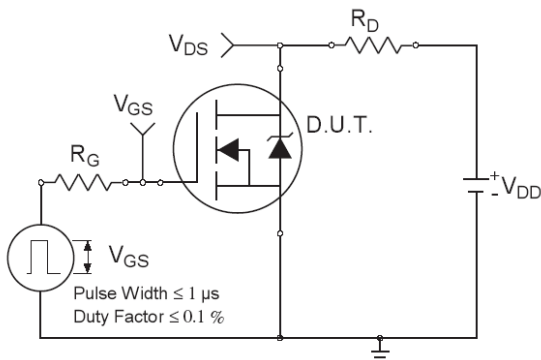


Fig 17a. Switching Time Test Circuit

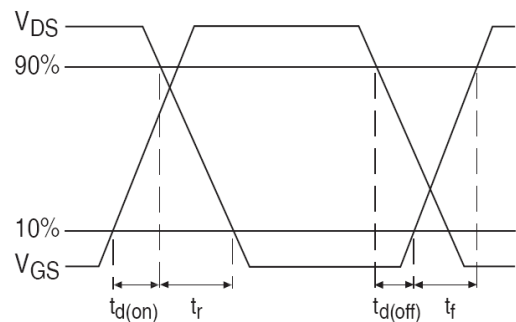


Fig 17b. Switching Time Waveforms

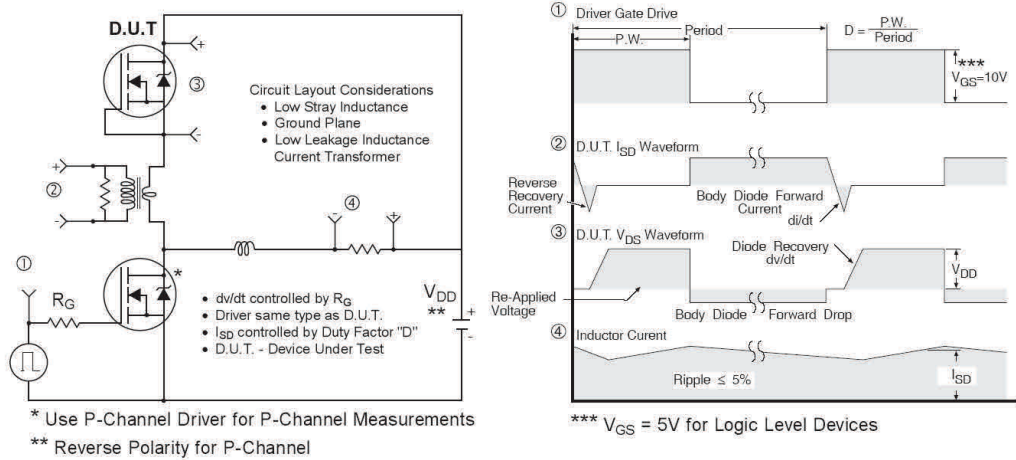
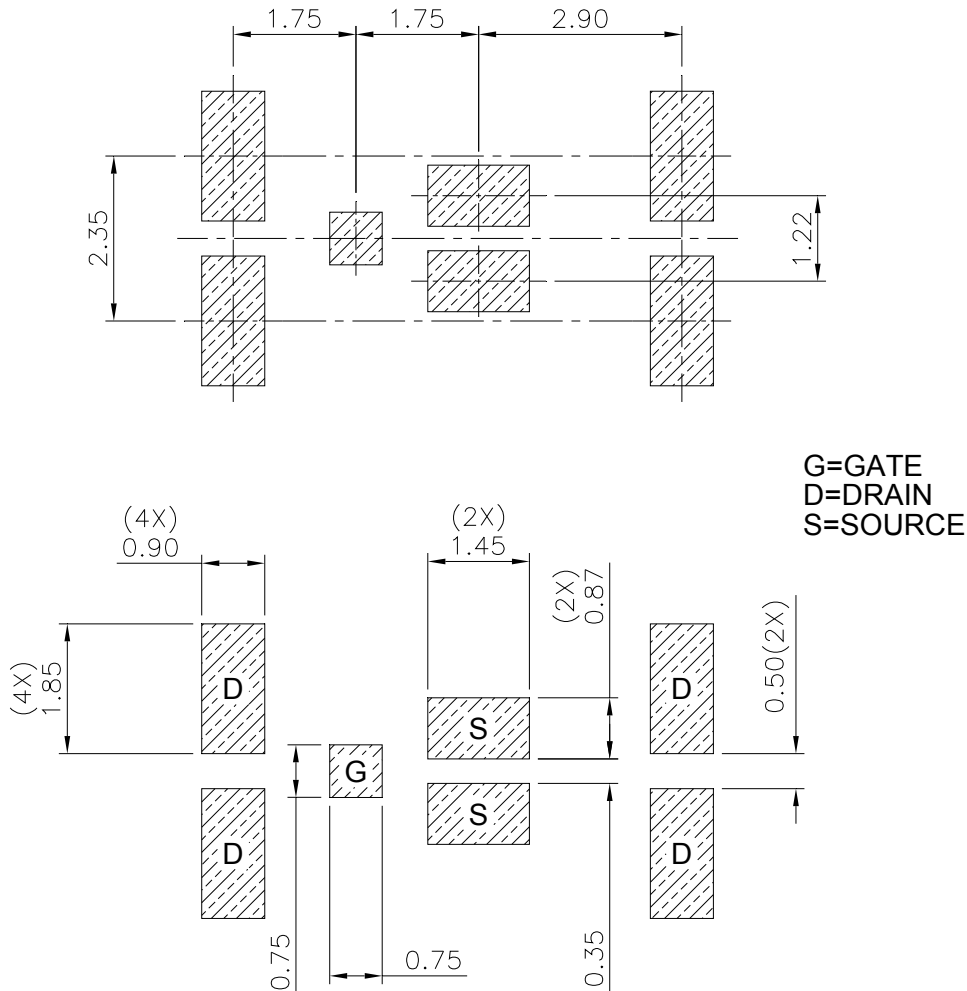


Fig 18. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs

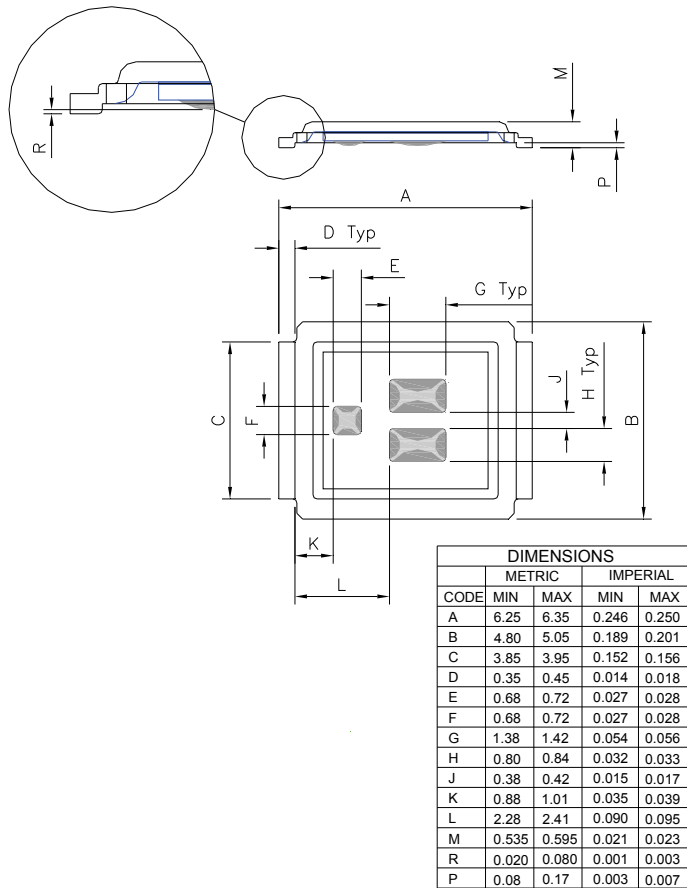
DirectFET™ Board Footprint, MX Outline (Medium Size Can, X-Designation).

Please see DirectFET™ application note [AN-1035](#) for all details regarding the assembly of DirectFET™. This includes all recommendations for stencil and substrate designs.

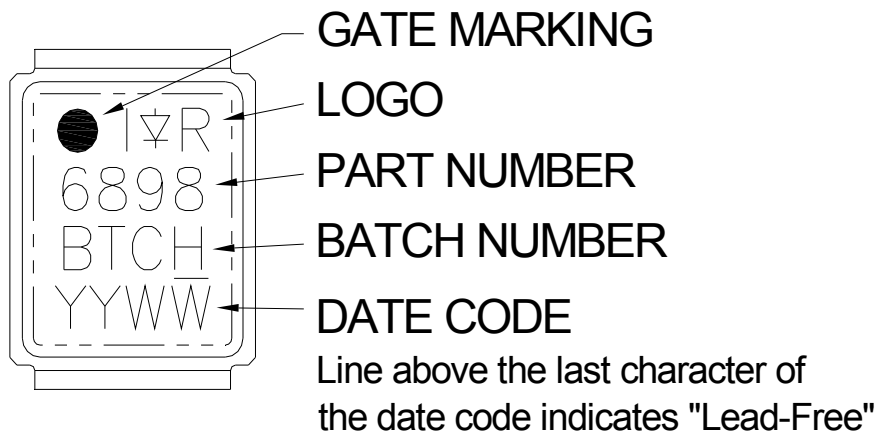


**DirectFET™ Outline Dimension, MX Outline
(Medium Size Can, X-Designation).**

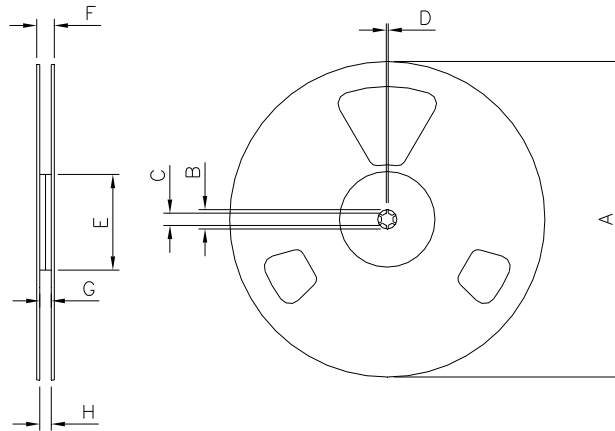
Please see DirectFET™ application note [AN-1035](#) for all details regarding the assembly of DirectFET™. This includes all recommendations for stencil and substrate designs.



DirectFET™ Part Marking



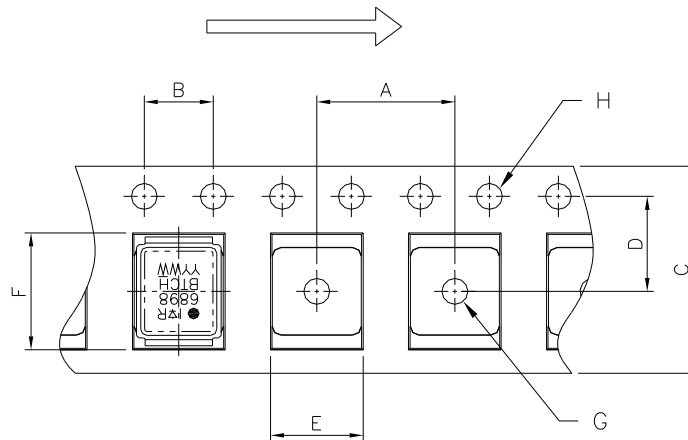
DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
 Std reel quantity is 4800 parts. (ordered as IRF6898MTRPbF). For 1000 parts on 7" reel, order IRF6898MTR1PbF

REEL DIMENSIONS								
CODE	STANDARD OPTION (QTY 4800)				TR1 OPTION (QTY 1000)			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C

LOADED TAPE FEED DIRECTION



NOTE: CONTROLLING DIMENSIONS IN MM

CODE	DIMENSIONS			
	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Qualification Information

Qualification Level	Industrial [†]	
Moisture Sensitivity Level	DirectFET™ Medium Can	MSL1 (per JEDEC J-STD-020D [†])
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comment
03/15/2013	<ul style="list-style-type: none"> • Updated header Qrr from 32nC to 66nC on page 1.
11/04/2019	<ul style="list-style-type: none"> • Changed datasheet with “Infineon” logo –all pages. • Changed Rth from “60°C/W” to “45°C/W” –page 3 • Changed ID @ TA 25C/70C from “35A/28A” to “40A/32A” –pages 1 & 2. • Changed Fig.1 to Fig.18 –pages 1 to 7. • Added disclaimer on last page.

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