# OptiMOS®-P2 Power-Transistor

**Product Summary**

| | | |
|---|---|---|
| $V_{DS}$ | -40 | V |
| $R_{DS(on)}$ (SMD Version) | 4.4 | mΩ |
| $I_D$ | -80 | A |

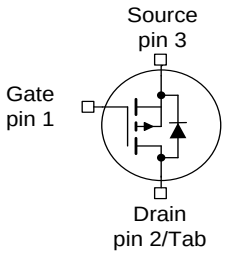
**Features**

- P-channel - Logic Level - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (RoHS compliant)
- 100% Avalanche tested

PG-TO263-3-2 PG-TO262-3-1 PG-TO220-3-1




| Type | Package | Marking |
|---|---|---|
| IPB80P04P4L-04 | PG-TO263-3-2 | 4P04L04 |
| IPI80P04P4L-04 | PG-TO262-3-1 | 4P04L04 |
| IPP80P04P4L-04 | PG-TO220-3-1 | 4P04L04 |




**Maximum ratings,** at $T_j$=25 °C, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| Continuous drain current[1] | $I_D$ | $T_C$=25°C, $V_{GS}$=-10V | -80 | A |
| | | $T_C$=100°C, $V_{GS}$=-10V[2] | -80 | |
| Pulsed drain current[2] | $I_{D,pulse}$ | $T_C$=25°C | -320 | |
| Avalanche energy, single pulse | $E_{AS}$ | $I_D$=-40A | 60 | mJ |
| Avalanche current, single pulse | $I_{AS}$ | - | -80 | A |
| Gate source voltage | $V_{GS}$ | - | +5/-16 | V |
| Power dissipation | $P_{tot}$ | $T_C$=25 °C | 125 | W |
| Operating and storage temperature | $T_j$, $T_{stg}$ | - | -55 ... +175 | °C |
| IEC climatic category; DIN IEC 68-1 | - | - | 55/175/56 | |

| Parameter | Symbol | Conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| **Thermal characteristics**[2] | | | | | | |
| Thermal resistance, junction - case | $R_{thJC}$ | - | - | - | 1.2 | K/W |
| Thermal resistance, junction - ambient, leaded | $R_{thJA}$ | - | - | - | 62 | |
| SMD version, device on PCB | $R_{thJA}$ | minimal footprint | - | - | 62 | |
| | | 6 $cm^2$ cooling area[3] | - | - | 40 | |
| **Electrical characteristics,** at $T_j$=25 °C, unless otherwise specified | | | | | | |
| **Static characteristics** | | | | | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}$=0V, $I_D$= -1mA | -40 | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$, $I_D$=-250µA | -1.2 | -1.7 | -2.2 | |
| Zero gate voltage drain current | $I_{DSS}$ | $V_{DS}$=-32V, $V_{GS}$=0V, $T_j$=25°C | - | -0.05 | -1 | µA |
| | | $V_{DS}$=-32V, $V_{GS}$=0V, $T_j$=125°C[2] | - | -20 | -200 | |
| Gate-source leakage current | $I_{GSS}$ | $V_{GS}$=-16V, $V_{DS}$=0V | - | - | -100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}$=-4.5V, $I_D$=-80A | - | 5.6 | 7.1 | mΩ |
| | | $V_{GS}$=-4.5V, $I_D$=-80A, SMD version | - | 5.3 | 6.8 | |
| | | $V_{GS}$=-10V, $I_D$=-80A | - | 4.1 | 4.7 | |
| | | $V_{GS}$=-10V, $I_D$=-80A, SMD version | - | 3.8 | 4.4 | |

| Parameter | Symbol | Conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| **Dynamic characteristics**[2] | | | | | | |
| Input capacitance | $C_{iss}$ | $V_{GS}$=0V, $V_{DS}$=-25V, $f$=1MHz | - | 8900 | 11570 | pF |
| Output capacitance | $C_{oss}$ | | - | 2533 | 3800 | |
| Reverse transfer capacitance | $C_{rss}$ | | - | 100 | 200 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$=-20V, $V_{GS}$=-10V, $I_D$=-80A, $R_G$=3.5Ω | - | 28 | - | ns |
| Rise time | $t_r$ | | - | 13 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 119 | - | |
| Fall time | $t_f$ | | - | 65 | - | |
| **Gate Charge Characteristics**[2] | | | | | | |
| Gate to source charge | $Q_{gs}$ | $V_{DD}$=-32V, $I_D$=-80A, $V_{GS}$=0 to -10V | - | 31 | 40 | nC |
| Gate to drain charge | $Q_{gd}$ | | - | 24 | 48 | |
| Gate charge total | $Q_g$ | | - | 135 | 176 | |
| Gate plateau voltage | $V_{plateau}$ | | - | 3.5 | - | V |
| **Reverse Diode** | | | | | | |
| Diode continous forward current[2] | $I_S$ | $T_C$=25°C | - | - | -80 | A |
| Diode pulse current[2] | $I_{S,pulse}$ | | - | - | -320 | |
| Diode forward voltage | $V_{SD}$ | $V_{GS}$=0V, $I_F$=-80A, $T_j$=25°C | - | -1 | -1.3 | V |
| Reverse recovery time[2] | $t_{rr}$ | $V_R$=-20V, $I_F$=-50A, $di_F/dt$=-100A/µs | - | 65 | - | ns |
| Reverse recovery charge[2] | $Q_{rr}$ | | - | 90 | - | nC |

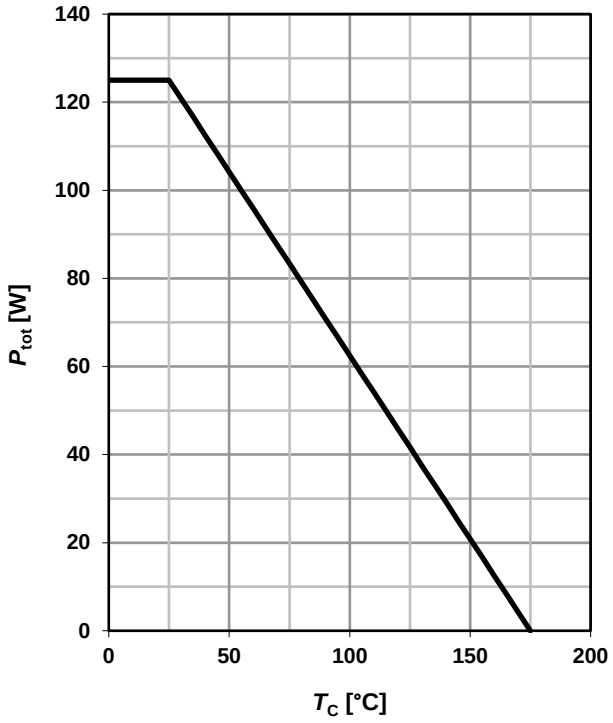
[1] Current is limited by bondwire; with an $R_{thJC}$ = 1.2K/W the chip is able to carry -137A at 25°C.

[2] Defined by design. Not subject to production test.

[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm$^2$ (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

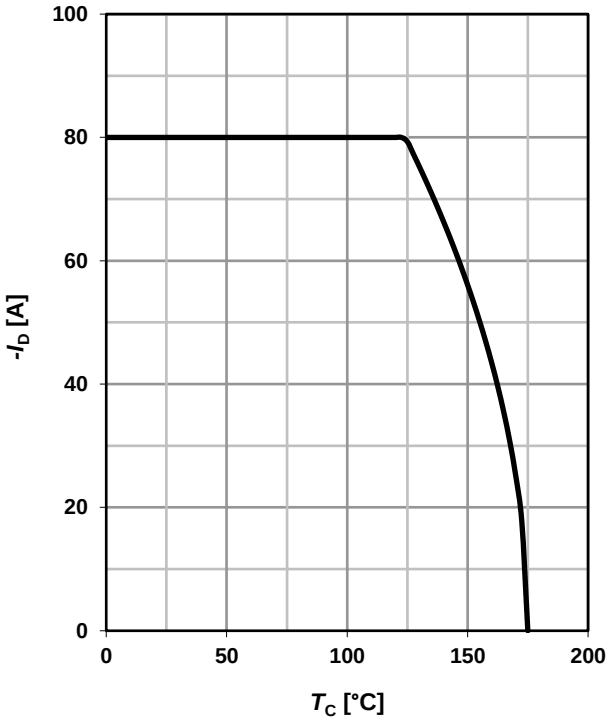
## 1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \leq -6V$




## 2 Drain current

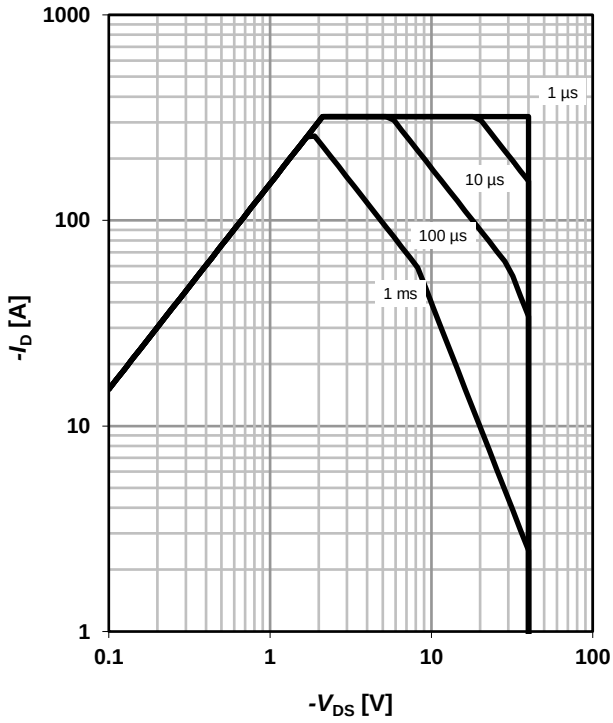
$I_D = f(T_C)$; $V_{GS} \leq -6V$; SMD




## 3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$; SMD

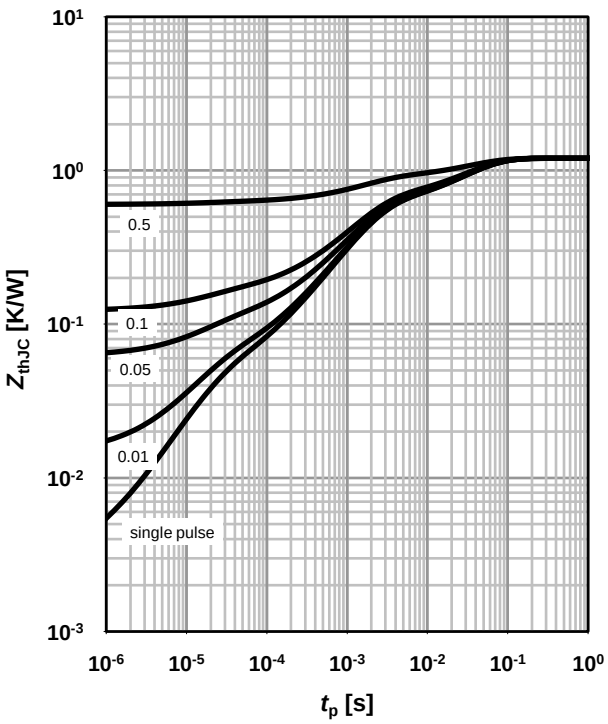
parameter: $t_p$




## 4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

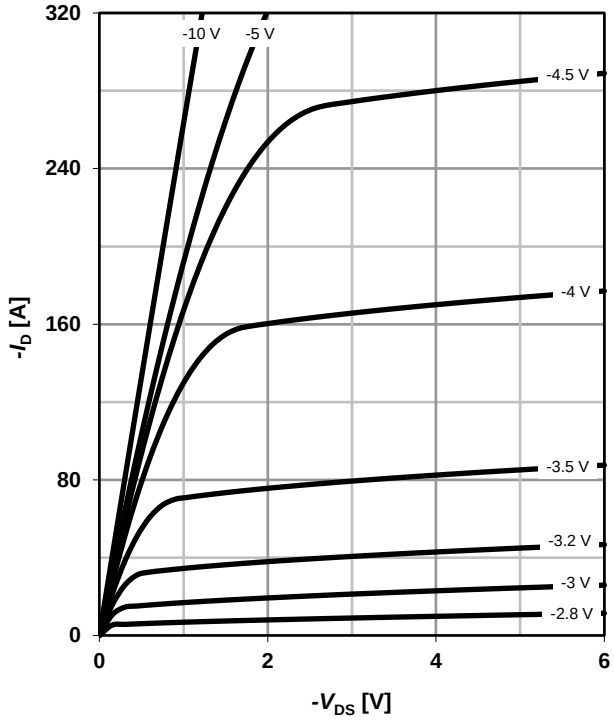
parameter: $D = t_p/T$



### 5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C; SMD

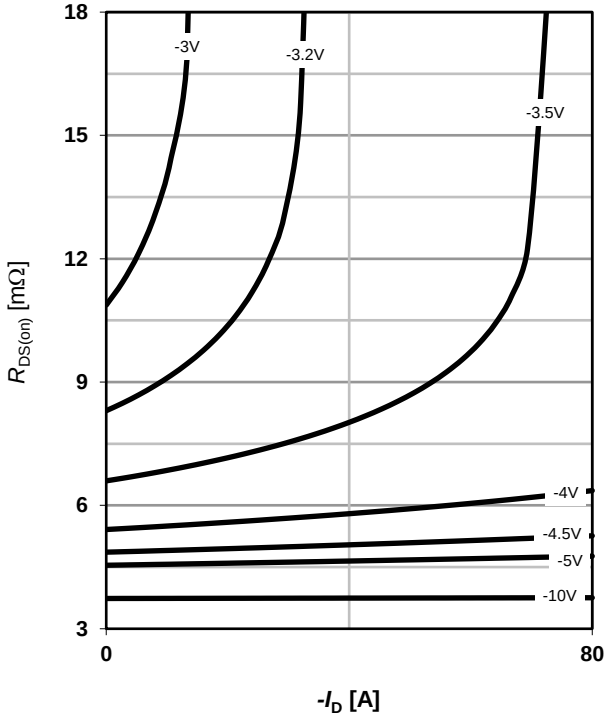
parameter: $V_{GS}$




### 6 Typ. drain-source on-state resistance

$R_{DS(on)} = (I_D)$; $T_j = 25$ °C; SMD

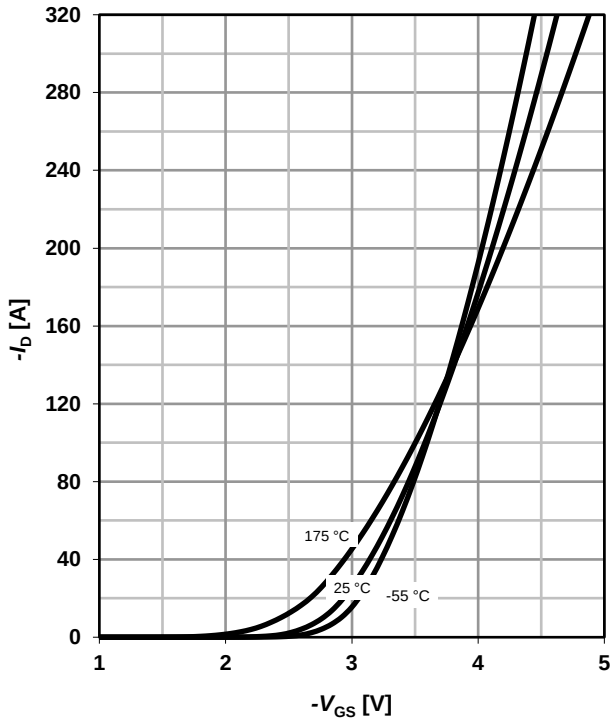
parameter: $V_{GS}$




### 7 Typ. transfer characteristics

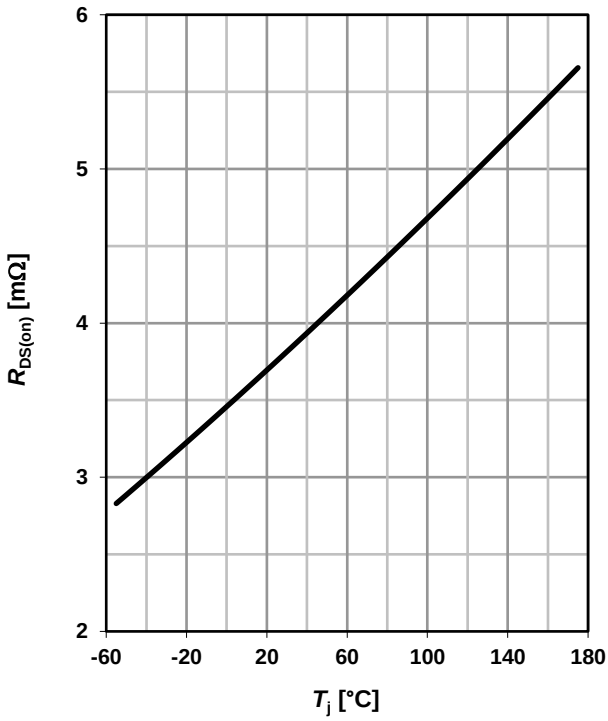
$I_D = f(V_{GS})$; $V_{DS} = -6$V

parameter: $T_j$




### 8 Typ. drain-source on-state resistance

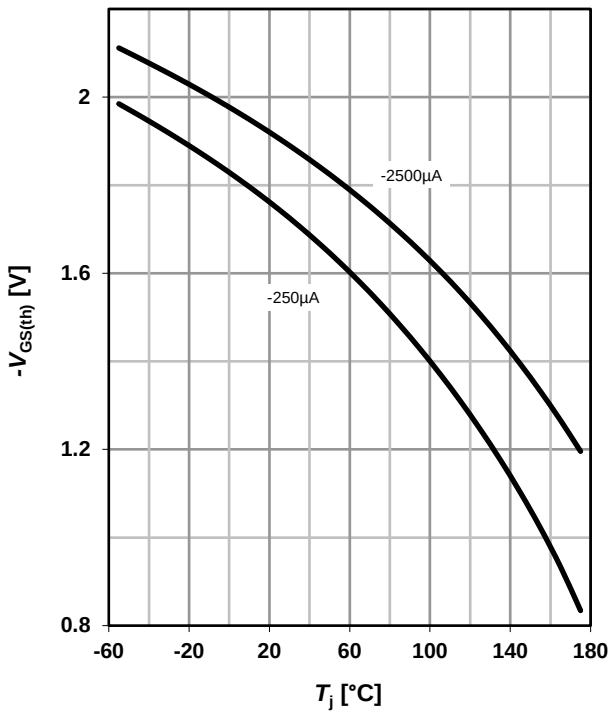
$R_{DS(on)} = f(T_j)$; $I_D = -80$ A; $V_{GS} = -10$ V; SMD



### 9 Typ. gate threshold voltage

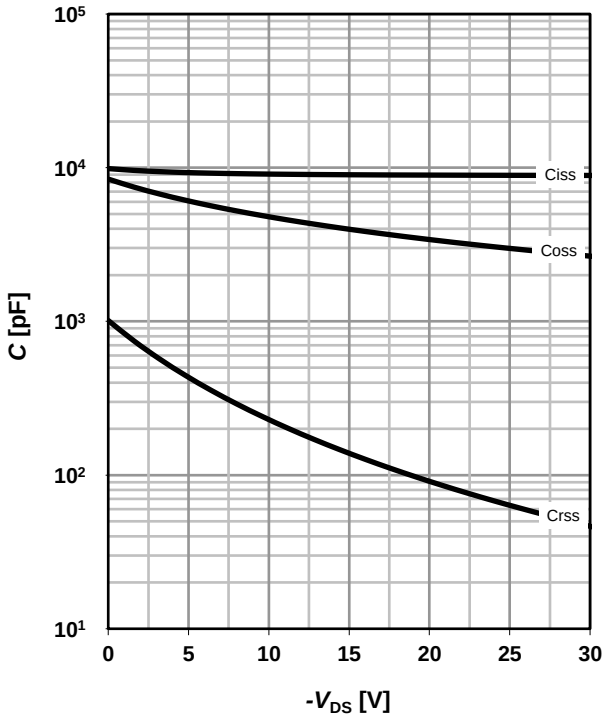
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: $I_D$




### 10 Typ. capacitances

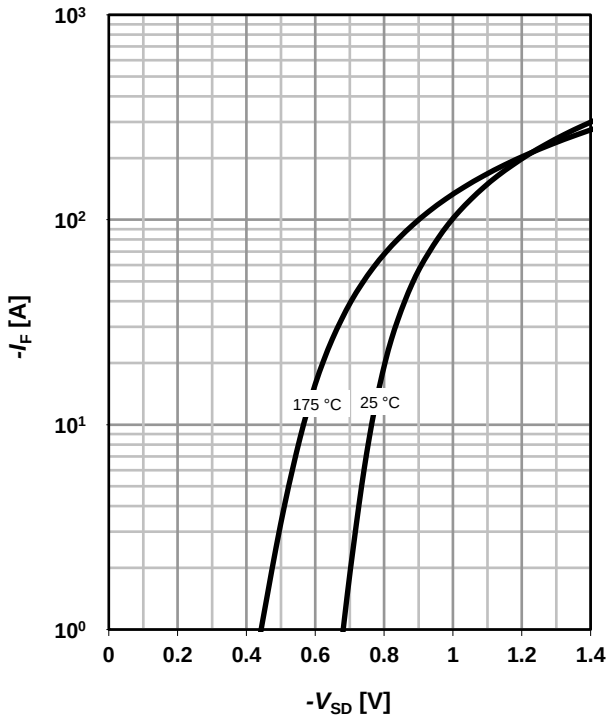
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f$ = 1 MHz




### 11 Typical forward diode characteristicis

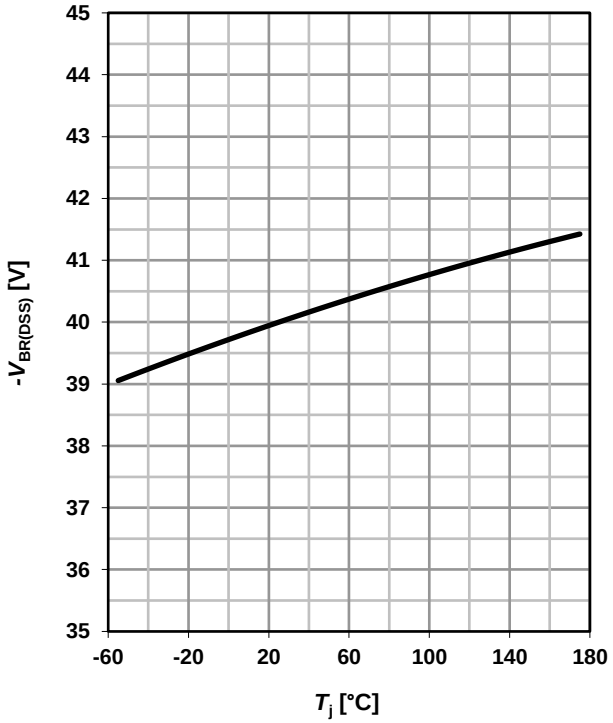
IF = f($V_{SD}$)

parameter: $T_j$




### 12 Drain-source breakdown voltage

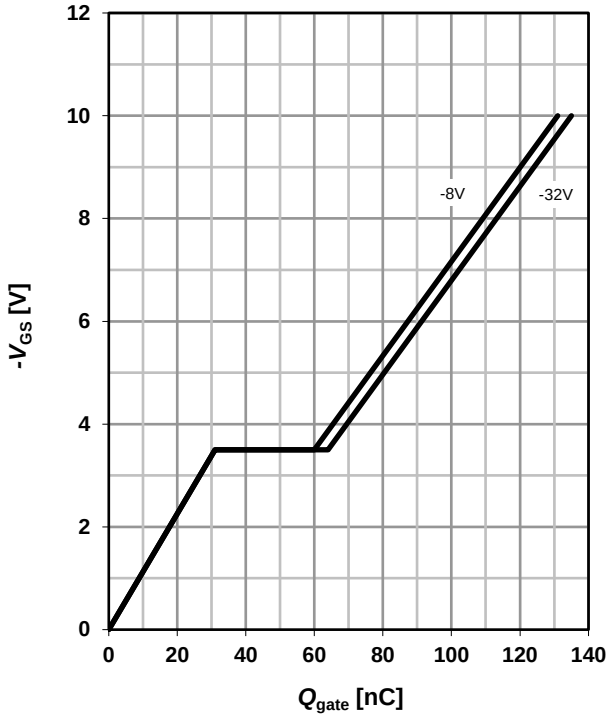
$V_{BR(DSS)} = f(T_j)$; $I_D$ = -1 mA



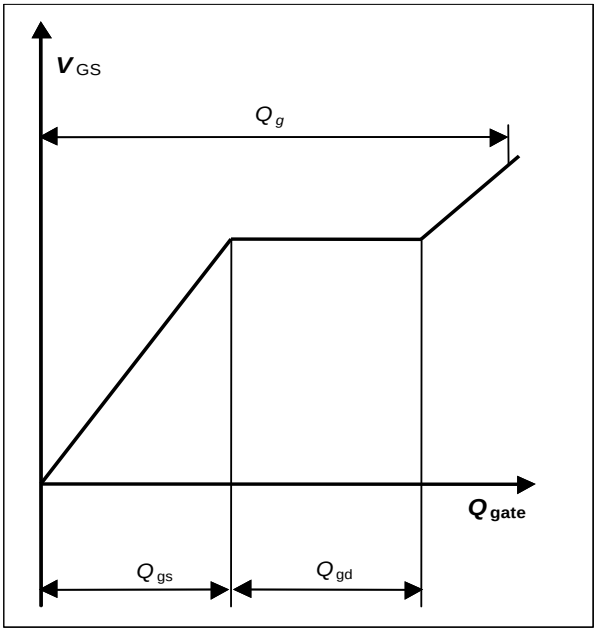
## 15 Typ. gate charge

$V_{GS}$ = f($Q_{gate}$); $I_D$ = -80 A pulsed

parameter: $V_{DD}$




## 16 Gate charge waveforms



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Revision History

| **Version** | Date | Changes |
|---|---|---|
| 1.0 | 28.01.2011 | Final Data Sheet |
| 1.1 | 03.07.2019 | $V_{GS}$ changed |