TVS Diodes

Transient Voltage Suppressor Diodes

ESD102-U4-05L

Ultra-Low Capacitance ESD Protection Array for Flow-Through PCB Layout

ESD102-U4-05L

Data Sheet

Revision 1.0, 2013-02-25
Final

Power Management & Multimarket

Edition 2013-02-25

Published by
Infineon Technologies AG
81726 Munich, Germany

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Revision History: Revision 0.9.1, 2012-11-28	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.0, 2013-02-25	
All	Status change to Final
7	ESD Characteristics updated

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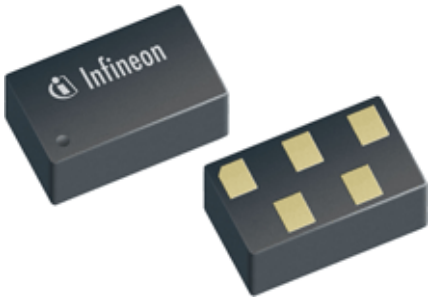
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Last Trademarks Update 2010-06-09

1 Ultra-Low Capacitance ESD Protection Array for Flow-Through PCB Layout

1.1 Features



- ESD / transient protection of high speed data lines exceeding:
  - **IEC61000-4-2 (ESD): ±24 kV (air), ±20 kV (contact)**
  - **IEC61000-4-4 (EFT): ±60 A / ±3 kV (5/50ns)**
  - **IEC61000-4-5 (Surge): ±3.5 A (8/20µs)**
- Maximum working voltage: V_{RWM} **= 3.3 V**
- Ultra low capacitance:
  - C_L **= 0.2 pF** I/O to I/O (typical)
  - C_L **= 0.4 pF** I/O to GND (typical)
- Extremely low leakage voltage: 1 nA (typical)
- Very low clamping voltage: V_{CL} = 8 V (typical) at I_{PP} = 16 A
- Very low dynamic resistance: R_{DYN} **= 0.19 Ω** (typical)
- TSLP-5-2 package with pad pitch 0.5 mm, optimized pad design to simplify PCB layout
- Pb-free and halogen free package (RoHS compliant)

1.2 Application Examples

- USB2.0 (D+, D-, ID), USB 3.0, 10/100/1000 Ethernet, Firewire
- DVI, HDMI, S-ATA, Display Port
- Mobile HDMI Link, MDDI, MIPI, etc.

1.3 Product Description

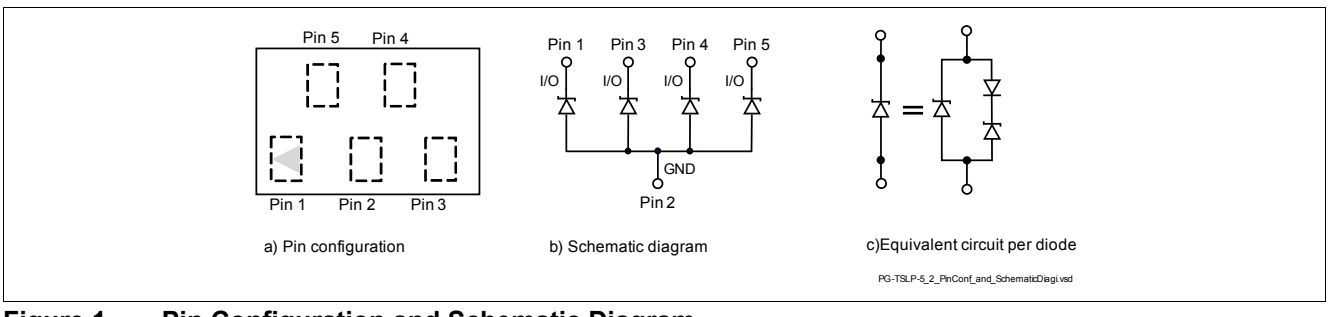


Figure 1 Pin Configuration and Schematic Diagram

Table 1 Ordering Information

Type	Package	Configuration	Marking code
ESD102-U4-05L	TSLP-5-2	4 lines, uni-directional	A

2 Characteristics

Table 2 Maximum Rating at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD discharge[1)] air contact	V_{ESD}	 -24 -20	 – –	 24 20	kV
Peak pulse current (t_p = 8/20 µs)[2)]	I_{PP}	-3.5	–	3.5	A
Peak pulse power t_p = 8/20 µs[2)] t_p = 100 ns[3)]	P_{PK}	 – –	 – –	 28 750	W
Operating temperature	T_{OP}	-40	–	125	°C
Storage temperature	T_{stg}	-65	–	150	°C

1) V_{ESD} according to IEC61000-4-2
2) I_{PP} according to IEC61000-4-5
3) Please refer to AN210[2]

2.1 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

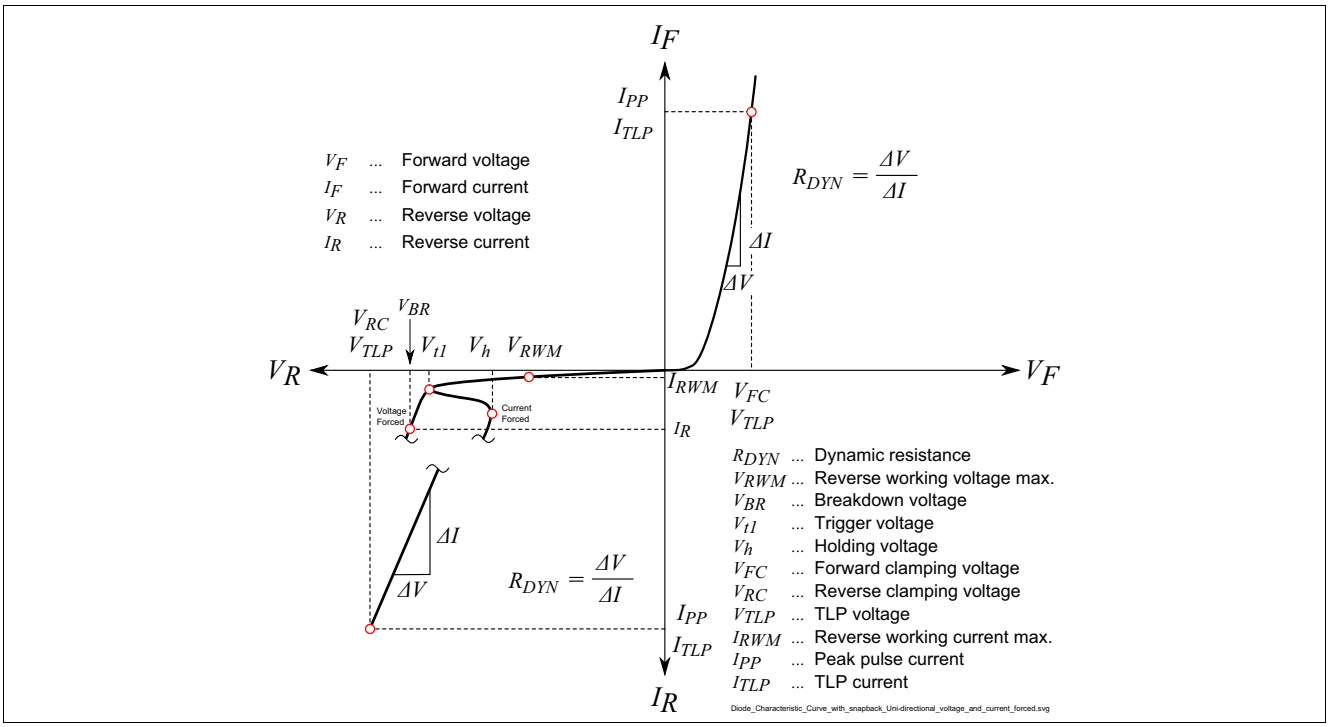


Figure 2 Definitions of electrical characteristics[1]

Table 3 DC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage[1]	V_{RWM}	–	–	3.3	V	I/O to GND
Reverse current[1]	I_R	–	1	50	nA	I/O to GND, V_R = 3.3 V
Breakdown voltage[1]	V_{BR}	–	6.2	–	V	I/O to GND
Reverse trigger voltage[2]	V_{t1}	–	6.2	–	V	I/O to GND
Reverse holding voltage[2]	V_h	3.35	4	4.4	V	I/O to GND, I_R = 10 mA

1) Voltage forced

2) Current forced

Table 4 RF Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance[1]	C_L	–	0.4	0.65	pF	V_R = 0 V, f = 1 MHz, I/O to GND
		–	0.2	0.35	pF	V_R = 0 V, f = 1 MHz, I/O to I/O
Channel capacitance matching between I/O to GND	$\Delta C_{i/o\text{-}GND}$	–	0.035	–	pF	V_R = 0 V, f = 1 MHz, I/O to GND
Channel capacitance matching between I/O to I/O	$\Delta C_{i/o\text{-}i/o}$	–	0.017	–	pF	V_R = 0 V, f = 1 MHz, I/O to I/O

1) Total capacitance line to ground

Table 5 ESD Characteristics[1)] at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage[2)]	V_{CL}	–	4.8	5.6	V	I_{PP} = 1 A, t_p = 8/20µs from I/O to GND
		–	6.2	7.4		I_{PP} = 3 A, t_p = 8/20µs from I/O to GND
Clamping voltage[3)]	V_{CL}	–	8	9.5		I_{TLP} = 16 A, from I/O to GND
		–	11	13.2		I_{TLP} = 30 A, from I/O to GND
Forward clamping voltage[2)]	V_{FC}	–	1.4	1.8		I_{PP} = 1 A, t_p = 8/20µs from GND to I/O
		–	2.3	2.9		I_{PP} = 3 A, t_p = 8/20µs from GND to I/O
Forward clamping voltage[3)]	V_{FC}	–	6	7.5		I_{TLP} = 16 A, from GND to I/O
		–	9	11.5		I_{TLP} = 30 A, from GND to I/O
Dynamic resistance[3)]	R_{DYN}	–	0.19	0.24	Ω	I/O to GND
		–	0.23	0.28	Ω	GND to any I/O

1) Not subject to production test - verified by design/ characterization

2) I_{PP} according to IEC61000-4-5

3) Please refer to Application Note AN210. TLP parameter: Z_0 = 50 Ω , t_p = 100ns, t_r = 300ps, averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristic between I_{PP1} = 10 A and I_{PP2} = 40 A.**[2]**

3 Typical Characteristics at T_A = 25 °C, unless otherwise specified

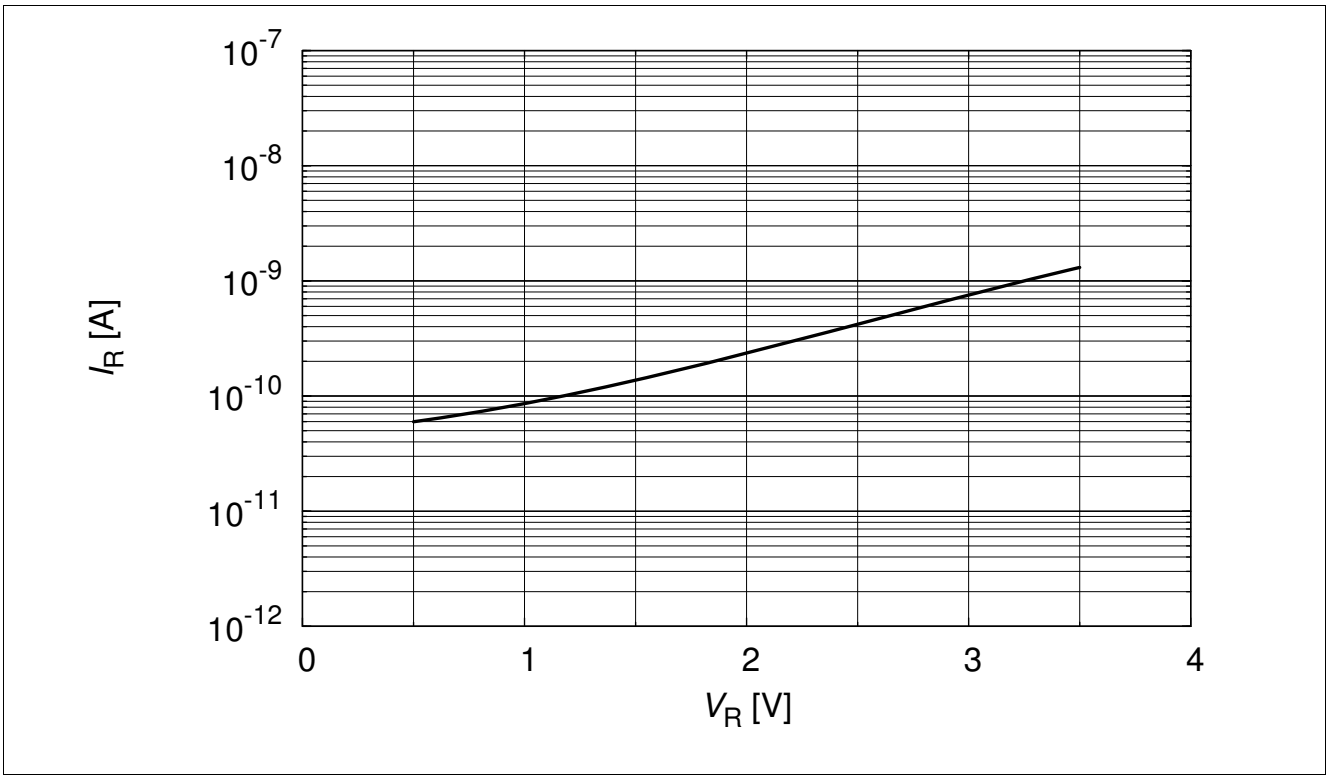


Figure 3 Reverse current, $I_R = (V_R)$

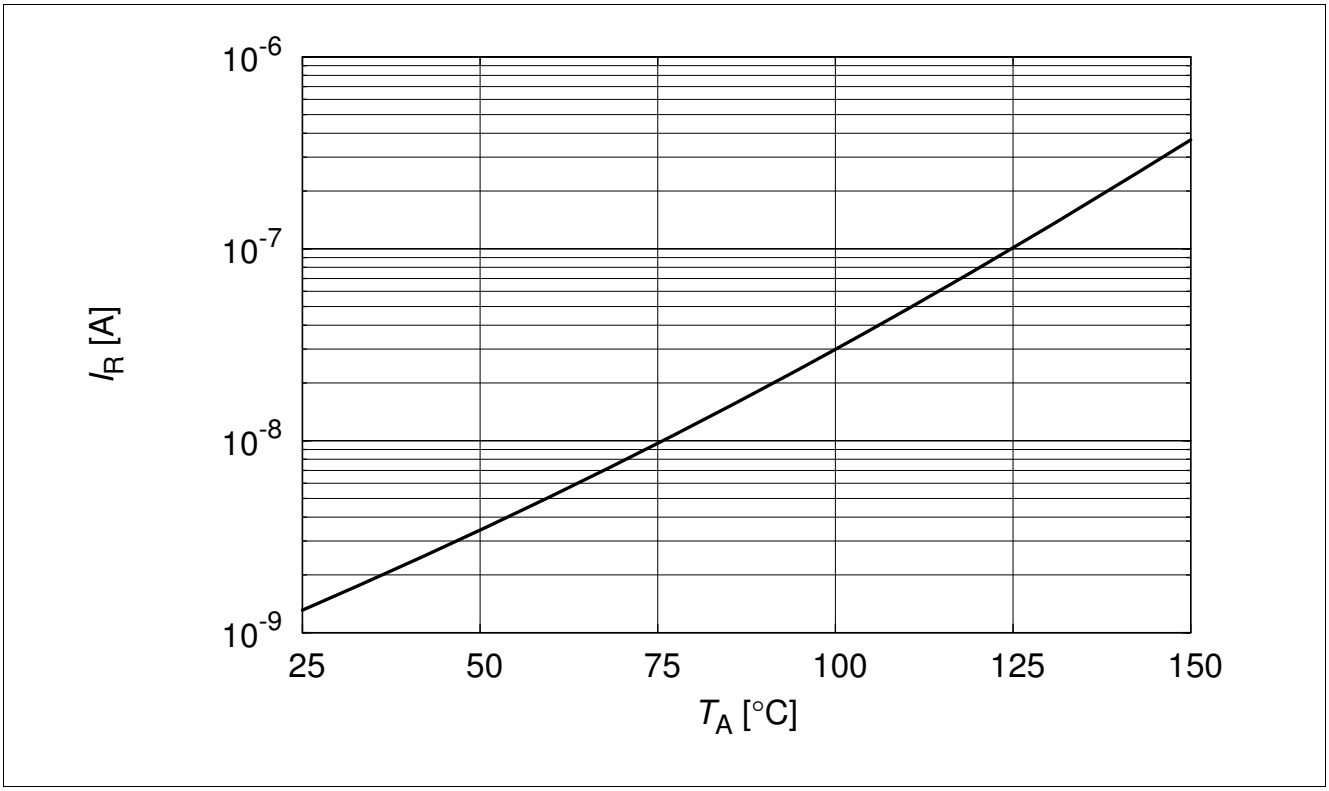


Figure 4 Reverse current: $I_R = f(T_A)$, V_R = 3.3 V

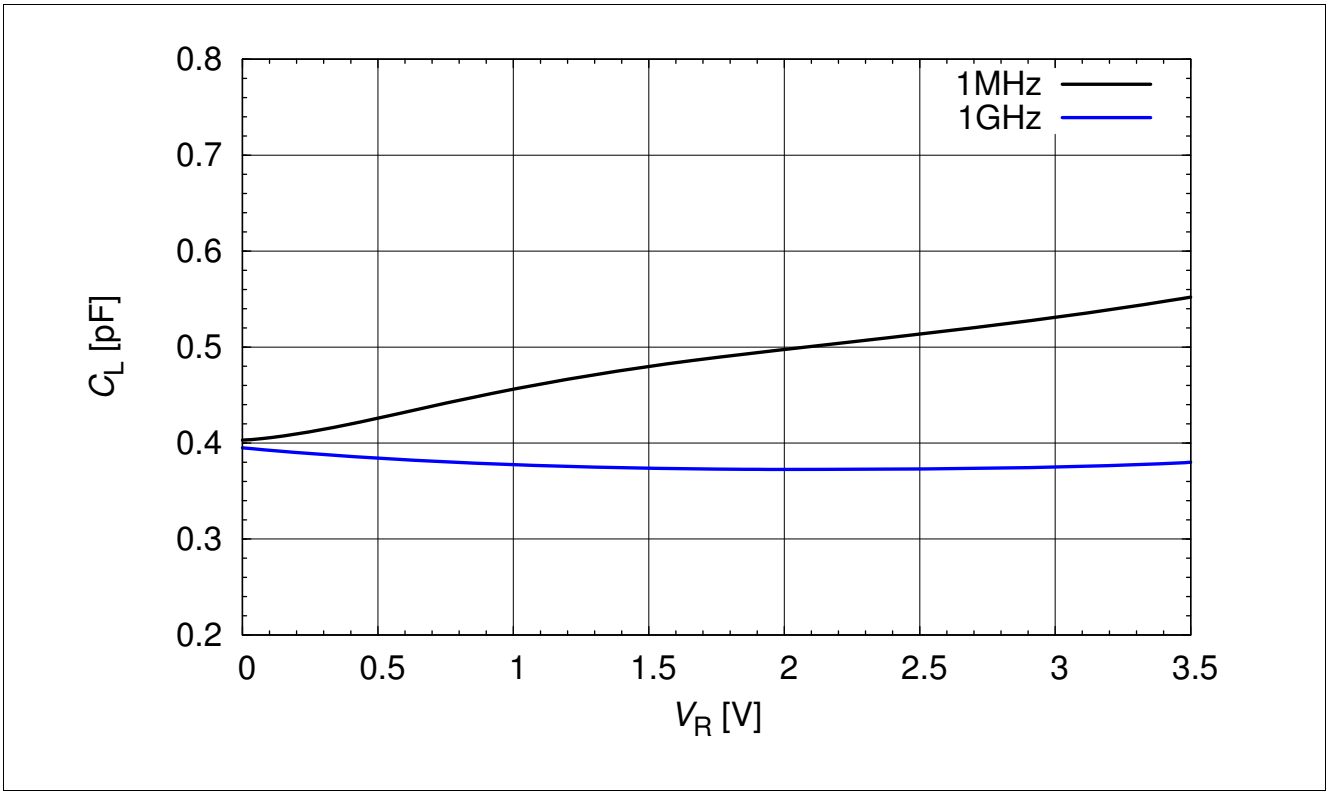


Figure 5 **Line capacitance: $C_L = f(V_R)$, f = 1MHz, from I/O to GND**

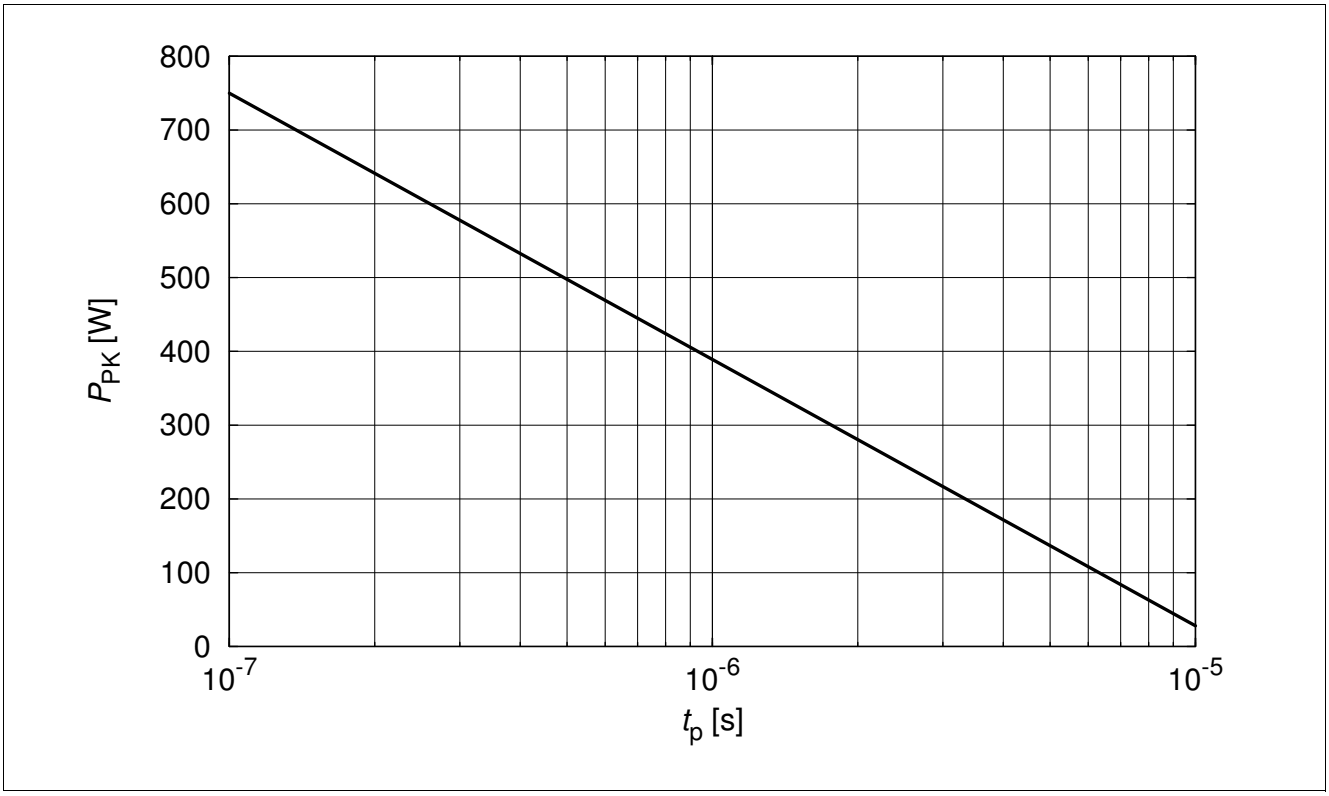


Figure 6 **Peak pulse power: $P_{PK} = f(t_p)$**

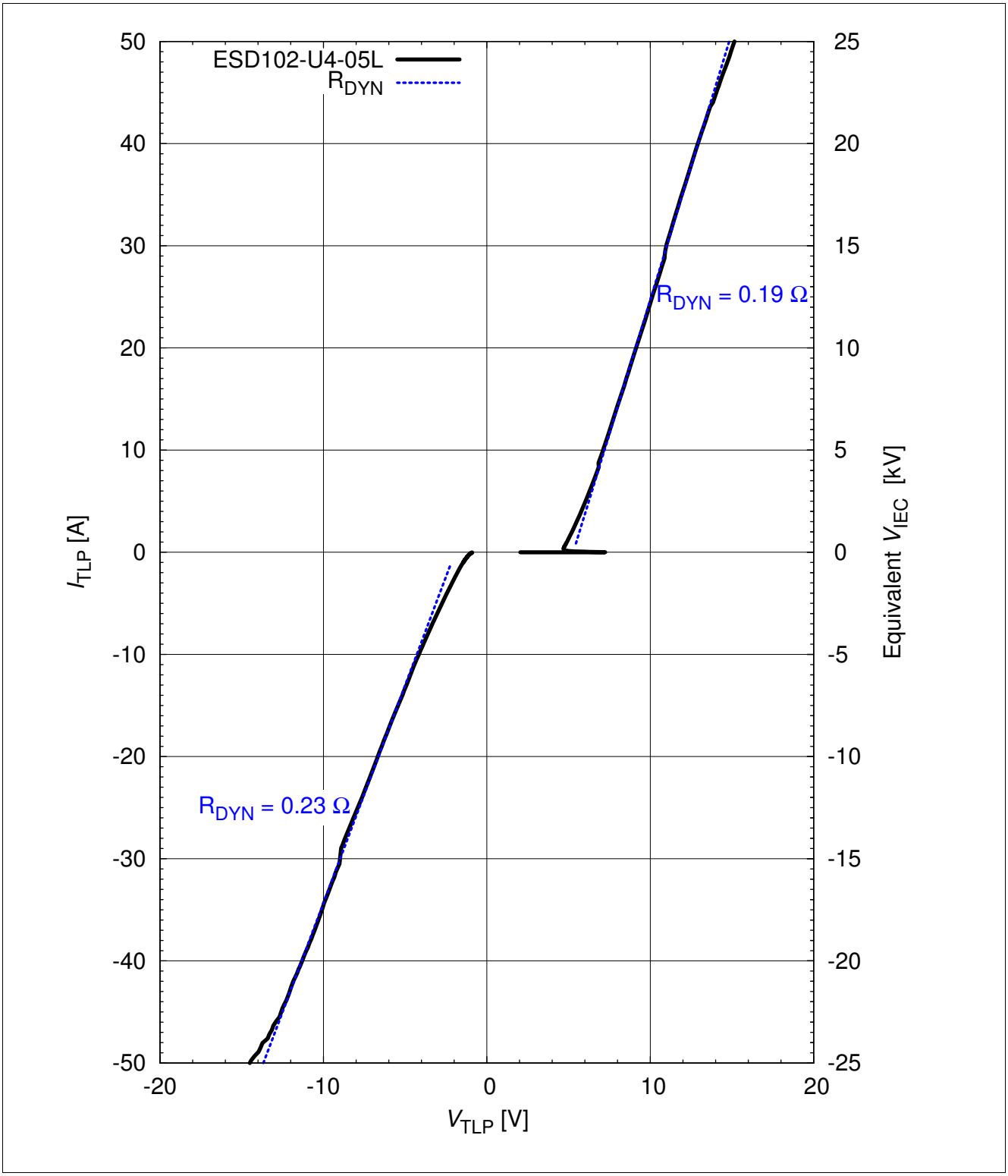


Figure 7 Clamping voltage $V_{TLP} = f(I_{TLP})$[2]

Note: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 300 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristic between I_{PP1} = 10 A and I_{PP2} = 40 A. The equivalent stress level V_{IEC} according IEC 61000-4-2 (R = 330 Ω, C = 150 pF) is calculated at the broad peak of the IEC waveform at t = 30 ns with 2 A / kV

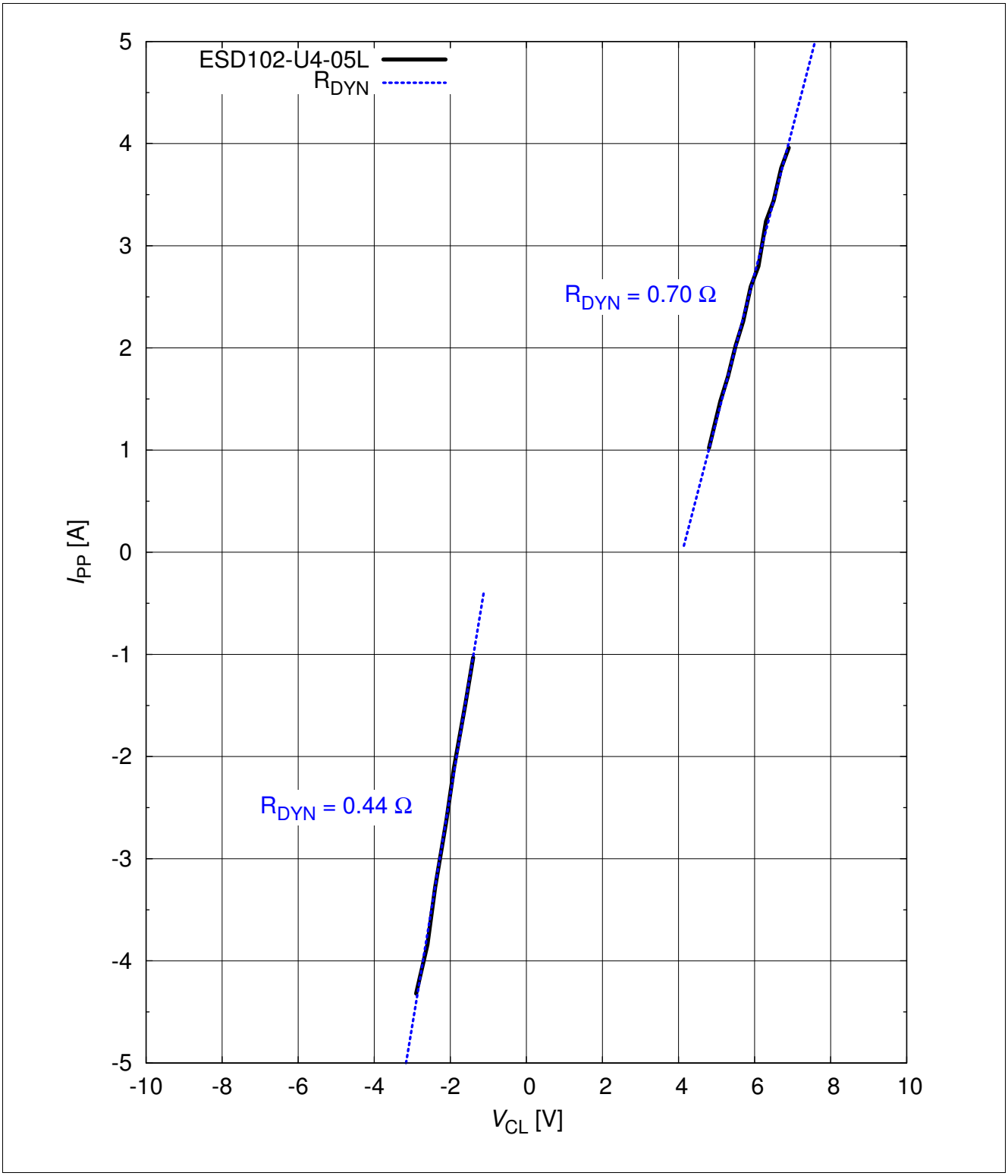


Figure 8 Pulse current (IEC61000-4-5) versus clamping voltage: $I_{PP} = f(V_{CL})$

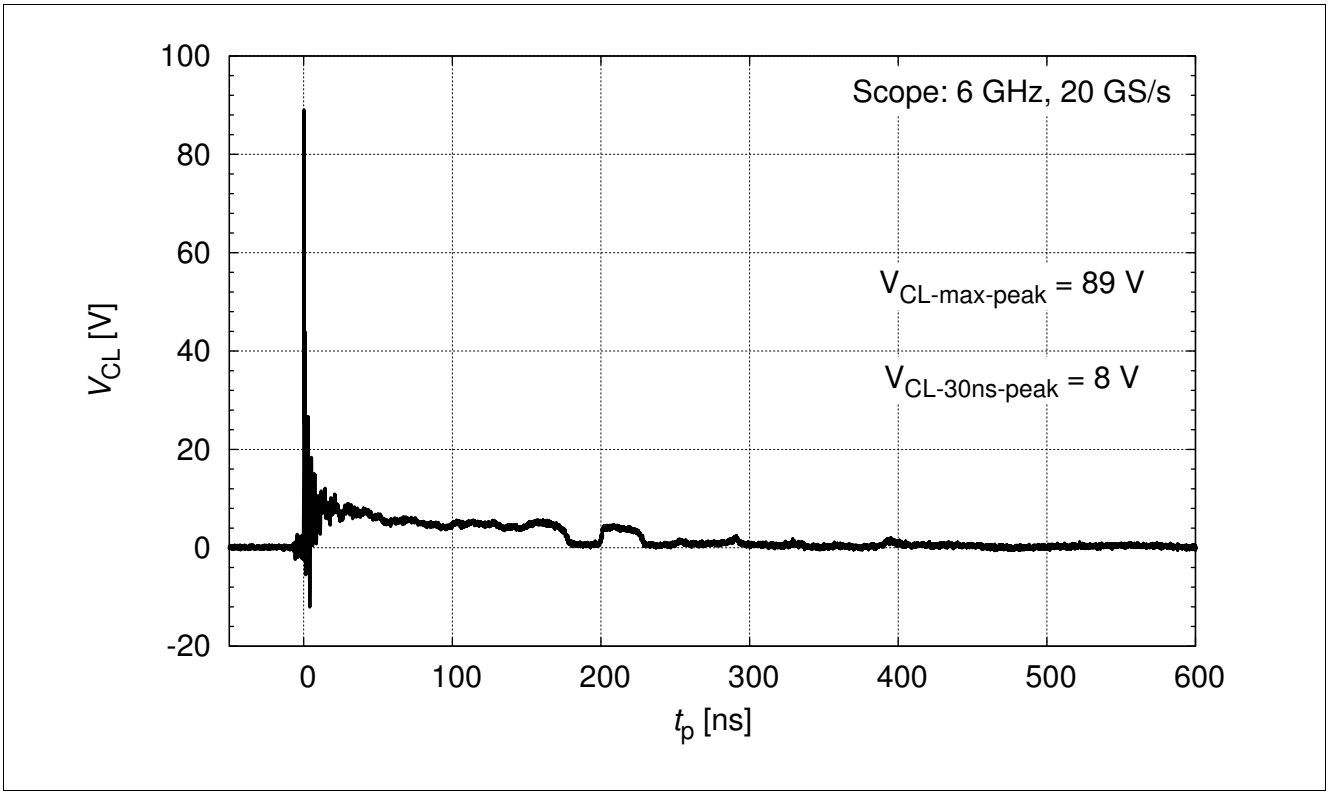


Figure 9 Clamping voltage at +8 kV discharge according IEC61000-4-2 (R = 330 Ω, C = 150 pF)

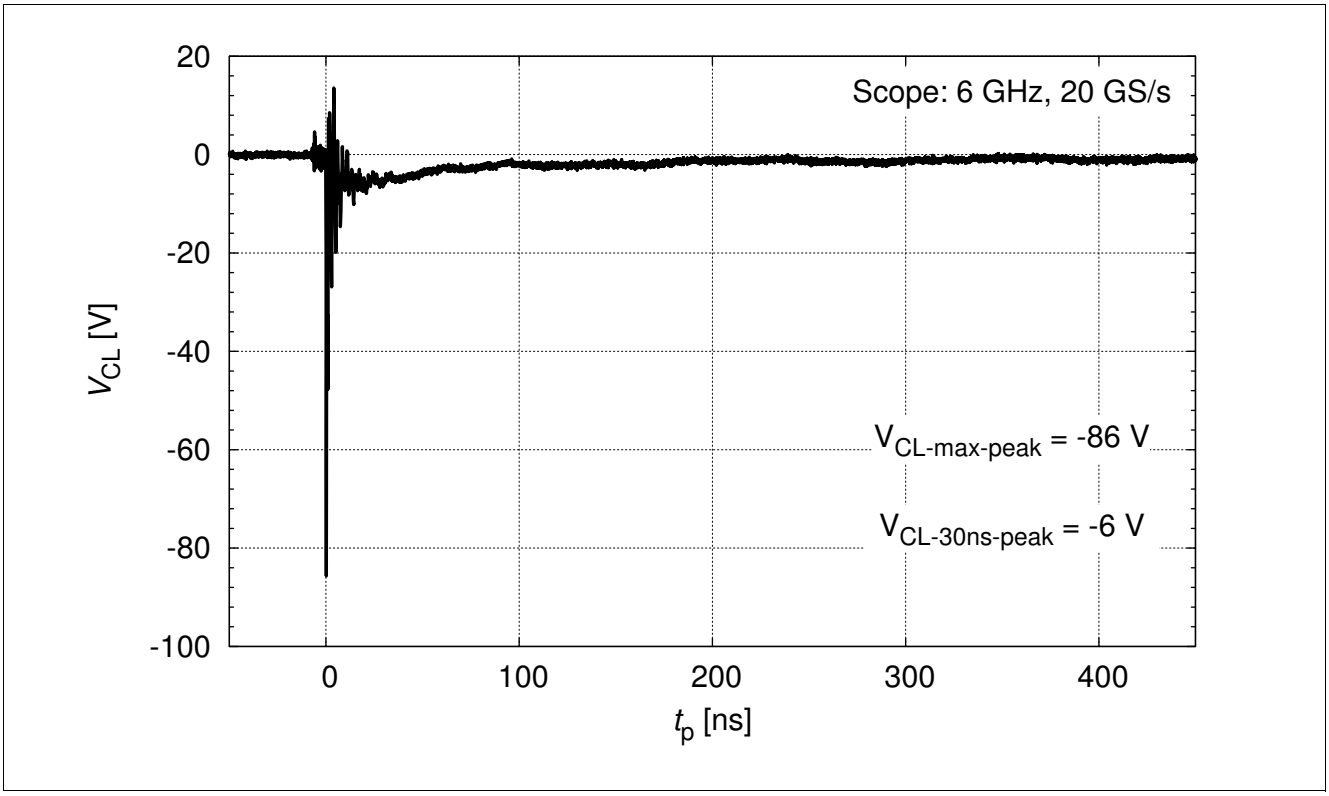


Figure 10 Clamping voltage at -8 kV discharge according IEC61000-4-2 (R = 330 Ω, C = 150 pF)

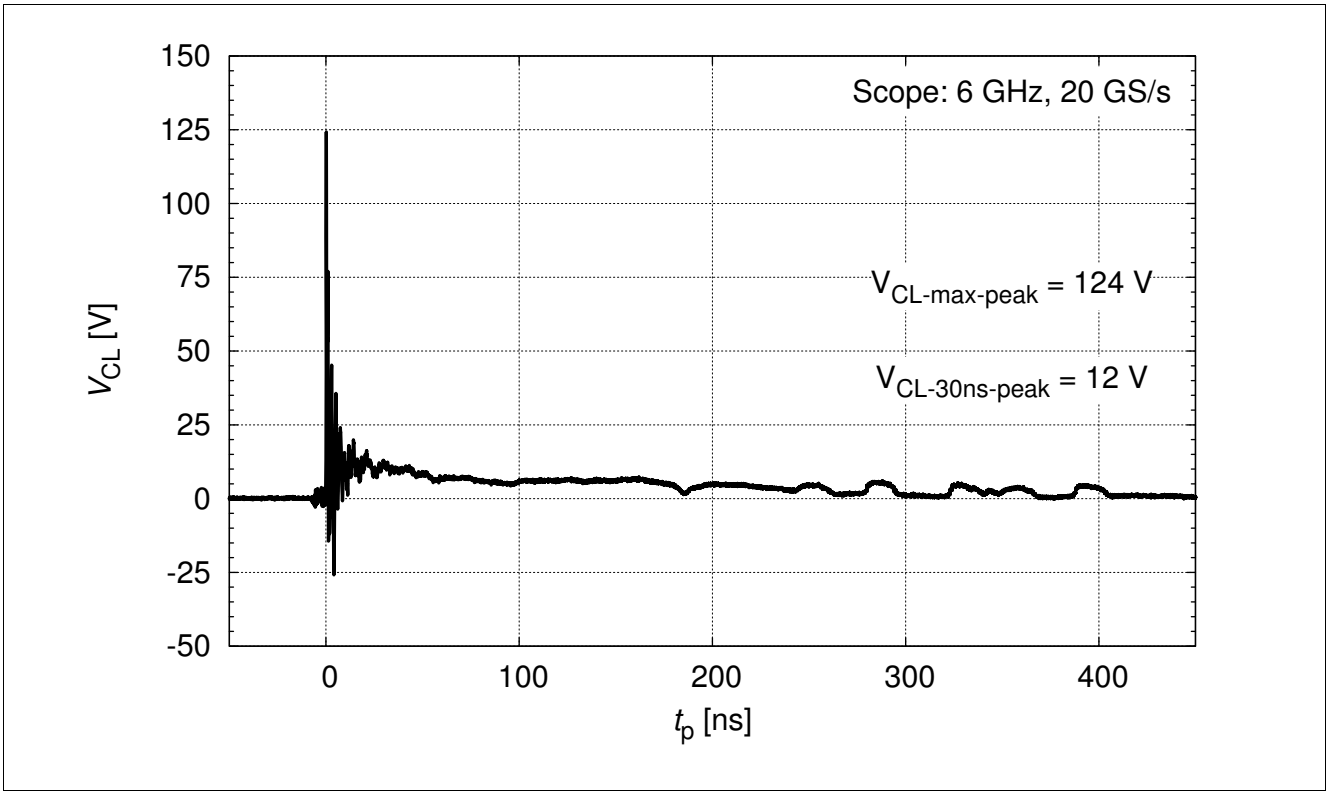


Figure 11 Clamping voltage at +15 kV discharge according IEC61000-4-2 (R = 330 Ohm, C = 150 pF)

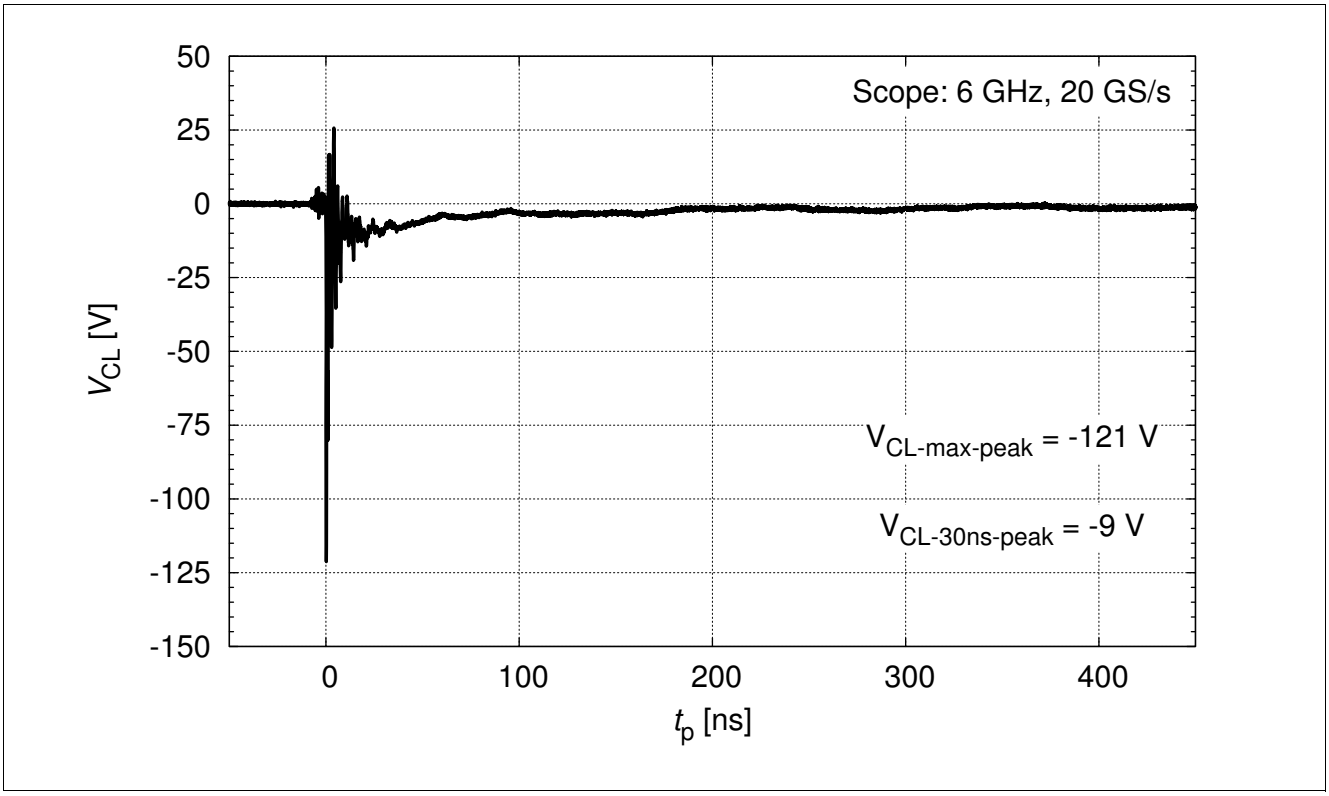


Figure 12 Clamping voltage at -15 kV discharge according IEC61000-4-2 (R = 330 Ω, C = 150 pF)

4 Application hints

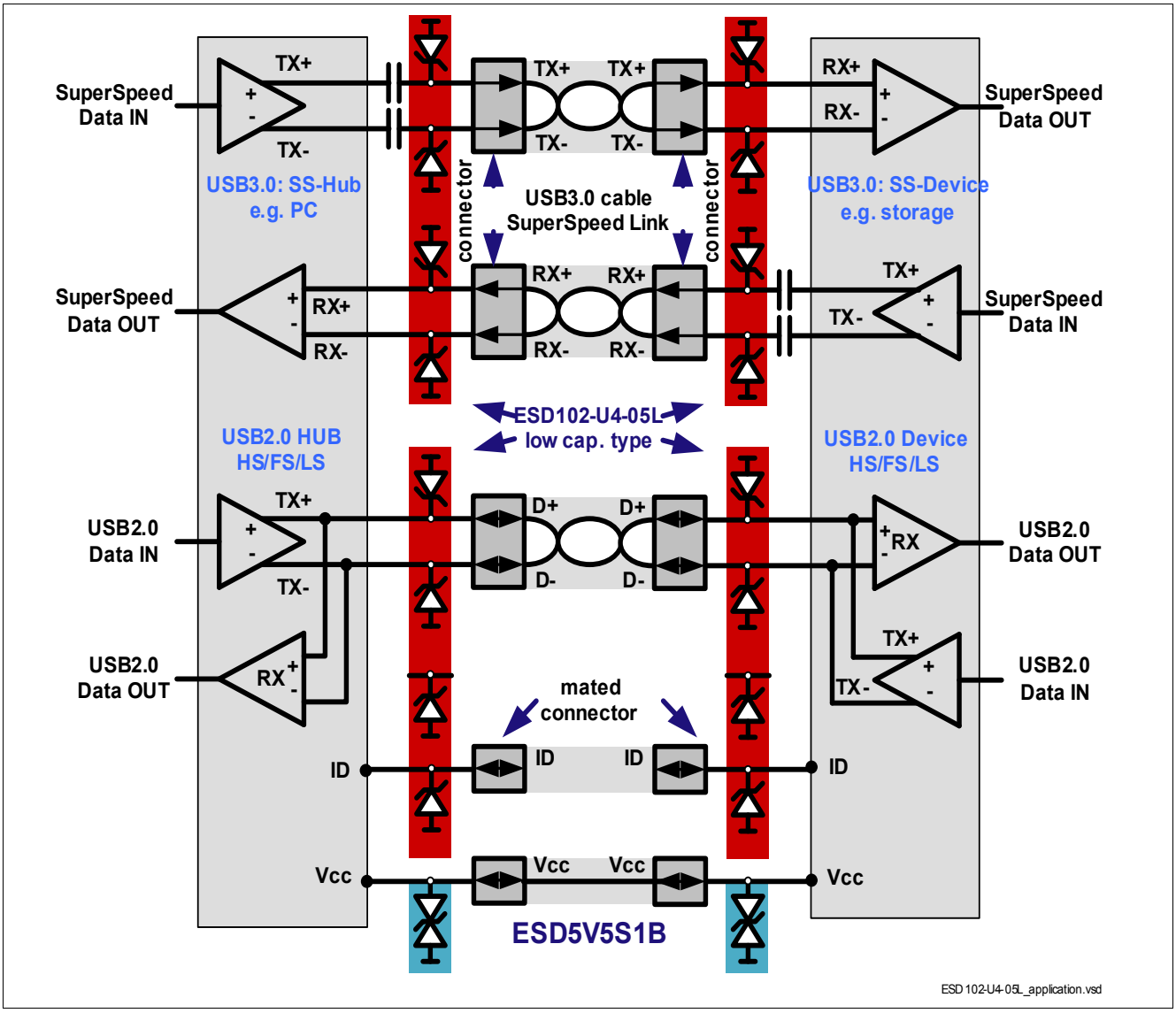


Figure 13 Application

High speed low voltage differential signaling (LVDS) is using a coupled line-pair, called ‘lane’ for data transmission.

In this data transmission systems load and source impedance as well the characteristic differential line impedance is well defined in the range of 90... 100 Ω for USB2.0/ USB3.0, MIPI, HDMI Thunderbolt.

The USB3.0 link provides a full duplex SuperSpeed link (dedicated TX and RX lanes, up to 5 Gb/s) and a USB2.0 link to maintain compatibility. In addition there is a ID pin for identification, the Vcc pin for 5 V supply.

To protect from ESD damage, suited ESD protection diodes should be placed close to the connector.

For the differential high-speed lines the TVS diodes must not have an impact to insertion loss even not for the third harmonic of the data signal. Signal integrity must not affected by the ESD diode capacitance, The use of ultra low capacitance ESD diode for the data line is mandatory. For the ID and the Vcc pin device capacitance is not critical. To handle the 5 V Vcc line, a 5 V (or even higher) ESD diode is required.

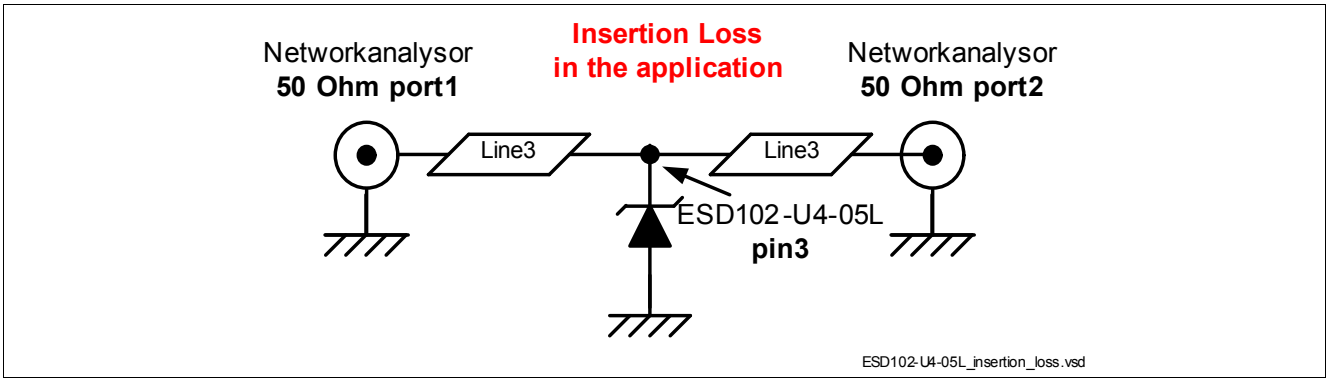


Figure 14 Insertion loss measured in 50 Ω environment, correlating to one line in the differential coupled LVDS line pair.

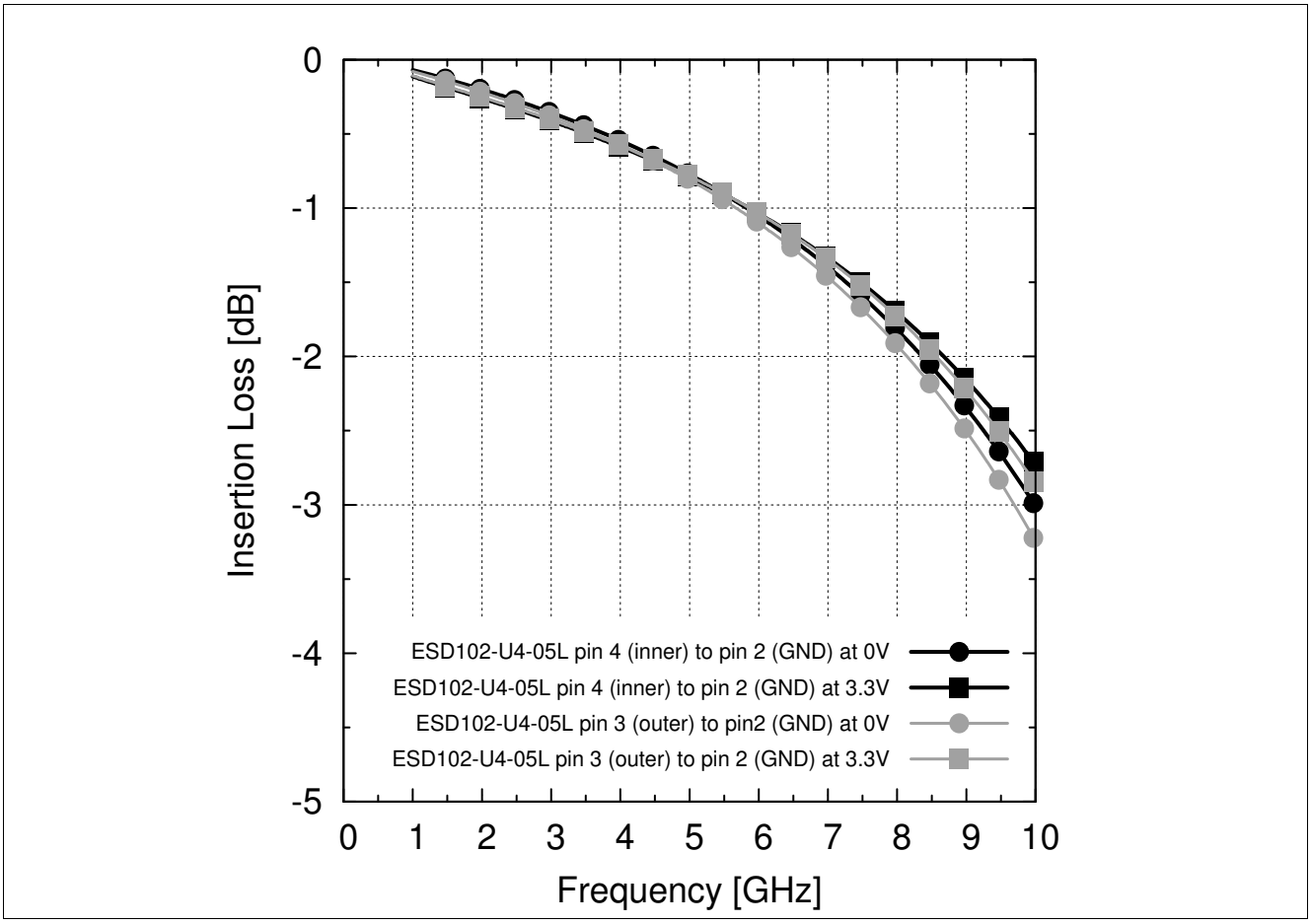


Figure 15 Insertion loss vs. frequency of ESD102-U5-05L in a 50 Ω system

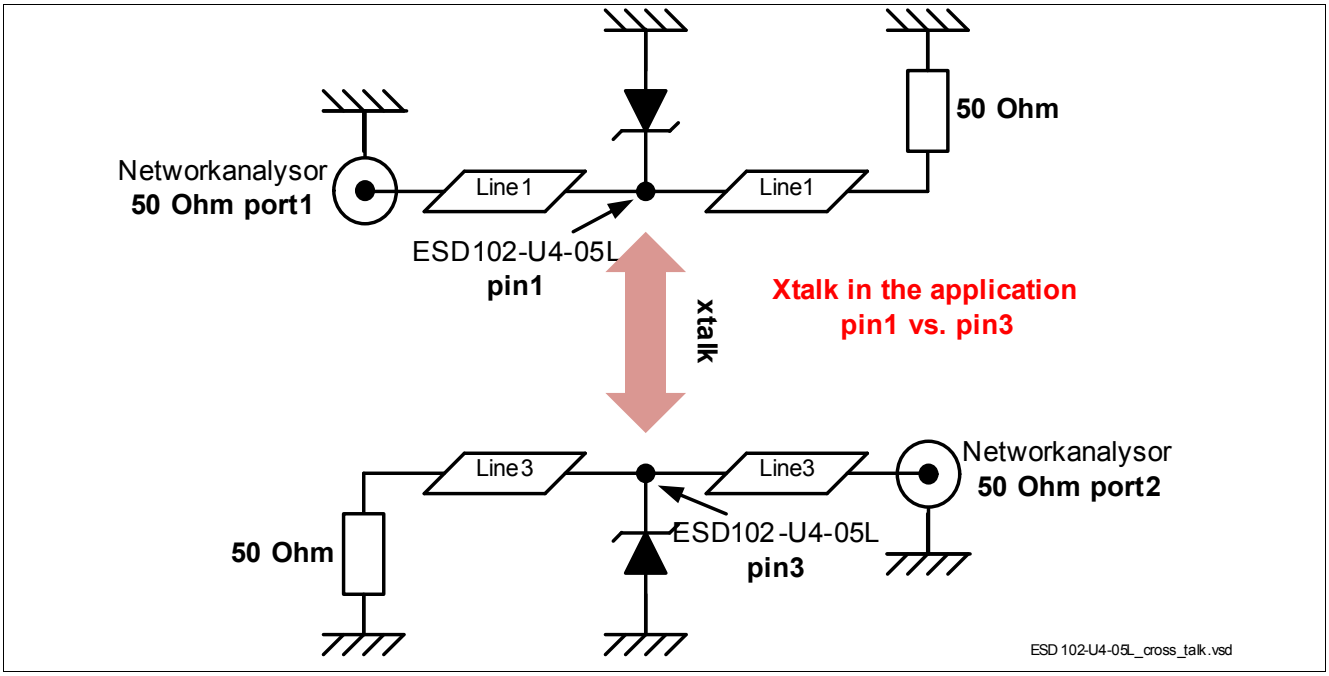


Figure 16 Crosstalk (xtalk) between two ESD diodes (part of ESD102-U4-05L) measured in USB3.0 SuperSpeed environment (100 Ω differential impedance)

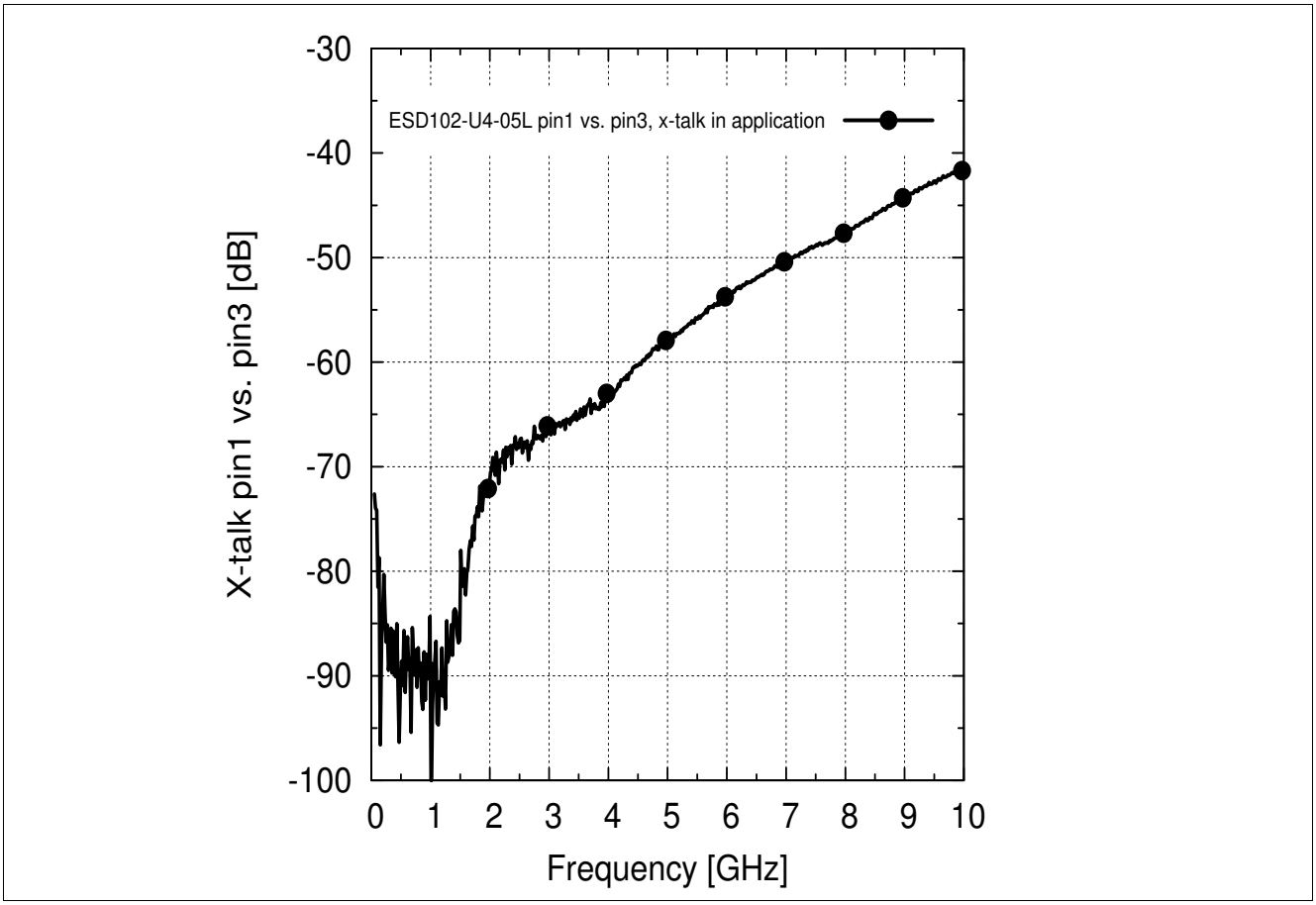


Figure 17 Xtalk vs. frequency of ESD102-U5-=5L in a 100 Ω system

5 Package Information

5.1 TSLP-5-2 (mm)

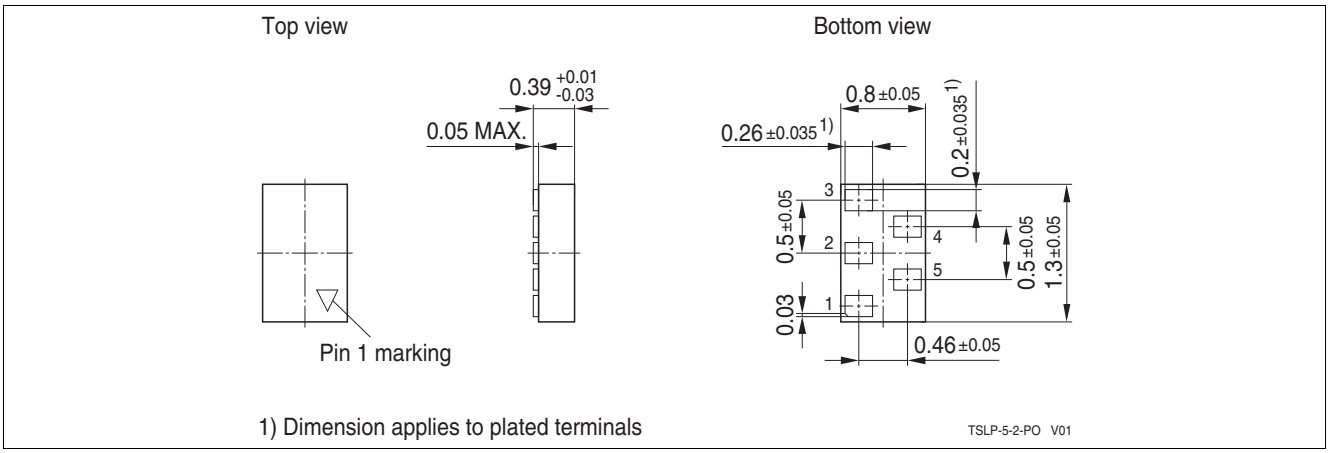


Figure 18 TSLP-5-2: Package overview

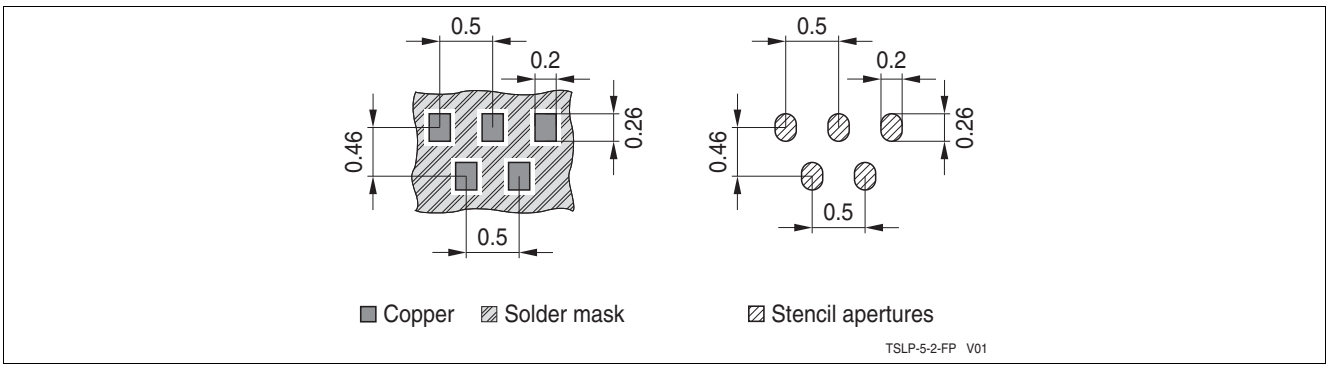


Figure 19 TSLP-5-2: Footprint

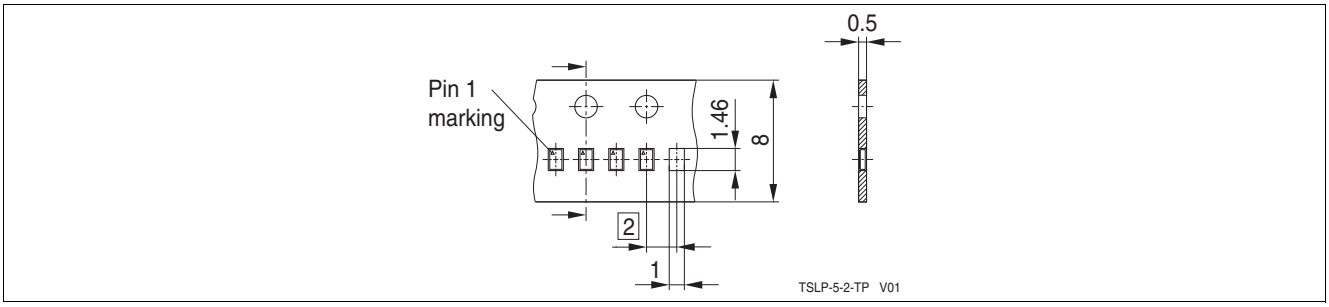


Figure 20 TSLP-5-2: Packing

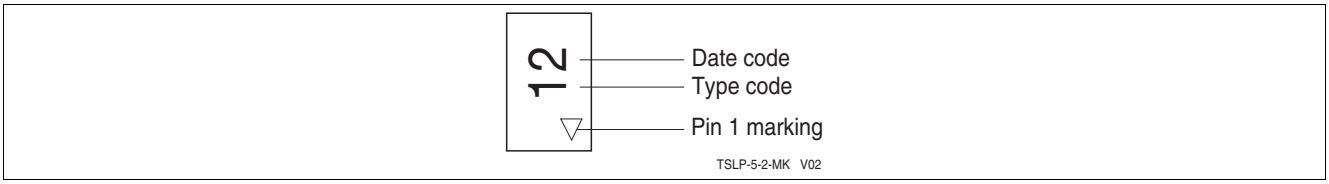


Figure 21 TSLP-5-2: Marking

References

[1] **On-chip ESD protection for integrated circuits**, Albert Z. H. Wang, ISBN:0-7923-7647-1

[2] Infineon Technologie AG - **Application Note AN210**: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology

[3] Infineon Technologie AG - **Application Note AN240**: Effective ESD Protection for USB3.0, combined with perfect Signal Intergrity.

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