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Pin Configuration and Functionality

1 Pin Configuration and Functionality

Table 1 Pin definitions and functions

Pin	Symbol	Function
1, 9, 10	N.C	Not Connected
2	SoftS	Soft-Start (Soft Start, Auto Restart & Frequency Jittering Control) The SoftS pin combines the function of Soft Start during Start Up and error detection for Auto Restart Mode. These functions are implemented and can be adjusted by means of an external capacitor at SoftS to ground. This capacitor also provides an adjustable blanking window for high load jumps, before the IC enters into Auto Restart Mode. Furthermore this pin is also used to control the period of frequency jittering during normal load.
3	FB	FB (Feedback) The information about the regulation is provided by the FB Pin to the internal Protection Unit and to the internal PWM-Comparator to control the duty cycle. The FB-Signal controls in case of light load the Active Burst Mode of the controller.
4	CS	CS (Current Sense) The Current Sense pin senses the voltage developed on the series resistor inserted in the source of the integrated Depl-CoolMOS™. If CS reaches the internal threshold of the Current Limit Comparator, the Driver output is immediately switched off. Furthermore the current information is provided for the PWM-Comparator to realize the Current Mode.
5, 6, 7, 8	Drain	Drain (Drain of 650 V¹ integrated CoolMOS™) Drain pins are connected to the Drain of integrated CoolMOS™.
11	VCC	VCC (Power supply) The VCC pin is the positive supply of the IC. The operating range is between 10.3 V and 26 V.
12	GND	GND (Ground) This is the common ground of the controller.

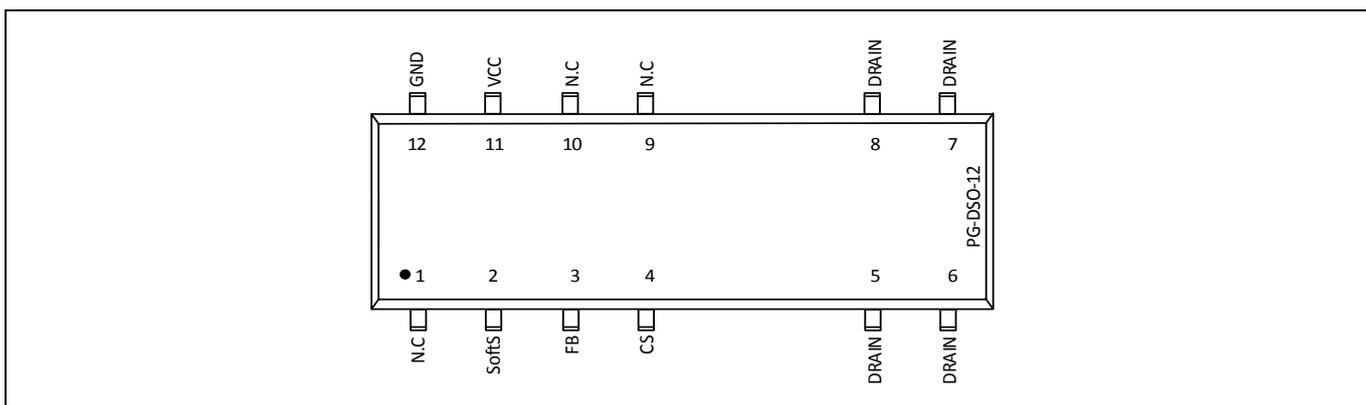


Figure 2 Pin configuration PG-DSO-12(top view)

¹at T_j=110°C

Representative Block Diagram

2 Representative Block Diagram

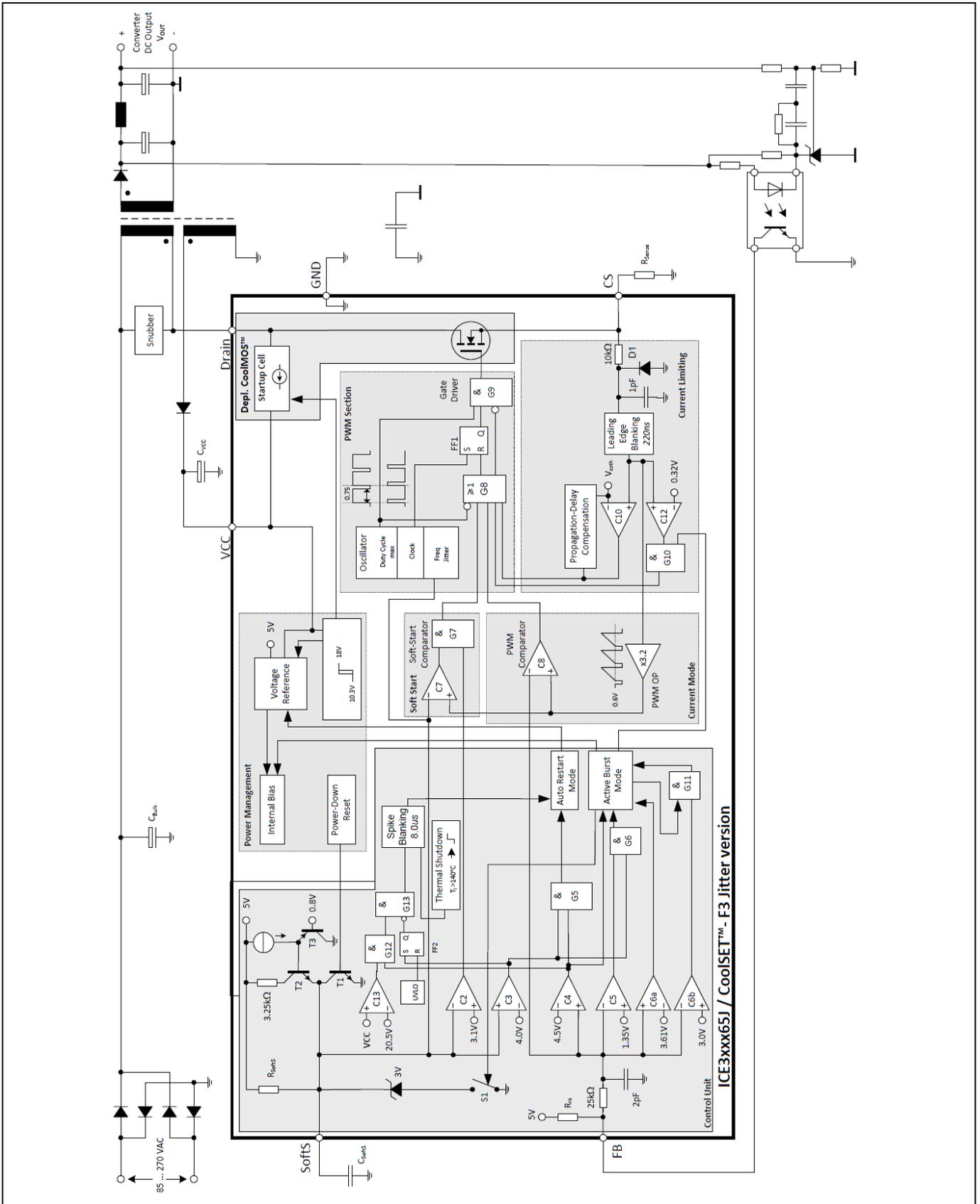


Figure 3 Representative Block Diagram

Functional Description

3 Functional Description

All values which are used in the functional description are typical values. For calculating the worst cases the min/max values which can be found in section 4 Electrical Characteristics have to be considered.

3.1 Introduction

CoolSET™-F3 Jitter version is the further development of the CoolSET™-F2 to meet the requirements for the lowest Standby Power at minimum load and no load conditions. A new fully integrated Standby Power concept is implemented into the IC in order to keep the application design easy. Compared to CoolSET™-F2 no further external parts are needed to achieve the lowest Standby Power. An intelligent Active Burst Mode is used for this Standby Mode. After entering this mode there is still a full control of the power conversion by the secondary side via the same optocoupler that is used for the normal PWM control. The response on load jumps is optimized. The voltage ripple on Vout is minimized. Vout is further on well controlled in this mode.

The usually external connected RC-filter in the feedback line after the optocoupler is integrated in the IC to reduce the external part count.

Furthermore a high voltage Startup Cell is integrated into the IC which is switched off once the Undervoltage Lockout on-threshold of 18V is exceeded. This Startup Cell is part of the integrated Depl. CoolMOS™. The external startup resistor is no longer necessary as this Startup Cell is connected to the Drain. Power losses are therefore reduced. This increases the efficiency under light load conditions drastically.

The Soft-Start capacitor is also used for providing an adjustable blanking window for high load jumps. During this time window the overload detection is disabled. With this concept no further external components are necessary to adjust the blanking window.

An Auto Restart Mode is implemented in the IC to reduce the average power conversion to in the event of malfunction or unsafe operating condition in the SMPS system. This feature increases the system's robustness and safety which would otherwise lead to a destruction of the SMPS. Once the malfunction is removed, normal operation is automatically initiated after the next Start Up Phase.

The internal precise peak current limitation reduces the costs for the transformer and the secondary diode. The influence of the change in the input voltage on the power limitation can be avoided together with the integrated Propagation Delay Compensation. Therefore the maximum power is nearly independent on the input voltage which is required for wide range SMPS. There is no need for an extra over-sizing of the SMPS, e.g. the transformer or the secondary diode.

Functional Description

3.2 Power Management

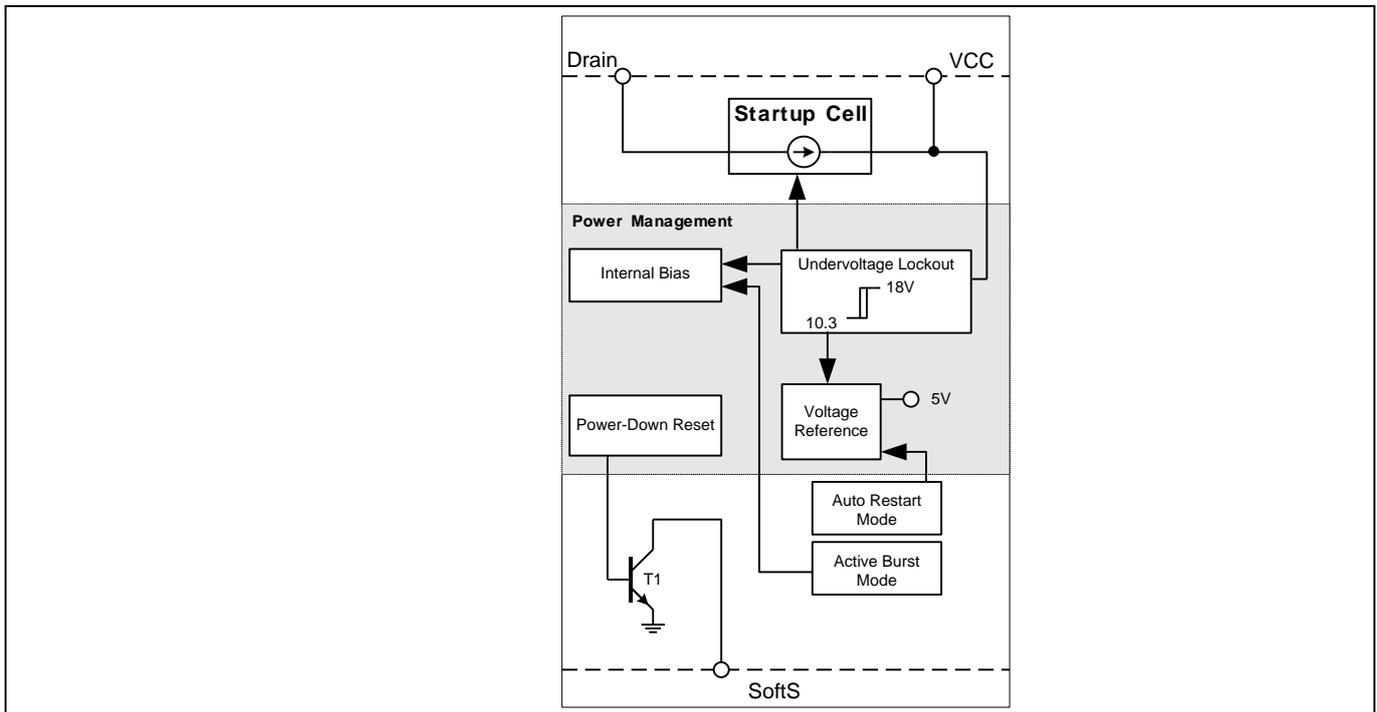


Figure 4 Power Management

The Undervoltage Lockout monitors the external supply voltage V_{VCC} . When the SMPS is plugged to the main line the internal Startup Cell is biased and starts to charge the external capacitor C_{VCC} which is connected to the VCC pin. The VCC charge current that is provided by the Startup Cell from the Drain pin is 1.05 mA. When V_{VCC} exceeds the on-threshold $V_{CCon}=18$ V, bias circuit is switched on. Then the Startup Cell is switched off by the Undervoltage Lockout and therefore no power losses present due to the connection of the Startup Cell to the Drain voltage. To avoid uncontrolled ringing at switch-on a hysteresis is implemented. The switch-off of the controller can only take place after Active Mode was entered and V_{VCC} falls below 10.3V.

The maximum current consumption before the controller is activated is about 300 μ A.

When V_{VCC} falls below the off-threshold $V_{CCoff}=10.3$ V the bias circuit is switched off and the Power Down reset let T1 discharging the soft-start capacitor C_{SoftS} at pin SoftS. Thus it is ensured that at every startup cycle the voltage ramp at pin SoftS starts at zero.

The bias circuit is switched off if Auto Restart Mode is entered. The current consumption is then reduced to 300 μ A.

Once the malfunction condition is removed, this block will then turn back on. The recovery from Auto Restart Mode does not require disconnecting the SMPS from the AC line.

When Active Burst Mode is entered, some internal Bias is switched off in order to reduce the current consumption to about 500 μ A while keeping a comparator (which trigger if V_{FB} has exceeded 3.61 V) and the Soft Start capacitor clamped at 3.0 V as this is necessary in this mode.

Functional Description

3.3 Startup Phase

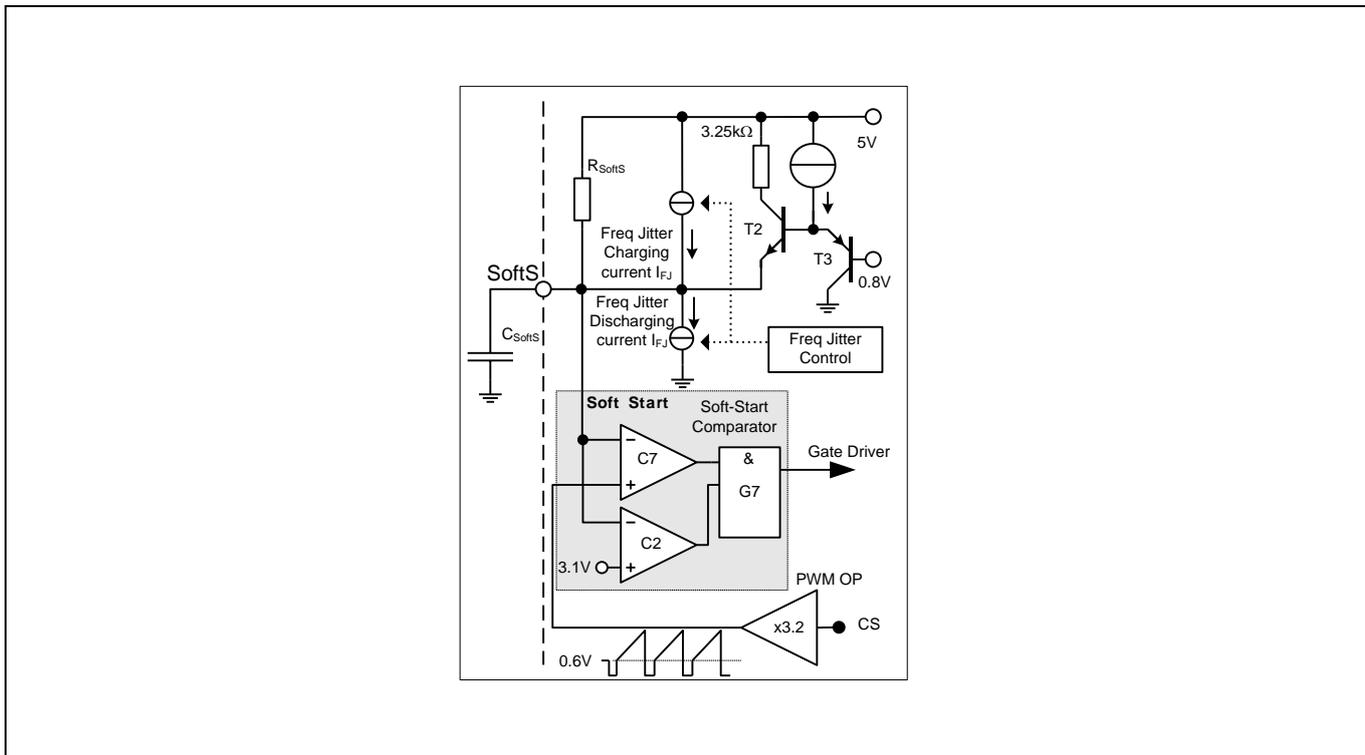


Figure 5 Soft Start

At the beginning of the Startup Phase, the IC provides a Soft Start duration whereby it controls the maximum primary current by means of a duty cycle limitation. A capacitor C_{SoftS} in combination with the internal pull up resistor R_{SoftS} determines the duty cycle until V_{SoftS} exceeds 3.1 V.

When the Soft Start begins, C_{SoftS} is immediately charged up to approx. 0.8 V by T2. Therefore the Soft Start Phase takes place between 0.8 V and 3.1 V. Above $V_{SoftS} = 3.1$ V there is no longer duty cycle limitation DC_{max} which is controlled by comparator C7 since comparator C2 blocks the gate G7 (see Figure 5). This maximum charge current in the very first stage when V_{SoftS} is below 0.8 V, is limited to 1.5 mA.

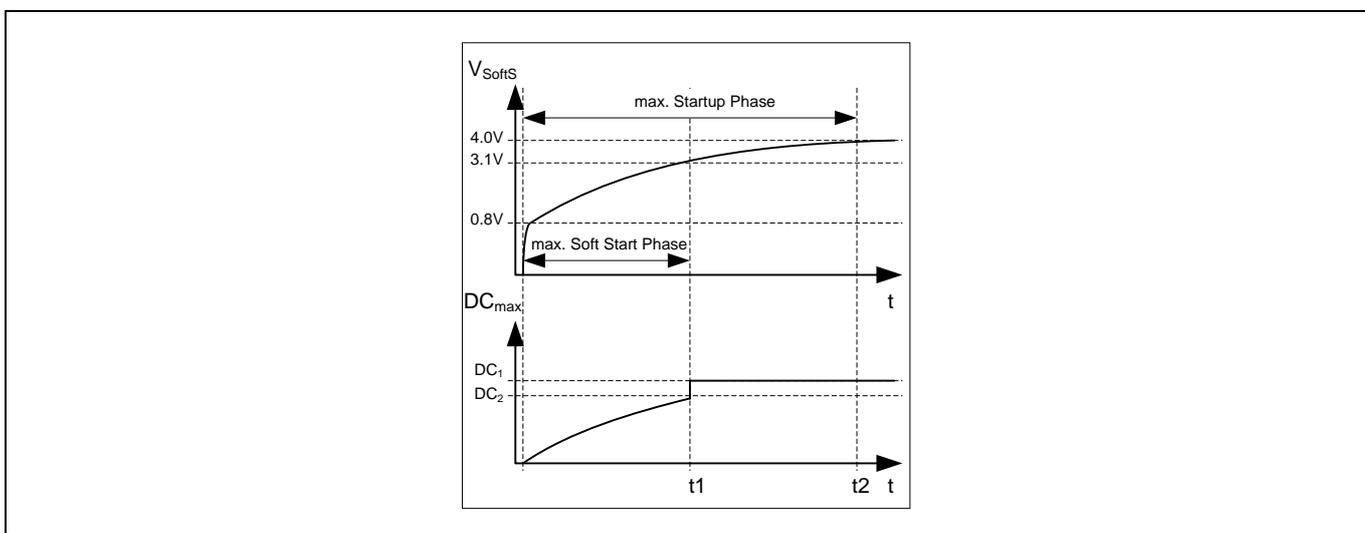


Figure 6 Startup Phase

Functional Description

By means of this extra charge stage, there is no delay in the beginning of the Startup Phase when there is still no switching. Furthermore Soft Start is finished at 3.1 V to have faster the maximum power capability. The duty cycles DC_1 and DC_2 are depending on the mains and the primary inductance of the transformer. The limitation of the primary current by DC_2 is related to $V_{SoftS} = 3.1$ V. But DC_1 is related to a maximum primary current which is limited by the internal Current Limiting with $CS = 1$ V. Therefore the maximum Startup Phase is divided into a Soft Start Phase until t_1 and a phase from t_1 until t_2 where maximum power is provided if demanded by the FB signal.

3.4 PWM Section

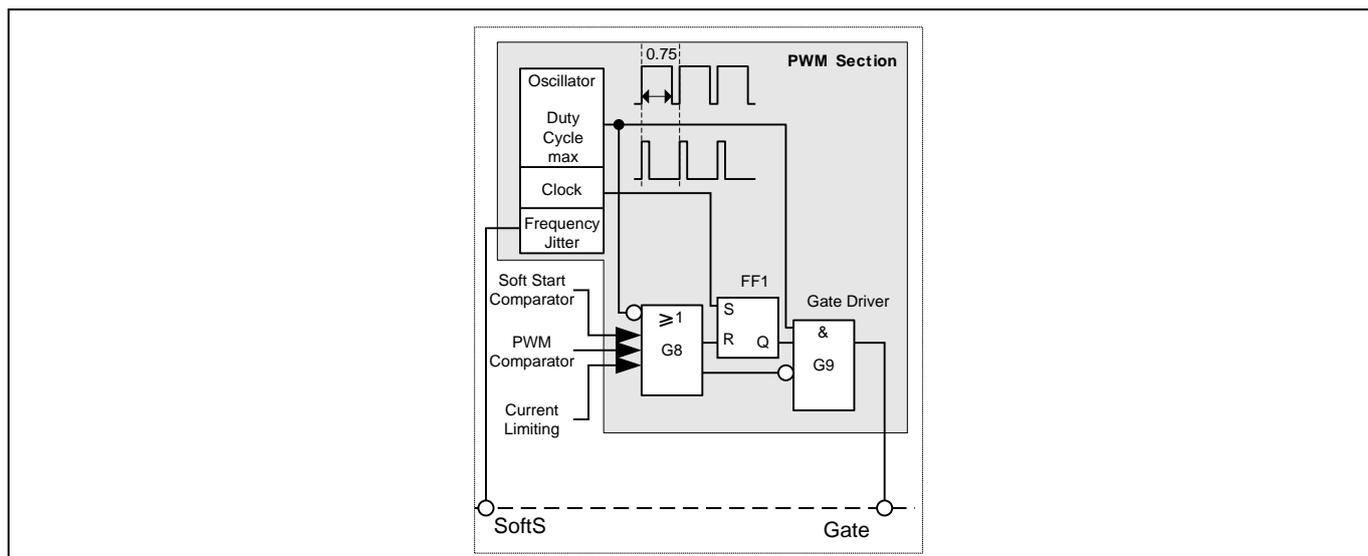


Figure 7 PWM Section

3.4.1 Oscillator and Jittering

The oscillator generates a fixed frequency with frequency jittering of $\pm 4\%$ from the fixed frequency (which is ± 2.7 kHz from 67 kHz) at a jittering period T_{FJ} . The switching frequency of ICE3B0x65JG is $f_{switch} = 67$ kHz.

A resistor, a capacitor and a current source and current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed, in order to achieve a very accurate switching frequency. The ratio of controlled charge to discharge current is adjusted to reach a maximum duty cycle limitation of $D_{max} = 0.75$.

Once the Soft Start period is over and when the IC goes into normal mode, the Soft Start capacitor will be charged and discharged through internal current source, I_{FJ} to generate a triangular waveform with a jittering period, T_{FJ} which is externally adjustable by the Soft Start capacitor, C_{SoftS} (See Figure 5).

$$T_{FJ} = k_{FJ} * C_{SoftS}$$

where k_{FJ} is a constant = 4 ms/ μ F

eg. $T_{FJ} = 4$ ms if $C_{SoftS} = 1$ μ F

Functional Description

3.4.2 PWM-Latch FF1

The oscillator clock output provides a set pulse to the PWM-Latch when initiating the internal CoolMOS™ conduction. After setting the PWM-Latch can be reset by the PWM comparator, the Soft Start comparator or the Current-Limit comparator. In case of resetting the driver is shut down immediately.

3.4.3 Gate Driver

The Gate Driver is a fast totem pole gate drive which is designed to avoid cross conduction currents.

The Gate Driver is active low at voltages below the undervoltage lockout threshold V_{VCCoff} .

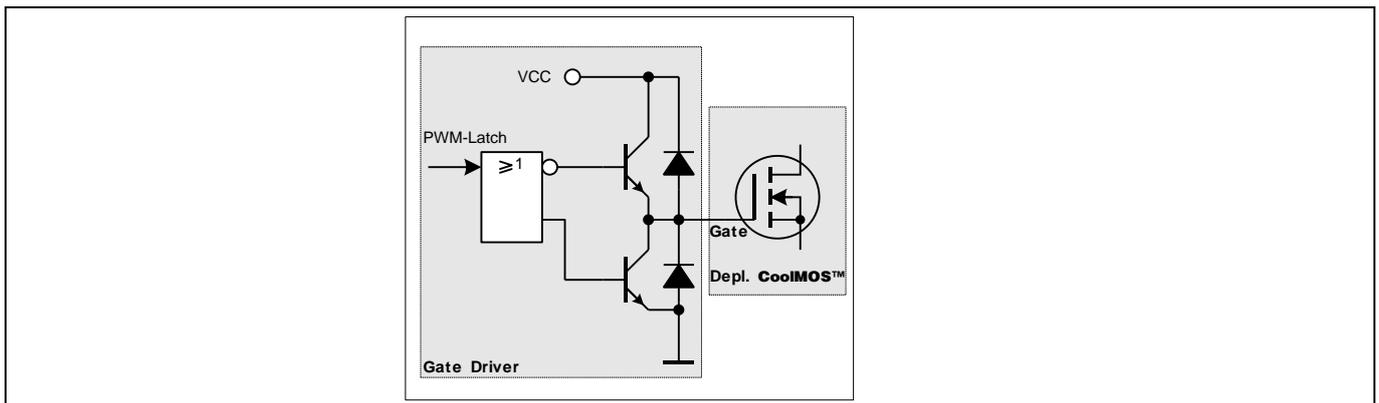


Figure 8 Gate Driver

3.5 Current Limiting

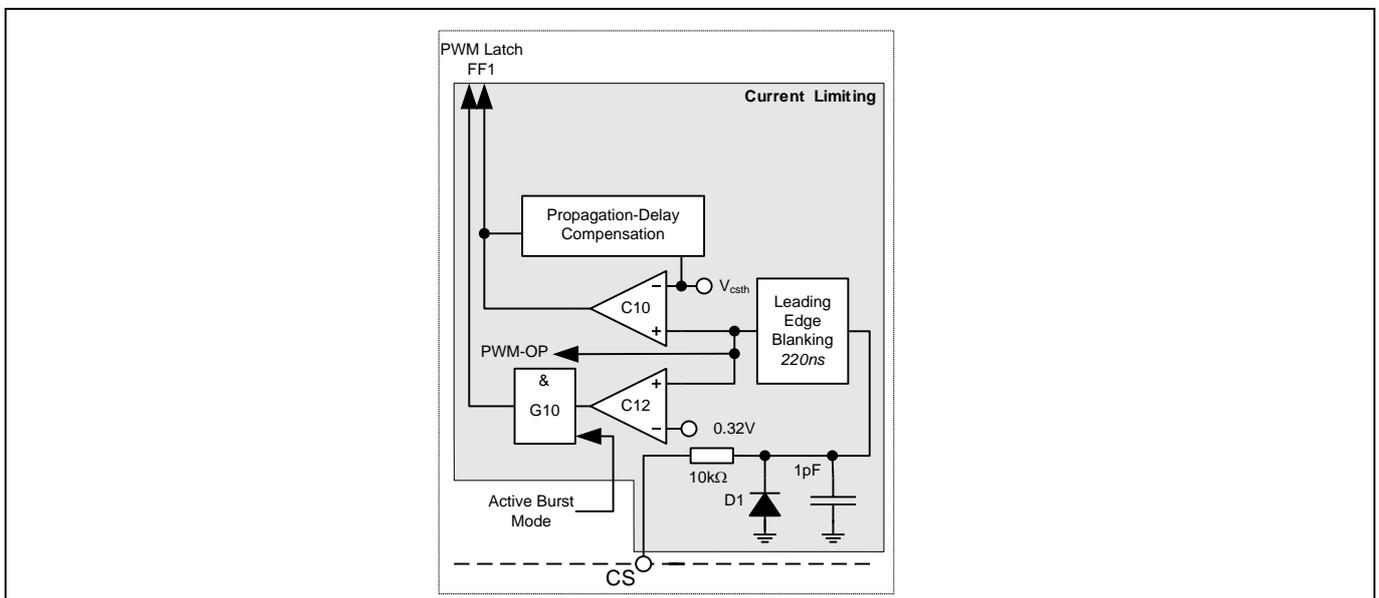


Figure 9 Current Limiting

There is a cycle by cycle Current Limiting realized by the Current-Limit comparator C10 to provide an overcurrent detection. The source current of the integrated Depl. CoolMOS™ is sensed via an external sense resistor R_{Sense} . By means of R_{Sense} the source current is transformed to a sense voltage V_{Sense} which is fed into the pin CS. If the voltage V_{Sense} exceeds the internal threshold voltage V_{csth} the comparator C10 immediately turns off the gate drive by resetting the PWM Latch FF1. A Propagation Delay Compensation is added to support the immediate shut down without delay of the integrated internal CoolMOS™ in case of

Functional Description

Current Limiting. The influence of the AC input voltage on the maximum output power can thereby be avoided.

To prevent the Current Limiting from distortions caused by leading edge spikes a Leading Edge Blanking is integrated in the current sense path for the comparators C10, C12 and the PWM-OP.

The output of comparator C12 is activated by the Gate G10 if Active Burst Mode is entered. Once activated the current limiting is thereby reduced to 0.32 V. This voltage level determines the power level when the Active Burst Mode is left if there is a higher power demand.

3.5.1 Leading Edge Blanking

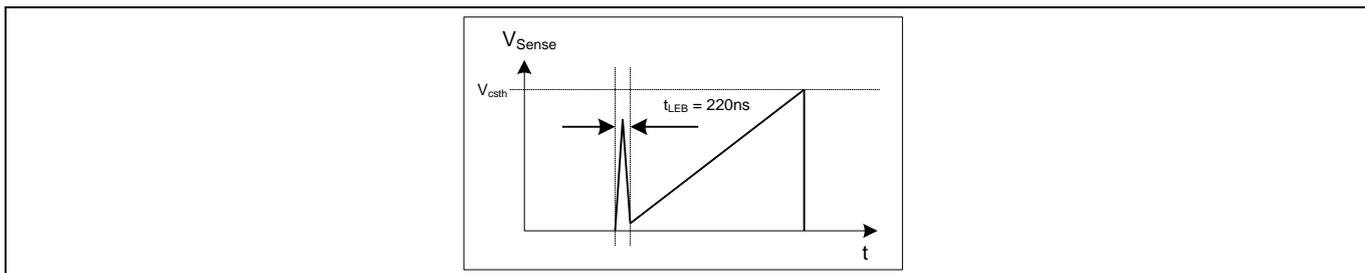


Figure 10 Leading Edge Blanking

Each time when the integrated internal CoolMOS™ is switched on a leading edge spike is generated due to the primary-side capacitances and secondary-side rectifier reverse recovery time. This spike can cause the gate drive to switch off unintentionally. To avoid a premature termination of the switching pulse, this spike is blanked out with a time constant of $t_{LEB} = 220$ ns. During this time, the gate drive will not be switched off.

3.5.2 Propagation Delay Compensation

In case of overcurrent detection, the switch-off of the integrated internal CoolMOS™ is delayed due to the propagation delay of the circuit. This delay causes an overshoot of the peak current I_{peak} which depends on the ratio of di/dt of the peak current (see Figure 10).

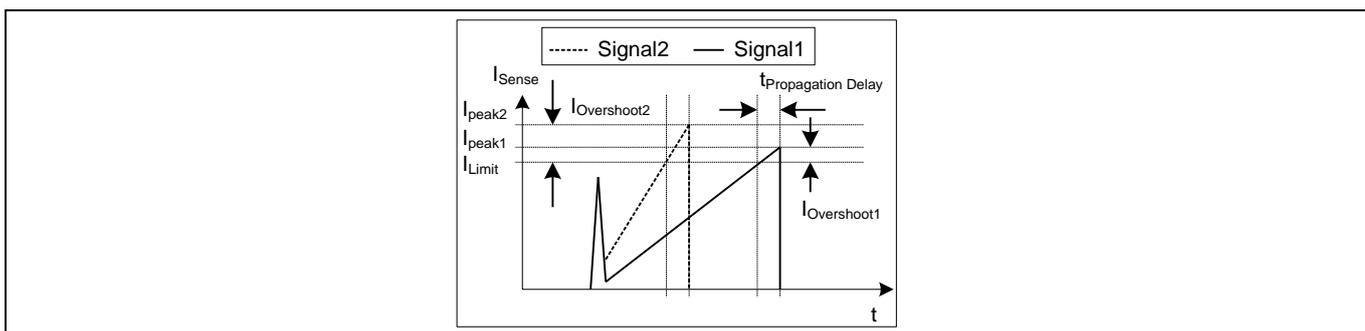


Figure 11 Current Limiting

The overshoot of Signal2 is bigger than of Signal1 due to the steeper rising waveform. This change in the slope is depending on the AC input voltage. Propagation Delay Compensation is integrated to limit the overshoot dependency on di/dt of the rising primary current. That means the propagation delay time between exceeding the current sense threshold V_{csth} and the switch off of the integrated internal CoolMOS™ is compensated over temperature within a wide range.

Functional Description

Current Limiting is now possible in a very accurate way.

E.g. $I_{peak} = 0.5\text{ A}$ with $R_{sense} = 2\ \Omega$. Without Propagation Delay Compensation the current sense threshold is set to a static voltage level $V_{csth} = 1\text{ V}$. A current ramp of $di/dt = 0.4\text{ A}/\mu\text{s}$, that means $dV_{sense}/dt = 0.8\text{ V}/\mu\text{s}$, and a propagation delay time of i.e. $t_{Propagation\ Delay} = 180\text{ ns}$ leads then to an I_{peak} overshoot of 14.4%. By means of propagation delay compensation the overshoot is only about 2% (see Figure 12).

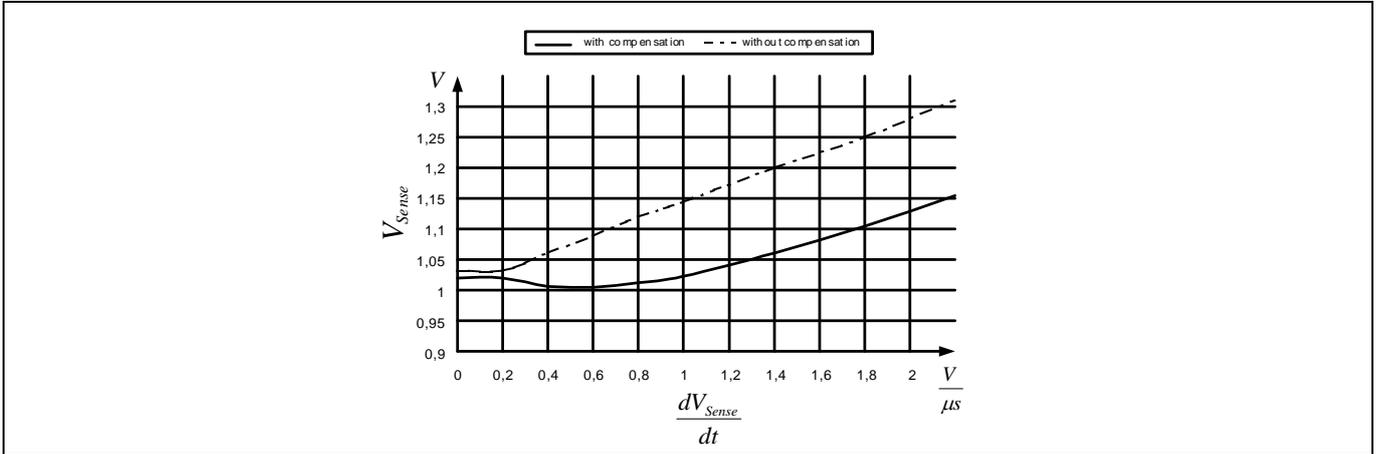


Figure 12 Overcurrent Shutdown

The Propagation Delay Compensation is realized by means of a dynamic threshold voltage V_{csth} (see Figure 13). In case of a steeper slope the switch off of the driver is earlier to compensate the delay.

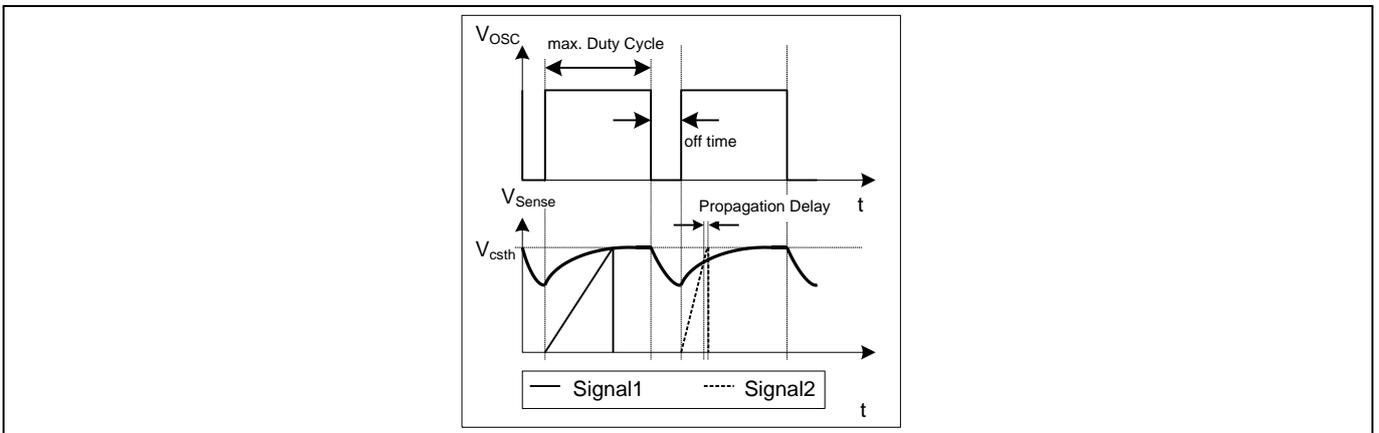


Figure 13 Dynamic Voltage Threshold V_{csth}

3.6 Control Unit

The Control Unit contains the functions for Active Burst Mode and Auto Restart Mode. The Active Burst Mode and the Auto Restart Mode are combined with an Adjustable Blanking Window which is depending on the external Soft Start capacitor. By means of this Adjustable Blanking Window, the IC avoids entering into these two modes accidentally. Furthermore it also provides a certain time whereby the overload detection is delayed. This delay is useful for applications which normally works with a low current and occasionally require a short duration of high current.

Functional Description

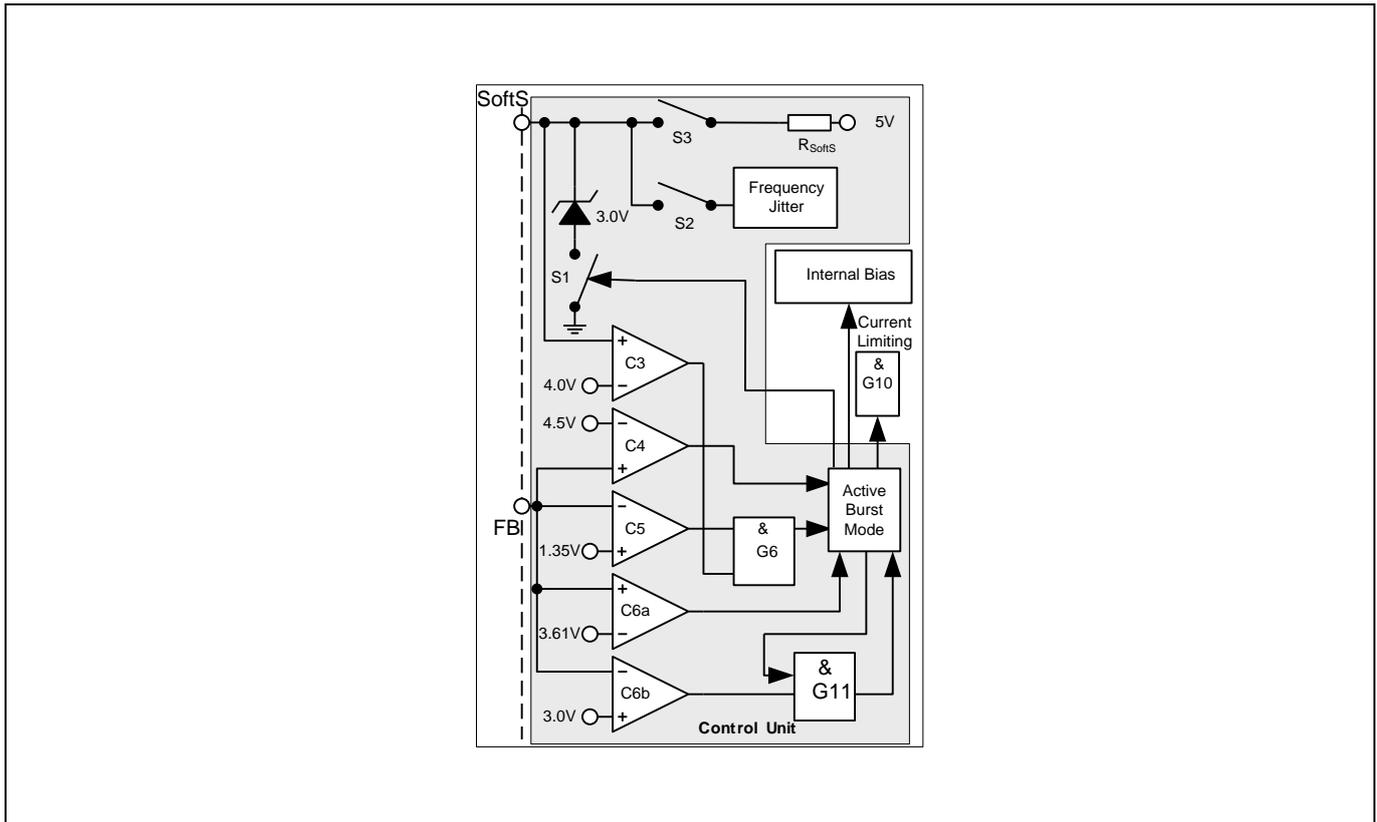


Figure 15 Active Burst Mode

The Active Burst Mode is located in the Control Unit. Figure 15 shows the related components.

3.6.2.1 Entering Active Burst Mode

The FB signal is always observed by the comparator C5 if the voltage level falls below 1.35 V. In that case the switch S1 and S2 is released which allow the capacitor C_{SoftS} to be charged via S3 starting from the swinging voltage level between 3.2 V and 3.6 V in normal operating mode. If V_{SoftS} exceeds 4.0 V the comparator C3 releases the gate G6 to enter the Active Burst Mode. The time window that is generated by combining the FB and SoftS signals with gate G6 avoids a sudden entering of the Active Burst Mode due to large load jumps. This time window can be adjusted by the external capacitor C_{SoftS} .

After entering Active Burst Mode a burst flag is set and the internal bias is switched off in order to reduce the current consumption of the IC down to approx. 500 μ A. Also, switch S1 is closed to clamp the Soft Start voltage to 3.0 V. In this Off State Phase the IC is no longer self supplied so that therefore V_{CC} has to provide the VCC current (see Figure 16). Furthermore gate G11 is then released to start the next burst cycle once V_{FB} has 3.0 V exceeded.

It has to be ensured by the application that the VCC remains above the Undervoltage Lockout Level of 10.3 V to avoid that the Startup Cell is accidentally switched on. Otherwise power losses are significantly increased. The minimum VCC level during Active Burst Mode is depending on the load conditions and the application. The lowest VCC level is reached at no load conditions at V_{OUT} .

3.6.2.2 Working in Active Burst Mode

After entering the Active Burst Mode the FB voltage rises as V_{OUT} starts to decrease due to the inactive PWM section. Comparator C6a observes the FB signal if the voltage level 3.6 V is exceeded. In that case the internal circuit is again activated by the internal Bias to start with switching. As now in Active Burst Mode

Functional Description

the gate G10 is released the current limit is only 0.32 V to reduce the conduction losses and to avoid audible noise. If the load at V_{OUT} is still below the starting level for the Active Burst Mode the FB signal decreases down to 3.0 V. At this level C6b deactivates again the internal circuit by switching off the internal Bias. The gate G11 is released as after entering Active Burst Mode the burst flag is set. If working in Active Burst Mode the FB voltage is changing like a saw tooth between 3.0 V and 3.61 V (see Figure 16).

3.6.2.3 Leaving Active Burst Mode

The FB voltage immediately increases if there is a high load jump. This is observed by comparator C4. As the current limit is ca. 32% during Active Burst Mode a certain load jump is needed that FB can exceed 4.5 V. At this time C4 resets the Active Burst Mode which also blocks C12 by the gate G10. Maximum current can now be provided to stabilize V_{OUT} .

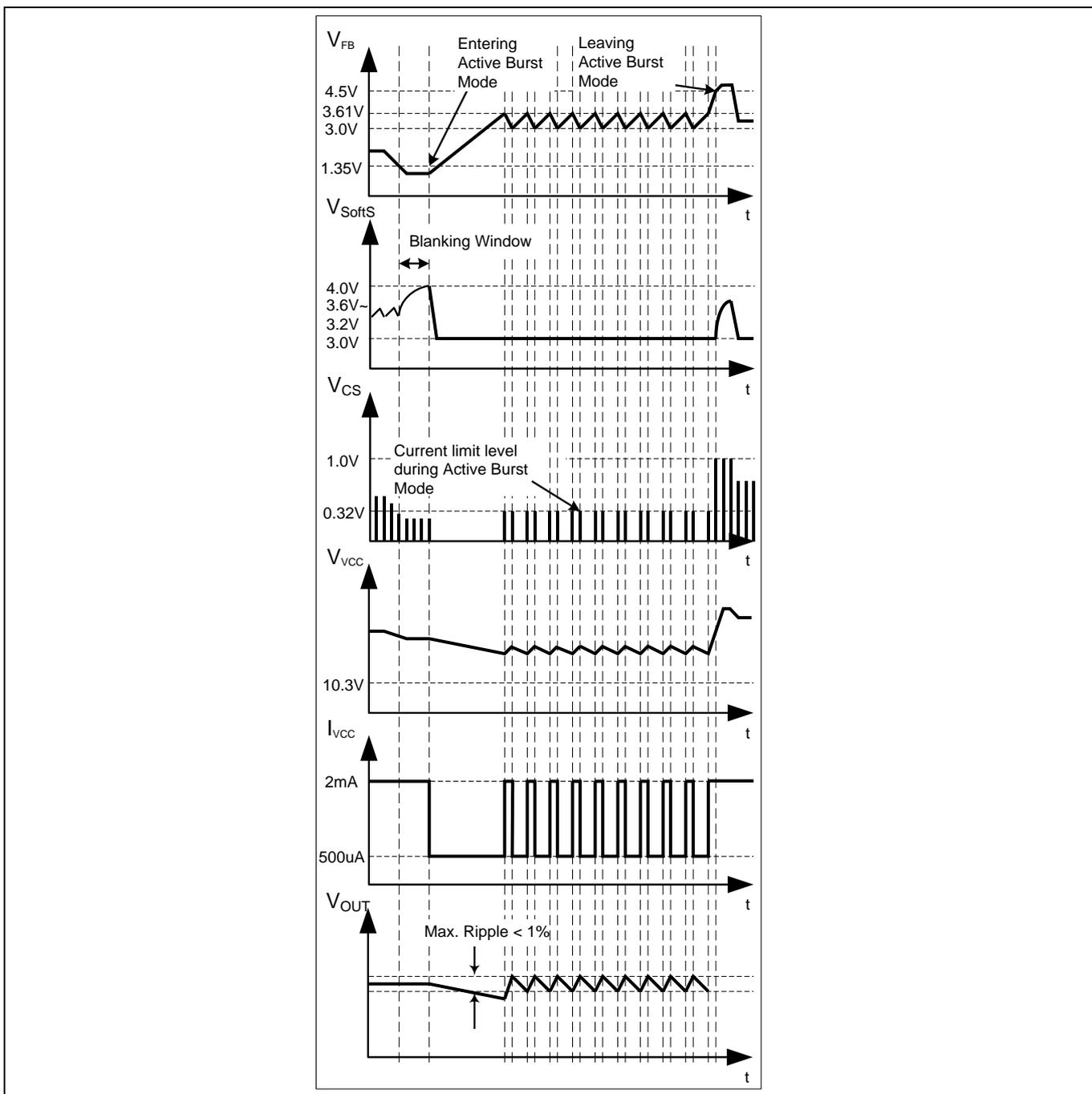


Figure 16 Signals in Active Burst Mode

Functional Description

3.6.3 Protection Modes

The IC provides several protection features that increase the SMPS system’s robustness and safety. The following table shows the possible system failures and the corresponding protection modes.

Table 2 Protection Modes

Protection function	Protection Mode
VCC Overvoltage	Auto Restart Mode I
Over temperature	Auto Restart Mode I
Over load	Auto Restart Mode II
Open Loop	Auto Restart Mode II
VCC Undervoltage	Auto Restart Mode II
Short Optocoupler	Auto Restart Mode II

3.6.3.1 Auto Restart Mode I

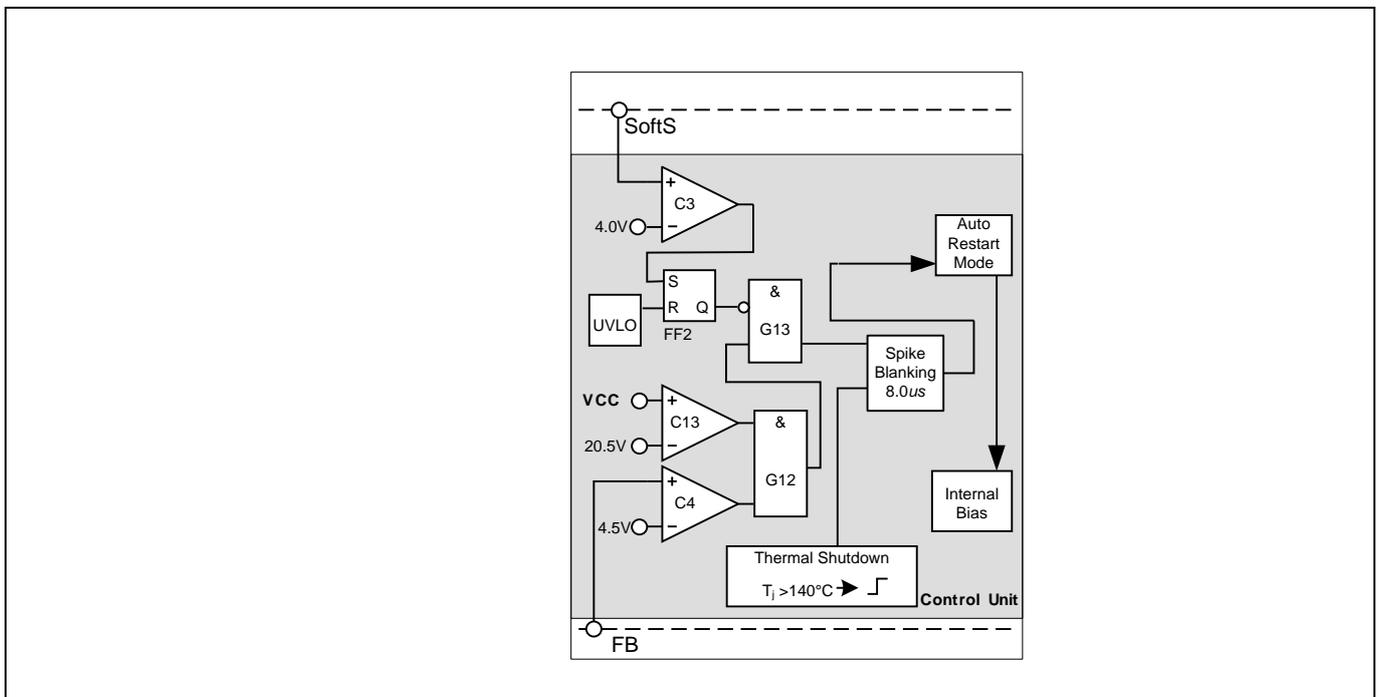


Figure 17 Auto Restart Mode I

The VCC voltage is observed by comparator C13 if 20.5 V is exceeded. The output of C13 is combined with both the output of C3 which checks for $V_{Softs} < 4.0V$ and the output of C4 which checks for $V_{FB} > 4.5V$. Therefore the overvoltage detection can only be active during Soft Start Phase ($V_{Softs} < 4.0V$) and when FB signal is outside the operating range $> 4.5V$. This means any small voltage overshoots of V_{VCC} during normal operating cannot trigger the Auto Restart Mode I.

In Order to ensure system reliability and prevent any false activation, a blanking time is implemented before the IC can enter into the Auto Restart Mode I. The output of the VCC overvoltage detection is fed into a spike blanking with a time constant of 8.0 µs.

The other fault detection which can result in the Auto Restart Mode I and has this 8.0 µs blanking time is the Overtemperature detection. This block checks for a junction temperature of higher than 140°C for malfunction operation.

Functional Description

Once Auto Restart Mode is entered, the internal bias is switched off in order to reduce the current consumption of the IC as much as possible. In this mode, the average current consumption is only 300 μA as the only working blocks are the reference block and the Undervoltage Lockout (UVLO) which controls the Startup Cell by switching on/off at V_{VCCon}/V_{VCCoff} .

As there is no longer a self supply by the auxiliary winding, VCC starts to drop. The UVLO switches on the integrated Startup Cell when VCC falls below 10.3 V. It will continue to charge VCC up to 18 V whereby it is switched off again and the IC enters into the Start Up Phase.

As long as all fault conditions have been removed, the IC will automatically power up as usual with switching cycle at the GATE output after Soft Start duration. Thus it is called Auto Restart Mode.

3.6.3.2 Auto Restart Mode II

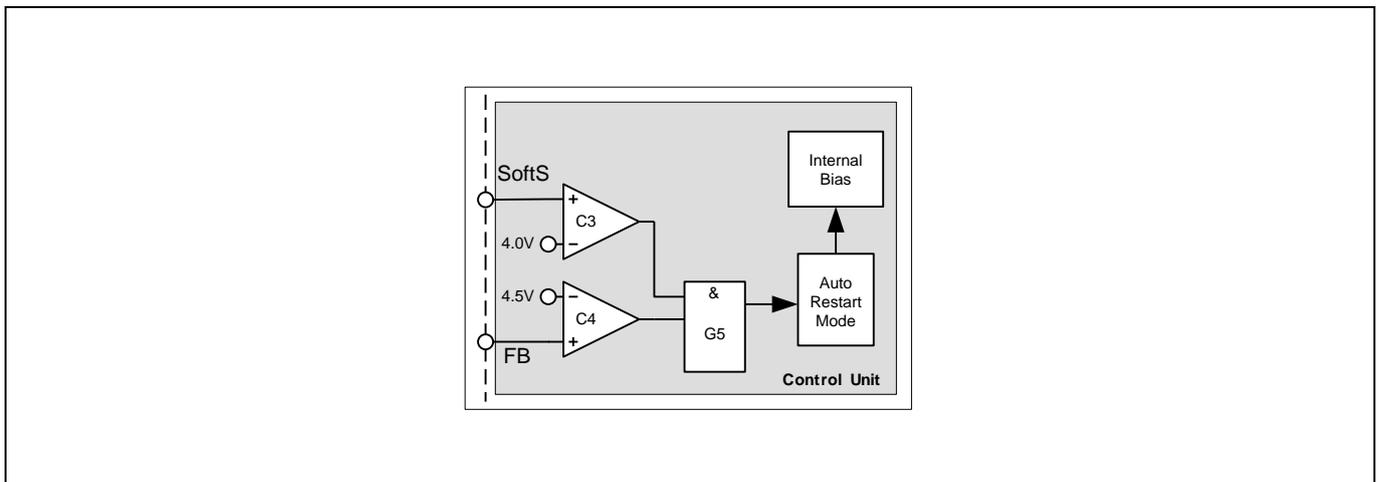


Figure 18 Auto Restart Mode II

In case of Overload or Open Loop, FB exceeds 4.5 V which will be observed by C4. At this time, the external Soft Start capacitor can now be charged further by the integrated pull up resistor R_{SoftS} via switch S3 (see Figure 14). If V_{SoftS} exceeds 4.0 V which is observed by C3, Auto Restart Mode II is entered as both inputs of the gate G5 are high.

This charging of the Soft Start capacitor from 3.2 V ~ 3.6 V to 4.0 V defines a blanking window which prevents the system from entering into Auto Restart Mode II unintentionally during large load jumps. In this event, FB will rise close to 5.0 V for a short duration before the loop regulates with FB less than 4.5 V. This is the same blanking time window as for the Active Burst Mode and can therefore be adjusted by the external C_{SoftS} .

In case of VCC undervoltage, i.e. VCC falls below 10.3 V, the IC will be turned off with the Startup Cell charging VCC as described earlier in this section. Once VCC is charged above 18 V, the IC will start a new startup cycle. The same procedure applies when the system is under Short Optocoupler fault condition, as it will lead to VCC undervoltage.

Electrical Characteristics

4 Electrical Characteristics

Note: All voltages are measured with respect to ground (Pin 12). The voltage levels are valid if other ratings are not violated.

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 11 (VCC) is discharged before assembling the application circuit. $T_o=25^{\circ}\text{C}$ unless otherwise specified.

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Drain Source Voltage	V_{DS}	-	650	V	$T_j=110^{\circ}\text{C}$
Pulse drain current, pulse width t_p limited by $T_j=150^{\circ}\text{C}$	ICE3B0365JG	I_{D_Plus1}	-	1.6	A
	ICE3B0565JG	I_{D_Plus2}	-	2.3	A
Avalanche energy, repetitive t_{AR} limited by max. $T_j=150^{\circ}\text{C}^1$	ICE3B0365JG	E_{AR1}	-	0.005	mJ
	ICE3B0565JG	E_{AR2}	-	0.01	mJ
Avalanche current, repetitive t_{AR} limited by max. $T_j=150^{\circ}\text{C}^1$	ICE3B0365JG	I_{AR1}	-	0.3	A
	ICE3B0565JG	I_{AR2}	-	0.5	A
VCC Supply Voltage	V_{VCC}	-0.3	27	V	
FB Voltage	V_{FB}	-0.3	5.0	V	
SoftS Voltage	V_{SoftS}	-0.3	5.0	V	
CS Voltage	V_{CS}	-0.3	5.0	V	
Junction Temperature	T_j	-40	150	$^{\circ}\text{C}$	Controller & CoolMOS™
Storage Temperature	T_s	-55	150	$^{\circ}\text{C}$	
Thermal Resistance (Junction–Ambient)	R_{thJA}	-	110	K/W	PG-DSO-16/12
ESD Capability	V_{ESD}	-	2	kV	Human body model ²

¹ Repetitive avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR} \cdot f$

² According to EIA/JESD22-A114-B (discharging a 100 pF capacitor through a 1.5 kΩ series resistor)

Electrical Characteristics

4.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Table 4 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC Supply Voltage	V_{VCC}	V_{VCCoff}	26	V	
Junction Temperature of Controller	T_{jCon}	-25	130	°C	Max value limited due to thermal shut down of controller
Junction Temperature of CoolMOS™	$T_{jCoolMOS}$	-25	150	°C	

4.3 Characteristics

4.3.1 Supply Section

Note: The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_j from -25 °C to 130 °C . Typical values represent the median values, which are related to 25 °C . If not otherwise stated, a supply voltage of $V_{VCC} = 18\text{ V}$ is assumed.

Table 5 Supply Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Start Up Current	$I_{VCCstart}$	-	300	450	μA	$V_{VCC} = 17\text{ V}$
VCC Charge Current	$I_{VCCcharge1}$	-	-	5.0	mA	$V_{VCC} = 0\text{ V}$
	$I_{VCCcharge2}$	0.55	1.05	1.60	mA	$V_{VCC} = 1\text{ V}$
	$I_{VCCcharge3}$	-	0.88	-	mA	$V_{VCC} = 17\text{ V}$
Leakage Current of Start Up Cell and CoolMOS™	$I_{startLeak}$	-	0.2	50	μA	$V_{Drain} = 450\text{ V}$ at $T_j = 100\text{ °C}$
Supply Current with Inactive Gate	I_{VCCsup_ng}	-	1.7	2.5	mA	Soft Start pin is open
Supply Current with Active Gate	I_{VCCsup_g}	-	2.5	3.6	mA	$V_{SoftS} = 3.0\text{ V}$, $I_{FB} = 0\text{ A}$
Supply Current in Auto Restart Mode with Inactive Gate	$I_{VCCrestart}$	-	300	-	μA	$I_{FB} = 0\text{ A}$, $I_{SoftS} = 0\text{ A}$
Supply Current in Active Burst Mode with Inactive Gate	$I_{VCCburst1}$	-	500	950	μA	$V_{FB} = 2.5\text{ V}$, $V_{SoftS} = 3.0\text{ V}$
	$I_{VCCburst2}$	-	500	950	μA	$V_{VCC} = 11.5\text{ V}$, $V_{FB} = 2.5\text{ V}$, $V_{SoftS} = 3.0\text{ V}$

Electrical Characteristics

VCC Turn-On Threshold	V _{VCCon}	17.0	18.0	19.0	V	
VCC Turn-Off Threshold	V _{VCCoff}	9.6	10.3	11.0	V	
VCC Turn-On/Off Hysteresis	V _{VCChys}	-	7.7	-	V	

4.3.2 Internal Voltage Reference

Table 6 Internal Voltage Reference

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Trimmed Reference Voltage	V _{REF}	4.90	5.00	5.10	V	measured at pin FB, I _{FB} = 0

4.3.3 PWM Section

Table 7 PWM Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Fixed Oscillator Frequency	f _{OSC1}	58	67	76	kHz	
	f _{OSC2}	62	67	74.5		
Frequency Jittering Range	f _{delta}	-	±2.7	-	kHz	T _j = 25°C
Max. Duty Cycle	D _{max}	0.70	0.75	0.80		
Min. Duty Cycle	D _{min}	0	-	-		V _{FB} < 0.3 V
PWM-OP Gain	A _V	3.0	3.2	3.4		
Max. Level of Voltage Ramp	V _{max-Ramp}	-	0.6	-	V	
V _{FB} Operating Range Min Level	V _{FBmin}	-	0.5	-	V	
V _{FB} Operating Range Max level	V _{FBmax}	-	-	4.3	V	CS=1 V, limited by Comparator C4 ¹
FB Pull-Up Resistor	R _{FB}	9	14	22	kΩ	
Soft_Start Pull-Up Resistor	R _{SoftS}	30	45	62	kΩ	

¹ The parameter is not subjected to production test - verified by design/characterization

Electrical Characteristics

4.3.4 Control Unit

Table 8 Control Unit

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Deactivation Level for SoftS Comparator C7 by C2	V _{SoftSC2}	2.98	3.10	3.22	V	V _{FB} = 5 V
Clamped V _{SoftS} Voltage during Burst Mode	V _{SoftSclmp_bm}	2.88	3.0	3.12	V	
Activation limit for Comparator C3	V _{SoftSC3}	3.85	4.00	4.15	V	V _{FB} = 5 V
SoftS Startup Current	I _{SoftSstart}	-	0.9	-	mA	V _{SoftS} = 0 V
Over Load & Open Loop Detection Limit for Comparator C4	V _{FBC4}	4.33	4.50	4.67	V	V _{SoftS} = 4.5 V
Active Burst Mode Level for Comparator C5	V _{FBC5}	1.23	1.35	1.43	V	V _{SoftS} = 4.5 V
Active Burst Mode Level for Comparator C6a	V _{FBC6a}	3.48	3.61	3.76	V	After Active Burst Mode is entered
Active Burst Mode Level for Comparator C6b	V _{FBC6b}	2.88	3.00	3.12	V	After Active Burst Mode is entered
Overvoltage Detection Limit	V _{VCCOVP}	19.5	20.5	21.5	V	V _{FB} = 5 V, V _{SoftS} = 3.0 V
Thermal Shutdown ¹	T _{JSD}	130	140	150	°C	
Spike Blanking	t _{Spike}	-	8	-	µs	

Note: The trend of all voltage levels in the Control Units is the same regarding the deviation except V_{VCCOVP}

4.3.5 Current Limiting

Table 9 Current Limiting

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Peak Current Limitation (incl. Propagation Delay) (see Figure 12)	V _{csth}	1.02	1.07	1.12	V	dV _{sense} /dt = 0.6 V/µs
Peak Current Limitation during Active Burst Mode	V _{CS2}	0.27	0.32	0.37	V	
Leading Edge Blanking	t _{LEB}	-	220	-	ns	V _{SoftS} = 3 V
CS Input Bias Current	I _{CSbias}	-1.0	-0.2	0	µA	V _{CS} = 0 V

¹ The parameter is not subjected to production test - verified by design/characterization. The thermal shutdown temperature refers to the junction temperature of the controller.

Electrical Characteristics

4.3.6 CoolMOS™ Section

Table 10 CoolMOS™ Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Drain Source Breakdown Voltage	$V_{(BR)DSS}$	600 650	- -	- -	V	$T_j = 25\text{ °C}$ $T_j = 110\text{ °C}$
Drain Source On-Resistance ICE3B0365JG	R_{DSon}	- -	6.45 13.70	7.50 17.00	Ω	$T_j = 25\text{ °C}$ $T_j = 125\text{ °C}^1$
ICE3B0565JG		- -	4.70 10.00	5.44 12.50		$T_j = 25\text{ °C}$ $T_j = 125\text{ °C}^1$
Effective output capacitance, energy related ICE3B0365JG	$C_{o(er)}$	-	3.65	-	pF	$V_{DS} = 0\text{ V to }480\text{ V}$
ICE3B0565JG		-	4.75			
Rise Time ²	t_{rise}	-	30	-	ns	
Fall Time ²	t_{fall}	-	30	-	ns	

¹ The parameter is not subjected to production test - verified by design/characterization

² Measured in a Typical Flyback Converter Application

Outline Dimension

5 Outline Dimension

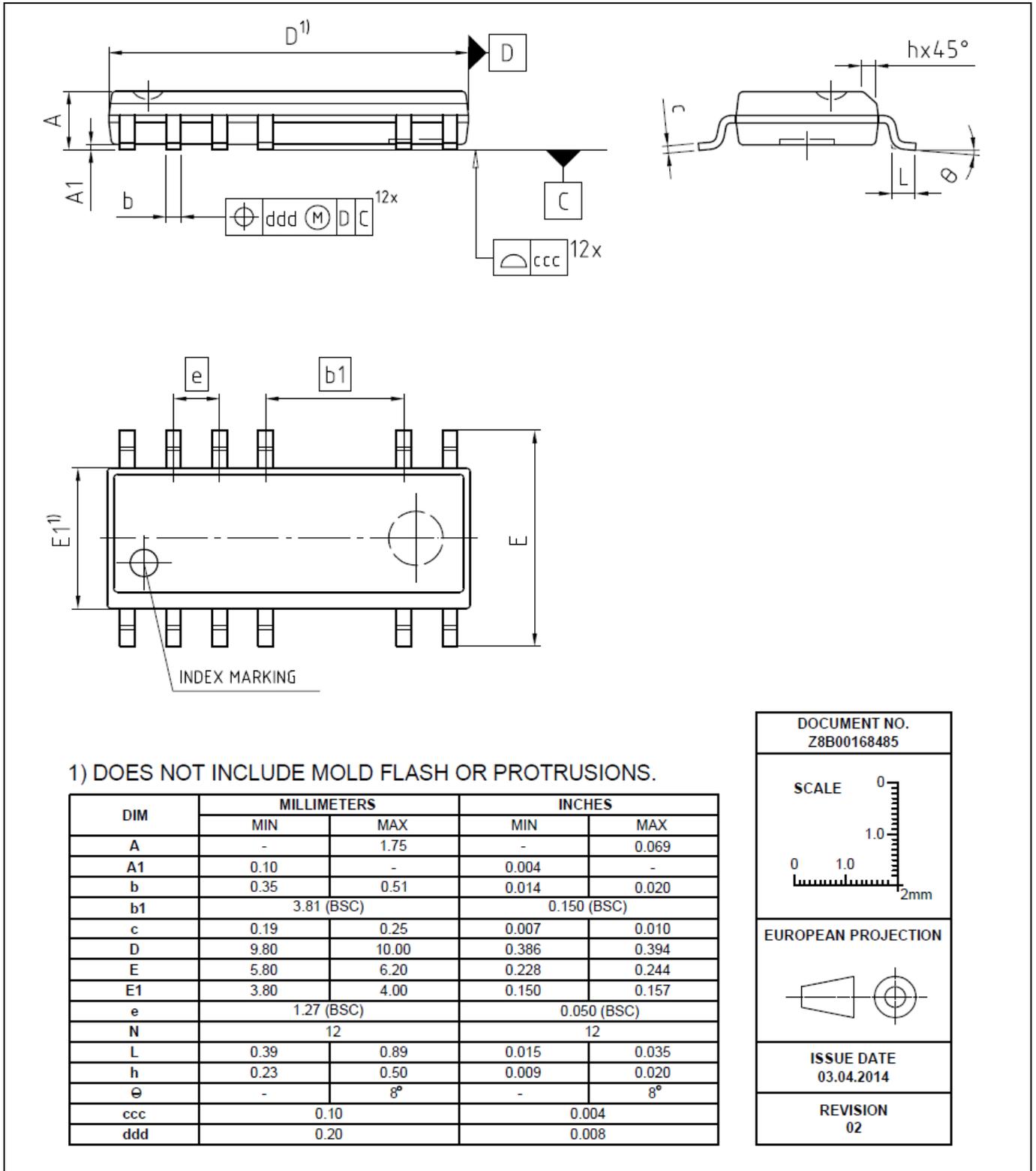


Figure 19 PG-DSO-12 (Pb-free lead plating Plastic Dual-in-Line Outline)

Marking

6 Marking

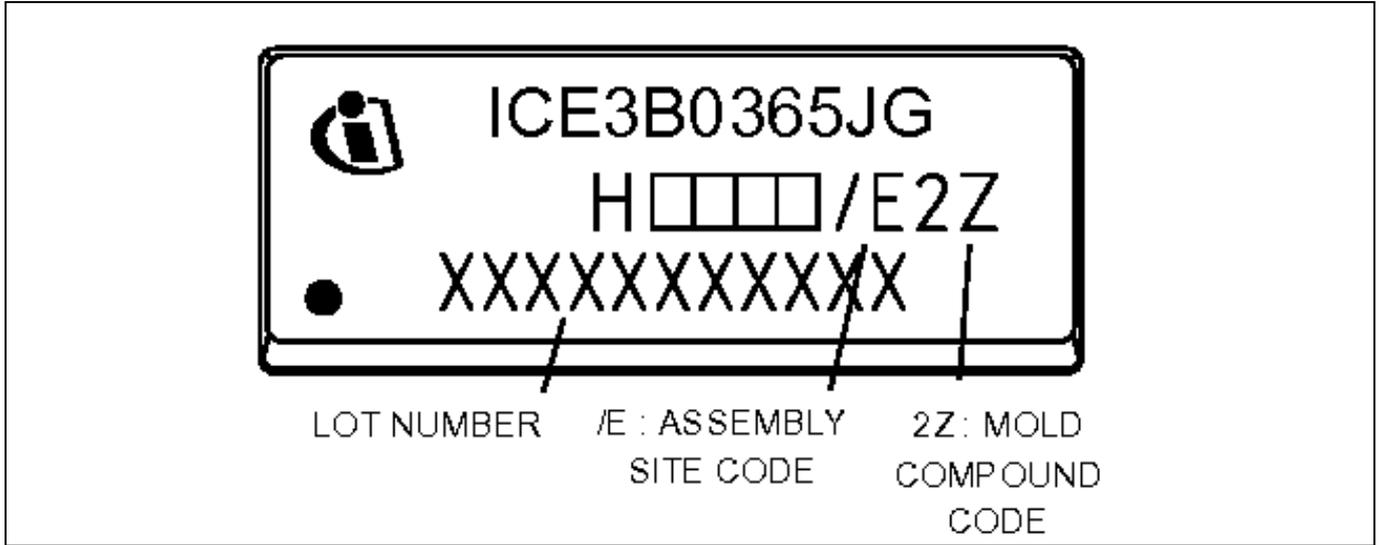


Figure 20 Marking for ICE3B0365JG

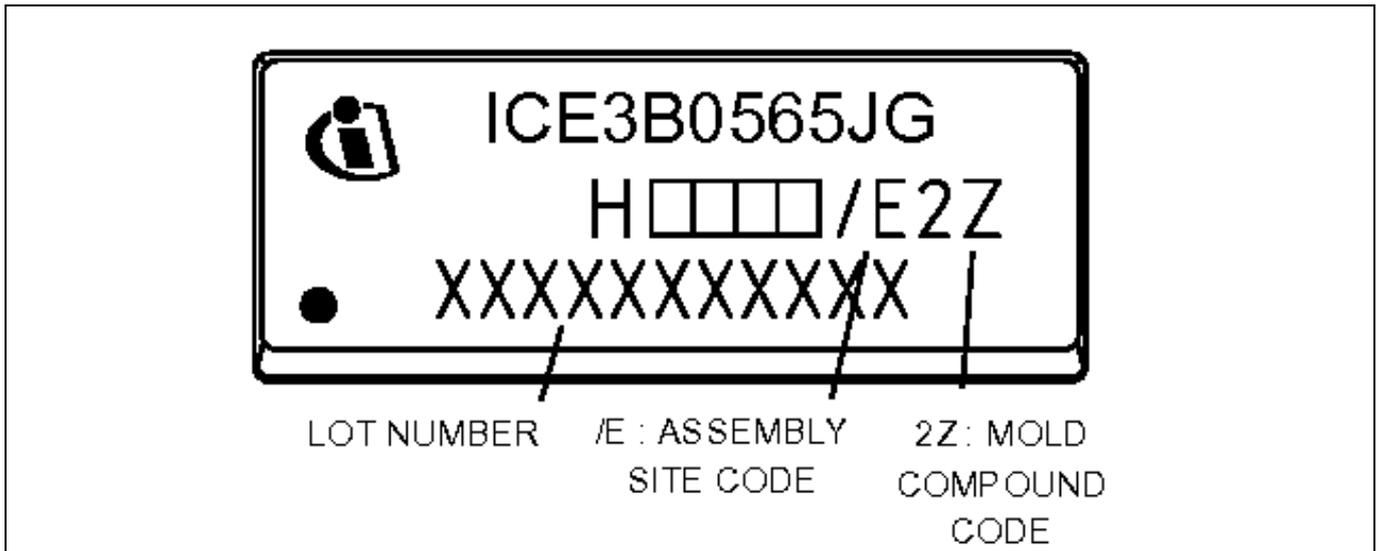


Figure 21 Marking for ICE3B0565JG

Schematic for recommended PCB layout

7 Schematic for recommended PCB layout

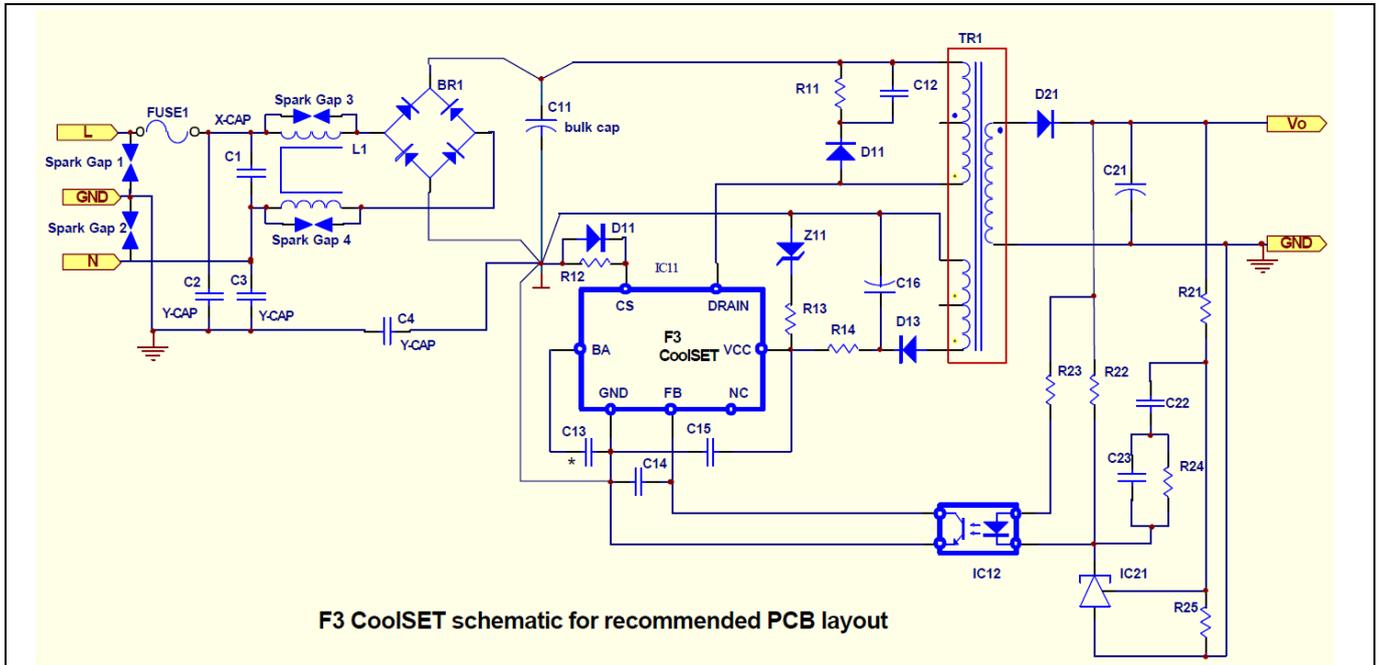


Figure 22 Schematic for recommended PCB layout

General guideline for PCB layout design using F3 CoolSET™ (Figure 22):

1. “Star Ground “at bulk capacitor ground, C11:

“Star Ground “means all primary DC grounds should be connected to the ground of bulk capacitor C11 separately in one point. It can reduce the switching noise going into the sensitive pins of the CoolSET™ device effectively. The primary DC grounds include the followings.

- a. DC ground of the primary auxiliary winding in power transformer, TR1, and ground of C16 and Z11.
- b. DC ground of the current sense resistor, R12
- c. DC ground of the CoolSET™ device, GND pin of IC11; the signal grounds from C13, C14, C15 and collector of IC12 should be connected to the GND pin of IC11 and then “star “connect to the bulk capacitor ground.
- d. DC ground from bridge rectifier, BR1
- e. DC ground from the bridging Y-capacitor, C4

2. High voltage traces clearance:

High voltage traces should keep enough spacing to the nearby traces. Otherwise, arcing would incur.

- a. 400 V traces (positive rail of bulk capacitor C11) to nearby trace: > 2.0 mm
- b. 600 V traces (drain voltage of CoolSET™ IC11) to nearby trace: > 2.5 mm

3. Filter capacitor close to the controller ground:

Filter capacitors, C13, C14 and C15 should be placed as close to the controller ground and the controller pin as possible so as to reduce the switching noise coupled into the controller.

Guideline for PCB layout design when > 3 kV lightning surge test applied (Figure 22)

1. Add spark gap

Schematic for recommended PCB layout

Spark gap is a pair of saw-tooth like copper plate facing each other which can discharge the accumulated charge during surge test through the sharp point of the saw-tooth plate.

a. Spark Gap 3 and Spark Gap 4, input common mode choke,
L1: Gap separation is around 1.5 mm (no safety concern)

b. Spark Gap 1 and Spark Gap 2, Live / Neutral to GROUND:

These 2 Spark Gaps can be used when the lightning surge requirement is > 6 kV.

230 V_{AC} input voltage application, the gap separation is around 5.5mm

115 V_{AC} input voltage application, the gap separation is around 3mm

2. Add Y-capacitor (C2 and C3) in the Live and Neutral to ground even though it is a 2-pin input

3. Add negative pulse clamping diode, D11 to the Current sense resistor, R12:

The negative pulse clamping diode can reduce the negative pulse going into the CS pin of the CoolSET™ and reduce the abnormal behavior of the CoolSET™. The diode can be a fast speed diode such as 1N4148.

The principle behind is to drain the high surge voltage from Live/Neutral to Ground without passing through the sensitive components such as the primary controller, IC11.

Revision history

Major changes since the last revision

Page or Reference	Description of change
1, 23	Revise wrong marking text

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