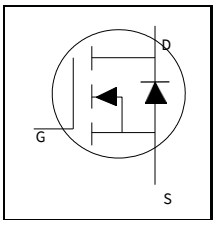
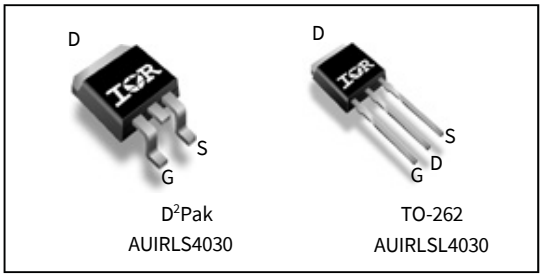
特性

- 针对逻辑电平驱动进行了优化
- 先进工艺技术
- 超低导通电阻
- 逻辑电平栅极驱动
- 工作温度 175°C
- 快速开关
- 允许达到 Tjmax 的重复雪崩
- 无铅，符合RoHS要求
- 汽车认证 *

HEXFET®功率MOSFET



V_{DSS}	100V
$R_{DS(on)}$ typ.	3.4mΩ
max	4.3mΩ
I_D	180A



G	D	S
Gate	Drain	Source

描述

这款HEXFET®功率MOSFET专为汽车应用而设计，采用最新的工艺技术实现单位硅面积极低的导通电阻。该设计的其他特点包括 175°C 工作结温、开关速度快和提高重复雪崩额定值。通过结合以上特点，使该设计成为一种极其高效和可靠的器件，可用于汽车应用和各种其他应用。

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRLSL4030	TO-262	Tube	50	AUIRLSL4030
AUIRLS4030	D²-Pak	Tube	50	AUIRLS4030
		Tape and Reel Left	800	AUIRLS4030TRL

绝对最大额定值

超过"绝对最大额定值"所列值的应力可能会对器件造成永久性损坏。这些仅仅是应力额定值，并不意味着器件在这些或任何其他超过该规范所示的条件下能够正常运行。延长暴露在绝对最大额定值条件的时间可能会影响器件的可靠性。热阻抗和功率耗散额定值是在装板和静止空气条件下测得的。环境温度（TA）为 25°C，除非另有规定。

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	180	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	130	
I_{DM}	Pulsed Drain Current ①	730	
P_D @T_C = 25°C	Power Dissipation	370	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy (Thermally limited) ②	305	mJ
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ①		mJ
dv/dt	Peak Diode Recovery ③	21	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature for 10 seconds	300(1.6mm from case)	

热阻抗

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦⑨	---	0.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount), D2 Pak⑧	---	40	

HEXFET® 是英飞凌的注册商标。

*认证标准可在 www.infineon.com 上找到

本数据手册的原文使用英文撰写。为方便起见，英飞凌提供了译文；由于翻译过程中可能使用了自动化工具，英飞凌不保证译文的准确性。 为确认准确性，请务必访问 infineon.com 参考最新的英文版本（控制文档）。

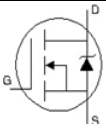
静态电气特性@T_J = 25°C（除非另有说明）

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	---	---	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	---	0.10	---	V/°C	Reference to 25°C, I_D = 5mA①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	---	3.4	4.3	mΩ	V_{GS} = 10V, I_D = 110A ④
		---	3.6	4.5		V_{GS} = 4.5V, I_D = 92A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	---	2.5	V	V_{DS} = V_{GS}, I_D = 250μA
gfs	Forward Trans conductance	320	---	---	S	V_{DS} = 25V, I_D = 110A
I_{DSS}	Drain-to-Source Leakage Current	---	---	20	μA	V_{DS} = 100V, V_{GS} = 0V
		---	---	250		V_{DS} = 100V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	---	---	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	---	---	-100		V_{GS} = -16V
R_G	Internal Gate Resistance	---	2.1	---	Ω	

动态电气特性在 T_J = 25°C时测得（除非另有规定）

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	---	87	130	nC	I_D = 110A V_{DS} = 50V V_{GS} = 4.5V ④
Q_{gs}	Gate-to-Source Charge	---	27	---		
Q_{gd}	Gate-to-Drain ("Miller") Charge	---	45	---		
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	---	42	---		
$t_{d(on)}$	Turn-On Delay Time	---	74	---	ns	V_{DD} = 65V I_D = 110A R_G = 2.7Ω V_{GS} = 4.5V ④
t_r	Rise Time	---	330	---		
$t_{d(off)}$	Turn-Off Delay Time	---	110	---		
t_f	Fall Time	---	170	---		
C_{iss}	Input Capacitance	---	11360	---	pF	V_{GS} = 0V V_{DS} = 50V f = 1.0 MHz
C_{oss}	Output Capacitance	---	670	---		
C_{rss}	Reverse Transfer Capacitance	---	290	---		
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	---	760	---		V_{GS} = 0V, V_{DS} = 0V to 80V ⑥
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)	---	1140	---		V_{GS} = 0V, V_{DS} = 0V to 80V ⑤

二极管特性

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	---	---	180	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	---	---	730		
V_{SD}	Diode Forward Voltage	---	---	1.3	V	T_J = 25°C, I_S = 110A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	---	50	---	ns	T_J = 25°C V_R = 85V, I_F = 110A di/dt = 100A/μs④
		---	60	---		T_J = 125°C
Q_{rr}	Reverse Recovery Charge	---	88	---	nC	T_J = 25°C
		---	130	---		T_J = 125°C
I_{RRM}	Reverse Recovery Current	---	3.3	---	A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

注：

① 重复额定值；脉冲宽度受最高结温限制。

② 受 T_{Jmax}限制，初始 T_J = 25°C、L = 0.05mH、R_G = 25Ω、I_{AS} = 110A、V_{GS}=10V。不建议在高于此值的情况运行器件。

③ I_{SD} ≤ 110A, di/dt ≤ 1330A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

④ 脉冲宽度≤ 400μs；占空比≤ 2%。

⑤ C_{oss} eff. (TR)是一个固定电容值， 当 V_{DS} 从 0 上升至 80% V_{DSS}时，其充电时间与 C_{oss} 相同。

⑥ C_{oss} eff. (ER) 是一个固定电容值， 当 V_{DS} 从 0 上升至 80% V_{DSS}时，其产生与 C_{oss} 相同的热量 。

⑦ R_θ 在 T_J 约为 90°C 时测得 。

⑧ 安装在 1 英寸见方PCB （FR-4 或 G-10 材料）上时。有关建议的封装和焊接技术，请参阅应用注释 #AN-994。

⑨ $R_{\theta JC}$值标定于器件初始时刻

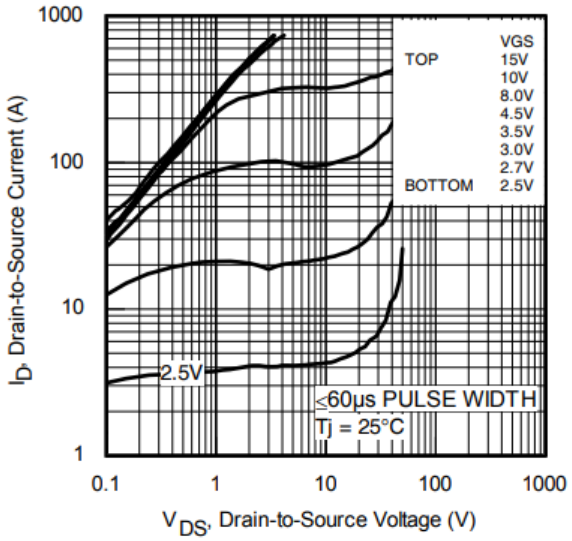


Fig 1. Typical Output Characteristics

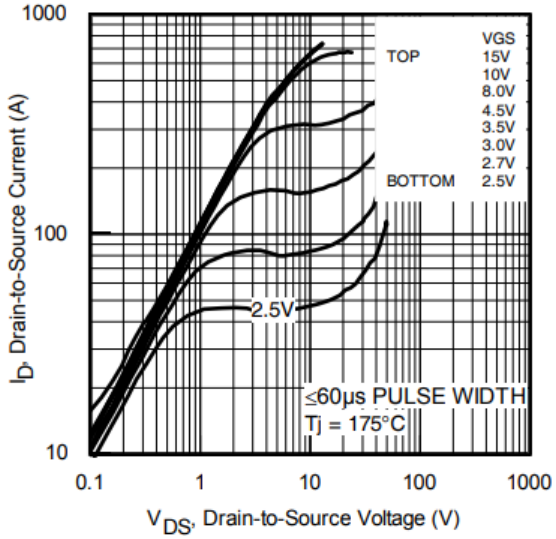


Fig 2. Typical Output Characteristics

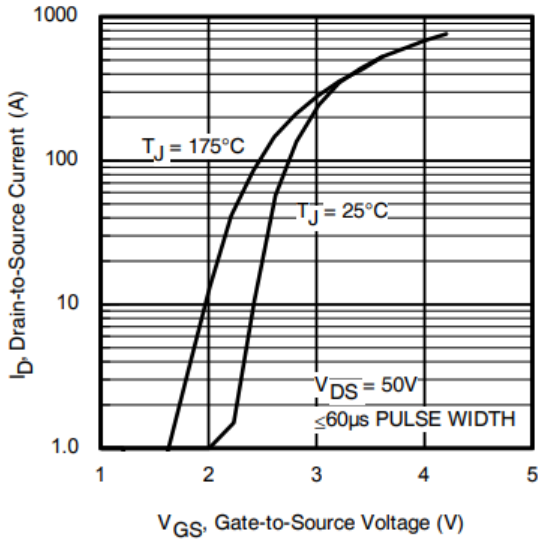


Fig 3. Typical Transfer Characteristics

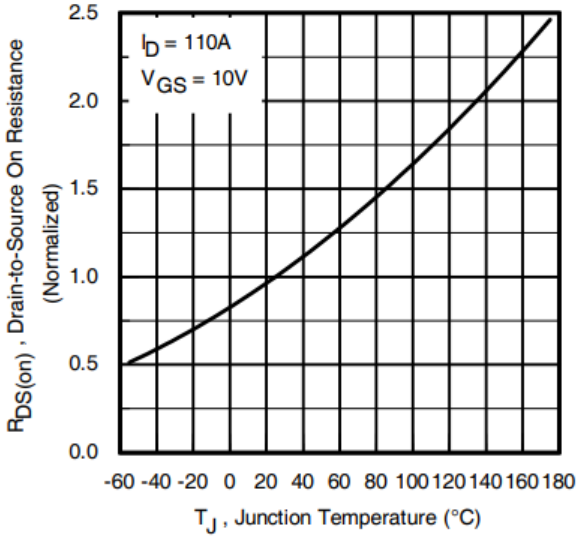


Fig 4. Normalized On-Resistance vs. Temperature

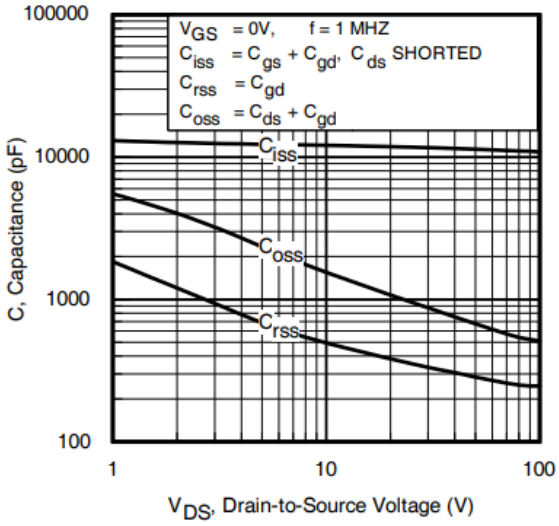


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

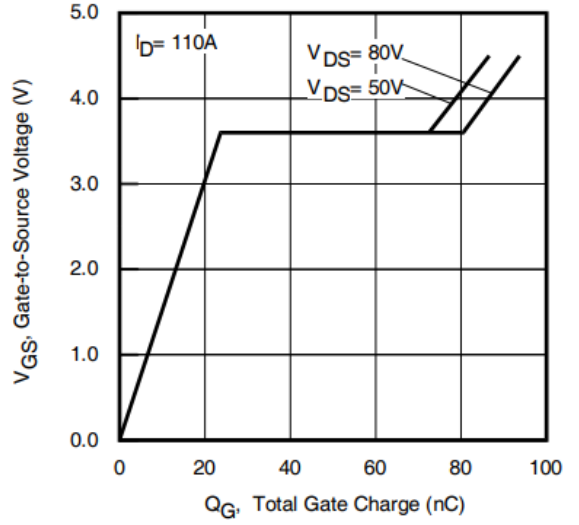


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

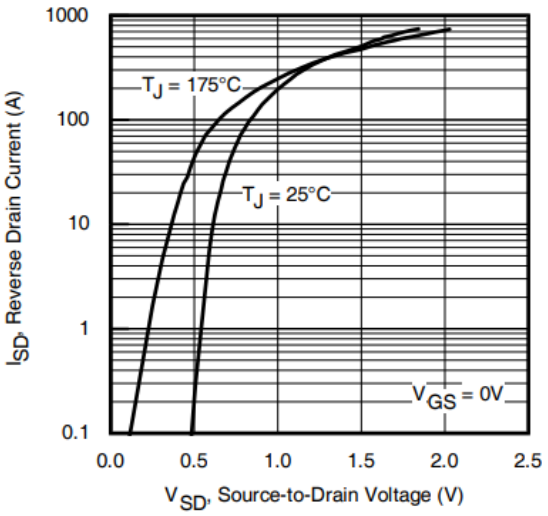


Fig 7. Typical Source-Drain Diode Forward Voltage

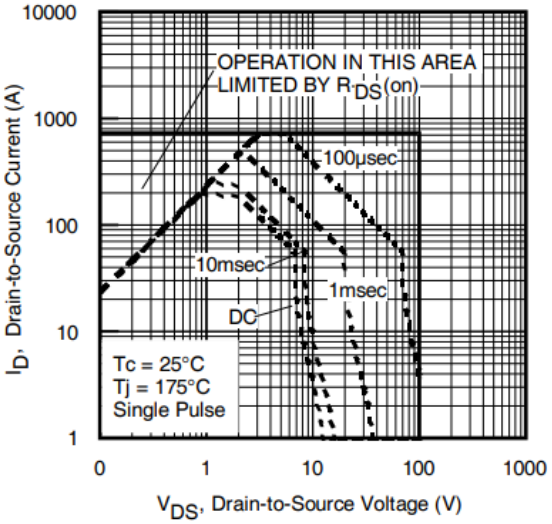


Fig 8. Maximum Safe Operating Area

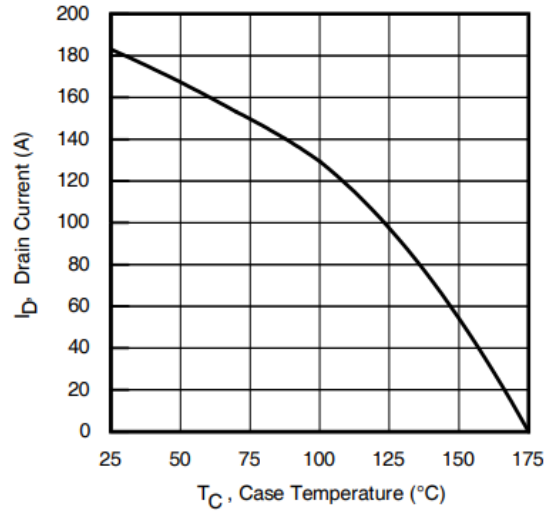


Fig 9. Maximum Drain Current vs. Case Temperature

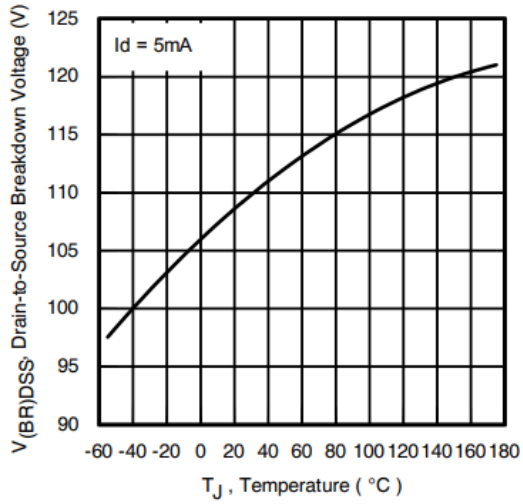


Fig 10. Drain-to-Source Breakdown Voltage

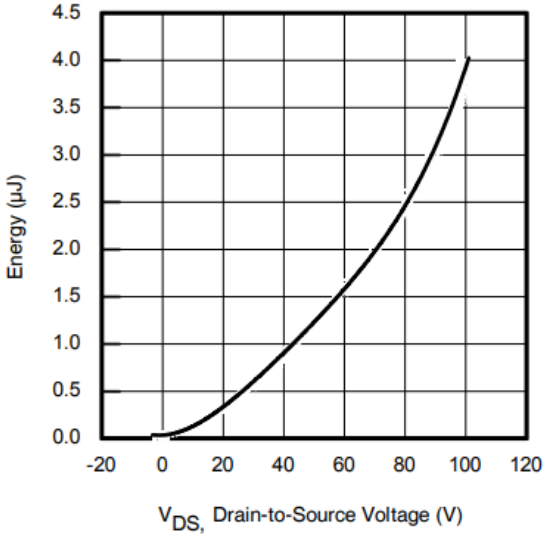


Fig 11. Typical C_{oss} Stored Energy

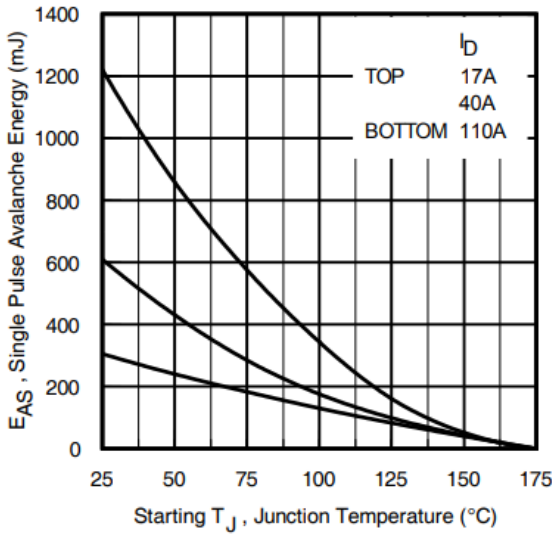
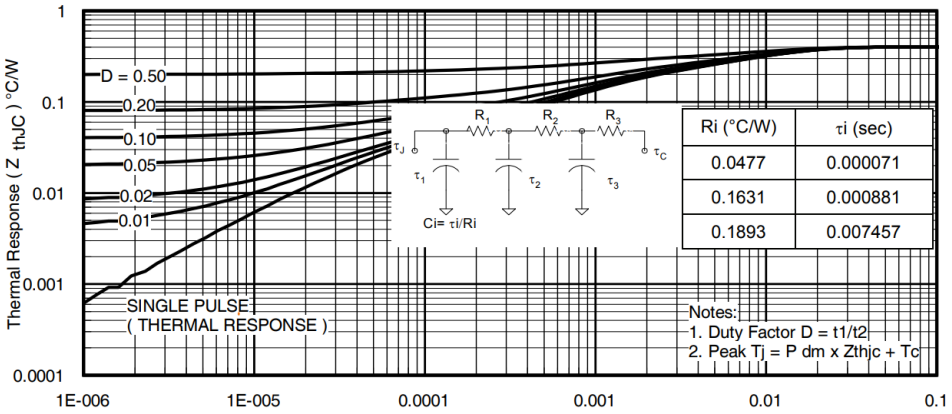
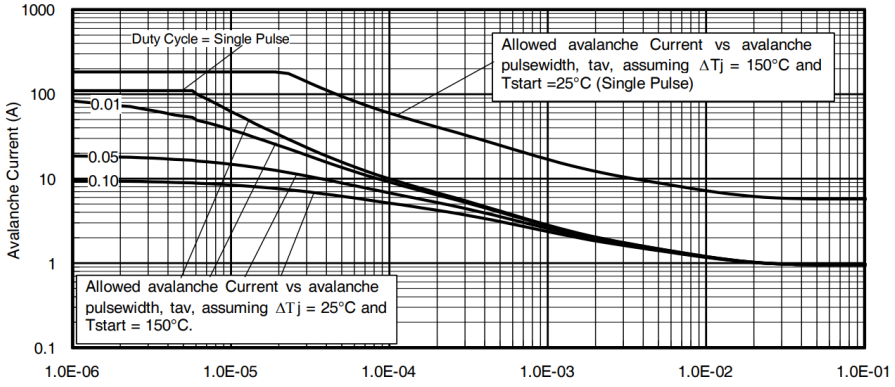


Fig 12. Maximum Avalanche Energy vs. Drain Current



t1，矩形脉冲持续时间（秒）

图 13.最大有效瞬态热阻，结到壳



tav（秒）

图 14.典型雪崩电流与脉冲宽度

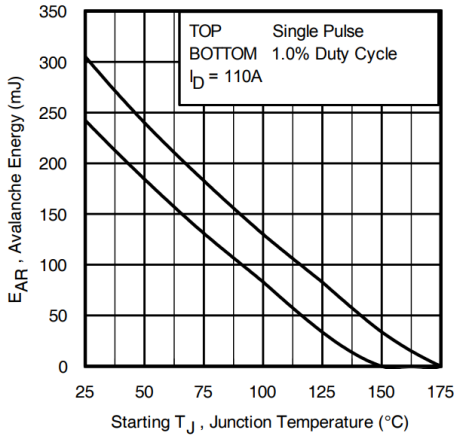


图 15.最大雪崩能量与温度的关系曲线

关于重复的雪崩曲线的注释，图 14、15：（有关详细信息，请参阅www.irf.com 上的 AN-1005）

1.雪崩失效假设：

纯粹的热现象和失效发生在结温远超 T_{jmax}的情况下。这对每种零件类型都是有效的。

2. 只要不超过 T_{jmax}，就可以在雪崩中安全运行。

3. 如下公式基于图 22a、22b 所示的电路和波形。

4. $P_{D\,(ave)}$ = 每个雪崩脉冲的平均功率耗散。

5. BV = 额定击穿电压（1.3 倍系数，考虑雪崩期间的电压增加）。

6. I_{av} = 可允许的雪崩电流。

7. Δ T = 可允许的结温上升，不得超过 T_{jmax} （图 14、15 中假设为 25°C）。

t_{av} = 雪崩的平均时间。

D = 雪崩占空比 = tav ·f

$Z_{thJC}(D, t_{av})$ = 瞬态热阻抗，见图 14) $PD\,(ave) = 1/2\,(1.3 \cdot BV \cdot I_{av})$

$= \Delta T / Z_{thJC}$

$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$

$E_{AS\,(AR)} = P_{D\,(ave)} \cdot t_{av}$

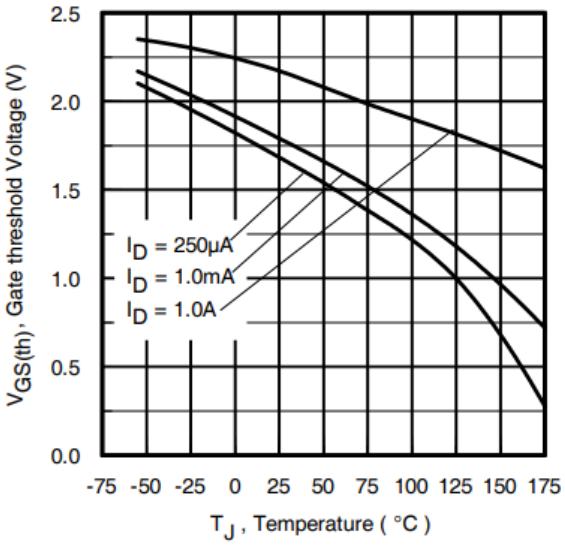


Fig 16. Threshold Voltage vs. Temperature

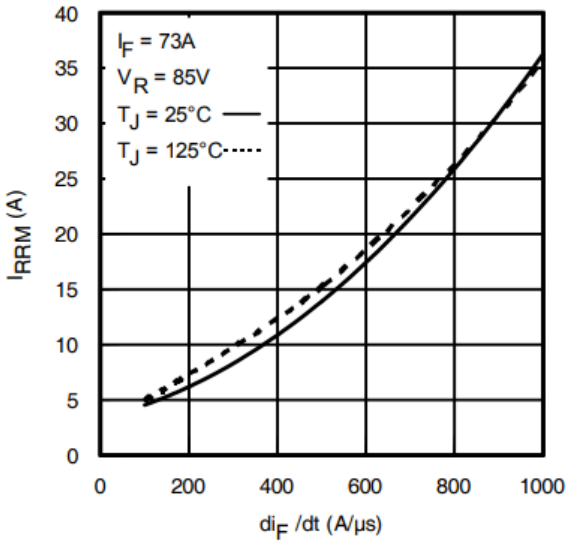


Fig 17. Typical Recovery Current vs. dif/dt

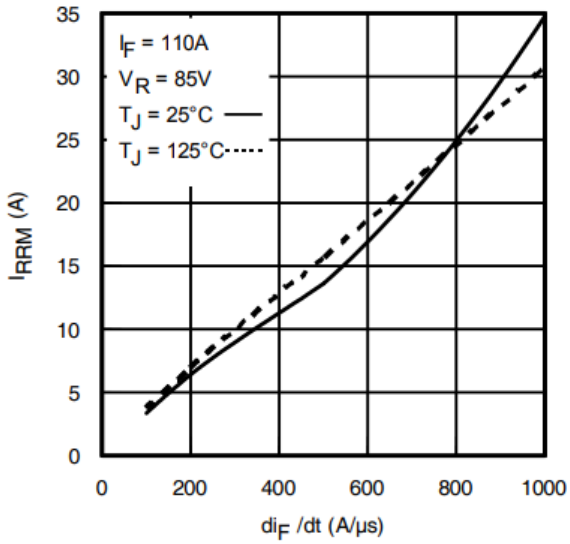


Fig 18. Typical Recovery Current vs. dif/dt

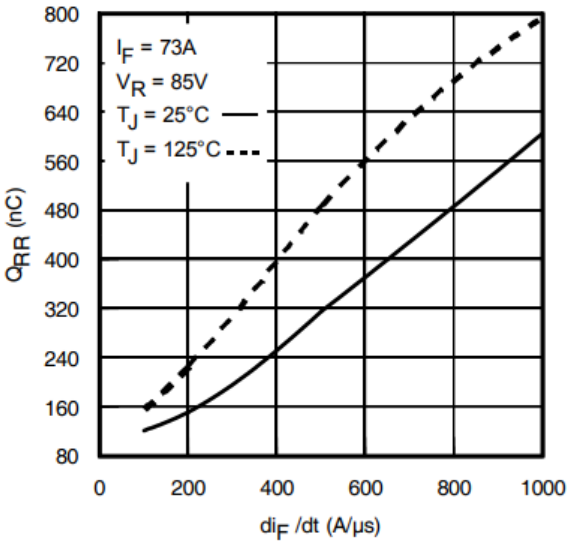


Fig 19. Typical Stored Charge vs. dif/dt

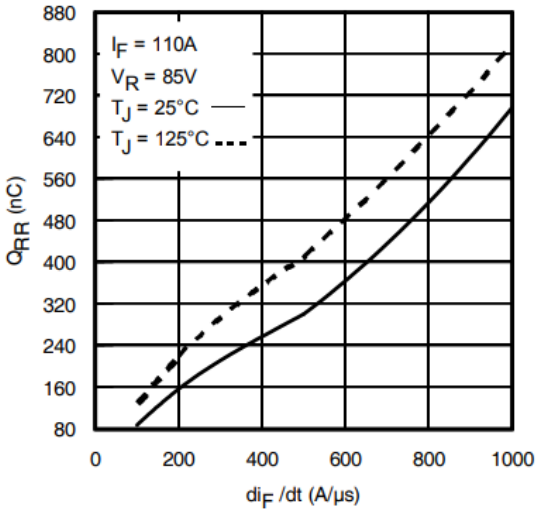


Fig 20. Typical Stored Charge vs. dif/dt

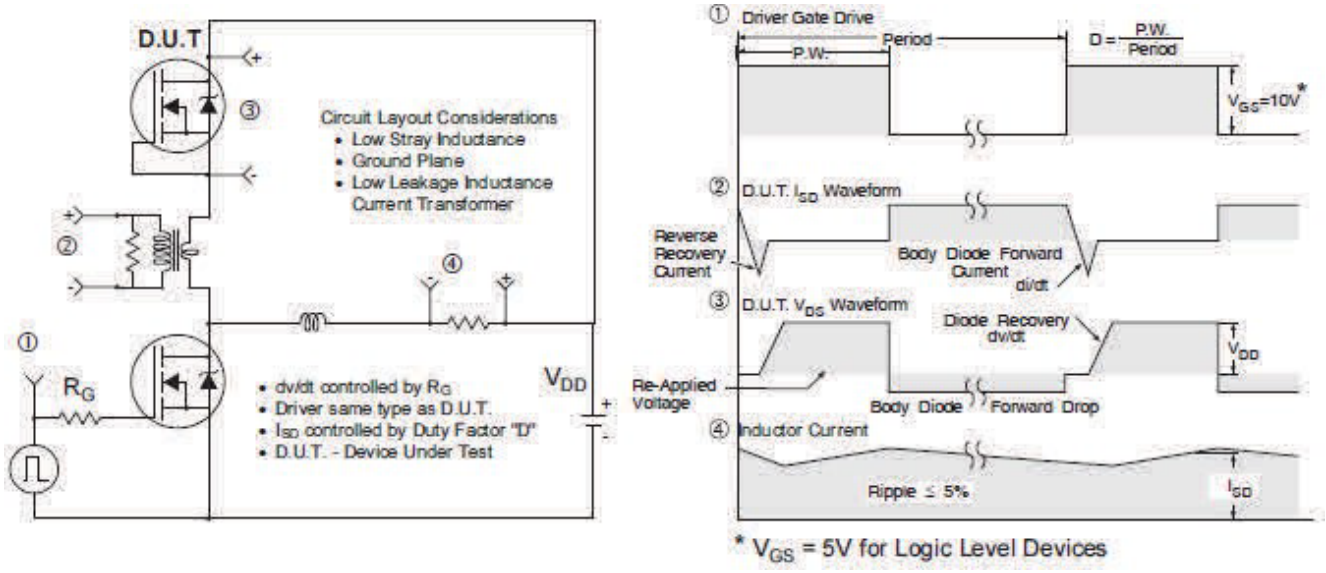


图 21. N 沟道 HEXFET® 功率 MOSFET 体内二极管峰值恢复 dv/dt 测试电路

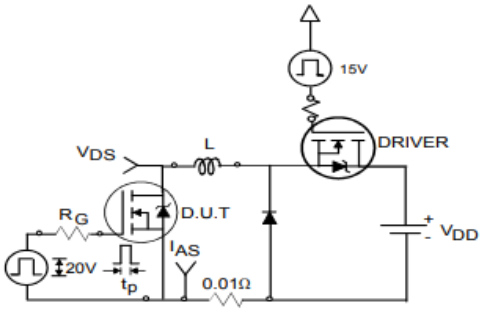


Fig 22a. Unclamped Inductive Test Circuit

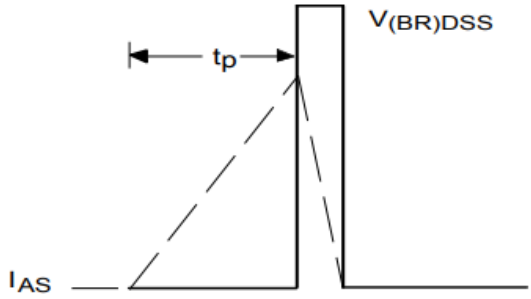


Fig 22b. Unclamped Inductive Waveforms

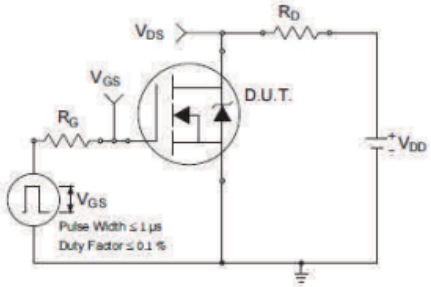


Fig 23a. Switching Time Test Circuit

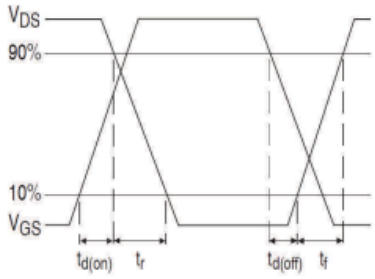


Fig 23b. Switching Time Waveforms

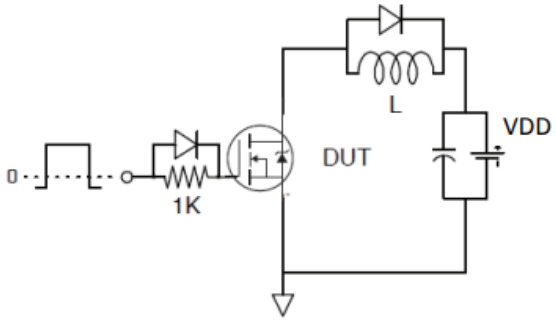


Fig 24a. Gate Charge Test Circuit

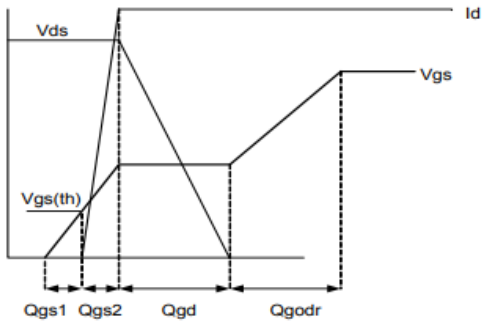
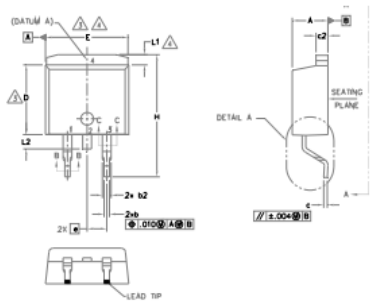


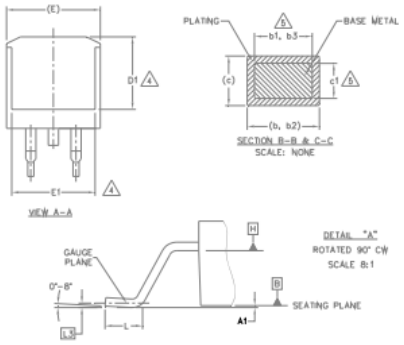
Fig 24b. Gate Charge Waveform

D ² Pak（TO-263AB） 封装外形（尺寸以毫米（英寸）为单位）



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270	–	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245	–	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.68	–	.066	4
L2	–	1.78	–	.070	
L3	0.25 BSC		.010 BSC		

LEAD ASSIGNMENTS

DIODES

1.– ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.– CATHODE
3.– ANODE

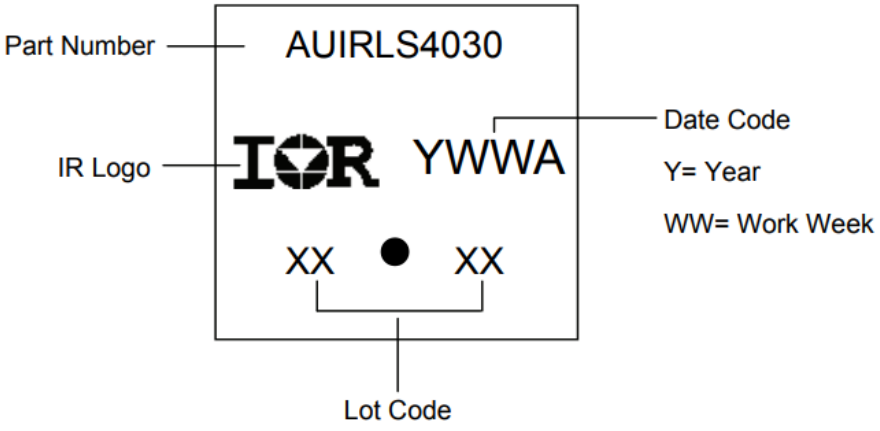
HEXFET

1.– GATE
2, 4.– DRAIN
3.– SOURCE

IGBTs, CoPACK

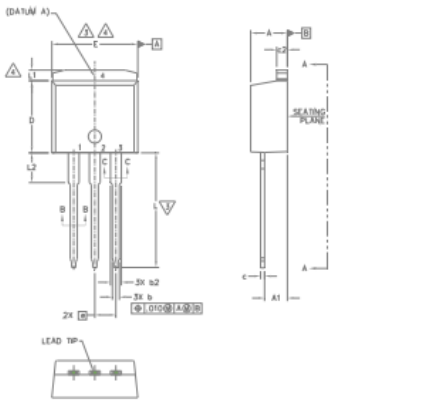
1.– GATE
2, 4.– COLLECTOR
3.– EMITTER

D ² Pak（TO-263AB）零件信息标识



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

TO-262 封装外形（尺寸以毫米（英寸）为单位）



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. – OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

IGBTs, CoPACK

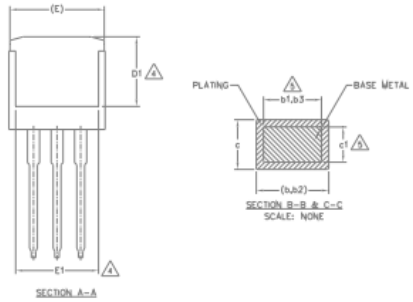
1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

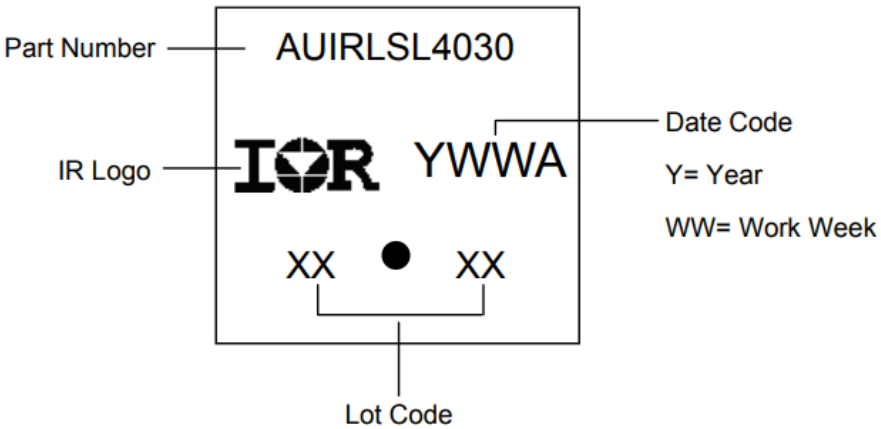
DIODES

1.– ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.– CATHODE
3.– ANODE



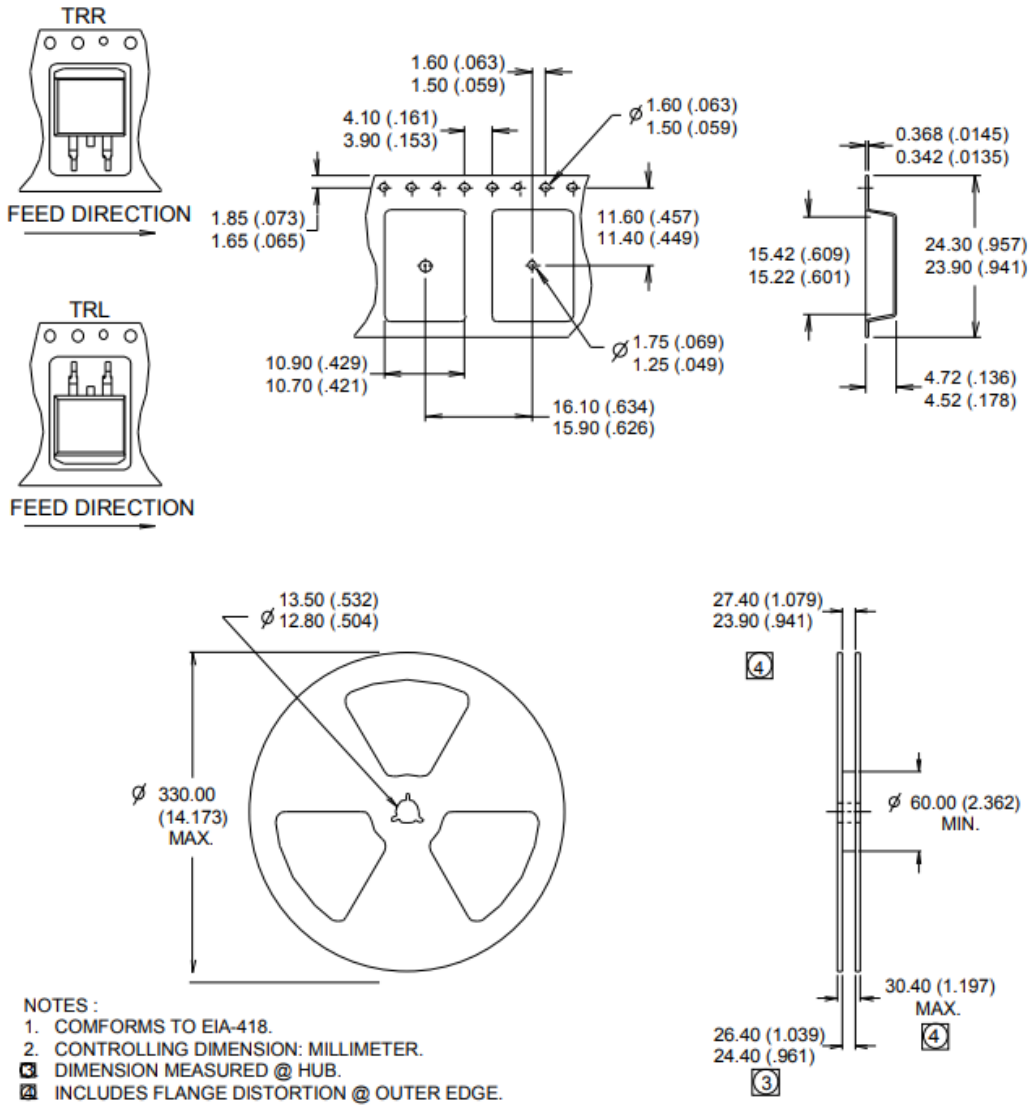
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270	–	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	–	1.65	–	.065	4
L2	3.56	3.71	.140	.146	

TO-262 零件标识信息



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

D ² Pak（TO-263AB）卷、带信息（尺寸以毫米（英寸）为单位）



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D^2-Pak	MSL1
		TO-262	
ESD	Machine Model	Class M4(+/- 800V)† (per AEC-Q101-002)	
	Human Body Model	Class H3A (+/- 6000V)† AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V)† AEC-Q101-005	
RoHS Compliant		Yes	

† 最高通过电压。

修订记录

Date	Comments
3/3/2014	• Added "Logic Level Gate Drive" bullet in the features section on page 1 • Updated data sheet with new IR corporate template
4/9/2014	• Updated package outline and part marking on page 8 & 9. • Updated Qualification table -TO262 Pak from "N/A" to "MSL1" on page 11. • Updated typo on the fig.19 and fig.20, unit of y-axis from "A" to "nC" on page 6.
11/6/2015	• Updated datasheet with corporate template • Corrected ordering table on page 1.

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