TLF4D985 evaluation board

User guide

About this document

Scope and purpose

This document explains how to use the OPTIREG™ TLF4D985 evaluation board V1.1. You should also refer to the corresponding datasheet of the PMIC.

Intended audience

This document is intended for engineers who develop applications and want to evaluate the functions of the PMIC via the evaluation board.

Attention: ***TLF4D985QKV0xR1 in design step A31 is mounted on the Evaluation Board V1.1. TLF4D985QKV0x in design step A11 is mounted on the Evaluation Board V1.0.***

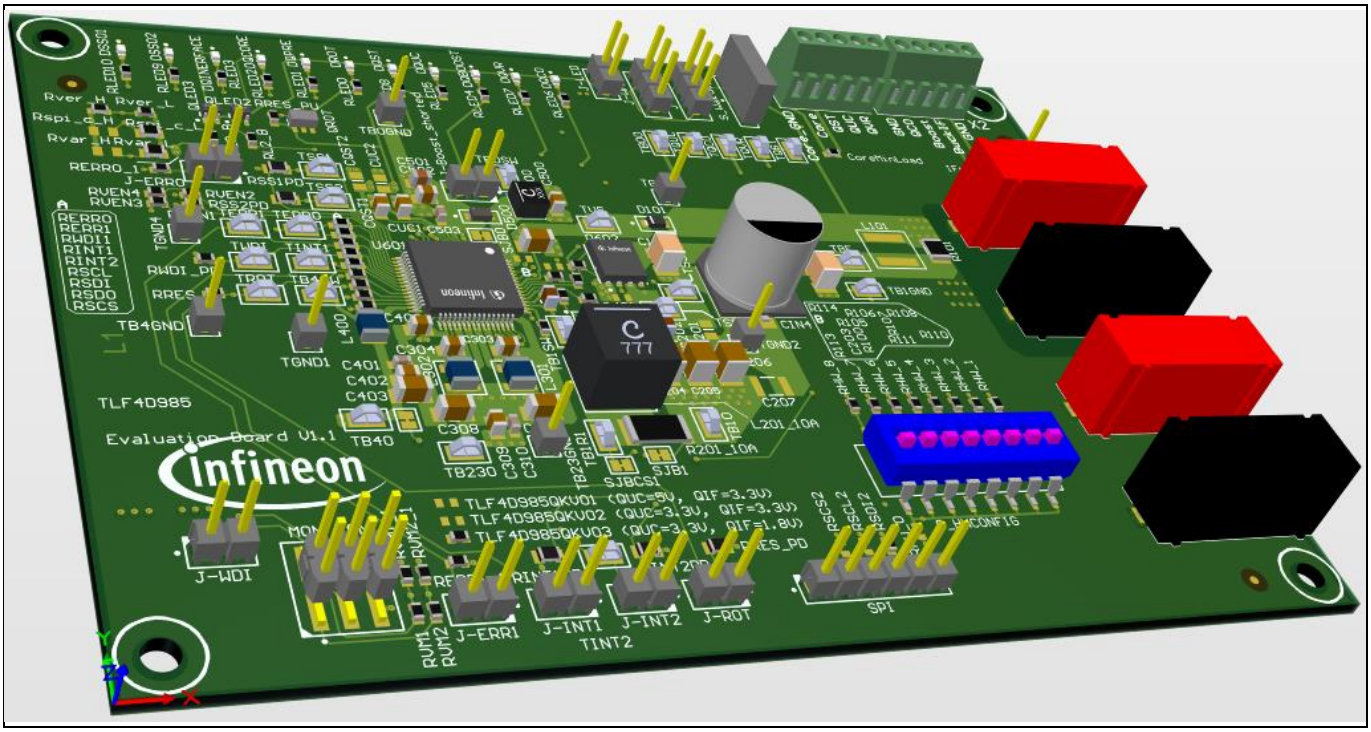


Figure 1 TLF4D985 evaluation board

Important notice

“Evaluation Boards and Reference Boards” shall mean products embedded on a printed circuit board (PCB) for demonstration and/or evaluation purposes, which include, without limitation, demonstration, reference and evaluation boards, kits and design (collectively referred to as “Reference Board”).

Environmental conditions have been considered in the design of the Evaluation Boards and Reference Boards provided by Infineon Technologies. The design of the Evaluation Boards and Reference Boards has been tested by Infineon Technologies only as described in this document. The design is not qualified in terms of safety requirements, manufacturing and operation over the entire operating temperature range or lifetime.

The Evaluation Boards and Reference Boards provided by Infineon Technologies are subject to functional testing only under typical load conditions. Evaluation Boards and Reference Boards are not subject to the same procedures as regular products regarding returned material analysis (RMA), process change notification (PCN) and product discontinuation (PD).

Evaluation Boards and Reference Boards are not commercialized products, and are solely intended for evaluation and testing purposes. In particular, they shall not be used for reliability testing or production. The Evaluation Boards and Reference Boards may therefore not comply with CE or similar standards (including but not limited to the EMC Directive 2004/EC/108 and the EMC Act) and may not fulfill other requirements of the country in which they are operated by the customer. The customer shall ensure that all Evaluation Boards and Reference Boards will be handled in a way which is compliant with the relevant requirements and standards of the country in which they are operated.

The Evaluation Boards and Reference Boards as well as the information provided in this document are addressed only to qualified and skilled technical staff, for laboratory usage, and shall be used and managed according to the terms and conditions set forth in this document and in other related documentation supplied with the respective Evaluation Board or Reference Board.

It is the responsibility of the customer’s technical departments to evaluate the suitability of the Evaluation Boards and Reference Boards for the intended application, and to evaluate the completeness and correctness of the information provided in this document with respect to such application.

The customer is obliged to ensure that the use of the Evaluation Boards and Reference Boards does not cause any harm to persons or third party property.
The Evaluation Boards and Reference Boards and any information in this document is provided "as is" and Infineon Technologies disclaims any warranties, express or implied, including but not limited to warranties of non-infringement of third party rights and implied warranties of fitness for any purpose, or for merchantability.

Infineon Technologies shall not be responsible for any damages resulting from the use of the Evaluation Boards and Reference Boards and/or from any information provided in this document. The customer is obliged to defend, indemnify and hold Infineon Technologies harmless from and against any claims or damages arising out of or resulting from any use thereof.

Infineon Technologies reserves the right to modify this document and/or any information provided herein at any time without further notice.

Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*

Table of contents

1 Board overview

Figure 2 gives a first overview of the most important interfaces.

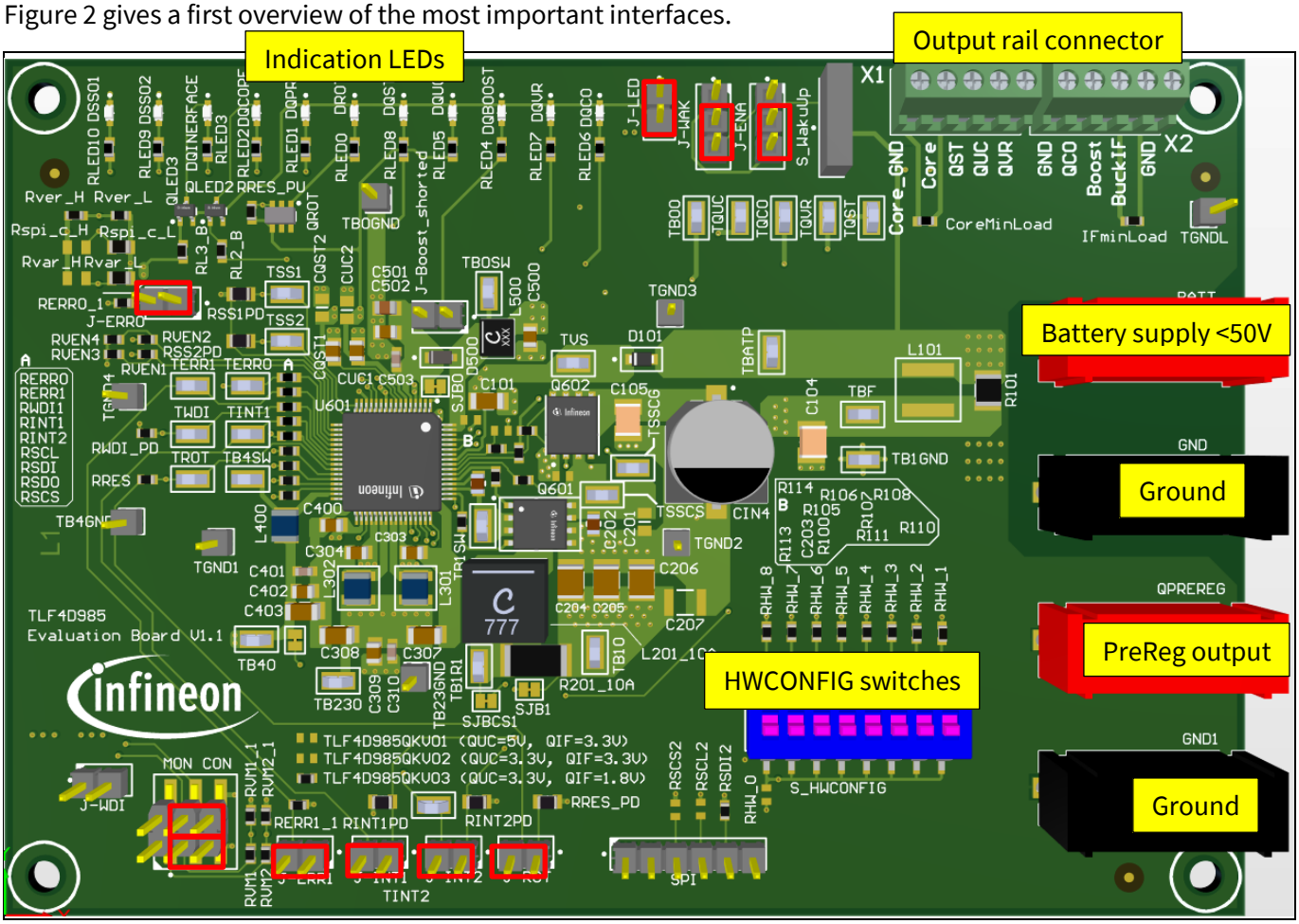


Figure 2 Main interfaces of the evaluation board, with the default jumper configuration

On the bottom side of the evaluation board is an Arduino Due interface. For use with the GUI, the evaluation board has to be mounted on top of an Aurix™ Shield Buddy TC375.

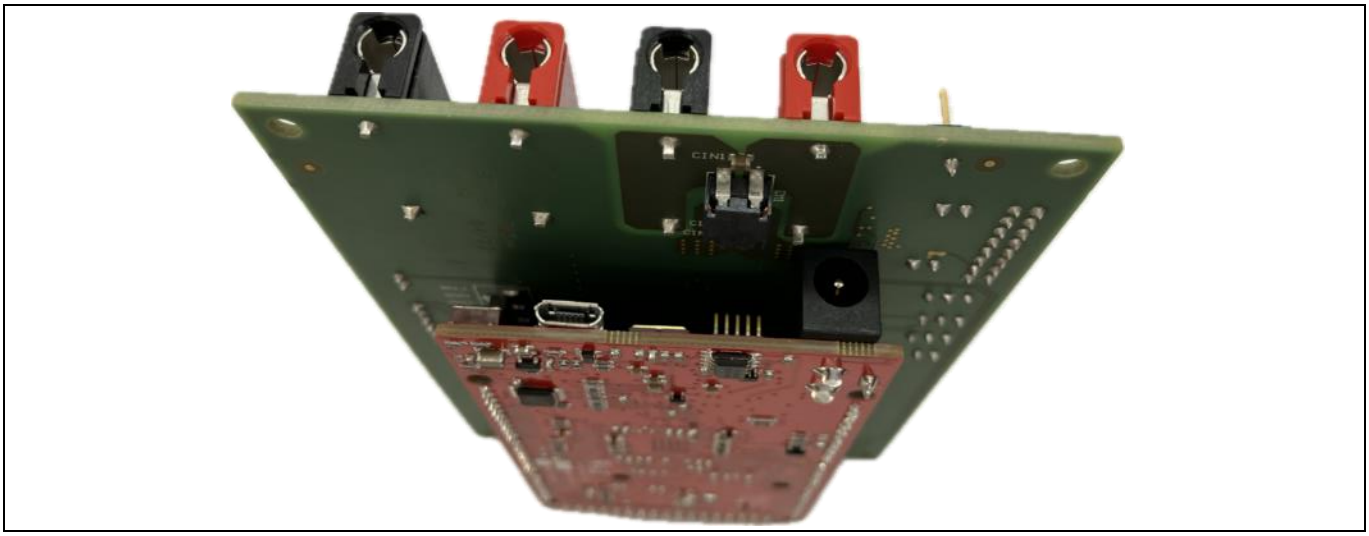


Figure 3 Evaluation board mounted on top of the AURIX™ Shield Buddy

1.1 Absolut maximum ratings

Table 2 Absolut maximum ratings

Parameter	Symbol	Values		Unit	Note
		Min	Max		
Board supply voltage	BATT	0	50	V	Because of used capacitors
PreReg output voltage	QPREREG	-0.3	7	V	
All Voltages on output rail connector to GND	LOAD CON	-0.3	7	V	

1.2 Jumper description

Table 2 describes the jumper settings of the evaluation board. Make sure the jumpers are set according to the environment before power up.

Table 3 Jumper description

Jumper	Setup (default in bold)	Description
J-ENA	1-2	Connects the TLF4D985 ENA DI Pin to the switch S-WakuUp
	2-3	Connects the TLF4D985 ENA DI Pin to an Aurix™ µC DO to trigger it via the GUI; If this configuration is selected, make sure jumper J-WAK is configured as 2-3 to prevent the simultaneous triggering of both, WAK and ENA.
J-WAK	1-2	Connects the TLF4D985 WAK DI Pin to an Aurix™ µC DO to trigger it via the GUI; If this configuration is selected, make sure jumper J-WAK is configured as 2-3 to prevent the simultaneous triggering of both, WAK and ENA.
	2-3	Connects the TLF4D985 WAK DI Pin to the switch S-WakuUp
J-LED	**Closed**	Activates all LEDs
J-WDI	**Closed**	Connects Aurix™ µC DO to TLF4D985 WD DI Pin
J-ERR0	**Closed**	Connects Aurix™ µC DO to TLF4D985 ERR0 DI Pin
J-ERR1	**Closed**	Connects Aurix™ µC DO to TLF4D985 ERR1 DI Pin
J-INT1	**Closed**	Connects Aurix™ µC DI to TLF4D985 INT1 DO Pin
J-INT2	**Closed**	Connects Aurix™ µC DI to TLF4D985 INT2 DO Pin
J-ROT	**Closed**	Connects Aurix™ µC DI to TLF4D985 ROT DO Pin
J-Boost_shorted	**Open**	Boost converter supplies the post LDOs
	Closed	Boost converter is shorted. Pre-regulator supplies the post LDOs
GD	**Open**	If closed, it connects the supply of Gate Drivers GD1 and GD2 to QPRE
J-L1	**Open**	Load for load jumps on QPRE, QCORE, QINTERFACE, QBOOST can be applied externally via these pins (in parallel to RL1)
J-L2	**Open**	Load for load jumps on QUC, QCO, QVR, QST can be applied externally via these pins (in parallel to RL2)
LOAD CON	-	Set jumpers to select which output rails should be loaded via MOSFETs. See schematic for pinout.
MON CON	-	Interface for the external voltage monitoring. See schematic for pinout.

<table>
<tr>
<td>S_HWCONFIG</td>
<td></td>
<td>Selects the HWCONFIG resistor and with this the status of MPS (MicroController Programming Support), PreReg voltage, Startup schema, Reset delay)
<table>
<tr><th>Switch in ON position</th><th>Resistor value</th><th>PreReg voltage / RESOUT delay / MPS mode / Startup schema</th></tr>
<tr><td>1</td><td>2k2</td><td>4.0V / 2ms / MPS=OFF /schA</td></tr>
<tr><td>2</td><td>3k3</td><td>4.0V / 2ms / MPS=OFF /schB</td></tr>
<tr><td>3</td><td>6k8</td><td>5.5V / 2ms / MPS=OFF /schA</td></tr>
<tr><td>4</td><td>15k</td><td>5.5V / 2ms / MPS=OFF /schB</td></tr>
<tr><td>5</td><td>22k</td><td>5.5V / 2ms / MPS=ON /schB</td></tr>
<tr><td>6</td><td>33k</td><td>5.5V / 2ms / MPS=ON /schA</td></tr>
<tr><td>7</td><td>68k</td><td>4.0V / 2ms / MPS=ON /schB</td></tr>
<tr><td>8</td><td>100</td><td>4.0V / 2ms / MPS=ON /schA</td></tr>
<tr><td>none</td><td>open</td><td>4.0V / 10ms / MPS=OFF /schA</td></tr>
</table>
</td>
</tr>
</table>

2 Getting started

This chapter focuses on the usage of the evaluation board in combination with Aurix™ Shield Buddy TC375 for configuring the DUT via the PC.

The evaluation board can also be used stand alone with the standard configuration. In this case, the MPS (MicroController Programming Support) has to be enabled via the HWCONFIG switches, in order to deactivate the µC supervision.

2.1 Evaluation environment overview

For using the OneEye GUI, the Aurix™ Shield Buddy TC375 needs to be used. For board ordering information, see Table 4.

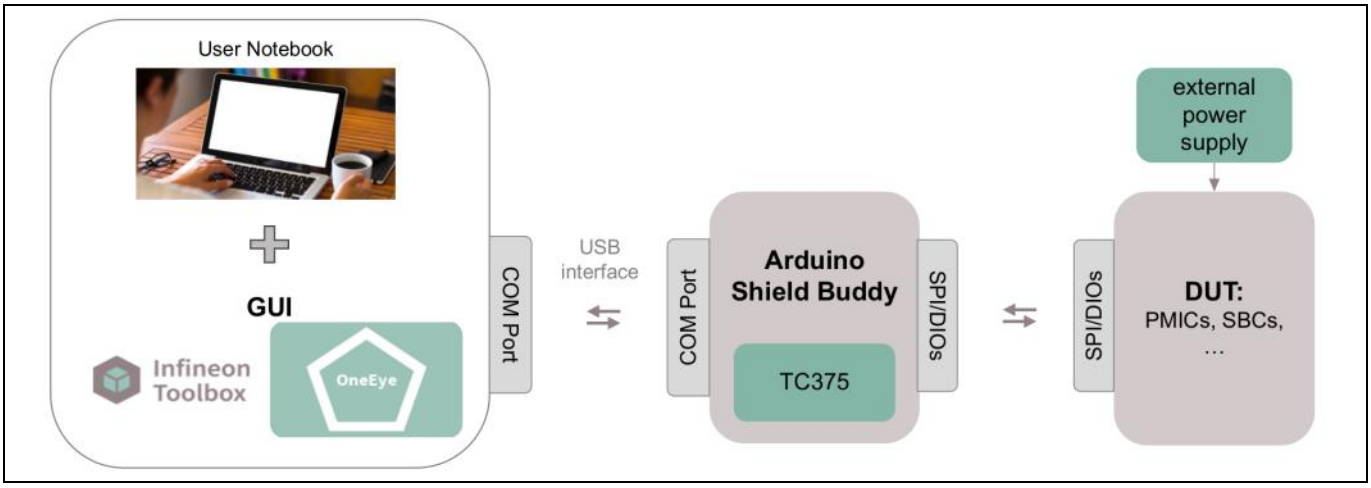


Figure 4 OneEye GUI communication concept

Table 4 Required hard- and software

Hardware	**Ordering information**
TLF4D985QKV01 BOARD or TLF4D985QKV02 BOARD or TLF4D985QKV03 BOARD	SP006004818 Or SP006004820 Or SP006004823
Aurix™ Shield Buddy TC375	SP005432164
Micro USB cable	
Software	
Device Access Server (DAS)	
OPTIREG™ TLF4D985 evaluation suite 1.1	
OneEye 2.72 or newer (getting installed with OPTIREG™ TLF4D985 evaluation suite)	

2.2 Initial steps

The following steps have to be executed at the very first time:

1. Downloading and installing OPTIREG™ TLF4D985 evaluation suite
2. Installing the Device Access Server (DAS)
3. Connect the Micro-USB cable from the Aurix™ Shield Buddy to your PC
4. Start the evaluation suite
5. Setup serial interface
6. Programm Aurix™ Shield Buddy
7. Disconnect the USB cable
8. Mount the TLF4D985 BOARD on top of the Aurix™ Shield Buddy (see Figure 3)

2.3 Steps at every startup

To correctly use the evaluation board and software you will need to:

1. Verify that the jumpers are mounted according to your needs, as shown in Table 3
2. Connect the Micro-USB cable from the Aurix™ Shield Buddy to your PC
3. Start the evaluation suite
4. Setup serial interface
5. Apply the specific OneEye configuration
6. Power the TLF4D985 BOARD via the banana plugs

Note: Especially when the PMIC is configured with disabled Microcontroller Programming Support (MPS), it is important to connect first the GUI to the Aurix™ Shield Buddy before powering the TLF4D985 BOARD. Otherwise it is not possible to configure microcontroller supervision functions of the PMIC within the initialization timeout. The PMIC will therefore move to FAILSAFE mode.

2.4 Step by step guide

2.4.1 Downloading and installing OPTIREG™ TLF4D985 evaluation suite

The *OPTIREG™ TLF4D985 evaluation suite* can be downloaded via the Infineon Developer Center for customers with an myInfineon account.

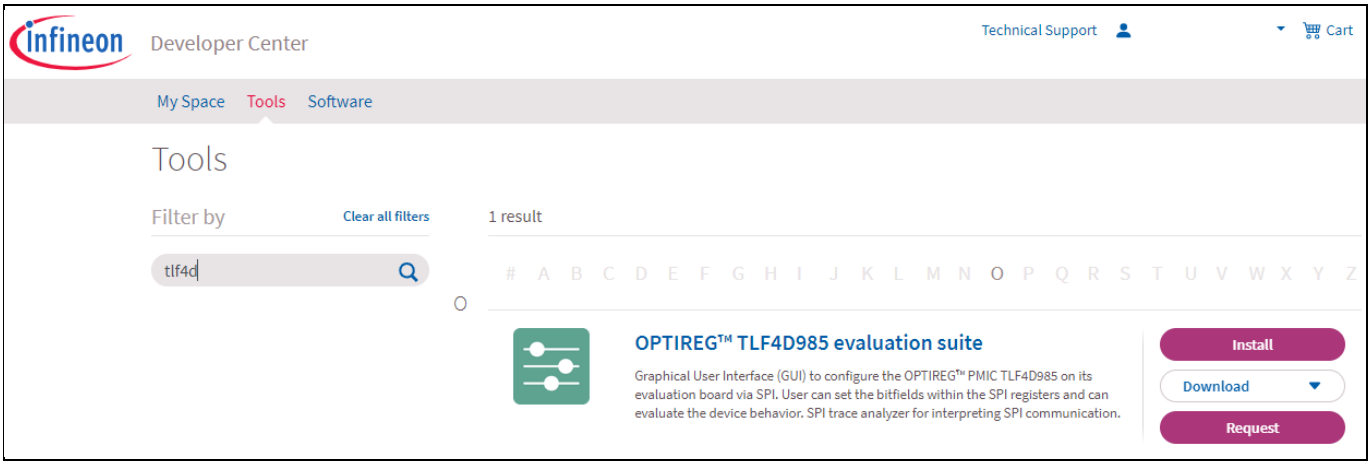


Figure 5 Downloading OPTIREG™ TLF4D985 evaluation suite via Infineon Developer Center

Please follow these steps to request a license:

1. Open Infineon Developer Center
2. Log in with your myInfineon account on the upper right side
3. Search for the *OPTIREG™ TLF4D985 evaluation suite* in the Tools section of the Developer Center

After downloading the executable, the installation wizard will guide you through the installation.

Note: The default installation directory is:
C:\Infineon\Tools\OPTIREG-TLF4D985-evaluation-suite\<version>

During the installation of the evaluation suite, the dependable program OneEye is installed as well.

2.4.2 Installing the Device Access Server (DAS)

Install the Device Access Server via the installer which is available here.

2.4.3 Start the evaluation suite

The evaluation suite can be started via windows start menu:
Infineon Developer Center -> OPTIREG™ TLF4D985 evaluation suite

Please select the tool “GUI for evaluation board” from the start screen by clicking on the icon.

Figure 6 Start screen of the evaluation suite

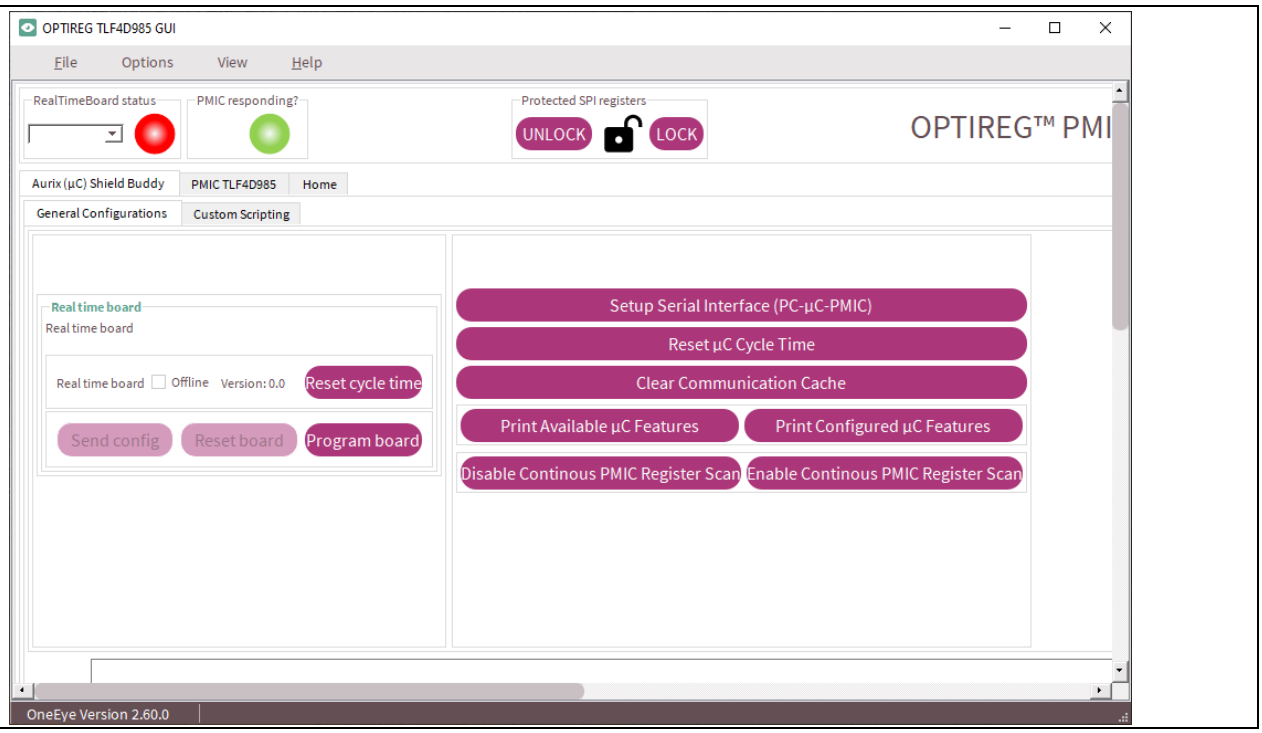


Figure 7 GUI after connecting to the unprogrammed real time board

The GUI is organized in rows and tabs, as follows:

1. Header with basic indicator items
    a. Status of the real time board connection (Aurix Shield Buddy)

b. Status of SPI communication to the PMIC

2. Tab selector
   a. "Aurix (µC) Shield Buddy"
      i. *General Configuration* for setting up the connection to the Shield-Buddy
      ii. Custom Scripting
   b. "PMIC TLF4D985" gives access via several sub-tabs to the PMIC
      i. Control: State machine and most important status flags
      ii. Basic config: Configuration items which are usually set once, specific to the application
      iii. Status: All status flags
      iv. Converters: Control and status of all voltage converters via several sub tabs
      v. Wakeup timer: Control of the wakeup timer
      vi. Watchdogs: Configuration of the watchdogs and how they should be served by the AURIX™ Shield buddy
      vii. ERR: Configuration of the error monitoring and how it should be served by the AURIX™ Shield buddy
      viii. RegisterTree: A tree view of all SPI registers
      ix. ReducedOperation / ABIST
   c. "Home" for navigation to other tools within that suite

2.4.4 Setup serial interface

Execute the following steps in OneEye to establish a connection after connecting the AURIX™ Shield Buddy via USB to your computer:

1. In the tab *Aurix (µC) Shield Buddy* → *General configurations*, click on *Setup Serial Interface (PC-µC-PMIC)*
2. In the new pop up window select the correct COM port, leave the baudrate at 256000, press the *connect* checkbox, and close this window.

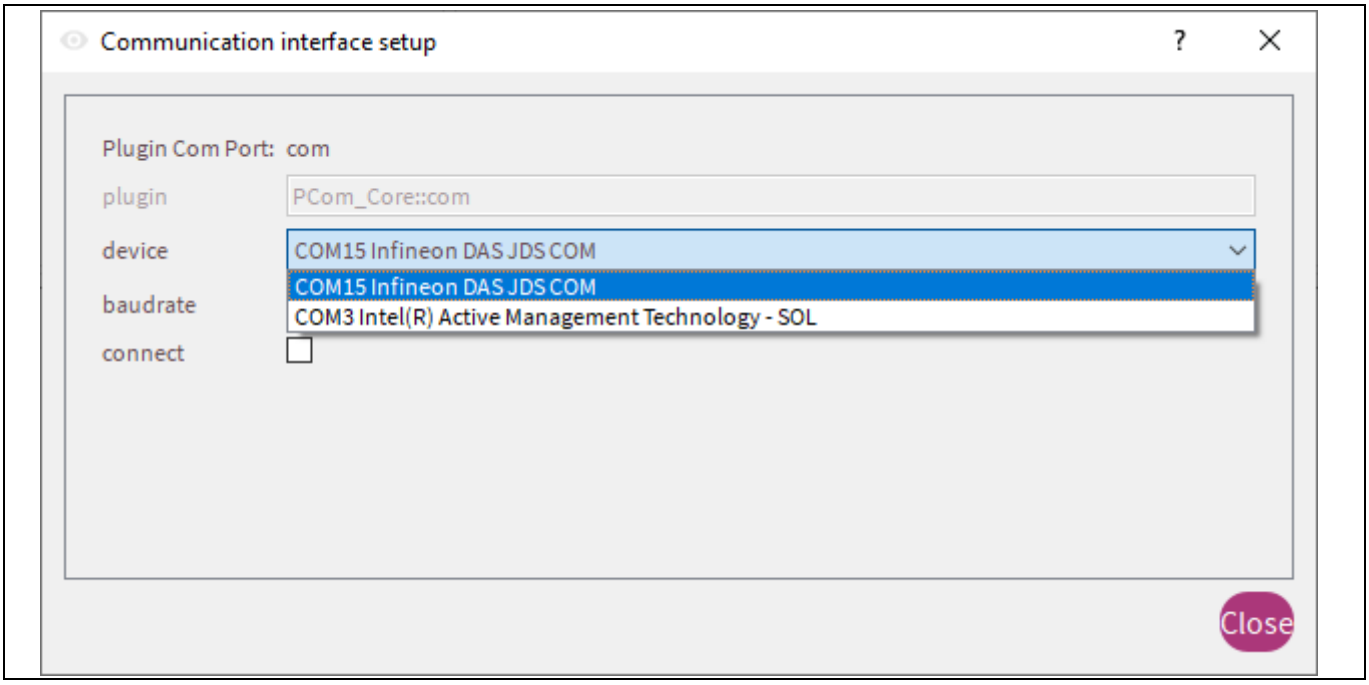


Figure 8 Communication interface setup

2.4.5 Programm Aurix™ Shield Buddy

As shown in Figure 4, in the evaluation environment the PC communicates with the DUT via the µC. To enable this communication channel, the µC needs to run the appropriate firmware.

1. Press the “Program board” button to start the programming
2. After some seconds the console window should show some text and header row shows the *RealTimeBoard status* as yellow = *Ready*. See Figure 9.
3. If not, check if the connection is setup correctly via the window shown in Figure 8.

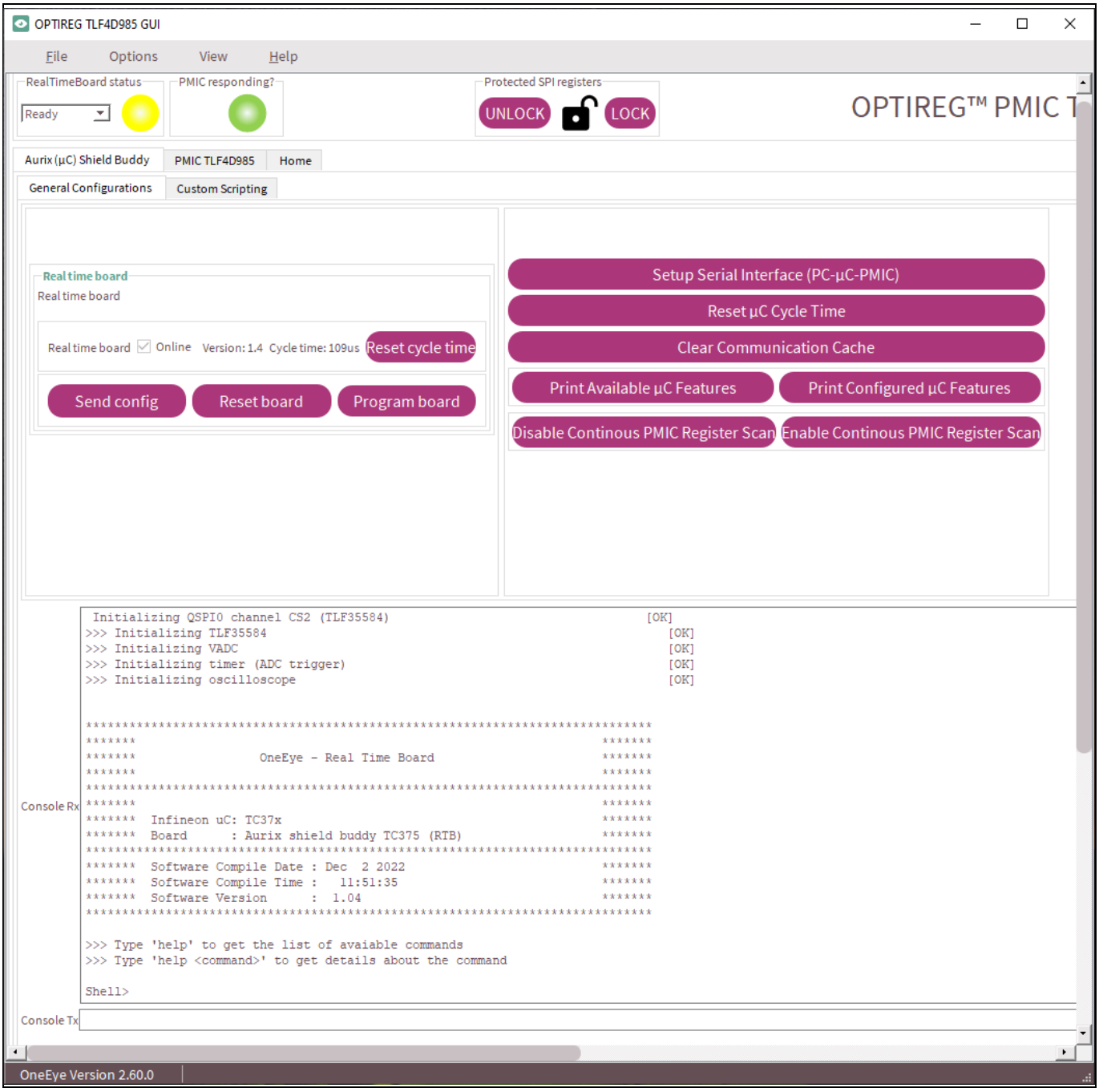


Figure 9 GUI after connecting to the real time board with firmware running

2.4.6 Apply the specific OneEye configuration

1. Click on *Send config* to send the PMIC specific configuration to the AURIX™ Shield Buddy. The status is reported in the Aurix Shell in the lower half of the tab.
   The *RealTimeBoard status* in the header row changes to green / *Configured*.

   Note: A project specific configuration can be sent only once to the µC within a reset cycle. If you want to rewrite the configuration, press Reset board *first and then press* Send config *again.*

   Note: For debugging reasons, you can open the Log box via View -> Log box or look into the Aurix Shell at lower half of the "General Configuration" tab.

2. After sending the configuration the GUI waits for the PMIC to start up. As soon as the RESOUT release is detected by the AURIX™ Shield Buddy, the watchdogs and error monitoring are automatically deactivated via SPI to allow the usage with deactivated microcontroller programming support (MPS).
3. Select the tab PMIC TLF4D985 to access the PMIC configuration.

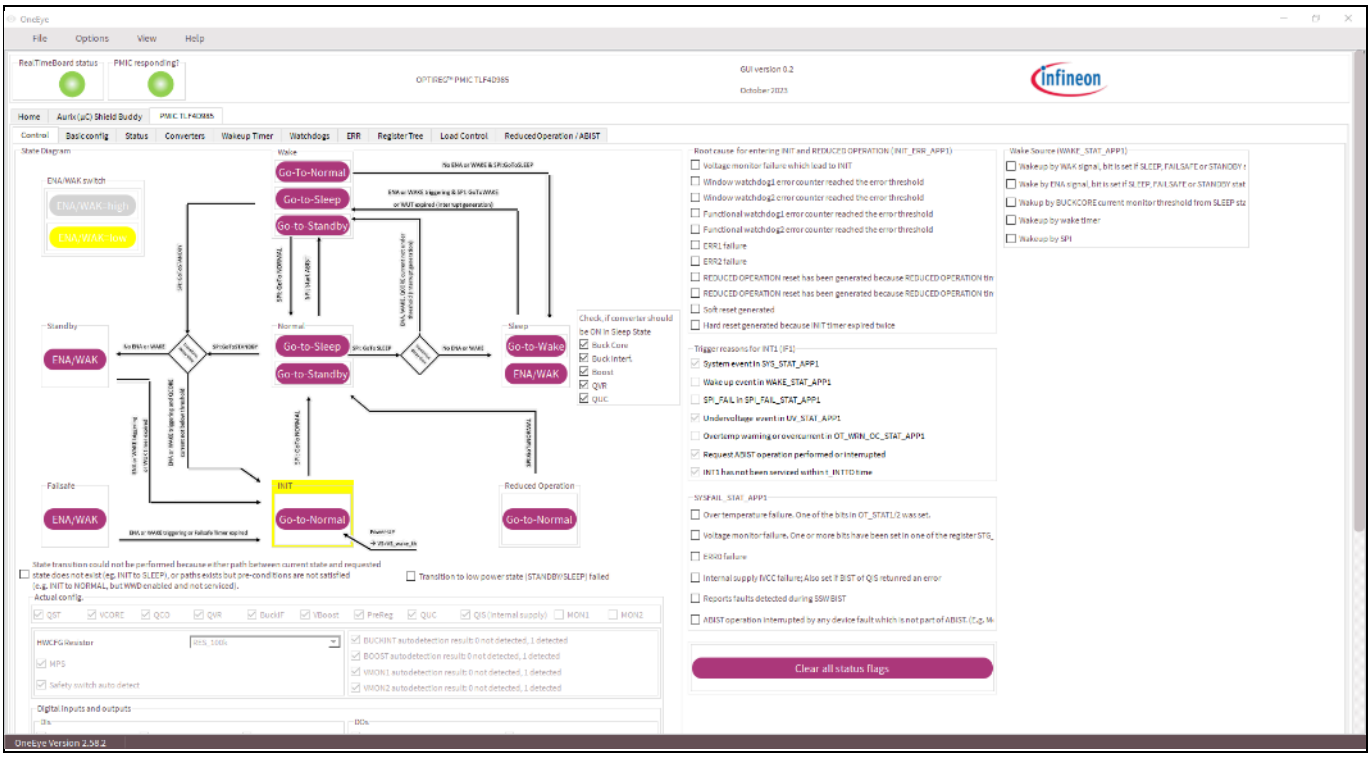


Figure 10 Tab "Control" after providing battery voltage to the TLF4D985 BOARD

3 Hints for using the GUI

3.1 Protected registers

Before a write command to a protected register is possible, an unlock command needs to be send via the unlock button in the header row.

With this, the controls of the GUI which are affected, gets activated and there can be changed by the user.

The changed value of the control / register gets applied with the lock command.

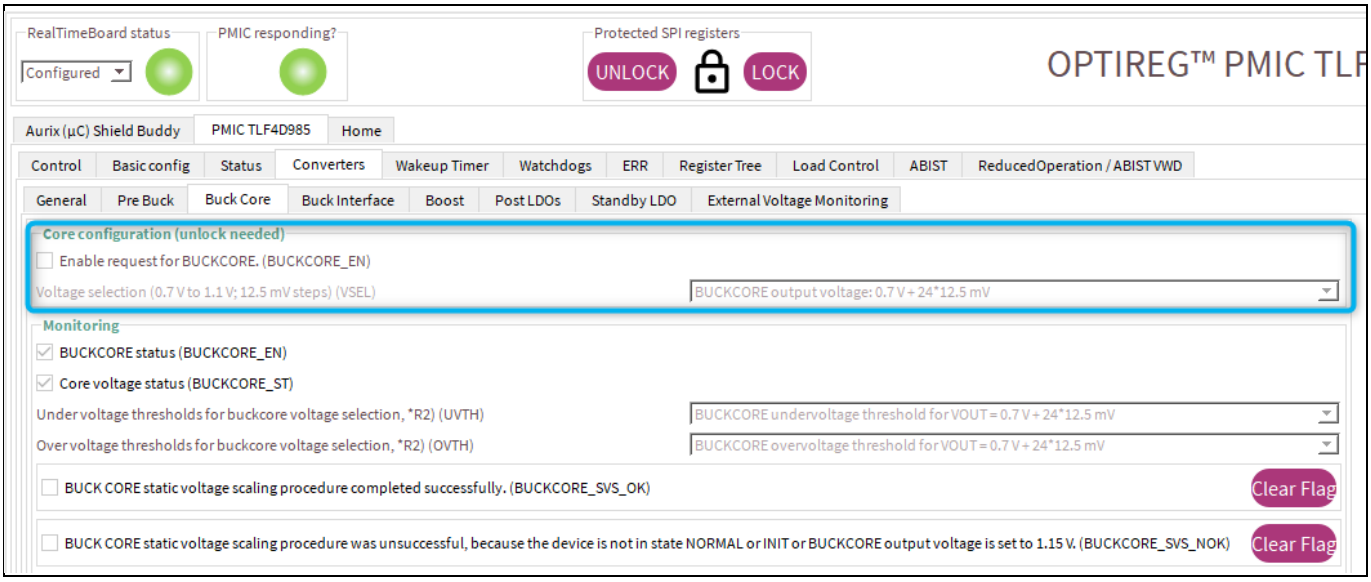


Figure 11 Bitfields of Protected Write registers are disabled (greyed out) if lock is active

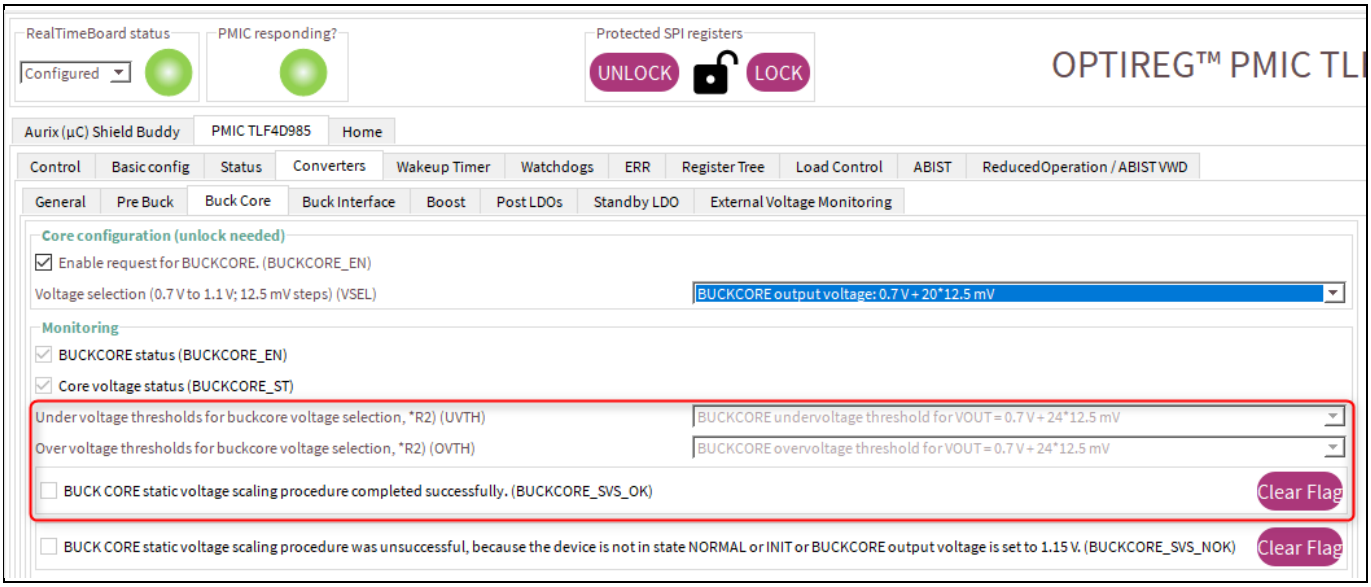


Figure 12 After unlocking bitfields can be written, but are not applied yet. Values in the red box are still unchanged.

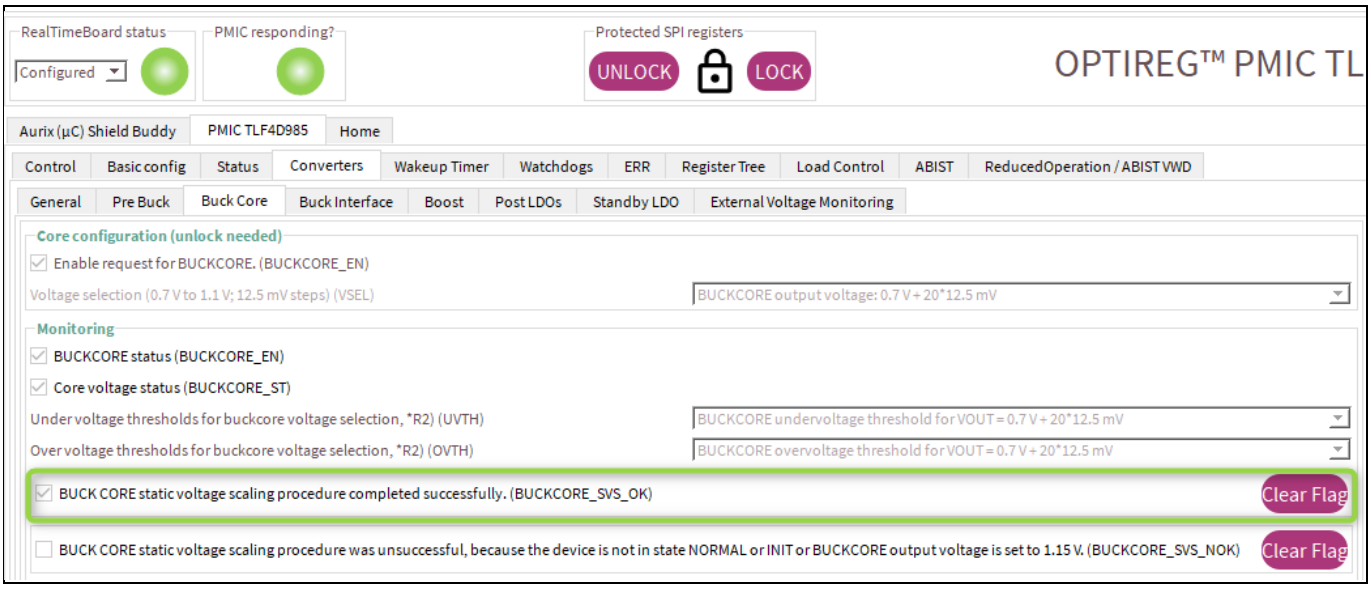


Figure 13 After locking the status values have changed accordingly

3.2 Watchdogs

After startup the Watchdogs are switched off by the GUI.

After unlocking the protected registers, the configuration bitfields are editable. Except for the Enable-Bitfield. The watchdogs can only be enabled or disabled via the buttons to enable / disable at the same time the watchdog service via the µC. After clicking on WWD1 ON or FWD1 ON, the watchdog configuration is read out and the watchdog service is applied accordingly.

To enable the watchdog:

1. Unlock the protected registers via the button in the header row
2. Configure the watchdog to your needs
3. Lock the protected registers
4. Press WWD1 ON or FWD1 ON

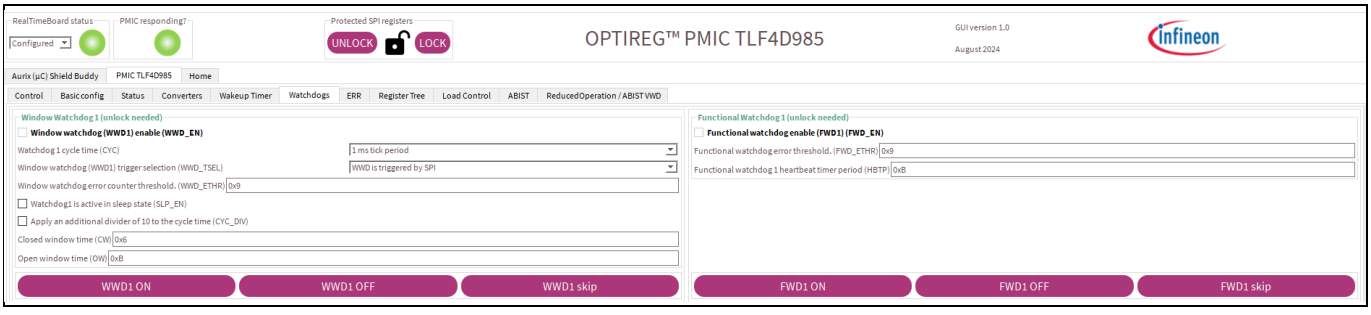


Figure 14 Controls of WWD1 and FWD1

When WWD1 skip is pressed, 2 watchdog services are skipped. The error counter value is incremented to 4 and is decremented to 0 afterwards because of valid services following afterwards.

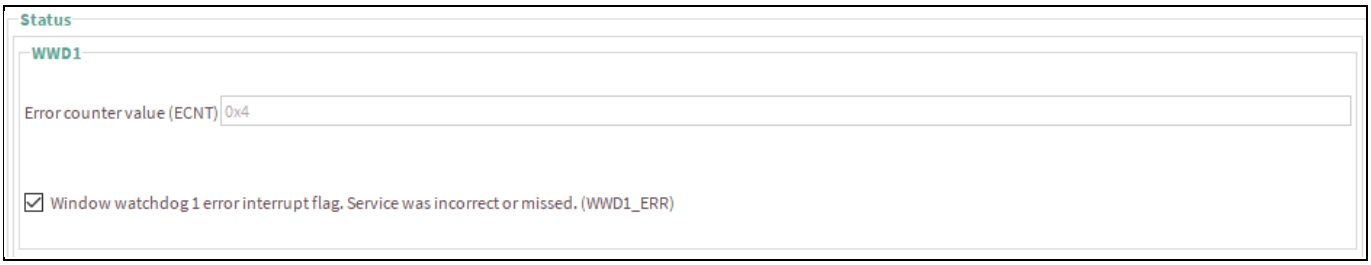


Figure 15 WWD1 error counter after 2 watchdog services were skipped

3.3 ERR-Monitoring

The configuration bitfields can be accessed after unlocking.

The enable bitfield can only be accessed via the buttons ERRx ON/OFF. The PWM generation is activated via the Duty-cycle:

- Button ERRx OFF sets Duty-cycle = 1
- Button ERRx ON sets Duty-cycle = 0.5. It can be modified manually as well

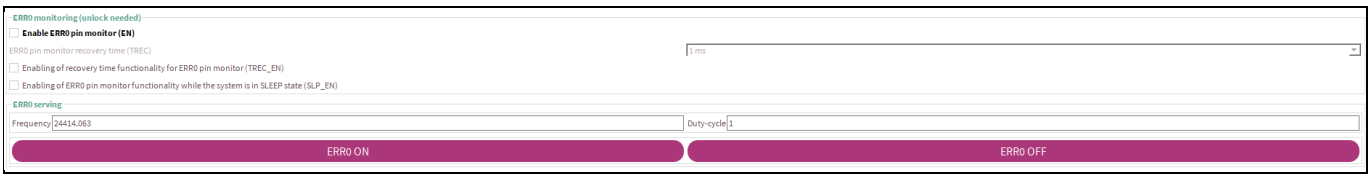


Figure 16 Controls of the ERR-Monitoring

Failure injection is not implemented in the GUI.

3.4 Scripting

The evaluation suite allows to define custom SPI sequences by defining JavaScript in the tab *Aurix (µC) Shield Buddy → Custom scripting*.

Figure 18 defines the basic instructions for reading and writing via SPI to the PMIC registers.

The output of the print command can be seen on the Shell output on the right side.

Note: The register content is frequently read in the background in order to show the content on the GUI. In case the SPI communication in the implemented JavaScript should be the only communication, the background read can be switched off via Aurix (µC) Shield Buddy → General Configurations → Disable Continous PMIC Register Scan.

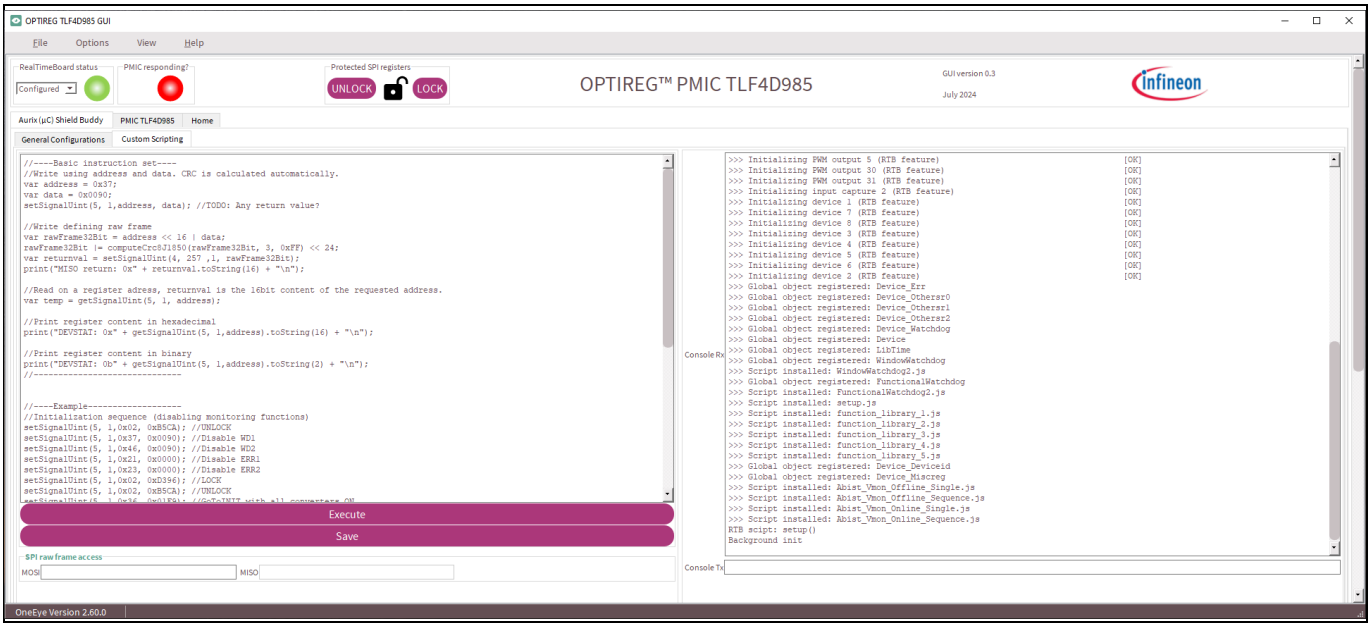


Figure 17 Custom scripting with the script to be run on the left side and the console output on the right side

```
//Write using address and data. CRC is calculated automatically.
var address = 0x37;
var data = 0x0090;
setSignalUint(5, 1,address, data);

//Write defining raw frame
var rawFrame32Bit = address << 16 | data;
rawFrame32Bit |= computeCrc8J1850(rawFrame32Bit, 3, 0xFF) << 24;
var returnval = setSignalUint(4, 257 ,1, rawFrame32Bit);
print("MISO return: 0x" + returnval.toString(16) + "\n");

//Read on a register adress, returnval is the 16bit content of the requested address.
var temp = getSignalUint(5, 1, address);

//Print register content in hexadecimal
print("DEVSTAT: 0x" + getSignalUint(5, 1,address).toString(16) + "\n");

//Print register content in binary
print("DEVSTAT: 0b" + getSignalUint(5, 1,address).toString(2) + "\n");
```

Figure 18 Basic instruction set to define a SPI sequence

3.5 Sending quickly a single raw SPI frame

Below the *Execute* and *Save* buttons on the *Custom Scripting* tab there are 2 text fields giving direct access to the SPI channel.

Follow this sequence:

1. Write the 32-bit hex value of the MOSI command in the field *MOSI raw value (hex)*
2. Press enter
3. The 32-bit MISO value of the same SPI frame is printed in the field *MISO raw value (hex)*

This interface is not implementing any protocol nor CRC checksum.

4 Known issues

4.1 TLF4D985 BOARD v1.0

Following known issues apply to the TLF4D985 evaluation board V1.0

- Design step A11 is mounted. An errata sheet applies, which can be found on Infineon myICP.
- The schematic is not designed according to the requested schematic in the latest datasheet. Please follow the schematic recommendation stated in the latest datasheet, which can be found on Infineon myICP.
- The output capacitor of BuckIF C402 is dimensioned with only 22 µF. The latest datasheet requests 47 µF. Depending on the effective capacitance, there can be oscillations on BuckIF output voltage at some load conditions.

4.1 TLF4D985 BOARD v1.1

- The layout is not implementing fully the concept of flat horizontal layout which is proposed in the EMC Appnote:
    - Output capacitors of BuckCore and BuckIF have GND only via the package corners to the exposed pad. It is better to have direct contact to GND plane at the capacitors.
    - The GND contact via the package corners is in addition for the HF current via the HF capacitors (100 nF / 1 µF).

5 BOM

Table 5 Bill of material

Quantity	Designator	Fitted	QuickPick
5	ADCH_CON, ADCL_CON, COMM_CON, PW_CON, PWML_CON	Fitted	0° (vertical) / Board-to-Board
2	BATT, QPREREG	Fitted	90° (right angle) / Board-to-Cable
4	C100, C106, CENA, CWAK	Fitted	1nF / 50V / 10% / X7R (EIA) / 0603 (1608)
1	C101	Fitted	1uF / 50V / 10% / X7R (EIA) / CAPC3216X180N
7	C102, C202, C203, C301, C302, CIN1, CIN2	Fitted	100nF / 50V / 20% / X7R (EIA) / 0805
6	C103, C309, C400, C402, C500, C502	Fitted	1uF / 16V / 20% / X7R (EIA) / CAPC2013X140N
2	C104, C105	Fitted	10uF / 50V / 20% / X7S (EIA) / 1210
0	C201	Not Fitted	1uF / 50V / 20% / X5R (EIA) / 0805 (2012)
3	C204, C205, C206	Fitted	22uF / 10V / 10% / X7R (EIA) / CAPC3225X270N
0	C207	Not Fitted	22uF / 10V / 10% / X7R (EIA) / CAPC3225X270N
6	C303, C304, CCO1, CQST1, CQVR1, CUC1	Fitted	4.7uF / 16V / 20% / X7R (EIA) / 0805 (2012)
0	C305, C306	Not Fitted	10uF / 25V / 10% / X7R (EIA) / 1206
3	C307, C308, C403	Fitted	47uF / 6.3V / 20% / X5R (EIA) / 1206 (3216)
3	C310, C401, C503	Fitted	100nF / 50V / 20% / X7R (EIA) / CAPC1608X90N
1	C501	Fitted	10uF / 16V / 10% / X7S (EIA) / 0805 (2012)
0	CCO2, CQST2, CQVR2, CUC2	Not Fitted	4.7uF / 16V / 20% / X7R (EIA) / 0805 (2012)
1	Ccomp	Fitted	2.7nF / 50V / 5% / X7R (EIA) / 0402 (1005)
1	CIN3	Fitted	4.7uF / 50V / 20% / X7R (EIA) / CAPC3216X180N
1	CIN4	Fitted	100uF / 50V / 20% / SMD
1	CM1	Fitted	
17	CoreMinLoad, RERR0, RERR1, RINT1, RINT2, RLED0, RLED1, RLED2, RLED3, RLED4, RLED5, RLED6, RLED7, RLED8, RLED9, RLED10, RWDI1	Fitted	1k / 1% / 0.1 / 0603
2	D100, D101	Fitted	Schottky Diode / SOD-323HE
1	D102	Fitted	Standard Diode / SOD
1	D103	Fitted	Zener Diode / SOD323
1	D104	Fitted	Zener Diode / SOD-123

5 BOM

Quantity	Designator	Fitted	QuickPick
1	D500	Fitted	Schottky Diode / MicroSMP (DO-219AD)
10	DQBOOST, DQCO, DQCORE, DQINERFACE, DQPRE, DQST, DQUC, DQVR, DSSO1, DSSO2	Fitted	LED / 0603
1	DROT	Fitted	LED / 1608 (0603)
1	Extended IO	Fitted	0° (vertical) / Board-to-Board
2	GND, GND1	Fitted	90° (right angle) / Board-to-Cable
2	IFminLoad, RRES_PU	Fitted	4.7k / 1% / 0.1 / 0603
2	J-ENA, J-WAK	Fitted	0° (vertical) / Board-to-Board
11	J-ENA-Default, J-ERR-DefaultERR0, J-ERR-DefaultERR1, J-INT1-default, J-INT2-default, J-INT3, J-INT4, J-LED-Default1, J-LED-Default2, J-WAK-Default1, J-WDI-Default	Fitted	
8	J-ERR0, J-ERR1, J-INT1, J-INT2, J-LED, J-ROT, J-WDI, J-Boost_shorted	Fitted	0° (vertical) / Board-to-Board
0	L101	Not Fitted	4.7uH / Standard / SMD
1	L201_10A	Fitted	6.8uH / Standard / 7.2mmX7.5mmX7mm
2	L301, L302	Fitted	1uH / Standard / 3225
0	L301_, L302_	Not Fitted	1uH / Standard / 4mm X 4mm
1	L400	Fitted	2.2uH / SMD
1	L500	Fitted	3.3uH / Standard / 3.2mm x 3.5mm
1	MON CON	Fitted	0° (vertical) / Board-to-Board/Cable
1	PWMH_CON	Fitted	0° (vertical) / Board-to-Board
1	Q101	Fitted	NPN / 415mW / 500mA / 80V / SOT23 (TO-236AB)
1	Q601	Fitted	N-Channel Enhancement / 31W / 45A / 40V / PG-TDSON-8-57
1	Q602	Fitted	N-Channel Enhancement / 65W / 20A / 55V / PG-TDSON-8-10
2	QLED2, QLED3	Fitted	NPN / 250mW / 100mA / 45V / SOT323
1	QROT	Fitted	P-Channel Enhancement / 2W / -6A / -20V / PG-TSOP-6
6	R100, R105, R107, R111, R113, TLF4D985QKV03 (QUC=3.3V, QIF=1.8V)	Fitted	0R / 0R / 0603
1	R101	Fitted	0R / 0R / 1210
2	R102, R103	Fitted	47k / 1% / 0.1 / 0603
1	R104	Fitted	300k / 1% / 0.1 / 0603
0	R106, R110, R114, RHW_0, TLF4D985QKV01 (QUC=5V, QIF=3.3V), TLF4D985QKV02 (QUC=3.3V, QIF=3.3V)	Not Fitted	0R / 0R / 0603
1	R108	Fitted	10R / 1% / 0.1 / 0603 (1608)
1	R109	Fitted	499k / 1% / 0.1 / 0603
1	R201_10A	Fitted	
1	Rcomp	Fitted	12k / 1% / 0.063 / 0402 (1005)

5 BOM

Quantity	Designator	Fitted	QuickPick
2	RENA, RWAK	Fitted	10k / 1% / 0.125 / 0805
2	RENAPD, RWAKPD	Fitted	49.9k / 1% / 0.125 / 0805
3	RERR0_1, RERR1_1, RWDI_PD	Fitted	51k / 1% / 0.1 / 0603
1	RHW_1	Fitted	2.2k / 1% / 0.1 / 0603
2	RHW_2, RSDI2	Fitted	3.3k / 1% / 0.1 / 0603
2	RHW_3, Rver_L	Fitted	6.8k / 1% / 0.1 / 0603
1	RHW_4	Fitted	15k / 1% / 0.1 / 0603
1	RHW_5	Fitted	22k / 1% / 0.1 / 0603
1	RHW_6	Fitted	33k / 1% / 0.1 / 0603
1	RHW_7	Fitted	68k / 1% / 0.1 / 0603
1	RHW_8	Fitted	100k / 1% / 0.1 / 0603
5	RINT1PD, RINT2PD, RRES_PD, RSS1PD, RSS2PD	Fitted	100k / 1% / 0.125 / 0805
2	RL2_B, RL3_B	Fitted	220R / 1% / 0.1 / 0603
7	RRES, RSCL, RSCS, RSDI, RSDO, RVEN1, RVEN2	Fitted	100R / 1% / 0.1 / 0603
0	RSCL2, RSCS2	Not Fitted	3.3k / 1% / 0.1 / 0603
0	Rspi_c_H, Rvar_H	Not Fitted	1k / 1% / 0.125 / 0805
2	Rspi_c_L, Rvar_L	Fitted	1k / 1% / 0.125 / 0805
6	RVEN3, RVEN4, RVM1, RVM1_1, RVM2, RVM2_1	Fitted	220k / 1% / 0.1 / 0603
1	Rver_H	Fitted	3k / 1% / 0.1 / 0603 (1608)
1	S_HWCONFIG	Fitted	
1	S_WakuUp	Fitted	
1	SPI	Fitted	0° (vertical) / Board-to-Board
26	TB1GND, TB1O, TB1R1, TB1SW, TB4O, TB4SW, TB23O, TBATP, TBF, TBOO, TBOSW, TERR0, TERR1, TINT1, TINT2, TQCO, TQST, TQUC, TQVR, TROT, TSS1, TSS2, TSSCG, TSSCS, TVS, TWDI	Fitted	None (onboard) / Board-to-Cable
8	TB4GND, TB23GND, TBOGND, TGND1, TGND2, TGND3, TGND4, TGNDL	Fitted	0° (vertical) / Board-to-Board
1	U601	Fitted	PG-LQFP-64-28
2	X1, X2	Fitted	0° (vertical) / Board-to-Cable

6 Schematic and assembly drawing

The schematic and assembly drawing are included at the end of this document.

Revision history

Document revision	Date	Description of changes
1.1	2026-02-17	Update for board version 1.1 and GUI version 1.1
1.0	2024-08-02	Update to OneEye 2.60 and GUI version 1.0
0.31	2023-11-08	Minor editorial changes
0.3	2023-10-31	Add instructions on license request Add chapter about scripting
0.2	2023-10-30	Initial release Change of template
0.1	2023-10-19	Initial draft

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2026-02-17

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

Z8F80518846

Warnings
Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

Index

Schematics Page Name

Page	
01	Cover Sheet / Revision History
02	TLF4D985_Main
03	Interfaces
04	Loadcontrol
05	
06	
07	
08	
09	
10	

00_Cover.SchDoc

Revision History

Rev.	Rel.	Date	Author	Description	Page(s)
1.0	-	2022-11-11	Demmelhuber	Initial Version of TLF4D985QKVSxx Evaluation Board based on TLF38885 Evaluation Board v1.1	
1.1		2025-11-15	schaffam	-Changed pinning of MON CON, to allow disabling via jumper -change BuckIF cap to 47µF -changed Pinheader to long ones -changed version marking -changed SSW to IPG20N06S2L-35A -changed SSW disabling routing -added gate resistor to SSW -changed version resistors -Removed load control circuitry and replaced by screw terminals -C201 changed to 1µF -Changed C307/C308 to 47µF -Add 10R resistor to at SSW gate -Changed D104 to 6.2V Zener -Removed shorting resistor D100 and mounted D100 as default -D100 changed to the recommended on in datasheet due to less reverse leakage -Add solder jumper in R3FBL -Change C400 to 1µF -Changed C304/C303 to 4.7µF, marked C305/C306 for not mounted -Added 1nF GateSource of RPP and SSW -Replaced solder jumper SJBx by larger ones -Remove SJB5 for AGND -Replaced 0R resistors from Variant marking with same type of 0R resistors used elsewhere -Changed RHW_2 to same manufacturer as RSDI2 -Changed D500 Partnumber -Change D101 to the same part as D100	

TLF4D985XX Evaluation Board

LQFP64 Variant

V1.1

2025

Title			
Variant	TLF4D985QKVS03	Approved	*
Size: A3	Document Name 00_Cover.SchDoc	Rel.	Rev.
Author:			
Date: 15.11.2025 Time: 19:16:17	SVN Revision: 494 [Locally Modified]		
	Sheet 1 of 4		

01_Main_power_supply.SchDoc

Output	V01	V02	V03
VQST	+5 V	+3.3 V	+3.3 V
VQUC	+5 V	+3.3 V	+3.3 V
BuckIF	+3.3 V	+3.3 V	+1.8 V
VCORE	+1.025 V		
VQVR	+5 V		
VQCO	+5 V		
VPRE	+4 V /+5.5 V		
VBOOST	+5.8 V		

Resistance	HW Configuration (see DS)
0R	4.0V / 10ms / MPS=OFF /schA
2.2k	4.0V / 2ms / MPS=OFF /schA
3.3k	4.0V / 2ms / MPS=OFF /schB
6.8k	5.5V / 2ms / MPS=OFF /schA
15k	5.5V / 2ms / MPS=OFF /schB
22k	5.5V / 2ms / MPS=ON /schB
33k	5.5V / 2ms / MPS=ON /schA
68k	4.0V / 2ms / MPS=ON /schB
100k	4.0V / 2ms / MPS=ON /schA
open	4.0V / 10ms / MPS=OFF /schA

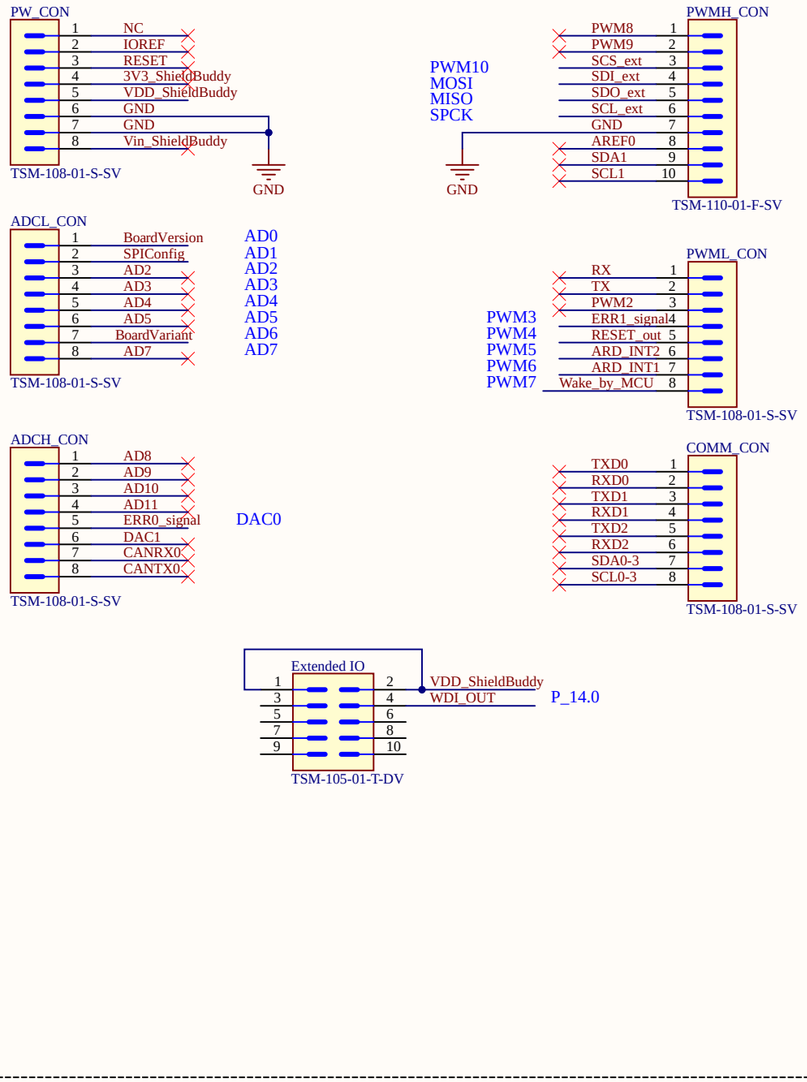
Ground test points

Connect differential traces (44 & 45) to point of load

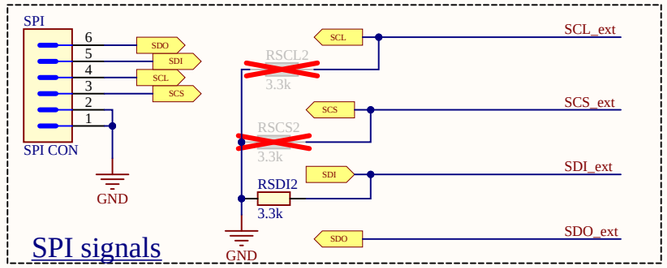
Title	
Variant	TLF4D985QKVS03
Approved	<Appr.>
Size: A3	Document Name: 01_Main_power_supply.SchDoc
Rel.	
Rev.	
Author:	
Date: 15.11.2025 Time: 19:16:17	SVN Revision: 495
Sheet 2 of 4	

02_Interfaces.SchDoc

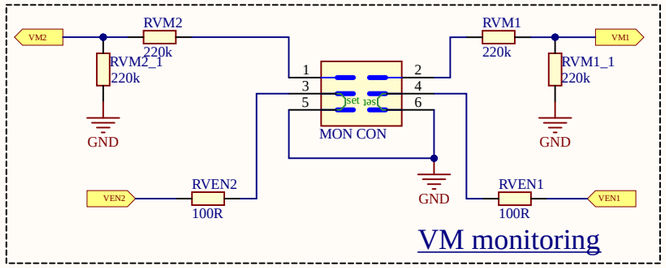
Arduino Shield Buddy Interface



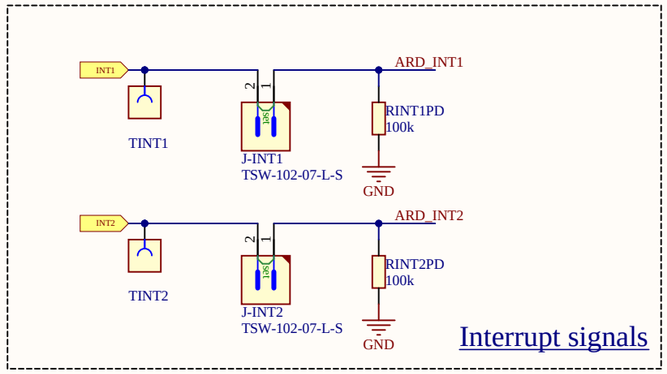
SPI signals



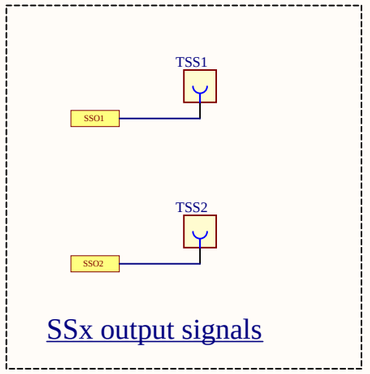
VM monitoring



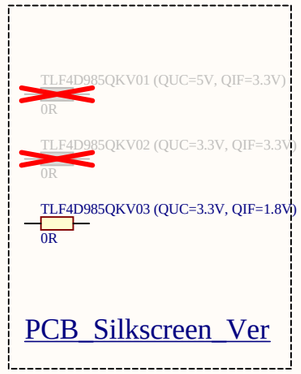
Interrupt signals



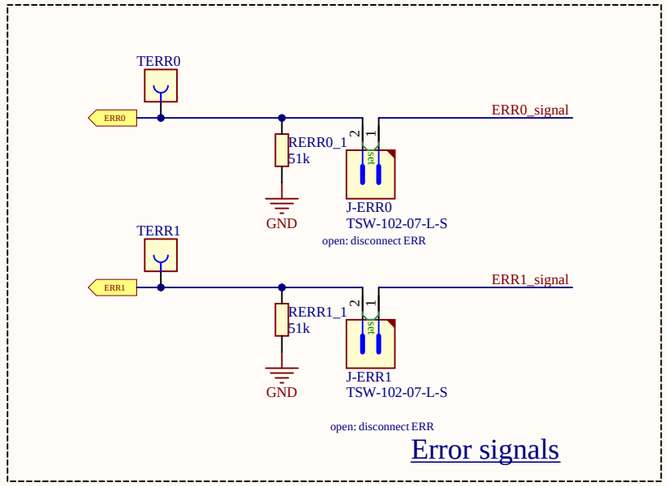
SSx output signals



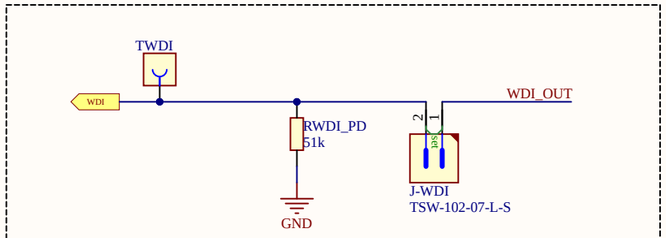
PCB_Silkscreen_Ver



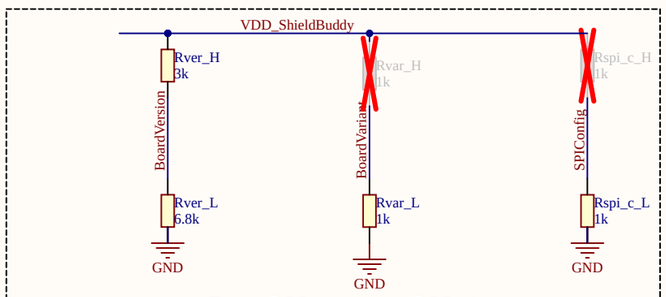
Error signals



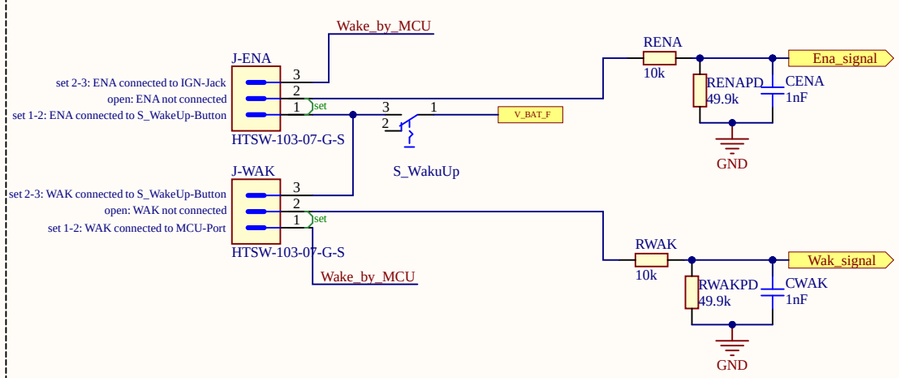
Window Watch Dog signal



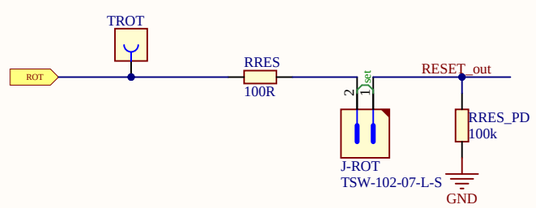
Board Version and Variant



WAKE / ENA source

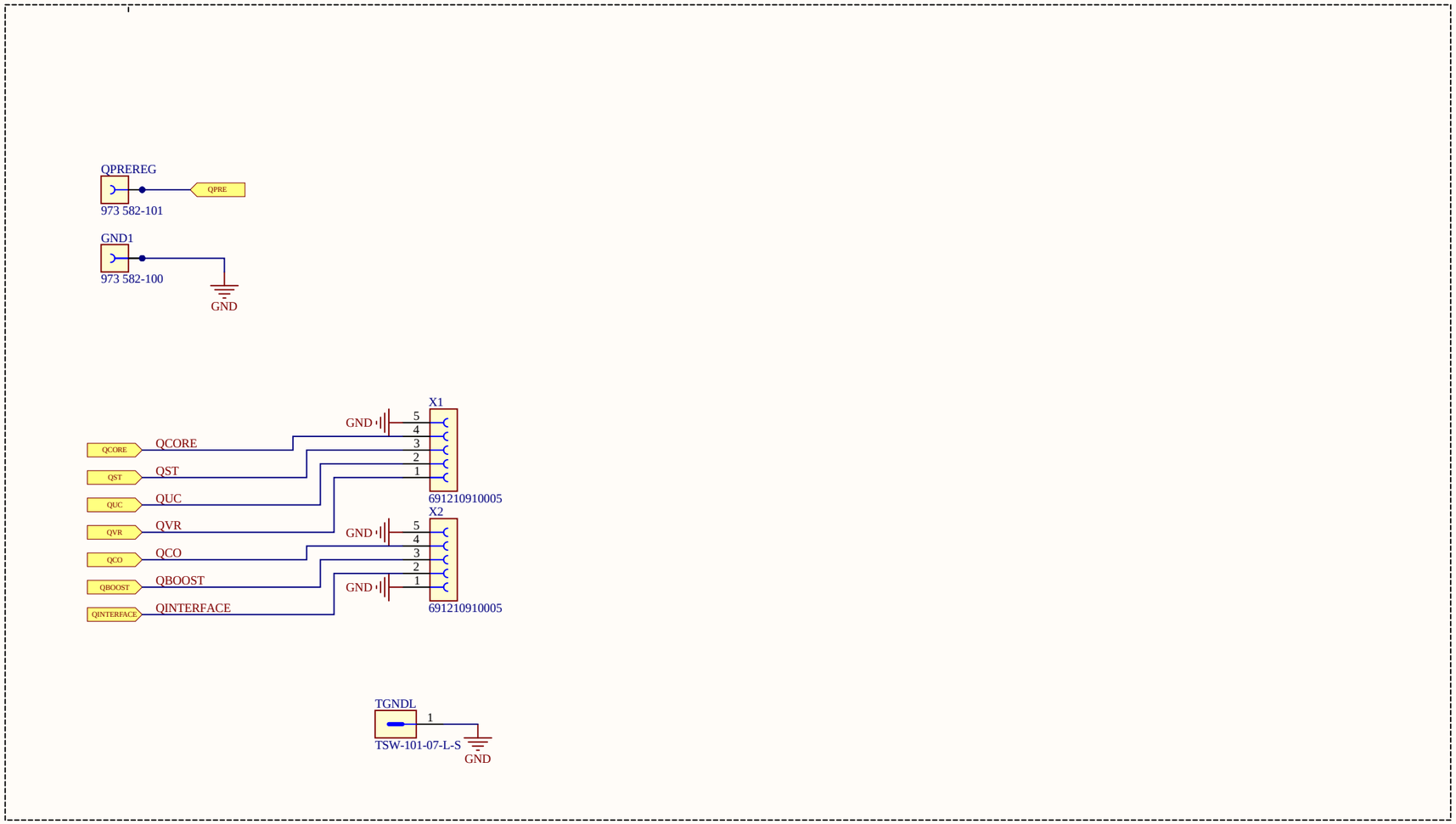


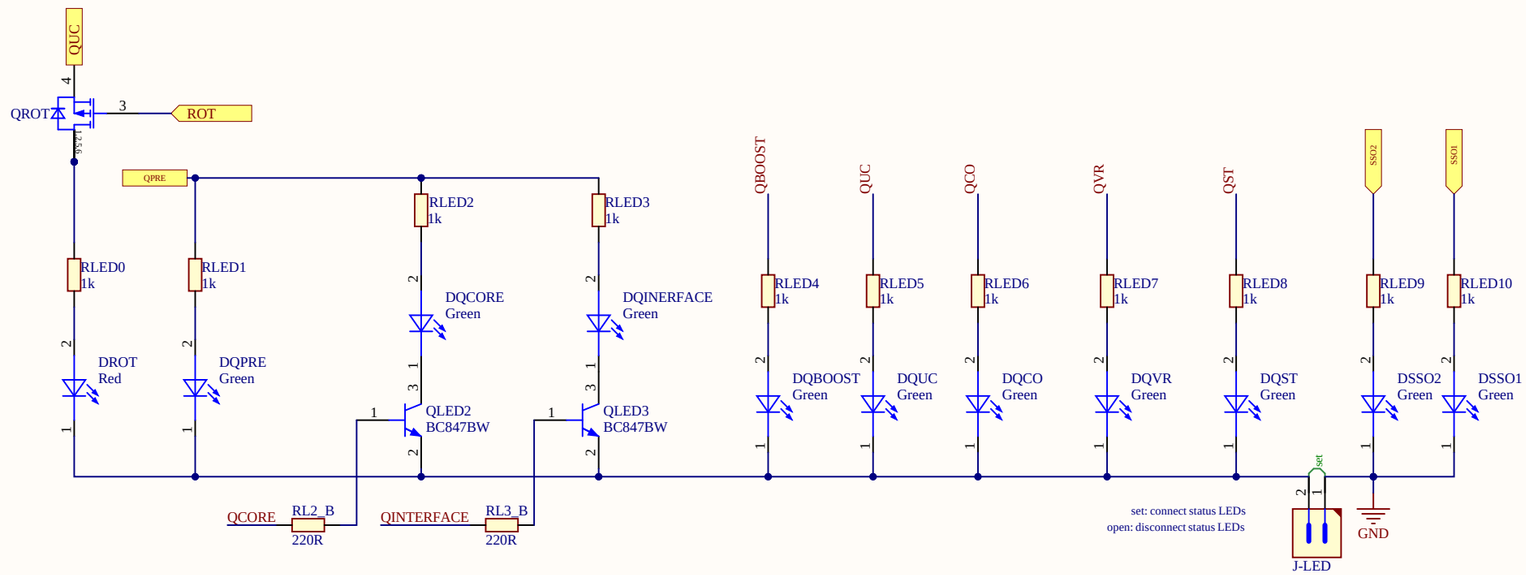
Reset signal

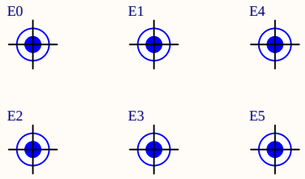


Title			
Variant	TLF4D985QKVS03	Approved	*
Size: A3	Document Name 02_Interfaces.SchDoc	Rel.	Rev.
Author:			
Date: 15.11.2025 Time: 19:16:18	SVN Revision: 490		
		Sheet 3	of 4

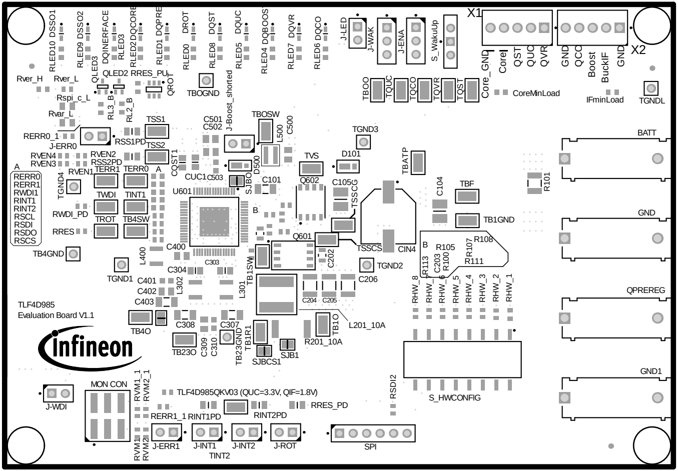
03_Loadcontrol.SchDoc







Title			
Variant	TLF4D985QKVS03	Approved	*
Size: A3	Document Name 03_Loadcontrol.SchDoc	Rel.	Rev.
Author:			
Date: 15.11.2025 Time: 19:16:18	SVN Revision: 485		
	Sheet 4 of 4		



	Datum	Name	Änd.-Nr.	Datum	Name	geprüft	Änd.-Nr.	Datum	Name	geprüft
gez.	15.11.2025	Lw/beflex								
gepr.										
Diese Zeichnung nur mit CAD ändern										

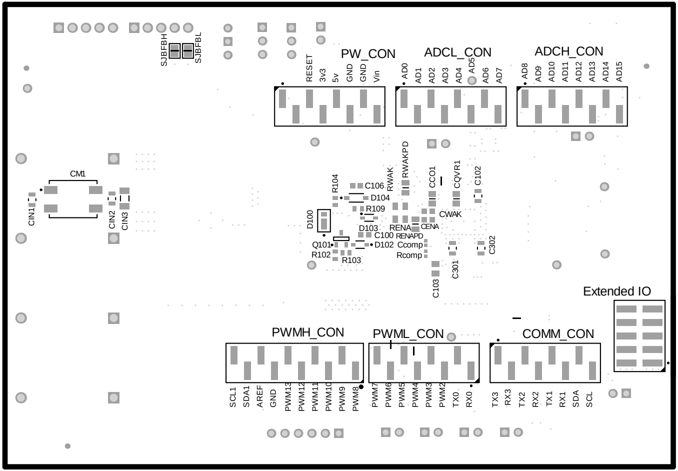
C:\Developer\svn\TLF4x_Family_CustomerSupport\Annapruna_Product_TLF4D985\08_Evaluation_Board_Project\Eval_TLF4D985xx_10A_v1.1\TLF4D985xx_LQFP.PcbDoc

KATEK Lead the category	Teile und Bearbeitung RoHS- u. REACH-konform	Benennung : TLF4D985QKVS03	Mass. : 2 : 1	LP.-Nr. : TLF4D985 Evaluation Board V1.1
			Blatt :	Zeichn.-Nr. : TLF4D985QKVS03

	1	2	3	4	5	6	7	8

A

B



C

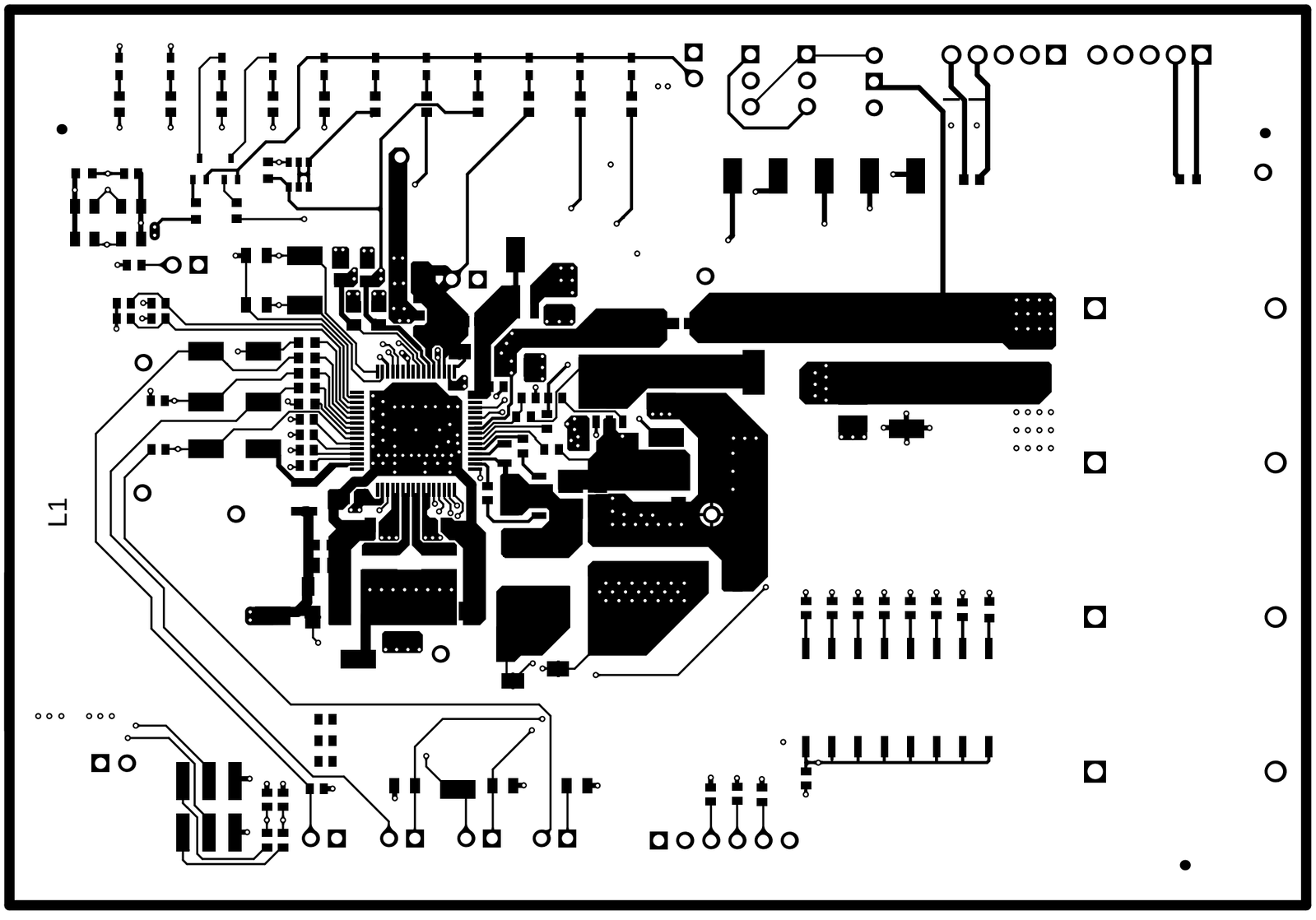
D

E

	Datum	Name	Änd.-Nr.	Datum	Name	geprüft	Änd.-Nr.	Datum	Name	geprüft
gez.	15.11.2025	Lw/beflex								
gepr.										
Diese Zeichnung nur mit CAD ändern										

C:\Developer\svn\TLF4x_Family_CustomerSupport\Annapruna_Product_TLF4D985\08_Evaluation_Board_Project\Eval_TLF4D985xx_10A_v1.1\TLF4D985xx_LQFP.PcbDoc

KATEK Lead the category	Teile und Bearbeitung RoHS- u. REACH-konform	Benennung : TLF4D985QKVS03	Mass. : 2 : 1	LP.-Nr. : TLF4D985 Evaluation Board V1.1
			Blatt :	Zeichn.-Nr. : TLF4D985QKVS03



	Datum	Name	Änd.-Nr.	Datum	Name	geprüft	Änd.-Nr.	Datum	Name	geprüft
gez.	11.11.2022	Lw/beflex								
gepr.										
Diese Zeichnung nur mit CAD ändern										

C:\Developer\svn\TLF4x_Family_CustomerSupport\Annapruna_Product_TLF4D985\08_Evaluation_Board_Project\Eval_TLF4D985xx_10A_v1.1\TLF4D985xx_LQFP.PcbDoc

KATEK
Lead the category

Teile und Bearbeitung
RoHS- u. REACH-konform

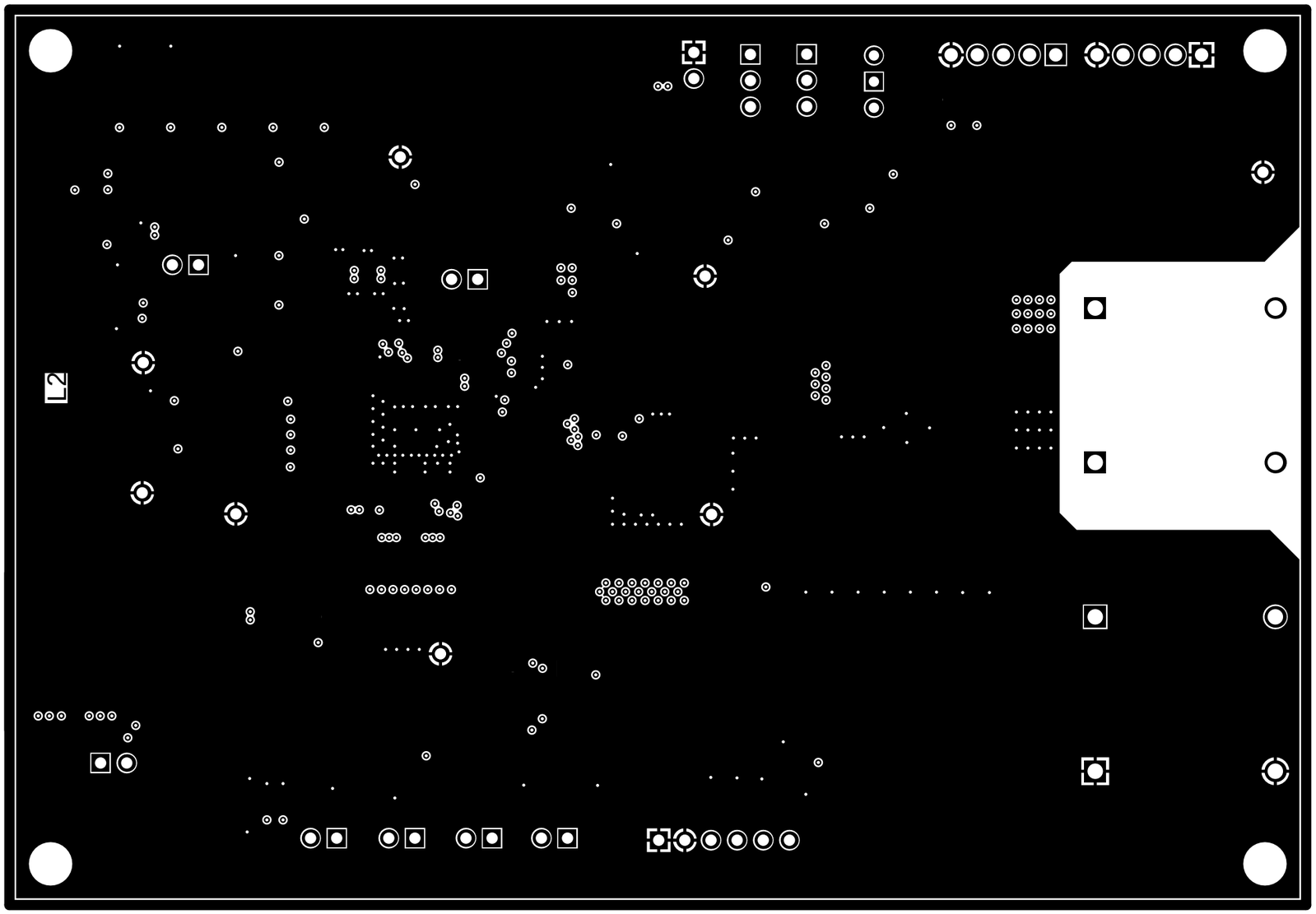
Benennung : .VariantenName

Mass. : 2 : 1

Blatt :

LP.-Nr. : TLF4D985 Evaluation Board V1.0

Zeichn.-Nr. : .VariantenNummer



	Datum	Name	Änd.-Nr.	Datum	Name	geprüft	Änd.-Nr.	Datum	Name	geprüft
gez.	11.11.2022	Lw/beflex								
gepr.										
Diese Zeichnung nur mit CAD ändern										

C:\Developer\svn\TLF4x_Family_CustomerSupport\Annapruna_Product_TLF4D985\08_Evaluation_Board_Project\Eval_TLF4D985xx_10A_v1.1\TLF4D985xx_LQFP.PcbDoc

KATEK
Lead the category

Teile und Bearbeitung
RoHS- u. REACH-konform

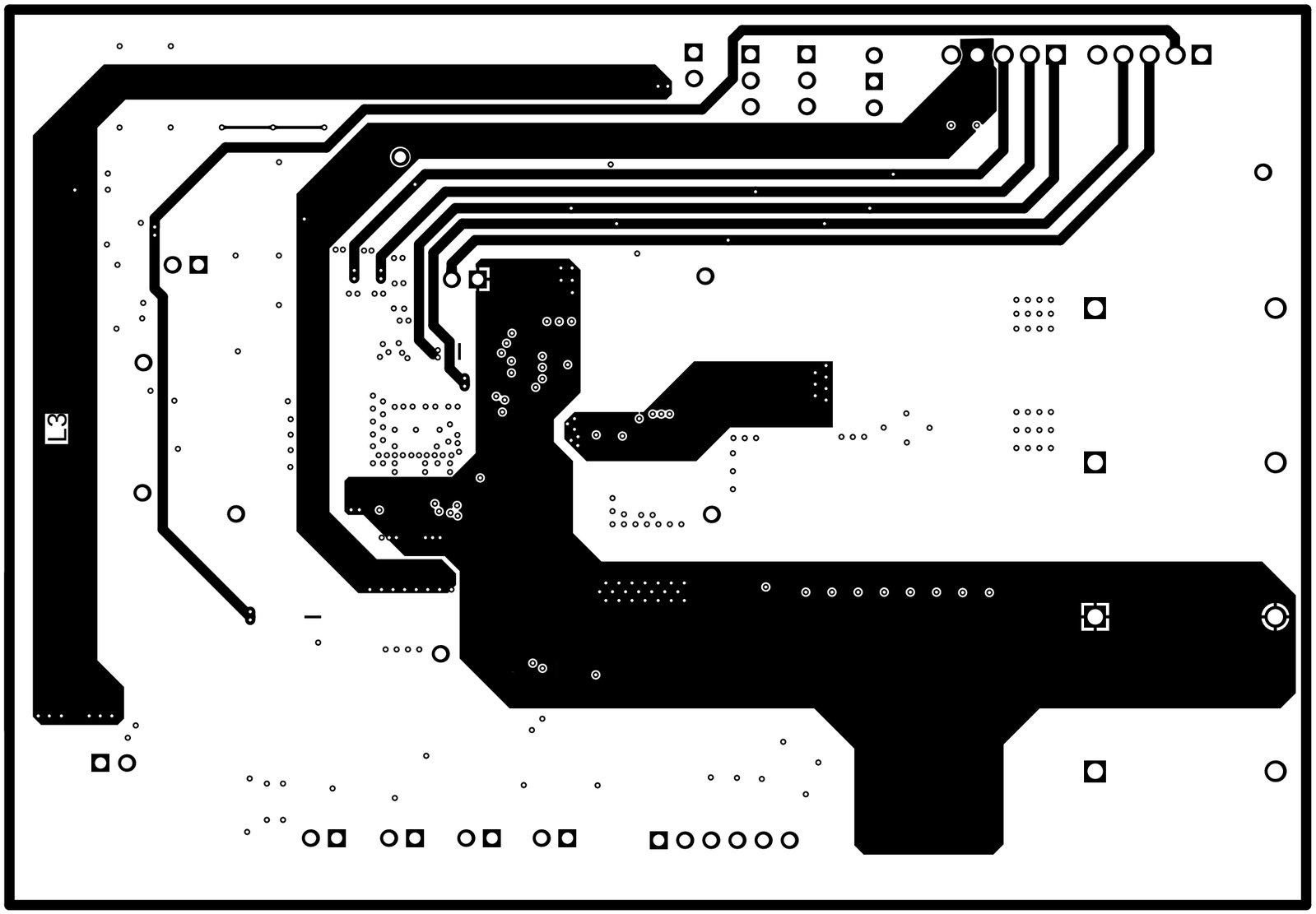
Benennung : .VariantenName

Mass. : 2 : 1

Blatt :

LP.-Nr. : TLF4D985 Evaluation Board V1.0

Zeichn.-Nr. : .VariantenNummer



	Datum	Name	Änd.-Nr.	Datum	Name	geprüft	Änd.-Nr.	Datum	Name	geprüft
gez.	11.11.2022	Lw/beflex								
gepr.										
Diese Zeichnung nur mit CAD ändern										

C:\Developer\svn\TLF4x_Family_CustomerSupport\Annapruna_Product_TLF4D985\08_Evaluation_Board_Project\Eval_TLF4D985xx_10A_v1.1\TLF4D985xx_LQFP.PcbDoc

KATEK
Lead the category

Teile und Bearbeitung
RoHS- u. REACH-konform

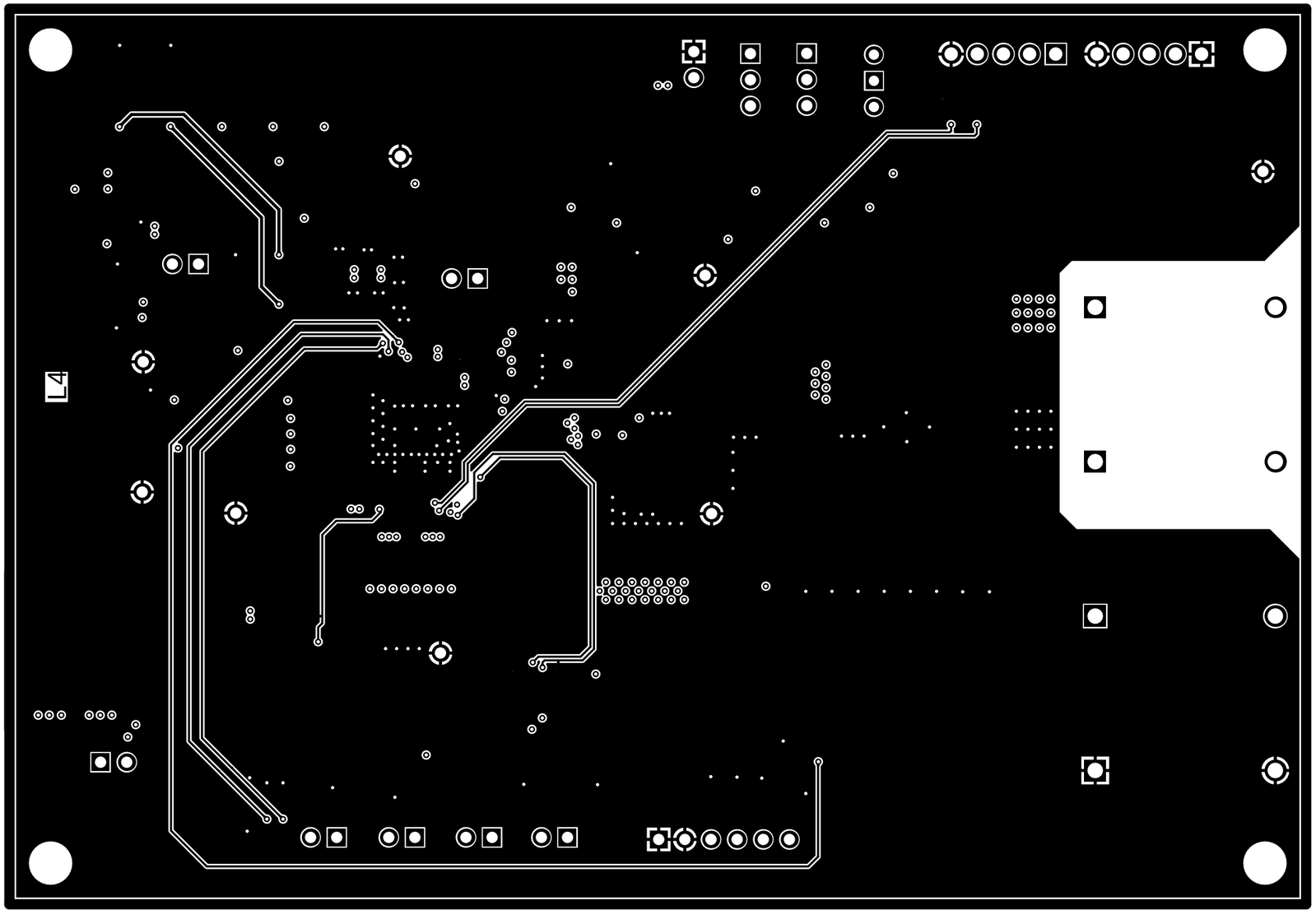
Benennung :
.VariantenName

Mass. : 2 : 1

Blatt :

LP.-Nr. : TLF4D985 Evaluation Board V1.0

Zeichn.-Nr. : .VariantenNummer



	Datum	Name	Änd.-Nr.	Datum	Name	geprüft	Änd.-Nr.	Datum	Name	geprüft
gez.	11.11.2022	Lw/beflex								
gepr.										
Diese Zeichnung nur mit CAD ändern										

C:\Developer\svn\TLF4x_Family_CustomerSupport\Annapruna_Product_TLF4D985\08_Evaluation_Board_Project\Eval_TLF4D985xx_10A_v1.1\TLF4D985xx_LQFP.PcbDoc

KATEK
Lead the category

Teile und Bearbeitung
RoHS- u. REACH-konform

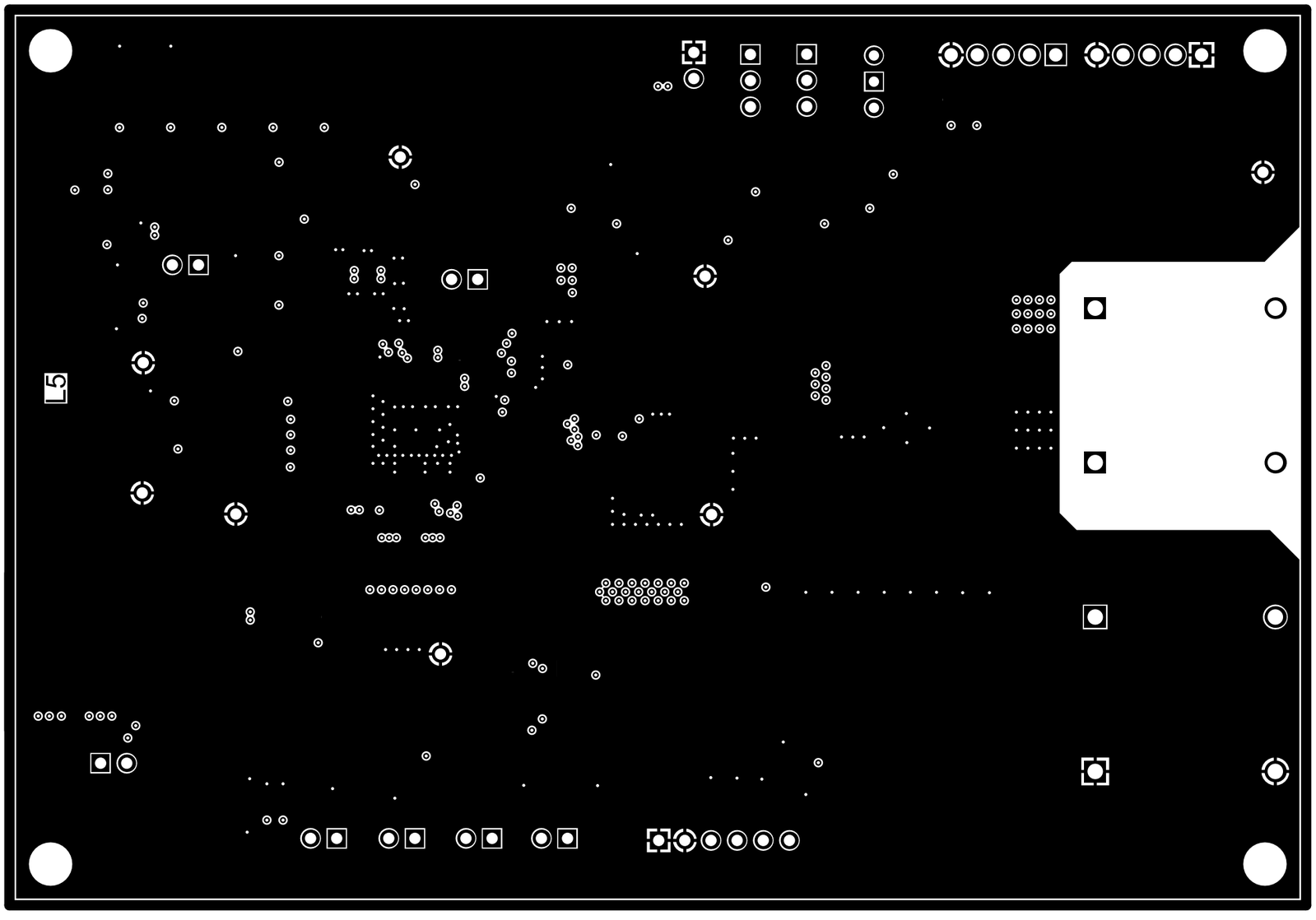
Benennung : .VariantenName

Mass. : 2 : 1

Blatt :

LP.-Nr. : TLF4D985 Evaluation Board V1.0

Zeichn.-Nr. : .VariantenNummer



	Datum	Name	Änd.-Nr.	Datum	Name	geprüft	Änd.-Nr.	Datum	Name	geprüft
gez.	11.11.2022	Lw/beflex								
gepr.										
Diese Zeichnung nur mit CAD ändern										

C:\Developer\svn\TLF4x_Family_CustomerSupport\Annapruna_Product_TLF4D985\08_Evaluation_Board_Project\Eval_TLF4D985xx_10A_v1.1\TLF4D985xx_LQFP.PcbDoc

KATEK
Lead the category

Teile und Bearbeitung
RoHS- u. REACH-konform

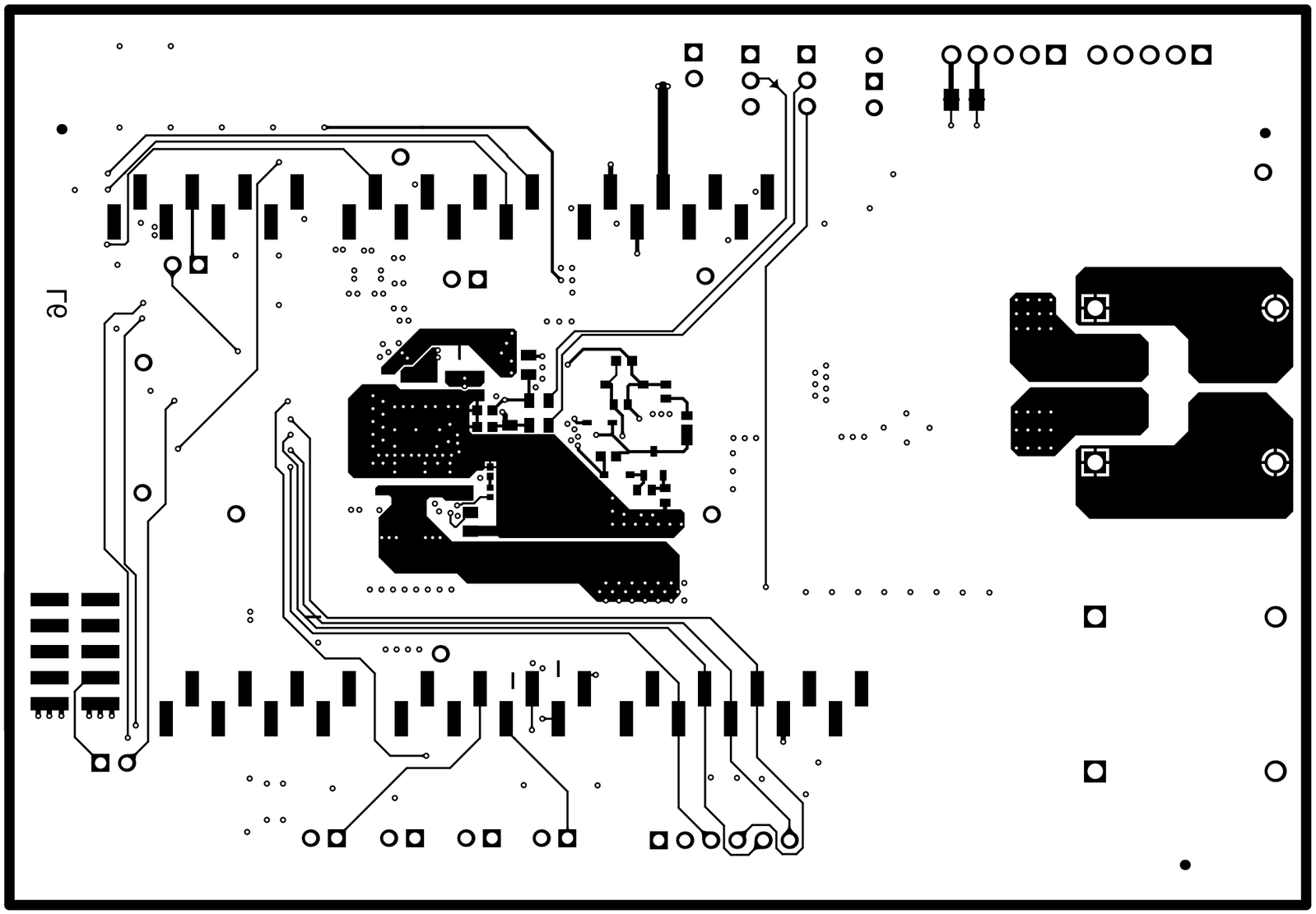
Benennung :
.VariantenName

Mass. : 2 : 1

Blatt :

LP.-Nr. : TLF4D985 Evaluation Board V1.0

Zeichn.-Nr. : .VariantenNummer



	Datum	Name	Änd.-Nr.	Datum	Name	geprüft	Änd.-Nr.	Datum	Name	geprüft
gez.	11.11.2022	Lw/beflex								
gepr.										
Diese Zeichnung nur mit CAD ändern										

C:\Developer\svn\TLF4x_Family_CustomerSupport\Annapruna_Product_TLF4D985\08_Evaluation_Board_Project\Eval_TLF4D985xx_10A_v1.1\TLF4D985xx_LQFP.PcbDoc

KATEK
Lead the category

Teile und Bearbeitung
RoHS- u. REACH-konform

Benennung : .VariantenName

Mass. : 2 : 1

Blatt :

LP.-Nr. : TLF4D985 Evaluation Board V1.0

Zeichn.-Nr. : .VariantenNummer