TLE9186

User manual

MOTIX™ TLE9186 gate driver IC for BLCD motors with current sense amplifier

About this document

Scope and purpose

This is the user manual of the product TLE9186QVW. The user manual provides additional information to the datasheet of the 3-phase gate driver TLE9186QVW for BLDC motor application from Infineon Technologies AG.

The user manual describes detailed technical aspects of the device required for integration in a system. The devices to which this manual applies are listed in the table "related devices" below. For the device's specification, please see the respective datasheet.

It contains detailed instructions on how to configure the device and how to use it in the application. This document contains information about:

- Additional information for each IC module: Additional functional information
- Diagnostic feature description: Diagnostics (additional information)
- SPI register definition: SPI (additional information)
- External components: Application information (additional information)

The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition, or quality of the device.

Intended audience

This document is intended for engineers who develop applications using TLE9186QVW.

For the device's specification, see the corresponding datasheet.

Related devices

Product type	Description and features	Package	Marking
TLE9186	Functional safety rated 3-phase bridge driver	VQFN-32	TLE9186QVW

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1 Additional functional information

This chapter includes additional information for each module of the device.

1.1 State machine (additional information)

This chapter provides additional information about the device state machine, which is described in the datasheet.

The device has three modes of operation:

- Sleep mode: low quiescent mode of device (INH_N = "low")
- Power-up mode: configuration of the device possible (INH_N = "high")
- Normal operation mode: active mode, where Gxx output stages can be turned on and off (INH_N = "high")

Transition between power-up mode and normal operation mode can be controlled by the microcontroller by SPI register PWR_MOD_CFG (register bits MODE_CTRL_x).

The following simplified table shows the behavior of the device depending on status of INH_N and control bits HBx_EN bit settings.

Table 1 State table

INH_N	Mode	Control bit for half-bridge	ERR_N	Output stages GHx and GLx
"low"	Sleep mode	X	OFF	OFF, safe state (passive discharge)
"high"	Power-up mode	X	"low"	OFF, safe state (passive discharge)
"high"	Normal-operation mode	disable	"high" see Note	OFF, safe state (passive discharge)
"high"	Normal-operation mode	enable	"high" see Note	ON, controlled by PWM inputs (if charge pump enabled and no LE1)

***Note**: The ERR_N pin is an open drain output pin. The resulting ERR_N level at the microcontroller input will be pulled up to "high" level due to the external pull-up resistor R_{ERR_PU}. ERR_N pin follows error indication according to configured failure behavior.*

1.1.1 Sleep mode

The sleep mode is the low quiescent current mode of the device. In sleep mode all device internal functions are deactivated and output stages are kept OFF. ERR_N pin is not driven actively "low" by the device and pulled up to VIO supply by R_{ERR_PU}.

Sleep mode is entered from normal operation mode OR power-up mode in case INH_N pin is set to "low" for $t > t_{INH_filter}$ AND without SPI communication during $t_{INH_L_WAIT}$. After $t_{INH_L_WAIT}$ expiration, sleep mode is entered after t_{SMA}.

1.1.1.1 INH_N pin function

The INH_N pin can be used to trigger sleep mode entry OR to trigger safe state entry without entering sleep mode and losing SPI configuration. There are various possibilities to cancel the power-down sequence of the device and to trigger safe state entry by the INH_N pin function:

1. INH_N pin set to "high" during $t_{INH_L_WAIT}$
2. Valid SPI communication detected by the device during $t_{INH_L_WAIT}$ (INHN_L_CFG = 0_B)
3. Valid SPI communication detected by the device during $t_{INH_L_WAIT}$ restarts $t_{INH_L_WAIT}$. If during $t_{INH_L_WAIT}$ no SPI communication is detected during $t_{INH_L_WAIT}$, the device will go to sleep mode (INHN_L_CFG = 1_B)

The diagrams below show the different cases for canceled power-down sequence and successful sleep mode entry.

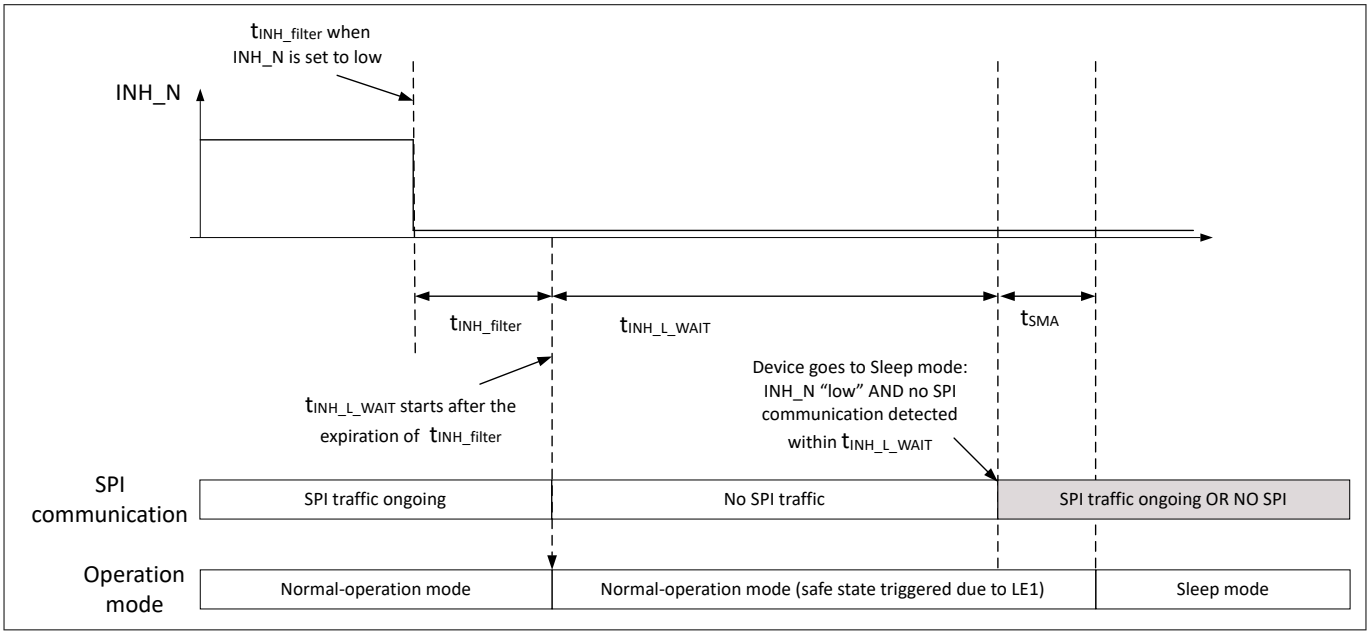

Figure 1 Sleep mode entry - power-down due to INH_N "low"

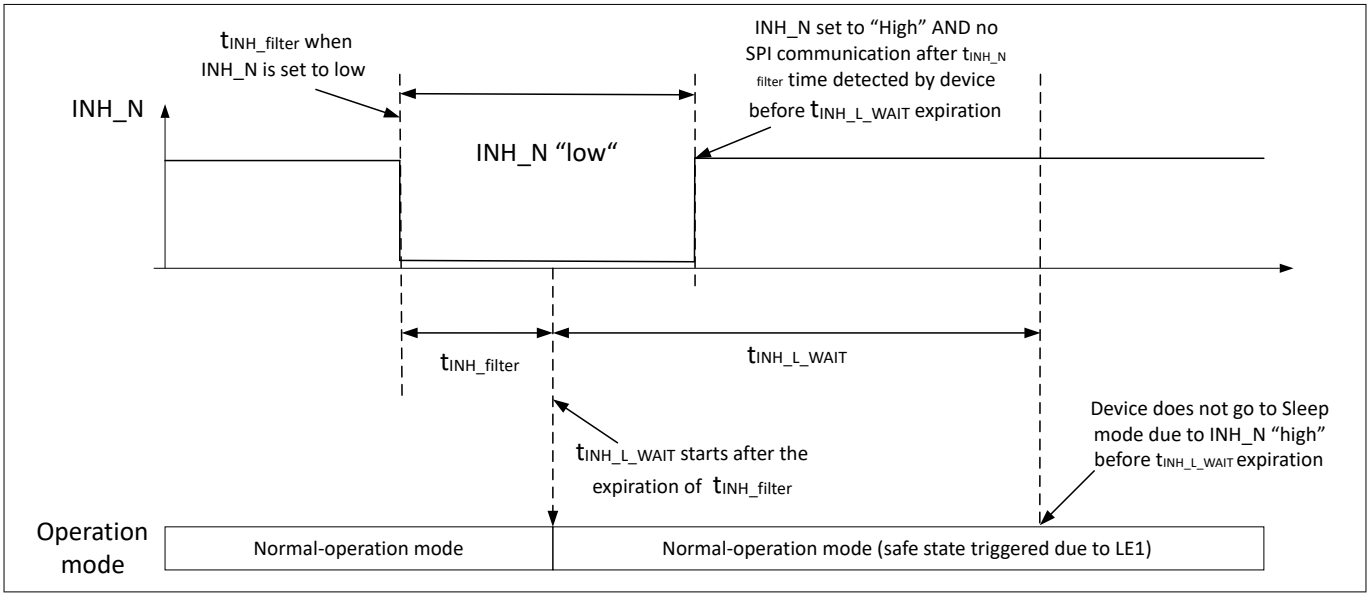

Figure 2 Canceled power-down due to INH_N "high" during $t_{INH_L_WAIT}$

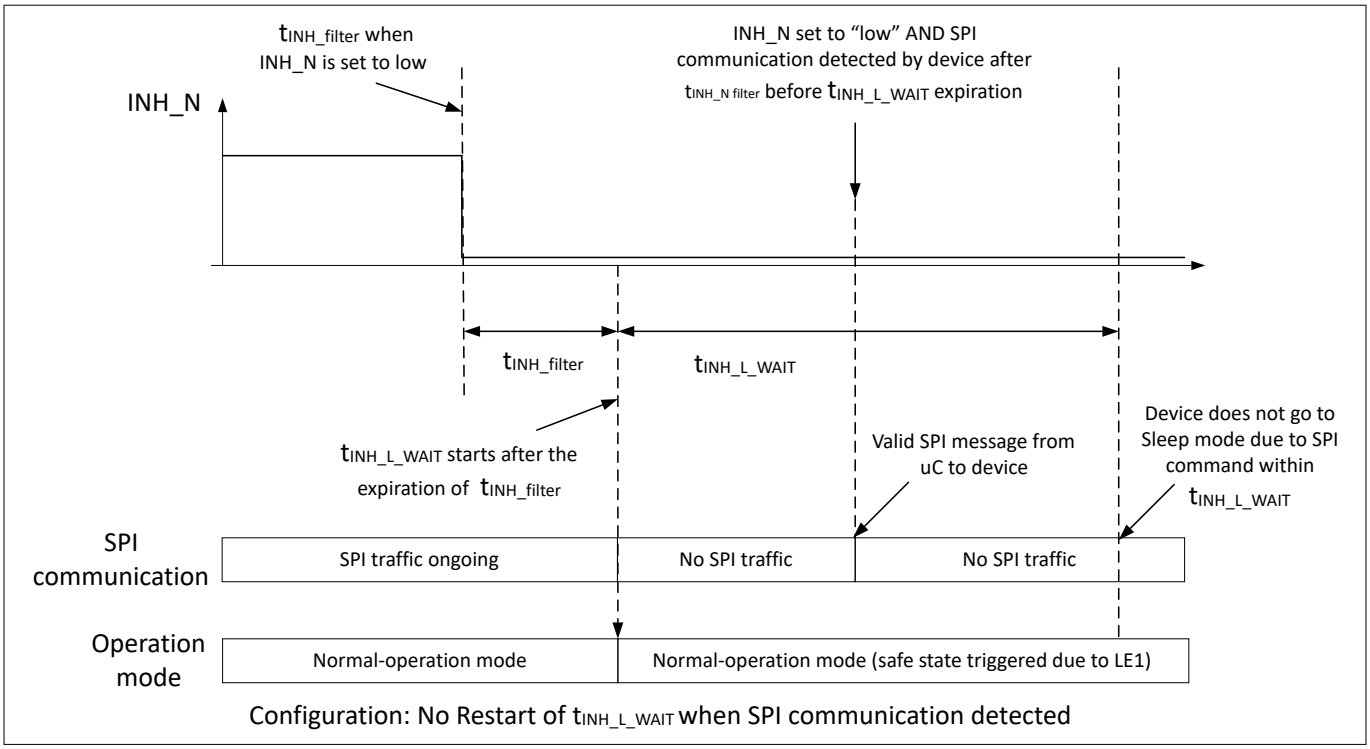

Figure 3 Canceled power-down due to SPI communication without restart of $t_{INH_L_WAIT}$

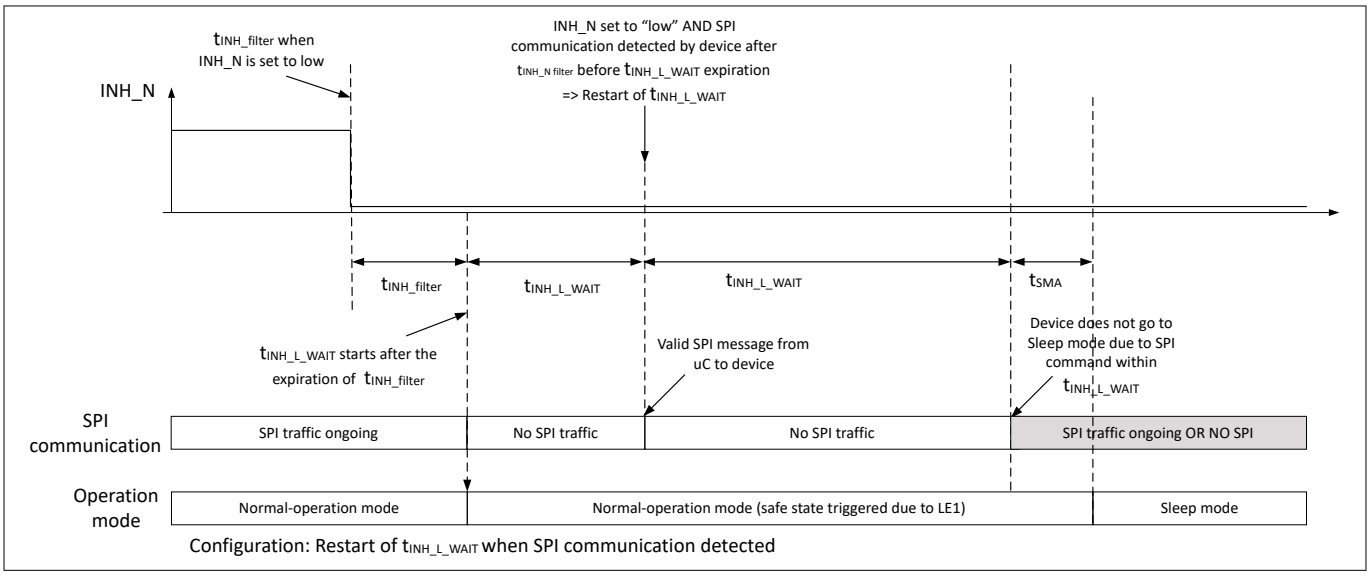

Figure 4 Canceled power-down due to SPI communication with restart of $t_{INH_L_WAIT}$

The device offers a configuration possibility to select if $t_{INH_L_WAIT}$ is restarted or not restarted after an SPI command while INH_N pin is "low" by control bit INH_L_CFG in SPI register CONFIG_SECURED:

- INH_L_CFG = "0": $t_{INH_L_WAIT}$ time is not restarted after an SPI command while INHN is low and current $t_{INH_L_WAIT}$ not expired (default)
- INH_L_CFG = "1": $t_{INH_L_WAIT}$ time is restarted after an SPI command while INHN is low and current $t_{INH_L_WAIT}$ not expired

1.1.2 Power-up mode

Once INH_N input pin is set to "high" by the microcontroller for t > t_{core_up}, then the mode of operation can be selected by SPI command by the microcontroller. When power-up mode is entered from sleep mode, the POR bit in register SUP_STAT is set to "1" to indicate a power-on reset detection. The POR bit has to be cleared by SPI write command. The mode of operation is selectable by control bits MODE_CTRL in register PWR_MOD_CFG. The device is in power-up mode when INH_N is set to "high" and mode control bits are set MODE_CTRL = 10_B. Power-up mode is the configuration mode of the device where the protected registers can also be configured. In power-up mode, safe state is forced and the Gxx output stages are OFF (passive clamping active, Gxx-GND passive discharge enabled).

Only in power-up mode the microcontroller can access/write via SPI command the device configuration register CONFIG_SECURED. The CONFIG_SECURED register is read-only in normal operation mode.

The default device configuration at power-up, after internal power on reset is released, is as follows:

- Internal digital core active
- Watchdog function disabled (WD_EN = 0)
- Charge pump disabled (CP_EN = 0)
- Current sense amplifier disabled (CSAx_EN = 0)
- Monitoring and diagnostics functions active
- Gate drivers OFF (Gxx-Sxx passive clamping active and Gxx-GND passive discharge enabled)
- The device is forced internally in safe state until transition to normal mode is performed
- ERR_N active "low"

The device changes mode of operation from normal mode to power-up mode if one of the actions below is executed:

- SPI write command for mode change is sent (set MODE_CTRL = 10_B)
- SPI write command to trigger clear configuration by CLR_CONFIG bit (reset to default setting of non-protected registers)

1.1.2.1 First SDO frame response

In sleep mode, if INH_N is set to "high" the device powers-up within t_{core_up} and SPI communication is possible. All registers are reset to default values.

The first SDO frame is the answer to the address sent by the microcontroller through the SDI frame in case SPI IFR is available.

In order to allow SPI communication between the microcontroller and the device:

- A correct and valid SDI frame has to be received by the device (no SPI error detected)
- A valid SDO frame with correct CRC8 has to be received by the microcontroller

***Note**:* *An invalid address in an SDI frame, will result in standard SDO answer from the device see "SPI error detection" in datasheet:*

- *Associated status bit is set*
- *The device sends data bits 0x00 in SDO frame*

1.1.2.2 Incorrect SPI command for mode change

In case an incorrect SPI SDI mode change command is sent by the microcontroller to the device, then:

- No mode change is triggered and the device remains in current mode of operation
- SPI SDI frame is ignored

- LFOK bit set to "0" in the next SDO response frame
- OFC bit set to "1"

1.1.3 Normal operation mode

The device is in normal operation mode when INH_N is set to "high", and mode control bits are set to MODE_CTRL = 01_B. Normal operation mode is the active mode of the device in which the output stages of the device can be controlled by PWM pattern of the microcontroller.

The device is set from power-up mode to normal operation mode, if a valid SPI write command to set MODE_CTRL = 01_B, provided that:

- $t_{core\text{-}up}$ has elapsed
- At least one correct SPI SDI frame command was received by the device. Correct SPI SDI frame must not lead to any of the following SPI failures: OFC, LFOK, CRC_FAIL, SPI_IA
- VSCP, VIO within the functional range
- Bit VIO_CFG in register CONFIG_SECURED has a valid configuration

***Note**:* *It is essential that the microcontroller writes a valid configuration setting into the register bit VIO_CFG in register CONFIG_SECURED before requesting a mode change from power-up mode to normal operation mode. In case one of the bit fields has no valid configuration, the device will ignore the SPI request to go to normal operation mode and stay in power-up mode.*

1.1.4 Power-up and power-down sequence

The figure below shows a power-up and power-down sequence example:

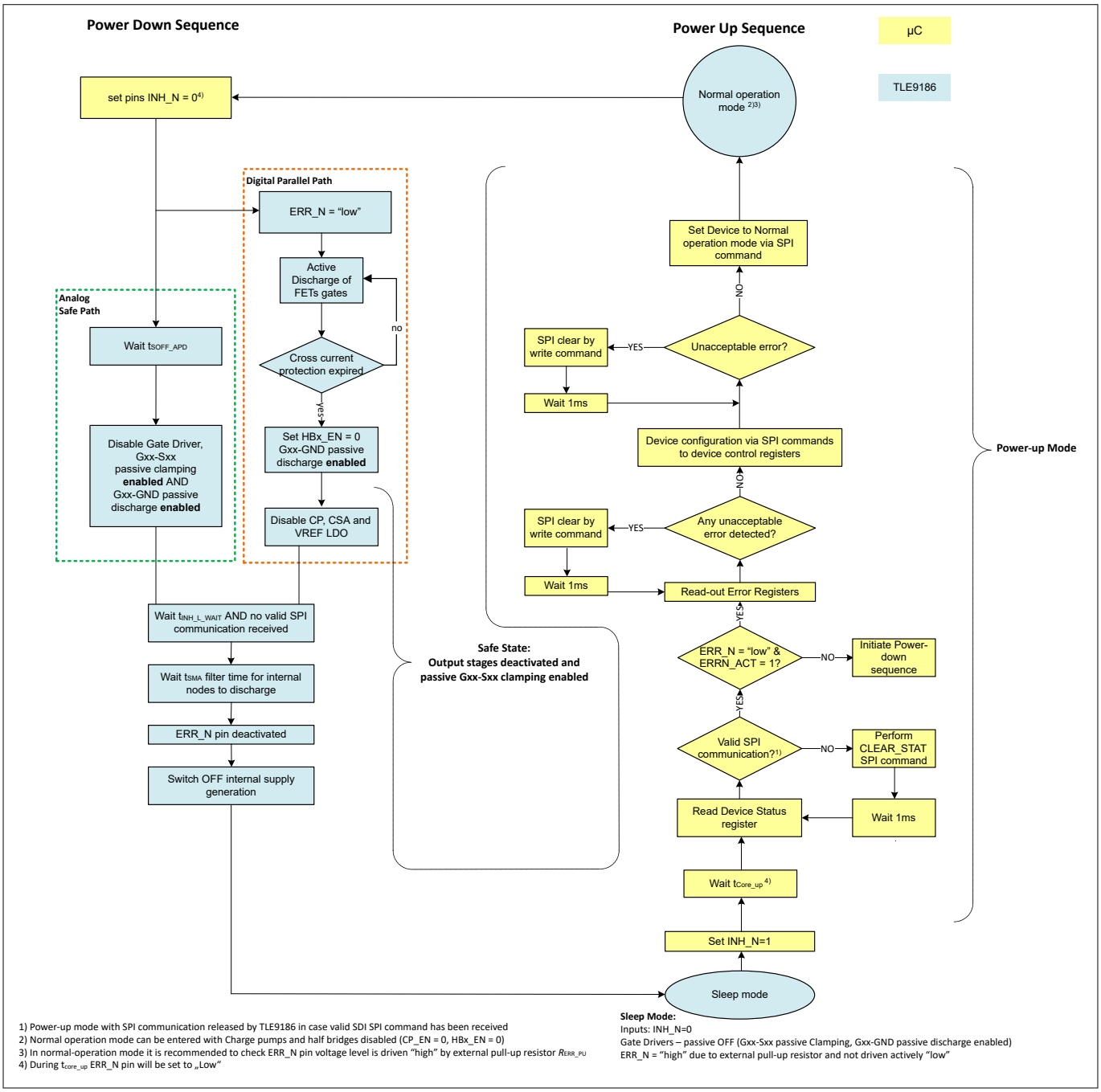

Figure 5 Power-up and power-down sequence

1.1.4.1 Guidance for unacceptable error detection

Any error reported by the device, preventing the device to go to normal operation mode OR causing safe state entry and preventing to toggle the Gxx output pins is considered as unacceptable error/failure detection. Assessment if an error detection is an unacceptable error depends on:

- Application use case
- Enabled and used functions of the device (for example: current sense amplifier, window watchdog)
- Device failure configuration

Therefore, the assessment of which error detection is an unacceptable error detection is the users responsibility. The list below provides guidance and recommendations on which errors are considered as an unacceptable error:

- Internal regulator overvoltage detection (REG_OV status bit) – not recommended to enter normal operation mode
- OTP error detection (OTP_ERR status bit) – not recommended to not enter normal operation mode
- VSCP undervoltage shutdown detection (VSCP_UV_SD status bit)
- VSCP overvoltage shutdown detection (VSCP_OV_SD status bit)
- Charge pump undervoltage detection (VCPH_UV status bit) in case charge pump enabled by SPI command (CP_EN = "1")
- In case CSA function used in application: current sense amplifier internal supply undervoltage detection (CSA_SUP_UV status bit)
- In case ERR_N pin used in application: ERR_N pin short to supply detection (ERRN_SHORT status bit), ERR_N pin cannot be used as error indication path towards microcontroller
- Thermal shutdown events (TSD_IC status bit, TSD_CP status bit)
- Latent fault detection (LAT_FAULT status bit set to "1"): latent fault detection in safety barrier - not recommended to enter normal operation mode
- In case VDH connected to motor bridge supply: VDH undervoltage detection (VDH_UV status bit set) – drain-source overvoltage on high-side MOSFET cannot be detected reliably
- VIO supply error detection (VIO_UV status bit AND VIO_OV status bit)
- SOFF_GDRV bit set to "0" in power-up mode: indication that at least one Gxx output stage is not correctly turned OFF – not recommended to enter normal operation mode

In case unacceptable error detection cannot be cleared by SPI clear by write command it is highly recommended to force safe state entry or to go to sleep mode.

1.2 Power supply (additional information)

This chapter provides additional information about the device charge pump power supply, which is described in the datasheet.

The charge pump requires external components and is the supply for floating high-side and low-side drivers in the gate driver unit. The charge pump external required components depend on the use case which is selected. The efficiency of the charge pump directly depends on the selected external components, especially on the forward voltage drop of the selected diode. The lower the forward voltage drop, the more efficient the charge pump works and as well the charge pump operation at low VSCP supply conditions is improved. For both use cases a series resistor and buffer capacitor is needed at the VSCP pin.

In case the charge pump external components are populated for a two stage charge pump, the CP_CFG needs to be set to "0".

In case the charge pump external components are populated for a three stage charge pump, the CP_CFG needs to be set to "1".

Table 2 Charge pump external components for use case

Use case	External components	Charge pump configuration (CP_CFG)	Comments
Typical use case: Two-stage charge pump configuration	Three external diodes and three external capacitors. Diode type BAV99, BAS16.	CP_CFG = 0_B	Used for functional range VSCP > 8 V. Charge pump current capability I_{VCPH} < 9 mA (6 x 60 nC @ 20 kHz)
Low VSCP supply use case: Three-stage charge pump configuration	Four external diode and four external capacitors. Diode type BAT54.	CP_CFG = 1_B	Used for extended functional range VSCP > 4.5 V. Charge pump current capability I_{VCPH} < 4.8 mA (6 x 40 nC @ 20 kHz). Recommended to set charge pump undervoltage to lower threshold (CP_UV_TH = "1")

In case the driver has to work in low VSCP supply voltages down to 4.5V, an additional diode and switching capacitor has to be added. In this option, the output current capability of the charge pump is reduced by approx. factor of two.

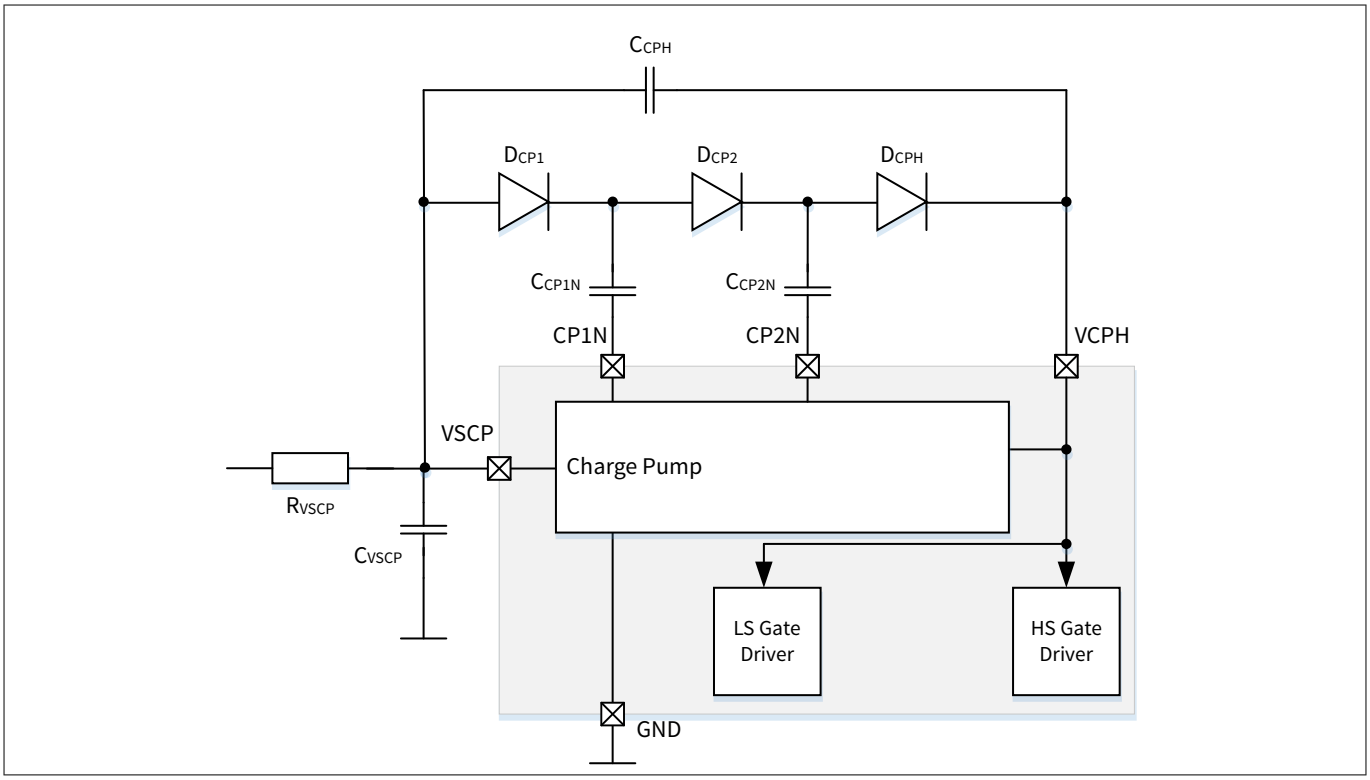

Figure 6 Charge pump external components: typical use case (CP_CFG = 0)

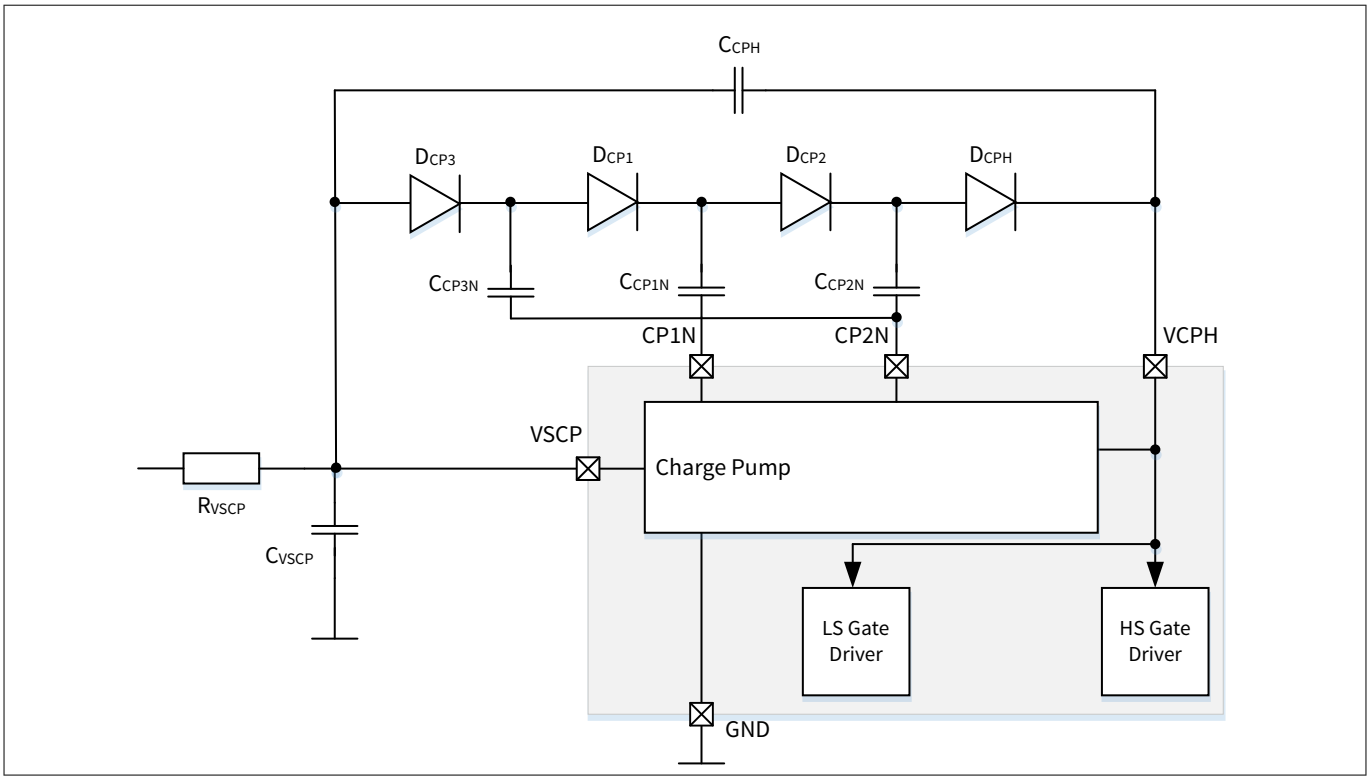

Figure 7 Charge pump external components: low VSCP supply use case (CP_CFG = 1)

Once the charge pump is enabled by SPI command (CP_EN = "1"), the charge pump requires t_{ON_VCPH} to ramp up, see figure below.

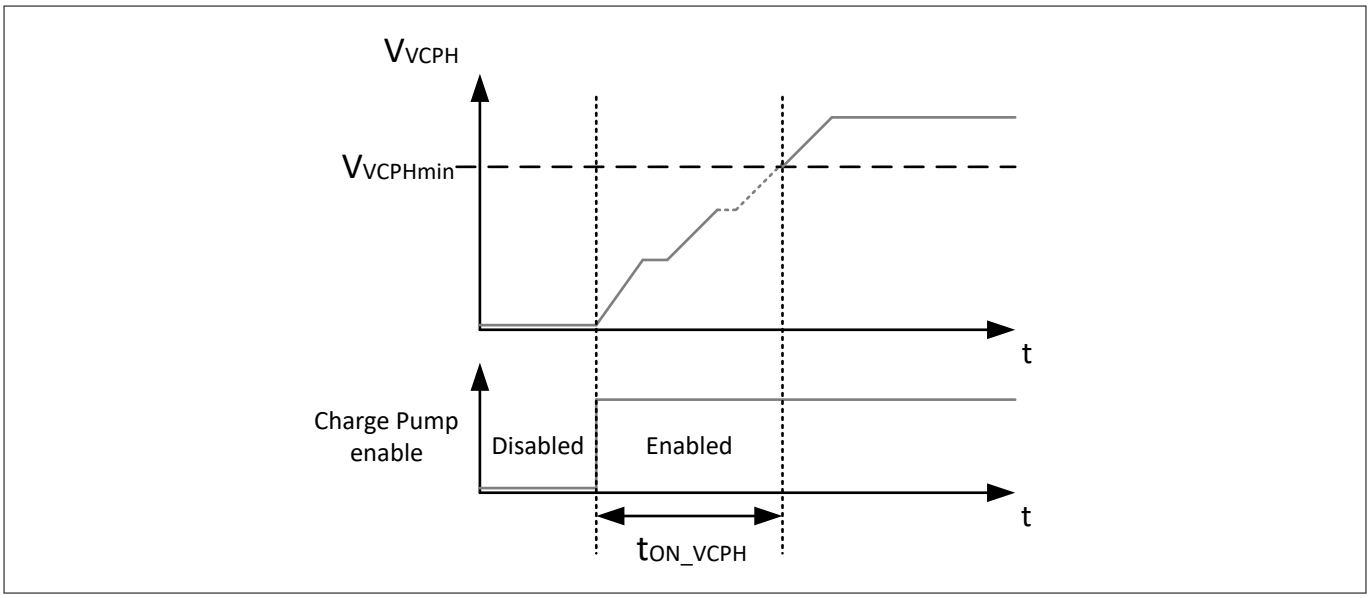

Figure 8 Timing diagram power-up charge pump

The maximum total gate charge for this device is limited by the charge pump current capability. In the datasheet, parameter P_GEN_12_10 specifies the current consumption of the IC when operating it with the total gate charge of a MOSFET in a typical application use case.

The current for parameter P_GEN_12_10 of the datasheet is calculated by I_{VCPH} = number of switching MOSFETs × f_{PWM} × Q_g = 6 × 20 kHz × 60 nC = 7.2 mA + additional external circuity supplied by charge pump (1 mA).

1.2.1 Charge pump frequency modulation feature

The device has a charge pump clock spreading feature, which has been implemented to improve the overall EMC performance of the device and to reduce EME spikes. A modulation of the charge pump frequency can be activated to reduce the peak emission. The modulation frequency is set by the control bits CP_FMOD in the GEN_CFG1 register. Following options are available:

- CP_FMOD: 00_B – no frequency modulation
- CP_FMOD: 01_B – modulation frequency 15.6 kHz
- CP_FMOD: 10_B – modulation frequency 31.2 kHz
- CP_FMOD: 11_B – modulation frequency 62.5 kHz

1.2.2 Charge pump operation modes

The charge pump module of the device is only supplied by VSCP pin. The charge pump changes its mode of operation depending on the VSCP supply condition. The table below shows the different operation modes of charge pump (for CP_MODE = 11_B).

Table 3 Charge pump mode (valid for CP_CFG = 0)

Charge pump mode (valid for CP_CFG = 0)	VSCP range	Related status bit
Double stage charge pump	$V_{VSCP} < V_{VSCP_HV}$	VSCP_H = 1
Single stage charge pump	$V_{VSCP_HV} < V_{VSCP}$	VSCP_H =0

Table 4 Charge pump mode (valid for CP_CFG = 1)

Charge pump mode (valid for CP_CFG = 1)	VSCP range	Related status bit
Triple stage charge pump	$V_{VSCP} < V_{VSCP_LV}$	VSCP_L = 1, VSCP_H = 1
Double stage charge pump	$V_{VSCP_LV} < V_{VSCP} < V_{VSCP_HV}$	VSCP_L = 0, VSCP_H = 1
Single stage charge pump	$V_{VSCP_HV} < V_{VSCP}$	VSCP_L = 0, VSCP_H = 0

The status bits VSCP_L and VSCP_H in register 0x25 (SUP_STAT) only reflect the current mode of operation of the charge pump (for CP_MODE = 11_B). No failure reaction is triggered by status bits VSCP_L and VSCP_H.

1.3 Gate driver (additional information)

This chapter provides additional information about the device gate driver output stages, which are described in the datasheet.

The device integrates six floating gate drivers capable of controlling a wide range of N-channel MOSFETs. These are configured as three high-side and three low-side drivers, forming a 3-phase inverter for controlling a BLDC motor. The output stages Gxx are deactivated by default in power-up mode and can be activated in normal operation mode.

The device offers the possibility to map PWM together. Either the GHx and GLx output stages of each phase are controlled separately by corresponding IHx_N and ILx input pins OR IHx_N input pins are deactivated and ILx input pins are used for corresponding half-bridge HBx control (one PWM input per half-bridge). With this feature the PWM input pins needed from microcontroller can be reduced by half. The control bit to enable this feature is SPI bit PWM_MAP in SPI register CONFIG_SECURED. In case PWM_MAP bit is set to "1":

- The ILx is propagated to both HSx and LSx of the corresponding half-bridge

- AND IPV_CCP failure reaction is deactivated (status bit not set, failure reaction not triggered)
- AND PWM alternation check is deactivated (PWM_CHCK)

A MOSFET turn-on request is defined as:

- HS turn-on request:
  - in case PWM_MAP = "0": when synchronized IHx_N high-low transition detected
  - in case PMW_MAP ="1": when synchronized ILx high-low transition detected
- LS turn-on request:
  - when synchronized ILx low-high transition detected

In normal operation mode, depending on bits HBx_EN, CP_EN, each high-side and low-side MOSFET can be:

- Kept off with the passive discharge (CP_EN = "0")
- Kept off actively (CP_EN = "1", HBx_EN = "1")
- Activated, and following PWM input pattern, applied by the microcontroller at the IHx_N and ILx pins (CP_EN = "1", HBx_EN = "1")

In normal operation mode the output stages can be activated. By default, the output stages are deactivated in normal operation mode. To activate the output stages, bits HBx_EN have to be set to "1" in register GEN_CFG1. Each HBx_EN bit enables/disables one half-bridge (refer to the table below).

Table 5 Enable output stages in normal operation mode

HB1_EN	HB2_EN	HB3_EN	GH1/GL1	GH2/GL2	GH3/GL3
0	0	0	Disabled	Disabled	Disabled
0	0	1	Disabled	Disabled	Follow PWM input Note
0	1	0	Disabled	Follow PWM input Note	Disabled
0	1	1	Disabled	Follow PWM input Note	Follow PWM input Note
1	0	0	Follow PWM input Note	Disabled	Disabled
1	0	1	Follow PWM input Note	Disabled	Follow PWM input Note
1	1	0	Follow PWM input Note	Follow PWM input Note	Disabled
1	1	1	Follow PWM input Note	Follow PWM input Note	Follow PWM input Note

***Note**: Provided no failure detected OR INH_N "low" pulse AND charge pump enabled (CP_EN control bit = "1").*

1.3.1 Active MOSFET and freewheeling MOSFET

The active MOSFET is the MOSFET that controls the slew rate at the motor phase. The freewheeling (FW) MOSFET is the MOSFET that does not control the slew rate at the motor phase. The device detects which MOSFET of a half-bridge is active and freewheeling MOSFET by the fast comparator thresholds V_{SHH} and V_{SHL}. The threshold of the comparators is configurable in register GEN_CFG2 by bits FAST_CMP_TH. The figure below shows the detection of active and freewheeling MOSFETs.

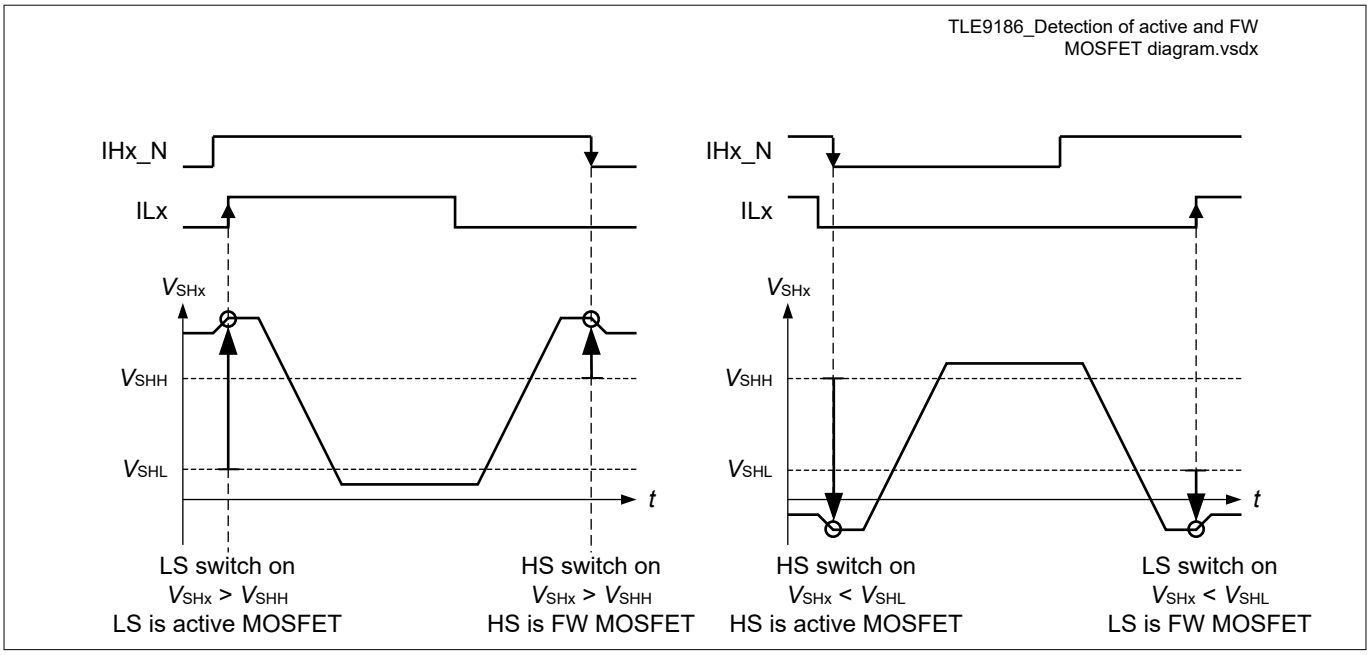

Figure 9 Detection of active and freewheeling MOSFET

The detection of active and freewheeling MOSFETs depends on the SHx voltage at the motor phase. The SHx motor phase voltage depends on the direction of the freewheeling current flowing through the MOSFETs. The figure below illustrates the mechanism.

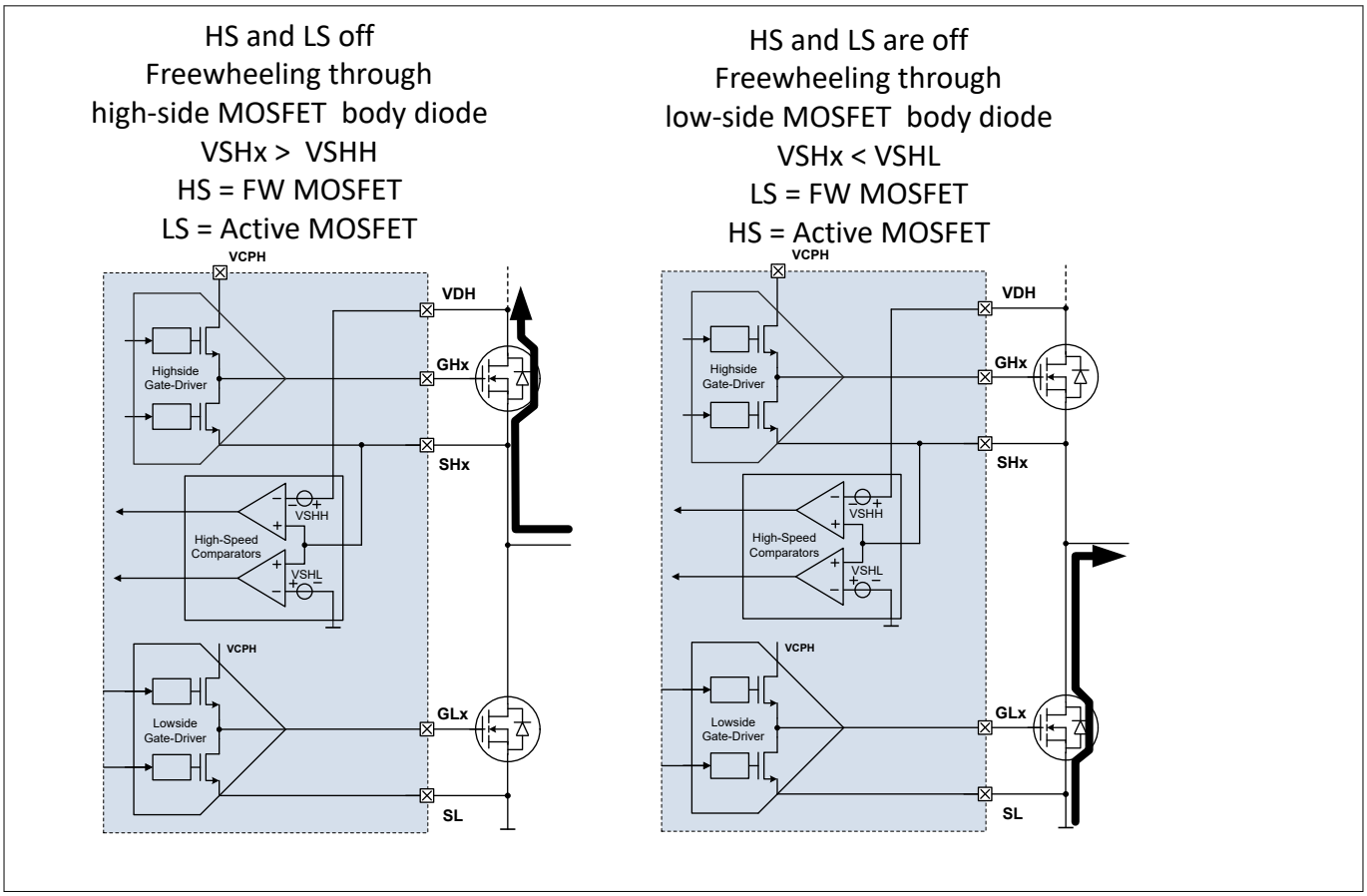

Figure 10 Detection of active and freewheeling MOSFETs depending on motor current - principle

- If the high-side *x* MOSFET is intended to be switched on and $V_{SHx} > V_{SHH}$, this high-side MOSFET is determined as freewheeling MOSFET
- If the low-side *x* MOSFET is intended to be switched on and $V_{SHx} < V_{SHL}$, this low-side MOSFET is determined as freewheeling MOSFET
- If $V_{SHL} < V_{SHx} < V_{SHH}$: no clear distinction between the freewheeling MOSFET and the active MOSFET. The next MOSFET to be turned on is turned on as if it was the active MOSFET

1.3.2 Gate current sequencer: turn ON and turn OFF of active MOSFET

This chapter provides additional information about current settings and timings for active turn ON and turn OFF of an GHx output stage.

Depending on the configuration of bit GDRV_CFG in register CONFIG_SECURED two different gate current sequencer schemes can be selected:

- GDRV_CFG = 0_B: time programmable referenced gate current sequencer (see Time programmable referenced gate current sequencer)
- GDRV_CFG = 1_B: fast comparator referenced gate current sequencer (see Fast comparator referenced gate current sequencer)

Table 6 Settings

Bit field	SPI register	Related electrical parameter	Comment
GDRV_CFG	CONFIG_SECURED	N/A	Configuration for gate sequencer scheme
GDRV_RNG	CONFIG_SECURED	N/A	Selection of gate current range for all gate currents
FW_CFG	CONFIG_SECURED	N/A	Selection of free-wheeling turn ON/OFF behavior see Freewheeling MOSFET
OFF_CFG	CONFIG_SECURED	N/A	Configuration of switch OFF behavior in case of detected faults leading to gate driver OFF (LE1, LE2) see Failure reaction: latched error (LE1 and LE2)
ION_HS_BNK, ION_LS_BNK	ION_HS1, ION_LS1	N/A	Turn ON bank configuration for HS and LS output stages
IOFF_HS_BNK, IOFF_LS_BNK	IOFF_HS1, IOFF_LS1	N/A	Turn OFF bank configuration for HS and LS output stages
I1ON_xx	I1ON_HS1, I1ON_LS1, I1ON_HS2, I1ON_LS2, I1ON_HS3, I1ON_LS3	I_{1ON}	Pre-charge current I_{1ON} applied during pre-charge phase
I2ON_xx	I2ON_HS1, I2ON_LS1, I2ON_HS2, I2ON_LS2, I2ON_HS3, I2ON_LS3	I_{2ON}	Charge current I_{2ON} applied during dV/dt phase

(table continues...)

Table 6 (continued) Settings

Bit field	SPI register	Related electrical parameter	Comment
ION	ON_IOFF_DIDT	I_{xON}	Charge current I_{ON} applied during di/dt phase
I3ON_HS	I3ON	I_{3ON}	Charge current applied during post-charge phase for HSx
I3ON_LS	I3ON	I_{3ON}	Charge current applied during post-charge phase for LSx
I1OFF_xx	I1OFF_HS1, I1OFF_LS1, I1OFF_HS2, I1OFF_LS2, I1OFF_HS3, I1OFF_LS3	I_{1OFF}	Pre-discharge current I_{1OFF} applied during pre-discharge phase
I2OFF_xx	I2OFF_HS1, I2OFF_LS1, I2OFF_HS2, I2OFF_LS2, I2OFF_HS3, I2OFF_LS3	I_{2OFF}	Discharge current I_{2OFF} applied during dV/dt phase
IOFF	ION_IOFF_DIDT	I_{xOFF}	Discharge current I_{ON} applied during di/dt phase
IDCHG_ST	GDRV_CFG3	I_{DCHG_ST}	Discharge current for safe state entry
IFW	GDRV_CFG3	I_{FW}	Freewheeling current
IHOLD	GDRV_CFG3	I_{HOLD}	Holding current. IHOLD accuracy follows the same specification as other gate current configurations. Please refer to parameter P_GDRV_02_15, P_GDRV_02_16, P_GDRV_02_17
ION_TR	GDRV_CFG3	N/A	Current step width configuration for ramping phase (applied only for fast comparator referenced gate sequencer)

The time the current is applied for each phase of the gate sequencer scheme is configurable. For the time programmable sequencer scheme, ten timings are required to be configured. For the fast comparator reference sequencer scheme, four timings are required to be configured in **bold**:

Table 7 Settings

Bit field	SPI register	Comment
T1ON_HS	TON_HS	Configurable pre-charge time for HSx
T2ON_HS	TON_HS	Configurable charge time for HSx (only applicable in case time programmable reference gate current sequencer scheme enabled)
T1ON_LS	TON_LS	Configurable pre-charge time for LSx

(table continues...)

Table 7 (continued) Settings

Bit field	SPI register	Comment
T2ON_LS	TON_LS	Configurable charge time for LSx (only applicable in case time programmable reference gate current sequencer scheme enabled)
T1OFF_HS	TOFF_HS	Configurable pre-discharge time for HSx
T2OFF_HS	TOFF_HS	Configurable discharge time for HSx (only applicable in case time programmable reference gate current sequencer scheme enabled)
T1OFF_LS	TOFF_LS	Configurable pre-discharge time for LSx
T2OFF_LS	TOFF_LS	Configurable discharge time for LSx (only applicable in case time programmable reference gate current sequencer scheme enabled)
T3OFF_HS	T3OFF	Configurable post-discharge time for HSx (only applicable in case time programmable reference gate current sequencer scheme enabled)
T3OFF_LS	T3OFF	Configurable post-discharge time for HSx (only applicable in case time programmable reference gate current sequencer scheme enabled)

Cross current protection time is configurable for active and freewheeling MOSFET separately by bit fields TCCP and TCCP_FW in register GDRV_CFG1. Additionally the applied clock ratio of the cross current protection time is configurable by bit TCCP_CFG in order to reduce the TCCP by a factor of two. By offering this option the user can select the cross current protection time in the range from either nominal 240 ns up to 3840 ns OR nominal 120 ns up to 1920 ns.

1.3.2.1 Time programmable referenced gate current sequencer

The time programmable referenced gate current sequencer GDRV_CFG = 0_B uses strictly SPI register based timings and gate current settings.

For the diagrams shown in this chapter, it is assumed the freewheeling MOSFET does not use the precharge/predischarge current (FW_CFG = "0").

1.3.2.1.1 Turn ON of a Gxx output stage

The turn-on of the active high-side MOSFET is done in four steps:

1. **Cross-current protection phase:** the cross-current protection time t_{CCP_FW} starts when the low-side control signal turns "OFF". During t_{FW}, the low-side MOSFET is turned OFF with the current I_{FW}, while the high-side is kept OFF with holding current I_{HOLD}. After t_{FW} expires the low-side MOSFET is kept switched off by the current I_{HOLD}. During the following three phases the low-side MOSFET is kept off with current I_{DCHG_MAX}
2. **Pre-charge phase:** only after t_{CCP_FW} is expired, the high-side control signal is acknowledged to be set to "ON". As soon as the high-side control "ON" signal is acknowledged, the gate of the high-side MOSFET is charged with the current I_{1ON_HS} for a duration of t_{1ON_HS}. When t_{1ON_HS} expires the charge phase is entered
3. **Charge phase (dI/dt phase and dV/dt phase):** in charge phase the charge current is set to the current I_{2ON_HSx}. The gate of the high-side MOSFET will be charged with I_{2ON_HSx} until t_{2ON_HS} expires. After that the post-charge phase is entered
4. **Post-charge phase**: in the post charge phase the charge current is set to I_{3ON_HS} until the end of t_{VDS_BLK} + t_{VDS_FILT}. After t_{VDS_BLK} + t_{VDS_FILT} expires, the current will be switched to the holding current I_{HOLD}

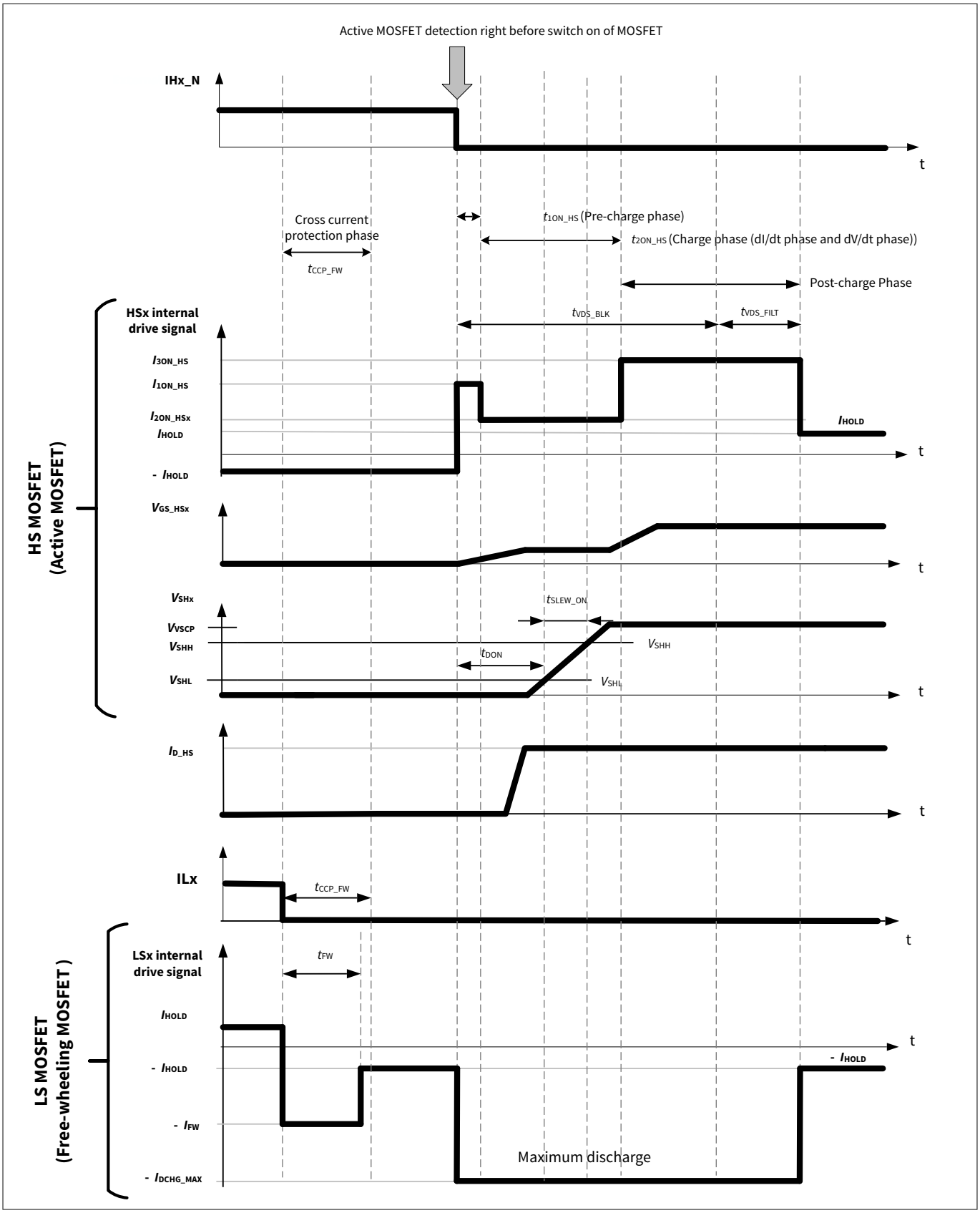

Figure 11 Turn-on of active HS MOSFET and turn-off of FW LS MOSFET

The turn-on of the active low-side MOSFET is done in four steps:

1. **Cross-current protection phase:** the cross-current protection time t_{CCP_FW} starts when the high-side control signal turns "OFF". During t_{FW}, the high-side MOSFET is turned off with the current I_{FW} while the low-side is kept off with holding current I_{HOLD}. After t_{FW} expires the high-side MOSFET is kept switched off by the current I_{HOLD}. During the following three phases the high-side MOSFET is kept off with current I_{DCHG_MAX}
2. **Pre-charge phase:** only after t_{CCP_FW} is expired, the low-side control signal is acknowledged to be set to "ON". As soon as the low-side control "ON" signal is acknowledged the gate of the low-side MOSFET is charged with the current I_{1ON_LS} for a duration of t_{1ON_LS}. When t_{1ON_LS} expires the charge phase is entered
3. **Charge phase (dI/dt phase and dV/dt phase):** in charge phase the charge current is set to the current I_{2ON_LSx}. The gate of the low-side MOSFET will be charged with I_{2ON_LSx} until t_{2ON_LS} expires. After that the post-charge phase is entered
4. **Post-charge phase**: in the post charge phase the charge current is set to I_{3ON_LS} until the end of t_{VDS_BLK} + t_{VDS_FILT}. After t_{VDS_BLK} + t_{VDS_FILT} expires, the current will be switched to the holding current I_{HOLD}

***Note**:*

- *t_{CCP_FW} is the minimum gate driver controlled cross current protection time. The microcontroller may extend the effective cross current protection time by providing an appropriate control signal pattern*
- *In case the active MOSFET is turned ON during t_{CCP_FW} (after t_{CCP_FW} but before t_{FW} expired), the freewheeling MOSFET switches directly from freewheeling discharge current I_{FW} to maximum discharge current I_{DCHG_MAX}*
- *In case of very low duty cycle (ON time < t_{DONx} + t_{SLEW_ONx}) the sequence is exited and t_{CCP} is started with turn off of the LSx or HSx output stage*

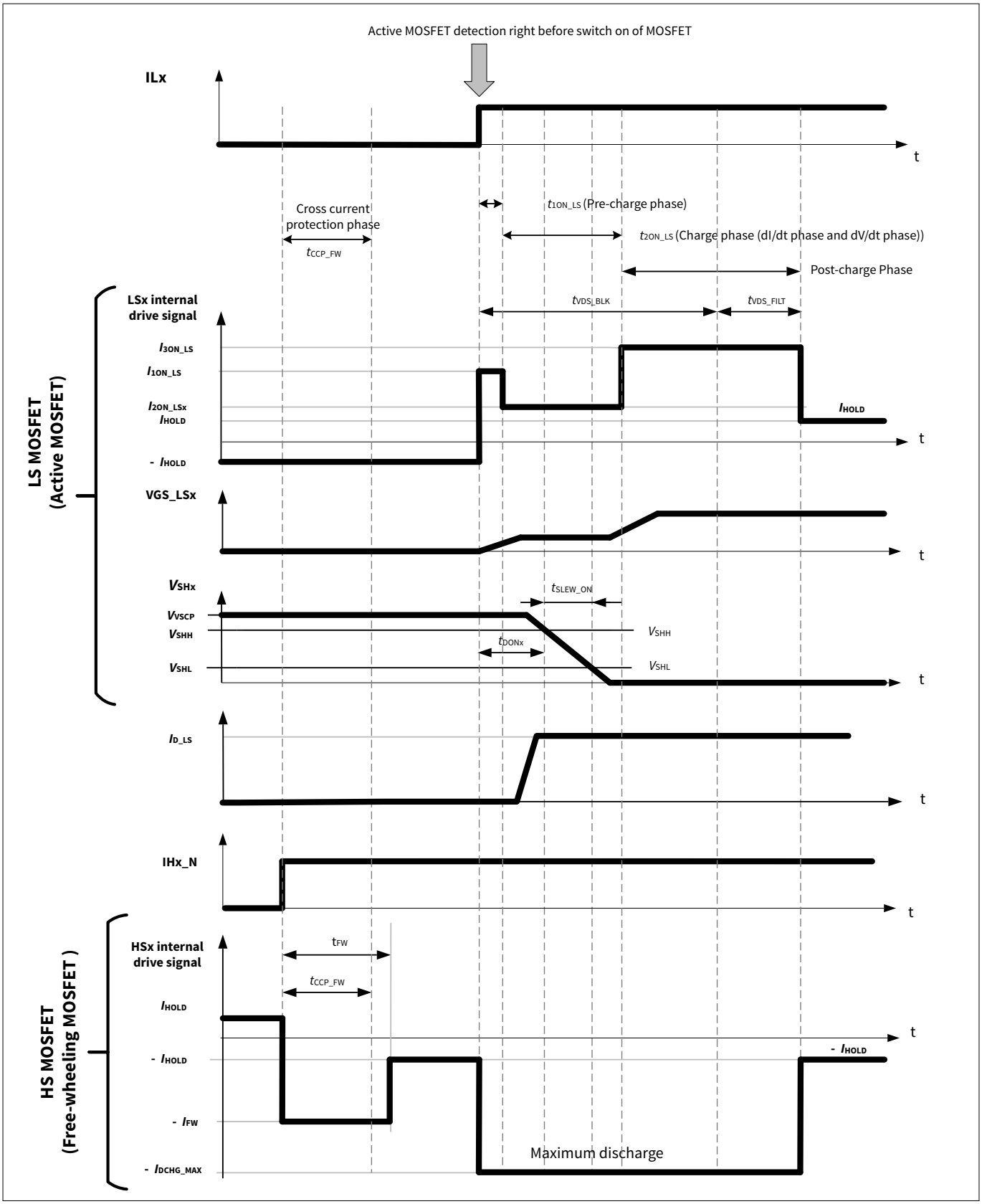

Figure 12 Turn-on of active LS MOSFET and turn-off of FW HS MOSFET

1.3.2.1.2 Turn OFF of a Gxx output stage

The turn-off of the active high-side MOSFET is done in four steps:

1. **Pre-discharge phase:** in case the high-side control signal is set to "OFF", the gate of the high-side MOSFET is discharged with the current I_{1OFF_HS} for a duration of t_{1OFF_HS}. After t_{1OFF_HS} expires the discharge phase is entered
2. **Discharge phase (dV/dt phase and dI/dt phase):** the gate of the high-side MOSFET is discharged with the current I_{2OFF_HSx} for a duration of t_{2OFF_HS}. After t_{2OFF_HS} expires the post discharge phase is entered
3. **Post discharge phase:** the gate of the high-side MOSFET is discharged with the current I_{DCHG_MAX} for a duration of t_{3OFF_HS}. After t_{3OFF_HS} expires the holding phase is entered
4. **Holding phase:** In the holding phase the high-side MOSFET will be kept off with the holding current I_{HOLD}. Only after t_{CCP} the low-side control signal is acknowledged to be set to "ON". As soon as the low-side control "ON" signal is acknowledged the low-side MOSFET is switched on with the current I_{FW} for the time t_{FW} . During the time t_{FW} the holding current for the high-side MOSFET is increased to I_{DCHG_MAX}. After I_{FW} is expired, both MOSFETs are kept in their current state by I_{HOLD}

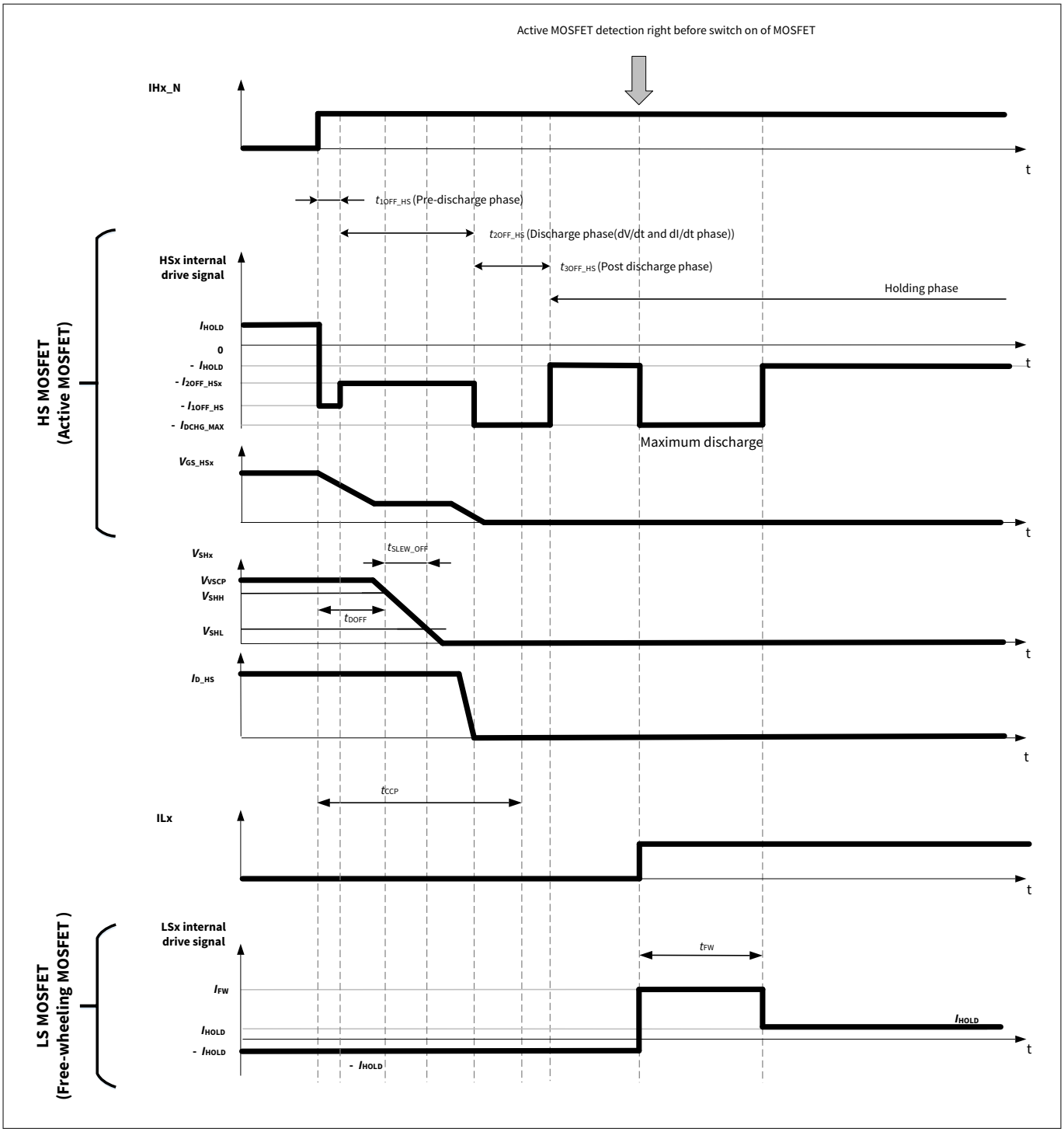

Figure 13 Turn-off of active HS MOSFET and turn-on of FW LS MOSFET

The turn-off of the active low-side MOSFET is done in four steps:

1. **Pre-discharge phase:** in case the low-side control signal is set to "OFF", the gate of the low-side MOSFET is discharged with the current I_{1OFF_LS} for a duration of t_{1OFF_LS}. After t_{1OFF_LS} expires the discharge phase is entered
2. **Discharge phase (dV/dt phase and dI/dt phase):** the gate of the low-side MOSFET is discharged with the current I_{2OFF_LSx} for a duration of t_{2OFF_LS}. After t_{2OFF_LS} expires the post discharge phase is entered

3. **Post discharge phase:** the gate of the low-side MOSFET is discharged with the current I_{DCHG_MAX} for a duration of t_{3OFF_LS}. After t_{3OFF_LS} expires the holding phase is entered
4. **Holding phase:** In the holding phase the low-side MOSFET will be kept off with the holding current I_{HOLD}. Only after t_{CCP} the high-side control signal is acknowledged to be set to "ON". As soon as the high-side control "ON" signal is acknowledged the high-side MOSFET is switched on with the current I_{FW} for the time t_{FW}. During the time t_{FW} the holding current for the low-side MOSFET is increased to I_{DCHG_MAX}. After t_{FW} is expired, both MOSFETs are kept in their current state by I_{HOLD}

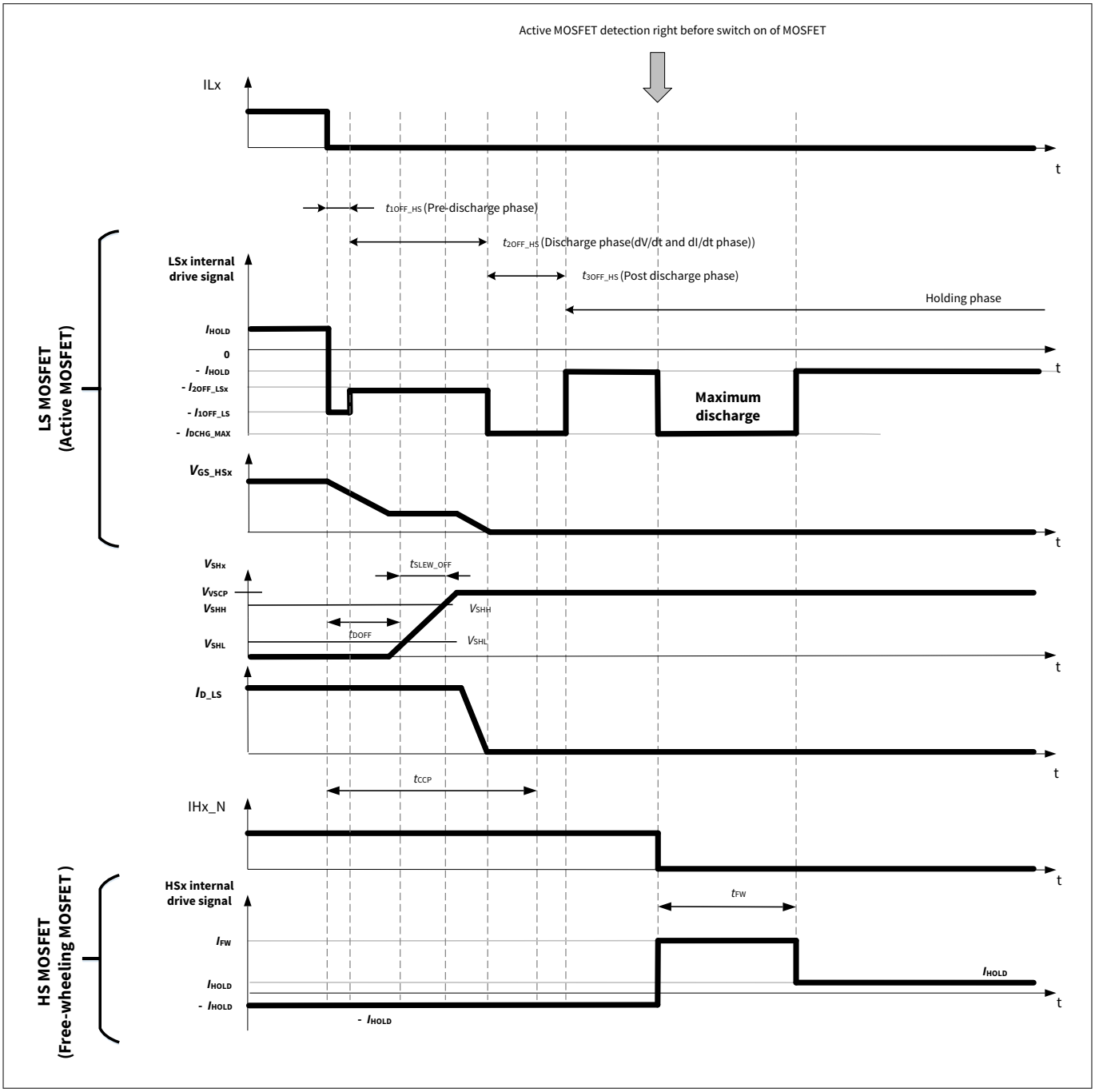

Figure 14 Turn-off of active LS MOSFET and turn-on of FW HS MOSFET

1.3.2.2 Fast comparator referenced gate current sequencer

The fast comparator referenced gate current sequencer GDRV_CFG = 1_B uses only SPI register based precharge and predischarge timings and gate current settings. The switching between the different gate current sequencer phases depends on the fast comparator thresholds V_{SHH} and V_{SHL}.

For the diagrams shown in this chapter, it is assumed the freewheeling MOSFET uses precharge/predischarge phase (t1ON_HS, t1ON_LS, t1OFF_HS, t1OFF_LS) (FW_CFG = "1").

1.3.2.2.1 Turn ON of a Gxx output stage

The turn-on of the active high-side MOSFET is done in five steps:

1. **Cross-current protection phase:** the cross-current protection time t_{CCP_FW} starts when the low-side control signal turns "OFF". During t_{CCP_FW}, the low-side MOSFET is turned off with pre-discharge current I_{1OFF_LS} for t_{1OFF_LS}. When t_{1OFF_LS} expires the freewheeling MOSFET is discharged with I_{FW} until $t_{OFF_timeout}$ has elapsed. After $t_{OFF_timeout}$ the freewheeling MOSFET is kept in its current state by I_{HOLD}. The low-side is kept off with current I_{DCHG_MAX} until $t_{VDS_BLK} + t_{VDS_FILT}$ has elapsed
2. **Pre-charge phase:** only after t_{CCP_FW} is expired, the high-side control signal is acknowledged to be set to "ON". As soon as the high-side control "ON" signal is acknowledged, the gate of the high-side MOSFET is charged with the current I_{1ON_HS} for a duration of t_{1ON_HS}. When I_{1ON_HS} expires it enters the Miller-charge phase. In case during pre-charge phase the phase voltage V_{SHx} reaches V_{SHL} before t_{1ON_HS}, then the current is changed from I_{1ON_HS}directly to I_{2ON_HSx}
3. **Charge phase (dI/dt phase):** the charge current is decreased from I_{1ON_HS} down to the charge current I_{ON}. The gate of the high-side MOSFET will be charged with I_{ON} until the phase voltage V_{SHx} reaches V_{SHL}
4. **Miller-charge phase (dV/dt phase):** the charge current is changed from I_{ON} to the Miller-charge current I_{2ON_HSx}. The gate of the high-side MOSFET will be charged with I_{2ON_HSx} until the phase voltage V_{SHx} reaches V_{SHH}
5. **Post-charge phase**: after the charge phase, the charge current is ramped up to post-charge current I_{3ON_HS} until the end of $t_{VDS_BLK} + t_{VDS_FILT}$. The ramping behavior is configurable by bit field ION_TR in SPI register GDRV_CFG3. If the device is still in the ramping phase of the post-charge current when $t_{VDS_BLK} + t_{VDS_FILT}$ has expired, the ramp phase will be extended until it reaches I_{3ON_HS}. After $t_{VDS_BLK} + t_{VDS_FILT}$ expires and I_{3ON_HS} is reached, the current will be switched to the holding current I_{HOLD}

***Note**:*

- *t_{CCP_FW} is the minimum gate driver controlled cross current protection time. The microcontroller may extend the effective cross current protection time by providing an appropriate control signal pattern*
- *In case the active MOSFET is turned ON after t_{CCP_FW} but before $t_{OFF_timeout}$ expires, the freewheeling MOSFET switches directly from freewheeling discharge current I_{FW} to maximum discharge current I_{DCHG_MAX}*
- *In case of very low duty cycle (ON time < $t_{DONx} + t_{SLEW_ONx}$) the sequence is exited and t_{CCP} is started with turn off of the HSx output stage. Register values for $t_{DONx} + t_{SLEW_ONx}$ are only updated in case V_{SHx} reaches the corresponding V_{SHH} OR V_{SHL} threshold*

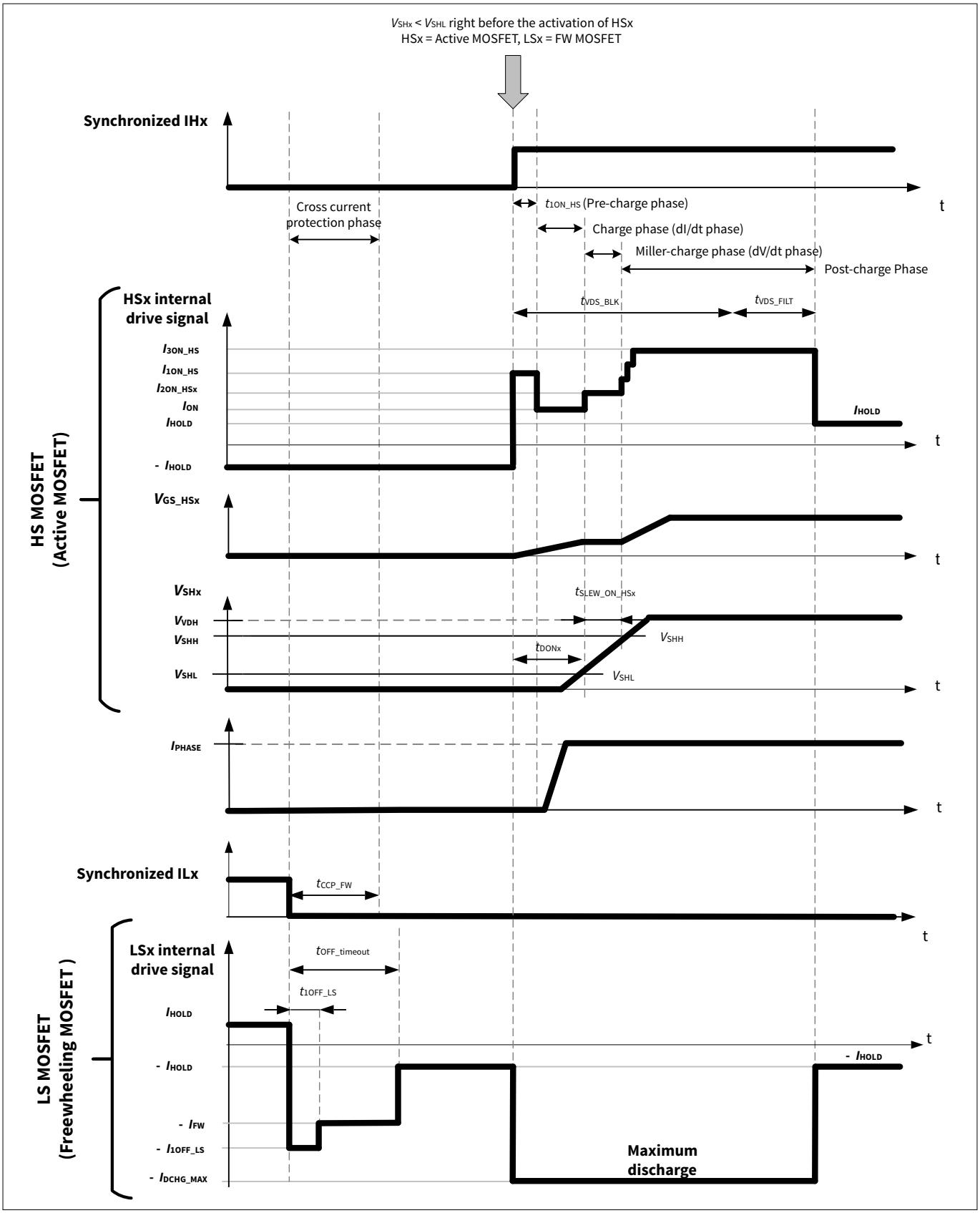

Figure 15 Turn-on of active HS MOSFET and turn-off of FW LS MOSFET

The turn-on of the active low-side MOSFET is done in five steps:

1. **Cross-current protection phase:** the cross-current protection time t_{CCP_FW} starts when the high-side control signal turns "OFF". During t_{CCP_FW}, the high-side MOSFET is turned off with pre-discharge current I_{1OFF_HS} for t_{1OFF_HS}. When t_{1OFF_HS} expires the freewheeling MOSFET is discharged with I_{FW} until $t_{OFF_timeout}$ has elapsed. After $t_{OFF_timeout}$ the freewheeling MOSFET is kept in its current state by I_{HOLD}. The high-side is kept off with current I_{DCHG_MAX} until $t_{VDS_BLK} + t_{VDS_FILT}$ has elapsed
2. **Pre-charge phase:** only after t_{CCP_FW} is expired, the low-side control signal is acknowledged to be set to "ON". As soon as the low-side control "ON" signal is acknowledged, the gate of the low-side MOSFET is charged with the current I_{1ON_LS} for a duration of t_{1ON_LS}. When t_{1ON_LS} expires it enters the Miller-charge phase. In case during pre-charge phase the phase voltage V_{SHx} reaches V_{SHH} before t_{1ON_LS}, then the current is changed from I_{1ON_LS} directly to I_{2ON_LSx}
3. **Charge phase (dI/dt phase):** the charge current is decreased from I_{1ON_LS} down to the charge current I_{ON}. The gate of the low-side MOSFET will be charged with I_{ON} until the phase voltage V_{SHx} reaches V_{SHH}
4. **Miller-charge phase (dV/dt phase):** the charge current is changed from I_{ON} to the Miller-charge current I_{2ON_LSx}. The gate of the low-side MOSFET will be charged with I_{2ON_LSx} until the phase voltage V_{SHx} reaches V_{SHL}
5. **Post-charge phase**: after the charge phase, the charge current is set to post-charge current I_{3ON_LS} until the end of $t_{VDS_BLK} + t_{VDS_FILT}$. If the device is still in the ramping phase of the post-charge current when $t_{VDS_BLK} + t_{VDS_FILT}$ has expired, the ramp phase will be extended until it reaches I_{3ON_LS}. After $t_{VDS_BLK} + t_{VDS_FILT}$ expires and I_{3ON_LS}. is reached, the current will be switched to the holding current I_{HOLD}

***Note**:*

- *t_{CCP_FW} is the minimum gate driver controlled cross current protection time. The microcontroller may extend the effective cross current protection time by providing an appropriate control signal pattern*
- *In case the active MOSFET is turned ON after t_{CCP_FW} but before $t_{OFF_timeout}$ expired, the freewheeling MOSFET switches directly from freewheeling discharge current I_{FW} to maximum discharge current I_{DCHG_MAX}*
- *In case of very low duty cycle (ON time < $t_{DONx} + t_{SLEW_ONx}$) the sequence is exited and t_{CCP} is started with turn off of the LSx output stage. Register values for t_{DONx} and t_{SLEW_ONx} are only updated in case V_{SHx} reaches the corresponding V_{SHH} OR V_{SHL} threshold*

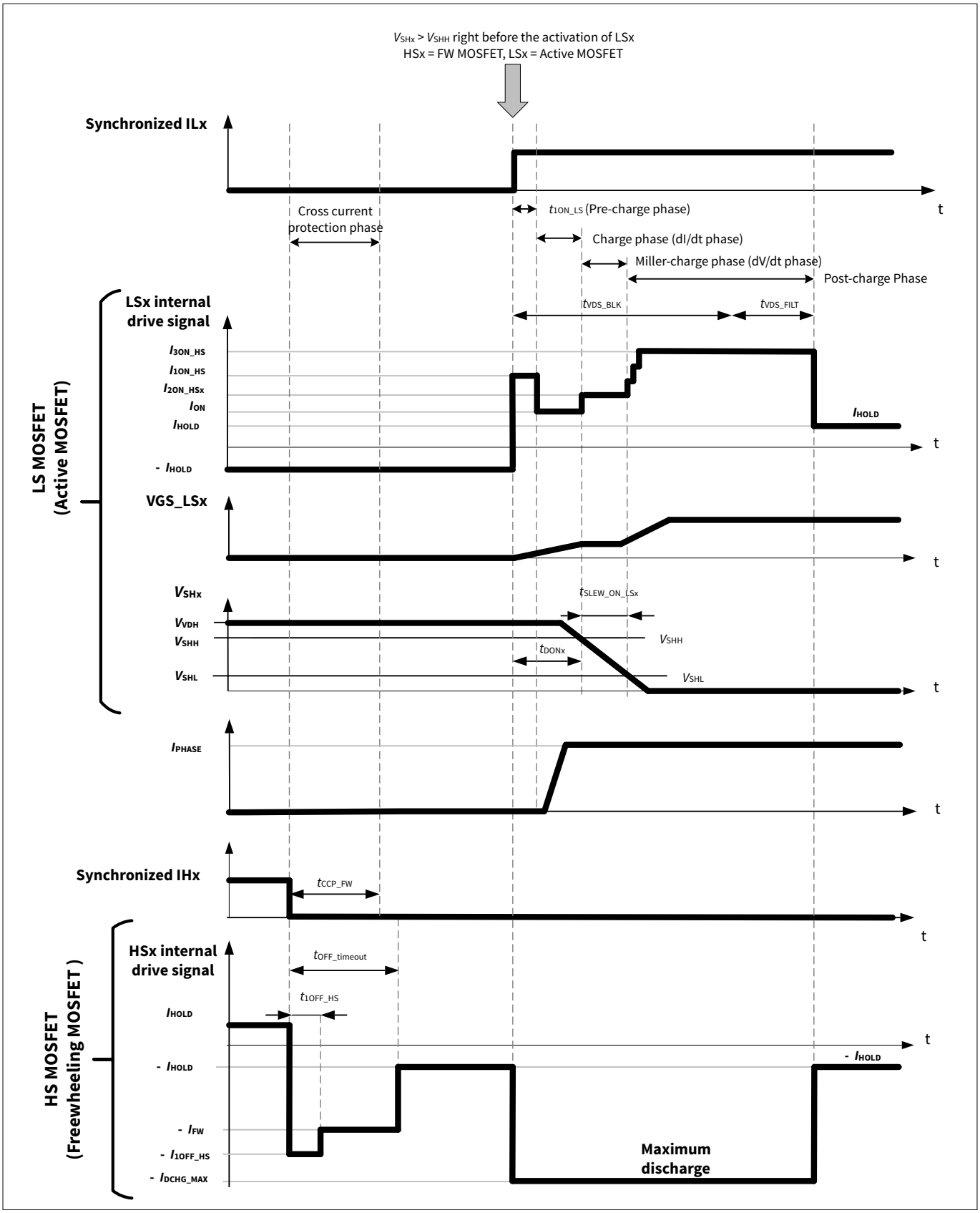

Figure 16 Turn-on of active LS MOSFET and turn-off of FW HS MOSFET

1.3.2.2.2 Turn OFF of a Gxx output stage

Cross-current protection time t_{CCP} represents the time after which the complementary MOSFET in the same half-bridge can be activated. Therefore, t_{CCP} is the minimum discharge time for the MOSFET. $t_{OFF_timeout}$ is the maximum time for discharge with discharge current I_{DCHG_MAX}. In case the microcontroller applies an external cross-current protection time, which is longer than the configured internal cross current protection time at the PWM input pins of the driver, the external cross current protection time is used.

The turn-off of the active HS MOSFET is done in five steps:

1. **Pre-discharge phase:** in case synchronized IHx is set to low, the gate of the high-side MOSFET is pre-discharged with the current I_{1OFF_HS} for a duration of t_{1OFF_HS}. After t_{1OFF_HS} time expires, the discharge current is changed to I_{2OFF_HSx}. In case during pre-discharge phase the phase voltage V_{SHx} reaches V_{SHH} before t_{1OFF_HS}, then the current is changed from I_{1OFF_HS} directly to I_{2OFF_HSx}
2. **Miller-discharge phase (dV/dt phase):** the gate of the high-side MOSFET is discharged with current I_{2OFF_HSx} until V_{SHx} reaches V_{SHL}. When V_{SHx} reaches V_{SHL} the post discharge phase is entered
3. **Discharge phase (dI/dt phase):** the discharge phase is part of the post discharge phase. When V_{SHx} reaches V_{SHL} the high-side MOSFET is discharged with I_{OFF} for the configured extension time t_{3OFF_HS}
4. **Post discharge phase:** once t_{3OFF_HS} expires the gate of the high-side MOSFET is discharged with the maximum discharge current I_{DCHG_MAX} until $t_{OFF_timeout}$ expires. After $t_{OFF_timeout}$ expires the holding phase is entered
5. **Holding phase:** after the $t_{OFF_timeout}$ expires the high-side MOSFET will be kept off with holding current I_{HOLD}

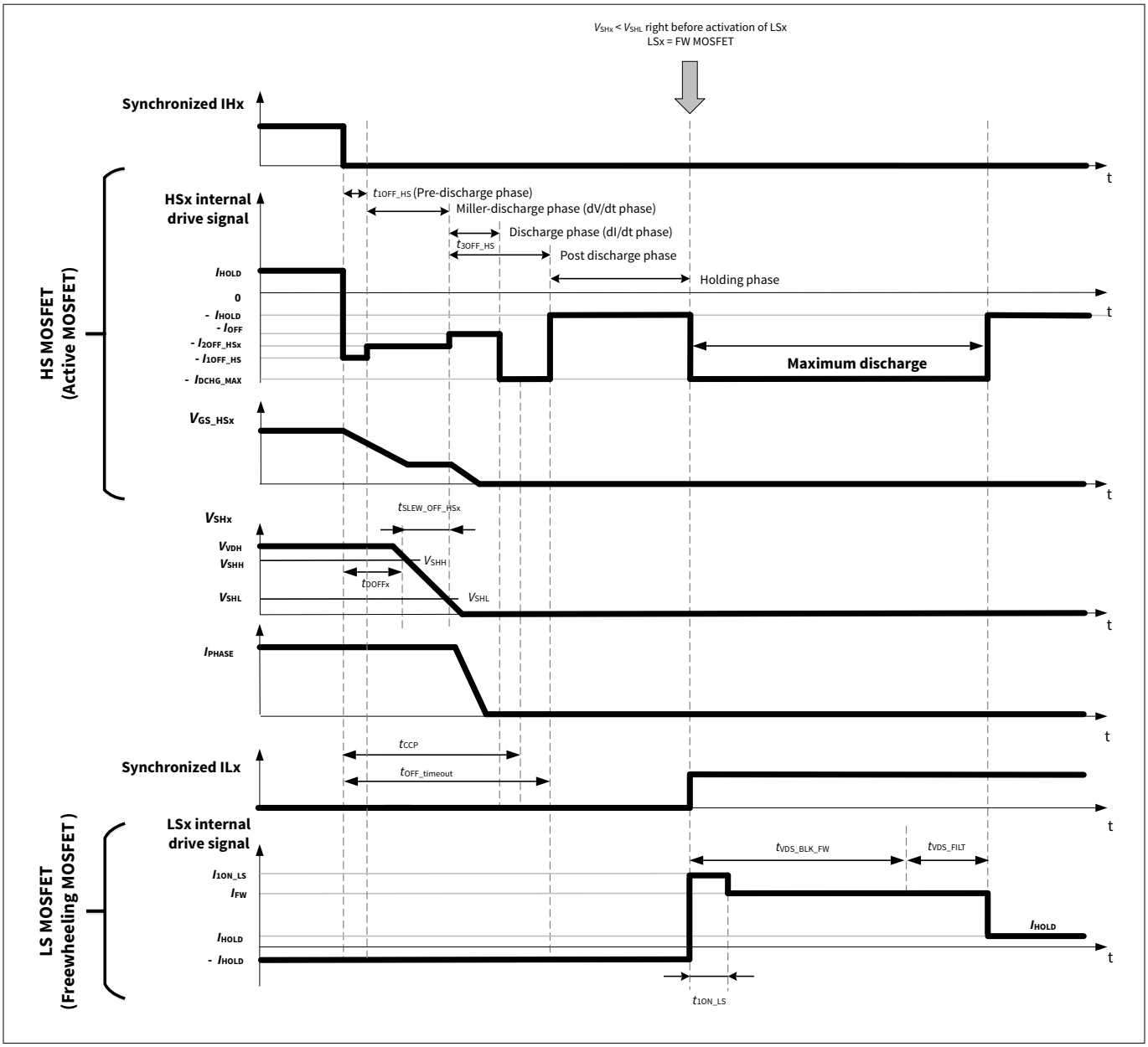

Figure 17 Turn-off of active HS MOSFET and turn-on of FW LS MOSFET

The turn-off of the active low-side MOSFET is done in five steps:

1. **Pre-discharge phase:** in case synchronized ILx is set to low, the gate of the high-side MOSFET is pre-discharged with the current I_{1OFF_LS} for a duration of t_{1OFF_LS}. After t_{1OFF_LS} time expires the discharge current is changed to I_{2OFF_LSx}. In case during pre-discharge phase the phase voltage V_{SHx} reaches V_{SHL} before t_{1OFF_LS}, then the current is changed from I_{1OFF_LS} directly to I_{2OFF_LSx}
2. **Miller-discharge phase (dV/dt phase):** the gate of the high-side MOSFET is discharged with current I_{2OFF_LSx} until V_{SHx} reaches V_{SHH}. When V_{SHx} reaches V_{SHH} the post discharge phase is entered
3. **Discharge phase (dI/dt phase):** the discharge phase is part of the post discharge phase. When V_{SHx} reaches V_{SHH} the low-side MOSFET is discharged with I_{OFF} for the configured extension time t_{3OFF_LS}
4. **Post discharge phase:** once t_{3OFF_LS} expires, the gate of the low-side MOSFET is discharged with the maximum discharge current I_{DCHG_MAX} until $t_{OFF_timeout}$ expires. After $t_{OFF_timeout}$ expires, the holding phase is entered
5. **Holding phase:** after the $t_{OFF_timeout}$ expires, the low-side MOSFET will be kept off with holding current I_{HOLD}

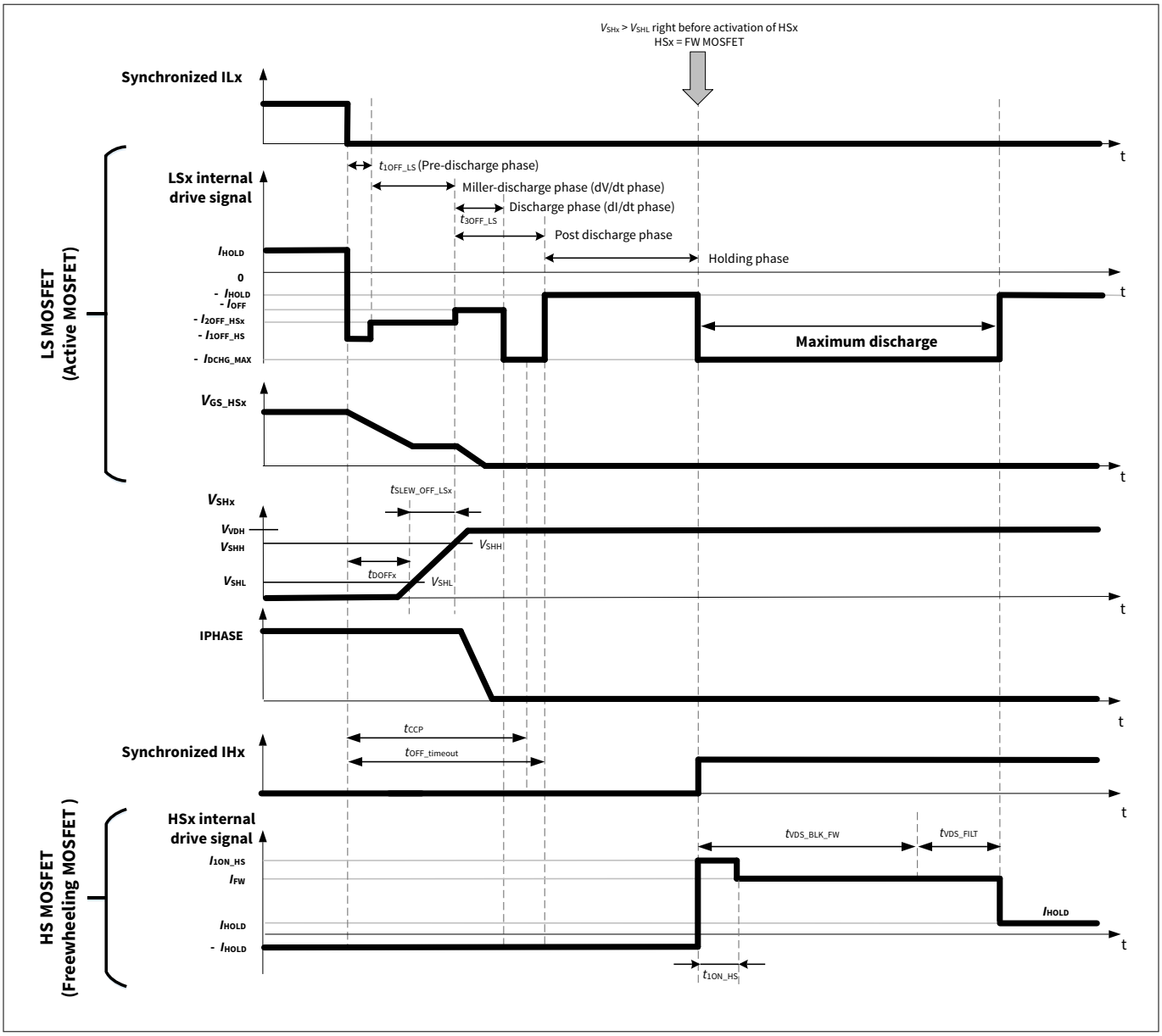

Figure 18 Turn-off of active LS MOSFET and turn-on of FW HS MOSFET

In the holding phase the active MOSFET will be kept off with the holding current I_{HOLD}. Only after t_{CCP} the control signal for the freewheeling MOSFET is acknowledged to be set to "ON". As soon as the freewheeling MOSFET control "ON" signal is acknowledged, the freewheeling MOSFET is switched on with the corresponding pre-charge current I_{1ON_HS} / I_{1ON_LS} for a duration of t_{1ON_HS} / t_{1ON_LS}. When t_{1ON_HS} / t_{1ON_LS} expires, the freewheeling MOSFET is charged with I_{FW} until $t_{VDS_BLK_FW}$ + t_{VDS_FILT} has elapsed. After $t_{VDS_BLK_FW}$ + t_{VDS_FILT} the freewheeling MOSFET is kept in its current state by I_{HOLD}.

1.3.3 Freewheeling MOSFET

As described in previous chapters, the device offers two different gate current sequencer schemes for the active MOSFET. For the passive freewheeling MOSFET, the device offers some configuration possibility as well, which changes the gate currents applied during turn ON and turn OFF of the freewheeling MOSFET. The behavior can be selected by control bit FW_CFG in SPI register CONFIG_SECURED:

- FW_CFG = "0" (default): freewheeling device does not use precharge/predischarge phase
- FW_CFG = "1": freewheeling device uses precharge/predischarge phase (t1ON_HS, t1ON_LS, t1OFF_HS,t1OFF_LS)

The figures below show the two possibilities of the freewheeling turn ON/OFF behavior.

Table 8 Freewheeling turn ON/OFF behavior

FW_CFG = "0"	FW_CFG = "1"
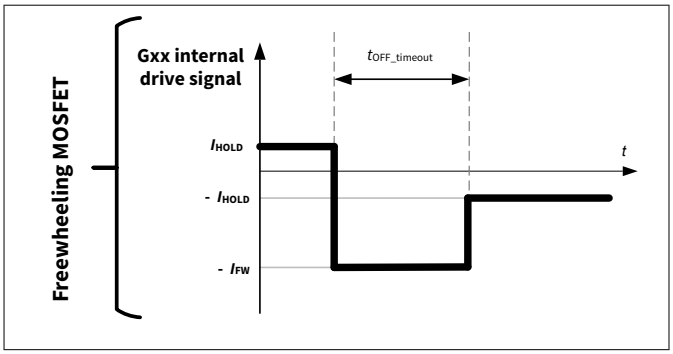	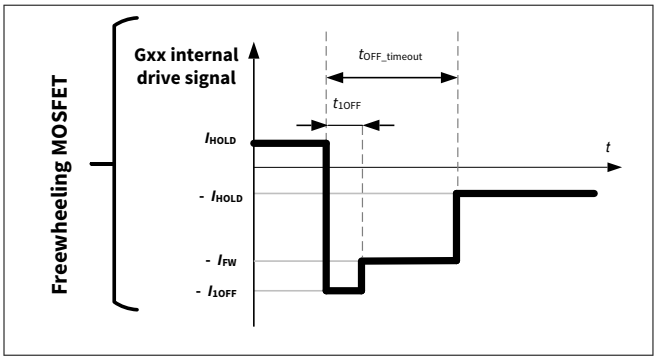
Figure 19 Turn OFF of FW MOSFET FW_CFG = "0"	**Figure 20 Turn OFF of FW MOSFET FW_CFG = "1"**
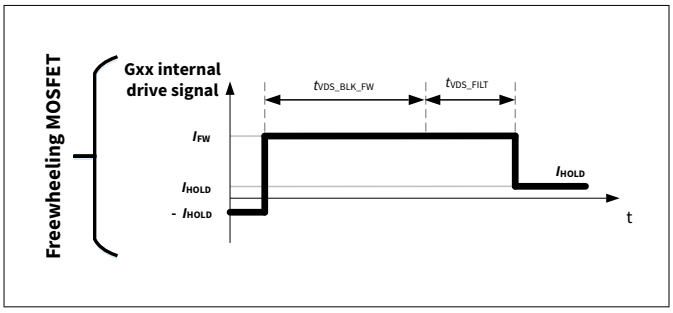	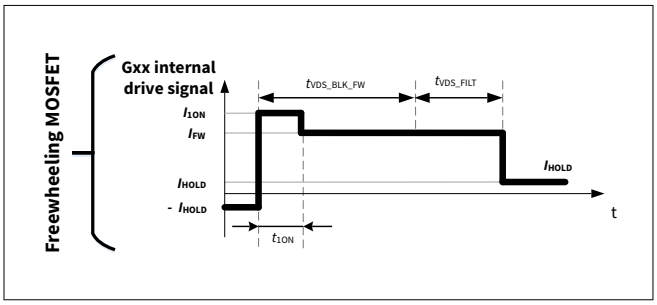
Figure 21 Turn ON of FW MOSFET FW_CFG = "0"	**Figure 22 Turn ON of FW MOSFET FW_CFG = "1"**

1.3.4 TDON, TDOFF and TSLEW_ON, TSLEW_OFF time measurements

All reported timings TDON_HS/LS, TDOFF_HS/LS, TSLEWON_HS/LS, and TSLEWOFF_HS/LS use the 37.5 MHz or 75 MHz clock (LSB step size) as configured by HBFREQ control bit.

LSB nominal 13.3 ns (1/75 MHz) if HBFREQ = 0

LSB nominal 26.6 ns (1/37.5 MHz) if HBFREQ = 1

Example: 75 MHz configured (HBFREQ = 0): TDOFF_HS2 0x16 → measured TDOFF time at HS2 is 22 * 1/75 MHz = 293 ns.

High-side MOSFET:

- Turn ON delay time of the high-side output stage t_{DON_HSx} is counted from the rising edge of the synchronized IHx until V_{SHx} reaches V_{SHL}
- Phase slew ON time of the high-side output stage $t_{SLEW_ON_HSx}$ is counted for V_{SHx} going from V_{SHL} to V_{SHH}
- If V_{SHx} does not reach V_{SHL} until t_{VDS_BLK} is elapsed, 0x7F and 0x00 will be saved in effective high-side MOSFET turn ON delay register and effective high-side MOSFET phase slew ON time register respectively

- If V_{SHx} has reached V_{SHH} when the rising edge of the synchronized IHx comes, 0x00 will be stored in both the effective high-side MOSFET turn ON delay register and the effective high-side MOSFET phase slew ON time register
- If V_{SHx} reaches V_{SHL} but does not reach V_{SHH} when t_{VDS_BLK} is elapsed, 0x7F will be saved in the effective high-side MOSFET phase slew ON time register
- Turn OFF delay time of the high side output stage t_{DOFF_HSx} is counted from the falling edge of the synchronized IHx until V_{SHx} reaches V_{SHL}
- Phase slew OFF time of the high-side output stage $t_{SLEW_OFF_HSx}$ is countedfor V_{SHx} going from V_{SHH} to V_{SHL}
- If V_{SHx} does not reach V_{SHL} until cross current protection time t_{CCP} is elapsed, 0x7F and 0x00 will be saved in effective high-side MOSFET turn OFF delay register and effective high-side MOSFET phase slew OFF time register respectively
- If V_{SHx} has reached V_{SHL} when the falling edge of the synchronized IHx comes, 0x00 will be stored in both the effective high-side MOSFET turn OFF delay register and the effective high-side MOSFET phase slew OFF time register
- If V_{SHx} reaches V_{SHH} but does not reach V_{SHL} when cross current protection time t_{CCP} is elapsed, 0x7F will be saved in the effective high-side MOSFET phase slew OFF time register

***Note**:*
- *If $V_{SHL} > V_{SHx} > V_{SHL}$ when the rising edge of the synchronized IHx comes, no effective turn ON delay time t_{DONx} time can be calculated, 0x00 will be written in the effective high-side MOSFET turn ON delay time and phase slew OFF registers - the internal calculation is discarded - the MOSFET is treated as an active MOSFET*
- *If IHx pulse is shorter than t_{VDS_BLK}/t_{CCP} but all timings were already calculated, the timing registers will be updated accordingly*

Low-side MOSFET:
- Turn ON delay time of the low-side output stage t_{DON_LSx} is counted from the rising edge of the synchronized ILx until V_{SHx} reaches V_{SHL}
- Phase slew ON time of the high-side output stage $t_{SLEW_ON_LSx}$ is counted for V_{SHx} going from V_{SHH} to V_{SHL}
- If V_{SHx} does not reach V_{SHL} until t_{VDS_BLK} is elapsed, 0x7F and 0x00 will be saved in effective low-side MOSFET turn ON delay register and effective low-side MOSFET phase slew ON time register respectively
- If V_{SHx} has reached V_{SHL} when the rising edge of the synchronized ILx comes, 0x00 will be stored in both the effective low-side MOSFET turn ON delay register and the effective low-side MOSFET phase slew ON time register
- If V_{SHx} reaches V_{SHH} but does not reach V_{SHL} when t_{VDS_BLK} is elapsed, 0x7F will be saved in the effective low-side MOSFET phase slew ON time register
- Turn OFF delay time of the low side output stage t_{DOFF_LSx} is counted from the falling edge of the synchronized ILx until V_{SHx} reaches V_{SHL}
- Phase slew OFF time of the low-side output stage $t_{SLEW_OFF_LSx}$ is counted for V_{SHx} going from V_{SHL} to V_{SHH}
- If V_{SHx} does not reach V_{SHL} until cross current protection time t_{CCP} is elapsed, and 0x7F and 0x00 will be saved in effective low-side MOSFET turn_off delay register and effective low-side MOSFET phase slew OFF time register respectively
- If V_{SHx} has reached V_{SHL} when the falling edge of the synchronized ILx comes, 0x00 will be stored in both the effective low-side MOSFET turn_off delay register and the effective low-side MOSFET SLEW_OFF time register
- If V_{SHx} reaches V_{SHL} but does not reach V_{SHH} when cross current protection time t_{CCP} is elapsed, 0x7F will be saved in the effective low-side MOSFET phase slew OFF time register

***Note**:*

- *If $V_{SHH} > V_{SHx} > V_{SHL}$ when the rising edge of the synchronized ILx comes then no effective turn ON delay time t_{DONx} can be calculated, 0x00 will be written in the effective low-side MOSFET turn ON delay time and phase slew OFF registers - the internal calculation is discarded and the MOSFET is treated as an active MOSFET*
- *If ILx pulse is shorter than t_{VDS_BLK}/t_{CCP} but all timings were already calculated, the timing registers will be updated accordingly*

1.4 Current sense amplifier (additional information)

This chapter provides additional information about the current sense amplifiers, which are described in the datasheet.

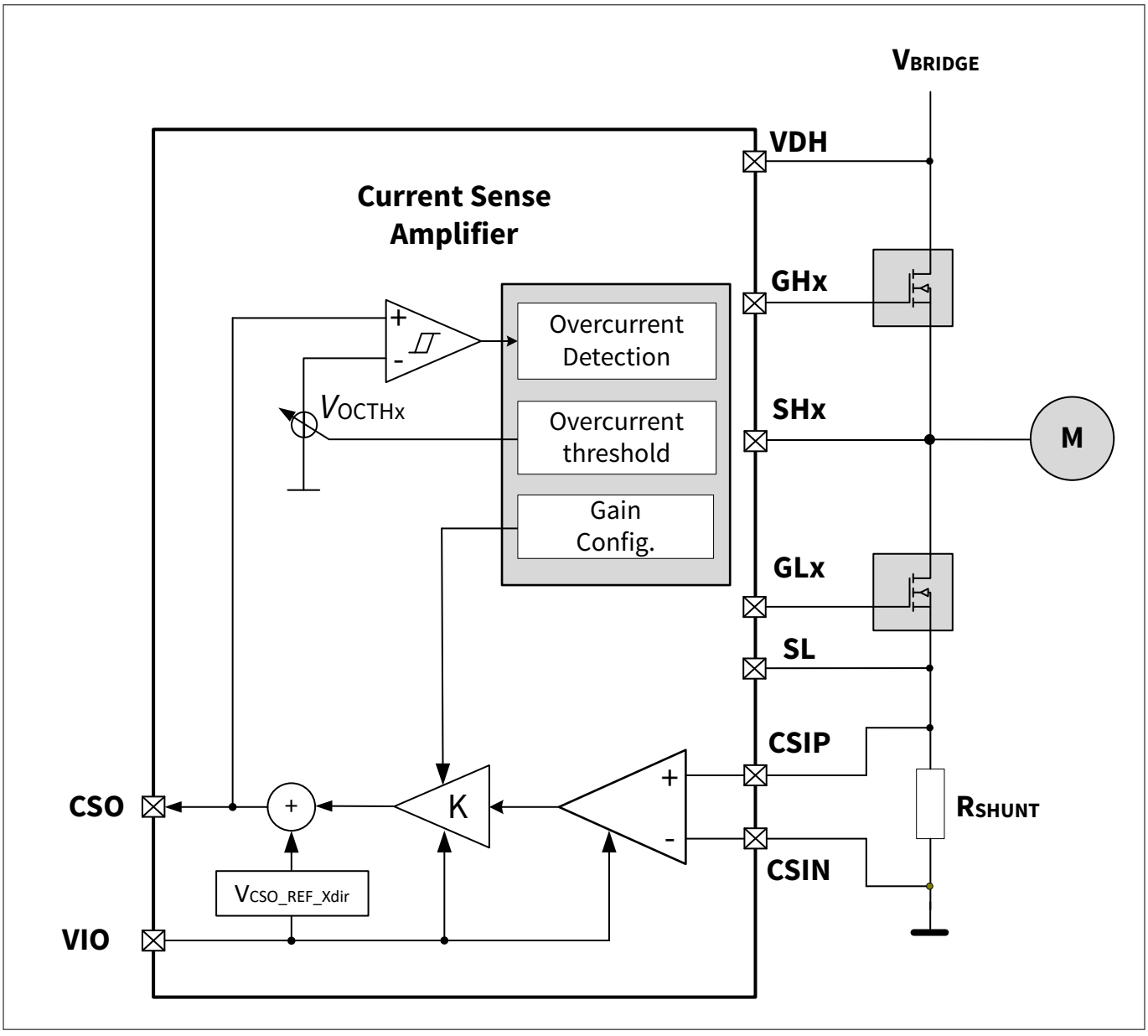

Figure 23 Simplified diagram: CSA module

The following table shows the possible configurations and their related configuration bits.

Table 9 Configuration options

Configuration option	Related SPI control bits	Related SPI status bit (diagnostics)
Gain settings for current sense amplifier	CSA_GAIN	
Uni- OR bi-directional CSA configuration	CSA_DIR	
Current sense amplifier capacitive load configuration	CSA_CLOAD	
Current sense amplifier gain test	CSA_GAIN_TST	
CSA overcurrent threshold	CSA_OC_TH	CSA_OC
CSA overcurrent filter time	CSA_TFOC	
VIO failure behavior for undervoltage and overvoltage detection	No configuration - fixed to LE1	VIO_UV, VIO_OV
PFB mapping on CSO	Configurable by CSO_MUX, refer to Phase feedback monitoring	PFBx

1.4.1 CSA gain settings

The gain of the current sense amplifier is configurable by configuration bit CSA_GAIN.

Table 10 CSA gain settings

Gain setting by bit CSA_GAIN	Description
000_B	Differential gain 6 V/V selected Note
001_B	Differential gain 8 V/V selectedNote
010_B	Differential gain 10 V/V selectedNote
011_B	Differential gain 15 V/V selectedNote
100_B	Differential gain 24 V/V selectedNote
101_B	Differential gain 40 V/V selectedNote

***Note**: Refer to the datasheet for latest nominal values and gain accuracy specification.*

1.4.2 CSA capacitance configuration

The device offers two configurable capacitance load ranges to adapt for the used output capacitance. Two capacitance load ranges are available, configurable by bit control bit CSA_CLOAD. The selection of the capacitance load range depends on the selected microcontroller and its current measurement (ADC) module.

- CSA_CLOAD = "1". Two external components required (C_{CSO1} & R_{CSO})
- CSA_CLOAD = "0". One external component required: C_{CSO2}. No output resistor R_{CSO} needed

Refer to External components for additional information.

1.5 SPI (additional information)

This chapter provides additional information about the serial peripheral interface (SPI), which is described in the datasheet.

When the device is power-up for the first time (INH_N set from "low" to "high"), the SPI frame format is in-frame response (IFR) by default. The SPI frame format can be changed to next-frame response (NFR) format by bits SPI_TYPE, and show the different types of SPI response frame formats. Each SPI command consists of one SDI and one SDO frame. Each SDI frame consists of an 8 bit address field, a 16 bit data field and an 8 bit CRC field. Each SDO frame consists of an 8 bit global status byte, a 16 bit data field and an 8 bit CRC8. Figure 26 shows the SDI and SDO frame content.

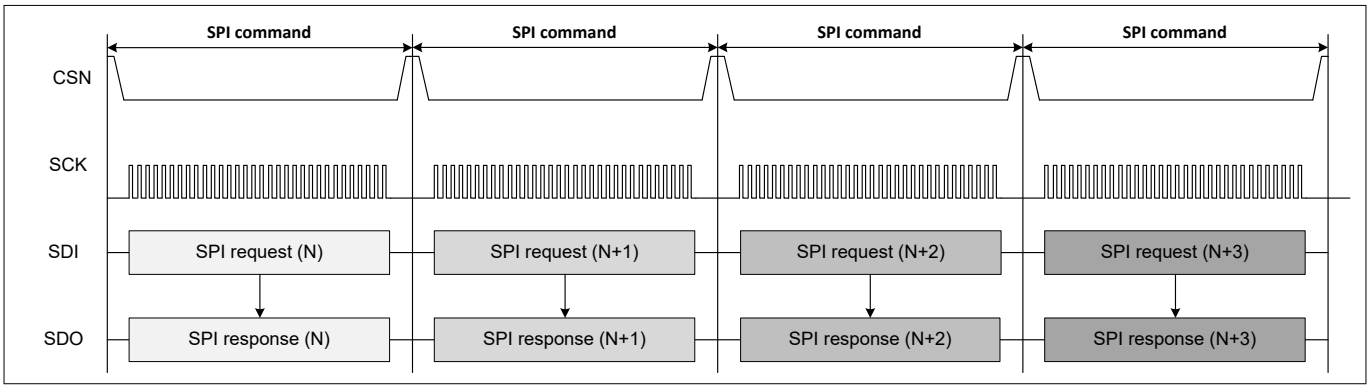

Figure 24 SPI commands with in-frame response format (IFR)

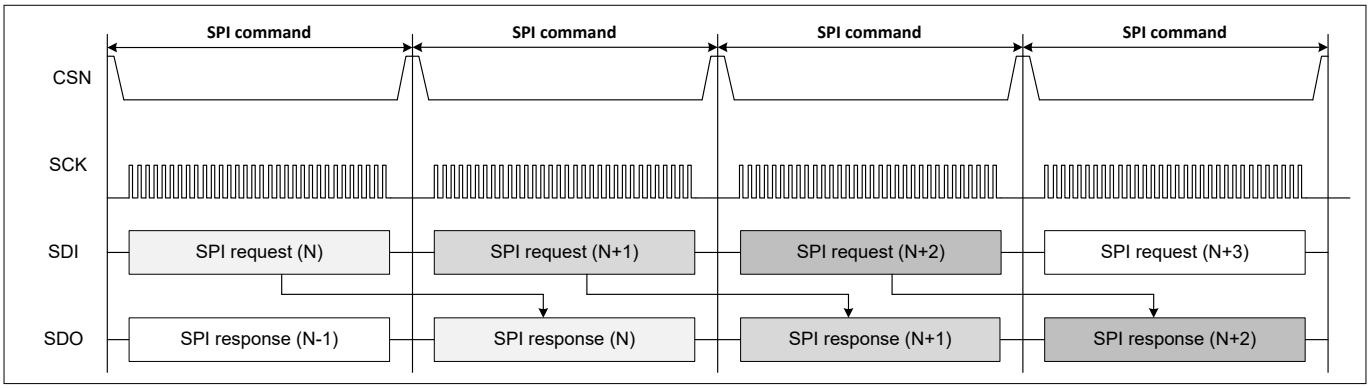

Figure 25 SPI commands with next-frame response format (NFR)

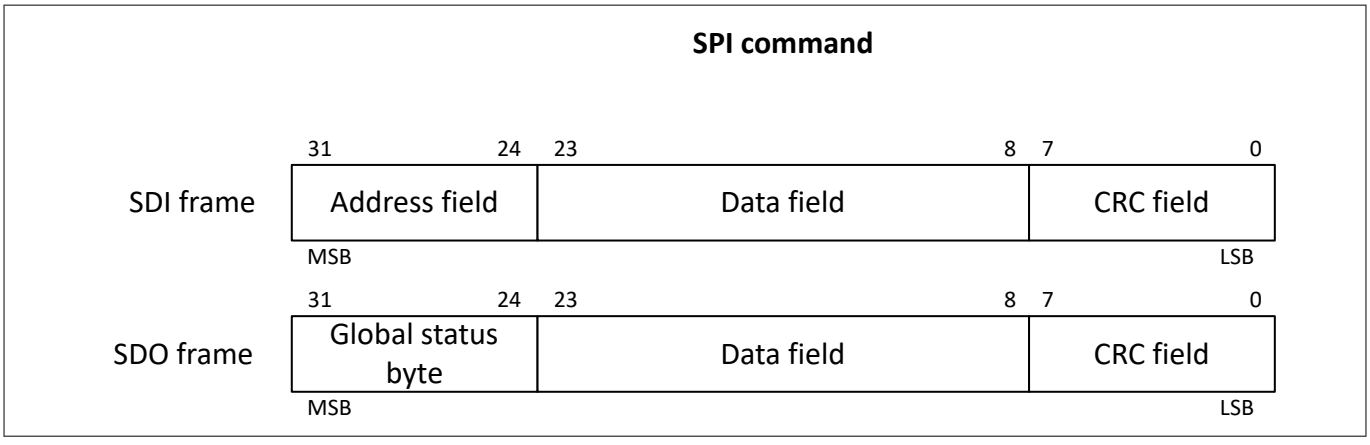

Figure 26 SPI command format

1.5.1 SPI status bits relation to global status byte

The SDO shifts out the global status register during the first eight SCK cycles to provide an overview of the device status shown in Table 11 as following (in Figure 27). The global status register consists of the following global status flags:

- B7 (OFC flag): at least one SPI frame is corrupted
- B6 (LFOK flag): last received SDI frame is correct
- B5 (VSUPE flag): supply status flag
- B4 (MISC flag): miscellaneous status flag
- B3 (BDRE flag): bridge driver status flag
- B2 (DE flag): device error indication using SPI register failure detection bits configured as error, latched error 1, latched error 2 OR in case safe state is forced
- B1 (DW flag): device warning indication using SPI register failure detection bits configured as warning
- B0 (POR): power on reset indication

***Note**: In case the SPI timing parameters according to datasheet are violated (for example CSN leading edge < t_{CSN_LDEL}), then the global status byte content might be set to 0x00. It is recommended to ignore the received SDO frame and to resend the SPI command request.*

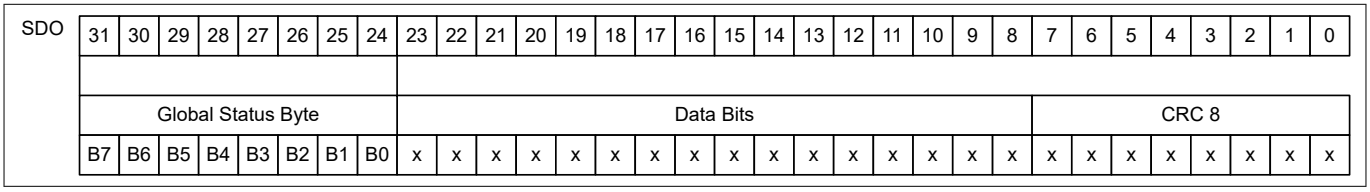

Figure 27 SDO frame with global status byte

Table 11 Global status byte information

Type of error	Name of global status flag	Failure reported in the global status byte	Global error flag	Related bits in SPI register (logical OR)
One SDI frame corrupted	OFC	OFC = 1	1	OFC
Last SDI frame correct	LFOK	LFOK = 0	1	SPI_IA, CRC_FAIL, FRAME_ERR
Supply error	VSUPE	VSUPE = 1	1	CSA_SUP_UV, VSCP_UV_SD, VSCP_OV_SD, VCPH_UV, VIO_UV,VIO_OV
Miscellaneous error	MISC	MISC = 1	1	OTP_ERR, WDE, WDLE, SDO_SHORT, CRC_FAIL, SPI_IA, CSN_TO, IPV_CCP_HB3, IPV_CCP_HB2, IPV_CCP_HB1, IPV_STP_HB3, IPV_STP_HB2, IPV_STP_HB1, PFB3_LE, PFB2_LE, PFB1_LE, ERRN_SHORT, CSA_OC, TSD_IC, TSD_CP, TSDW, VDH_UV

(table continues...)

Table 11 (continued) Global status byte information

Type of error	Name of global status flag	Failure reported in the global status byte	Global error flag	Related bits in SPI register (logical OR)
Bridge driver error	BDRE	BDRE = 1	1	Bits in SPI register BD_STAT: DSOV_HSx, DSOV_LSx, IHx_MISS, ILx_MISS
Device error indication	DE	DE = 1	1	Related bit set AND failure reaction configured as: LE1, LE2, Error OR Safe state triggered (for example, power-up mode)
Device warning indication	DW	DW = 1	0	Related bit set AND failure reaction configured as: Warning
Power ON reset	POR	POR = 1	1	POR
No error indication and no power ON reset		OFC = 0 LFOK = 1 VSUPE = 0 VSCPE = 0 DSOV = 0 DE = 0 DW = X POR = 0	0	n.a.

DE status flag is used in the application to:

- Indicate a failure has detected
- Feedback towards microcontroller in case safe state is entered/forced

DE status flag and ERR_N pin behavior are linked for failure reaction which are configured as error, latched error 1, latched error 2:

- In case ERR_N pin "low", then DE status bit set to "1"
- In case ERR_N pin is not driven actively "low" by the device, then DE status bit "0"

In power-up mode, safe state is internally forced and ERR_N pin is set to "low". The DE status flag is set to "1" independent of any failure detected by the device.

1.5.2 CSN time-out additional information

In order to detect permanent CSN "low" cases (for example, CSN pin short to GND) and in order to avoid manipulated communication for parallel ICs the device offers a CSN time-out detection.

The CSN time-out feature can be disabled by bit CSN_TO_DIS. The failure behavior of CSN time-out detection is fixed as a warning.

If the CSN pin is set to "low" for t > t_{CSN_TO} a CSN time-out is detected and the following additional steps are performed:

- SDO pin is set to tri-state
- CSN_TO status bit is set to "1"

In case CSN time-out function is disabled by CSN_TO_DIS, CSN_TO status bit will not be cleared if it is already set to "1", until a clear request is triggered by SPI clear command. In case a valid SDI frame is received within the CSN "low" phase and before CSN time-out detection, the SDI frame will be accepted by the device even if CSN time-out is detected.

1.5.3 Clear by SPI write command

Example for successful clear on write SPI command:

If in register 0x25 the error condition for VSCP undervoltage is set, in order to successfully reset this specific error condition the SPI command requires:

- SPI write command: C = "1"
- Address: 0x25
- Write data: at least bit VSCP_UV field has to be set to "1"
- Correct CRC8

For in-frame response when a clear by SPI write command is requested, in case during the CSN "low" time a status bit is set to "1" by the device, this status bit will not be reset to "0" by SPI clear by write command and will be visible in the next SPI frame.

1.5.4 Clear SPI status registers

The device offers multiple ways to clear a status register:

- SPI clear by write command of dedicated SPI bit, see Clear by SPI write command OR
- Reset of all SPI status bits by SPI write command in register PWR_MOD_CFG bit CLR_STATS. Clear request of all SPI status register by CLR_STATS is triggered only once when SPI write command to CLR_STATS bit is triggered. Once SPI status registers are cleared CLR_STATS bit remains set to "1"

In order to check for correct SPI communication during power-up of the device the user may send a dummy SPI command and check for correct SPI SDO frame response. If correct move forward, if SDO frame is incorrect, then wait 1 ms and try again by sending a dummy SPI command. Another procedure is to send the SPI clear by write command and to retry valid SPI communication after 1 ms as stated, for example, in the power-up sequence in Power-up and power-down sequence.

1.5.5 Clear SPI register configuration

The device offers the possibility to clear/reset the SPI control register by SPI write command in register PWR_MOD_CFG bit CLR_CONFIG. The request to reset the control SPI status register by CLR_CONFIG is triggered only once when SPI write command to CLR_CONFIG bit is triggered. Once the reset is performed by the device CLR_CONFIG bit is set to "0". In this case the device control registers are reset to default configuration, and the following actions are taken by the device:

- The device resets all SPI control registers to default configuration except CONFIG_SECURED register
- The device changes the mode of operation to power-up mode (forced safe state)

When a complete reset of control and status registers is requested by the microcontroller via SPI, it is recommended to send two consecutive SPI commands:

- First, clear the configuration registers by SPI write command in register PWR_MOD_CFG bit CLR_CONFIG - the device goes to power-up mode and several modules will be disabled (default configuration)
- Second, clear all status information by SPI write command

If the status registers are cleared at the same time with the configuration registers, several status information bits might not be cleared since the function behind is still enabled and triggering event might still be present.

1.5.6 Global error flag

The global error flag (GEF) can be used to either receive a very fast status update on error detection of the device or can be used to map other signals besides the SPI communication to the SDO pin. In the latter case, the SDO pin can be used, for example, as a digital indicator of the phase status by using the phase feedback feature (PFB).

Global error flag indication is configurable by bits GEF_CFG. Besides the global error flag indication the status of phase feedback phase 1 (PFB1), phase feedback phase 2 (PFB2), phase feedback phase 3 (PFB3) OR XOR function of all PFBx signals can be mapped to the global error flag.

When the GEF bit is configured as a global error flag, the microcontroller can run a quick diagnosis without any SPI clock pulse if a fault condition is detected. The global error flag is a logic OR combination of following bits of the global status byte: GEF = (OFC) OR NOT(LFOK) OR (VSUPE) OR (MISC) OR (BRDE) OR (DE) OR (POR).

1.5.7 SPI timing information

INH start up timing for SPI

Once INH is set from "low" to "high", SPI communication is possible after t_{core_up}.

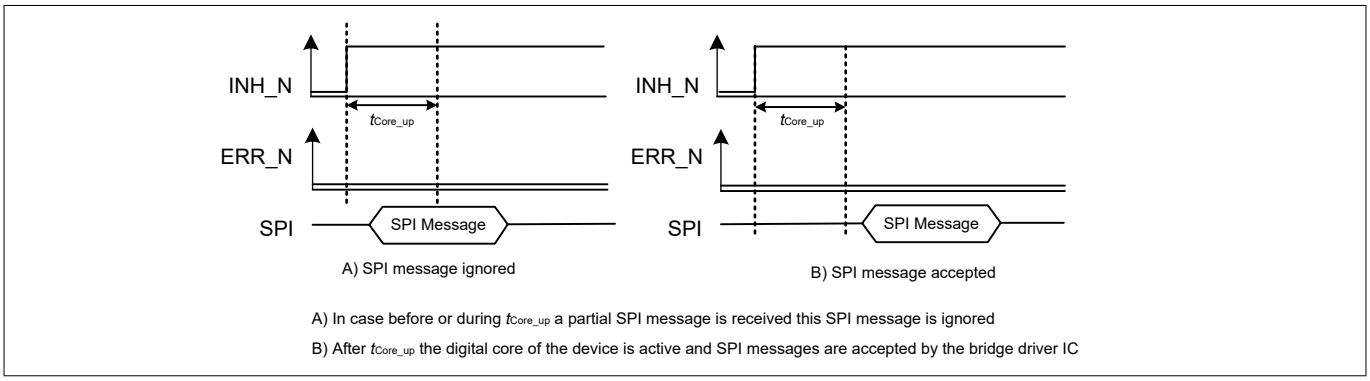

Figure 28 Setup time from INH rising edge to first SPI communication

SDI, SCK, CSN and SDO timing information

All provided timing parameters defined in the datasheet refer to the device pins: SCK, SDI, SDO, and CSN. The microcontroller output strength and the input circuitry between microcontroller and bridge driver can cause a delay on the input pins SCK, SDI, and CSN. For valid SPI communication SPI timing parameters minimum t_{SDI_hold}, t_{SDI_SET}, t_{SCK_L} and t_{SCK_H} for correct device SDI sampling and maximum t_{SDO_VDEL} for correct microcontroller data reception are essential.

For all SPI communication frequencies, it is recommended to ensure input signal rise and fall times at pins SDI, CSN, SCK are < 10% of used clock period t_{pSCK}. t_{SDO_VDEL} starts when $V_{SCK} > V_{SPI_H}$.

1.5.8 SPI communication error detection

The SPI incorporates error flags LFOK and OFC in the global status byte to supervise and preserve the data integrity.

If the following SPI errors are detected during a given frame, the error flag OFC is set to "1" AND LFOK is set to "0" in the next SDO frame:

- The number of SCK clock pulses received for the duration CSN = 0 is (protocol error):
  - Not zero
  - Or less than 32
  - Or more than 32
- Incorrect CRC8 detection in received SDI frame

- The microcontroller sends an SPI command to an unused address
- A clock polarity error is detected: the incoming clock signal was high during CSN rising or falling edges (protocol error)
- Any write command to protected registers in normal mode after successful configuration of the device
- The wrong checksum control bit was received

The following additional SPI communication failures are possible:

- Timing error (inter-frame delay violation). In this case, one of the two consecutive SPI frames is interpreted as corrupted by the device will lead to an SPI error. OFC = 1, LFOK = 0 visible in the next valid SPI frame
- Access error (SPI write request to read-only bit). All reserved bits in the SPI register specification are read-only bits. In this case, no error is reported by the device as long as the incoming SDI frame, including CRC8, is correct. The SPI write command is ignored by the device. An exception is the CONFIG_SECURED register. If the device is in normal operation mode and an SPI write access is sent by the microcontroller during normal mode to CONFIG_SECURED register, then OFC = 1, LFOK = 0 is reported in the next SPI SDO frame

1.5.9 SPI format change via SPI command

After power-up of the device by default, the SPI frame format is configured as an in-frame response (IFR). An SPI frame format can be configured via bits SPI_TYPE. The SPI frame format can be changed in power-up mode only.

This chapter describes how the device behaves during the transition of the SPI frame format configuration from in-frame response (IFR) to next-frame response (NFR) and vice versa.

Once the microcontroller requests an SPI frame format change via SPI command, the command is accepted by the device after having received the complete SDI frame and the SDI frame is valid. The device interprets the SPI SDI frame always at CSN low-high transition after the SPI command has finished and implicitly the SDO output frame has already been sent to the microcontroller. For the SPI command, the microcontroller must expect in the current frame an SDO content according to the present SPI frame configuration, which is configured before sending the SPI command to change the SPI frame format. Starting with the next SPI command, the SPI frame format for the SDO is changed according to the configuration.

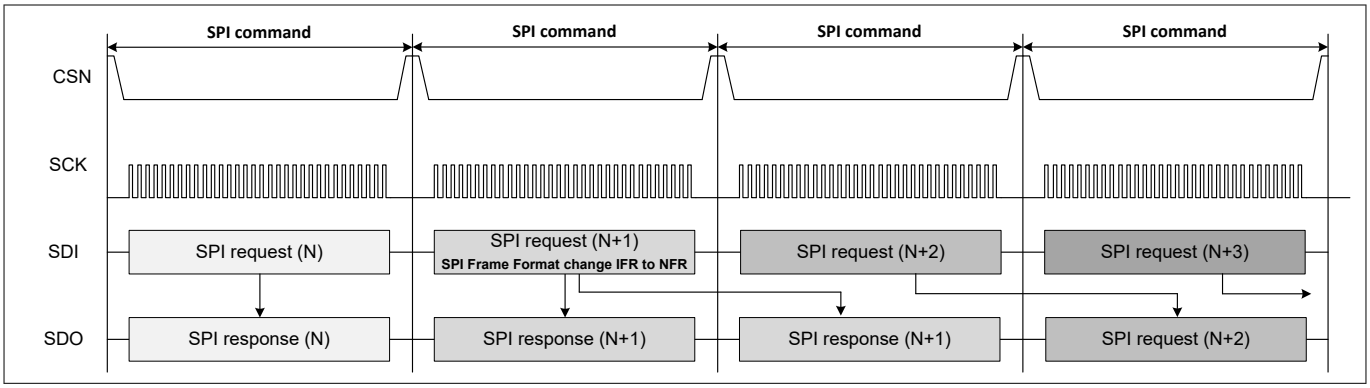

Figure 29 SPI frame format change: NFR to IFR

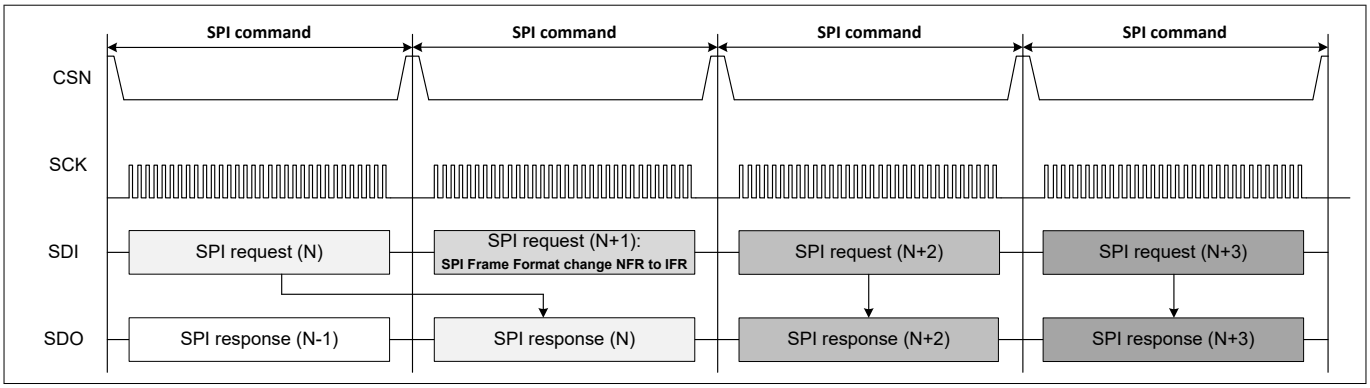

Figure 30 SPI frame format change: IFR to NFR

***Note**: For the SPI frame format change from IFR to NFR the SDO response content can change even though the same address content is sent via SDO consecutively. In the above example, this relates to SDI frame (N+1). SDO N+1 (IFR) is the content before the register updates. The SDO response for SDI frame N+2 (NFR) is the content of the same address after the content has been updated.*

1.5.10 CRC8 calculation

As shown in Figure 26 the SDI frame and SDO frame of an SPI command include a CRC field at the end of the frame. For a valid SPI command, the CRC field has to match to the sent content of the SDI and SDO frame. The CRC field has to be filled with the correct calculated CRC8. This chapter includes additional information for the CRC8 calculation for SDI and SDO frame. The CRC calculation uses the CRC8 of SAE J1850 standard polynomial calculation.

Table 12 CRC8 calculation

CRC result width	**8 bits**
Polynomial	$0x1D_H$
Initial value	$0xFF_H$
XOR value	$0xFF_H$
Check	$0x4B_H$
Magic check	$0xC4_H$

1.5.10.1 CRC8 calculation for SDI frame

The microcontroller calculates the CRC for the SDI frame. The CRC calculation starts with byte 3 and ends with byte 1. For SDI frame the CRC8 is calculated for the SDI 24 payload bits in the order of received 7 bit address + 1 bit C and 16 bit write data, CRC8 bits excluded.

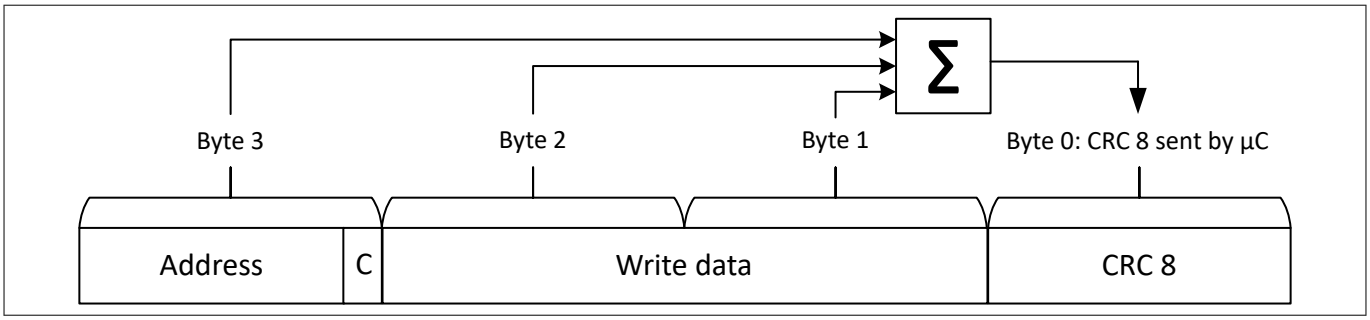

Figure 31 SDI byte order for CRC8 calculation

Example: the correct calculated CRC8 for SPI write command on register 0x04 with data field content 0xE9EF is 0x3B. The complete SDI frame is 0x09E9EF3B.

1.5.10.2 CRC8 calculation for SDO frame

The device calculates the CRC8 for the SDO frame. The CRC calculation includes the following SDO frame elements:

- Byte 4: concatenated logic "0" + 7 bit physical register address of the data shifted on SDO in the data field
- Byte 3: global status information byte
- Byte 2 + byte 1: 16-bit data field

The CRC8 calculation starts with byte 4 and ends with byte 1.

***Note**: In case of in-frame response, the byte 4 content is the received address in the SDI frame of the current SPI transfer, while in case of next-frame response, the byte 4 content is the received address in the SDI frame of the previous SPI frame.*

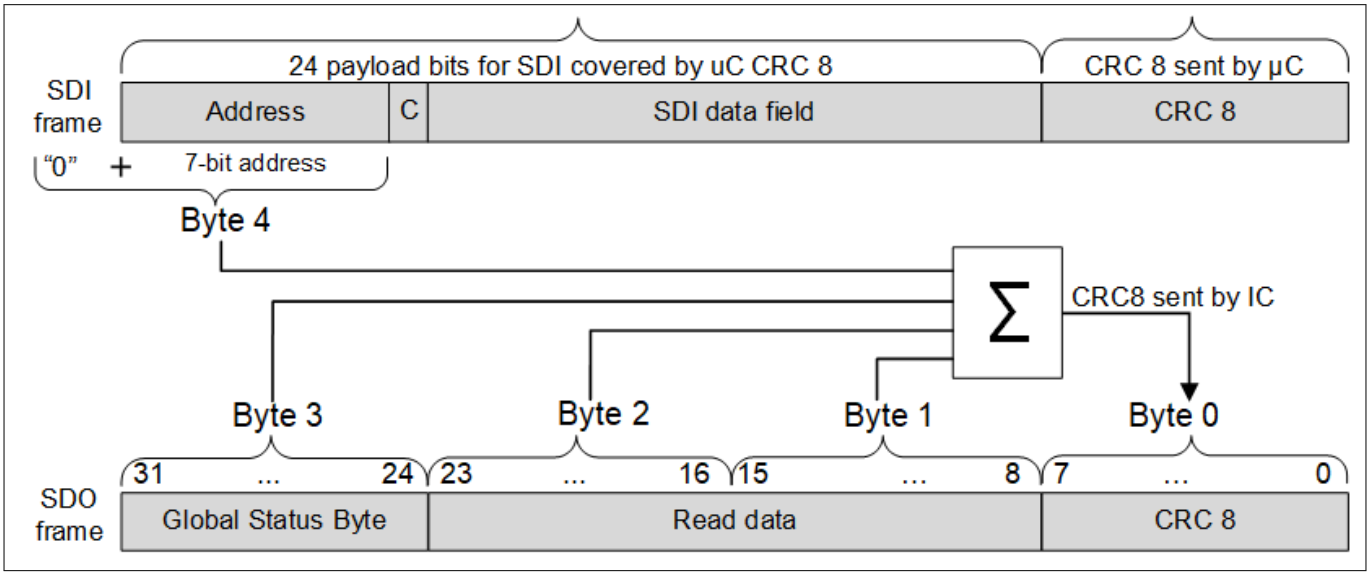

Figure 32 In-frame-response SDO byte order for CRC8 algorithm

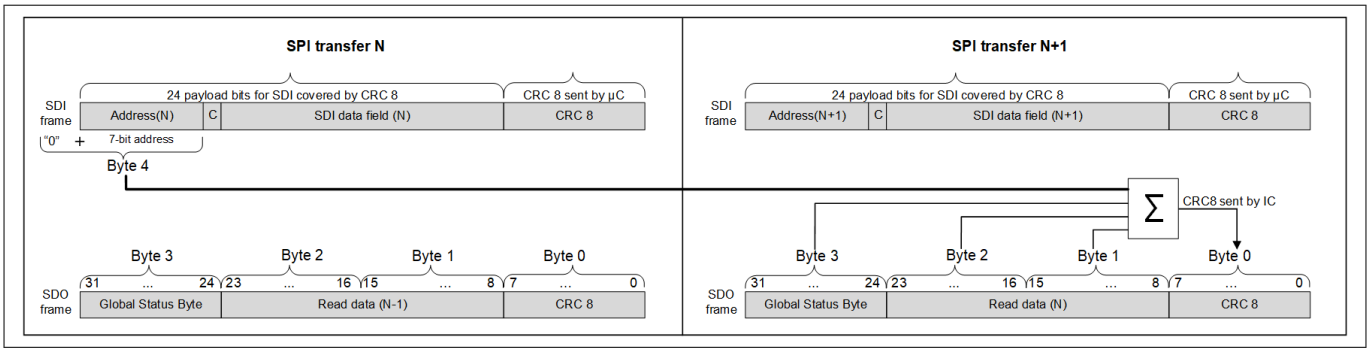

Figure 33 Next-frame-response SDO byte order for CRC8 algorithm

Example: the correct calculated CRC8 for an SDO frame with SDI address content 0x04, global status byte content 0x5D and data content 0xE9EF is 0xA3. The complete SDO frame is 0x5DE9EFA3.

1.6 Diagnostics (additional information)

The table below an overview of available supervision functions and related status bits.

Table 13 Diagnostics overview

Diagnostic	Device internal self-test availbale	Failure behavior	Related configuration/ control bits	Related status bits
Power supply supervision functions				
VSCP undervoltage shutdown detection	YES	LE1	VSCP_MON_ST	VSCP_UV_SD
VSCP overvoltage shutdown detection	YES	LE1	VSCP_MON_ST	VSCP_OV_SD
VIO undervoltage detection	YES	LE1	VIO_MON_ST	VIO_UV
VIO overvoltage detection	YES	LE1	VIO_MON_ST	VIO_OV
Charge pump undervoltage detection	YES	LE1	CP_UV_TH, CPMON_ST	VCPH_UV
Gate driver internal supervision functions				
Overtemperature warning detection	YES	LE1, W	TW_FM, TW_TH, TSD_ST	TSDW
Overtemperature shutdown detection (general IC or charge pump)	YES	LE1	TSD_ST	TSD_IC, TSD_CP
Internal clock monitoring	YES	LE1	CLK_MON_ST	–
Internal core supply monitoring	YES	LE1	REG_UV_ST	–

(table continues...)

Table 13 (continued) Diagnostics overview

Diagnostic	Device internal self-test availbale	Failure behavior	Related configuration/ control bits	Related status bits
Motor bridge output stage supervision functions				
Drain-source overvoltage detection	YES	LE1, LE2	TFVDS, TBLANK, TBLANK_FW, HS_DSOVTH, LS_DSOVTH, DSOV_FM, DSOV_ST	DSOV_LSx, DSOV_HSx
VDH undervoltage detection	YES	W	–	VDH_UV
OFF state diagnostics	NO	N.A.	OFF_DIAG_EN, HBxIDIAG	VSHx_L, VSHx_H
Phase feedback monitoring	NO	LE1, W	PFB_EN, PFB_FM, TPFB	PFBx_H_CNT, PFBx, PFB_LE
Current sense amplifier supervision functions				
CSA overcurrent detection	YES	LE1, E	CSA_DIR, CSA_OC_TH, CSA_TFOC, CSA_GAIN, CSA_OC_FM, CSA_OC_ST	CSA_OC
Internal CSA supply monitoring	YES	LE1, W	CSA_SUP_ST	CSA_SUP_UV
Interface to microcontroller supervision functions				
PWM alternation monitoring	NO	E, W	PWM_CHK_EN, PWM_CHK_FM	ILx_MISS, IHx_MISS
ERR_N stuck "high"	NO	LE1, W	ERRN_FM	ERRN_SHORT
SDO stuck detection	NO	LE1, E	SDO_SHORT_FM	SDO_SHORT
Window watchdog failure detection	NO	LE1, E	WD_EN, WD_PER, WD_FAIL, CHECKSUM, WD_CNT, WD_FM, WD_CLK_CNT,	WDLE, WDE
Shoot through violation	NO	LE1, W	HBx_EN	IPV_STP_HBx
Input pattern violation	NO	LE1, W	IPV_CCP_DIS, IPV_CCP_FM, TCCP_FW, TCCP	IPV_CCP_HBx
INH_N low pulse detection	NO	LE1, LE1 with automatic restart	INHN_REC_FM	INHN_L_DET

1.6.1 Failure reaction definition

The device can be configured in four different ways to react to failures which it detects. Refer to the device datasheet for failure reaction description. The following chapters include additional information related to the configurable failure reaction of the device, such as timing diagrams. The table below shows the possible configurations and priorities.

Table 14 Failure reaction priority

Configured failure reaction	Priority
Latched error 1 (LE1) - safe state INH_N pin = "low"	1
Latched error 2 (LE2)	2
Error (E)	3
Warning (W)	

***Note**:*

- *Error and warning failure behavior have the same priority. In both cases, the output stages for the gate driver remain active in normal operation mode*
- *In the figures below, Ixx represents the PWM input pin signals ILx and IHx_N. Gxx-Sxx represents the gate to source output signal on GLx-SL and GHx to SHx pins*

1.6.1.1 Failure reaction: warning (W)

Failure behavior for transient error detection, and permanent error detection for failure reaction warning (W) are shown in the figures below.

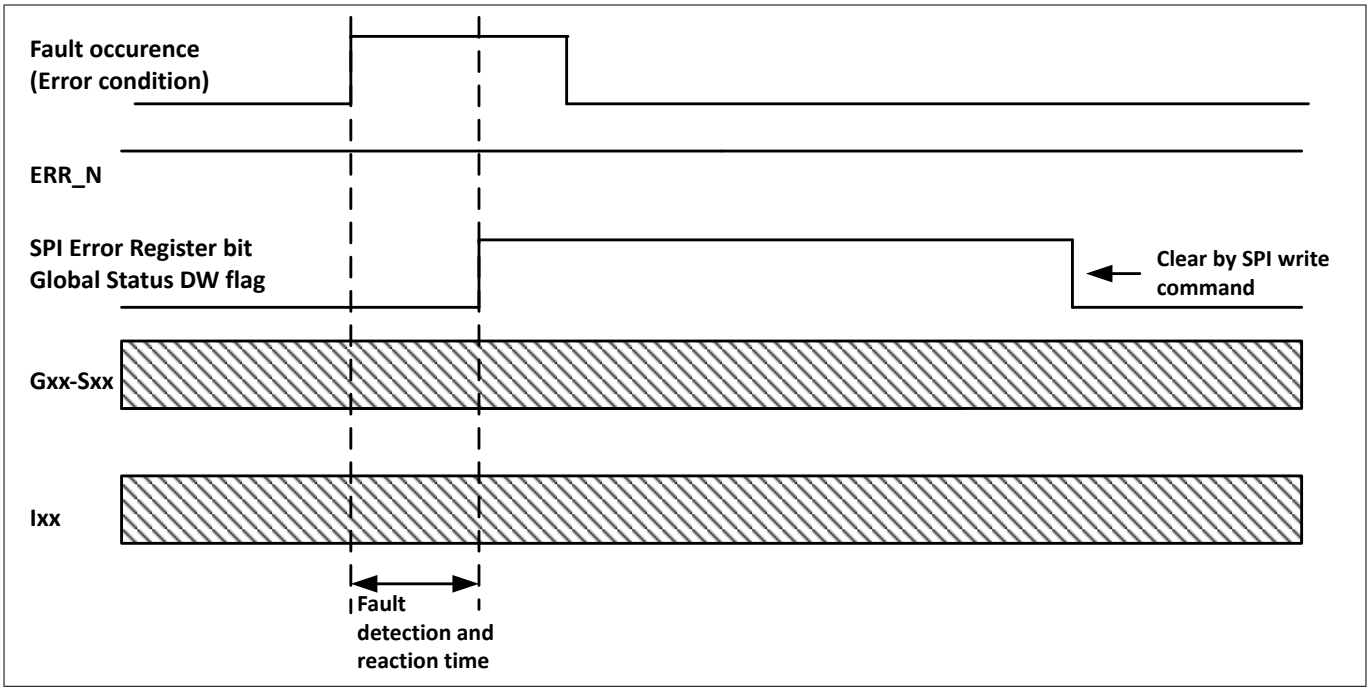

Figure 34 Timing diagram warning: transient fault occurrence

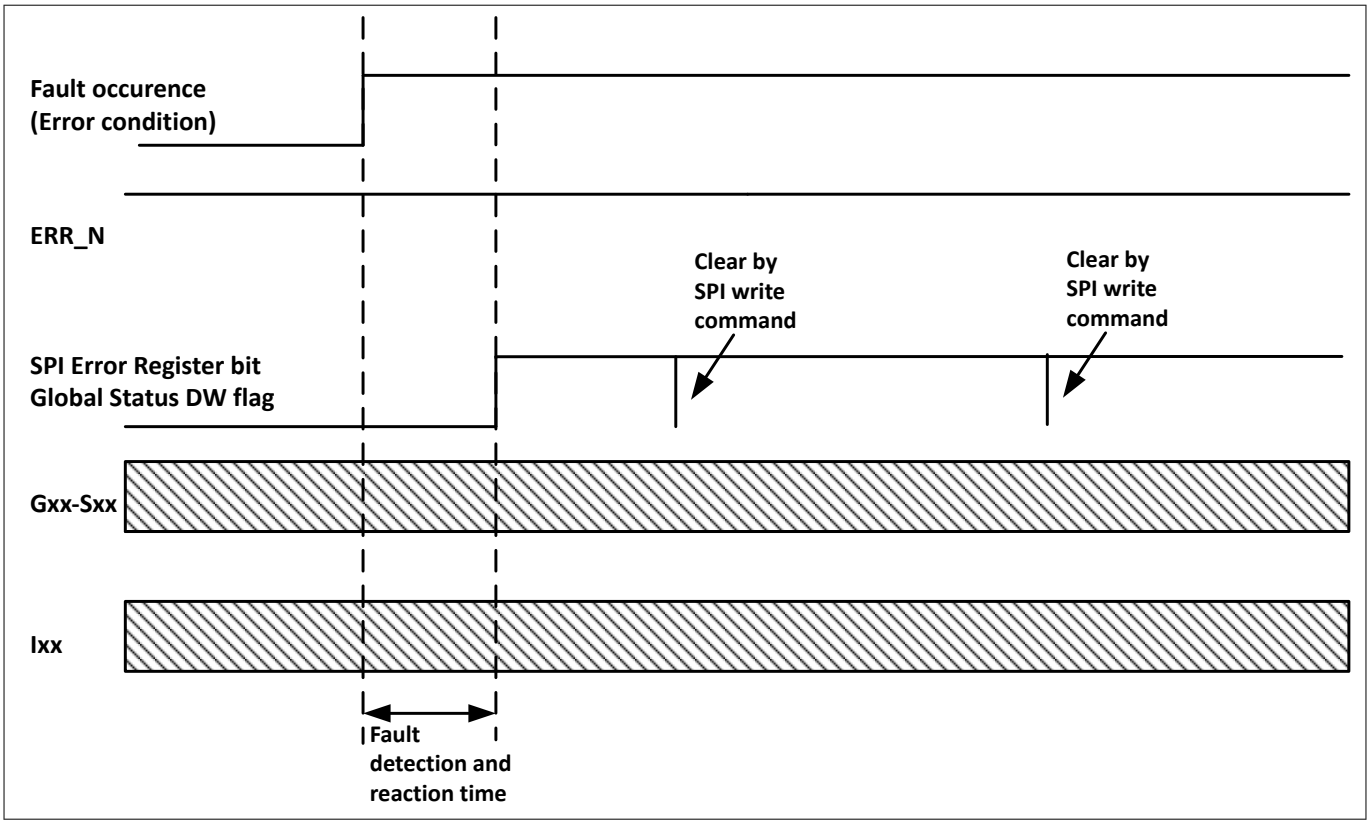

Figure 35 Timing diagram warning: permanent fault occurrence

1.6.1.2 Failure reaction: error (E)

Failure behavior for transient error detection, and permanent error detection for failure reaction error (E) are shown in the figures below.

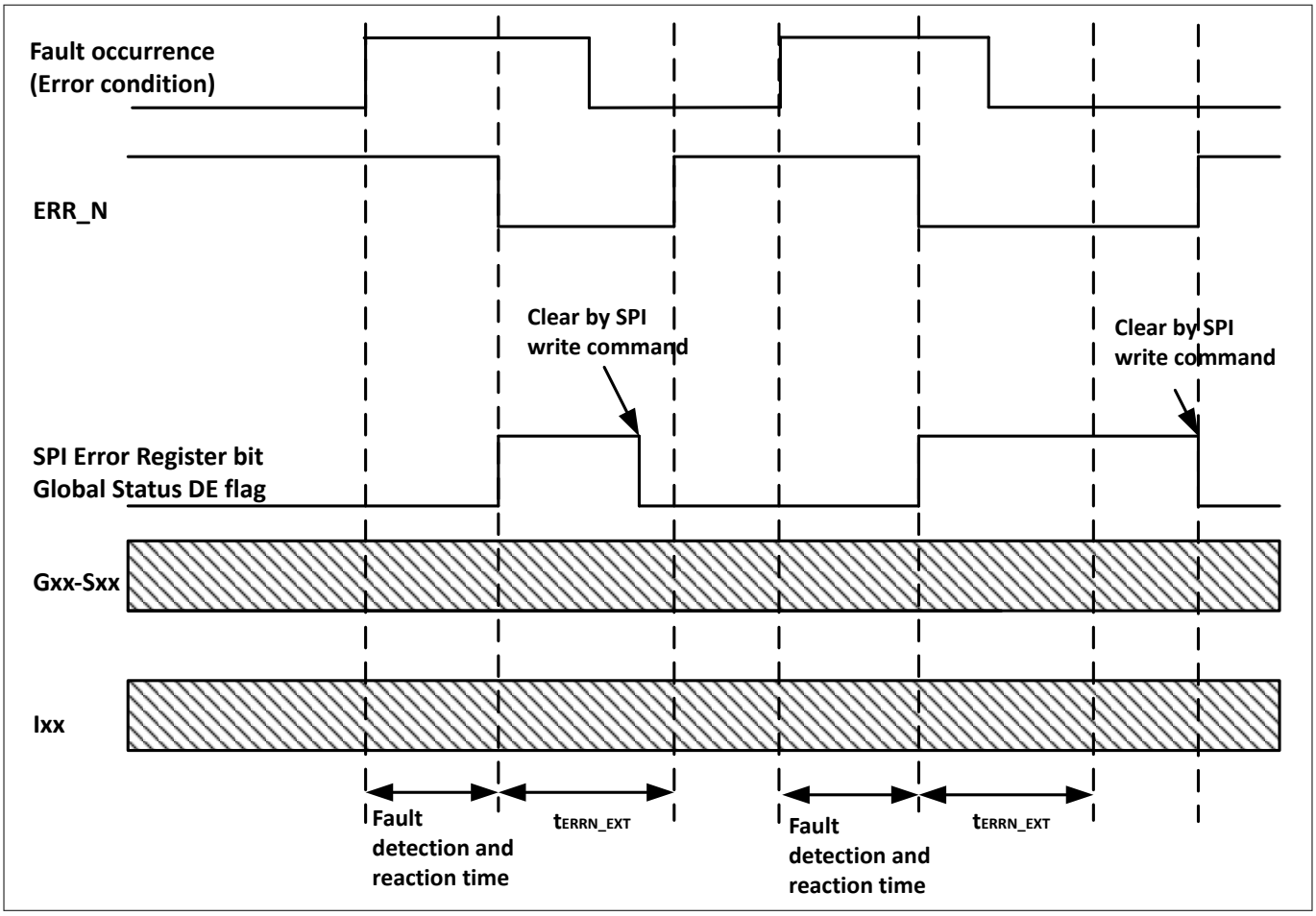

Figure 36 Timing diagram error: transient fault occurrence

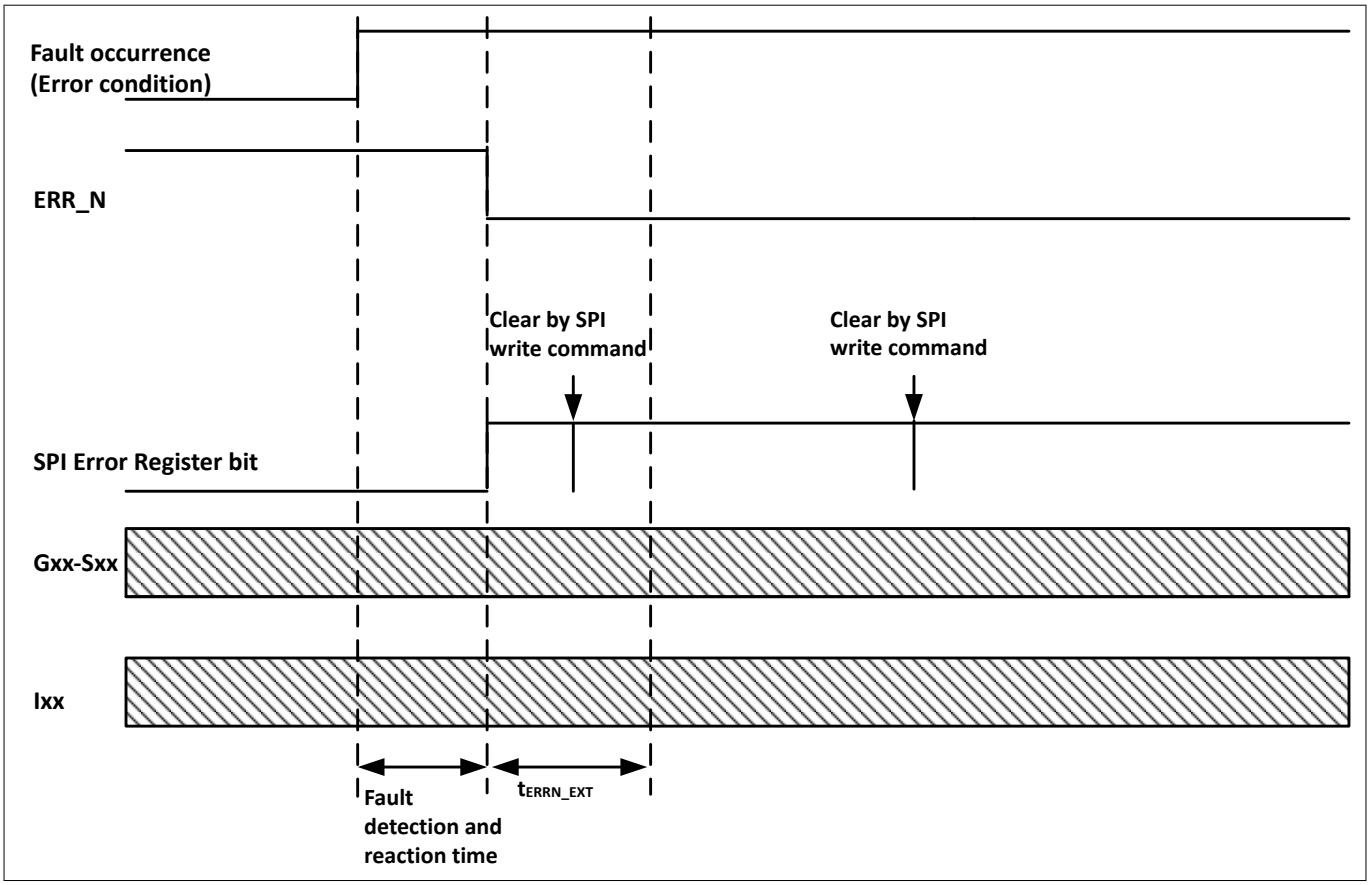

Figure 37 Timing diagram error: permanent fault occurrence

1.6.1.3 Failure reaction: latched error (LE1 and LE2)

Failure behavior for transient error detection, and permanent error detection for failure reaction latched error 1 (LE1) and latched error 2 (LE2) are shown in the figures below.

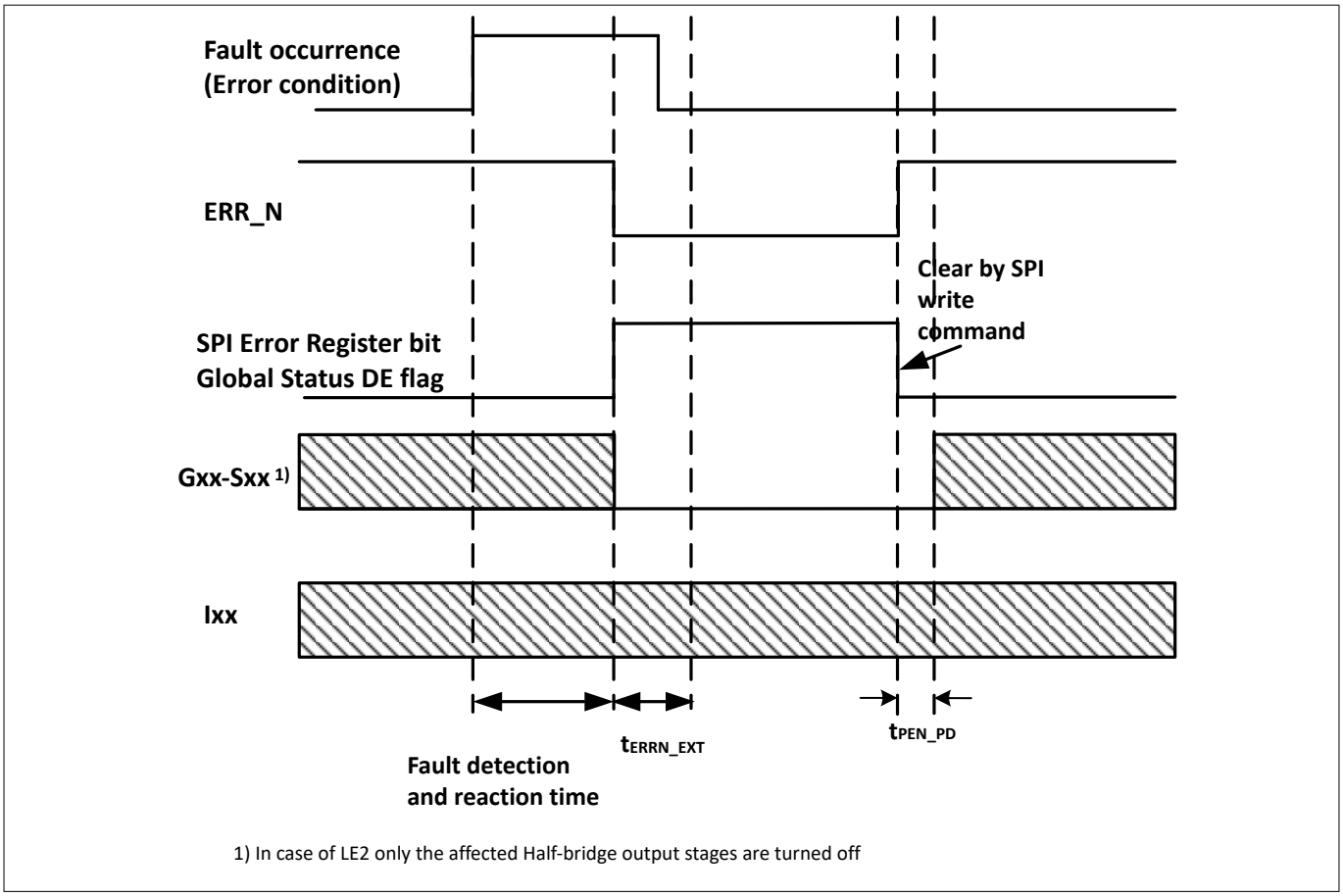

Figure 38 Timing diagram latched error: transient fault occurrence

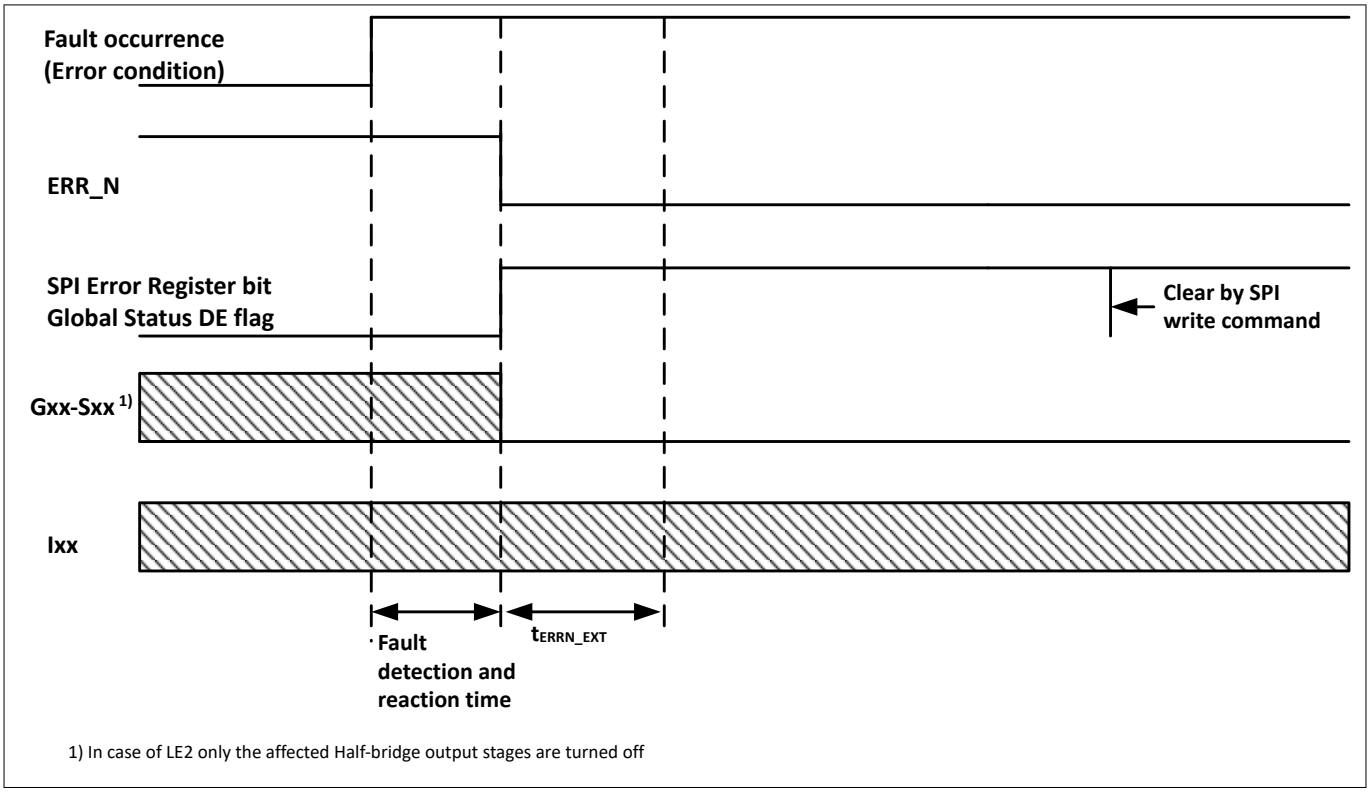

Figure 39 Timing diagram latched error: permanent fault occurrence

In case a failure is detected by the device, which is configured as latched error 1 (LE1) or latched error 2 (LE2); or in case safe state entry is triggered by external command by INH_N pin, the switch OFF behavior of the Gxx output stages is configurable by control pin OFF_CFG in SPI register CONFIG_SECURED:

- OFF_CFG = "0" (default): turn-OFF gate drivers with active turn-OFF settings (default)
- OFF_CFG = "1": turn OFF gate drivers using I_{1OFF} for T_{1OFF} and I_{DCHG_ST} for TCCP

In case of a fault detection leading to LE1 failure reaction, the device enters safe state (see Safe state (additional information)). For LE1 and LE2 failure reaction, ERR_N pin is set to "low" and status bit ERRN_ACT is set to"1".

1.6.1.3.1 Passive to active PWM transition

If the device enters safe state (LE1 failure reaction) with passive discharge enabled, when the latched error detection is cleared by SPI reset command, the gate driver output stages are switched from passive discharge to active discharge within t_{PEN_PD}.

1.6.2 Self-test functions

The device offers various self-test possibilities for extended diagnostics during the ramp up phase of the application or even during the operation of the application. To initiate a self-test run, the microcontroller must send an SPI write command with at least one data bit logic "1" to the related self-test bits in self-test control register SELF_TEST_CFG.

All self-tests that are triggered by the microcontroller, by SPI command, are subject to a self-test timeout $t_{ST_timeout}$. For a correct evaluation of a self-test triggered by the microcontroller via SPI command it is recommended to ensure that no failure is detected before running the self-test routine. If a failure is detected, this causes the SPI status bit to be set to "1", before the self-test runs.

After the self-test has run, the device sets the self-test control bit to "0". There are two general status bits that provide information on the self-test:

- ST_RDY (self-test ready) - a read-clear status bit indicating that the self-test has finished
- ST_RES (self-test result) - a read-only message that indicates whether the self-test was successful or not

The self-test result status bit ST_RES shall be interpreted by the microcontroller only if ST_RDY = "1" (self-test finished). As long as ST_RDY is "0", ST_RES is not relevant. If a self-test does not lead to a successful result within $t_{ST_timeout}$, the self-test routine is automatically exited and self-test reports a failure (ST_RDY = "1" AND ST_RES = "0").

ST_RES and ST_RDY bits default value is logic "0" at power-up.

Before any self-test request, it is recommended that the microcontroller checks that there is no failure detected by the device, which blocks the correct execution of the self-test by the device. Depending on the configured failure reaction in the application, it is recommended to confirm correct behavior of the ERR_N pin "low" status and status bits ERRN_ACT, SOFF_ACT, SOFF_GDRV. For more information on triggering the self-test functions, refer to the related chapters.

The following self-test functions are available:

- Overtemperature monitoring self-test
- Drain-source overvoltage monitoring self-test
- VIO monitoring self-test
- Charge pump monitoring self-test
- VSCP and VDH monitoring self-test
- PFB monitoring monitoring self-test
- CSA overcurrent monitoring self-test
- Safe path activation self-test
- CSA internal supply monitoring self-test

- Internal regulator undervoltage monitoring self-test
- Clock monitoring self-test
- Bias and latent fault detection self-test

1.6.2.1 ERR_N pin functional check

The correct function of the ERR_N pin can be either tested by performing the self-tests, described in previous chapter by triggering the configured failure reaction causing ERR_N pin "low", OR a dedicated SPI command can be sent by the microcontroller to trigger ERR_N pin "low". In normal operation mode, in case no failure is detected, the ERR_N pin is not driven actively "low" by the device but pulled "high" due to the external pull-up resistor. In normal operation mode by SPI write command to SPI control bit ERRN_ON in SPI register GEN_CFG1 the microcontroller can request the device to pull ERR_N pin "low" without any error detection:

- ERRN_ON = "1": ERR_N pin is pulled "low" by the device
- ERRN_ON = "0": ERR_N pin is not pulled "low" by the device (in case no other error detected OR forced safe state)

With this feature the user can easily confirm the correct function of the ERR_N pin.

1.6.2.2 Safe state entry functional check

The correct entry of safe state entry, either tested by performing the self-tests described in previous chapter by triggering the configured failure reaction causing safe state entry, OR a dedicated SPI command can be sent by the microcontroller to trigger safe state entry. In normal operation mode by SPI write command to SPI control bit SOFF_ON in SPI register GEN_CFG1 the microcontroller can request the device to pull ERR_N pin "low" without any error detection:

- SOFF_ON = "1": safe state entry forced without error detection
- SOFF_ON = "0": safe state entry not forced

1.6.3 Overtemperature

The device offers two overtemperature thresholds:

- Overtemperature warning threshold T_{jW}
- Overtemperature shutdown threshold T_{jSD}

The figure below shows the options for configuring thresholds and failure behavior.

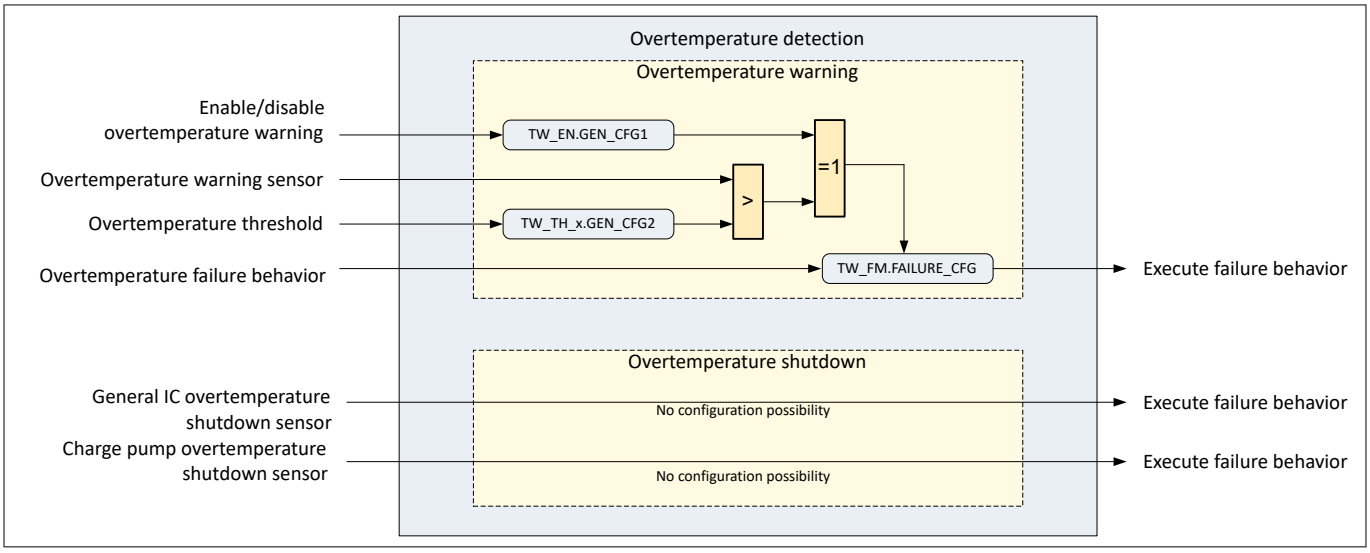

Figure 40 Configuration of overtemperature detection

1.6.3.1 Overtemperature warning

The overtemperature warning can be activated or deactivated by bit TW_EN. The overtemperature warning has four configurable thresholds for T_{jW}. If the overtemperature warning sensor reaches T_{jW} for $t > t_{TSDf}$ bit TW_EN is set to 1, then TSDW bit is set and related flag in the global status byte is set.

If thermal warning is activated, the failure reaction behavior is configurable by bit field TW_FM. Thermal warning temperature threshold is configurable by bit field TW_TH.

To clear the TW status bit, the following conditions must be met:

- The temperature warning condition has disappeared OR temperature warning is disabled (TW_EN = 0) AND
- The microcontroller clears the TSDW status bit by SPI write command OR
- Clear status register SPI command (CLR_STATS)

***Note**: If the TW_EN bit is set to "0" overtemperature warning is disabled, the TSDW status bit will not be cleared if already set to "1", until a clear SPI write command.*

1.6.3.2 Overtemperature shutdown

If the general temperature sensor OR charge pump temperature sensor reaches T_{jSD} for t > t_{TSDf}, the device reaches overtemperature shutdown threshold and behaves as follows:

- The failure reaction is latched error 1 (LE1). Safe state is entered
- In case of charge pump overtemperature shutdown detection bit, TSD_CP is set to "1" AND CP_EN bit is set to "0"
- In case of general IC overtemperature shutdown detection bit, TSD_IC is set to "1" AND CP_EN bit is set to "0"

All outputs remain deactivated until the TSD_CP, TSD_IC bit is cleared by SPI write command. To resume normal functionality of the gate drivers, the following conditions must be met:

- The temperature shutdown condition has disappeared AND
- The microcontroller clears the associated TSD bit in the related register by SPI write command
- AND enable the CP module via SPI command (if disabled due to corresponding TSD shutdown event)

1.6.4 Drain-source overvoltage monitoring

The device offers a drain-source overvoltage monitoring feature to avoid cross current and short circuits at the motor bridges. The following table shows the possibilities for configurations and their related control bits. Control and status bits can be found in the SPI register overview.

Table 15 Configuration options

Configuration option	Related SPI control bit	Related SPI status bit
Blank time for active MOSFET	TVDSBLK	
Blank time for freewheeling MOSFET	TVDSBLKFW	
Drain-source overvoltage threshold for high-side MOSFET	HS_DSOVTH	DSOV_HSx
Drain-source overvoltage threshold for low-side MOSFET	LS_DSOVTH	DSOV_LSx
Drain-source filter time	TVDSFILT	

(table continues...)

Table 15 (continued) Configuration options

Configuration option	Related SPI control bit	Related SPI status bit
Drain-source overvoltage failure reaction	DSOV_FM	

The figure below illustrates the possibilities for configuration.

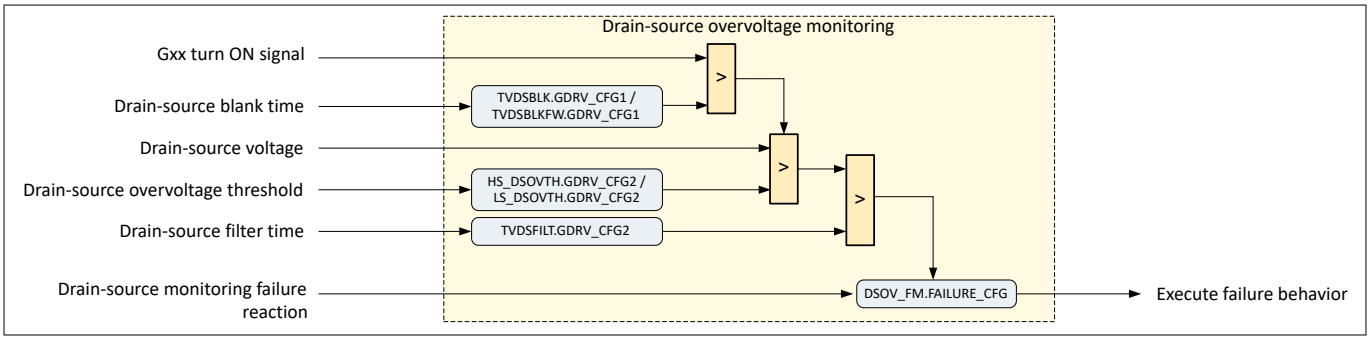

Figure 41 Configuration of drain-source overvoltage monitoring

1.6.4.1 Drain-source comparator check during run time

The correct function of the drain-source comparators is monitored in normal operation mode. If an output stage Gxx is turned on, after expiration of t_{VDS_BLK} and t_{VDS_FILT}, the status of the complementary drain-source comparator is controlled.

- For high-side output stages enabled GHx: a correct functioning of the drain-source comparator of the complementary low-side drain-source monitor is detected, if GHx is on AND V_{SHx} - V_{SL} > V_{DSOV_TH} after t > t_{VDS_BLK} + t_{VDS_FILT}
- For low-side output stages enabled GLx: a correct functioning of the drain-source comparator of the complementary high-side drain-source monitor is detected, if GLx is on AND V_{VDH} - V_{SHx} > V_{DSOV_TH} after t > t_{VDS_BLK} + t_{VDS_FILT}

In case drain-source comparator status of the complementary comparator is not indicating a drain-source overvoltage event after t > t_{VDS_BLK} + t_{VDS_FILT}, then latent fault bit for drain-source monitoring DSOV_LF_HBx and additionally the DW global status bit is set.

1.6.4.2 VDH pin external circuitry

Due to external RC filtering at the VDH pin, there can be a voltage shift between the VDH pin voltage and the bridge supply if the bridge supply drops or rises during operation. This delayed voltage shifts can cause false drain-source overvoltage detections or mask a drain-source overvoltage detection. Wrong drain-source overvoltage detection could already occur with 1 µs RC time constant, with dVS/dt = 0.5 V/µs for 2 µs.

The root cause of faster slopes at bridge supply can be undersized electrolytic capacitors, low temperature (ESR), or ageing of the capacitor. Either the ESR of the DC link capacitors is improved or the RC filtering timing constant is reduced. It is possible that nothing is visible at room temperature without aging of the caps. It is recommended to perform tests at low temperature and high peak currents at phase.

1.6.5 Phase feedback monitoring

The device offers a phase feedback monitoring feature to monitor the phases' switching and comparing it to the requested PWM input signals. The following table shows the possibilities for configuration and its related control bits. Some PFB monitoring functions use unfiltered VSHH and VSHL comparator thresholds and other use t_{PFB_filter} filtered VSHH and VSHL comparator signals. Refer to the table below for more information.

Table 16 Configuration options

Configuration option	Related SPI control bit or status bit	Comment
PFBx function at CSO pin	CSO_MUX	This configuration is used as well for PFBx output at CSO pin. In case PFBx is mapped on CSO, then it uses *filtered* VSHH and VSHL thresholds. *Filtered* with t_{PFB_filter}
Enable/disable PFB monitoring	PFB_EN	In case phase feedback monitoring is disabled, PFB_LE bit will not be cleared if already set to "1", until an SPI clear by write command
Enable half-bridges	HBx_EN	PFBx status bits is PFB monitoring function is only enabled in case HBx_EN control bit is set to "1"
PFB monitoring blanking time extension	TPFB	Configurable time applicable during turn ON of MOSFET
PFB monitoring failure reaction	PFB_FM	Configurable failure reaction in case PFBx_LE is set to "1"
Fast comparator threshold configuration	FAST_CMP_TH	Fast comparator threshold V_{SHH} and V_{SHL} used for current controlled output stage feature and PFB monitoring
PFBx status bits	PFB3, PFB2, PFB1	PFBx status bits are updated to "1" when *filtered* VSHH fast comparator threshold is reached and updated to 0 when *filtered* fast comparator threshold VSHL is reached. *Filtered* with t_{PFB_filter}
PFB failure detection	PFB1_LE, PFB2_LE, PFB3_LE	Set to "1" in case one PFBx monitoring detects failure. PFB failure detection uses t_{PFB_filter} filtered signals. *Filtered* with t_{PFB_filter}
PFBx "high" time counter	PFBx_H_CNT	Three separate "high" time counters for each SHx phase. This counter starts when *filtered* VSHH comparator threshold is reached and stops when *filtered* VSHL comparator threshold is reached. Once it is stopped the value is stored/accessible by SPI read command. *Filtered* with t_{PFB_filter}
PFBx counter ready bit	CNTx_RDY	Three separate bits indicate if PFBx_H_CNT is counting (PFBx = 1) or if phase "high" time has finished and PFBx_H_CNT is valid

Phase feedback monitoring is enabled by default and can be deactivated by PFB_EN bit set to "0". In case the half-bridge is disabled by HBx_EN = "0", then PFBx status bits are not updated and PFB monitoring is disabled for the corresponding half-bridge. Only for enabled half-bridges (HBx_EN = "1") the PFBx status bits are updated and PFB monitoring is enabled. In case PFB monitoring is enabled by the HBx_EN control bit, then PFB error reporting is disabled in case VDH undervoltage is detected by the device. PFB error reporting is automatically re-enabled in case VDH undervoltage event disappears. PFBx status bits and PFBx counters will continue to be updated in case VDH undervoltage.

In case an PWM turn ON signal (for example IL1 = "high") the output stage is turned on in normal operation mode. A configurable timer TPFB is started after the drain-source monitoring blanking time t_{VDS_BLK} has elapsed. After TPFB has expired, the phase comparator signals are checked if the phase has been driven towards V_{SHL} or V_{SHH} accordingly. If the comparator feedback does not match to expected turn-on output stage, then a phase feedback monitoring error is detected and the PFB_LE status bit is set to "1". The failure reaction is configurable via control bits PFB_FM. The thresholds V_{SHH} and V_{SHL} of the fast comparators are configurable by control bit FAST_CMP_TH.

If phase feedback monitoring was disabled, then all related status bits are set to "0". If the status bit is set to "1", it will not be automatically reset by deactivation of the feature until an SPI clear by write command. The figure below illustrates configuration possibilities.

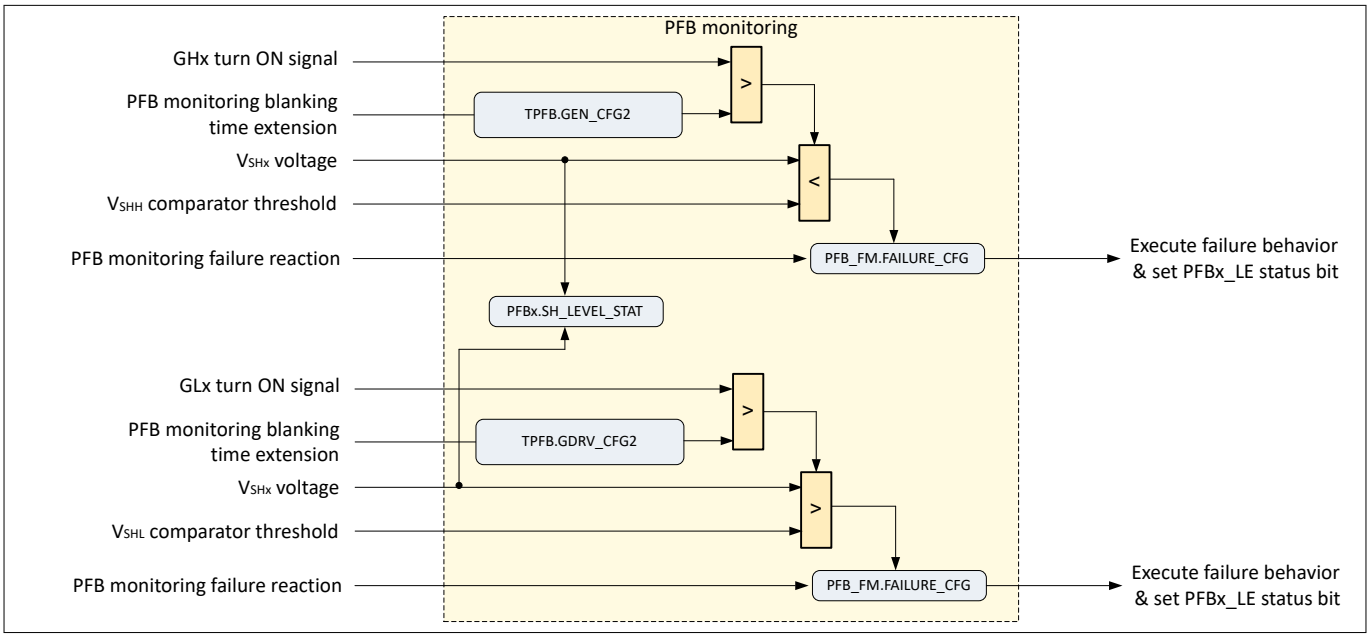

Figure 42 Configuration of PFB monitoring

In normal mode, if the low-side output stage of a half-bridge is turned ON, the device expects after TPFB to receive a PFB feedback signal showing PFBx = "0".

If the high-side output stage of a half-bridge is turned ON, the device expects after TPFB to receive PFB feedback signal showing PFBx = "1".

The figures below show two examples of correct switching of output stages for high-side and low-side output stages. In case of failure (for example, the output stage does not turn ON, the phase has a short circuit to supply or GND) and the PFBx state is not as expected, the PFB_LE bit is set and the configured failure reaction is triggered.

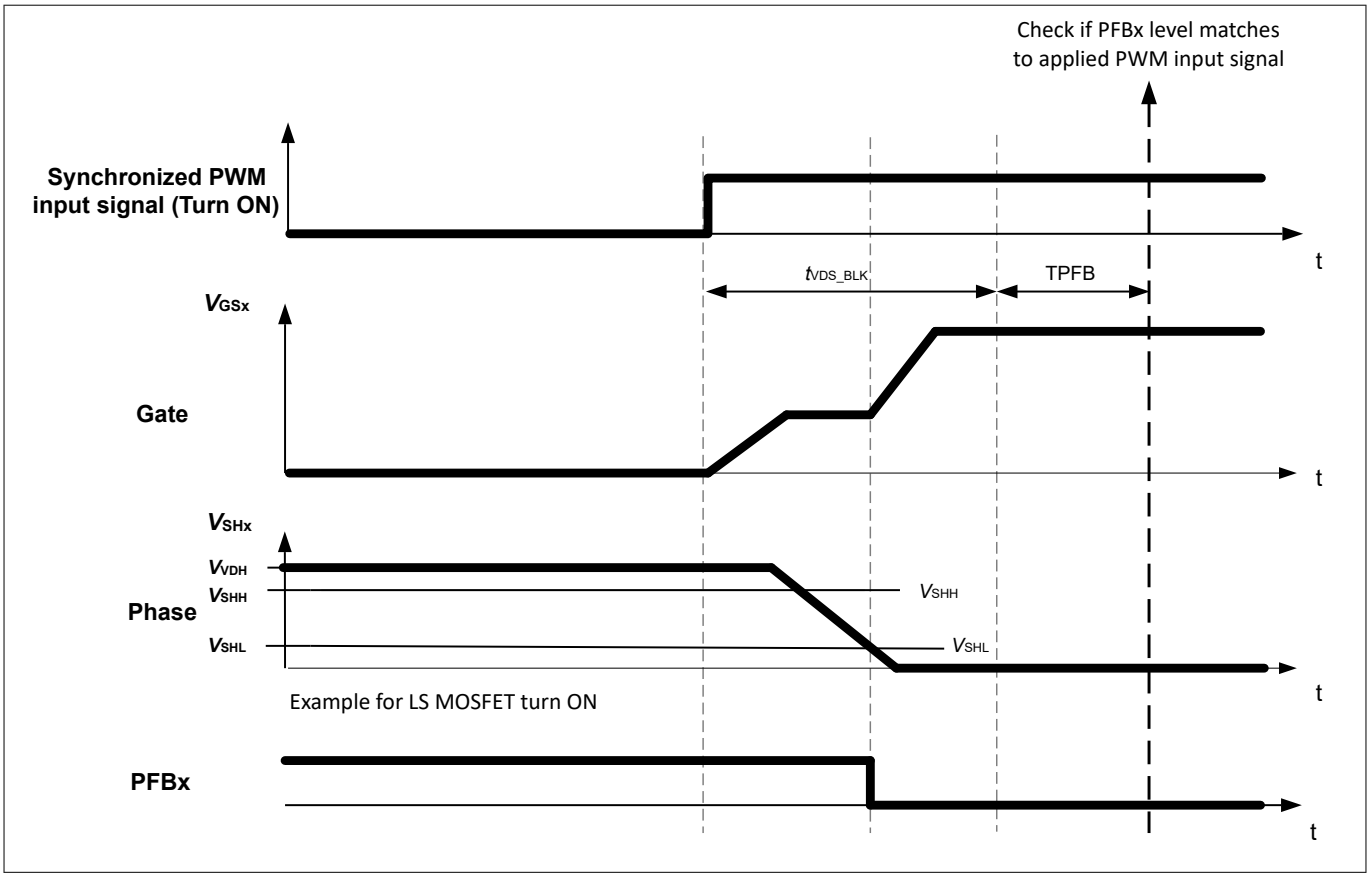

Figure 43 Example: PFB monitoring feature for the LS output stage

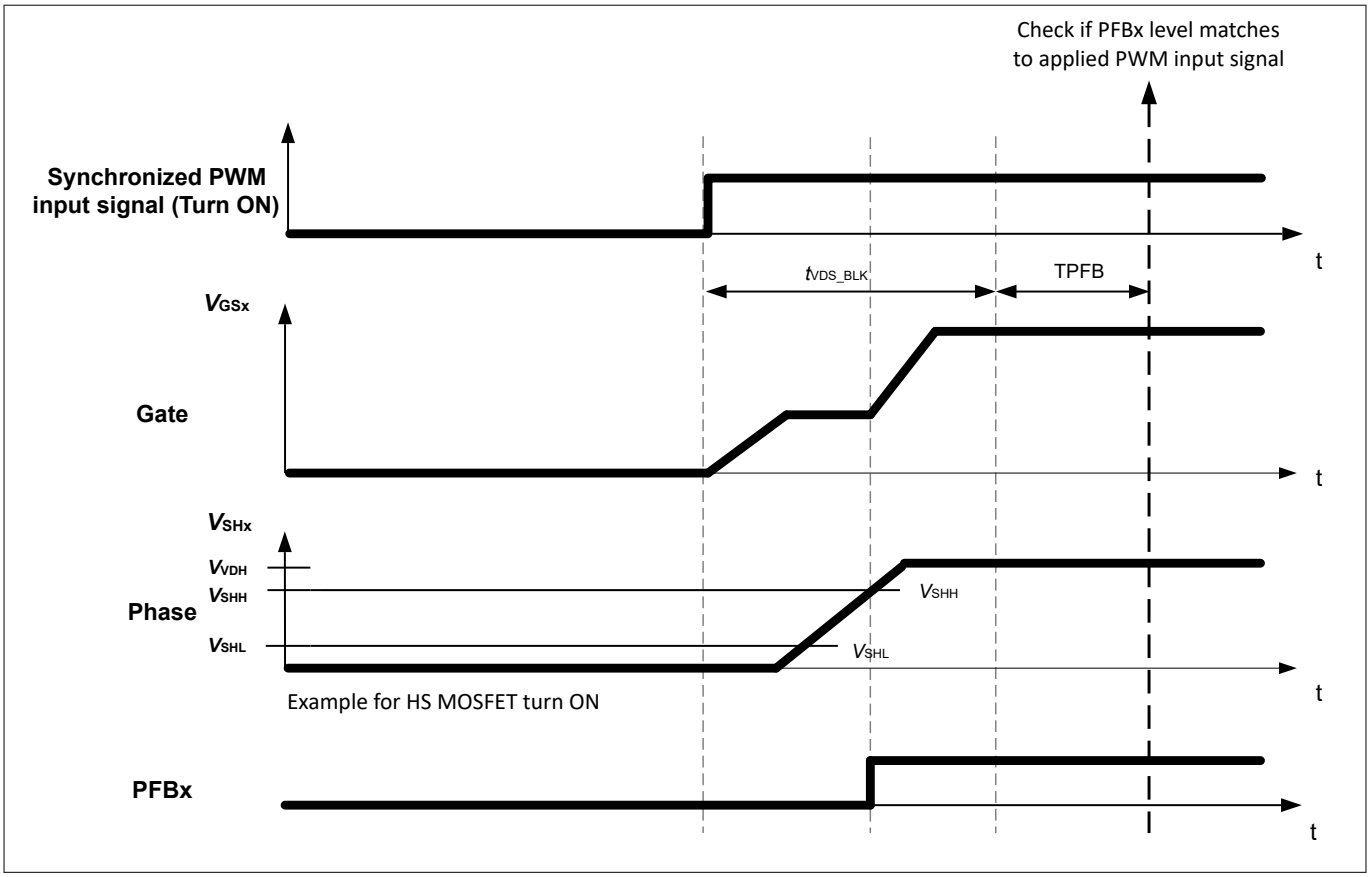

Figure 44 Example : PFB monitoring feature for the HS output stage

1.6.5.1 PFB "high" counter feature

The device includes a counter to measure the PFBx "high" time. The feature is enable for each phase in case the half-bridge is enabled (HBx_EN = 1).

If $V_{SHx} > V_{SHH}$, the counter starts to count until $V_{SHx} < V_{SHL}$. The value for each phase is stored in associated register PHASEx_CNT in bit field PFBx_H_CNT. If $V_{SHx} > V_{SHH}$ for longer than the maximum counter time, then $0x0FFF_H$ is written to PFBx_H_CNT. The clock frequency of the counter is f_{PFB_CNT} (P_DIAG_08_02).

The updated counter value can be read by the microcontroller once CNTx_RDY status bit is set to "1". When the internal CNTx counter is restarted, then the CNTx_RDY bit is cleared but the PFBx_CNT is kept until an updated counter value is available.

Each time a measured PFBx "high" time is written by the device into bit field PFBx_H_CNT, the PFBx_CNT_UPD bit is set to "1" to signalize an updated value. Bit PFBx_CNT_UPD can be cleared by SPI clear by write command by the microcontroller. This mechanism is used to check if PFBx_H_CNT has been updated since last SPI clear command.

***Note**: In case CNTx_RDY status bits are not used for read-out by the microcontroller it is recommended to read the PFBx_H_CNT counter register during low-side output stage ON phase.*

The PFBx "high" counters can be used by the microcontroller to check if the phase switching follows the applied duty cycle at the PWM input pins. The microcontroller accesses the three PFBx "high" counters and counter ready bits in registers PHASE1_CNT, PHASE2_CNT, PHASE3_CNT by three SPI read-out commands. The microcontroller receives a "high" counter value for each phase, which can be used to check and confirm if the phases are following the PWM signal and duty cycle. Since the SPI communication and read-out commands may happen asynchronously to the motor control scheme, the received PFBx "high" counters represent a snapshot of an applied switching period. The CNTx_RDY bit indicates if the "high" counter of the associated

phase is still counting or if the phase is "low" and the counter value is the most recent. The following figure shows an example.

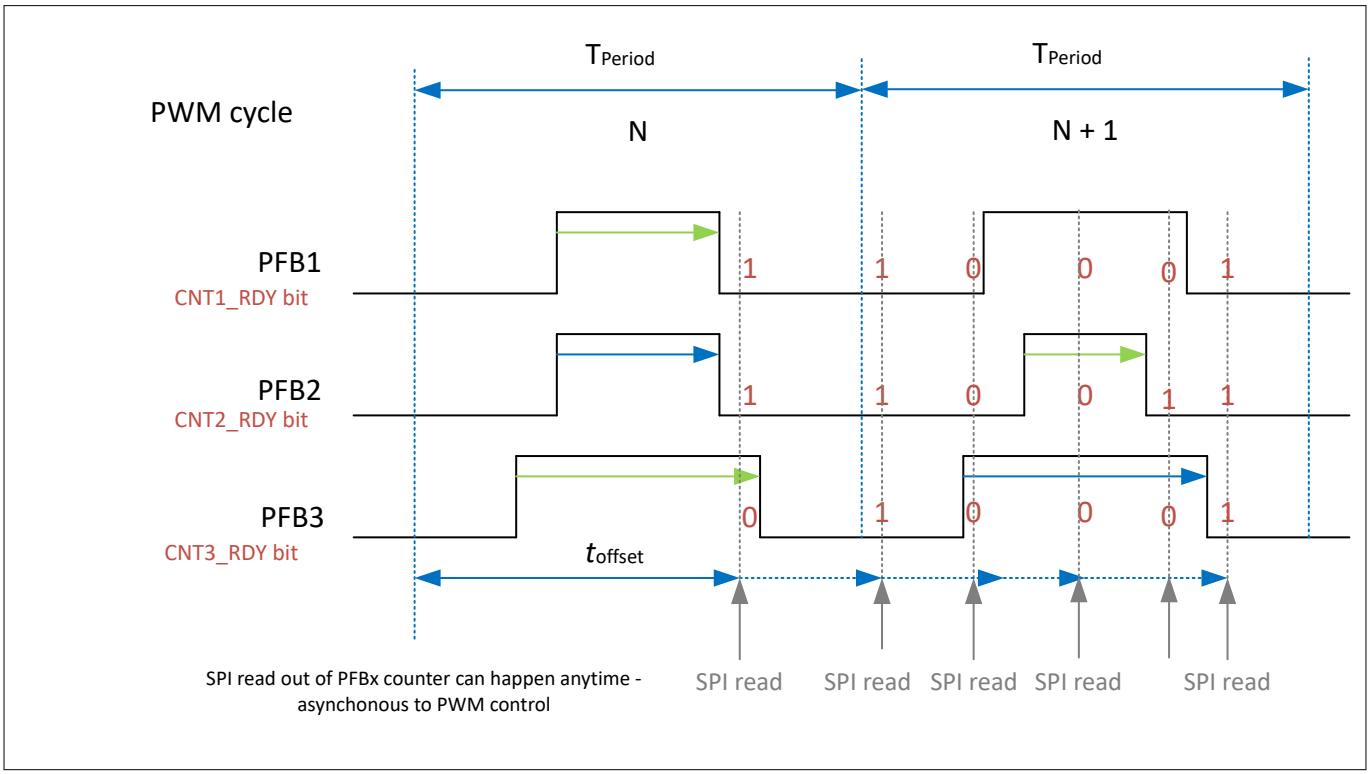

Figure 45 Example: PFBx "high" counter read-out indicating the duty cycle

The device includes three separate PFBx counter update bits (PFBx_CNT_UPD) for each PFBx status register PFB1_H_CNT, PFB2_H_CNT and PFB3_H_CNT. The PFBx_CNT_UPD bit set to “1” by device when a counter measurement has finished and PFBx_H_CNT value is written to respective PFBx status register. PFBx_CNT_UPD bit is set to "1" by the device in case an updated value of the PFBx_H_CNT is written by the device in the respective PFBx status register. The microcontroller has to reset the PFBx_CNT_UPD update bit to "0" by SPI write command.

This mechanism can be used by the microcontroller to verify the PFBx counters are not stuck but continuously updated by check of PFBx_CNT_UPD bit during SPI read command of PFBx status registers.

1.6.5.2 PFBx direct access on CSO pin

The state of the SHx phases can be evaluated by the microcontroller at CSO pin of the device by redirecting the phase feedback (PFBx) signal to CSA output pin. PFBx state depends on the fast comparator thresholds V_{SHL} and V_{SHH}:

- PFBx is set to "0" if $V_{SHx} < V_{SHL}$
- PFBx is set to "1" if $V_{SHx} > V_{SHH}$
- If $V_{SHx} > V_{SHL}$ AND $V_{SHx} < V_{SHH}$, then the previously detected state is shown at PFBx

The XOR (PFB1, PFB2, PFB3) function changes its state with every change of one PFBx signal.

By default the current sense amplifier function is visible at CSO output pin. The function of the CSO output pin can be modified by control bit CSO_MUX.

Table 17 CSO_MUX control bit settings

CSO_MUX control bit setting	Selected configuration
CSO_MUX = 000_B	Current sense amplifier function selected
CSO_MUX = 001_B	PFB1 state redirected to CSO output pin
CSO_MUX = 010_B	PFB2 state redirected to CSO output pin
CSO_MUX = 011_B	PFB3 state redirected to CSO output pin
CSO_MUX = 100_B	XOR of PFB1, PFB2 and PFB3 redirected to CSO output pin

The PFBx signal redirected to SDO and CSO pin is the real time SHx monitoring by the fast comparator V_{SHL} and V_{SHH}.

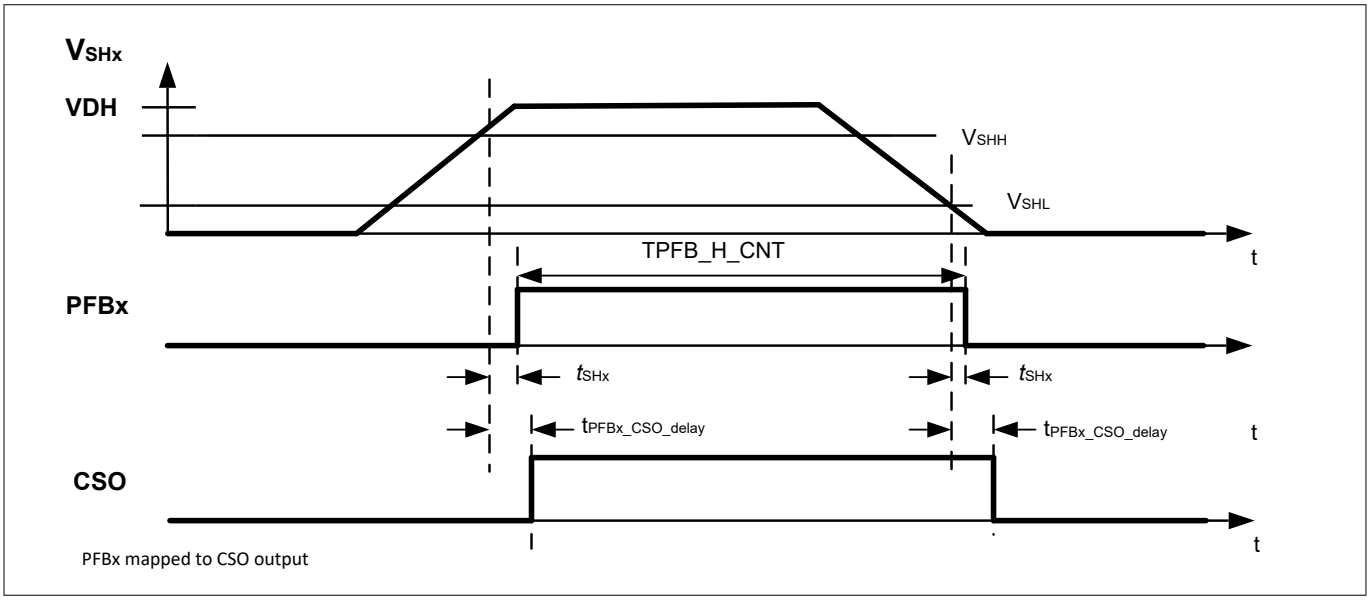

Figure 46 Timing diagram - PFBx mapped to CSO output

1.6.6 Off-state monitoring

The device offers off-state diagnostics to check motor connections and to detect if the phase pins (SHx) are shorted to SLx/GND or to VDH or if they are open.

To support the off-state diagnostics, the gate driver of each MOSFET provides pull-up and pull-down currents at the SHx pins.

The pull-up current sources are active in case the following conditions are all met:

- The charge pump is active (CP_EN = 1)
- The half-bridge is enabled (HBx_EN = 1)
- Device is in normal operation mode
- The off-state diagnostics is enabled by a control bit (OFF_DIAG_EN = 1)

The following failures can be detected:

- Detection of open load conditions
- SHx shorted to VBAT
- SHx shorted to GND

The pull-down currents of each gate driver are activated by the control bits HBxIDIAG. The following table shows the possibilities for configuration and their related control bits.

Table 18 Configuration options

Configuration option	Related SPI control or status bits	Comment
Enable/disable off-state diagnostics	OFF_DIAG_EN	
Half bridge pull-down current at low-side	HBxIDIAG	
SLx comparator state for phase x	VSHx_L	
VDH comparator state for phase x	VSHx_H	
PFBx state	PFBx	PFBx can optionally be read-out via SPI

If the charge pump module or not all half-bridges have been enabled before setting OFF_DIAG_EN = 1, no error will be signalized and the result of the diagnostics is not reliable. The device does not run an internal check on the configuration for off-state diagnostics and correct configuration has to be ensured by the microcontroller.

In case OFF_DIAG_EN = 0 , the HBxIDIAG configuration bits have no effect when set to 1 (SPI write command is accepted, bit level updated by the device but not propagated to the gate drivers). While the OFF_DIAG_EN = 1 (off-state diagnostics enabled):

- The gate drivers are forced into active discharge state (PWM control inputs are masked)
- AND internal pull-down current is controlled by the configuration bits HBxIDIAG

***Note**: If external bridge failure tests are implemented (such as: pull-down and pull-up resistors), it is recommended to dimension external resistors higher ohmic than internal off-state diagnostic currents.*

1.6.6.1 Interpreting the results of the off-state diagnostics

In normal operation mode, during the off-state diagnostic check (provided HBx_EN = 1, CP_EN = 1, OFF_DIAG_EN = 1), the level of the output voltage SHx can be read via the status bits VSHx_L and VSHx_H:

- VSHx_L = 0_B AND VSHx_H = 0_B : VSHx low ($V_{SHx} < V_{SHL}$)
- VSHx_L = 1_B AND VSHx_H = 1_B: VSHx high ($V_{SHx} > V_{SHH}$)

Based on the HBxIDIAG settings (activation of the pull-down currents of LSx MOSFETs) the SHx level can be controlled to high or low and read-out by the microcontroller via VSHx_H and VSHx_L status bits. Depending on the read-out, the following failures can be differentiated:

- MOSFET short circuit to GND
- MOSFET short circuit to VSCP
- Open load (disconnected motor)

A sequence of four configurations has to be performed by the microcontroller via SPI for the pull-down currents. The results are also interpreted strictly by the microcontroller:

- Configuration 1: HB1IDIAG, HB2IDIAG, HB3IDIAG are all disabled
- Configuration 2: HB1IDIAG, HB2IDIAG are enabled while HB3IDIAG is disabled
- Configuration 3: HB2IDIAG, HB3IDIAG are enabled while HB1IDIAG is disabled
- Configuration 4: HB1IDIAG, HB3IDIAG are enabled while HB2IDIAG is disabled

The results are interpreted by the microcontroller according to the table below:

The table shows an example using status bits VSHx_L of each phases for off-state diagnostics. The off-state diagnostics can be implemented in analogously way using status bits VSHx_H.

Table 19 Example using status bits VSHx_L

Load condition (failure scenario)	Config	HB1IDIAG	HB2IDIAG	HB3IDIAG	VSH1_L	VSH2_L	VSH3_L
Normal conditions (expected outputs)	1	OFF	OFF	OFF	HIGH	HIGH	HIGH
	2	ON	ON	OFF	LOW	LOW	LOW
	3	OFF	ON	ON	LOW	LOW	LOW
	4	ON	OFF	ON	LOW	LOW	LOW
One phase short to VSCP	1	OFF	OFF	OFF	HIGH	HIGH	HIGH
	2	ON	ON	OFF	HIGH	HIGH	HIGH
	3	OFF	ON	ON	HIGH	HIGH	HIGH
	4	ON	OFF	ON	HIGH	HIGH	HIGH
One phase short to SLx	1	OFF	OFF	OFF	LOW	LOW	LOW
	2	ON	ON	OFF	LOW	LOW	LOW
	3	OFF	ON	ON	LOW	LOW	LOW
	4	ON	OFF	ON	LOW	LOW	LOW
Open load phase 1 (SH1)	1	OFF	OFF	OFF	HIGH	HIGH	HIGH
	2	ON	ON	OFF	LOW	LOW	LOW
	3	OFF	ON	ON	HIGH	LOW	LOW
	4	ON	OFF	ON	LOW	LOW	LOW
Open load phase 2 (SH2)	1	OFF	OFF	OFF	HIGH	HIGH	HIGH
	2	ON	ON	OFF	LOW	LOW	LOW
	3	OFF	ON	ON	LOW	LOW	LOW
	4	ON	OFF	ON	LOW	HIGH	LOW
Open load phase 3 (SH3)	1	OFF	OFF	OFF	HIGH	HIGH	HIGH
	2	ON	ON	OFF	LOW	LOW	HIGH
	3	OFF	ON	ON	LOW	LOW	LOW
	4	ON	OFF	ON	LOW	LOW	LOW

The phase pins SHx are monitored by the two comparators with thresholds V_{SHL} and V_{SHH}.

The SHx level is indicated via the status bits VSHx_L and depending on the pull-down current configuration, (enabled or not) the correct functionality of SHx pins can be detected.

During this test, the target is to enable 2 pull-down currents at a time and check if the SHx can be pulled low or not by this internal current. By design, it ensures that 2 x I_{PDDIAG} current is always stronger (higher) than 3 x I_{PUDIAG} current (which is always ON - the total current of 3 HS gate drivers in active discharge phase).

1.6.7 CSA monitoring

The current sense block includes several monitoring features and functions:

- CSA overcurrent monitoring, see CSA overcurrent monitoring

- Internal CSA supply monitoring, see CSA supply monitoring
- CSA gain accuracy test, see CSA gain check function

1.6.7.1 CSA overcurrent monitoring

The device monitors the voltage drop over the external shunt via pins CSIP and CSIN. The voltage drop is amplified by the configured gain setting and resulting amplified signal is indicated at CSA output pin CSO. The direction of the current sense amplifier is configurable by bit CSA_DIR.

Gain settings are configurable for each CSA independently by bits CSA_GAIN.

If the resulting output voltage at pin CSO reaches the configured overcurrent threshold for longer than the configured overcurrent filter time, then overcurrent failure is detected.

Overcurrent filter time is configurable by bits CSA_TFOC. Overcurrent threshold is configurable by bits CSA_OC_TH.

The failure reaction of overcurrent failure detection is configurable by bit CSA_OC_FM.

For unidirectional CSA configuration an overcurrent event is detected if:

- CSO is above configured V_{OCTHx_Unidir} for t > t_{fOC}

For bidirectional CSA configuration an overcurrent event is detected if:

- CSO is above configured V_{OCTHx_BidirH} for t > t_{fOC} OR
- CSO is below configured V_{OCTHx_BidirL} for t > t_{fOC}

Overcurrent thresholds are visualized for unidirectional CSA configuration in Figure 47 and for bidirectional CSA configuration in Figure 48.

The following table shows the possibilities for configuration and its related control bits.

Table 20 Configuration options

Configuration option	Related SPI control bit	Related SPI status bit
Enable disable current sense amplifier	CSA_EN	
CSA direction configuration (unidirectional/bidirectional)	CSA_DIR	
CSA overcurrent threshold	CSA_OC_TH	
CSA overcurrent filter time	CSA_TFOC	
CSA overcurrent failure behavior	CSA_OC_FM	CSA_OC
CSA gain setting	CSA_GAIN	
CSA gain test enable/disable	CSA_GAIN_TST	

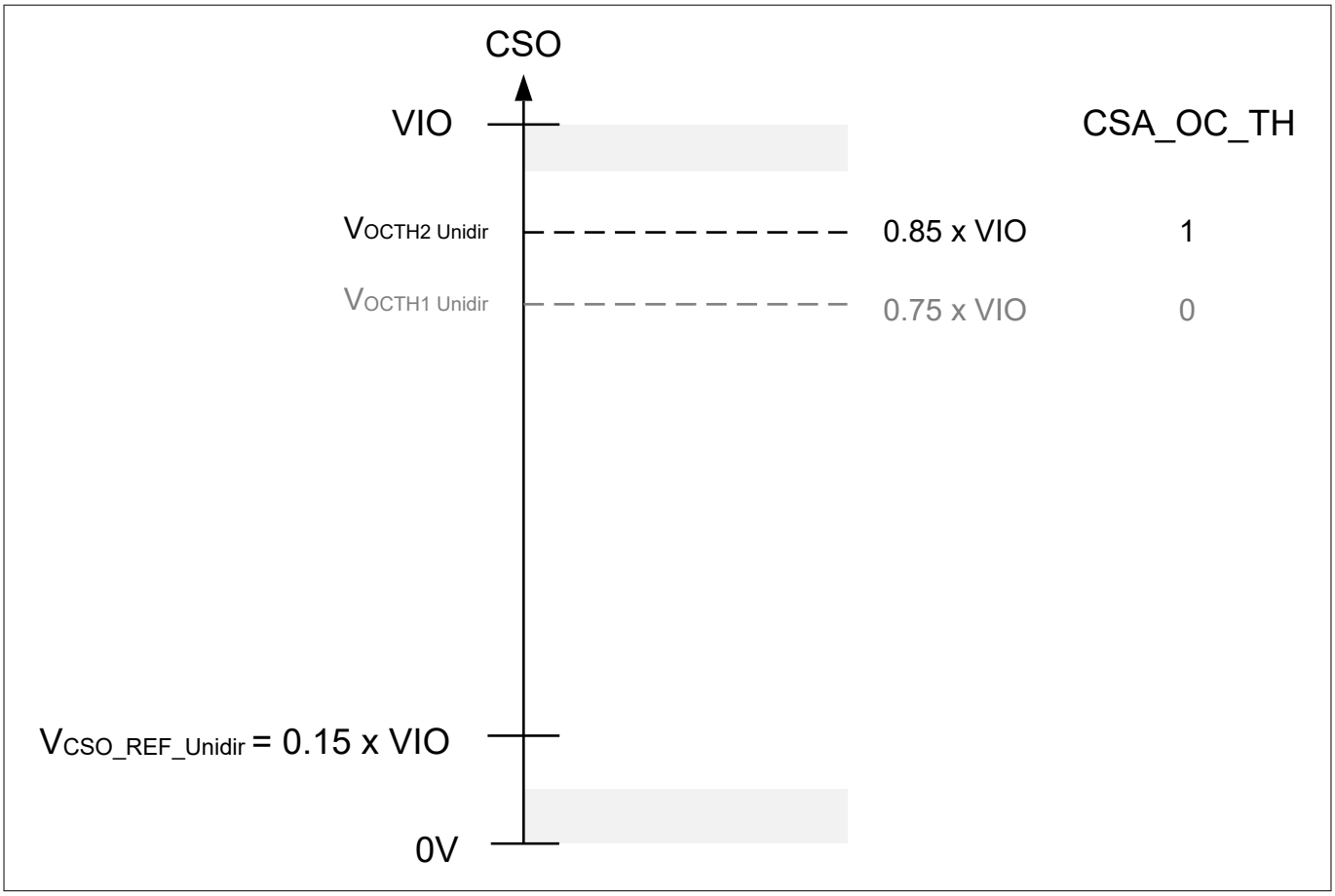

Figure 47 Overcurrent threshold unidirectional diagram

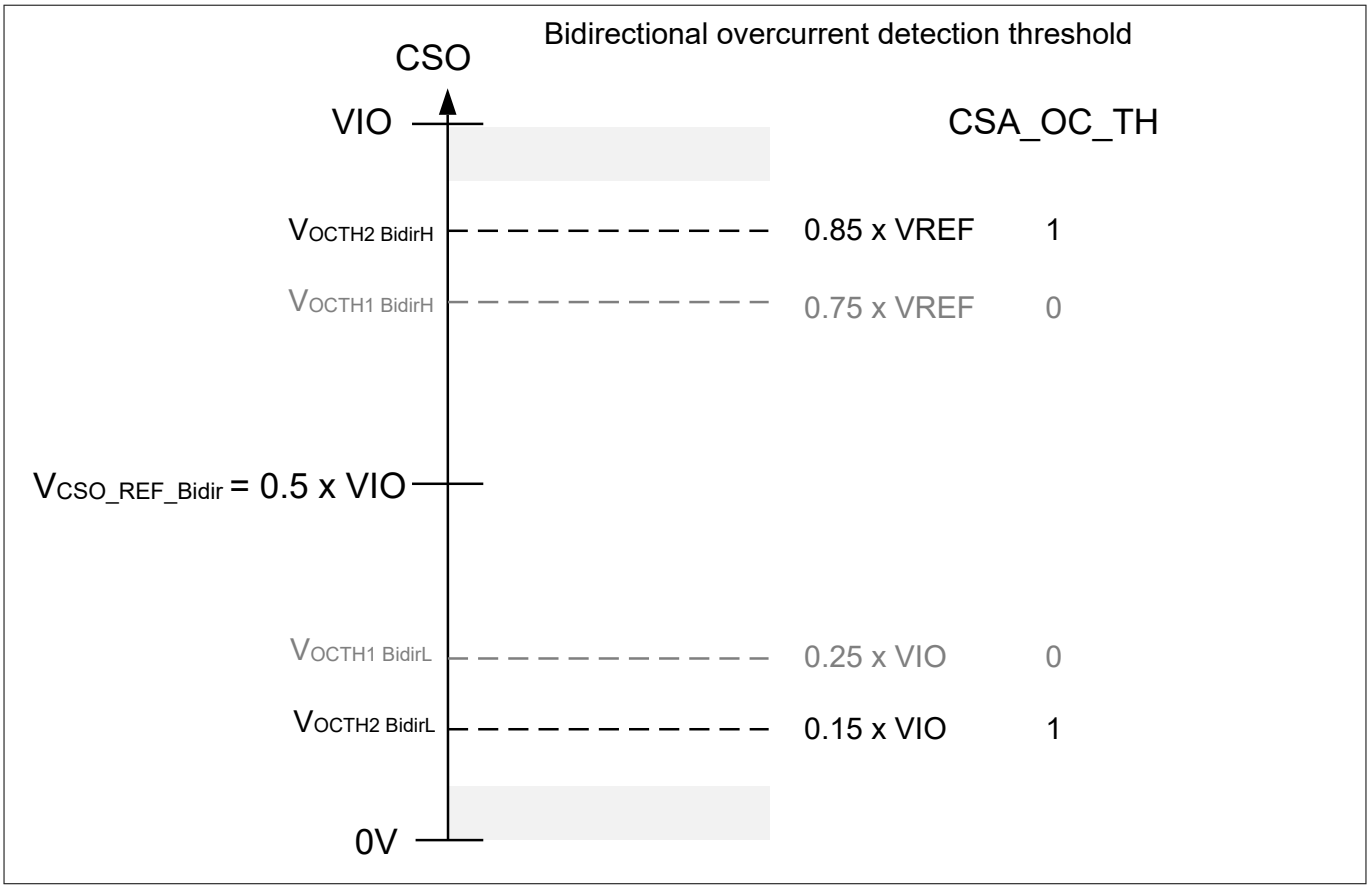

Figure 48 Overcurrent threshold bidirectional diagram

1.6.7.2 CSA supply monitoring

The internal supply for the current sense amplifier is monitored. Failure behavior when undervoltage is detected follows the configuration of CSA_SUP_UV_FM.

If an undervoltage is detected at the CSA supply regulator then:

- The configured failure behavior, as defined by CSA_SUP_UV_FM, is executed
- CSA module is disabled (CSA_EN = 0)
- The error detection bit CSA_SUP_UV for supply undervoltage is set

1.6.7.3 CSA gain check function

The device offers a feature to check the applied gain at CSO pin by the microcontroller. Therefore, an internally generated reference voltage $V_{CSA_GAIN_ACC}$ is overimposed at the selected input pins CSIP and CSIN. This feature can be enabled in normal operation mode or power-up mode for the CSA module which is enabled by CSA_EN = "1". To trigger the feature, the applicable CSA channel is selected by bit CSA_GAIN_TST by the microcontroller. The differential voltage $V_{CSA_GAIN_ACC}$ is internally overimposed at CSIP/CSIN inputs of the current sense amplifier and multiplied with configured gain setting. After t_{CSA_SET}, the microcontroller can check CSO voltage if it is in the expected range. It is recommended to subtract the CSO voltage with CSA_GAIN_TST = "0". The test can be performed as well during run time, since an internal differential voltage is added on top of the external one.

1.6.8 Supply monitoring

The device includes three system supply monitoring features:

- VIO supply monitoring: supply of internal digital core, current sense amplifier and I/O pins
- VSCP supply monitoring: supply of charge pump and gate driver output stages
- VDH supply monitoring: reference supply pin for drain-source overvoltage monitoring and PFB monitoring

1.6.8.1 VIO supply monitoring

The VIO pin is the supply of the internal logical core of the device. VIO supply is the same supply as the microcontroller supply and is monitored for under- and overvoltage. The following table shows the possibilities for configuration and their related control bits.

Table 21 Configuration options

Configuration options	Related control or status bit	Comment
VIO configuration (3.3 V/5 V supply)	VIO_CFG	Protected control bit - only configurable in power-up mode. Mandatory to be configured before entering normal operation mode
Overvoltage detection of VIO	VIO_OV	
Undervoltage detection of VIO	VIO_UV	Can only be detected in case $V_{VIO} > V_{VIO_PORf}$

In case VIO_CFG configuration bits are set to 00_B or 11_B, the device is locked in power-up mode (no transition to normal operation mode possible).

Independent of the VIO_FM configuration bits, in case of an VIO undervoltage event in normal operation mode the device will:

- Set the VIO_UV status bit
- Set SDO pin to tri-state
- Block input digital IO pins: IHx_N, ILx
- Not accept additional SPI commands
- Enter safe state
- Disable the current sense amplifier. If CSA recovers after VIO undervoltage event is configurable by control bit CSA_REC

As soon as the VIO_UV event is not present anymore, the device accepts SPI communication.

In case of VIO overvoltage detection in normal operation mode the device will:

- Set the VIO_UV status bit
- Enter safe state
- Set SDO pin to tri-state

The digital input pins are not blocked (PWM operation is possible) and CSA remains enabled.

1.6.8.2 VSCP supply monitoring

The bridge and charge pump supply status at the VSCP pin is monitored for under- and overvoltage. Both VSCP undervoltage and overvoltage failure reactions are fixed to latched error 1 (LE1) and additionally, in both cases the charge pump is deactivated.

With control bits CP_REC_UV and CP_REC_OV the user can decide if the charge pump is re-enabled automatically in case VSCP undervoltage or overvoltage disappears.

1.6.8.3 VDH supply monitoring

The device includes a VDH undervoltage detection feature. VDH undervoltage detection function is enabled in power-up mode and normal operation mode. Failure reaction is fixed to warning (W).

In case of failure detection the status bit VDH_UV is set to "1". The function can be used to:

- Check the correct function of the external safety switch between VDH and VSCP (in case used in the application)
- Latent fault detection for loss of drain-source overvoltage detection for HSx MOSFET

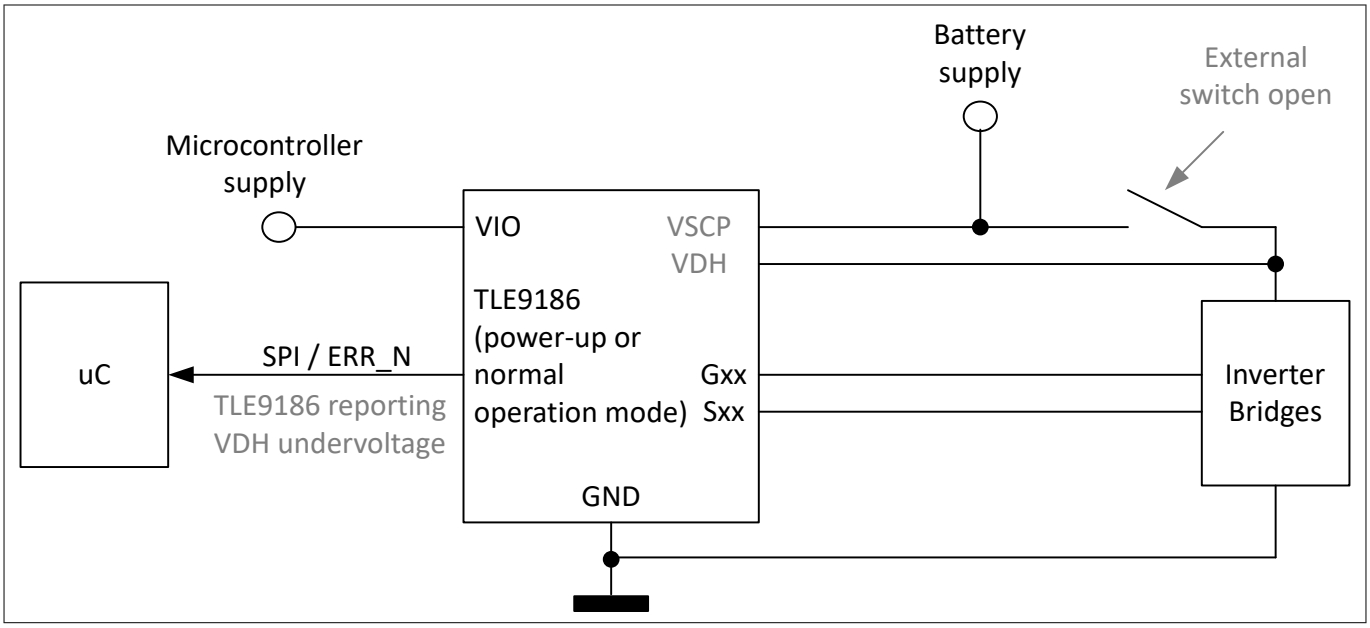

Figure 49 Example - VDH undervoltage detection with external switch

1.6.8.4 VCPH monitoring

To assure enough supply voltage to drive the output stages, the bridge driver includes a VCPH pin undervoltage monitoring function. The differential voltage between pin VCPH and VSCP is monitored for undervoltage. The undervoltage detection threshold of VPCH pin is configurable by control bit CP_UV_TH. Failure reaction of VCPH undervoltage detection is not configurable and fixed to latched error 1 (LE1).

Table 22 Settings

Setting	Nominal configured VCPH undervoltage threshold	Comments
CP_UV_TH = 0	8.5 V	Typical use case
CP_UV_TH = 1	7.5 V	Recommended for low VSCP supply (low supply configuration)

To avoid too much overdrive supply voltage at VCPH pin, the device includes as well an over-voltage comparator for VCPH supply monitoring. The VCPH voltage is monitoring against a VCPH overdrive target voltage threshold and is used for the charge pump clock gating scheme. In case the differential voltage VCPH - VSCP is above the VCPH overdrive target voltage threshold (approx. 15 V), the charge pump clock is stopped for the second charge pump stage and is restarted when VCPH is detected below VCPH overdrive target voltage threshold. No additional failure reaction is triggered and no SPI status bit is set.

The correct function of both VCPH undervoltage and VCPH overvoltage comparators can be tested by dedicated charge pump monitoring self-test.

1.6.9 Internal IC supervision functions

The device includes two internal IC monitoring functions:

- Internal clock monitoring: the internal clock of the device is monitored
- Internal regulator undervoltage monitoring: internal regulator is required for the internal digital core

If the internal clock is not working or an undervoltage of the internal regulator is detected by the device, then:

- Power ON reset occurs
- The device enters safe state
- The device re-initializes the power-up sequence
- After t_{core_up} SPI commands are accepted while VIO is within the functional range
- All registers are reset to the default values
- Device in power-up mode, internally forced safe state

1.6.10 Window watchdog

An integrated window watchdog supervises the integrity of the communication with the microcontroller. The watchdog is used to monitor the software execution of the microcontroller and to detect and report errors or loss of SPI communication via SPI status registers or ERRN. Failure behavior is configurable by control bits WD_FM.

1.6.10.1 Usage of window watchdog function

In order to enable the watchdog function, the WD_EN bit has to be set to "1" in register CONFIG_SECURED in power-up mode. A correct SPI SDI frame write command to the register WD_CFG is a successful servicing of the window watchdog. Window watchdog period and watchdog error counter is configurable via SPI by the microcontroller in power-up mode and normal operation mode. Window watchdog ratio is fixed to 40% open window period and 60% locked window period.

The window watchdog period is configured by register bits WD_PER in register WD_CFG. The window watchdog clock counter (WD_CLK_CNT) counts the internal clock cycles between two consecutive correct SPI window watchdog servicing commands. The window watchdog error counter (WD_CNT) counts failed or missed window watchdog serving commands. The result of the error counter and the clock counter is stored in the registers SPI_STAT and WD_CLK_CNT. The following table shows the possibilities for configuration and their related control and status bits.

Table 23 Configuration options

Configuration option	Related control bit	Related SPI status bit (diagnostics)
Enable window watchdog	WD_EN	
Window watchdog period	WD_PER	
Window watchdog error counter	WD_FAIL	WD_CNT
Window watchdog configuration checksum bit	CHECKSUM	
Window watchdog failure behavior	WD_FM	WDE, WDLE
Distance between two consecutive correct window watchdog service routines		WD_CLK_CNT

Watchdog failure behavior is configurable by bits (WD_FM).

Following configuration possibilities are available:

- Warning (W)
- Latched error 1 (LE1)

HBx_EN bits are automatically cleared if a window watchdog error has been detected and failure reaction for WD is set to LE1 (WD_FM=00b).

A checksum bit is part of the SPI command to trigger the watchdog and to set the watchdog setting. The sum of the 16 data bits in the register WD_CFG needs to have even parity. This is realized by either setting the bit CHECKSUM to 0 or 1. If the checksum is wrong, then:

- The SPI command is ignored, in case the watchdog is not triggered or the settings are not changed and SPI error is reported via OFC = 1 and LFOK = 0 status flags
- AND watchdog is not triggered
- AND watchdog settings are not changed in the WD_CFG register

A wrong checksum setting when sending a write SPI command to WD_CFG register will cause an SPI failure detection independent of if window watchdog feature enabled or not.

1.6.10.1.1 Correct and incorrect window watchdog servicing

The window watchdog is implemented with a fixed ratio between open window and closed window timings:

- 40% open window
- 60% locked window

A correct watchdog service is defined as a valid SPI write command by the microcontroller in the configuration register WD_CFG within the safe trigger area. The timing diagram of correct window watchdog trigger area is shown in figure below.

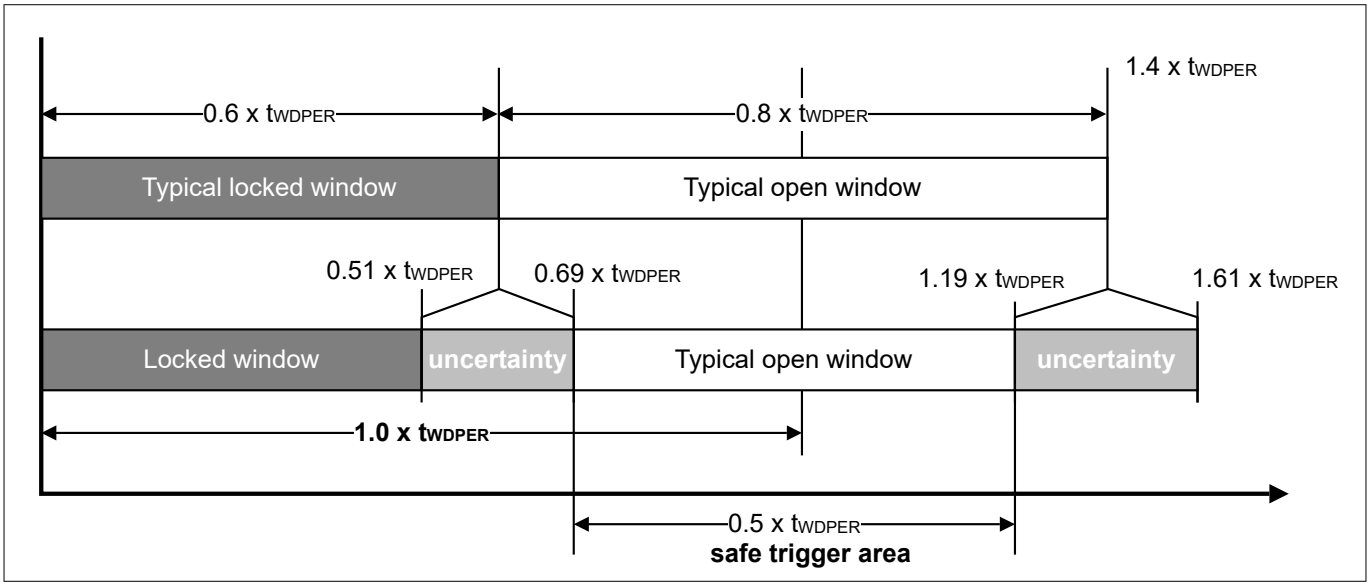

Figure 50 Window watchdog servicing timing diagram

A window watchdog fail counter is implemented to configure the number of watchdog fails when the configured failure reaction of the device is triggered. The window watchdog fail counter is configurable by WD_FAIL bits in the WD_CFG register. The status of watchdog fails counter can be read out by the microcontroller in the SPI_STAT status register on bits WD_CNT. These bits are read-only bits and cannot be cleared by SPI command. Once the WD_CNT counter has reached the configured number of watchdog fails (WD_CNT decimal = 2 x WD_FAIL decimal):

- The WDLE (watchdog latched error) status bit set to "1" in SPI_STATS status register
- AND triggers the configured IC failure reaction to watchdog failure

The failure reaction is configurable by the WD_FM bits in the FAILURE_CFG register. In case WDLE is set and WD_FM = 0_B, the HBx_EN bits are set to "0" by the device.

In case of correct window watchdog servicing, then:

- Internal clock counter will be stored into the register WD_CLK_CNT
- Internal clock counter is restarted
- The status bit WDE is set to "0" in the SPI_STAT register
- DW global status bit is set to "0"
- Error counter WD_CNT is decremented by 1
- Locked window is started

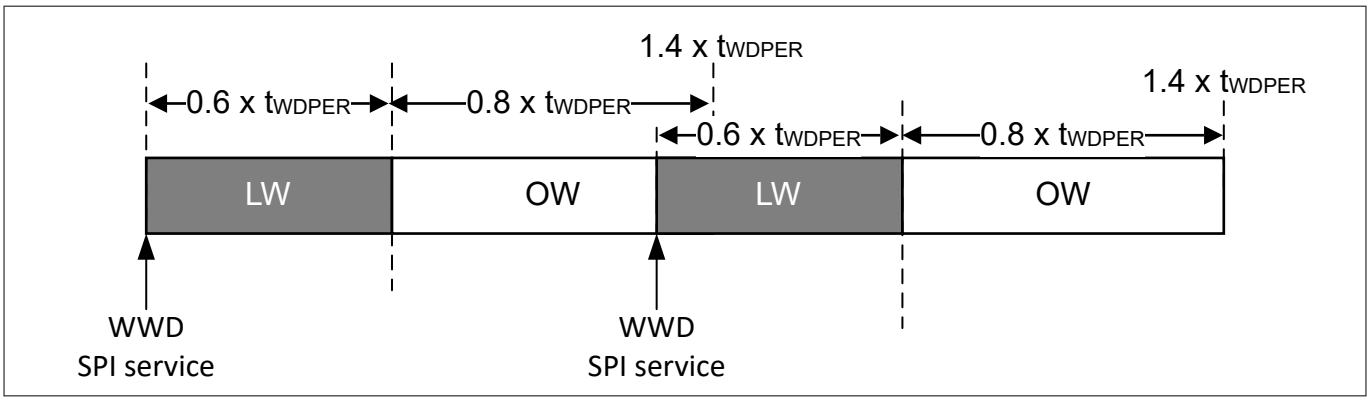

Figure 51 Example for correct window watchdog service

An incorrect window watchdog trigger is defined as:

- A correct SPI write command in the WD_CFG register during watchdog locked window
- OR a missing correct write SPI command in the watchdog open window

In case window watchdog servicing fails either by servicing within locked window watchdog period or missing correct service during the complete open window watchdog period, then:

- The window watchdog is restarted with an open window
- The error counter WD_CNT is incremented by 2
- The clock counter will continue counting until correct WD servicing is performed. 0xFFFF will be written into the register bits WD_CLK_CNT if the counter reaches its maximum value

As soon as the first window watchdog service fails the window watchdog error bit WDE bit is set to "1". Additionally, any incorrect window watchdog servicing will set the global status device warning (DW) flag. Any correct window watchdog servicing will reset the global status device warning (DW) flag, unless WDLE status bit is set. If the error counter reaches the configured limit in defined by bits WD_FAIL in register WD_CFG the configured failure behavior defined by bit WD_FM is executed and watchdog latched error WDLE status bit is set. WDE and WD_CNT are a read-only SPI register bit. It is automatically updated by the device.

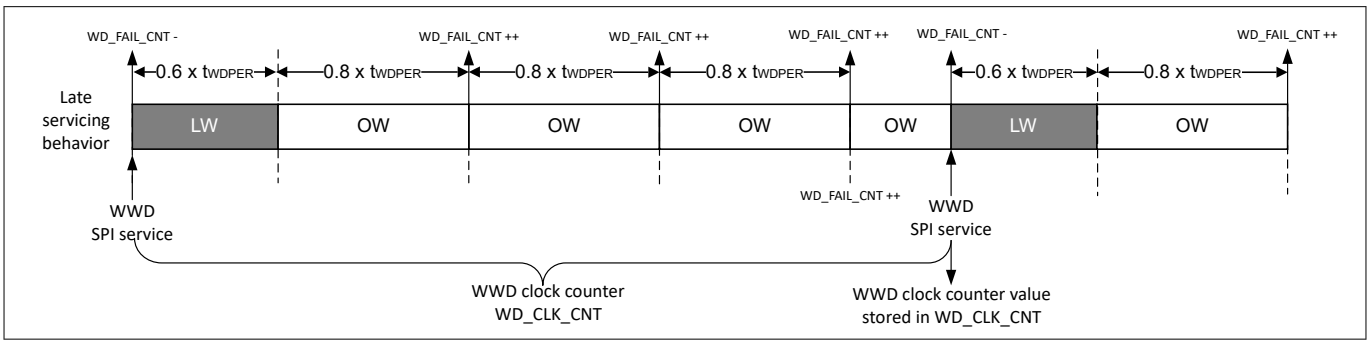

Figure 52 Example for incorrect window watchdog service and clock counter storage

1.6.10.1.2 Enable window watchdog device behavior

The microcontroller can enable or disable the window watchdog by SPI write command only in device power-up mode. The control bit to enable or disable the window watchdog is WD_EN in secured configuration register CONFIG_SECURED:

- WD_EN = "0" , watchdog is disabled
- WD_EN = "1" , watchdog is enabled

As soon as the window watchdog is enabled in power-up mode by setting WD_EN = "1" configuration bit, the watchdog starts with open window. During open window the watchdog can be serviced by valid SPI window watchdog service command by the microcontroller. The figure below shows the behavior of the device once window watchdog function is enabled.

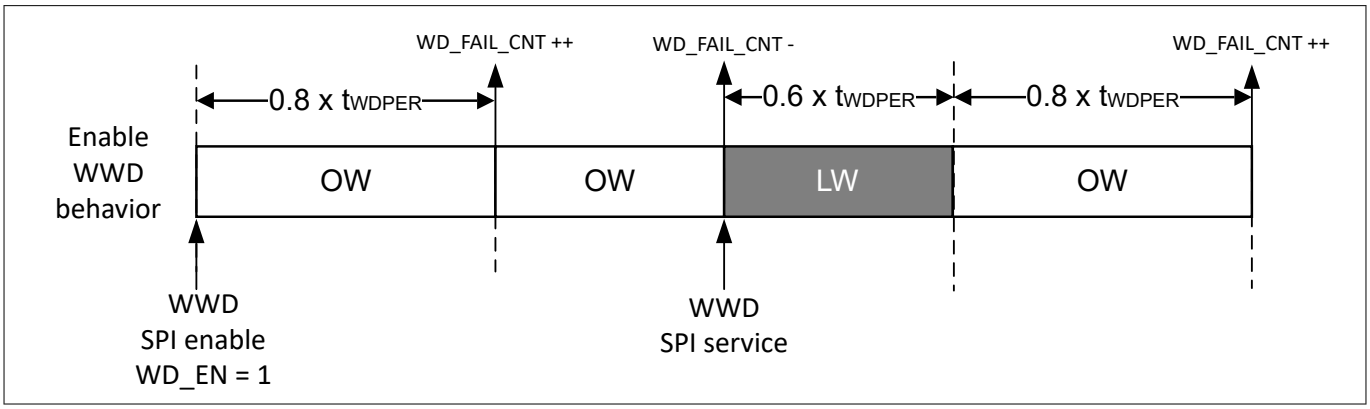

Figure 53 Enable window watchdog function

1.6.10.1.3 Disable window watchdog

By default the window watchdog function is disabled and hence all related status and counter bits related to window watchdog function are set to "0". If window watchdog function is disabled by WD_EN = 0, then:

- All status bits are cleared (WDE = 0, WD_CNT = 0, WD_CLK_CNT = 0)
- AND internal clock and fails counters are reset
- WDLE status bit will not be cleared if already set to "1", until an SPI clear by write command

In case window watchdog is disabled, then all related window watchdog status bits are set to "0" and kept "0". In case the status bit is set to "1", it will not be automatically reset by deactivation of the feature.

1.6.10.2 Window watchdog clock counter

The window watchdog clock counter counts the internal clock cycles between two consecutive correct SPI window watchdog serving commands. The internal watchdog clock counter is implemented to give the microcontroller the possibility to measure the internal bridge driver oscillator frequency – value and accuracy. For every valid window watchdog servicing command, the window watchdog clock counter result is stored in 16 bit register WD_CLK_CNT. The result is stored until the next valid window watchdog servicing.

The window watchdog clock counter is restarted if:

- A correct watchdog trigger via SPI write command is received OR
- A WDLE = 1 cleared via SPI command is received

If the watchdog clock counter reaches a maximum value $0xFFFF_H$ before a correct watchdog servicing:

- The window watchdog clock counter is stopped
- The value $0xFFFF_H$ is stored in the WD_CLK_CNT status register

The watchdog clock counter restarts with the next valid watchdog servicing event. The watchdog clock counter counts the number of internal clock cycles on nominal 4.8µs period (f_{CLKint} = 75Mhz) in between two

consecutive correct watchdog servicing SPI commands. For a configured WD_PER = 111 (256 ms) the WD_CLK_CNT is expected to report $0xD055_H$ for an nominal internal oscillator frequency f_{CLKint}.

1.6.10.3 Resume normal operation from watchdog error

If the failure reaction of the window watchdog is configured as latched error 1 (LE1), there are two possibilities to reactivate the output stages and to recover from window watchdog error detection.

Option 1: the device reactivates the output stages in normal operation mode, if the microcontroller:

1. Performs SPI CLR_STATS command. This leads to WDLE = "0"
2. Reactivates the half-bridges by setting half-bridge mode HBx_EN = 1

Option 2:

1. The microcontroller sets WDLE bit to "0" by SPI write command. This leads to a restart of the window watchdog with open window
2. Reactivate half-bridges by setting half-bridge mode HBx_EN = 1

The WDLE status bit can be cleared:

- Via SPI clear by write command
- OR via SPI write command in register PWR_MOD_CFG bit CLR_STATS

1.6.10.4 Window watchdog internal clock frequency relationship

The window watchdog can be used to measure the internal clock frequency of the device f_{CLKint} of typ. 75 MHz.

To evaluate the internal clock frequency f_{CLKint} two consecutive correct window watchdog services are required. At every correct watchdog service via SPI write command in the WD_CFG register, the current value of the watchdog clock counter is stored in the WD_CLK_CNT status register.

The WD_CLK_CNT content does not change until the next correct watchdog trigger.

This internal watchdog clock counter is stored in the status register WD_CLK_CNT.

The watchdog clock counter counts the number of internal clock cycles on typ. 4.8 µs ticks in between two consecutive correct watchdog servicing (trigger) SPI commands.

Example:

- For a configured WD_PER = 110 (128 ms) the WD_CLK_CNT is expected to report $0x682A_H$ for an ideal internal oscillator frequency of 75 MHz (watchdog clock counter step of 4.8µs)

1.6.11 PWM monitoring

In bridge applications, it has to be assured that the external high-side and low-side MOSFETs are not turned ON at the same time. This could cause high current, high heat and potential destruction of the MOSFET, when for example, connecting directly the battery voltage to GND. Therefore, the bridge driver includes various PWM input pin monitoring features:

- Shoot through protection
- Cross current protection
- Input pattern violation monitoring
- PWM alternation monitoring

The cross-current protection and shoot-through protection is continuously enabled for each half-bridge as long as HBx_EN = 1. Figure 54 illustrates a summary of the protection and detection features.

The following table shows the possibilities for configuration and their related control bits. Figure 55 illustrates configuration possibilities.

Additionally the PWM input pins are monitored for alternating PWM turn on signals at IHx_N and ILx pins (see PWM alternation monitoring).

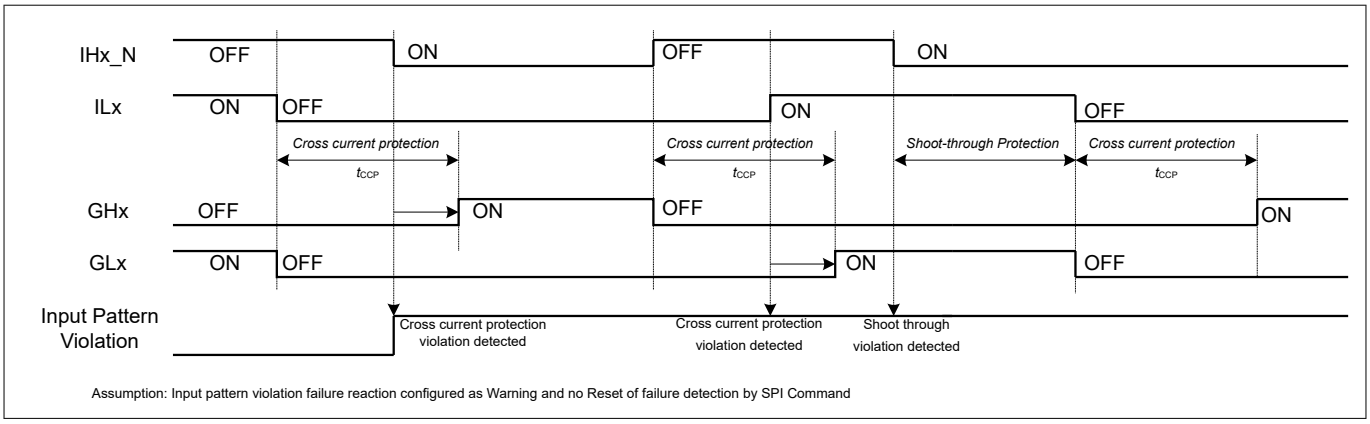

Figure 54 PWM input pin monitoring

Table 24 Configuration options

Configuration options	Related control or status bit	Comment
Enable/disable input pattern violation reporting	IPV_CCP_DIS	The cross current protection feature is not disabled by disabling the input pattern violation reporting feature. Shoot through protection and reporting cannot be deactivated
Cross current time violation failure reaction	IPV_CCP_FM	
Cross current protection time configuration for active MOSFET	TCCP	
Cross current protection time configuration for freewheeling MOSFET	TCCP_FW	
Shoot through failure reaction	IPV_STP_FM	Shoot through violation is considered to be a severe failure and cannot be deactivated. If no active reaction by the device is desired in case a shoot through violation is detected, then a failure reaction warning can be configured
Input pattern violation for cross current time detection at related half-bridge	IPV_CCP_HB3, IPV_CCP_HB2, IPV_CCP_HB1	
Input pattern violation for shoot through detection at related half-bridge	IPV_STP_HB3, IPV_STP_HB2, IPV_STP_HB1	

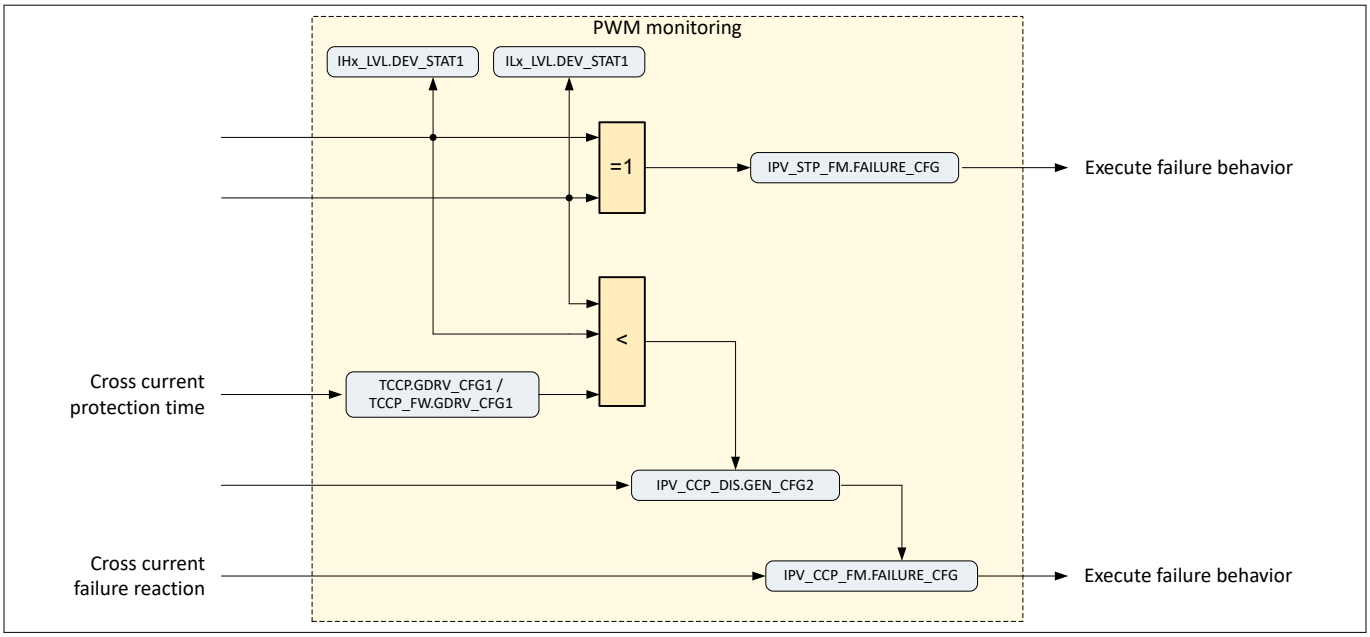

Figure 55 Simplified configuration of PWM input monitoring diagram

1.6.11.1 Shoot through protection

Shoot through protection is active in normal operation mode for activated half-bridges configured by bit HBx_EN.

The implemented locking mechanism (shoot through protection) avoids two complementary output stages Gxx of a half-bridge to be turned on at the same time. If one output stage is turned on, any turn-on signal (including glitches) of the complementary output stage is blocked. Hence a short circuit of the bridge due to faulty input signals or faulty input driving sequences cannot occur.

Failure reaction for shoot through protection is configurable by bit IPV_STP_FM. Shoot through protection cannot be deactivated. If no active reaction by the device is desired in case a violation of the shoot through protection is detected, then a failure reaction warning can be configured as warning.

1. If IHx_N is set to "low" for t > t_{STP_filt}, while ILx is already "high". In this case IPV_STP_HBx is set
2. If ILx is set to "high" for t > t_{STP_filt}, while IHx_N is already "low". In this case IPV_STP_HBx is set

1.6.11.2 Cross current protection

An additional cross conduction protection is offered by the cross current protection time. The cross current protection time defines the time frame between one MOSFET being turned off and the complementary MOSFET of the half-bridge being turned on.

The cross current protection time is generated by the device and is configurable separately for the active and freewheeling MOSFET. The cross current protection time t_{CCP} and t_{CCP_FW} can be configured in 16 steps.

Nominal cross current protection time (TCCP_CFG = 0) for active and freewheeling output stage is defined as:

- t_{CCP_FW} = 240 ns + 240 ns x TCCP_FW [3:0]D
- t_{CCP} = 240 ns + 240 ns x TCCP [3:0]D

There is the possibility to reduce the cross current protection time by factor 2 by setting TCCP_CFG to "1". In this case TCCP, TCCP_FW and$t_{OFF_timeout}$ (P_GDRV_02_24) is reduced to half. Nominal cross current protection time (TCCP_CFG = 1) for active and freewheeling output stage is defined as:

- t_{CCP_FW} = 120 ns + 120 ns x TCCP_FW [3:0]D
- t_{CCP} = 120 ns + 120 ns x TCCP [3:0]D

If the PWM input pins IHx_N and ILx are separately controlled by two microcontroller GPIOs, then in addition to the internal generated cross current protection time, the microcontroller can apply and control the external cross current protection time (for example see Figure 56).

In this case, usually the external PWM signal includes an external cross current protection time which is greater than the device's cross current protection time. Only in cases of failure, such as corrupted microcontroller signals or shorted signals, the internally generated cross current protection time is visible at the Gxx output pins.

Especially for applications where PWM input pins IHx_N and ILx of one half-bridge are controlled by one single GPIO of the microcontroller, the device-internally generated cross current protection time is of very high interest.

In this case, the application relies on the internally generated cross current protection time of the device. Example see Figure 57.

***Note**: No cross current protection time is generated by the device for the first turn ON cycle of a Gxx output stage. In power-up mode and sleep mode Gxx output stages are turned OFF and when entering normal operation mode Gxx output stage are turned ON for the first time by the device depending on the applied IHx_N/ILx signal.*

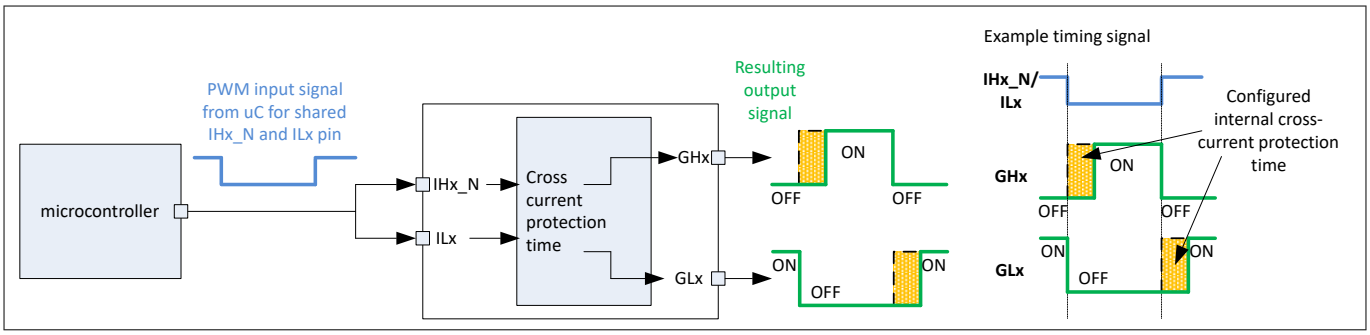

Figure 56 Example: shared PWM inputs - internal cross current protection time generation

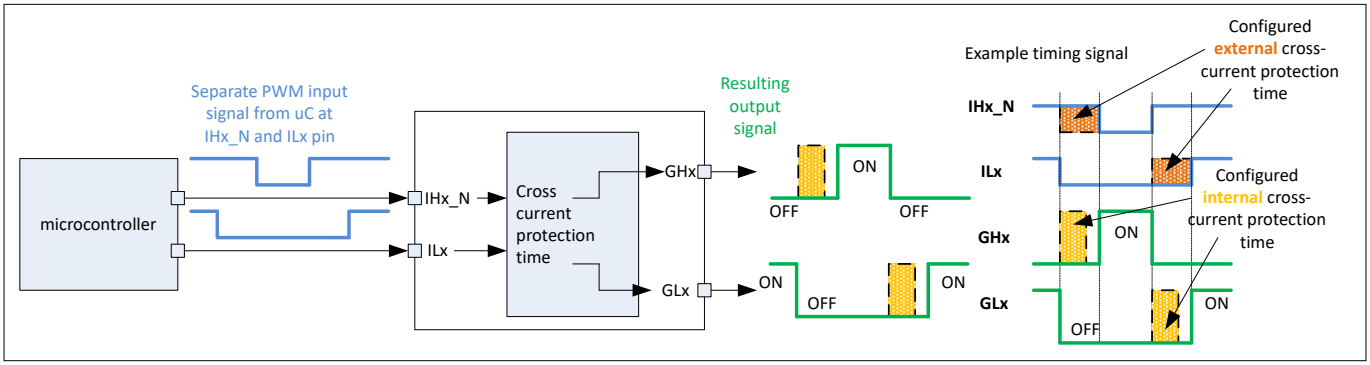

Figure 57 Example: separate PWM inputs - external cross current protection time generation

1.6.11.3 Input pattern violation monitoring

A monitoring of the PWM input pins IHx_N and ILx has been integrated to check if the output pattern of the microcontroller violates the cross current protection time of the bridge driver IC. Therefore, the synchronized IHx_N and ILx signals are compared and checked against the cross current protection time TCCP. Failure bit IPV_CCP_HBx, indicating the affected input pin ILx OR IHx_N which violates the TCCP time, is set in case an input pattern violation is enabled.

The input pattern violation monitoring feature can be disabled by IPV_CCP_DIS. The failure behavior is configurable via SPI during configuration IPV_CCP_FM. When IHx_N is set to "low" while ILx of the same bridge

is set to "high" within the cross current protection time, then in case of latched error 1 (LE1) failure behavior configuration:

- Failure reaction latched error 1 - the device enters safe state
- DE flag is set in the global status byte
- IPV_CCP_HBx is set (see Figure 54)

In case the IPV_CCP_DIS configuration bit is set to "1", status bits IPV_CCP_HBx will not be reported anymore (set to 0) and failure reaction for input pattern violation is disabled. The cross-current protection is not disabled.

***Note**:*
- *It is recommended to deactivate the input pattern violation feature (IPV_CCP_DIS = 1), if the input pins IHx_N to ILx are connected together*
- *In case input pattern violation monitoring is disabled, IPV_CCP_HBx bit will not be cleared if already set to "1", until a clear by SPI write command*

1.6.11.4 PWM alternation monitoring

In BLDC application usually in one half-bridge the high-side and low-side output stages are turned ON and turned OFF alternating. In order to detect and indicate one PWM input pin did not receive a turn ON request while the complementary PWM input still receives periodically turn ON requests, the device includes a PWM alternation monitoring feature. Target is to detect if one PWM input (one per half-bridge) is stuck OFF by, for example, open pin failure. Each enabled half-bridge is monitored at input pins IL1 & IH1_N, IL2 & IH2_N, IL3 & IH3_N for PWM alternation.

PWM alternation monitoring can be disabled and enabled by control bit PWM_CHK_EN.

While the corresponding half-bridge enabled, the device monitors if PWM turn ON request is periodically alternating between HS and LS gate drivers of the same half-bridge. A valid PWM turn ON request is detected by the device if a PWM turn ON signal is applied t > t_{SYNC}. Pulses smaller then t_{SYNC} will not be detected by the device and will trigger failure detection.

A PWM alternation monitoring failure is detected in case one PWM input pin of a half-bridge receives four consecutive turn ON requests, while on the complementary no turn ON request has been detected. In case of failure detection corresponding IHx_MISS/ILx_MISS status bit is set. The failure reaction is configurable by bit PWM_CHK_FM.

***Note**:*
- *If the feature is used in the application, the user has to ensure PWM turn ON requests at input pins ILx/IHx_N shorter than 40 ns are not applied in order to avoid false error reporting*
- *In case PWM alternation monitoring feature is used in the application it is recommended that the microcontroller checks if PWM input pins are connected to the bridge driver by SPI interrogation of IHxN_LVL and ILx_LVL status bits during start-up of the application*
- *If PWM alternation monitoring is disabled, then all related status bits are set to "0" and kept "0". In case the status bit is set to "1", it will not be automatically reset by deactivation of the feature until an SPI clear by write command*

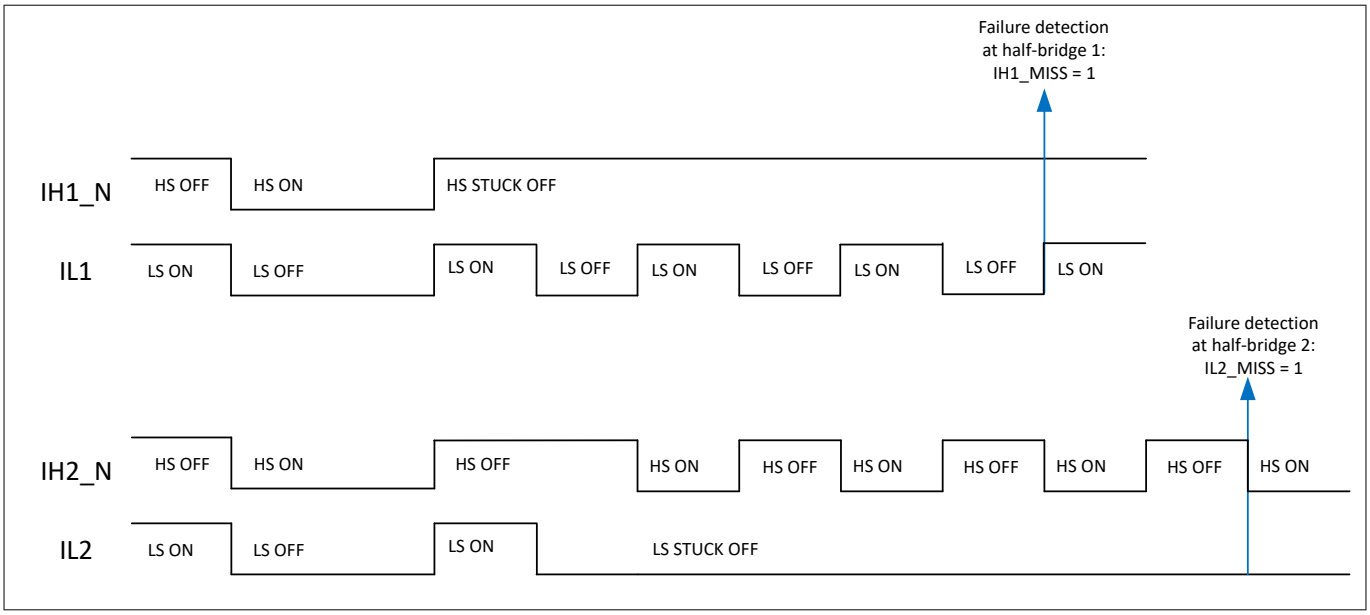

Figure 58 Example: PWM alternation monitoring failure detection

1.6.11.4.1 Latent fault check: PWM input stuck OFF

It is recommended to perform a start-up check to confirm PWM input pins ILx and IHx_N are not stuck OFF (ILx = "low", IHx_N = "high") by SPI read-out of IHxN_LVL and ILx_LVL status bits. Additionally, the microcontroller may check if PWM alternation monitoring failure detection reporting works as specified. Following steps have to be performed:

- Ensure device failure reaction is error: PWM_CHK_FM = "1_B"
- Ensure IHx_N = "high" AND ILx = "low" for used half-bridges of the device
- Ensure that the device is in normal operation mode and output stages can be controlled (CP_EN = "1")
- Ensure that the half-bridges are enabled: HBx_EN = "1". Only enabled half-bridges are monitored for PWM alternation
- Ensure no other failure is detected and reported by device
- Apply four consecutive ILx = "high" pulses for t > 1 µs while IHx_N pin is kept "high"
- Check if ERR_N pin is set to "low"
- Check if DE status flag is set to "1" AND IHx_MISS = "1"

Similar procedure can be applied for the complementary PWM input pin.

1.6.12 Digital output pin failure detection

Both digital output pins ERR_N and SDO include an output pin failure detection. Failure detection can be read-out via SPI. In case of failure detection the affected pin is deactivated.

1.6.12.1 ERR_N pin stuck "high" detection

The ERR_N overload detection can detect a short circuit condition to supply. In case ERR_N pin is shorted to supply, then:

- The ERR_N output pad is disabled
- The error register bit ERRN_SHORT is set accordingly
- Failure reaction according to bit ERRN_FM is executed

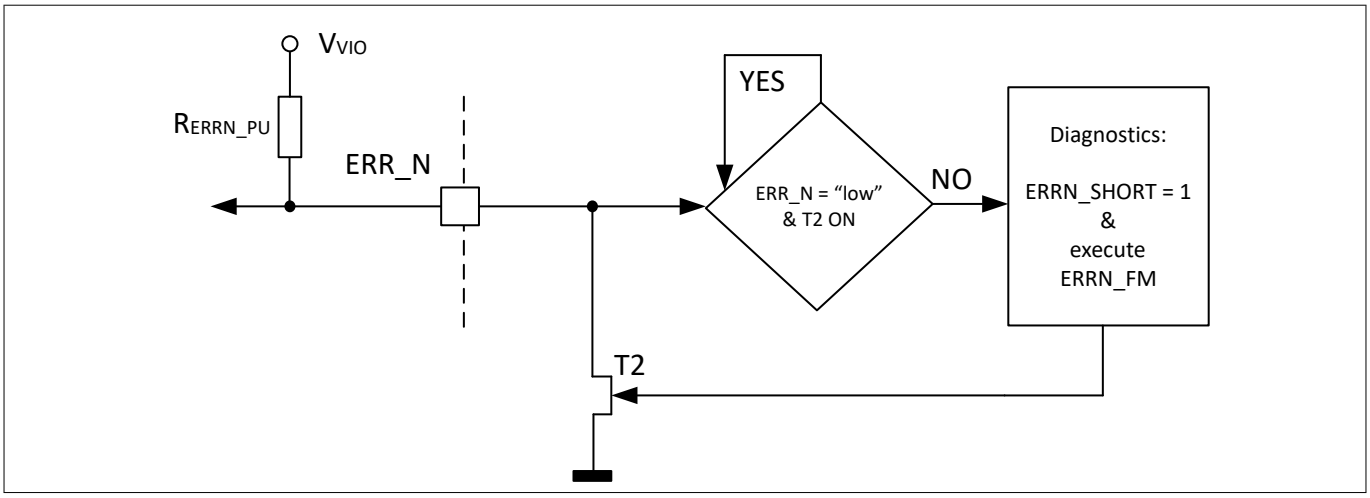

Figure 59 Block diagram: ERR_N stuck "high" detection

1.6.12.2 SDO short to supply or ground detection

The SDO overload detection can distinguish between the following failure cases:

- Short circuit to GND
- Short circuit to microcontroller supply

If one of the above listed short circuit conditions is detected:

- The SDO output pad is set to tri-state (disabled) until the next SPI command is triggered by the microcontroller
- The corresponding status bit SDO_SHORT is set
- The failure reaction according to bit SDO_SHORT_FM is executed

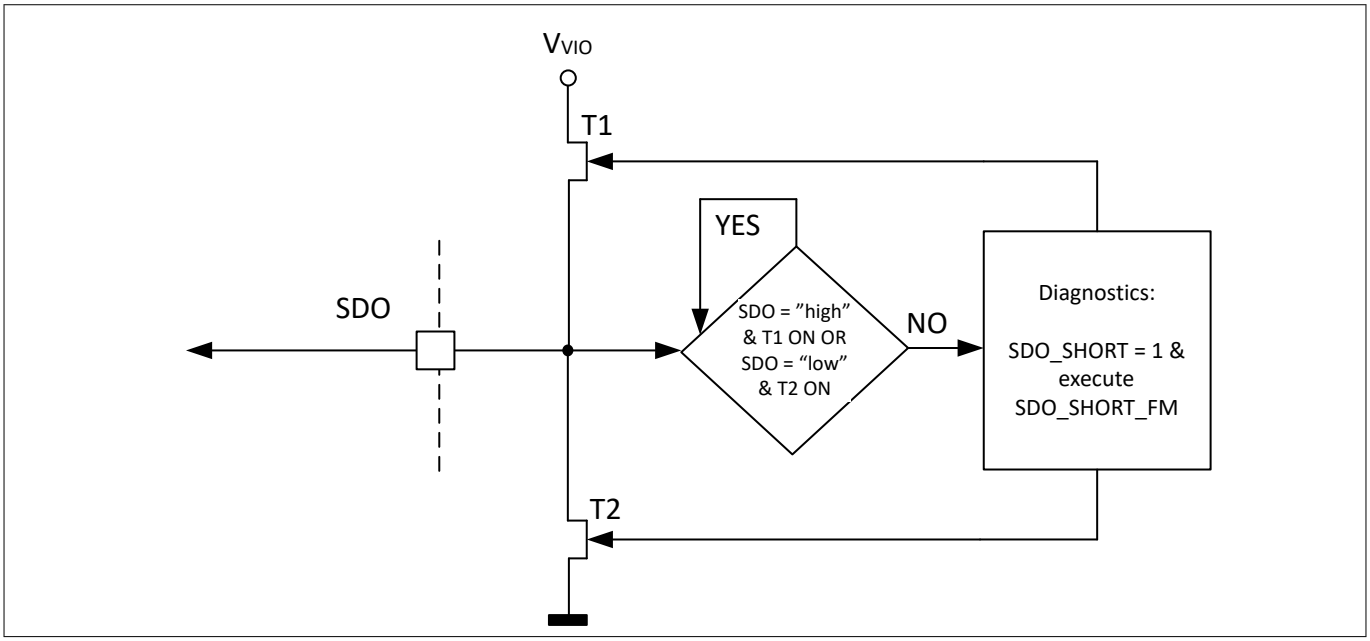

Figure 60 Block diagram: SDO overload detection

To detect a short circuit condition at the SDO pin, the SPI communication has to be triggered, see figure below.

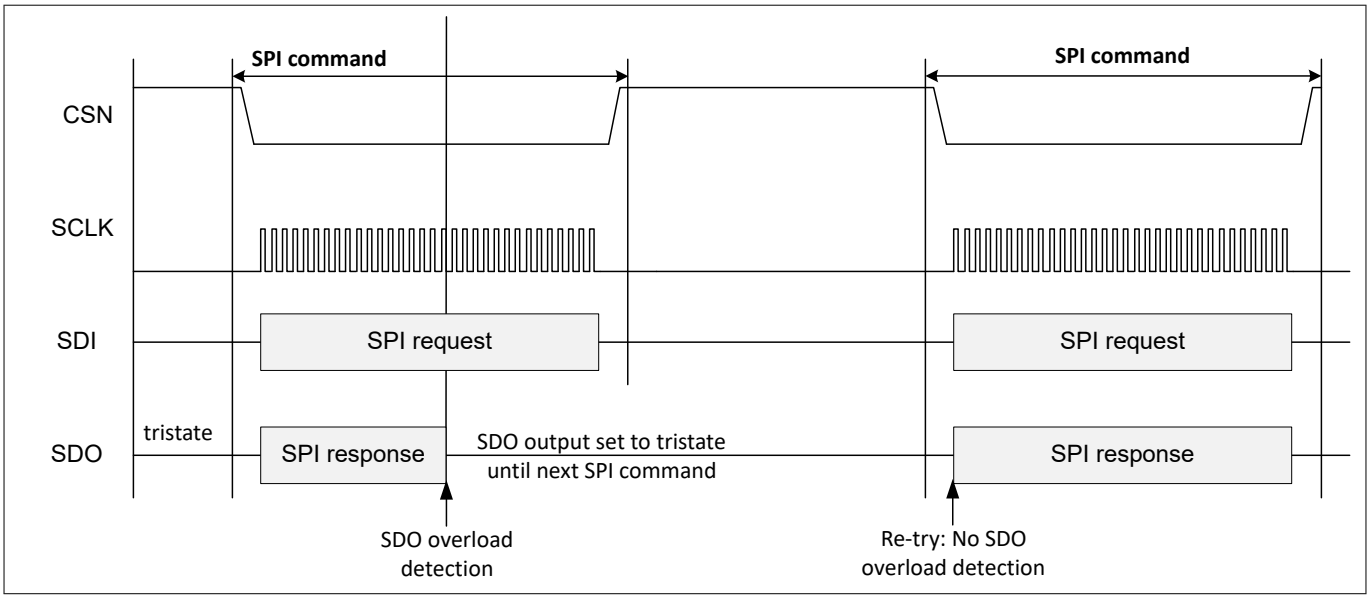

Figure 61 Timing diagram: SDO overload detection

1.7 Safe state (additional information)

The safe state of the device is triggered by three different root causes:

1. INH_N input pin is set to "low" OR
2. Device in power-up mode (forced safe state) OR
3. Device in normal operation mode AND failure detected which triggers latched error 1 (LE1) failure reaction

The device indicates safe state entry towards the microcontroller by setting status bit SOFF_ACT ="1" in register DEV_STAT1 ($0x27_H$). Additionally, ERR_N pin is set to "low" at the same time, and global status flag DE is set to "1" in global status byte.

SOFF_ACT status is set to "1" only when safe state entry is issued via the digital SOFF path. The analog gate driver module safe state entry feedback (status bit SOFF_GDRV) indicates:

- SOFF_GDRV = 1 that the gate drivers are all in safe state
- SOFF_GDRV = 0 at least 1 out of 6 gate drivers was not switched OFF

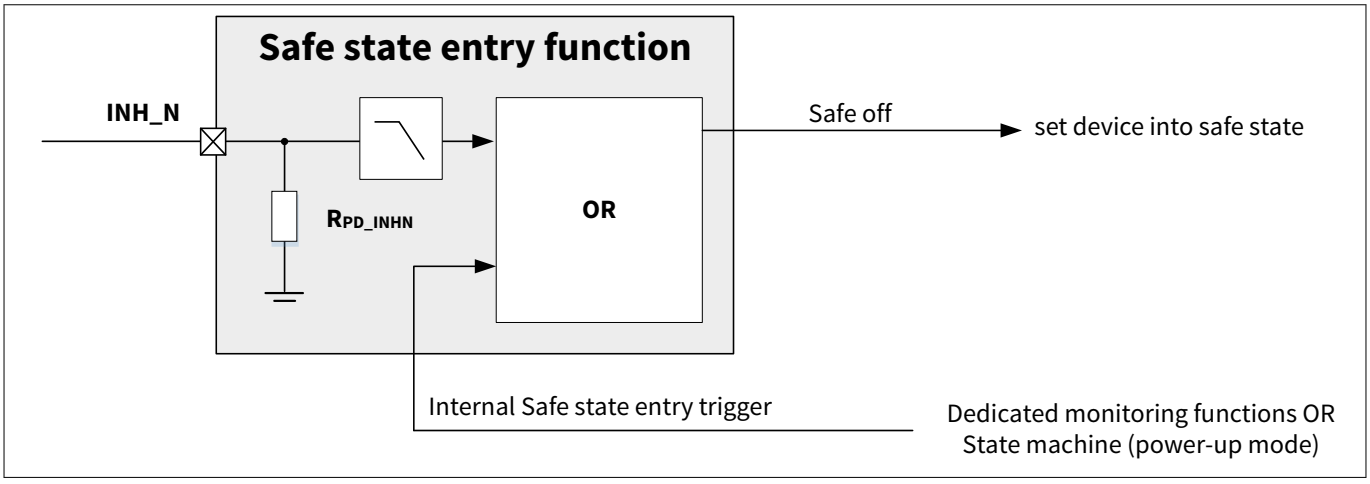

Figure 62 Safe state trigger events

The safe state activation has two independent paths:

- Analog safe path
- Digital safe path

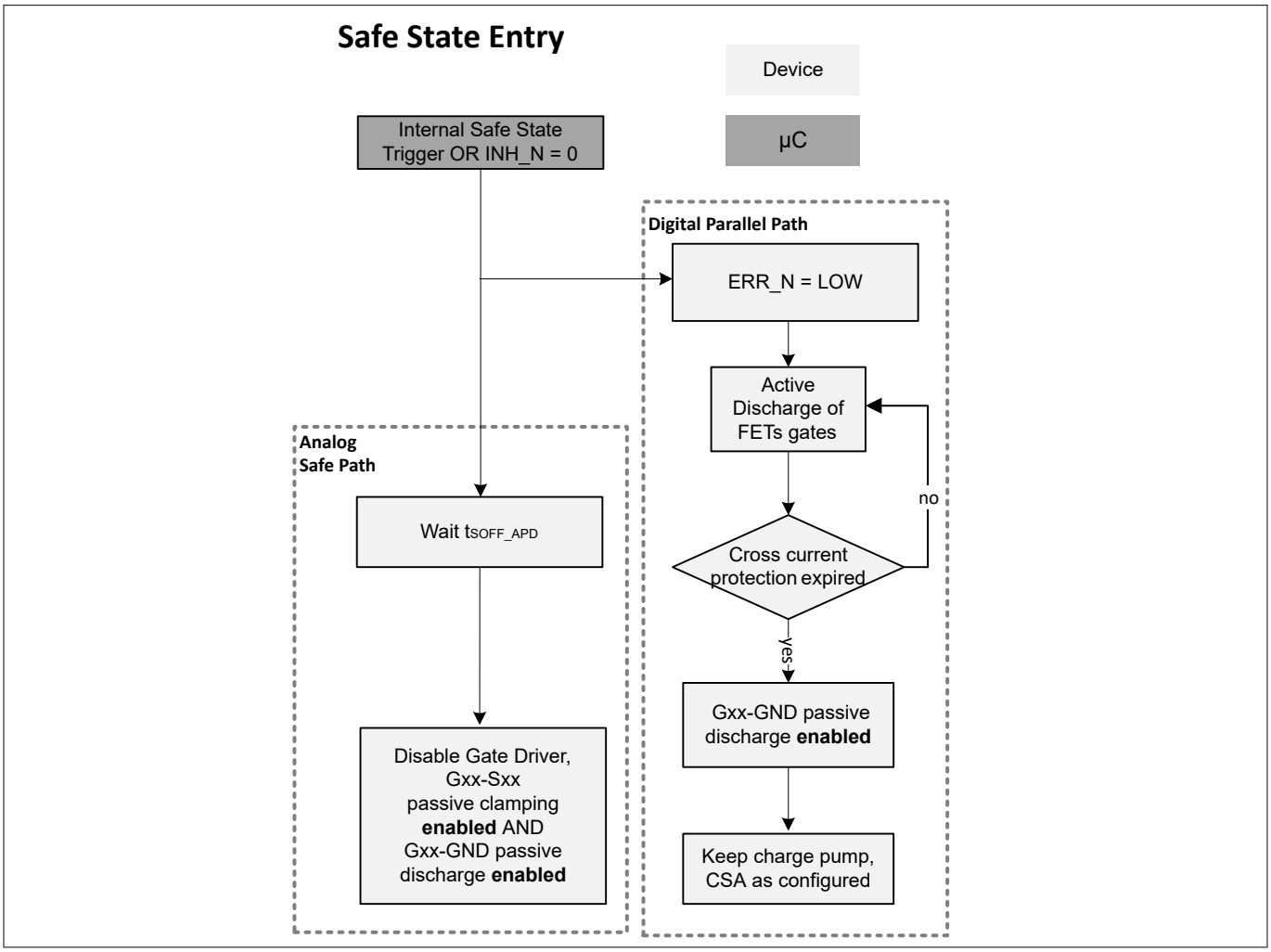

Figure 63 Entry of safe state

In case of safe state trigger event detected the device will enter safe state via the digital safe path. Additionally, following actions are performed by the device:

- ERR_N pin is set to "low"
- All output stages are actively turned off with IDCHG_ST for configured cross current protection time once the pre-discharge time TPDCHG has elapsed
- The gate driver output stages is kept off with passive discharge

***Note**: The ERR_N pin is only pulled low if no short circuit to the supply has been detected on the ERR_N pin.*

In case of safe state trigger event detected the device will enter safe state via the analog safe path.

After analog filter time t_{SOFF_APD}, the gate driver output stages are turned off and kept off with Gxx-Sxx passive clamping enabled AND Gxx-GND passive discharge enabled.

In case safe state entry is triggered by INH_N pin "low" for t > $t_{INHN_L_WAIT}$ AND no valid SPI communication is received by the device, the device will enter sleep mode with Gxx-Sxx passive clamping enabled AND Gxx-GND passive discharge enabled. Once sleep mode is entered ERR_N will not be driven actively "low" by the device and pulled "high" by the external pull-up resistor R_{ERR_PU}.

Safe state is exited if:

- The INH_N pin is set to "high" AND

- No internal failure is detected which is configured as latched error 1 (LE1) AND
- Microcontroller has cleared errors related to the safe state triggering event if any by SPI clear command AND
- Device is in normal operation mode

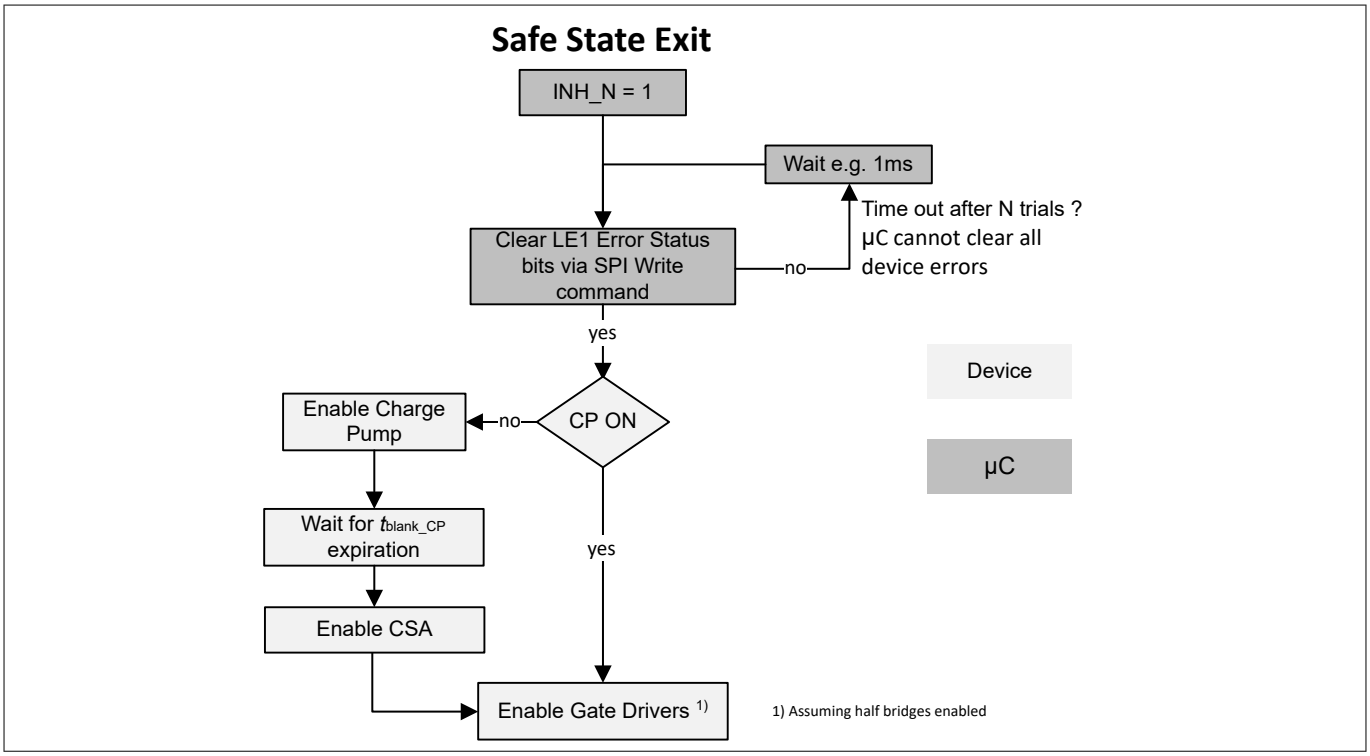

Figure 64 Safe state exit

The safe state entry can be triggered by SPI command by setting SOFF_ON control bit to "1" in SPI register GEN_CFG1, see Safe state entry functional check.

2 SPI register specification

SPI register specification includes nominal values. For settings options and exact values of timings, currents or thresholds refer to the device datasheet for further information.

2.1 SPI bit field types

The following bit field types are available in the device:

Table 25 SPI bit field types

Bit field type	Short description	Explanation
rw	read & write	External read and write access
r	read only	External read access only
rwh	read & write hardware access	External read and write access; device can modify bit field (set to '0')
rw1ch	read & clear by write	Read by software/set to '1' by device, write '1' by software to clear
res	reserved	Reserved bit field - always read as '0'

2.2 Registers overview - TLE9186 (ascending offset address)

Table 26 Registers overview - TLE9186 (ascending offset address)

Short name	Long name	Offset address	See
CONFIG_SECURED	Power-up configuration protected register	01_H	87
PWR_MOD_CFG	Mode control register	02_H	89
WD_CFG	Watchdog configuration register	03_H	90
GEN_CFG1	General configuration register 1	04_H	91
GEN_CFG2	General configuration register 2	05_H	93
GDRV_CFG1	Gate driver configuration register 1	07_H	95
GDRV_CFG2	Gate driver configuration register 2	08_H	97
GDRV_CFG3	Gate driver configuration register 3	09_H	100
TON_HS	Gate Driver Configuration register - TON_HS	$0A_H$	101
TON_LS	Gate Driver Configuration register - TON_LS	$0B_H$	106
TOFF_HS	Gate Driver Configuration register - TOFF_HS	$0C_H$	111
TOFF_LS	Gate Driver Configuration register - TOFF_LS	$0D_H$	116
T3OFF	Gate Driver Configuration register - T3OFF	$0E_H$	121
ION_HS1	Gate driver Configuration register - ION_HS1	$0F_H$	126
ION_LS1	Gate driver Configuration register - ION_LS1	10_H	131
ION_HS2	Gate driver Configuration register - ION_HS2	11_H	136
ION_LS2	Gate driver Configuration register - ION_LS2	12_H	141
ION_HS3	Gate driver Configuration register - ION_HS3	13_H	146

(table continues...)

Table 26 (continued) Registers overview - TLE9186 (ascending offset address)

Short name	Long name	Offset address	See
ION_LS3	Gate driver Configuration register - ION_LS3	14_H	151
I3ON	Gate driver Configuration register - I3ON	15_H	156
ION_IOFF_DIDT	Gate driver Configuration register - ION_IOFF_DIDT	16_H	161
IOFF_HS1	Gate driver Configuration register - IOFF_HS1	17_H	166
IOFF_LS1	Gate driver Configuration register - IOFF_LS1	18_H	171
IOFF_HS2	Gate driver Configuration register - IOFF_HS2	19_H	176
IOFF_LS2	Gate driver Configuration register - IOFF_LS2	$1A_H$	181
IOFF_HS3	Gate driver Configuration register - IOFF_HS3	$1B_H$	186
IOFF_LS3	Gate driver Configuration register - IOFF_LS3	$1C_H$	191
CSA_CFG	Current sense amplifier configuration register	$1D_H$	196
FAILURE_CFG	Failure reaction configuration register 1	$1E_H$	198
SELF_TEST_CFG	Self-test configuration register	$1F_H$	200
SUP_STAT	Supply monitoring status register	25_H	202
SPI_STAT	SPI status register (SPI and WD monitoring)	26_H	204
DEV_STAT1	Device status register 1: Operation mode and digital input pins levels	27_H	206
DEV_STAT2	Device status register 2: Input pattern violation, ERR_N, CSA, TSD monitoring	28_H	208
LF_STAT	Latent faults and self-tests status register: internal faults, self-tests results	29_H	210
SH_LEVEL_STAT	Phase pins monitoring	$2A_H$	211
BD_STAT	HS & LS Gate Drivers monitoring	$2B_H$	212
WD_CLK_CNT	Watchdog clock counter	$2C_H$	214
PHASE1_CNT	Phase 1 high time counter	$2D_H$	215
PHASE2_CNT	Phase 2 high time counter	$2E_H$	216
PHASE3_CNT	Phase 3 high time counter	$2F_H$	217
TDON_TDOFF_HS1	Effective MOSFET turn-on/off delay time HS1	30_H	218
TDON_TDOFF_LS1	Effective MOSFET turn-on/off delay time LS1	31_H	219
TDON_TDOFF_HS2	Effective MOSFET turn-on/off delay time HS2	32_H	220
TDON_TDOFF_LS2	Effective MOSFET turn-on/off delay time LS2	33_H	221
TDON_TDOFF_HS3	Effective MOSFET turn-on/off delay time HS3	34_H	222
TDON_TDOFF_LS3	Effective MOSFET turn-on/off delay time LS3	35_H	223
TSLEW_ON_OFF_HS1	Effective MOSFET slew rate time HS1	36_H	224
TSLEW_ON_OFF_LS1	Effective MOSFET slew rate time LS1	37_H	225
TSLEW_ON_OFF_HS2	Effective MOSFET slew rate time HS2	38_H	226
TSLEW_ON_OFF_LS2	Effective MOSFET slew rate time LS2	39_H	227

(table continues...)

Table 26 (continued) Registers overview - TLE9186 (ascending offset address)

Short name	Long name	Offset address	See
TSLEW_ON_OFF_HS3	Effective MOSFET slew rate time HS3	$3A_H$	228
TSLEW_ON_OFF_LS3	Effective MOSFET slew rate time LS3	$3B_H$	229

2.3 Power-up configuration protected register

CONFIG_SECURED Offset address: 01_H

Power-up configuration protected register DefaultReset value: 0040_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		CP_CLK_SEL		CP_CFG	WD_EN	PWM_MAP	INHN_L_CFG	SPI_TYPE		VIO_CFG		GDRV_RNG	GDRV_CFG	OFF_CFG	FW_CFG
res		rw		rw	rw	rw	rw	rw		rw		rw	rw	rw	rw

Field	Bits	Type	Description
FW_CFG	0	rw	**Freewheeling device charge/discharge phase configuration** 0_B Freewheeling device does not use precharge/predischarge phase (Default) 1_B Freewheeling device uses precharge/predischarge phase (t1ON_HS, t1ON_LS, t1OFF_HS,t1OFF_LS)
OFF_CFG	1	rw	**Switch OFF behavior in case of detected faults leading to gate driver OFF** 0_B Turn-off gate drivers with active turn-off settings (default) 1_B Static using I1OFF for T1OFF and IDCHG_ST for TCCP
GDRV_CFG	2	rw	**Gate Driver Operation Mode Configuration** 0_B Gate Driver SPI configured timing for sequencer phase changes (Default) 1_B Gate Driver Automatic sequencer phase transitions based on SHx sensing
GDRV_RNG	3	rw	**Gate Driver Output Current Range Configuration** 0_B Gate Driver output current range configured to 0.5mA...100mA (Default) 1_B Gate Driver output current range configured to 1mA...150mA
VIO_CFG	5:4	rw	**VIO voltage level configuration bits** 00_B VIO not configured, monitoring VIO thresholds (VIO_UV threshold ~3V, VIO_OV threshold ~5.45V) (Default) 01_B VIO configured as 5V supply level 10_B VIO configured as 3.3V supply level 11_B VIO not configured, monitoring VIO thresholds (VIO_UV threshold ~3V, VIO_OV threshold ~5.45V)
SPI_TYPE	7:6	rw	**SPI SDO response type configuration bits** 00_B reserved 01_B SPI in-frame response configured (Default) 10_B SPI out-of-frame response configured 11_B reserved

(table continues...)

(continued)

Field	Bits	Type	Description
INHN_L_CFG	8	rw	**INHN low detection wait time configuration** 0_B tINHN_L_WAIT time is not restarted after a SPI command while INHN is low and current tINHN_L_WAIT not expired (Default) 1_B tINHN_L_WAIT time is restarted after a SPI command while INHN is low and current tINHN_L_WAIT not expired
PWM_MAP	9	rw	**PWM mapping to gate drivers configuration** 0_B IHxN used for HS drivers control, ILx used for LS drivers control (Default) 1_B IHxN deactivated, ILx used for corresponding half-bridge HBx control (one PWM input per half-bridge)
WD_EN	10	rw	**Watchdog enable** 0_B Watchdog monitoring disabled (Default) 1_B Watchdog monitoring enabled
CP_CFG	11	rw	**Charge pump Configuration** 0_B Two-stage charge pump configuration at low VSCP (Default) 1_B Three-stage charge pump configuration at low VSCP
CP_CLK_SEL	13:12	rw	**Charge Pump Clock selection** 00_B 250kHz (Default) 01_B 225kHz 10_B 200kHz 11_B 175kHz
0	15:14	res	**Reserved** Read as 0; shall be written with 0.

2.4 Mode control register

PWR_MOD_CFG Offset address: 02_H

Mode control register DefaultReset value: 0002_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR_CONFIG	**CLR_STATS**	**0**												**MODE_CTRL**	
rw	rw	res												rw	

Field	Bits	Type	Description
MODE_CTRL	1:0	rw	**Device operation mode configuration** 00_B reserved 01_B Normal operation mode selected 10_B Power-up mode selected (Default) 11_B reserved
CLR_STATS	14	rw	**Clear SPI device status registers** 0_B SPI status registers not cleared (Default) 1_B Trigger SPI status registers clear
CLR_CONFIG	15	rw	**Clear SPI device configuration registers** 0_B SPI configuration registers not cleared (Default) 1_B Trigger SPI configuration registers clear
0	13:2	res	**Reserved** Read as 0; shall be written with 0.

2.5 Watchdog configuration register

WD_CFG Offset address: 03_H

Watchdog configuration register DefaultReset value: $001D_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHECKSUM	**0**									**WD_FAIL**			**WD_PER**		
rw	res									rw			rw		

Field	Bits	Type	Description
WD_PER	2:0	rw	**Watchdog period configuration** 000_B 2ms 001_B 4ms 010_B 8ms 011_B 16ms 100_B 32ms 101_B 64ms (Default) 110_B 128ms 111_B 256ms
WD_FAIL	5:3	rw	**Watchdog error counter configuration** 000_B 2 001_B 4 010_B 6 011_B 8 (Default) 100_B 10 101_B 12 110_B 14 111_B 15
CHECKSUM	15	rw	**Watchdog configuration checksum bit** 0_B counts as 0 for checksum calculation (Default) 1_B counts as 1 for checksum calculation
0	14:6	res	**Reserved** Read as 0; shall be written with 0.

2.6 General configuration register 1

GEN_CFG1 Offset address: 04_H

General configuration register 1 DefaultReset value: 6904_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CP_EN	**CP_MODE**		**CP_FMOD**		**CP_REC_UV**	**CP_REC_OV**	**PFB_EN**	**HB3_EN**	**HB2_EN**	**HB1_EN**	**HBFREQ**	**CSA_EN**	**TW_EN**	**ERRN_ON**	**SOFF_ON**
rwh	rw		rw		rw	rw	rw	rwh	rwh	rwh	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SOFF_ON	0	rw	**Safe State activation via SPI command** 0_B Safe State not forced active (Default) 1_B Safe State forced active
ERRN_ON	1	rw	**ERRN function activation via SPI command** 0_B ERRN not forced active (Default) 1_B ERRN forced active
TW_EN	2	rw	**Thermal warning function activation via SPI command** 0_B Thermal warning monitoring disabled 1_B Thermal warning monitoring enabled (Default)
CSA_EN	3	rw	**Current sense amplifier enable** 0_B Current sense amplifier disabled (Default) 1_B Current sense amplifier enabled
HBFREQ	4	rw	**Half-bridge synchronization frequency** 0_B 75MHz (Default) 1_B 37.5MHz
HB1_EN	5	rwh	**Half-bridge 1 enable** 0_B Half-bridge 1 disabled (Default) 1_B Half-bridge 1 enabled
HB2_EN	6	rwh	**Half-bridge 2 enable** 0_B Half-bridge 2 disabled (Default) 1_B Half-bridge 2 enabled
HB3_EN	7	rwh	**Half-bridge 3 enable** 0_B Half-bridge 3 disabled (Default) 1_B Half-bridge 3 enabled
PFB_EN	8	rw	**Phase feedback monitoring enable** 0_B PFB function disabled 1_B PFB function enabled (Default)
CP_REC_OV	9	rw	**Charge pump recovery in case of VSCP_OV_SD event** 0_B Automatic restart disabled (Default) 1_B Automatic restart enabled, Charge pump restarts when VSCP_OV_SD event not present anymore

(table continues...)

(continued)

Field	Bits	Type	Description
CP_REC_UV	10	rw	**Charge pump recovery in case of VSCP_UV_SD event** 0_B Automatic restart disabled (Default) 1_B Automatic restart enabled, Charge pump restarts when VSCP_UV_SD event not present anymore
CP_FMOD	12:11	rw	**Charge pump frequency modulation configuration** 00_B Frequency modulation disabled 01_B Modulation frequency set to 15.6kHz (Default) 10_B Modulation frequency set to 31.2kHz 11_B Modulation frequency set to 62.5kHz
CP_MODE	14:13	rw	**Charge Pump Operation Mode configuration bits** 00_B Charge Pump forced in double stage(if CP_CFG=0) or three-stage (if CP_CFG=1) charge pump operation mode 01_B Charge pump forced in double stage charge pump operation mode 10_B Charge pump forced in single stage charge pump operation mode 11_B Charge pump automatic operation mode change enabled (Default)
CP_EN	15	rwh	**Charge pump function enable** 0_B Charge pump disabled (Default) 1_B Charge pump enabled

2.7 General configuration register 2

GEN_CFG2 Offset address: 05_H

General configuration register 2 DefaultReset value: 0800_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPFB	**0**			**TW_TH**		**0**			**CP_UV_TH**	**CSN_TO_DIS**	**IPV_CCP_DIS**	**HB3IDIAG**	**HB2IDIAG**	**HB1IDIAG**	**OFF_DIAG_EN**
rw	res			rw		res			rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
OFF_DIAG_EN	0	rw	**OFF-state diagnostic function enable** 0_B OFF-state diagnostic disabled (Default) 1_B OFF-state diagnostic enabled
HB1IDIAG	1	rw	**OFF-state diagnostic control of HB1 pull-down current** 0_B Pull-down current for off-state diagnostics disabled (Default) 1_B Pull-down current for off-state diagnostics enabled
HB2IDIAG	2	rw	**OFF-state diagnostic control of HB2 pull-down current** 0_B Pull-down current for off-state diagnostics disabled (Default) 1_B Pull-down current for off-state diagnostics enabled
HB3IDIAG	3	rw	**OFF-state diagnostic control of HB3 pull-down current** 0_B Pull-down current for off-state diagnostics disabled (Default) 1_B Pull-down current for off-state diagnostics enabled
IPV_CCP_DIS	4	rw	**Disable input pattern violation for cross-current protection** 0_B Input pattern violation due to cross-current protection error signalized by status bits IPV_CCP_HBx (Default) 1_B Input pattern violation due to cross-current protection error not signalized by status bits IPV_CCP_HBx
CSN_TO_DIS	5	rw	**CSN time-out disable option** 0_B CSN time-out is enabled (Default) 1_B CSN time-out is disabled
CP_UV_TH	6	rw	**Charge Pump under-voltage threshold selection** 0_B VCPH_UV 8.5V typical falling threshold selected (Default) 1_B VCPH_UV 7V typical falling threshold selected
TW_TH	11:10	rw	**Temperature warning threshold selection** 00_B Temperature warning at 130 degC 01_B Temperature warning at 140 degC 10_B Temperature warning at 150 degC (Default) 11_B Temperature warning at 160 degC
TPFB	15	rw	**PFB monitoring filter time configuration** 0_B Filter time configured as 2 xTVDSFILT (Default) 1_B Filter time configured as 4 x TVDSFILT

(table continues...)

(continued)

Field	Bits	Type	Description
0	9:7, 14:12	res	**Reserved** Read as 0; shall be written with 0.

2.8 Gate driver configuration register 1

GDRV_CFG1 Offset address: 07_H

Gate driver configuration register 1 DefaultReset value: 8888_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TVDSBLK				**TVDSBLK_FW**				**TCCP**				**TCCP_FW**			
rw				rw				rw				rw			

Field	Bits	Type	Description
TCCP_FW	3:0	rw	**Cross-current protection time configuration of the freewheeling MOSFET** 0_H 0.24µs 1_H 0.48µs 2_H 0.72µs 3_H 0.96µs 4_H 1.2µs 5_H 1.44µs 6_H 1.68µs 7_H 1.92µs 8_H 2.16µs (Default) 9_H 2.4µs A_H 2.64µs B_H 2.88µs C_H 3.12µs D_H 3.36µs E_H 3.6µs F_H 3.84µs
TCCP	7:4	rw	**Cross-current protection time configuration of the active MOSFET** 0_H 0.24µs 1_H 0.48µs 2_H 0.72µs 3_H 0.96µs 4_H 1.2µs 5_H 1.44µs 6_H 1.68µs 7_H 1.92µs 8_H 2.16µs (Default) 9_H 2.4µs A_H 2.64µs B_H 2.88µs C_H 3.12µs D_H 3.36µs E_H 3.6µs F_H 3.84µs

(table continues...)

(continued)

Field	Bits	Type	Description
TVDSBLK_FW	11:8	rw	**Blanking time configuration of the freewheeling MOSFET** 0_H 0.24µs 1_H 0.48µs 2_H 0.72µs 3_H 0.96µs 4_H 1.2µs 5_H 1.44µs 6_H 1.68µs 7_H 1.92µs 8_H 2.16µs (Default) 9_H 2.4µs A_H 2.64µs B_H 2.88µs C_H 3.12µs D_H 3.36µs E_H 3.6µs F_H 3.84µs
TVDSBLK	15:12	rw	**Blanking time configuration of the active MOSFET** 0_H 0.24µs 1_H 0.48µs 2_H 0.72µs 3_H 0.96µs 4_H 1.2µs 5_H 1.44µs 6_H 1.68µs 7_H 1.92µs 8_H 2.16µs (Default) 9_H 2.4µs A_H 2.64µs B_H 2.88µs C_H 3.12µs D_H 3.36µs E_H 3.6µs F_H 3.84µs

2.9 Gate driver configuration register 2

GDRV_CFG2 Offset address: 08_H

Gate driver configuration register 2 DefaultReset value: 5989_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCCP_CFG	**PWM_CHK_EN**	**TFW**						**TVDSFILT**		**HS_DSOVTH**			**LS_DSOVTH**		
rw	rw	rw						rw		rw			rw		

Field	Bits	Type	Description
LS_DSOVTH	2:0	rw	**LS MOSFETs drain-source threshold configuration** 000_B 150mV 001_B 200mV (Default) 010_B 250mV 011_B 300mV 100_B 350mV 101_B 400mV 110_B 500mV 111_B 600mV
HS_DSOVTH	5:3	rw	**HS MOSFETs drain-source threshold configuration** 000_B 150mV 001_B 200mV (Default) 010_B 250mV 011_B 300mV 100_B 350mV 101_B 400mV 110_B 500mV 111_B 600mV
TVDSFILT	7:6	rw	**Drain-source monitoring comparators filter time** 00_B 0.5µs 01_B 1µs 10_B 2µs (default) 11_B 3µs

(table continues...)

(continued)

Field	Bits	Type	Description
TFW	13:8	rw	**Freewheeling device charge/discharge time** 00_H 27ns 01_H 53ns 02_H 80ns 03_H 107ns 04_H 133ns 05_H 160ns 06_H 187ns 07_H 213ns 08_H 240ns 09_H 267ns $0A_H$ 293ns $0B_H$ 320ns $0C_H$ 347ns $0D_H$ 373ns $0E_H$ 400ns $0F_H$ 427ns 10_H 453ns 11_H 480ns 12_H 507ns 13_H 533ns 14_H 560ns 15_H 587ns 16_H 613ns 17_H 640ns 18_H 667ns 19_H 693ns (Default) $1A_H$ 720ns $1B_H$ 747ns $1C_H$ 773ns $1D_H$ 800ns $1E_H$ 827ns $1F_H$ 853ns 20_H 880ns 21_H 907ns 22_H 933ns 23_H 960ns 24_H 987ns 25_H 1013ns 26_H 1040ns 27_H 1067ns 28_H 1093ns 29_H 1120ns $2A_H$ 1147ns $2B_H$ 1173ns $2C_H$ 1200ns

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 1227ns $2E_H$ 1253ns $2F_H$ 1280ns 30_H 1307ns 31_H 1333ns 32_H 1360ns 33_H 1387ns 34_H 1413ns 35_H 1440ns 36_H 1467ns 37_H 1493ns 38_H 1520ns 39_H 1547ns $3A_H$ 1573ns $3B_H$ 1600ns $3C_H$ 1627ns $3D_H$ 1653ns $3E_H$ 1680ns $3F_H$ 1707ns
PWM_CHK_EN	14	rw	**Enable PWM alternation monitoring function** 0_B PWM alternation check disabled 1_B PWM alternation check enabled(Default)
TCCP_CFG	15	rw	**Cross-Current protection times clock selection** 0_B Normal TCCP and TCCP_FW (Default) 1_B Reduced TCCP and TCCP_FW by factor 2

2.10 Gate driver configuration register 3

GDRV_CFG3 Offset address: 09_H

Gate driver configuration register 3 DefaultReset value: $016A_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						ION_TR		IHOLD		IFW			IDCHG_ST		
res						rw		rw		rw			rw		

Field	Bits	Type	Description
IDCHG_ST	2:0	rw	**Gate Driver static discharge current configuration** 000_B 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) 001_B 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 010_B 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) (Default) 011_B 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 100_B 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 101_B 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 110_B 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 111_B 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)
IFW	5:3	rw	**Freewheeling charge and discharge current setting** 000_B 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) 001_B 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 010_B 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 011_B 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 100_B 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 101_B 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) (Default) 110_B 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 111_B 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)
IHOLD	7:6	rw	**Bridge Driver Hold Current configuration** 00_B 10mA 01_B 15mA (default) 10_B 20mA 11_B 30mA
ION_TR	9:8	rw	**Configuration of the transition to post-charge phase current** 00_B I3ON post-charge current is reached by a ramp current from I2ON with a 2 current steps per HBFREQ clock cycle 01_B I3ON post-charge current is reached by a ramp current from I2ON with a 4 current steps per HBFREQ clock cycle (Default) 10_B I3ON post-charge current is reached by a ramp current from I2ON with a 8 current steps per HBFREQ clock cycle 11_B I3ON post-charge current applied directly after I2ON phase
0	15:10	res	**Reserved** Read as 0; shall be written with 0.

2.11 Gate Driver Configuration register - TON_HS

TON_HS Offset address: $0A_H$

Gate Driver Configuration register - TON_HS DefaultReset value: 0717_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**T1ON_HS**						**0**		**T2ON_HS**					
res		rw						res		rw					

Field	Bits	Type	Description
T2ON_HS	5:0	rw	**High Side gate driver charge time configuration** 00_H 27ns 01_H 53ns 02_H 80ns 03_H 107ns 04_H 133ns 05_H 160ns 06_H 187ns 07_H 213ns 08_H 240ns 09_H 267ns $0A_H$ 293ns $0B_H$ 320ns $0C_H$ 347ns $0D_H$ 373ns $0E_H$ 400ns $0F_H$ 427ns 10_H 453ns 11_H 480ns 12_H 507ns 13_H 533ns 14_H 560ns 15_H 587ns 16_H 613ns 17_H 640ns (default) 18_H 667ns 19_H 693ns $1A_H$ 720ns $1B_H$ 747ns $1C_H$ 773ns $1D_H$ 800ns $1E_H$ 827ns $1F_H$ 853ns 20_H 880ns 21_H 907ns 22_H 933ns 23_H 960ns 24_H 987ns 25_H 1013ns 26_H 1040ns 27_H 1067ns 28_H 1093ns 29_H 1120ns $2A_H$ 1147ns $2B_H$ 1173ns $2C_H$ 1200ns

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 1227ns $2E_H$ 1253ns $2F_H$ 1280ns 30_H 1307ns 31_H 1333ns 32_H 1360ns 33_H 1387ns 34_H 1413ns 35_H 1440ns 36_H 1467ns 37_H 1493ns 38_H 1520ns 39_H 1547ns $3A_H$ 1573ns $3B_H$ 1600ns $3C_H$ 1627ns $3D_H$ 1653ns $3E_H$ 1680ns $3F_H$ 1707ns

(table continues...)

(continued)

Field	Bits	Type	Description
T1ON_HS	13:8	rw	**High Side gate driver pre-charge time configuration** 00_H 27ns 01_H 53ns 02_H 80ns 03_H 107ns 04_H 133ns 05_H 160ns 06_H 187ns 07_H 213ns (default) 08_H 240ns 09_H 267ns $0A_H$ 293ns $0B_H$ 320ns $0C_H$ 347ns $0D_H$ 373ns $0E_H$ 400ns $0F_H$ 427ns 10_H 453ns 11_H 480ns 12_H 507ns 13_H 533ns 14_H 560ns 15_H 587ns 16_H 613ns 17_H 640ns 18_H 667ns 19_H 693ns $1A_H$ 720ns $1B_H$ 747ns $1C_H$ 773ns $1D_H$ 800ns $1E_H$ 827ns $1F_H$ 853ns 20_H 880ns 21_H 907ns 22_H 933ns 23_H 960ns 24_H 987ns 25_H 1013ns 26_H 1040ns 27_H 1067ns 28_H 1093ns 29_H 1120ns $2A_H$ 1147ns $2B_H$ 1173ns $2C_H$ 1200ns

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 1227ns $2E_H$ 1253ns $2F_H$ 1280ns 30_H 1307ns 31_H 1333ns 32_H 1360ns 33_H 1387ns 34_H 1413ns 35_H 1440ns 36_H 1467ns 37_H 1493ns 38_H 1520ns 39_H 1547ns $3A_H$ 1573ns $3B_H$ 1600ns $3C_H$ 1627ns $3D_H$ 1653ns $3E_H$ 1680ns $3F_H$ 1707ns
0	7:6, 15:14	res	**Reserved** Read as 0; shall be written with 0.

2.12 Gate Driver Configuration register - TON_LS

TON_LS Offset address: $0B_H$

Gate Driver Configuration register - TON_LS DefaultReset value: 0717_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**T1ON_LS**						**0**		**T2ON_LS**					
res		rw						res		rw					

Field	Bits	Type	Description
T2ON_LS	5:0	rw	**Low Side gate driver charge time configuration** 00_H 27ns 01_H 53ns 02_H 80ns 03_H 107ns 04_H 133ns 05_H 160ns 06_H 187ns 07_H 213ns 08_H 240ns 09_H 267ns $0A_H$ 293ns $0B_H$ 320ns $0C_H$ 347ns $0D_H$ 373ns $0E_H$ 400ns $0F_H$ 427ns 10_H 453ns 11_H 480ns 12_H 507ns 13_H 533ns 14_H 560ns 15_H 587ns 16_H 613ns 17_H 640ns (Default) 18_H 667ns 19_H 693ns $1A_H$ 720ns $1B_H$ 747ns $1C_H$ 773ns $1D_H$ 800ns $1E_H$ 827ns $1F_H$ 853ns 20_H 880ns 21_H 907ns 22_H 933ns 23_H 960ns 24_H 987ns 25_H 1013ns 26_H 1040ns 27_H 1067ns 28_H 1093ns 29_H 1120ns $2A_H$ 1147ns $2B_H$ 1173ns $2C_H$ 1200ns

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 1227ns $2E_H$ 1253ns $2F_H$ 1280ns 30_H 1307ns 31_H 1333ns 32_H 1360ns 33_H 1387ns 34_H 1413ns 35_H 1440ns 36_H 1467ns 37_H 1493ns 38_H 1520ns 39_H 1547ns $3A_H$ 1573ns $3B_H$ 1600ns $3C_H$ 1627ns $3D_H$ 1653ns $3E_H$ 1680ns $3F_H$ 1707ns

(table continues...)

(continued)

Field	Bits	Type	Description
T1ON_LS	13:8	rw	**Low Side gate driver pre-charge time configuration** 00_H 27ns 01_H 53ns 02_H 80ns 03_H 107ns 04_H 133ns 05_H 160ns 06_H 187ns 07_H 213ns (default) 08_H 240ns 09_H 267ns $0A_H$ 293ns $0B_H$ 320ns $0C_H$ 347ns $0D_H$ 373ns $0E_H$ 400ns $0F_H$ 427ns 10_H 453ns 11_H 480ns 12_H 507ns 13_H 533ns 14_H 560ns 15_H 587ns 16_H 613ns 17_H 640ns 18_H 667ns 19_H 693ns $1A_H$ 720ns $1B_H$ 747ns $1C_H$ 773ns $1D_H$ 800ns $1E_H$ 827ns $1F_H$ 853ns 20_H 880ns 21_H 907ns 22_H 933ns 23_H 960ns 24_H 987ns 25_H 1013ns 26_H 1040ns 27_H 1067ns 28_H 1093ns 29_H 1120ns $2A_H$ 1147ns $2B_H$ 1173ns $2C_H$ 1200ns

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 1227ns $2E_H$ 1253ns $2F_H$ 1280ns 30_H 1307ns 31_H 1333ns 32_H 1360ns 33_H 1387ns 34_H 1413ns 35_H 1440ns 36_H 1467ns 37_H 1493ns 38_H 1520ns 39_H 1547ns $3A_H$ 1573ns $3B_H$ 1600ns $3C_H$ 1627ns $3D_H$ 1653ns $3E_H$ 1680ns $3F_H$ 1707ns
0	7:6, 15:14	res	**Reserved** Read as 0; shall be written with 0.

2.13 Gate Driver Configuration register - TOFF_HS

TOFF_HS Offset address: $0C_H$

Gate Driver Configuration register - TOFF_HS DefaultReset value: 0717_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**T1OFF_HS**						**0**		**T2OFF_HS**					
res		rw						res		rw					

Field	Bits	Type	Description
T2OFF_HS	5:0	rw	**High Side gate driver discharge time configuration** 00_H 27ns 01_H 53ns 02_H 80ns 03_H 107ns 04_H 133ns 05_H 160ns 06_H 187ns 07_H 213ns 08_H 240ns 09_H 267ns $0A_H$ 293ns $0B_H$ 320ns $0C_H$ 347ns $0D_H$ 373ns $0E_H$ 400ns $0F_H$ 427ns 10_H 453ns 11_H 480ns 12_H 507ns 13_H 533ns 14_H 560ns 15_H 587ns 16_H 613ns 17_H 640ns (Default) 18_H 667ns 19_H 693ns $1A_H$ 720ns $1B_H$ 747ns $1C_H$ 773ns $1D_H$ 800ns $1E_H$ 827ns $1F_H$ 853ns 20_H 880ns 21_H 907ns 22_H 933ns 23_H 960ns 24_H 987ns 25_H 1013ns 26_H 1040ns 27_H 1067ns 28_H 1093ns 29_H 1120ns $2A_H$ 1147ns $2B_H$ 1173ns $2C_H$ 1200ns

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 1227ns $2E_H$ 1253ns $2F_H$ 1280ns 30_H 1307ns 31_H 1333ns 32_H 1360ns 33_H 1387ns 34_H 1413ns 35_H 1440ns 36_H 1467ns 37_H 1493ns 38_H 1520ns 39_H 1547ns $3A_H$ 1573ns $3B_H$ 1600ns $3C_H$ 1627ns $3D_H$ 1653ns $3E_H$ 1680ns $3F_H$ 1707ns

(table continues...)

(continued)

Field	Bits	Type	Description
T1OFF_HS	13:8	rw	**High Side gate driver pre-discharge time configuration** 00_H 27ns 01_H 53ns 02_H 80ns 03_H 107ns 04_H 133ns 05_H 160ns 06_H 187ns 07_H 213ns (default) 08_H 240ns 09_H 267ns $0A_H$ 293ns $0B_H$ 320ns $0C_H$ 347ns $0D_H$ 373ns $0E_H$ 400ns $0F_H$ 427ns 10_H 453ns 11_H 480ns 12_H 507ns 13_H 533ns 14_H 560ns 15_H 587ns 16_H 613ns 17_H 640ns 18_H 667ns 19_H 693ns $1A_H$ 720ns $1B_H$ 747ns $1C_H$ 773ns $1D_H$ 800ns $1E_H$ 827ns $1F_H$ 853ns 20_H 880ns 21_H 907ns 22_H 933ns 23_H 960ns 24_H 987ns 25_H 1013ns 26_H 1040ns 27_H 1067ns 28_H 1093ns 29_H 1120ns $2A_H$ 1147ns $2B_H$ 1173ns $2C_H$ 1200ns

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 1227ns $2E_H$ 1253ns $2F_H$ 1280ns 30_H 1307ns 31_H 1333ns 32_H 1360ns 33_H 1387ns 34_H 1413ns 35_H 1440ns 36_H 1467ns 37_H 1493ns 38_H 1520ns 39_H 1547ns $3A_H$ 1573ns $3B_H$ 1600ns $3C_H$ 1627ns $3D_H$ 1653ns $3E_H$ 1680ns $3F_H$ 1707ns
0	7:6, 15:14	res	**Reserved** Read as 0; shall be written with 0.

2.14 Gate Driver Configuration register - TOFF_LS

TOFF_LS Offset address: $0D_H$

Gate Driver Configuration register - TOFF_LS DefaultReset value: 0717_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**T1OFF_LS**						**0**		**T2OFF_LS**					
res		rw						res		rw					

Field	Bits	Type	Description
T2OFF_LS	5:0	rw	**Low Side gate driver discharge time configuration** 00_H 27ns 01_H 53ns 02_H 80ns 03_H 107ns 04_H 133ns 05_H 160ns 06_H 187ns 07_H 213ns 08_H 240ns 09_H 267ns $0A_H$ 293ns $0B_H$ 320ns $0C_H$ 347ns $0D_H$ 373ns $0E_H$ 400ns $0F_H$ 427ns 10_H 453ns 11_H 480ns 12_H 507ns 13_H 533ns 14_H 560ns 15_H 587ns 16_H 613ns 17_H 640ns (Default) 18_H 667ns 19_H 693ns $1A_H$ 720ns $1B_H$ 747ns $1C_H$ 773ns $1D_H$ 800ns $1E_H$ 827ns $1F_H$ 853ns 20_H 880ns 21_H 907ns 22_H 933ns 23_H 960ns 24_H 987ns 25_H 1013ns 26_H 1040ns 27_H 1067ns 28_H 1093ns 29_H 1120ns $2A_H$ 1147ns $2B_H$ 1173ns $2C_H$ 1200ns

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 1227ns $2E_H$ 1253ns $2F_H$ 1280ns 30_H 1307ns 31_H 1333ns 32_H 1360ns 33_H 1387ns 34_H 1413ns 35_H 1440ns 36_H 1467ns 37_H 1493ns 38_H 1520ns 39_H 1547ns $3A_H$ 1573ns $3B_H$ 1600ns $3C_H$ 1627ns $3D_H$ 1653ns $3E_H$ 1680ns $3F_H$ 1707ns

(table continues...)

(continued)

Field	Bits	Type	Description
T1OFF_LS	13:8	rw	**Low Side gate driver pre-discharge time configuration** 00_H 27ns 01_H 53ns 02_H 80ns 03_H 107ns 04_H 133ns 05_H 160ns 06_H 187ns 07_H 213ns (default) 08_H 240ns 09_H 267ns $0A_H$ 293ns $0B_H$ 320ns $0C_H$ 347ns $0D_H$ 373ns $0E_H$ 400ns $0F_H$ 427ns 10_H 453ns 11_H 480ns 12_H 507ns 13_H 533ns 14_H 560ns 15_H 587ns 16_H 613ns 17_H 640ns 18_H 667ns 19_H 693ns $1A_H$ 720ns $1B_H$ 747ns $1C_H$ 773ns $1D_H$ 800ns $1E_H$ 827ns $1F_H$ 853ns 20_H 880ns 21_H 907ns 22_H 933ns 23_H 960ns 24_H 987ns 25_H 1013ns 26_H 1040ns 27_H 1067ns 28_H 1093ns 29_H 1120ns $2A_H$ 1147ns $2B_H$ 1173ns $2C_H$ 1200ns

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 1227ns $2E_H$ 1253ns $2F_H$ 1280ns 30_H 1307ns 31_H 1333ns 32_H 1360ns 33_H 1387ns 34_H 1413ns 35_H 1440ns 36_H 1467ns 37_H 1493ns 38_H 1520ns 39_H 1547ns $3A_H$ 1573ns $3B_H$ 1600ns $3C_H$ 1627ns $3D_H$ 1653ns $3E_H$ 1680ns $3F_H$ 1707ns
0	7:6, 15:14	res	**Reserved** Read as 0; shall be written with 0.

2.15 Gate Driver Configuration register - T3OFF

T3OFF Offset address: $0E_H$

Gate Driver Configuration register - T3OFF DefaultReset value: 1717_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**T3OFF_HS**						**0**		**T3OFF_LS**					
res		rw						res		rw					

Field	Bits	Type	Description
T3OFF_LS	5:0	rw	**Low Side gate driver post-discharge time configuration** 00_H 27ns 01_H 53ns 02_H 80ns 03_H 107ns 04_H 133ns 05_H 160ns 06_H 187ns 07_H 213ns 08_H 240ns 09_H 267ns $0A_H$ 293ns $0B_H$ 320ns $0C_H$ 347ns $0D_H$ 373ns $0E_H$ 400ns $0F_H$ 427ns 10_H 453ns 11_H 480ns 12_H 507ns 13_H 533ns 14_H 560ns 15_H 587ns 16_H 613ns 17_H 640ns (Default) 18_H 667ns 19_H 693ns $1A_H$ 720ns $1B_H$ 747ns $1C_H$ 773ns $1D_H$ 800ns $1E_H$ 827ns $1F_H$ 853ns 20_H 880ns 21_H 907ns 22_H 933ns 23_H 960ns 24_H 987ns 25_H 1013ns 26_H 1040ns 27_H 1067ns 28_H 1093ns 29_H 1120ns $2A_H$ 1147ns $2B_H$ 1173ns $2C_H$ 1200ns

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 1227ns $2E_H$ 1253ns $2F_H$ 1280ns 30_H 1307ns 31_H 1333ns 32_H 1360ns 33_H 1387ns 34_H 1413ns 35_H 1440ns 36_H 1467ns 37_H 1493ns 38_H 1520ns 39_H 1547ns $3A_H$ 1573ns $3B_H$ 1600ns $3C_H$ 1627ns $3D_H$ 1653ns $3E_H$ 1680ns $3F_H$ 1707ns

(table continues...)

(continued)

Field	Bits	Type	Description
T3OFF_HS	13:8	rw	**High Side gate driver post-discharge time configuration** 00_H 27ns 01_H 53ns 02_H 80ns 03_H 107ns 04_H 133ns 05_H 160ns 06_H 187ns 07_H 213ns 08_H 240ns 09_H 267ns $0A_H$ 293ns $0B_H$ 320ns $0C_H$ 347ns $0D_H$ 373ns $0E_H$ 400ns $0F_H$ 427ns 10_H 453ns 11_H 480ns 12_H 507ns 13_H 533ns 14_H 560ns 15_H 587ns 16_H 613ns 17_H 640ns (Default) 18_H 667ns 19_H 693ns $1A_H$ 720ns $1B_H$ 747ns $1C_H$ 773ns $1D_H$ 800ns $1E_H$ 827ns $1F_H$ 853ns 20_H 880ns 21_H 907ns 22_H 933ns 23_H 960ns 24_H 987ns 25_H 1013ns 26_H 1040ns 27_H 1067ns 28_H 1093ns 29_H 1120ns $2A_H$ 1147ns $2B_H$ 1173ns $2C_H$ 1200ns

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 1227ns $2E_H$ 1253ns $2F_H$ 1280ns 30_H 1307ns 31_H 1333ns 32_H 1360ns 33_H 1387ns 34_H 1413ns 35_H 1440ns 36_H 1467ns 37_H 1493ns 38_H 1520ns 39_H 1547ns $3A_H$ 1573ns $3B_H$ 1600ns $3C_H$ 1627ns $3D_H$ 1653ns $3E_H$ 1680ns $3F_H$ 1707ns
0	7:6, 15:14	res	**Reserved** Read as 0; shall be written with 0.

2.16 Gate driver Configuration register - ION_HS1

ION_HS1 Offset address: $0F_H$

Gate driver Configuration register - ION_HS1 DefaultReset value: 2020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ION_HS_BNK		**I1ON_HS1**						**0**		**I2ON_HS1**					
rw		rw						res		rw					

Field	Bits	Type	Description
I2ON_HS1	5:0	rw	**HS1 Gate Driver charge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
I1ON_HS1	13:8	rw	**HS1 Gate Driver pre-charge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)
ION_HS_BNK	15:14	rw	**Banking configuration of I1ON, I2ON HS charge current** 00_B I1ON_HS1 pre-charge current settings applied for all 3x HS MOSFET gate drivers, I2ON_HS1 charge current setting applied only for all 3xHS MOSFET gate drivers (Default) 01_B reserved 10_B reserved 11_B I1ON_HS1 pre-charge current setting applied only for HS1 MOSFET gate driver, I2ON_HS1 charge current setting applied only for HS1 MOSFET gate driver
0	7:6	res	**Reserved** Read as 0; shall be written with 0.

2.17 Gate driver Configuration register - ION_LS1

ION_LS1 Offset address: 10_H

Gate driver Configuration register - ION_LS1 DefaultReset value: 2020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ION_LS_BNK		**I1ON_LS1**						**0**		**I2ON_LS1**					
rw		rw						res		rw					

Field	Bits	Type	Description
I2ON_LS1	5:0	rw	**LS1 Gate Driver charge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
I1ON_LS1	13:8	rw	**LS1 Gate Driver pre-charge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)
ION_LS_BNK	15:14	rw	**Banking configuration of I1ON, I2ON LS charge current** 00_B I1ON_LS1 pre-charge current settings applied for all 3x LS MOSFET gate drivers , I2ON_LS1 charge current setting applied only for all 3x LS MOSFET gate drivers (Default) 01_B reserved 10_B reserved 11_B I1ON_LS1 pre-charge current setting applied only for LS1 MOSFET gate driver , I2ON_LS1 charge current setting applied only for LS1 MOSFET gate driver
0	7:6	res	**Reserved** Read as 0; shall be written with 0.

2.18 Gate driver Configuration register - ION_HS2

ION_HS2 Offset address: 11_H

Gate driver Configuration register - ION_HS2 DefaultReset value: 2020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**I1ON_HS2**						**0**		**I2ON_HS2**					
res		rw						res		rw					

Field	Bits	Type	Description
I2ON_HS2	5:0	rw	**HS2 Gate Driver charge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
I1ON_HS2	13:8	rw	**HS2 Gate Driver pre-charge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)
0	7:6, 15:14	res	**Reserved** Read as 0; shall be written with 0.

2.19 Gate driver Configuration register - ION_LS2

ION_LS2 Offset address: 12_H

Gate driver Configuration register - ION_LS2 DefaultReset value: 2020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**I1ON_LS2**						**0**		**I2ON_LS2**					
res		rw						res		rw					

Field	Bits	Type	Description
I2ON_LS2	5:0	rw	**LS2 Gate Driver charge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
I1ON_LS2	13:8	rw	**LS2 Gate Driver pre-charge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)
0	7:6, 15:14	res	**Reserved** Read as 0; shall be written with 0.

2.20 Gate driver Configuration register - ION_HS3

ION_HS3 Offset address: 13_H

Gate driver Configuration register - ION_HS3 DefaultReset value: 2020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**I1ON_HS3**						**0**		**I2ON_HS3**					
res		rw						res		rw					

Field	Bits	Type	Description
I2ON_HS3	5:0	rw	**HS3 Gate Driver charge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
I1ON_HS3	13:8	rw	**HS3 Gate Driver pre-charge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)
0	7:6, 15:14	res	**Reserved** Read as 0; shall be written with 0.

2.21 Gate driver Configuration register - ION_LS3

ION_LS3 Offset address: 14_H

Gate driver Configuration register - ION_LS3 DefaultReset value: 2020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**I1ON_LS3**						**0**		**I2ON_LS3**					
res		rw						res		rw					

Field	Bits	Type	Description
I2ON_LS3	5:0	rw	**LS3 Gate Driver charge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
I1ON_LS3	13:8	rw	**LS3 Gate Driver pre-charge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)
0	7:6, 15:14	res	**Reserved** Read as 0; shall be written with 0.

2.22 Gate driver Configuration register - I3ON

I3ON Offset address: 15_H

Gate driver Configuration register - I3ON DefaultReset value: 2020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**I3ON_HS**						**0**		**I3ON_LS**					
res		rw						res		rw					

Field	Bits	Type	Description
I3ON_LS	5:0	rw	**Low Side gate driver post-charge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
I3ON_HS	13:8	rw	**High Side gate driver post-charge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)
0	7:6, 15:14	res	**Reserved** Read as 0; shall be written with 0.

2.23 Gate driver Configuration register - ION_IOFF_DIDT

ION_IOFF_DIDT Offset address: 16_H

Gate driver Configuration register - ION_IOFF_DIDT DefaultReset value: 2020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**ION**						**0**		**IOFF**					
res		rw						res		rw					

Field	Bits	Type	Description
IOFF	5:0	rw	**Gate driver discharge current during dI/dT phase** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
ION	13:8	rw	**Gate driver charge current during dI/dT phase** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)
0	7:6, 15:14	res	**Reserved** Read as 0; shall be written with 0.

2.24 Gate driver Configuration register - IOFF_HS1

IOFF_HS1 Offset address: 17_H

Gate driver Configuration register - IOFF_HS1 DefaultReset value: 2020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOFF_HS_BNK		**I1OFF_HS1**						**0**		**I2OFF_HS1**					
rw		rw						res		rw					

Field	Bits	Type	Description
I2OFF_HS1	5:0	rw	**HS1 Gate Driver discharge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
I1OFF_HS1	13:8	rw	**HS1 Gate Driver pre-discharge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)
IOFF_HS_BNK	15:14	rw	**Banking configuration of I1OFF, I2OFF HS discharge current** 00_B I1OFF_HS1 pre-discharge current settings applied for all 3x HS MOSFET gate drivers , I2OFF_HS1 discharge current setting applied only for all 3xHS MOSFET gate drivers (Default) 01_B reserved 10_B reserved 11_B I1OFF_HS1 pre-discharge current setting applied only for HS1 MOSFET gate driver, I2OFF_HS1 discharge current setting applied only for HS1 MOSFET gate driver
0	7:6	res	**Reserved** Read as 0; shall be written with 0.

2.25 Gate driver Configuration register - IOFF_LS1

IOFF_LS1 Offset address: 18_H

Gate driver Configuration register - IOFF_LS1 DefaultReset value: 2020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOFF_LS_BNK		**I1OFF_LS1**						**0**		**I2OFF_LS1**					
rw		rw						res		rw					

Field	Bits	Type	Description
I2OFF_LS1	5:0	rw	**LS1 Gate Driver discharge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
I1OFF_LS1	13:8	rw	**LS1 Gate Driver pre-discharge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)
IOFF_LS_BNK	15:14	rw	**Banking configuration of I1OFF, I2OFF LS discharge current** 00_B I1OFF_LS1 pre-discharge current settings applied for all 3x LS MOSFET gate drivers , I2OFF_LS1 discharge current setting applied only for all 3x LS MOSFET gate drivers (Default) 01_B reserved 10_B reserved 11_B I1OFF_LS1 pre-discharge current setting applied only for LS1 MOSFET gate driver , I2OFF_LS1 discharge current setting applied only for LS1 MOSFET gate driver
0	7:6	res	**Reserved** Read as 0; shall be written with 0.

2.26 Gate driver Configuration register - IOFF_HS2

IOFF_HS2 Offset address: 19_H

Gate driver Configuration register - IOFF_HS2 DefaultReset value: 2020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**I1OFF_HS2**						**0**		**I2OFF_HS2**					
res		rw						res		rw					

Field	Bits	Type	Description
I2OFF_HS2	5:0	rw	**HS2 Gate Driver discharge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
I1OFF_HS2	13:8	rw	**HS2 Gate Driver pre-discharge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)
0	7:6, 15:14	res	**Reserved** Read as 0; shall be written with 0.

2.27 Gate driver Configuration register - IOFF_LS2

IOFF_LS2 Offset address: $1A_H$

Gate driver Configuration register - IOFF_LS2 DefaultReset value: 2020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**I1OFF_LS2**						**0**		**I2OFF_LS2**					
res		rw						res		rw					

Field	Bits	Type	Description
I2OFF_LS2	5:0	rw	**LS2 Gate Driver discharge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
I1OFF_LS2	13:8	rw	**LS2 Gate Driver pre-discharge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)
0	7:6, 15:14	res	**Reserved** Read as 0; shall be written with 0.

2.28 Gate driver Configuration register - IOFF_HS3

IOFF_HS3 Offset address: $1B_H$

Gate driver Configuration register - IOFF_HS3 DefaultReset value: 2020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**I1OFF_HS3**						**0**		**I2OFF_HS3**					
res		rw						res		rw					

Field	Bits	Type	Description
I2OFF_HS3	5:0	rw	**HS3 Gate Driver discharge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
I1OFF_HS3	13:8	rw	**HS3 Gate Driver pre-discharge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)
0	7:6, 15:14	res	**Reserved** Read as 0; shall be written with 0.

2.29 Gate driver Configuration register - IOFF_LS3

IOFF_LS3 Offset address: $1C_H$

Gate driver Configuration register - IOFF_LS3 DefaultReset value: 2020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**I1OFF_LS3**						**0**		**I2OFF_LS3**					
res		rw						res		rw					

Field	Bits	Type	Description
I2OFF_LS3	5:0	rw	**LS3 Gate Driver discharge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
I1OFF_LS3	13:8	rw	**LS3 Gate Driver pre-discharge current setting** 00_H 0.5mA (GDRV_RNG = 0), 1mA (GDRV_RNG = 1) 01_H 0.7mA (GDRV_RNG = 0), 1.4mA (GDRV_RNG = 1) 02_H 0.8mA (GDRV_RNG = 0), 1.8mA (GDRV_RNG = 1) 03_H 1.1mA (GDRV_RNG = 0), 2.3mA (GDRV_RNG = 1) 04_H 1.3mA (GDRV_RNG = 0), 2.9mA (GDRV_RNG = 1) 05_H 1.6mA (GDRV_RNG = 0), 3.5mA (GDRV_RNG = 1) 06_H 2mA (GDRV_RNG = 0), 4.3mA (GDRV_RNG = 1) 07_H 2.4mA (GDRV_RNG = 0), 5.2mA (GDRV_RNG = 1) 08_H 2.8mA (GDRV_RNG = 0), 6.2mA (GDRV_RNG = 1) 09_H 3.4mA (GDRV_RNG = 0), 7.3mA (GDRV_RNG = 1) $0A_H$ 3.9mA (GDRV_RNG = 0), 8.5mA (GDRV_RNG = 1) $0B_H$ 4.5mA (GDRV_RNG = 0), 9.8mA (GDRV_RNG = 1) $0C_H$ 5.3mA (GDRV_RNG = 0), 11.1mA (GDRV_RNG = 1) $0D_H$ 6.1mA (GDRV_RNG = 0), 12.5mA (GDRV_RNG = 1) $0E_H$ 6.9mA (GDRV_RNG = 0), 14.2mA (GDRV_RNG = 1) $0F_H$ 7.8mA (GDRV_RNG = 0), 15.9mA (GDRV_RNG = 1) 10_H 8.8mA (GDRV_RNG = 0), 17.7mA (GDRV_RNG = 1) 11_H 9.8mA (GDRV_RNG = 0), 19.5mA (GDRV_RNG = 1) 12_H 10.9mA (GDRV_RNG = 0), 21.4mA (GDRV_RNG = 1) 13_H 12mA (GDRV_RNG = 0), 23.4mA (GDRV_RNG = 1) 14_H 13.3mA (GDRV_RNG = 0), 25.4mA (GDRV_RNG = 1) 15_H 14.4mA (GDRV_RNG = 0), 27.5mA (GDRV_RNG = 1) 16_H 15.9mA (GDRV_RNG = 0), 29.6mA (GDRV_RNG = 1) 17_H 17.3mA (GDRV_RNG = 0), 31.9mA (GDRV_RNG = 1) 18_H 18.7mA (GDRV_RNG = 0), 34.2mA (GDRV_RNG = 1) 19_H 20.2mA (GDRV_RNG = 0), 36.5mA (GDRV_RNG = 1) $1A_H$ 21.7mA (GDRV_RNG = 0), 39mA (GDRV_RNG = 1) $1B_H$ 23.3mA (GDRV_RNG = 0), 41.5mA (GDRV_RNG = 1) $1C_H$ 24.9mA (GDRV_RNG = 0), 43.9mA (GDRV_RNG = 1) $1D_H$ 26.6mA (GDRV_RNG = 0), 47mA (GDRV_RNG = 1) $1E_H$ 28.2mA (GDRV_RNG = 0), 49.1mA (GDRV_RNG = 1) $1F_H$ 30mA (GDRV_RNG = 0), 51.8mA (GDRV_RNG = 1) 20_H 31.8mA (GDRV_RNG = 0), 54.5mA (GDRV_RNG = 1) (default) 21_H 33.7mA (GDRV_RNG = 0), 57.2mA (GDRV_RNG = 1) 22_H 35.5mA (GDRV_RNG = 0), 60mA (GDRV_RNG = 1) 23_H 37.4mA (GDRV_RNG = 0), 63mA (GDRV_RNG = 1) 24_H 39.4mA (GDRV_RNG = 0), 66mA (GDRV_RNG = 1) 25_H 41.4mA (GDRV_RNG = 0), 69mA (GDRV_RNG = 1) 26_H 43.4mA (GDRV_RNG = 0), 71.7mA (GDRV_RNG = 1) 27_H 45.4mA (GDRV_RNG = 0), 74.5mA (GDRV_RNG = 1) 28_H 47.4mA (GDRV_RNG = 0), 77.8mA (GDRV_RNG = 1) 29_H 49.6mA (GDRV_RNG = 0), 80.9mA (GDRV_RNG = 1) $2A_H$ 51.7mA (GDRV_RNG = 0), 84mA (GDRV_RNG = 1) $2B_H$ 53.9mA (GDRV_RNG = 0), 87.1mA (GDRV_RNG = 1) $2C_H$ 56mA (GDRV_RNG = 0), 90.2mA (GDRV_RNG = 1)

(table continues...)

(continued)

Field	Bits	Type	Description
			$2D_H$ 58.2mA (GDRV_RNG = 0), 93.3mA (GDRV_RNG = 1) $2E_H$ 60.4mA (GDRV_RNG = 0), 96.5mA (GDRV_RNG = 1) $2F_H$ 62.6mA (GDRV_RNG = 0), 99.7mA (GDRV_RNG = 1) 30_H 65mA (GDRV_RNG = 0), 102.9mA (GDRV_RNG = 1) 31_H 67.3mA (GDRV_RNG = 0), 106mA (GDRV_RNG = 1) 32_H 69.6mA (GDRV_RNG = 0), 109.5mA (GDRV_RNG = 1) 33_H 72mA (GDRV_RNG = 0), 112.6mA (GDRV_RNG = 1) 34_H 74.3mA (GDRV_RNG = 0), 115.7mA (GDRV_RNG = 1) 35_H 76.7mA (GDRV_RNG = 0), 119mA (GDRV_RNG = 1) 36_H 79.1mA (GDRV_RNG = 0), 122.4mA (GDRV_RNG = 1) 37_H 81.5mA (GDRV_RNG = 0), 125.8mA (GDRV_RNG = 1) 38_H 83.9mA (GDRV_RNG = 0), 129.1mA (GDRV_RNG = 1) 39_H 86.4mA (GDRV_RNG = 0), 132.4mA (GDRV_RNG = 1) $3A_H$ 88.9mA (GDRV_RNG = 0), 135.7mA (GDRV_RNG = 1) $3B_H$ 91.4mA (GDRV_RNG = 0), 139mA (GDRV_RNG = 1) $3C_H$ 93.9mA (GDRV_RNG = 0), 142.4mA (GDRV_RNG = 1) $3D_H$ 96.4mA (GDRV_RNG = 0), 145.8mA (GDRV_RNG = 1) $3E_H$ 99mA (GDRV_RNG = 0), 149.2mA (GDRV_RNG = 1) $3F_H$ 101.5mA (GDRV_RNG = 0), 152.6mA (GDRV_RNG = 1)
0	7:6, 15:14	res	**Reserved** Read as 0; shall be written with 0.

2.30 Current sense amplifier configuration register

CSA_CFG Offset address: $1D_H$

Current sense amplifier configuration register DefaultReset value: 0075_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		CSA_REC	CSO_MUX			CSA_GAIN_TST	CSA_GAIN			CSA_DIR	CSA_CLOAD	CSA_OC_TH		CSA_TFOC	
res		rw	rw			rw	rw			rw	rw	rw		rw	

Field	Bits	Type	Description
CSA_TFOC	1:0	rw	**Current sense amplifier overcurrent filter time setting** 00_B 3us 01_B 6us (Default) 10_B 10us 11_B 50us
CSA_OC_TH	3:2	rw	**Current sense amplifier overcurrent detection threshold** 00_B 0.75xVREF and 0.25xVREF threshold settings 01_B 0.8xVREF and 0.2xVREF threshold settings (Default) 10_B 0.85xVREF and 0.15xVREF threshold settings 11_B 0.9xVREF and 0.1xVREF threshold settings
CSA_CLOAD	4	rw	**Current sense amplifier output capacitive load range** 0_B CSA output capacitive load CLOAD <400pF 1_B CSA output capacitive load ~2.2nF (Default)
CSA_DIR	5	rw	**Direction of current sense amplifier** 0_B unidirectional current measurement 1_B bidirectional current measurement (Default)
CSA_GAIN	8:6	rw	**Current sense amplifier differential gain configuration** 000_B Differential gain 6V/V selected 001_B Differential gain 8V/V selected (Default) 010_B Differential gain 10V/V selected 011_B Differential gain 15V/V selected 100_B Differential gain 24V/V selected 101_B Differential gain 40V/V selected 110_B reserved 111_B reserved
CSA_GAIN_TST	9	rw	**CSA gain check function** 0_B gain check function disabled (Default) 1_B gain check function enabled

(table continues...)

(continued)

Field	Bits	Type	Description
CSO_MUX	12:10	rw	**Current Sense Amplifier Output redirection of digital PFB signals** 000_B CSA normal functionality (Default) 001_B PFB1 redirected to CSO output 010_B PFB2 redirected to CSO output 011_B PFB3 redirected to CSO output 100_B XOR of PFB1,2,3 redirected to CSO output 101_B reserved … 111_B reserved
CSA_REC	13	rw	**CSA recovery in case of VIO under-voltage event** 0_B CSA automatic restart disabled (default) 1_B CSA automatic restart enabled, CSA restarts when VIO_UV event not present (independent of VIO_UV status bit)
0	15:14	res	**Reserved** Read as 0; shall be written with 0.

2.31 Failure reaction configuration register 1

FAILURE_CFG Offset address: $1E_H$

Failure reaction configuration register 1 DefaultReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**DSOV_FM**	**PFB_FM**	**IPV_CCP_FM**	**IPV_STP_FM**	**ERRN_FM**	**TW_FM**	**WD_FM**	**OTP_ERR_FM**	**INHN_REC_FM**	**SDO_SHORT_FM**	**PWM_CHK_FM**	**CSA_SUP_UV_FM**		**CSA_OC_FM**	
res	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	

Field	Bits	Type	Description
CSA_OC_FM	1:0	rw	**Current sense amplifiers overcurrent failure reaction** 00_B latched error 1 (LE1) failure reaction triggered (Default) 01_B error (E) failure reaction triggered 10_B warning (W) failure reaction triggered 11_B latched error 1 (LE1) with automatic PWM recovery when event is not present
CSA_SUP_UV_FM	3:2	rw	**Internal supply of CSA module under-voltage failure reaction** 00_B warning (W) failure reaction triggered (Default) 01_B error (E) failure reaction triggered 10_B latched error 1 (LE1) failure reaction triggered 11_B reserved
PWM_CHK_FM	4	rw	**Failure reaction in case of missing PWM alternation detection** 0_B error (E) failure reaction triggered (Default) 1_B warning (W) failure reaction triggered
SDO_SHORT_FM	5	rw	**SDO short to supply OR ground failure reaction** 0_B error (E) failure reaction triggered (Default) 1_B latched error 1 (LE1) failure reaction triggered
INHN_REC_FM	6	rw	**INHN recovery after INHN low level reaction** 0_B once INHN high detected PWM control automatic restart (Default) 1_B once INHN high detected, forced safe state kept until INHN_L_DET cleared
OTP_ERR_FM	7	rw	**OTP module error failure reaction configuration** 0_B latched error 1 (LE1) failure reaction triggered (Default) 1_B warning (W) failure reaction triggered
WD_FM	8	rw	**Window watchdog failure reaction** 0_B latched error 1 (LE1) failure reaction triggered (Default) 1_B error (E) failure reaction triggered
TW_FM	9	rw	**Temperature warning failure reaction** 0_B warning (W) failure reaction triggered (Default) 1_B latched error 1 (LE1) failure reaction triggered

(table continues...)

(continued)

Field	Bits	Type	Description
ERRN_FM	10	rw	**ERRN short to supply failure reaction** 0_B latched error 1 (LE1) failure reaction triggered (Default) 1_B warning (W) failure reaction triggered
IPV_STP_FM	11	rw	**Shoot-through protection violation failure reaction** 0_B latched error 1 (LE1) failure reaction triggered (Default) 1_B warning (W) failure reaction triggered
IPV_CCP_FM	12	rw	**Input pattern violation due to TCCP violation failure reaction** 0_B latched error 1 (LE1) failure reaction triggered (Default) 1_B warning (W) failure reaction triggered
PFB_FM	13	rw	**Phase feedback monitoring failure reaction** 0_B latched error 1 (LE1) failure reaction triggered (Default) 1_B warning (W) failure reaction triggered
DSOV_FM	14	rw	**Drain-source overvoltage failure reaction** 0_B latched error 1 (LE1) failure reaction triggered (Default) 1_B latched error 2 (LE2) failure reaction triggered
0	15	res	**Reserved** Read as 0; shall be written with 0.

2.32 Self-test configuration register

SELF_TEST_CFG Offset address: $1F_H$

Self-test configuration register DefaultReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				DSOV_ST	VIO_MON_ST	PFB_ST	TSD_ST	SOFF_ST	VSCP_MON_ST	CPMON_ST	CSA_SUP_ST	CSA_OC_ST	REG_UV_ST	CLK_MON_ST	LAT_FAULT_ST
res				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
LAT_FAULT_ST	0	rw	**Latent faults detector self-test enable** 0_B self-test disabled (Default) 1_B self-test enabled
CLK_MON_ST	1	rw	**Digital core clock monitoring self-test enable** 0_B self-test disabled (Default) 1_B self-test enabled
REG_UV_ST	2	rw	**Internal regulator under voltage self-test enable** 0_B self-test disabled (Default) 1_B self-test enabled
CSA_OC_ST	3	rw	**Current sense amplifier over-current supply self-test enable** 0_B self-test disabled (Default) 1_B self-test enabled
CSA_SUP_ST	4	rw	**Current sense amplifier internal supply self-test enable** 0_B self-test disabled (Default) 1_B self-test enabled
CPMON_ST	5	rw	**VCPH overdrive and undervoltage monitoring Self-test enable** 0_B self-test disabled (Default) 1_B self-test enabled
VSCP_MON_ST	6	rw	**VSCP monitoring self-test enable** 0_B self-test disabled (Default) 1_B self-test enabled
SOFF_ST	7	rw	**Safe state activation path self-test enable** 0_B self-test disabled (Default) 1_B self-test enabled
TSD_ST	8	rw	**Overtemperature monitoring self-test enable** 0_B self-test disabled (Default) 1_B self-test enabled
PFB_ST	9	rw	**PFB logic self-test enable** 0_B self-test disabled (Default) 1_B self-test enabled

(table continues...)

(continued)

Field	Bits	Type	Description
VIO_MON_ST	10	rw	**VIO monitoring self-test enable** 0_B self-test disabled (Default) 1_B self-test enabled
DSOV_ST	11	rw	**Drain-source monitoring self-test enable** 0_B self-test disabled (Default) 1_B self-test enabled
0	15:12	res	**Reserved** Read as 0; shall be written with 0.

2.33 Supply monitoring status register

SUP_STAT Offset address: 25_H

Supply monitoring status register DefaultReset value: 0080_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POR	**0**						**VSCP_UV_SD**	**VSCP_OV_SD**	**VCPH_UV**	**VSCP_L**	**VSCP_H**	**VDH_UV**	**CSA_SUP_UV**	**VIO_UV**	**VIO_OV**
rw1ch	res						rw1ch	rw1ch	rw1ch	r	r	rw1ch	rw1ch	rw1ch	rw1ch

Field	Bits	Type	Description
VIO_OV	0	rw1ch	**VIO overvoltage detection** 0_B no VIO over-voltage detected 1_B VIO over-voltage event detected
VIO_UV	1	rw1ch	**VIO undervoltage detection** 0_B no VIO under-voltage detected 1_B VIO under-voltage event detected
CSA_SUP_UV	2	rw1ch	**Current sense amplifier internal supply undervoltage** 0_B no under-voltage detected 1_B CSA_SUP under-voltage detected
VDH_UV	3	rw1ch	**VDH pin under-voltage detection** 0_B no VDH under voltage detected 1_B VDH under voltage event detection
VSCP_H	4	r	**VSCP High undervoltage detection** 0_B no VSCP_H under-voltage detected 1_B VSCP_H under-voltage event detected
VSCP_L	5	r	**VSCP Low undervoltage detection** 0_B no VSCP_L under-voltage detected 1_B VSCP_L under-voltage detected
VCPH_UV	6	rw1ch	**Charge pump output VCPH undervoltage detection** 0_B no VCPH UV detected 1_B VCPH under-voltage event detected
VSCP_OV_SD	7	rw1ch	**VSCP overvoltage shutdown detection** 0_B no VSCP_OV_SD detected 1_B VSCP_OV_SD over-voltage event detected
VSCP_UV_SD	8	rw1ch	**VSCP undervoltage shutdown detection** 0_B no VSCP_UV_SD detected 1_B VSCP_UV_SD under-voltage event detected
POR	15	rw1ch	**Power on reset detection** 0_B no POR event (since last clear command) 1_B POR event occured

(table continues...)

(continued)

Field	Bits	Type	Description
0	14:9	res	**Reserved** Read as 0; shall be written with 0.

2.34 SPI status register (SPI and WD monitoring)

SPI_STAT Offset address: 26_H

SPI status register [SPI and WD monitoring) DefaultReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OTP_ERR	**0**	**WD_CNT**					**WDE**	**WDLE**	**0**	**SDO_SHORT**	**CSN_TO**	**OFC**	**CRC_FAIL**	**SPI_IA**	**FRAME_ERR**
rw1ch	res	r					r	rw1ch	res	rw1ch	rw1ch	rw1ch	rw1ch	rw1ch	rw1ch

Field	Bits	Type	Description
FRAME_ERR	0	rw1ch	**SPI frame error detection** 0_B no frame error detected 1_B SPI failure due to frame error detected
SPI_IA	1	rw1ch	**Invalid SPI access detection** 0_B no invalid access detected 1_B SPI failure due to invalid access detected
CRC_FAIL	2	rw1ch	**CRC failure detection** 0_B no CRC failure detected 1_B CRC failure detected
OFC	3	rw1ch	**One SPI frame corrupted detection** 0_B no corrupted SPI frame detected since last clear of OFC bit 1_B one corrupted SPI frame detected since last clear of OFC bit
CSN_TO	4	rw1ch	**CSN time-out detection** 0_B no CSN time-out detected 1_B CSN time-out detected
SDO_SHORT	5	rw1ch	**SDO short to supply or ground detection** 0_B no SDO short detected 1_B SDO short to supply or ground detected
WDLE	7	rw1ch	**Watchdog latched error detection** 0_B no watchdog latched error 1_B watchdog latched error detected, WD_CNT reached the WD_FAIL configured number of fails
WDE	8	r	**Watchdog error detection** 0_B no incorrect watchdog service detected 1_B incorrect watchdog service detected

(table continues...)

(continued)

Field	Bits	Type	Description
WD_CNT	13:9	r	**Watchdog error counter** 00_H no WD failure detected 01_H 1 WD failure detected 02_H 2 WD failures detected 03_H 3 WD failures detected 04_H 4 WD failures detected 05_H 5 WD failures detected 06_H 6 WD failures detected 07_H 7 WD failures detected 08_H 8 WD failures detected 09_H 9 WD failures detected $0A_H$ 10 WD failures detected $0B_H$ 11 WD failures detected $0C_H$ 12 WD failures detected $0D_H$ 13 WD failures detected $0E_H$ 14 WD failures detected $0F_H$ 15 WD failures detected
OTP_ERR	15	rw1ch	**OTP configuration error detection** 0_B no OTP error detected during OTP readout 1_B OTP error detected during loading operation
0	6, 14	res	**Reserved** Read as 0; shall be written with 0.

2.35 Device status register 1: Operation mode and digital input pins levels

DEV_STAT1

Offset address: 27_H

Device status register 1: Operation mode and digital input pins levels

Reset values see: Table 27

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV_STAT		**0**		**SOFF_ACT**	**ERR_ACT**	**0**	**IH3N_LVL**	**IH2N_LVL**	**IH1N_LVL**	**IL3_LVL**	**IL2_LVL**	**IL1_LVL**	**INHN_L_DET**	**INH_N_LVL**	**ERR_N_LVL**
r		res		r	r	res	r	r	r	r	r	r	rw1ch	r	r

Field	Bits	Type	Description
ERR_N_LVL	0	r	**ERR_N output pin level monitoring (real time input pin monitoring)** 0_B ERR_N pin voltage level detected as low 1_B ERR_N pin voltage level detected as high
INH_N_LVL	1	r	**INH_N input pin level monitoring (real time input pin monitoring)** 0_B INH_N pin voltage level detected as low 1_B INH_N pin voltage level detected as high
INHN_L_DET	2	rw1ch	**INH_N input pin low level detection (canceled power-down event)** 0_B no INH_N pin voltage low level detected during operation 1_B INH_N pin voltage low level detected during operation
IL1_LVL	3	r	**LS1 PWM input pin level monitoring (real time input pin monitoring)** 0_B IL1 pin voltage level detected as low 1_B IL1 pin voltage level detected as high
IL2_LVL	4	r	**LS2 PWM input pin level monitoring (real time input pin monitoring)** 0_B IL2 pin voltage level detected as low 1_B IL2 pin voltage level detected as high
IL3_LVL	5	r	**LS3 PWM input pin level monitoring (real time input pin monitoring)** 0_B IL3 pin voltage level detected as low 1_B IL3 pin voltage level detected as high
IH1N_LVL	6	r	**HS1 PWM input pin level monitoring (real time input pin monitoring)** 0_B IH1_N pin voltage level detected as low 1_B IH1_N pin voltage level detected as high
IH2N_LVL	7	r	**HS2 PWM input pin level monitoring (real time input pin monitoring)** 0_B IH2_N pin voltage level detected as low 1_B IH2_N pin voltage level detected as high

(table continues...)

(continued)

Field	Bits	Type	Description
IH3N_LVL	8	r	**HS3 PWM input pin level monitoring (real time input pin monitoring)** 0_B IH3_N pin voltage level detected as low 1_B IH3_N pin voltage level detected as high
ERRN_ACT	10	r	**ERR_N pin active low** 0_B ERRN pin not active 1_B ERRN pin activated (active pull low)
SOFF_ACT	11	r	**Safe state activation** 0_B safe state not active 1_B Safe state active
DEV_STAT	15:14	r	**Device operation mode status information** 00_B invalid setting 01_B device in power-up mode 10_B device in normal mode 11_B invalid setting
0	9, 13:12	res	**Reserved** Read as 0; shall be written with 0.

Table 27 Reset values of DEV_STAT1

Reset	Reset value	Note
DefaultReset	0110 100X XXXX XXXX$_B$	Original reset value: 0b0100110XXXXXX010

2.36 Device status register 2: Input pattern violation, ERR_N, CSA, TSD monitoring

DEV_STAT2

Device status register 2: Input pattern violation, ERR_N, CSA, TSD monitoring

Offset address: 28_H

DefaultReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**IPV_CCP_HB3**	**IPV_CCP_HB2**	**IPV_CCP_HB1**	**IPV_STP_HB3**	**IPV_STP_HB2**	**IPV_STP_HB1**	**0**	**PFB3_LE**	**PFB2_LE**	**PFB1_LE**	**ERRN_SHORT**	**CSA_OC**	**TSDW**	**TSD_IC**	**TSD_CP**
res	rw1ch	rw1ch	rw1ch	rw1ch	rw1ch	rw1ch	res	rw1ch	rw1ch	rw1ch	rw1ch	rw1ch	rw1ch	rw1ch	rw1ch

Field	Bits	Type	Description
TSD_CP	0	rw1ch	**Charge pump overtemperature detection** 0_B no charge pump over-temperature detected 1_B charge pump over-temperature detected
TSD_IC	1	rw1ch	**General overtemperature shutdown detection** 0_B no general IC over temperature detected 1_B general IC over temperature event detected
TSDW	2	rw1ch	**Over temperature warning detection** 0_B no over temperature warning detected 1_B over temperature warning detected
CSA_OC	3	rw1ch	**CSA overcurrent detection** 0_B no CSA over current detected 1_B CSA over current detected
ERRN_SHORT	4	rw1ch	**ERR_N pin short to supply detection** 0_B no ERRN pin short to supply detected 1_B ERRN pin short to supply detected
PFB1_LE	5	rw1ch	**Phase feedback monitoring of SH1 latched error detection** 0_B no phase feedback error detected 1_B phase feedback latched error detected
PFB2_LE	6	rw1ch	**Phase feedback monitoring of SH2 latched error detection** 0_B no phase feedback error detected 1_B phase feedback latched error detected
PFB3_LE	7	rw1ch	**Phase feedback monitoring of SH3 latched error detection** 0_B no phase feedback error detected 1_B phase feedback latched error detected
IPV_STP_HB1	9	rw1ch	**Half-bridge 1 input pattern violation due to shoot-through protection** 0_B no shoot-through protection pattern violation for HB1 1_B shoot-through protection input pattern violation for HB1

(table continues...)

(continued)

Field	Bits	Type	Description
IPV_STP_HB2	10	rw1ch	**Half-bridge 2 input pattern violation due to shoot-through protection** 0_B no shoot-through protection input pattern violation for HB2 1_B shoot-through protection input pattern violation for HB2
IPV_STP_HB3	11	rw1ch	**Half-bridge 3 input pattern violation due to shoot-through protection** 0_B no shoot-through protection input pattern violation for HB3 1_B shoot-through protection input pattern violation for HB3
IPV_CCP_HB1	12	rw1ch	**Half-bridge 1 input pattern violation due to cross-current protection** 0_B no cross-current input pattern violation for HB1 1_B cross-current input pattern violation for HB1
IPV_CCP_HB2	13	rw1ch	**Half-bridge 2 input pattern violation due to cross-current protection** 0_B no cross-current input pattern violation for HB2 1_B cross-current input pattern violation for HB2
IPV_CCP_HB3	14	rw1ch	**Half-bridge 3 input pattern violation due to cross-current protection** 0_B no cross-current input pattern violation for HB3 1_B cross-current input pattern violation for HB3
0	8, 15	res	**Reserved** Read as 0; shall be written with 0.

2.37 Latent faults and self-tests status register: internal faults, self-tests results

LF_STAT

Latent faults and self-tests status register: internal faults, self-tests results

Offset address: 29_H

DefaultReset value: 0400_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					SOFF_GDRV	BIAS_LF	0			DSOV_LF_HB3	DSOV_LF_HB2	DSOV_LF_HB1	LAT_FAULT	ST_RDY	ST_RES
res					r	rw1ch	res			rw1ch	rw1ch	rw1ch	rw1ch	rw1ch	r

Field	Bits	Type	Description
ST_RES	0	r	**Self-test result** 0_B no self-test enabled or at least one self-test not successful 1_B all self-test performed (in parallel) were successful
ST_RDY	1	rw1ch	**Self-test status** 0_B self-test not enabled or self-test running 1_B self-test finished
LAT_FAULT	2	rw1ch	**Internal latent fault detection** 0_B no internal latent fault detected 1_B internal latent fault detected
DSOV_LF_HB1	3	rw1ch	**Half-bridge 1 drain-source monitor latent fault detection** 0_B no Drain-Source monitoring latent fault detected in HB1 1_B Drain-Source monitoring latent fault detected in HB1
DSOV_LF_HB2	4	rw1ch	**Half-bridge 2 drain-source monitor latent fault detection** 0_B no Drain-Source monitoring latent fault detected in HB2 1_B Drain-Source monitoring latent fault detected in HB2
DSOV_LF_HB3	5	rw1ch	**Half-bridge 3 drain-source monitor latent fault detection** 0_B no Drain-Source monitoring latent fault detected in HB3 1_B Drain-Source monitoring latent fault detected in HB3
BIAS_LF	9	rw1ch	**Central bias monitoring latent fault detection** 0_B no bias monitoring latent fault detected 1_B central bias monitoring latent fault detected
SOFF_GDRV	10	r	**Safe state entry indication with all 6 gate drivers** 0_B device not in safe state (if SOFF_ACT=0) or at least one gate driver cannot enter safe state (if SOFF_ACT=1) 1_B all 6 gate drivers have entered safe state
0	8:6, 15:11	res	**Reserved** Read as 0; shall be written with 0.

2.38 Phase pins monitoring

SH_LEVEL_STAT Offset address: $2A_H$

Phase pins monitoring DefaultReset value: $3BBF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		PFB3	PFB2	PFB1	0					VSH3_H	VSH3_L	VSH2_H	VSH2_L	VSH1_H	VSH1_L
res		r	r	r	res					r	r	r	r	r	r

Field	Bits	Type	Description
VSH1_L	0	r	**Phase 1 voltage monitoring (SH1) VSHL** 0_B VSH1 < VSHL 1_B VSH1 > VSHL
VSH1_H	1	r	**Phase 1 voltage monitoring (SH1) VSHH** 0_B VSH1 < VSHH 1_B VSH1 > VSHH
VSH2_L	2	r	**Phase 2 voltage monitoring (SH2) VSHL** 0_B VSH2 < VSHL 1_B VSH2 > VSHL
VSH2_H	3	r	**Phase 2 voltage monitoring (SH2) VSHH** 0_B VSH2 < VSHH 1_B VSH2 > VSHH
VSH3_L	4	r	**Phase 3 voltage monitoring (SH3) VSHL** 0_B VSH3 < VSHL 1_B VSH3 > VSHL
VSH3_H	5	r	**Phase 3 voltage monitoring (SH3) VSHH** 0_B VSH3 < VSHH 1_B VSH3 > VSHH
PFB1	11	r	**Phase feedback comparator level of SH1 phase** 0_B SH1 low level detected 1_B SH1 high level detected
PFB2	12	r	**Phase feedback comparator level of SH2 phase** 0_B SH2 low level detected 1_B SH2 high level detected
PFB3	13	r	**Phase feedback comparator level of SH3 phase** 0_B SH3 low level detected 1_B SH3 high level detected
0	10:6, 15:14	res	**Reserved** Read as 0; shall be written with 0.

2.39 HS & LS Gate Drivers monitoring

BD_STAT Offset address: $2B_H$

HS & LS Gate Drivers monitoring DefaultReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**IH3_MISS**	**IH2_MISS**	**IH1_MISS**	**IL3_MISS**	**IL2_MISS**	**IL1_MISS**	**DSOV_HS3**	**DSOV_HS2**	**DSOV_HS1**	**DSOV_LS3**	**DSOV_LS2**	**DSOV_LS1**	**0**		
res	rw1ch	rw1ch	rw1ch	rw1ch	rw1ch	rw1ch	rw1ch	rw1ch	rw1ch	rw1ch	rw1ch	rw1ch	res		

Field	Bits	Type	Description
DSOV_LS1	3	rw1ch	**Drain-source overvoltage monitoring of LS1** 0_B no drain-source overvoltage detected 1_B drain-source overvoltage detected
DSOV_LS2	4	rw1ch	**Drain-source overvoltage monitoring of LS2** 0_B no drain-source overvoltage detected 1_B drain-source overvoltage detected
DSOV_LS3	5	rw1ch	**Drain-source overvoltage monitoring of LS3** 0_B no drain-source overvoltage detected 1_B drain-source overvoltage detected
DSOV_HS1	6	rw1ch	**Drain-source overvoltage monitoring of HS1** 0_B no drain-source over-voltage detected 1_B drain-source over-voltage detected
DSOV_HS2	7	rw1ch	**Drain-source overvoltage monitoring of HS2** 0_B no drain-source over-voltage detected 1_B drain-source over-voltage detected
DSOV_HS3	8	rw1ch	**Drain-source overvoltage monitoring of HS3** 0_B no drain-source over-voltage detected 1_B drain-source over-voltage detected
IL1_MISS	9	rw1ch	**PWM alternation check - detection of stuck IL1 PWM input pin** 0_B IL1 PWM pin functionality ok or PWM alternation check disabled 1_B IL1 PWM pin stuck low detected
IL2_MISS	10	rw1ch	**PWM alternation check - detection of stuck IL2 PWM input pin** 0_B IL3 PWM pin functionality ok or PWM alternation check disabled 1_B IL2 PWM pin stuck low detected
IL3_MISS	11	rw1ch	**PWM alternation check - detection of stuck IL3 PWM input pin** 0_B IL3 PWM pin functionality ok or PWM alternation check disabled 1_B IL3 PWM pin stuck low detected
IH1_MISS	12	rw1ch	**PWM alternation check - detection of stuck IH1_N PWM input pin** 0_B IH1_N PWM pin functionality ok or PWM alternation check disabled 1_B IH1_N PWM pin stuck high detected

(table continues...)

(continued)

Field	Bits	Type	Description
IH2_MISS	13	rw1ch	**PWM alternation check - detection of stuck IH2_N PWM input pin** 0_B IH2_N PWM pin functionality ok or PWM alternation check disabled 1_B IH2_N PWM pin stuck high detected
IH3_MISS	14	rw1ch	**PWM alternation check - detection of stuck IH3_N PWM input pin** 0_B IH3_N PWM pin functionality ok or PWM alternation check disabled 1_B IH3_N PWM pin stuck high detected
0	2:0, 15	res	**Reserved** Read as 0; shall be written with 0.

2.40 Watchdog clock counter

WD_CLK_CNT Offset address: $2C_H$

Watchdog clock counter DefaultReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD_CLK_CNT															
r															

Field	Bits	Type	Description
WD_CLK_CNT	15:0	r	**Internal clock counter between two consecutive correct watchdog services. LSB of nominal 2.4us** 0000_H min. value: read-only data $FFFF_H$ max. value: read-only data

2.41 Phase 1 high time counter

PHASE1_CNT Offset address: $2D_H$

Phase 1 high time counter DefaultReset value: 8000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PFB1	**PFB1_CNT_UPD**	**CNT1_RDY**	**PFB1_H_CNT**												
r	rw1ch	r	r												

Field	Bits	Type	Description
PFB1_H_CNT	12:0	r	**Phase 1 (SH1) high time counter, LSB of nominal 1/fPFB_CNT** 0000_H min. value: read-only data $0FFF_H$ max. value: read-only data
CNT1_RDY	13	r	**PFB1_H counter ready for read indication** 0_B PFB1 counter disabled or counter not ready for read 1_B PFB1 counter ready for read
PFB1_CNT_UPD	14	rw1ch	**PFB1 counter update indication** 0_B PFB1 counter has not been updated at least once since the last SPI read-out 1_B PFB1 counter has been updated at least once since the last SPI read-out
PFB1	15	r	**Phase feedback comparator level of SH1 phase** 0_B SH1 low level detected 1_B SH1 high level detected

2.42 Phase 2 high time counter

PHASE2_CNT Offset address: $2E_H$

Phase 2 high time counter DefaultReset value: 8000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PFB2	**PFB2_CNT_UPD**	**CNT2_RDY**	**PFB2_H_CNT**												
r	rw1ch	r	r												

Field	Bits	Type	Description
PFB2_H_CNT	12:0	r	**Phase 2 (SH2) high time counter, LSB of nominal 1/fPFB_CNT** 0000_H min. value: read-only data $0FFF_H$ max. value: read-only data
CNT2_RDY	13	r	**PFB2_H counter ready for read indication** 0_B PFB2 counter disabled or counter not ready for read 1_B PFB2 counter ready for read
PFB2_CNT_UPD	14	rw1ch	**PFB2 counter update indication** 0_B PFB2 counter has not been updated at least once since the last SPI read-out 1_B PFB2 counter has been updated at least once since the last SPI read-out
PFB2	15	r	**Phase feedback comparator level of SH2 phase** 0_B SH2 low level detected 1_B SH2 high level detected

2.43 Phase 3 high time counter

PHASE3_CNT Offset address: $2F_H$

Phase 3 high time counter DefaultReset value: 8000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PFB3	**PFB3_CNT_UPD**	**CNT3_RDY**	**PFB3_H_CNT**												
r	rw1ch	r	r												

Field	Bits	Type	Description
PFB3_H_CNT	12:0	r	**Phase 3 (SH3) high time counter, LSB of nominal 1/fPFB_CNT** 0000_H min. value: read-only data $0FFF_H$ max. value: read-only data
CNT3_RDY	13	r	**PFB3_H counter ready for read indication** 0_B PFB3 counter disabled or counter not ready for read 1_B PFB3 counter ready for read
PFB3_CNT_UPD	14	rw1ch	**PFB3 counter update indication** 0_B PFB3 counter has not been updated at least once since the last SPI read-out 1_B PFB3 counter has been updated at least once since the last SPI read-out
PFB3	15	r	**Phase feedback comparator level of SH3 phase** 0_B SH3 low level detected 1_B SH3 high level detected

2.44 Effective MOSFET turn-on/off delay time HS1

TDON_TDOFF_HS1 Offset address: 30_H

Effective MOSFET turn-on/off delay time HS1 DefaultReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS1_ ACT	**LS1_ ACT**	**TDON_HS1**							**TDOFF_HS1**						
r	r	r							r						

Field	Bits	Type	Description
TDOFF_HS1	6:0	r	**Effective turn-off delay time of HS1 MOSFET** 00_H min. value: read-only data $7F_H$ max. value: read-only data
TDON_HS1	13:7	r	**Effective turn-on delay time of HS1 MOSFET** 00_H min. value: read-only data $7F_H$ max. value: read-only data
LS1_ACT	14	r	**LS1 detection as active MOSFET when turned ON** 0_B LS1 is not the active MOSFET 1_B LS1 is the active MOSFET
HS1_ACT	15	r	**HS1 detection as active MOSFET when turned ON** 0_B HS1 is not the active MOSFET 1_B HS1 is the active MOSFET

2.45 Effective MOSFET turn-on/off delay time LS1

TDON_TDOFF_LS1 Offset address: 31_H

Effective MOSFET turn-on/off delay time LS1 DefaultReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS1_ ACT	**LS1_ ACT**	**TDON_LS1**							**TDOFF_LS1**						
r	r	r							r						

Field	Bits	Type	Description
TDOFF_LS1	6:0	r	**Effective turn-off delay time of LS1 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
TDON_LS1	13:7	r	**Effective turn-on delay time of LS1 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
LS1_ACT	14	r	**LS1 detection as active MOSFET when turned ON** 0_B LS1 is not the active MOSFET 1_B LS1 is the active MOSFET
HS1_ACT	15	r	**HS1 detection as active MOSFET when turned ON** 0_B HS1 is not the active MOSFET 1_B HS1 is the active MOSFET

2.46 Effective MOSFET turn-on/off delay time HS2

TDON_TDOFF_HS2 Offset address: 32_H

Effective MOSFET turn-on/off delay time HS2 DefaultReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS2_ ACT	**LS2_ ACT**	**TDON_HS2**							**TDOFF_HS2**						
r	r	r							r						

Field	Bits	Type	Description
TDOFF_HS2	6:0	r	**Effective turn-off delay time of HS2 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
TDON_HS2	13:7	r	**Effective turn-on delay time of HS2 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
LS2_ACT	14	r	**LS2 detection as active MOSFET when turned ON** 0_B LS2 is not the active MOSFET 1_B LS2 is the active MOSFET
HS2_ACT	15	r	**HS2 detection as active MOSFET when turned ON** 0_B HS2 is not the active MOSFET 1_B HS2 is the active MOSFET

2.47 Effective MOSFET turn-on/off delay time LS2

TDON_TDOFF_LS2 Offset address: 33_H

Effective MOSFET turn-on/off delay time LS2 DefaultReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS2_ ACT	**LS2_ ACT**	**TDON_LS2**							**TDOFF_LS2**						
r	r	r							r						

Field	Bits	Type	Description
TDOFF_LS2	6:0	r	**Effective turn-off delay time of LS2 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
TDON_LS2	13:7	r	**Effective turn-on delay time of LS2 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
LS2_ACT	14	r	**LS2 detection as active MOSFET when turned ON** 0_B LS2 is not the active MOSFET 1_B LS2 is the active MOSFET
HS2_ACT	15	r	**HS2 detection as active MOSFET when turned ON** 0_B HS2 is not the active MOSFET 1_B HS2 is the active MOSFET

2.48 Effective MOSFET turn-on/off delay time HS3

TDON_TDOFF_HS3 Offset address: 34_H

Effective MOSFET turn-on/off delay time HS3 DefaultReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS3_ACT	**LS3_ACT**	**TDON_HS3**							**TDOFF_HS3**						
r	r	r							r						

Field	Bits	Type	Description
TDOFF_HS3	6:0	r	**Effective turn-off delay time of HS3 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
TDON_HS3	13:7	r	**Effective turn-on delay time of HS3 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
LS3_ACT	14	r	**LS3 detection as active MOSFET when turned ON** 0_B LS3 is not the active MOSFET 1_B LS3 is the active MOSFET
HS3_ACT	15	r	**HS3 detection as active MOSFET when turned ON** 0_B HS3 is not the active MOSFET 1_B HS3 is the active MOSFET

2.49 Effective MOSFET turn-on/off delay time LS3

TDON_TDOFF_LS3 Offset address: 35_H

Effective MOSFET turn-on/off delay time LS3 DefaultReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS3_ ACT	**LS3_ ACT**	**TDON_LS3**							**TDOFF_LS3**						
r	r	r							r						

Field	Bits	Type	Description
TDOFF_LS3	6:0	r	**Effective turn-off delay time of LS3 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
TDON_LS3	13:7	r	**Effective turn-on delay time of LS3 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
LS3_ACT	14	r	**LS3 detection as active MOSFET when turned ON** 0_B LS3 is not the active MOSFET 1_B LS3 is the active MOSFET
HS3_ACT	15	r	**HS3 detection as active MOSFET when turned ON** 0_B HS3 is not the active MOSFET 1_B HS3 is the active MOSFET

2.50 Effective MOSFET slew rate time HS1

TSLEW_ON_OFF_HS1 Offset address: 36_H

Effective MOSFET slew rate time HS1 DefaultReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS1_ACT	**LS1_ACT**	**TSLEW_ON_HS1**							**TSLEW_OFF_HS1**						
r	r	r							r						

Field	Bits	Type	Description
TSLEW_OFF_HS1	6:0	r	**Effective turn-off slew rate time of HS1 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
TSLEW_ON_HS1	13:7	r	**Effective turn-on slew rate time of HS1 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
LS1_ACT	14	r	**LS1 detection as active MOSFET when turned ON** 0_B LS1 is not the active MOSFET 1_B LS1 is the active MOSFET
HS1_ACT	15	r	**HS1 detection as active MOSFET when turned ON** 0_B HS1 is not the active MOSFET 1_B HS1 is the active MOSFET

2.51 Effective MOSFET slew rate time LS1

TSLEW_ON_OFF_LS1 Offset address: 37_H

Effective MOSFET slew rate time LS1 DefaultReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS1_ACT	**LS1_ACT**	**TSLEW_ON_LS1**							**TSLEW_OFF_LS1**						
r	r	r							r						

Field	Bits	Type	Description
TSLEW_OFF_LS1	6:0	r	**Effective turn-off slew rate time of LS1 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
TSLEW_ON_LS1	13:7	r	**Effective turn-on slew rate time of LS1 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
LS1_ACT	14	r	**LS1 detection as active MOSFET when turned ON** 0_B LS1 is not the active MOSFET 1_B LS1 is the active MOSFET
HS1_ACT	15	r	**HS1 detection as active MOSFET when turned ON** 0_B HS1 is not the active MOSFET 1_B HS1 is the active MOSFET

2.52 Effective MOSFET slew rate time HS2

TSLEW_ON_OFF_HS2 Offset address: 38_H

Effective MOSFET slew rate time HS2 DefaultReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS2_ACT	**LS2_ACT**	**TSLEW_ON_HS2**							**TSLEW_OFF_HS2**						
r	r	r							r						

Field	Bits	Type	Description
TSLEW_OFF_HS2	6:0	r	**Effective turn-off slew rate time of HS2 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
TSLEW_ON_HS2	13:7	r	**Effective turn-on slew rate time of HS2 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
LS2_ACT	14	r	**LS2 detection as active MOSFET when turned ON** 0_B LS2 is not the active MOSFET 1_B LS2 is the active MOSFET
HS2_ACT	15	r	**HS2 detection as active MOSFET when turned ON** 0_B HS2 is not the active MOSFET 1_B HS2 is the active MOSFET

2.53 Effective MOSFET slew rate time LS2

TSLEW_ON_OFF_LS2 Offset address: 39_H

Effective MOSFET slew rate time LS2 DefaultReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS2_ACT	**LS2_ACT**	**TSLEW_ON_LS2**							**TSLEW_OFF_LS2**						
r	r	r							r						

Field	Bits	Type	Description
TSLEW_OFF_LS2	6:0	r	**Effective turn-off slew rate time of LS2 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
TSLEW_ON_LS2	13:7	r	**Effective turn-on slew rate time of LS2 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
LS2_ACT	14	r	**LS2 detection as active MOSFET when turned ON** 0_B LS2 is not the active MOSFET 1_B LS2 is the active MOSFET
HS2_ACT	15	r	**HS2 detection as active MOSFET when turned ON** 0_B HS2 is not the active MOSFET 1_B HS2 is the active MOSFET

2.54 Effective MOSFET slew rate time HS3

TSLEW_ON_OFF_HS3 Offset address: $3A_H$

Effective MOSFET slew rate time HS3 DefaultReset value: 0000_H

15	14	13 12 11 10 9 8 7	6 5 4 3 2 1 0
HS3_ACT	**LS3_ACT**	**TSLEW_ON_HS3**	**TSLEW_OFF_HS3**
r	r	r	r

Field	Bits	Type	Description
TSLEW_OFF_HS3	6:0	r	**Effective turn-off slew rate time of HS3 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
TSLEW_ON_HS3	13:7	r	**Effective turn-on slew rate time of HS3 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
LS3_ACT	14	r	**LS3 detection as active MOSFET when turned ON** 0_B LS3 is not the active MOSFET 1_B LS3 is the active MOSFET
HS3_ACT	15	r	**HS3 detection as active MOSFET when turned ON** 0_B HS3 is not the active MOSFET 1_B HS3 is the active MOSFET

2.55 Effective MOSFET slew rate time LS3

TSLEW_ON_OFF_LS3 Offset address: $3B_H$

Effective MOSFET slew rate time LS3 DefaultReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS3_ACT	**LS3_ACT**	**TSLEW_ON_LS3**							**TSLEW_OFF_LS3**						
r	r	r							r						

Field	Bits	Type	Description
TSLEW_OFF_LS3	6:0	r	**Effective turn-off slew rate time of LS3 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
TSLEW_ON_LS3	13:7	r	**Effective turn-on slew rate time of LS3 MOSFET** 00_H min. Value: read-only data $7F_H$ max. value: read-only data
LS3_ACT	14	r	**LS3 detection as active MOSFET when turned ON** 0_B LS3 is not the active MOSFET 1_B LS3 is the active MOSFET
HS3_ACT	15	r	**HS3 detection as active MOSFET when turned ON** 0_B HS3 is not the active MOSFET 1_B HS3 is the active MOSFET

3 Application information (additional information)

This chapter includes additional information on external circuitry needed for the device. An example application diagram with all required and optional external components is shown below.

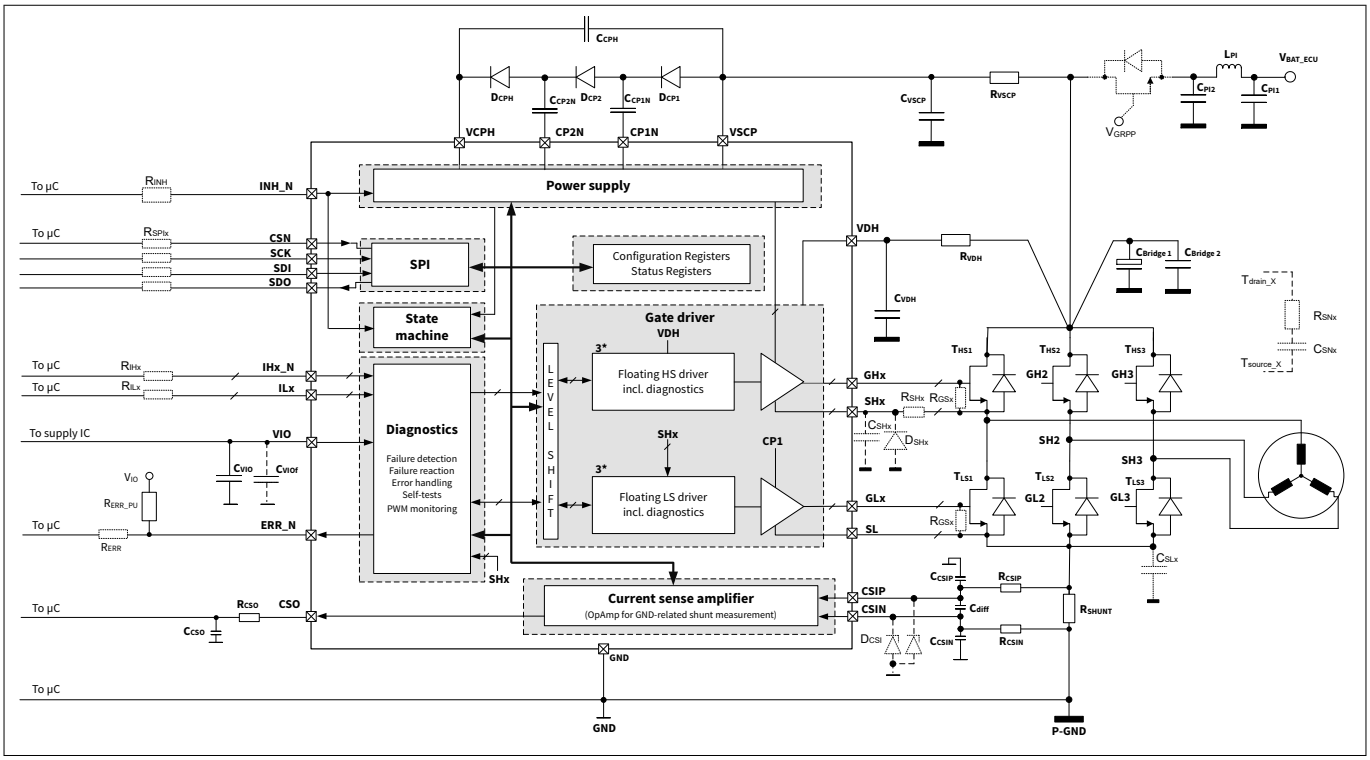

Figure 65 Simplified application example with all components

3.1 External components

Required and optional external components with nominal values for *TLE9186QVW* are listed below. The external components' values depend on the application conditions and must be chosen accordingly

Table 28 External components

Name	Description	Recommended nominal Value	Unit	Comment
C_{VSCP}	VSCP filter capacitor	2.2	µF	Required
R_{VSCP}	VSCP series resistor	2	Ω	Required
C_{CP1N}, C_{CP2N}	Charge pump 1 and charge pump 2 floating capacitor	220	nF	Required in the two-stage charge pump configuration
C_{CP1N}, C_{CP2N}, C_{CP3N}	Charge pump 1, charge pump 2 and charge pump 3 floating capacitor	220	nF	Required in the three-stage charge pump configuration

(table continues...)

Table 28 (continued) External components

Name	Description	Recommended nominal Value	Unit	Comment
C_{CPH}	Charge pump 2 buffer capacitor	470	nF	Required
D_{CP1}, D_{CP2}, D_{CPH}	Charge pump diodes	BAS16T, BAV99S		Required in the two-stage charge pump configuration
D_{CP1}, D_{CP2}, D_{CP3}, D_{CPH}	Charge pump diodes	BAT54S, BAT54TW, BAT54SDW		Required in the three-stage charge pump configuration
C_{VIO}	VIO capacitor	2.2	µF	Required
C_{VIOf}	VIO filter capacitor	1	nF	Optional
C_{VDH}	VDH filter capacitor	3.3	nF	Required
R_{VDH}	VDH series resistor	50	Ω	Required
C_{CSIP}, C_{CSIN}	OpAmp input filter capacitor	22	nF	Required
R_{CSIP}, R_{CSIN}	OpAmp input resistor	2	Ω	Required
C_{DIFF}	OpAmp differential capacitor	22	nF	Required
R_{CSO}	OpAmp output resistor	50	Ω	Only required in combination with CCSO1
C_{CSO1}	OpAmp output capacitor	2.2	nF	Only required in combination with RCSO
C_{CSO2}	OpAmp output capacitor	220	pF	No output resistor RCSO needed
R_{Shunt}	Shunt resistor	0.5 - 2	mΩ	value application-dependent
R_{SPIx}, R_{INH}, R_{IHx}, R_{ILx}, R_{ERR}	Series resistor microcontroller	1	kΩ	Optional
R_{ERR_PU}	ERR_N pull-up resistor	30	kΩ	Required
R_{GSx}	Gate-source resistor	100	kΩ	Optional
R_{SHx}	Phase source resistor	0 … 10	Ω	Optional

(table continues...)

Table 28 (continued) External components

Name	Description	Recommended nominal Value	Unit	Comment
C_{SHx}	Phase source capacitor	470	pF	Optional
D_{SHx}	Phase source diode			Optional
C_{SLx}	Source low-side FET capacitor	1	nF	Optional
D_{CSI}	OpAmp input clamping diodes			Optional
R_{SNx}	Snubber resistor	1 ... 10	Ω	Optional
C_{SNx}	Snubber capacitor	0.1 … 22	nF	Optional
$C_{Bridge1}$	VBridge ELCO capacitor per half-bridge	1	mF	Optional
$C_{Bridge2}$	VBridge ceramic capacitor per half-bridge	1	µF	Optional

The snubber circuit is optional only. If snubber circuit is mounted the value of the snubber resistor may vary from 1 to 10 Ω (nominal values) and the snubber capacitor may vary from 0.1 to 22 nF (nominal values).

3.1.1 Optional components explanation

The external components listed below are not required for the correct operation of the device. They are optional for the device but might be required by the application. It is the system integrator's responsibility to assess whether the external component is required by the application and to select appropriate optional component values.

Table 29 Optional external components

Name	Description	Further explanation
C_{VIOf}	VIO capacitor filter capacitor	For improved electromagnetic emission results it is recommended to place C_{VIOf} capacitor very close to the VIO pin (pin 9) and direct connection to GND pin (pin 4). Furthermore it is recommended to connect GND (pin 4) directly to E-Pad. E-pad connected to PCB GND layer.
R_{SPIx}, R_{IHx}, R_{ILx}, R_{ERR}	Series resistor microcontroller	Recommended if the device is to be operated outside specified absolute maximum ratings of the device, such as GND shift between device and over external IC. Series resistors can be used to protect external ICs from high voltage due to internal failure propagation in the device
R_{GSx}	Gate-source resistor	Recommended in case of open gate pin failure on PCB and PCB open pin failure cannot be excluded

(table continues...)

Table 29 (continued) Optional external components

Name	Description	Further explanation
R_{SHx}	Phase source resistor	Recommended in case device operation is outside specified absolute maximum ratings of device
C_{SHx}	Phase source capacitor	May improve electromagnetic immunity
D_{SHx}	Phase source diode	Recommended if the device is to be operated outside specified absolute maximum ratings of device
C_{SLx}	Source low-side FET capacitor	Recommended for improved electromagnetic immunity
D_{CSI}	Current sense amplifier protection diode	Optional component to protect the current sense amplifier inputs pins against damage due to absolute maximum ratings violation
R_{SNx}	Snubber resistor	The snubber circuit is optional only. If snubber circuit is mounted the value of the snubber resistor may vary from 1 to 10 Ω (nominal values) and the snubber capacitor may vary from 0.1 to 22 nF (nominal values)
C_{SNx}	Snubber capacitor	
$C_{Bridge1}$	V_{Bridge} ELCO capacitor per half-bridge	–
$C_{Bridge2}$	V_{Bridge} ceramic capacitor per half-bridge	–
D_{ISPx}	Current sense amplifier protection diode	This optional components is needed to protect the current sense amplifier inputs pins against damage due to AMR violation caused by solder joint issues at the external shunt resistor R_{SHUNT}

Since the ERR_N pin of the device is an open-drain output, an external pull-up resistor R_{ERR_PU} to microcontroller supply VIO is needed to pull ERR_N signal "high". The optional series resistor R_{ERR} protects the microcontroller from damage in case the pull-up resistor R_{ERR_PU} is shorted. Dimensioning depends on supply and the maximum current capability of the microcontroller.

Series resistors at the serial peripheral interface (SPI) and IHx/ILx PWM input pins can limit the maximum switching frequency. Additionally the voltage divider created by external series resistor and internal device pull-down or pull-up resistors have to be considered to ensure correct logic "low" and "high" levels.

3.1.2 Electrical characteristics table - external component deviation

The specification of the external component values are specified including the deviation of the nominal values. Deviations included in minimum and maximum values listed in external components deviation specification. Product-, temperature- and aging deviation included. Include voltage derating. Unless otherwise specified, the deviation for external components are:

- Resistor: ±10%
- Capacitor: -50% ... +30%

Table 30 Electrical characteristics table - external component deviation

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Supply						
VIO capacitor	C_{VIO}	1	2.2	6.1	µF	–
VSCP filter capacitor	C_{VSCP}	1	2.2	4.5	µF	–
VSCP series resistor	R_{VSCP}	1.0	2.0	4.0	Ω	–
Charge pump 1 and 2 floating capacitor	C_{CP1N}, C_{CP2N}, C_{CP3N}	150	220	290	nF	–
Charge pump 2 buffer capacitor	C_{CPH}	330	470	600	nF	–
Charge pump diode	D_{CP1}, D_{CP2}, D_{CP3} D_{CPH}					Standard diode used for charge pump is BAV99, BAS16 or BAT54. For three-stage charge pump configuration use BAT54 or diode with equivalent electrical characteristics. The voltage drop over the charge pump diodes has direct impact on the efficiency of the charge pump and resulting VCPH overdrive voltage
Motor bridge						
VDH filter capacitor	C_{VDH}	1	3.3	4.7	nF	–
VDH resistor	R_{VDH}	25	50	200	Ω	–
Current sense amplifier						
OpAmp positive input filter capacitor	C_{CSIP}	10	22	33	nF	–
OpAmp negative input filter capacitor	C_{CSIN}	10	22	33	nF	–
OpAmp differential input filter capacitor	C_{Diff}	9	22	43	nF	–

(table continues...)

Table 30 (continued) Electrical characteristics table - external component deviation

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
OpAmp input resistor	R_{CSIN}, R_{CSIP}	0.99	2	3.3	Ω	Cut off frequency dependent. Cut off frequency should be in the range of 5... 10 MHz. R_{CSIN} = 2 Ω + C_{Diff} = 22 nF, C_{CSIN} = 22 nF
OpAmp output resistor	R_{CSO}	25	47	75	Ω	–
OpAmp output capacitor 1	C_{CSO1}	1	2.2	2.4	nF	Series resistor R_{CSO} required
OpAmp output capacitor 2	C_{CSO2}	10	150	400	pF	No external series resistor R_{CSO} required
Microcontroller interface						
ERR_N pull-up resistor	R_{ERR_PU}	15	30	100	kΩ	–

Revision history

Document version	Date of release	Description of changes
1.10	2026-01-08	• Editorial changes • Corrected description for unacceptable error detection in Guidance for unacceptable error detection • Updated drawing "Detection of active and freewheeling MOSFET" in Active MOSFET and freewheeling MOSFET • Corrected footnote in Turn ON of a Gxx output stage • Corrected description for post-charge phase in Turn ON of a Gxx output stage • Corrected description in TDON, TDOFF and TSLEW_ON, TSLEW_OFF time measurements • Corrected table description and removed auto-restart and braking failure reaction in SPI status bits relation to global status byte • Updated window watchdog clock counter examples in Window watchdog internal clock frequency relationship and Window watchdog clock counter
1.00	2025-12-05	User manual available

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