# KIT_PSC3M6_CC1 Kit user guide

## About this document

### Scope and purpose

This document describes the features and hardware details of the PSOC™ Control C3M6 Digital Power Control Card and Interface Board. It provides an evaluation platform for digital control applications based on the PSOC™ Arm® Cortex®-M33 MCU. The board is part of Infineon's Digital Power Evaluation Platform kits.

### Intended audience

This document is intended for users of the KIT_PSC3M6_CC1 kit. This board is designed for use under laboratory conditions.

### Evaluation board

This board is to be used during the design-in process for evaluating and measuring characteristic curves, and for checking datasheet specifications.

***Note**: PCB and auxiliary circuits are NOT optimized for final customer design.*

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# Safety precautions

***Note**: Please note the following warnings regarding the hazards associated with development systems.*

**Table 1 Safety precautions**

| | |
|---|---|
|  | **Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.* |

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# 1 Introduction

The PSOC™ Control C3M6 Digital Power Control Card Kit enables evaluation and development of applications using the PSOC™ control C3 Main line Series MCU (hereafter referred to as the PSOC™ C3M6 MCU).

The PSOC™ Control C3M6 Digital Power Control Card Kit consists of two boards:

1. PSOC™ Control C3M6 Digital Power Control Card
2. PSOC™ Control C3M6 Interface Board

The control card features a dual footprint that supports both the E-LQFP-100 (primary) and E-LQFP-64 (alternate) packages. It includes a standard 120-pin edge connector for baseboard compatibility. The card also includes an onboard programmer/debugger, status and user LEDs, a reset button, a CAN transceiver, and a dedicated USB connection for the MCU. The board operates from a standalone 3.3 V supply.

The interface board features a 120-pin mating connector for the control card. All I/Os of the PSOC™ C3M6 MCU are routed to standard 2.54 mm-pitch headers for easy access.

The PSC3P6xx and PSC3M6xx devices are based on the Arm® Cortex®-M33 processor and operate at frequencies of up to 180 MHz with DSP and FPU capabilities. In addition to the CPU subsystem, the devices include advanced real-time control peripherals, such as a high-performance programmable analog subsystem with ADCs, DACs, op amps, and comparators, as well as advanced timers with high-resolution capabilities. The devices support one Active mode and five low-power modes to help manage and reduce power consumption based on application requirements.

Use ModusToolbox™ to develop and debug PSOC™ C3M6 MCU projects. ModusToolbox™ software is a comprehensive set of development tools that integrates Infineon devices into existing development workflows.

## 1.1 Kit contents

The KIT_PSC3M6_CC1 kit includes the following kit components:

- PSOC™ Control C3M6 Control Card
- PSOC™ Control C3M6 Interface Board
- USB Type-C to USB Type-A 2.0 cable
- Quick Start Guide (printed on the kit package)

## 1.2 Getting started

The following sections help familiarize users with this evaluation kit:

- The Kit operation section describes the major features of the PSOC™ Control C3M6 Digital Power Control Card and functions such as programming, debugging, UART, ADC, CAN, and $I^2C$
- The Hardware section provides a detailed hardware description, kit schematics, and the bill of materials (BOM) for reference
- ModusToolbox™ software supports application development using the PSOC™ Control C3M6 Digital Power Control Card
- ModusToolbox™ software is a free development ecosystem that includes the Eclipse IDE for ModusToolbox™ software and the PSOC™ Control C3M6 SDK for the PSOC™ Control C3M6 MCU
- ModusToolbox™ software enables configuration of device resources and middleware libraries, development of C and assembly source code, and programming and debugging of the device. Download the software from the ModusToolbox™ home page
- A wide range of code examples is available for evaluating the PSOC™ Control C3M6 Digital Power Control Card. These examples help users become familiar with the PSOC™ Control C3M6 MCU and develop custom designs. Access these examples through the ModusToolbox™ Project Creator tool. Alternatively, visit the Code examples for ModusToolbox™ software page to access the examples

## 1.3 Additional learning resources

Infineon provides a wealth of information for the PSOC™ Control C3 Arm® Cortex®-M33 MCU to help users select the appropriate PSOC™ device and efficiently integrate it into their designs.

## 1.4 Technical support

For assistance, visit Infineon Support. Questions can also be posted in the Infineon Developer Community.

For quick assistance, use the self-help resources available in the Technical Documents section.

# 2 Kit operation

This chapter introduces the features of the PSOC™ Control C3M6 Digital Power Control Card, including its theory of operation, the onboard XMC4200 programming and debugging functionality, and the communication interfaces supported by the PSOC™ Control C3M6 MCU.

## 2.1 Theory of operation

The PSOC™ Control C3M6 Digital Power Control Card is built around the PSOC™ Control C3M6 MCU. Figure 1 shows the block diagram of the PSOC™ Control C3M6 MCU used on the board. For detailed information about device features, see the device datasheet.

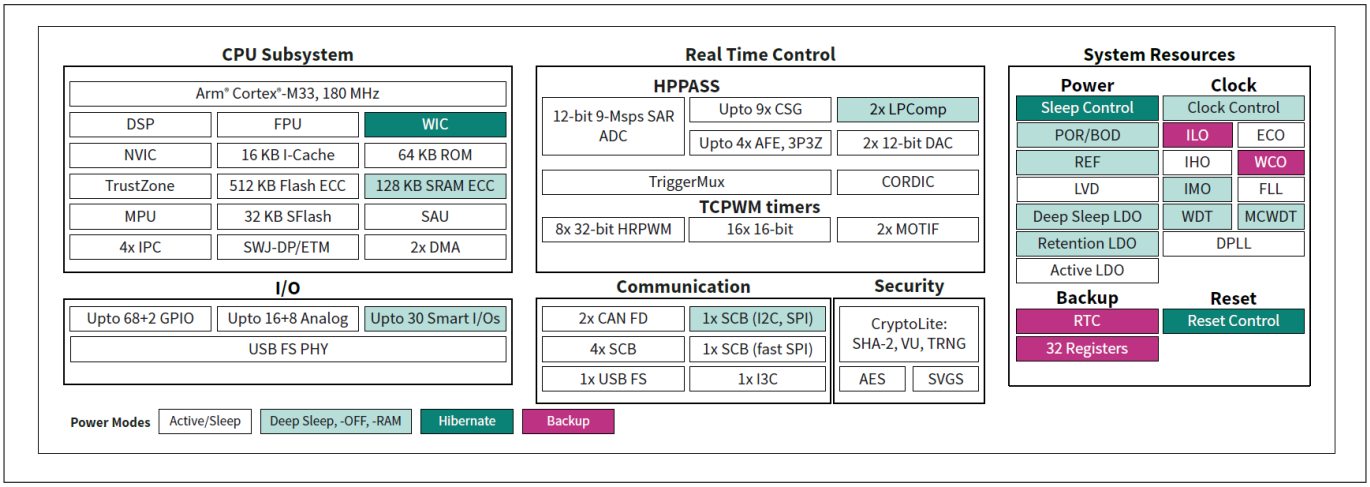



**Figure 1 PSOC™ C3M6 MCU block diagram**

Figure 2 shows the block diagram of the PSOC™ Control C3M6 Digital Power Control Card.

## 2 Kit operation

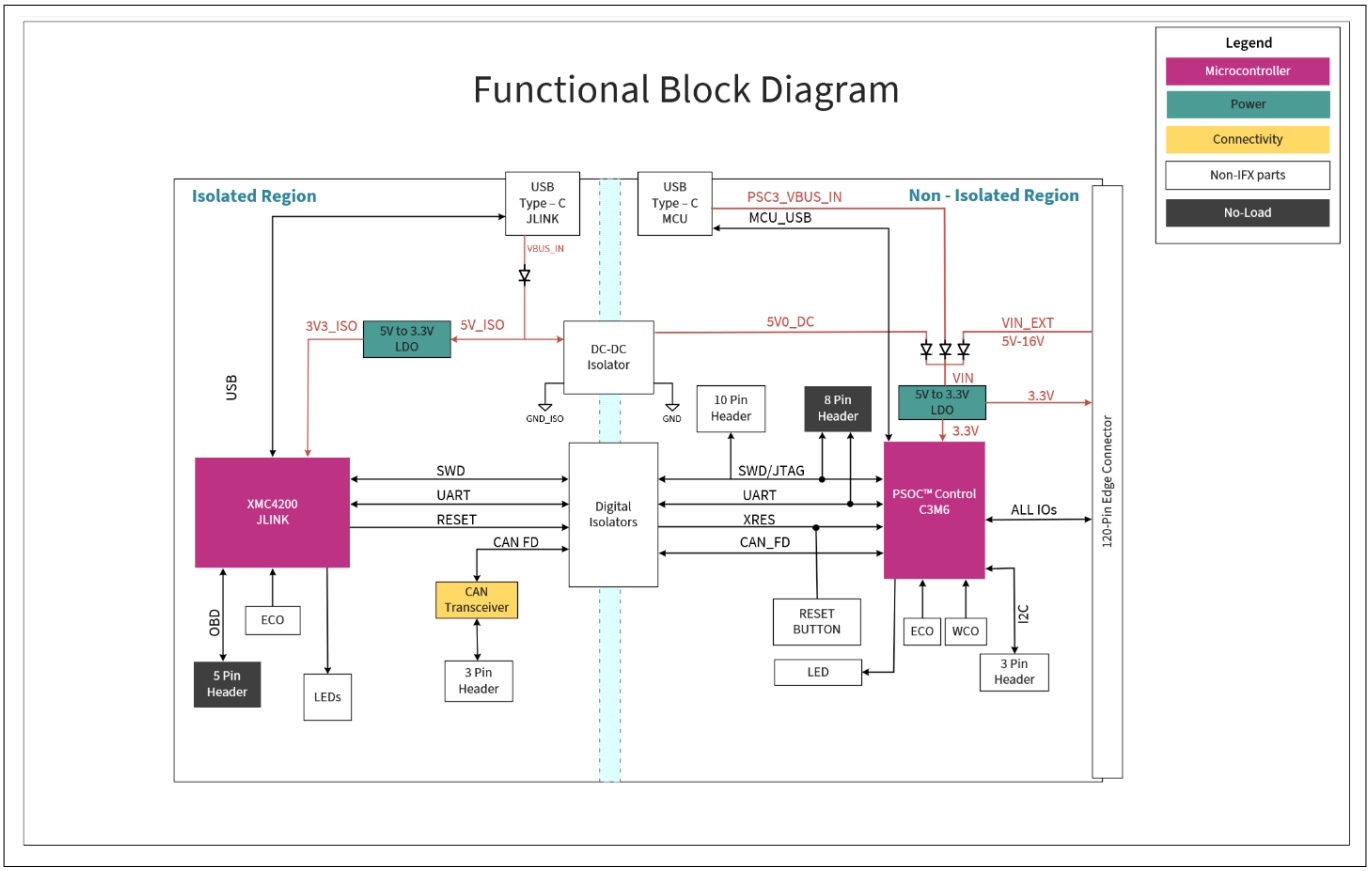



**Figure 2 PSC3M6 kit functional block diagram**

## 2 Kit operation

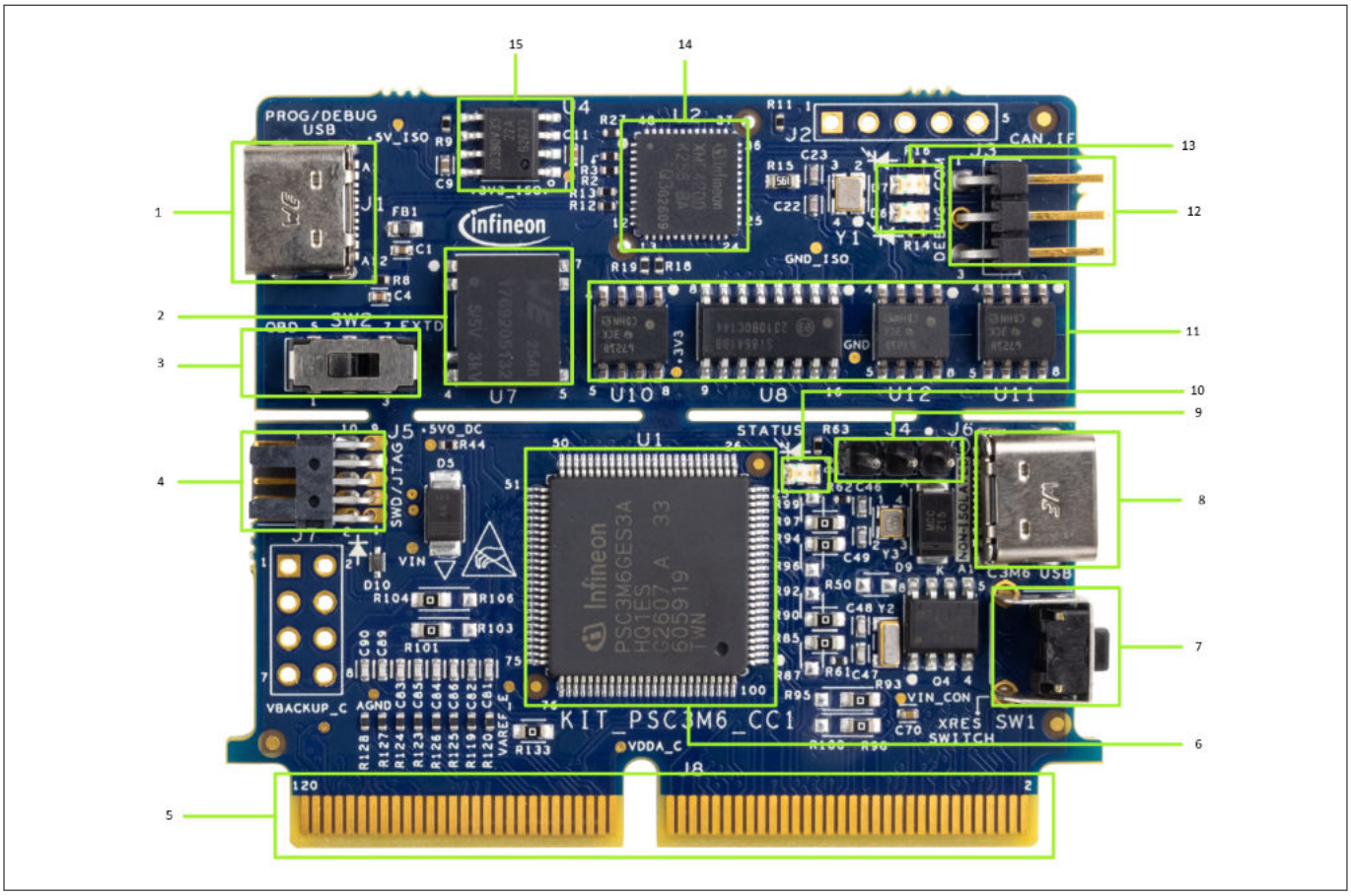



**Figure 3** **PSOC™ Control C3M6 Digital Power Control Card - Top view**

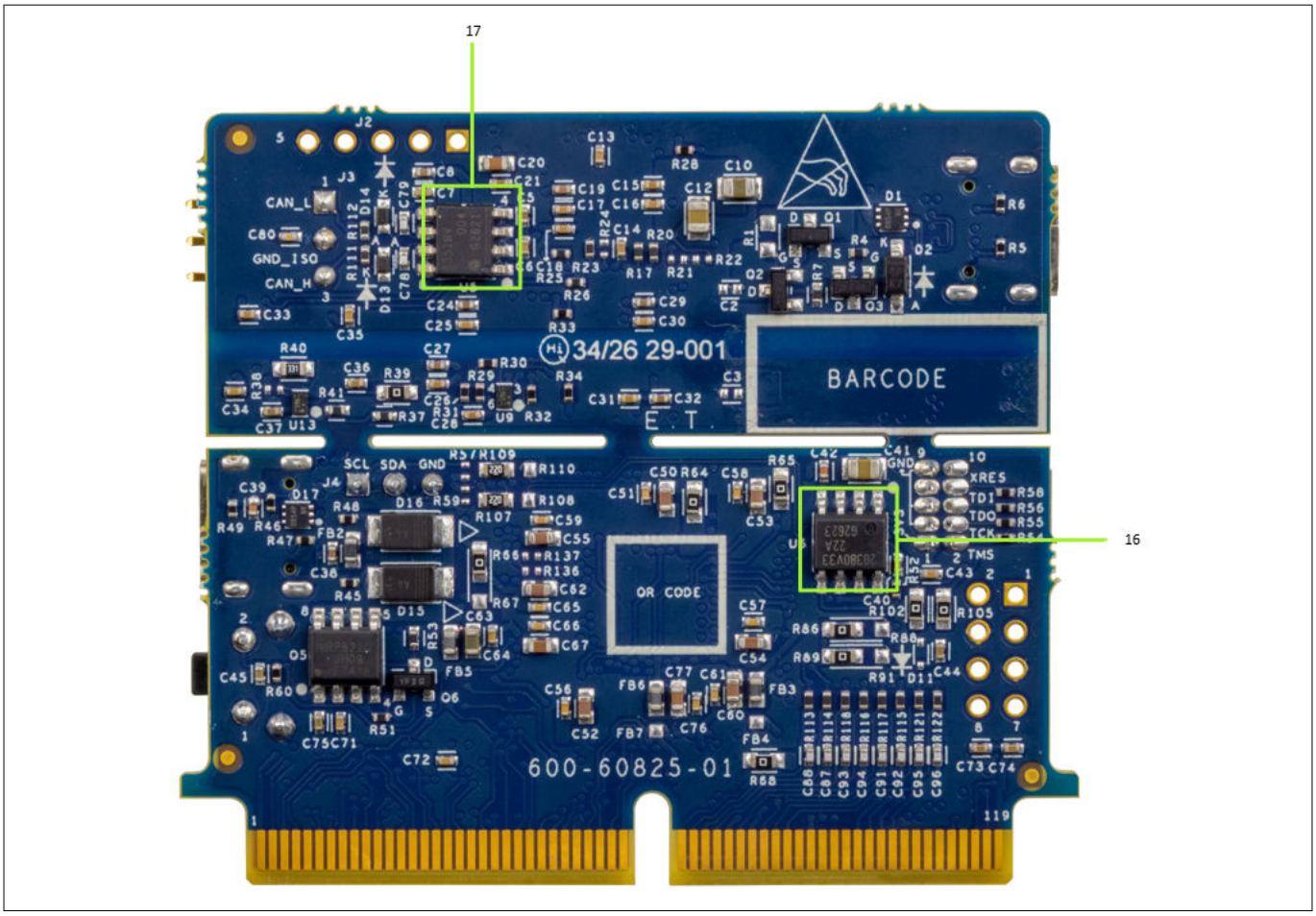



**Figure 4 PSOC™ Control C3M6 Digital Power Control Card - Bottom view**

The PSOC™ Control C3M6 Digital Power Control Card includes the following peripherals:

1. **Programmer/Debugger USB connector (J1)**: Connect a USB cable between this connector and a PC to use the onboard XMC4200 programmer/debugger and provide power to the board
2. **DC-DC power isolator (1769205132, U7)**: This power isolator converts a 5 V input into an isolated 5 V output and provides 3 kV functional isolation for industrial, measurement, and microcontroller applications
3. **Programmer switch (SW2)**: This switch allows users to select the onboard debugger (OBD) or an external debugger (EXTD) for programming the PSOC™ C3M6 MCU
4. **10-pin programming header (J5)**: This header allows programming and debugging of the PSOC™ C3M6 MCU using an external programmer, such as MiniProg4
5. **120-pin edge-finger connector (J8)**: This connector provides access to all I/Os of the PSOC™ C3M6 MCU for external connections. A mating connector is available on the interface board
6. **PSOC™ Control C3M6 MCU (U1)**: This kit is designed to demonstrate the features of the PSOC™ C3M6 MCU. The board provides a dual footprint for the MCU. A 100-pin LQFP package (U1) is populated by default and can be replaced with a 64-pin LQFP package (U3)
7. **Reset switch (SW1)**: This switch resets the PSOC™ C3M6 MCU by connecting the *XRES* pin to ground
8. **Target USB device connector (J6)**: Connect a USB cable between this connector and a PC to use USB device applications on the PSOC™ C3M6 MCU
9. **I²C header (J4)**: I²C signals are routed to the header pins for external connections
10. **USER LED (D8)**: This onboard LED is controlled by the PSOC™ C3M6 MCU. The LED is active low; drive the corresponding pin low to turn on the LED

11. **Digital isolators (U8, U10, U11, U12)**: All signals between the XMC4200 programmer/debugger and the PSOC™ C3M6 MCU, including SWD, UART, CAN, and RESET, are isolated using digital isolators. These devices provide capacitive isolation of up to 2.5 kV RMS.
12. **CAN header (J3)**: CAN signals are routed to this header
13. **XMC4200 status LEDs (D6, D7)**: The red (DEBUG) and green (COM) LEDs indicate the programming and connection status of the XMC4200
14. **XMC4200 Programmer/Debugger (U2)**: The XMC4200 device serves as the onboard programmer/debugger and supports the Arm® JTAG interface, SWD programming, and a multi-CAN interface. For more information, refer to the XMC4200 datasheet
15. **Programmer/Debugger power supply (`TLS203B0EJV33XUMA1`, U4)**: This isolated LDO supplies 3.3 V to the onboard programmer/debugger
16. **PSOC™ C3M6 MCU power supply (`TLS203B0EJV33XUMA1`, U6)**: This non-isolated LDO supplies 3.3 V to the PSOC™ C3M6 MCU
17. **CAN transceiver (`TLE9351BVSJXTMA1`, U5)**: This high-speed CAN FD transceiver supports data rates of up to 5 Mbps and provides low EMC emissions and low-power standby operation

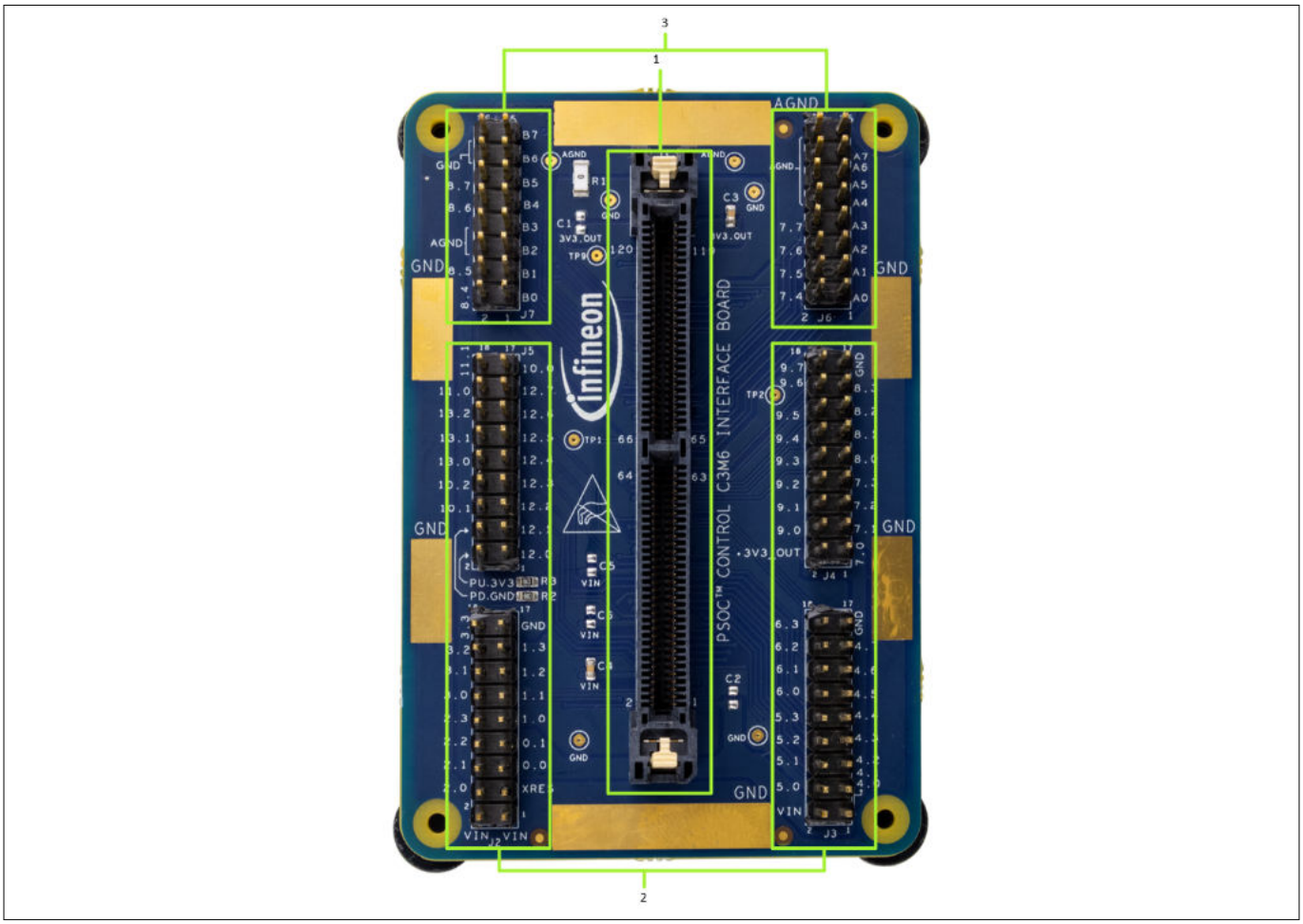



**Figure 5 PSOC™ Control C3M6 Interface board**

The PSOC™ Control C3M6 Interface board includes the following peripherals:

1. **120-pin edge-finger connector (J1)**: This connector serves as the mating connector for the edge finger on the control card. Through this connector, all I/Os of the PSC3M6 MCU are expanded and made available on the interface board

2. **Digital I/O expansion headers (J2, J3, J4, and J5)**: These connectors serve as I/O expansion headers for the digital I/O signals of the PSC3M6 MCU
3. **Analog I/O expansion headers (J6 and J7)**: These connectors serve as I/O expansion headers for the analog I/O signals of the PSC3M6 MCU, except for P8.6 and P8.7 on J7

## 2.2 Using the OOB example – PSOC™ Control C3 MCU: Hello world

By default, the PSOC™ Control C3M6 Digital Power Control Card is preprogrammed with the PSOC™ Control C3 MCU: Hello World code example.

For a detailed description of the code example, refer to the `README.md` file. To view the file, visit the `README.md` page in the GitHub repository. Alternatively, create a ModusToolbox™ project using the code example and review the `README.md` file in the application directory.

***Note**: If the default code example is overwritten, it can be restored by programming the PSOC™ Control C3 MCU: Hello World code example available for the PSOC™ Control C3M6 Digital Power Control Card BSP.*

The following steps explain how to use the code example:

1. Connect the board's programmer/debugger USB connector, **J1** (PROG/DEBUG USB), to the PC using the provided USB cable
2. Open a terminal application and select the enumerated COM port. Configure the serial port for 115200 baud, 8 data bits, no parity, and 1 stop bit (8N1)
3. Press **SW1** (XRES switch) on the board. Verify that the terminal application displays the code example title and related text, as shown in Figure 6

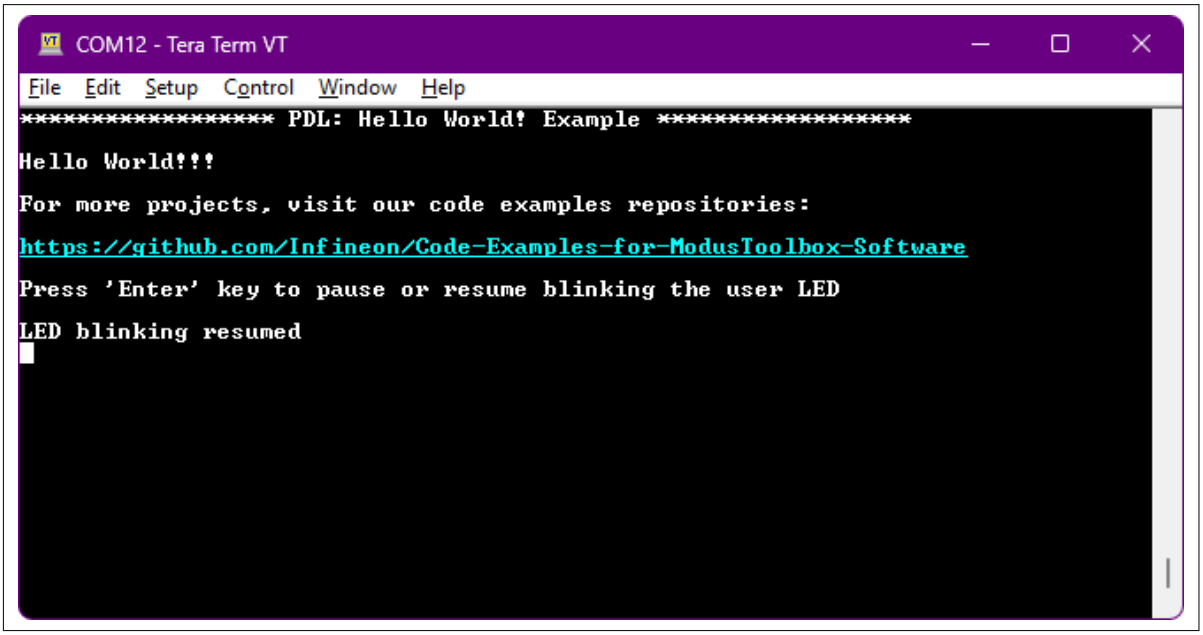



**Figure 6 Hello world message in the terminal**

4. Verify that the user LED (STATUS) blinks at 1 Hz
5. Click the terminal application window and press **Enter**. Verify that the LED (STATUS) stops blinking. The terminal displays the message: **"LED blinking paused"**
6. Press **Enter** again. Verify that the LED (STATUS) resumes blinking at 1 Hz. The terminal displays the message: **"LED blinking resumed"**

## 2.3 Creating and running a ModusToolbox™ project for KIT_PSC3M6_CC1

1. Connect the board to the PC using the provided USB cable through the onboard J-Link USB connector J1 (PROG/DEBUG USB). The board enumerates as a USB composite device

   ***Note**: To use the J-Link debugger, install the J-Link software on the PC*

   a. Download and install the latest J-Link software and documentation pack from the J-Link/J-Trace Downloads page. PSC3M/P6 devices require J-Link version 9.68 or later
   b. Add the J-Link installation folder to the environment variables using the variable name `MTB_JLINK_DIR`

2. Follow these steps to import the desired code example (application) into a new workspace in Eclipse IDE for ModusToolbox™:

   ***Note**: ModusToolbox™ supports several other IDEs. For more information, refer to the application note AN243049 - Getting started with PSOC™ Control C3M/P6 MCU on ModusToolbox™ software*

   a. Click **New Application** in the **Quick Panel**

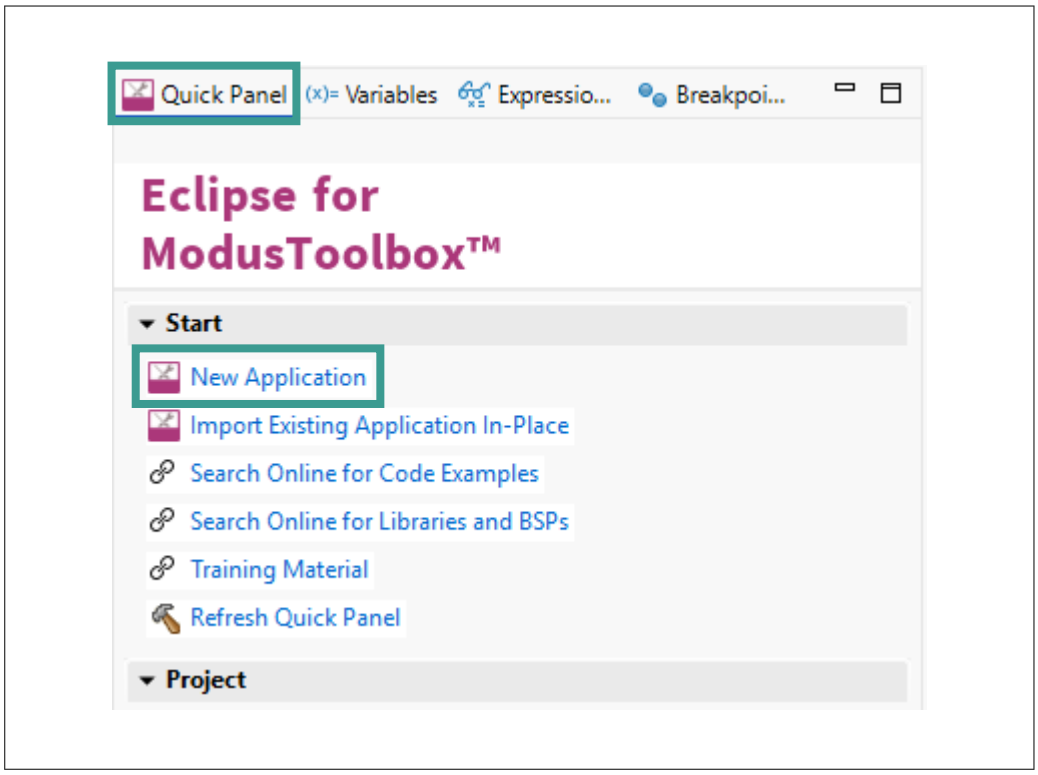



**Figure 7 Opening Project Creator**

   b. Select the BSP in the **Choose Board Support Package** window

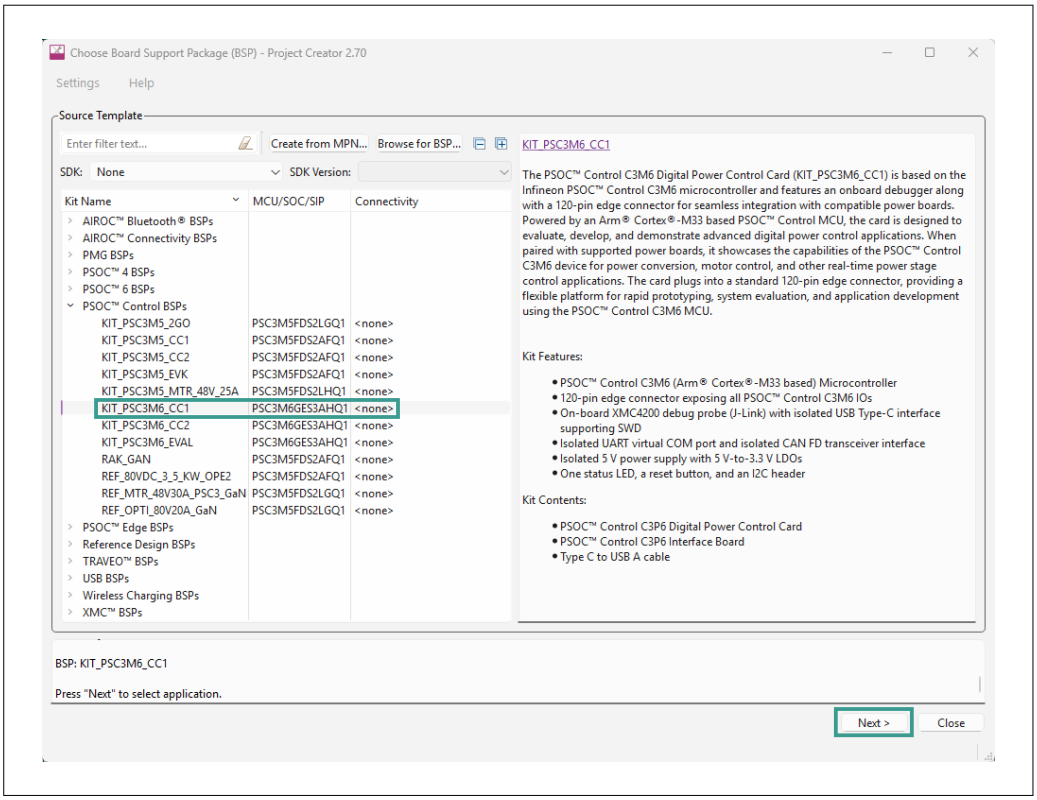



**Figure 8 Board Support Package selection in Project Creator**

**c.** Click **Next**

**d.** Select the application in the **Select Application** window, and then click **Create**

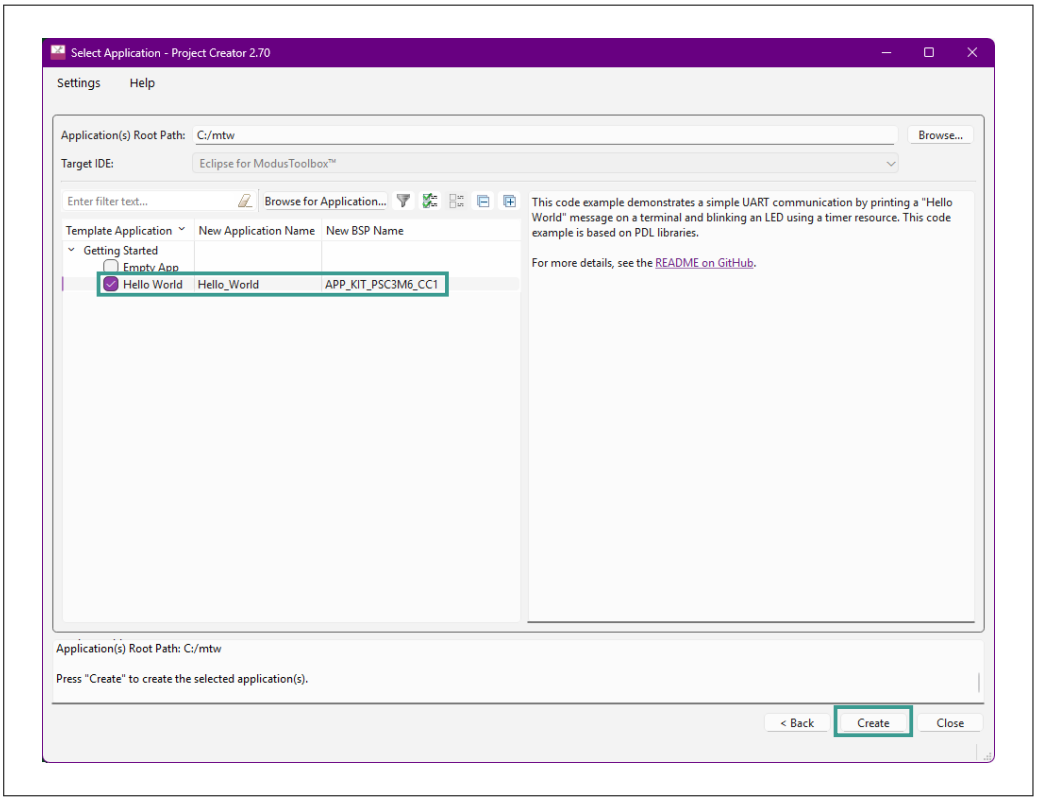



**Figure 9 Code example selection in Project Creator**

**3.** To build and program the application, select the project in the **Project Explorer**. In the **Quick Panel** , scroll to the **Launches** section and click **<Application Name> Program**

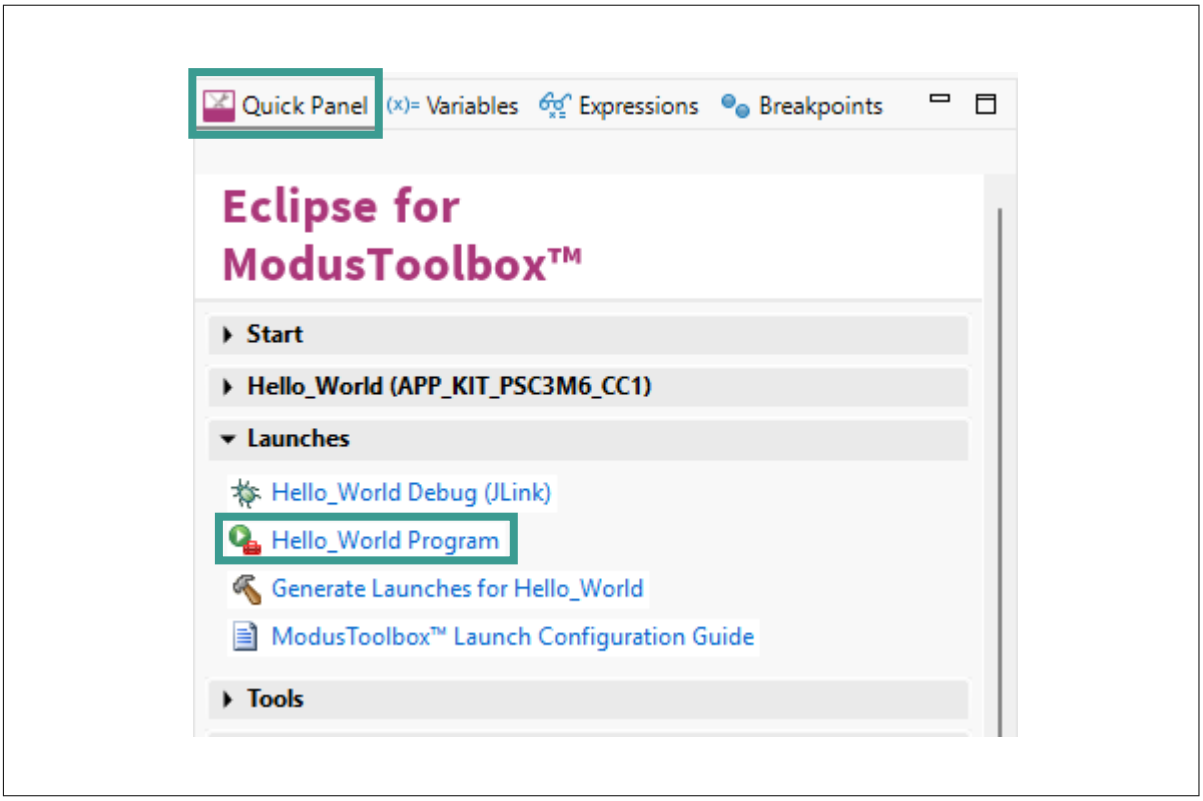



**Figure 10 Programming in ModusToolbox™ Eclipse IDE**

**4.** ModusToolbox™ has an integrated debugger. To debug an application, select the project in the **Project Explorer**. In the **Quick Panel**, scroll to the **Launches** section and click **<Application Name> Debug**

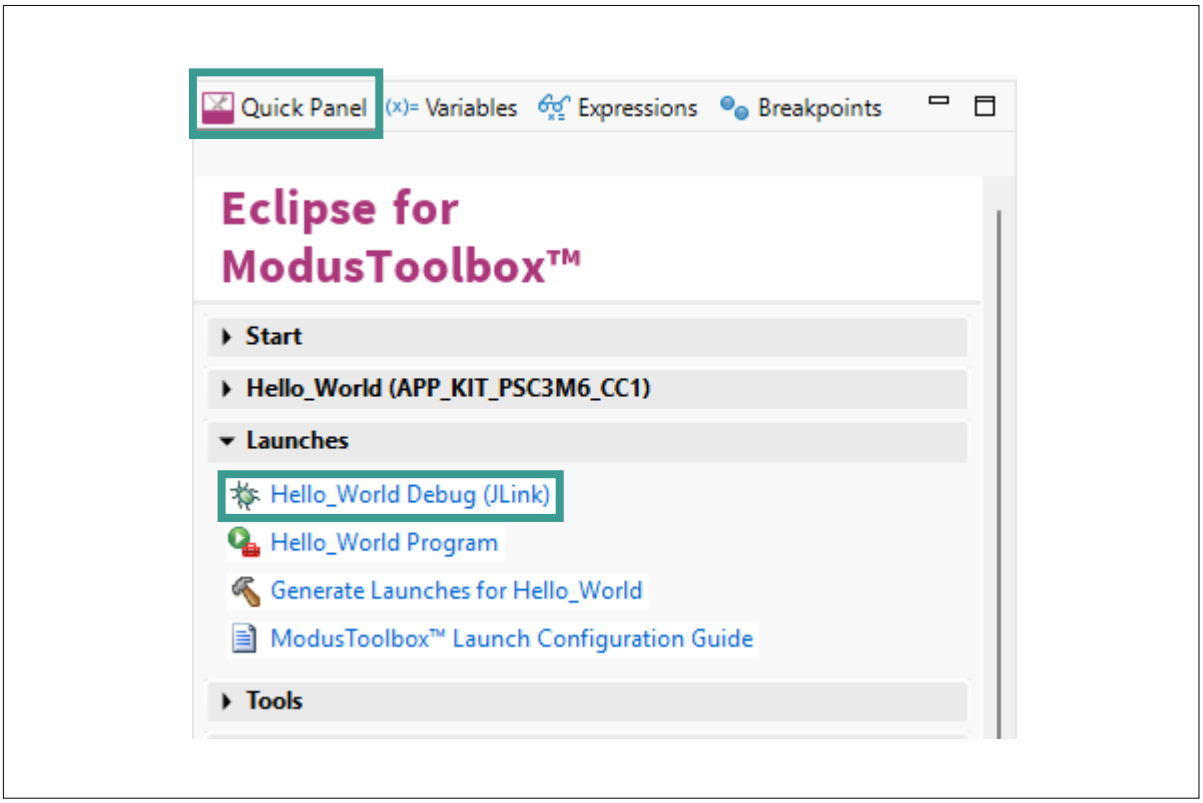



**Figure 11 Debugging in ModusToolbox™ Eclipse IDE**

# 3 Hardware

## 3.1 Control card

The control card integrates the target PSC3M6 controller, the onboard XMC4200 programmer/debugger, isolated programming and communication paths, power-conversion circuitry, clock sources, user controls, and the board-edge connection into a single assembly.

The board is divided into two domains:

- An isolated programmer domain built around the XMC4200 programmer/debugger and the CAN transceiver
- A non-isolated target domain built around the PSC3M6 controller, target USB connector, power-source selection circuitry, target headers, clock sources, reset circuitry, and the 120-pin edge connector

Current and signals cross the programmer-to-target boundary only through the DC-DC isolator and the installed digital isolation devices that carry SWD, UART, CAN, and reset signals between the two domains. The remaining target circuitry is referenced to GND or AGND, while the programmer USB circuitry and CAN transceiver are referenced to `GND_ISO`.

By default, the programmer USB connector provides power and communication to the onboard debugger. The target USB connector and the edge connector provide additional entry points to the target power tree.

The following sections describe the power stages, programmer/debugger, target MCU, CAN subsystem, isolated interfaces, user controls, connectors, and routing options in greater detail.

***Note**: Connector current ratings, GPIO voltage tolerance, ADC input limits, isolation withstand voltage, hot-plug behavior, and system-level power limits are not defined by the schematic package and must not be inferred from it.*

### 3.1.1 Power supply

The power system accepts the supported USB and edge-connector power sources, maintains isolation between the programmer and target domains, and generates the power rails required by the XMC4200 programmer/debugger and the target PSC3M6 controller. Power conversion is implemented using two isolated-domain regulators, one target-domain regulator, and a DC-DC isolator that transfers power across the programmer-to-target boundary without connecting the two ground domains. Loads in the programmer domain return to the isolated ground, while loads in the target domain return to target ground or analog ground.

The board can be powered through the programmer USB connector, target USB connector, or edge connector. The programmer USB connector supplies the isolated domain and the input of the DC-DC isolator. The target-side output of the isolator is connected to the combined VIN rail through D5. The target USB supply is connected to VIN through FB2 and D16, while the edge-connector supply is connected through the external-input protection circuit and D15. U6 converts VIN to the 3.3 V target supply.

Reference and backup supply alternatives are described in the Rework section. Table 2 lists the power path from each source to the corresponding rail and load.

**Table 2 Power-tree summary**

| Source | Conditioning | Combined rail | Conversion/ load | Domain | Default |
|---|---|---|---|---|---|
| J1 VBUS | FB1, Q1-Q3/D2 | +5V0_ISO | U4 to +3V3_ISO; U7 input | GND_ISO | Fitted; R1 bypass DNI |
| U7 output | D5 | VIN | U6 to +3V3 | GND | Fitted |

**(table continues...)**

**Table 2 (continued) Power-tree summary**

| Source | Conditioning | Combined rail | Conversion/ load | Domain | Default |
|---|---|---|---|---|---|
| J8 VIN_CON | Q4-Q6/D9, D15 | VIN | U6 to +3V3 | GND | Fitted; R50 bypass DNI |
| J6 VBUS | FB2, D16 | VIN | U6 to +3V3 | GND | Fitted |

Figure 12 shows each input source from protection through conversion or ORing to the 3.3 V target rail.

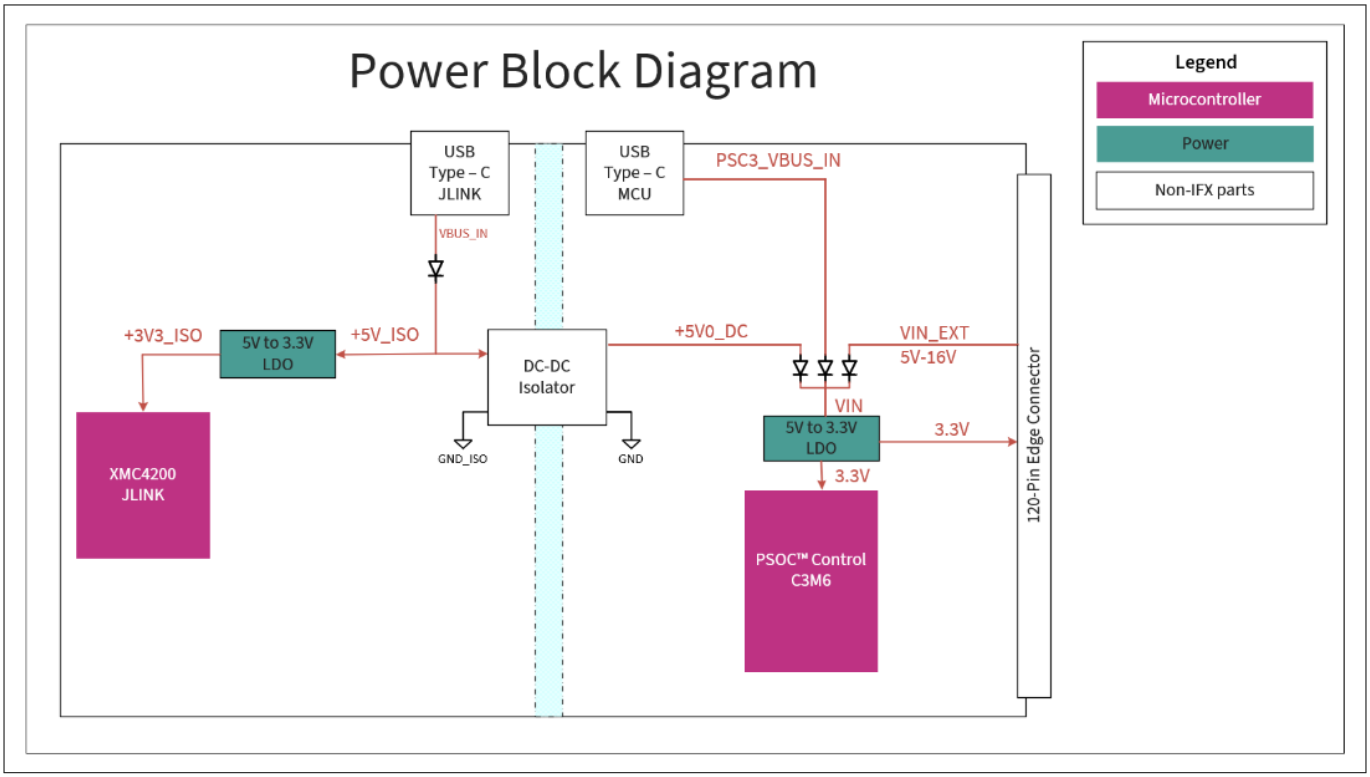



**Figure 12 Power block diagram**

### 3.1.1.1 Isolated power supply

The isolated power-supply entry combines USB power input and USB data conditioning for the XMC4200-side isolated domain.

By default, J1 VBUS feeds FB1 and the protection path. Its D+ and D− conductors pass through TVS array D1 and 22 Ω series resistors R2 and R3 before reaching U2. The CC pins are terminated with 5.1 kΩ resistors R5 and R6, and the connector shield is coupled to `GND_ISO` through R8 and C4.

Do not confuse J1 with the target USB connector J6, which is connected to the target GND rather than `GND_ISO`.

Power and data remain within the same isolated domain but follow different component paths. The power path conditions VBUS into the isolated rails described in the Programmer supply section, while the data path carries USB D+ and USB D− directly to U2. The shield coupling is not a direct signal-ground connection, and the SBU pins are unused.

Because the source package does not include negotiated-current or USB-role information, describe the connector only by its verified sink-side CC resistors, VBUS path, and USB 2.0 data connectivity.

Table 3 summarizes the programmer USB entry by function, implementation, population status, and destination domain.

***Note**: The schematic does not provide a supported procedure for operating the board with R1 fitted. Therefore, the behavior of the protection network under this condition is not established by the source package.*

**Table 3 Programmer USB entry**

| Function | Implementation | Population | Destination/domain |
|---|---|---|---|
| VBUS | FB1 and Q1-Q3/D2 | Fitted | +5V0_ISO/GND_ISO |
| D+/D- | D1 and R2/R3, 22 Ω | Fitted | U2 USB/GND_ISO |
| CC1/CC2 | R5/R6, 5.1 kΩ | Fitted | J1 local termination |
| Shield | R8 parallel C4 | Fitted | GND_ISO coupling |

Figure 13 shows the J1 VBUS connection and the protected D+/D− differential pair routed separately to distinguish the power-supply path from the USB data path.

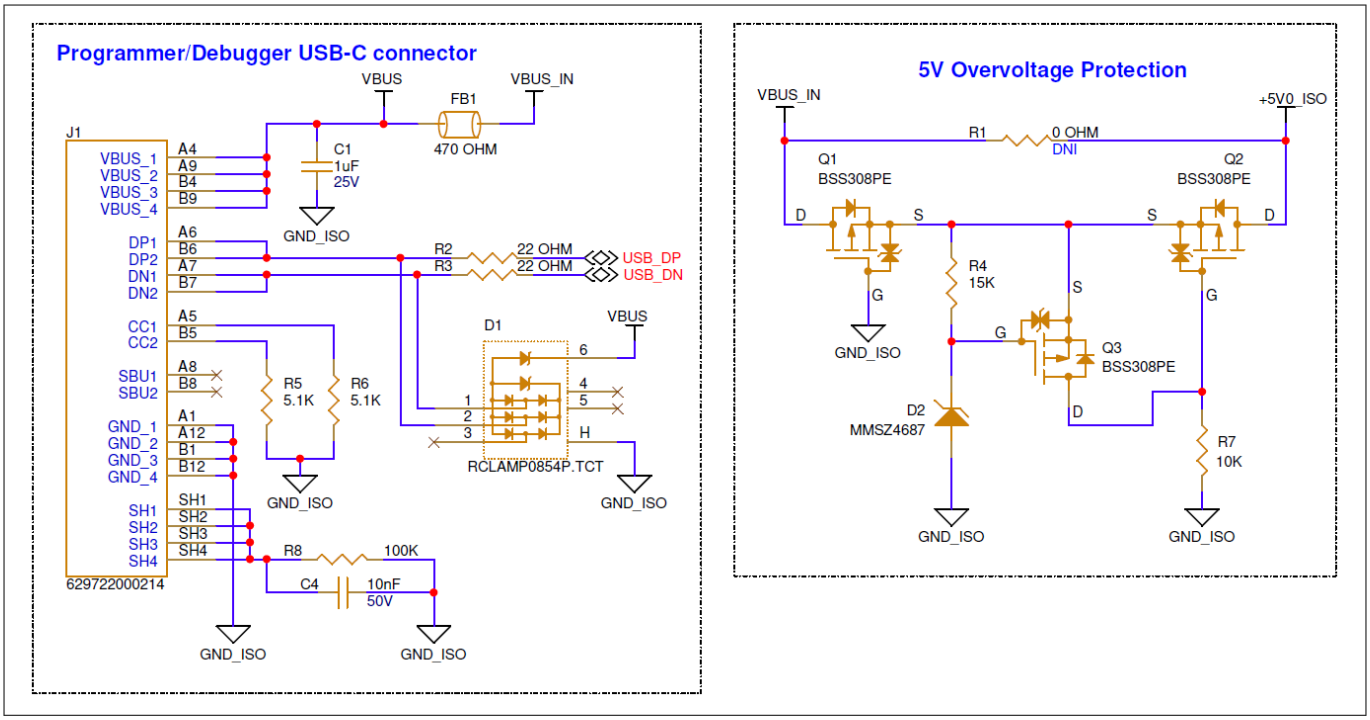



**Figure 13 Isolated power supply**

### 3.1.1.2 DC-DC isolator

The DC-DC stage transfers power from the isolated programmer supply to the target-side power tree, allowing the target domain to be powered from the programmer USB connector without a direct galvanic connection between GND_ISO and target GND.

By default, U7 receives +5V0_ISO referenced to GND_ISO and generates +5V0_DC referenced to target GND. The output is routed through diode D5, which contributes to the VIN rail and, consequently, supplies U6 and the 3.3 V target rail described in the Non-isolated power supply section.

The isolation boundary is defined by both the supply rails and their associated return paths, not by the voltage rail name alone. Loads connected to +5V0_DC share target GND through the output side of the converter, whereas U7 input circuitry and programmer-side loads share GND_ISO.

***Note**: Test equipment connected across both domains can compromise this isolation, even when U7 is installed, because externally connected grounds are outside the control of the board.*

Downstream, the D5 diode path described in ORing power is one of three ORing inputs connected to VIN. As a result, the contribution of +5V0_DC to the target supply depends on the other ORing-source diodes and on the available power sources.

Table 4 summarizes the input and output domains on each side of U7.

***Warning**: **Preserve the intended isolation boundary. Grounded test equipment can externally connect GND_ISO and target GND.***

***Note**: The isolation description provided in the BOM does not constitute assembled-board isolation certification.*

**Table 4 DC-DC domain summary**

| Side | Rail | Ground | Component/ population | Destination |
|---|---|---|---|---|
| Input | +5V0_ISO | GND_ISO | U7 fitted | Isolated DC-DC input |
| Output | +5V0_DC | GND | U7 fitted | D5, then VIN |

Figure 14 shows +5V0_ISO and GND_ISO traced across U7 to +5V0_DC and target GND.

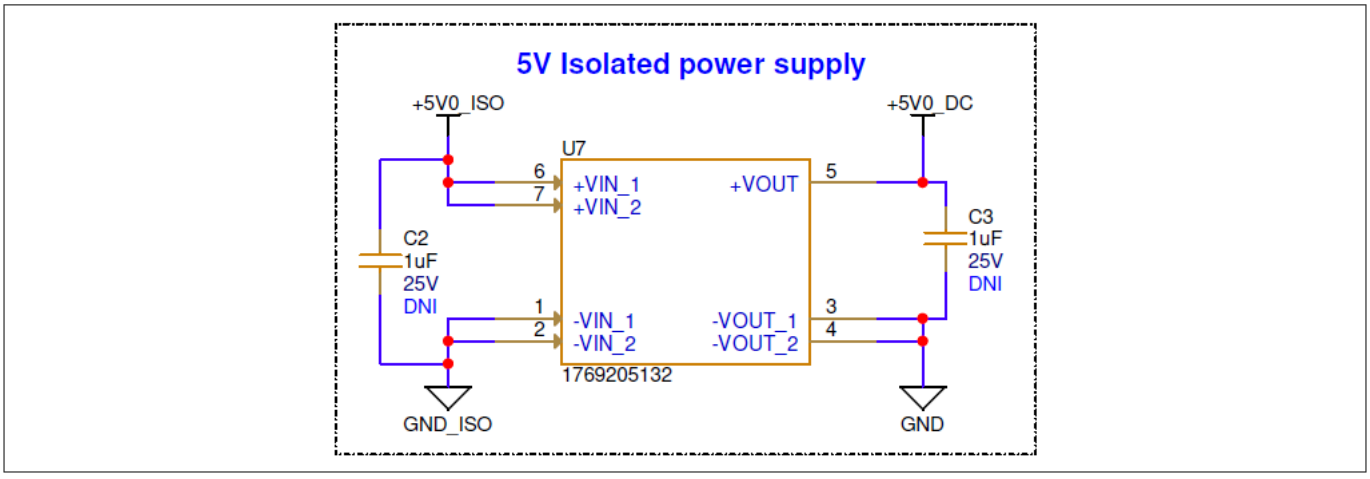



**Figure 14 DC-DC isolated power supply**

### 3.1.1.3 Programmer supply

This circuit generates protected programmer-domain 3.3 V rails from the programmer USB connector J1 (5 V), providing a stable isolated supply for the onboard XMC4200 debugger and its local interfaces.

By default, current flows from the J1 VBUS through the fitted ferrite bead FB1 and the fitted Q1-Q3/D2 overvoltage-protection network to +5V0_ISO, and then through the fitted regulator U4 to +3V3_ISO. Both rails return to GND_ISO and supply the programmer-side circuitry.

The fitted signal path performs two functions in sequence. The input-conditioning stage generates +5V0_ISO, as described in the DC-DC isolator, and U4 generates the local logic rail.

Figure 15 shows the isolated power-supply section.

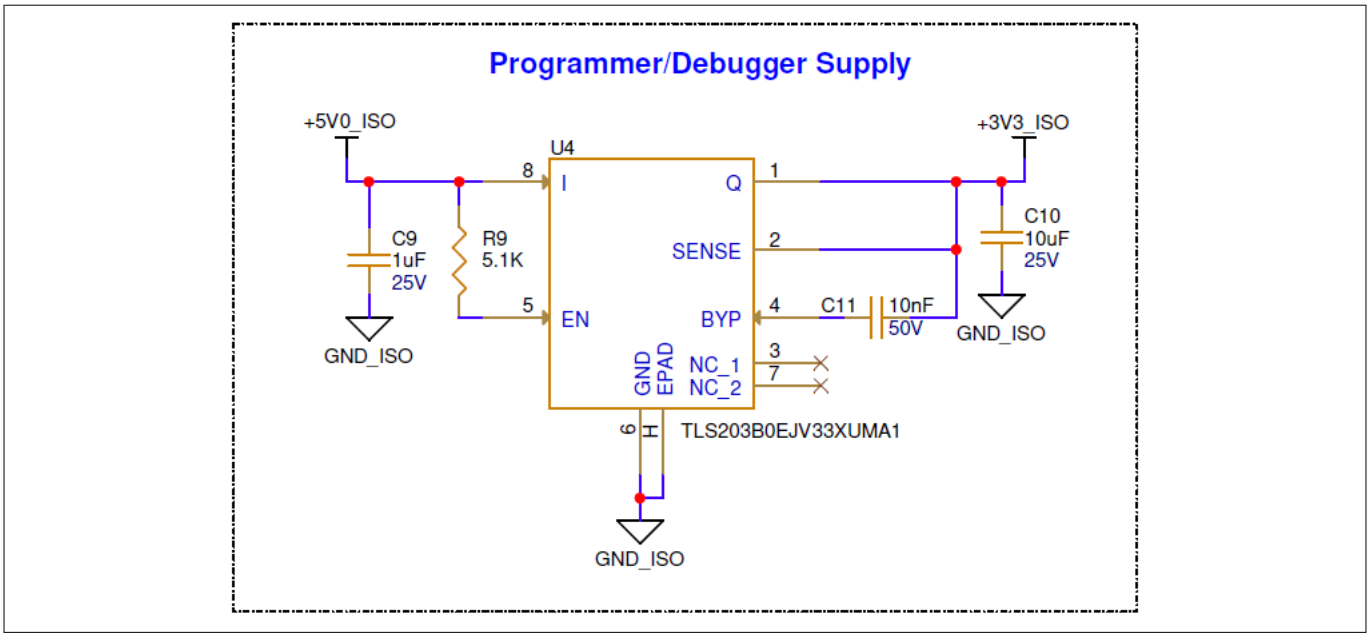



**Figure 15 Programmer supply**

### 3.1.1.4 Non-isolated power supply

A dedicated, non-isolated USB Type-C device connector (J6) is connected to the PSOC™ C3M6 MCU and serves as one of the 5 V power sources (PSC3_VBUS_IN) for the MCU.

The non-isolated supply generates the target +3V3 rail from VIN for the target PSC3M6 controller and associated target-side circuitry.

By default, VIN can be supplied through the three ORing diodes described in ORing power, which lists the diode, destination, and default population status for each path.

**Table 5 Target USB entry - Non isolated power supply**

| Function | Implementation | Population | Destination/domain |
|---|---|---|---|
| PSC3_VBUS_IN | FB2 and Q4-Q5/D9 | Fitted | PSC3_VBUS_IN/GND |
| D+/D- | D17 and R107/R109, 22 ohm | Fitted | U1 USB/GND |
| CC1/CC2 | R46/R47, 5.1 kΩ | Fitted | J6 local termination |
| Shield | R49 parallel C39 | Fitted | GND coupling |

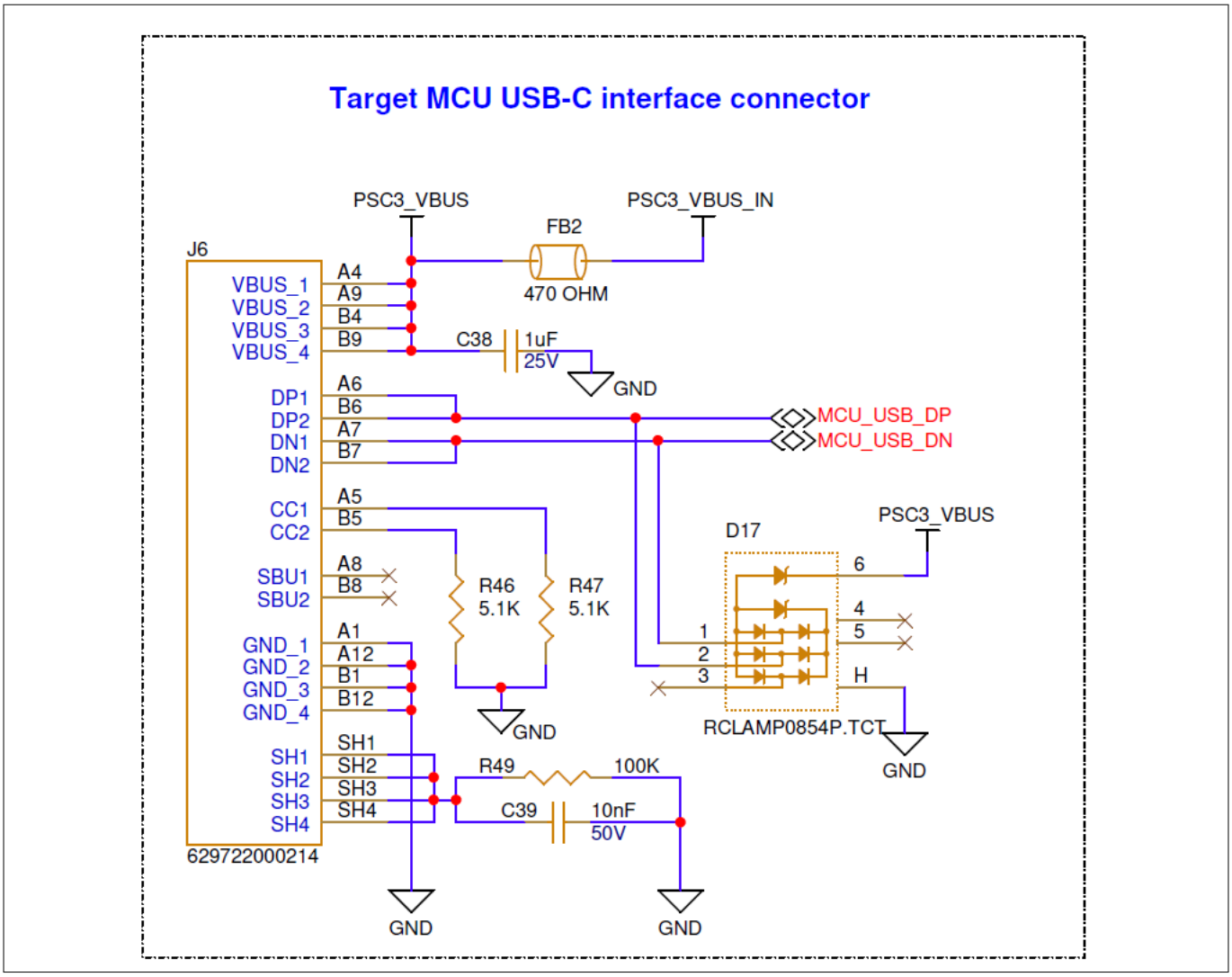



**Figure 16 Non-isolated power supply**

### 3.1.1.5 MCU supply

The PSOC™ C3M6 MCU is powered by a non-isolated 3.3 V (+3V3) rail generated from the 5 V (VIN) output of an ORing circuit through the non-isolated LDO regulator U6.

Regulator U6 converts VIN to +3V3, which supplies the target logic and MCU-derived domains. Diode D10 is connected to the +3V3 rail, while the equivalent footprint for D11 is DNI. The BOM description for U6 specifies a 3.3 V, 300 mA regulator; however, it does not account for board loading, conversion losses, or thermal conditions in the assembled system.

The output of U6 serves as the common source for the target MCU supply links, target-side isolation channels, clock circuits, reset network, and indicators described elsewhere.

D10 and D11 are parallel assembly alternatives and do not represent selectable operating modes.

***Note**: The 300 mA BOM specification for U6 is not a target-board current budget.*

The MCU supply network distributes +3V3 to the target controller's digital, USB, analog, reference, and backup-power domains.

**Table 6 Target regulator and rail protection**

| Item | Input | Output/function | Population | Limitation |
|---|---|---|---|---|
| U6 | VIN | +3V3 | Fitted | 300 mA is component BOM description |
| D10 | +3V3 | Rail TVS path | Fitted | No board-level surge guarantee |
| D11 | +3V3 | Alternate identical footprint | DNI | Not active in released BOM |

Figure 17 shows the generation of +3V3 from the VIN rail.

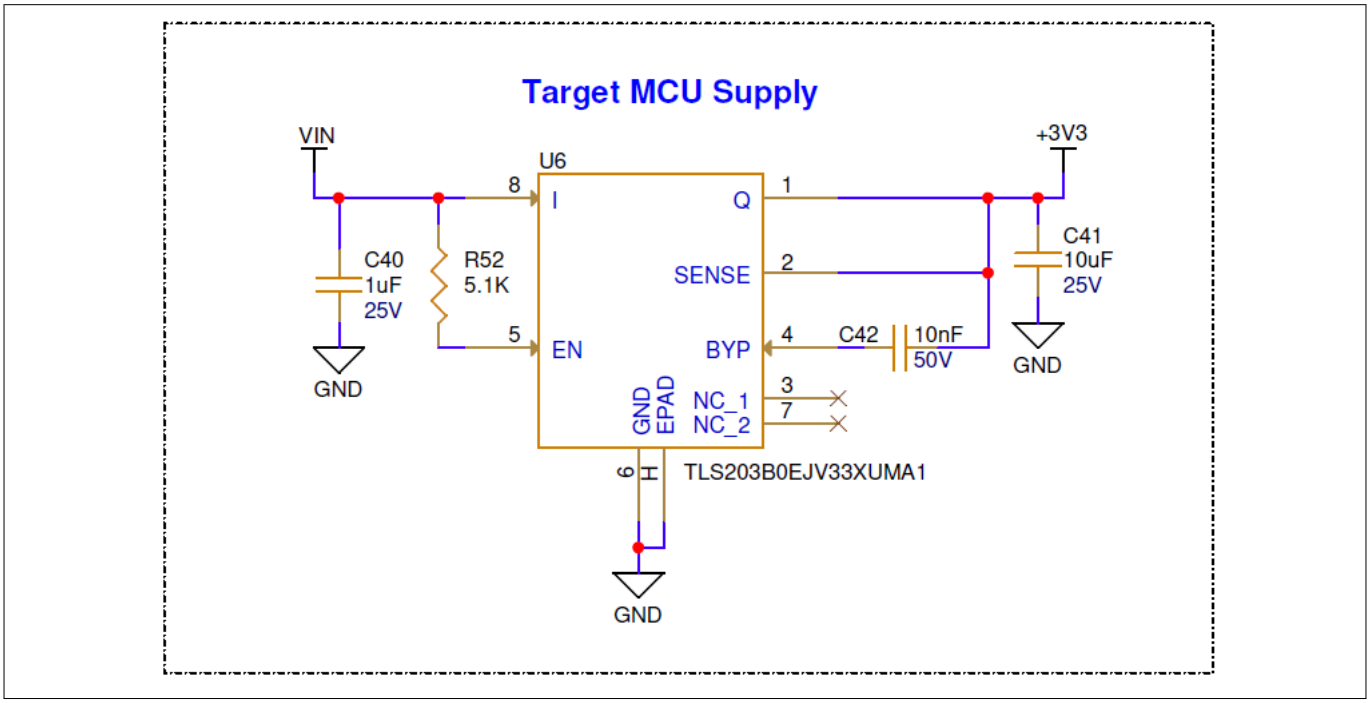



**Figure 17 Target MCU supply**

### 3.1.1.6 ORing power

The ORing network passively combines three target power sources into VIN while limiting direct backfeed through the fitted Schottky diode paths.

By default, the `+5V0_DC` path reaches VIN through D5, the protected `VIN_EXT` path reaches VIN through D15, and the target USB path `PSC3_VBUS_IN` reaches VIN through D16. These three sources correspond to the isolated DC-DC output, external edge-connector input, and target USB connector described earlier.

The network performs passive source combining only. The available sources do not define priority, current sharing, simultaneous-source recommendations, reverse-current limits, or the total VIN load budget.

Each diode feeds the same downstream VIN node. As a result, a source present at any input can influence the rail according to the passive network and the actual source voltages.

***Note**: Do not treat the three inputs as independently software-selectable sources because the combining behavior is determined entirely by the diode network and the connected source voltages.*

Table 7 summarizes each source, its fitted diode, and the corresponding user impact.

**Table 7 VIN ORing paths**

| Source | Fitted series element | Destination | Population | User consequence |
|---|---|---|---|---|
| +5V0_DC | D5 | VIN | Fitted | Isolated supply can contribute |
| VIN_EXT | D15 | VIN | Fitted | Protected edge input can contribute |
| PSC3_VBUS_IN | D16 | VIN | Fitted | Target USB can contribute |

Figure 18 shows the three installed diode paths routed from `+5V0_DC`, `VIN_EXT`, and `PSC3_VBUS_IN` to the common VIN node.

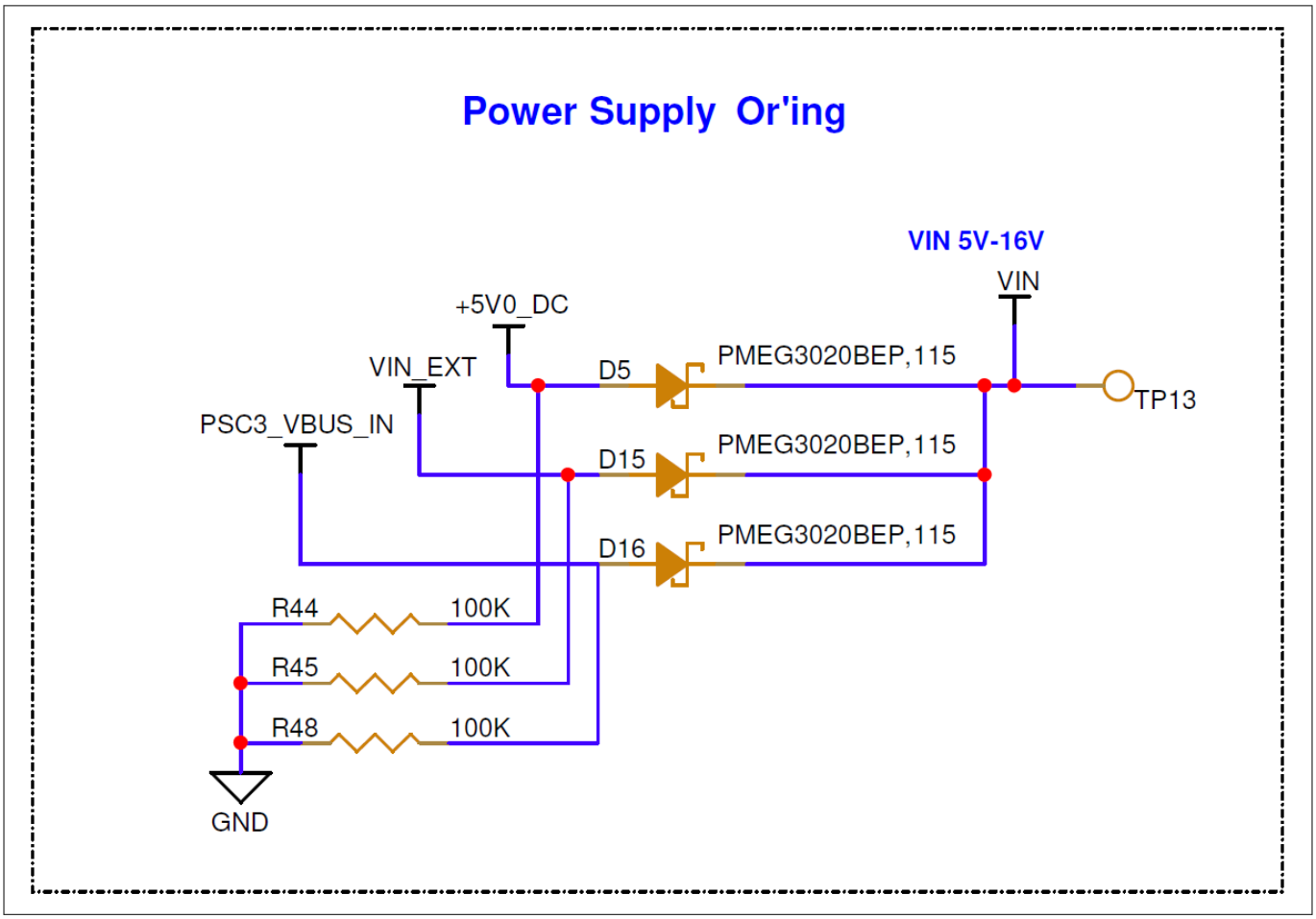



**Figure 18 Power ORing circuit**

### 3.1.1.7 Overvoltage protection

Two discrete overvoltage-protection networks condition the programmer USB input and the external edge-input path before these sources enter their downstream rails.

By default, on the programmer side, `VBUS_IN` passes through Q1-Q3 with D2 to `+5V0_ISO`, and R1 is DNI as the direct bypass. On the edge-input side, `VIN_CON` passes through Q4-Q6 with D9 to `VIN_EXT`, and R50 is DNI as the direct bypass. The downstream diodes described in the ORing power section then feed the power tree.

***Note**: Labels such as "5 V overvoltage protection" and "16 V overvoltage protection" identify schematic blocks and do not represent guaranteed board thresholds or surge-compliance limits.*

The two DNI bypasses would bypass their respective protection networks if populated and therefore materially change fault handling on the associated input path. Because these two networks are independent, a fault or bypass on one path does not, by itself, alter the behavior of the other.

Table 8 compares the two protection paths by input source, fitted network, protected output, and DNI bypass.

***Warning**: **Do not bypass either protection network without released engineering instructions and a review of the resulting input path.***

**Table 8 Protection-path comparison**

| Input | Fitted network | Protected output | DNI bypass | Schematic label |
|---|---|---|---|---|
| VBUS_IN | Q1-Q3 and D2 (4.3 V Zener) | +5V0_ISO | R1, 0 Ω | 5 V overvoltage protection |
| VIN_CON | Q4-Q6 and D9 (15 V Zener) | VIN_EXT | R50, 0 Ω | 16 V overvoltage protection |

Figure 19 and Figure 20 shows the programmer and edge-input protection paths and identifies the associated DNI bypass link for each path.

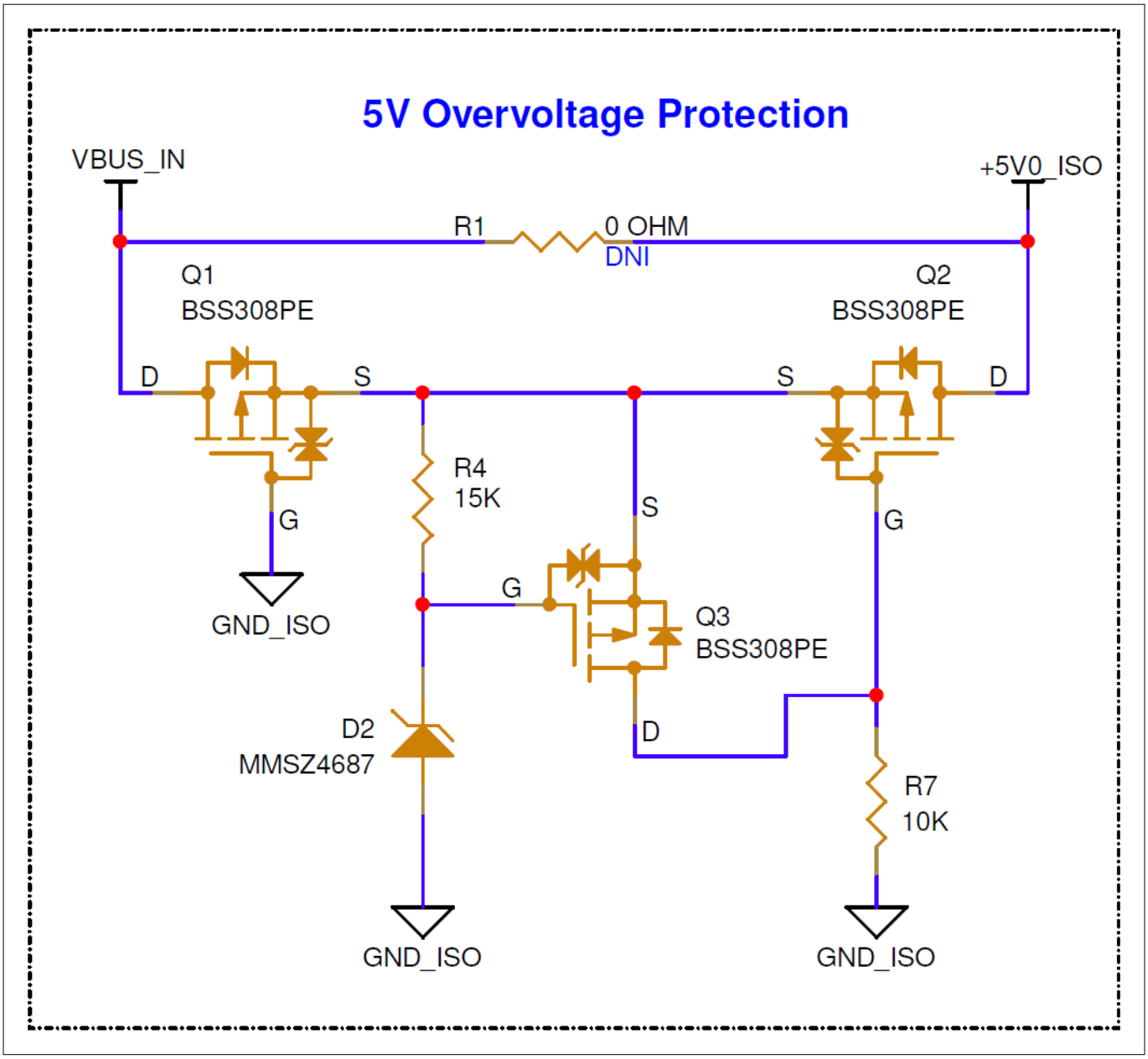



**Figure 19** **5 V overvoltage protection circuit**

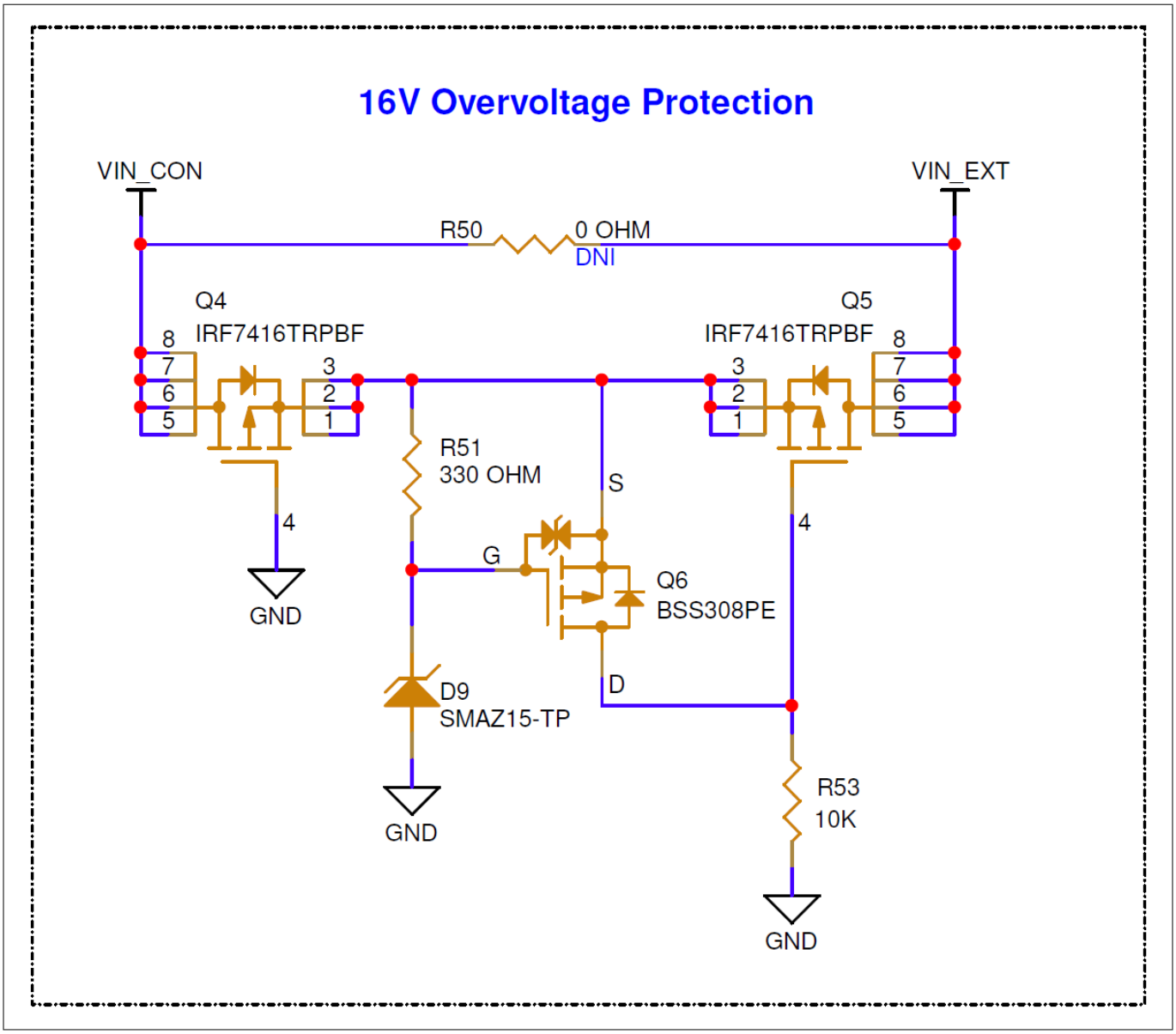



**Figure 20 16 V overvoltage protection circuit**

## 3.1.2 XMC4200 programmer

The XMC4200 programmer/debugger is used to program and debug the PSOC™ C3M6 MCU.

An onboard XMC4200 MCU, which features a 32-bit Arm® Cortex®-M4 CPU, programs and debugs the PSOC™ C3M6 MCU. It is connected to a PC through the isolated USB Type-C connector (J1) and interfaces with the SWD, UART, and other communication interfaces of the PSOC™ C3M6 MCU.

Some features of the XMC4200 MCU are listed below.

**CPU subsystem**:

- High-performance 32-bit Arm® Cortex®-M4 CPU
- 16-bit and 32-bit Thumb-2 instruction set
- DSP/MAC instructions
- System timer (`SysTick`) for operating-system support
- 16 KB on-chip boot ROM
- Up to 256 KB on-chip flash memory with a 1 KB instruction cache

**Communication peripherals**:

- USB 2.0 device interface with an integrated PHY
- Controller Area Network (MultiCAN) interface with Full-CAN/Basic-CAN support, two nodes, 64 message objects (MO), and data rates of up to 1 Mbps
- Four Universal Serial Interface Channels (USIC)

**Control peripherals**:

- Four high-resolution PWM (HRPWM) channels
- Window Watchdog Timer (WDT) for safety-sensitive applications
- Real-Time Clock (RTC) module with alarm support

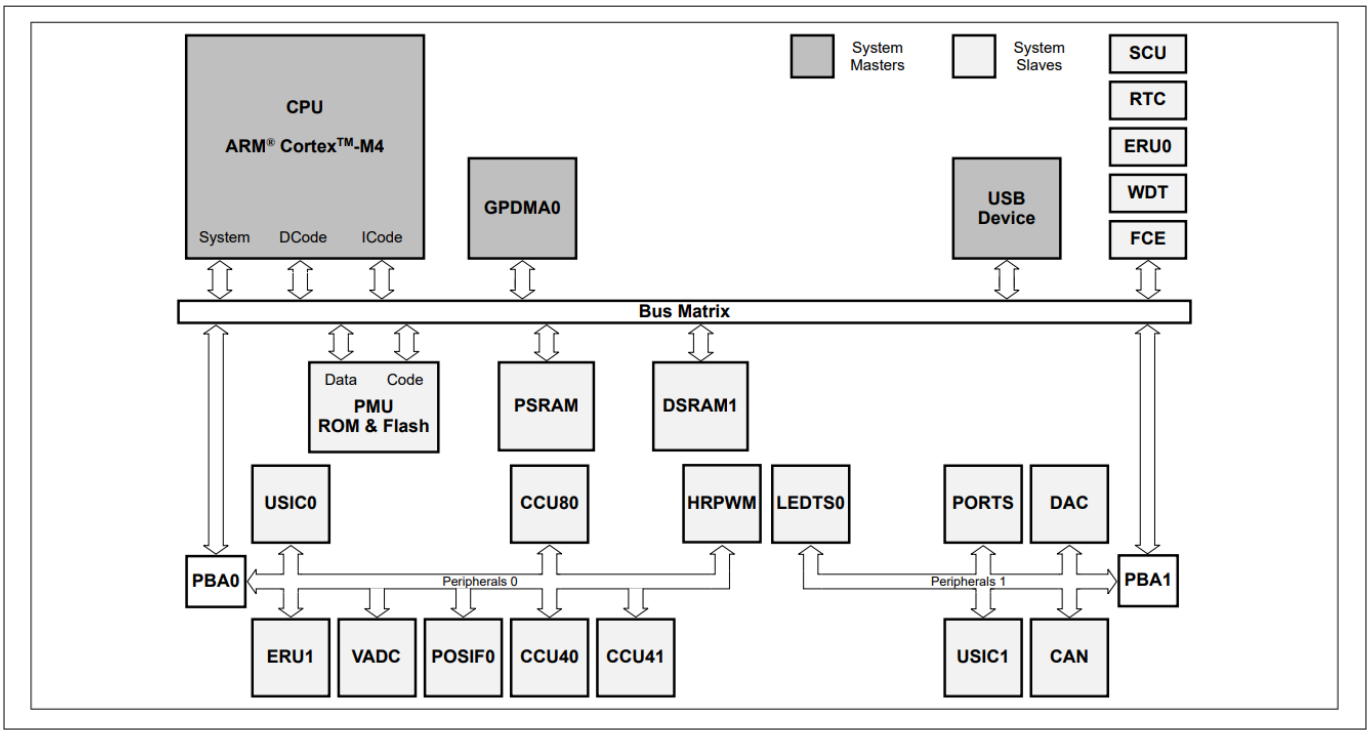



**Figure 21 XMC4200 architecture**

For more information, refer to the following resources:

- XMC4200 Webpage
- XMC4100/XMC4200 family datasheet

The device can be enabled using SEGGER J-Link firmware. Program this firmware using the SEGGER configuration utility to ensure that each device receives the required license.

The onboard XMC4200 circuit provides the USB-connected hardware interface for programming and target-control signal paths across the isolation boundary. U2 serves as the onboard programmer/debugger for the target PSC3M6 controller and resides in the isolated programmer domain rather than the target domain.

The programmer connections are grouped into four related sections:

- Board-level architecture and interfaces
- Isolated-domain power supply
- I/O subsystem routing to the isolation devices and optional header
- Clock architecture

Hardware connectivity alone does not establish driver support, virtual COM-port functionality, programmed firmware, or a default demonstration application.

### 3.1.2.1 Architecture

The XMC4200 architecture section identifies the device's board-level role and the verified interfaces connected to it on the control card. It does not describe firmware, software, or driver behavior that is not supported by the available documentation.

By default, U2 is populated with an XMC4200-Q48F256 BA device in a VQFN-48 package.

By default, U2 receives USB data and the `+3.3 V_ISO` supply, uses the populated crystal Y1 as its clock source, and connects to the SWD, reset, UART, and CAN-control paths that cross to the target side through the digital isolators described in Isolated interfaces. D6 and D7 provide local debugger and communication status indications, and the optional programming header J2 is not populated (DNI).

All XMC4200 connections are confined to the isolated programmer domain. None of the interfaces listed in Table 9 connect directly to the target GND or AGND domains. Only the digital isolators described in Isolated interfaces and the DC-DC isolator described in DC-DC isolator transfer signals or power between the programmer and target domains.

Table 9 summarizes these verified board-level connections only. It does not describe CPU or peripheral capabilities beyond the information provided in the BOM description.

**Table 9 XMC4200 board interfaces**

| Interface | Verified endpoint | Domain | Population |
|---|---|---|---|
| USB | J1 through D1 and R2/R3 | GND_ISO | Fitted |
| Clock | Y1, C22, C23 | GND_ISO | Fitted |
| Debug/control | SWD, reset, UART, CAN-side nets | Across isolators | Fitted paths |
| Indicators | D6 DEBUG_LED; D7 COM_LED | +3V3_ISO | Fitted |
| OBD header | J2 | GND_ISO | DNI |

Figure 22 shows the XMC4200 USB, clock, control, LED, and optional-header signal groups. Use this figure together with the I/O subsystem to trace each signal destination in detail.

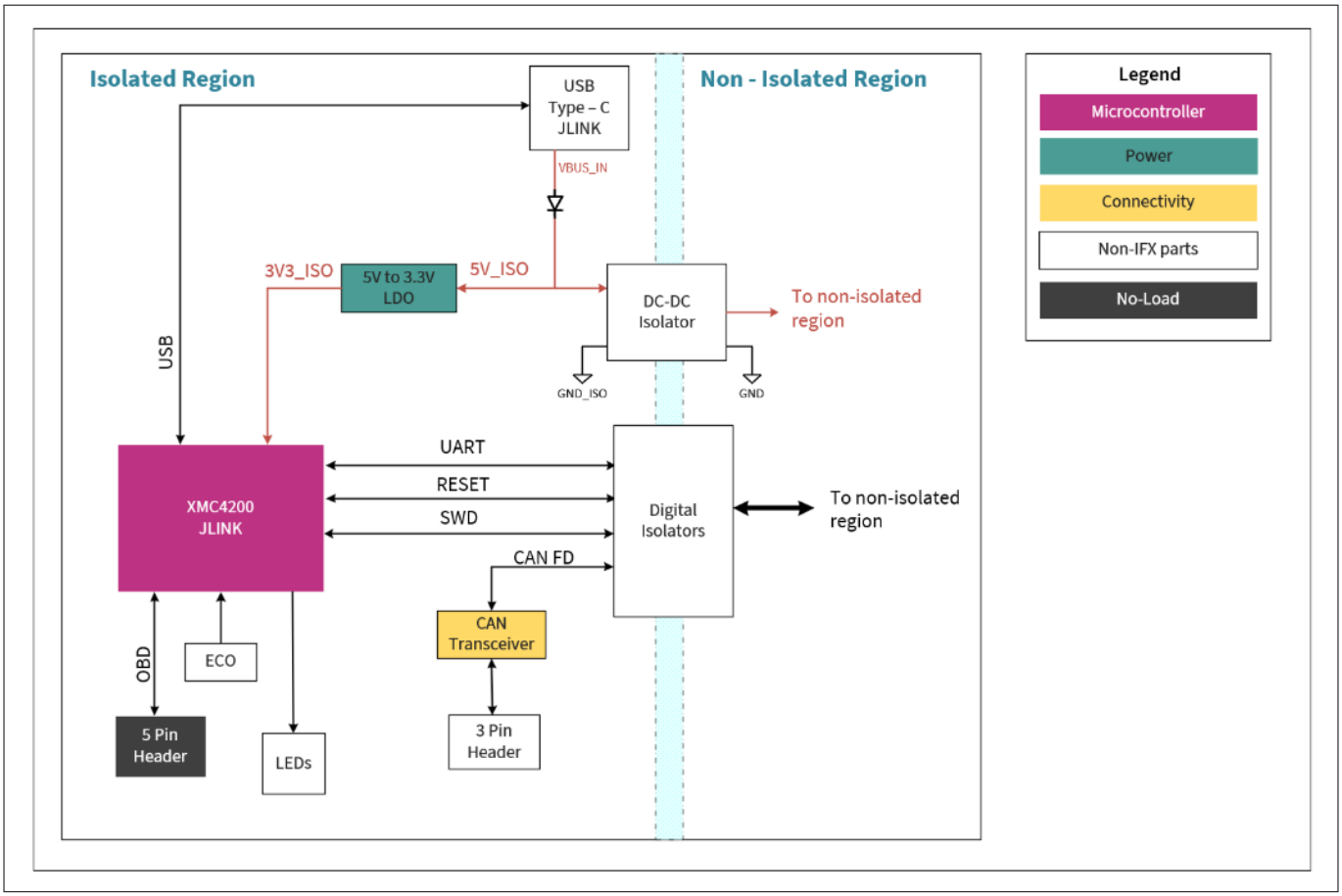



**Figure 22 XMC4200 board-level interface architecture**

### 3.1.2.2 Power supply system

The programmer power subsystem supplies U2 and its local interfaces from the isolated `+3V3_ISO` rail.

By default, `+5V0_ISO` is generated by the programmer input network and converted to `+3V3_ISO` by the isolated regulator U4. The onboard XMC4200, its clock circuitry, status LEDs, USB-side logic, and isolator-side channels operate from this power domain and return to `GND_ISO`.

3.3 V serves as the supply voltage for the core, digital I/O, and analog functions of the device. The power domains and architecture are as follows:

- **VDDP**: Digital supply voltage (3.3 V)
- **VDDC**: Core supply voltage (1.3 V, internally generated)
- **VBAT**: Battery supply voltage for hibernate domains (3.3 V)
- **VDDA**: ADC analog supply voltage (3.3 V)

Target-side power crosses through the DC-DC isolator, while target control signals cross through the digital isolators described in the Isolated interfaces section.

***Note**: The schematic does not directly connect `GND_ISO` to target GND at any point in this power path.*

The isolated power supply (U4) remains entirely on the programmer side, while the DC-DC isolator (U7) is the only verified power-transfer component into the target power tree. No separate XMC4200 supply-selection option exists for the onboard debugger.

Figure 23 shows the power-domain connections of the onboard XMC4200.

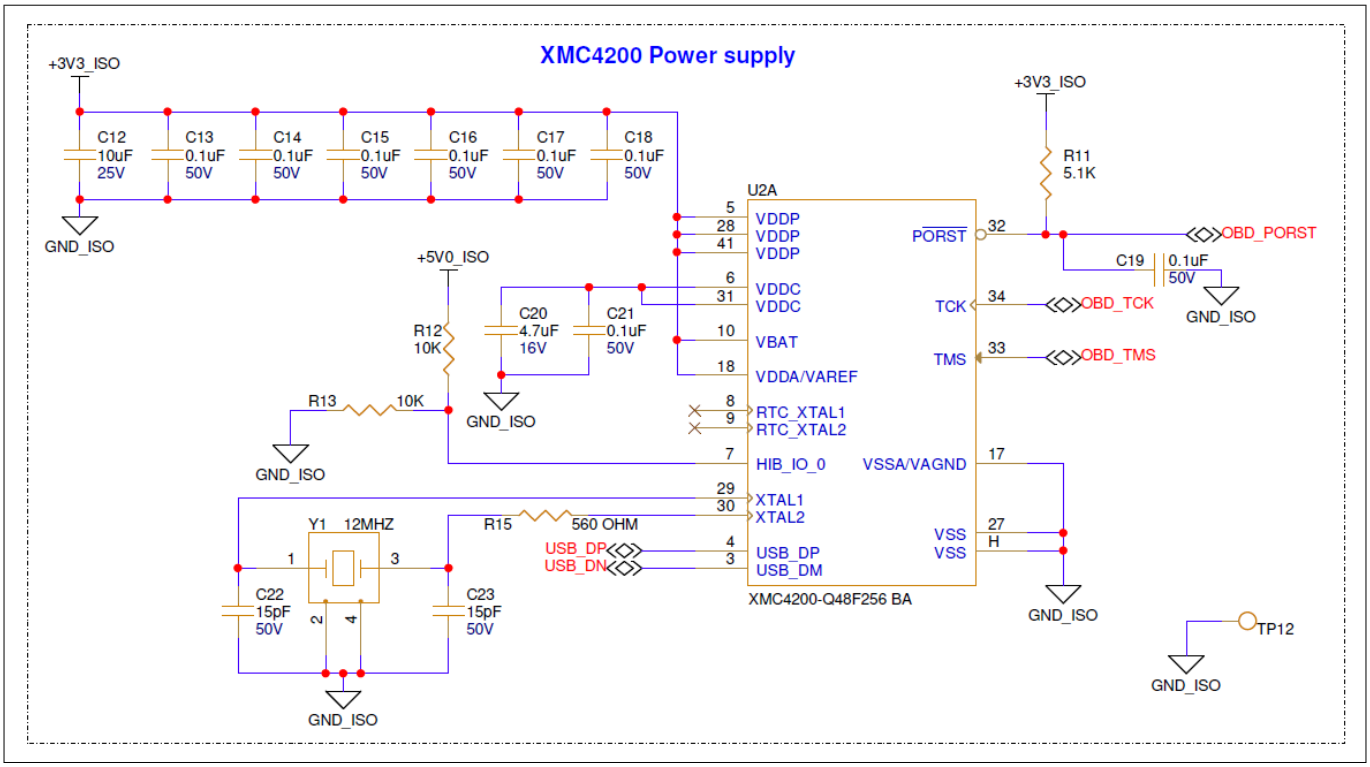



**Figure 23 XMC4200 power domain circuit**

### 3.1.2.3 I/O subsystem

The XMC4200 I/O subsystem routes debug, reset, serial, CAN-control, LED, and optional-header signals to their board-level destinations.

By default, USB connects directly within the programmer domain, while SWD, UART, CAN-control, and reset signals route through isolators U8 and U10 to U12. Populated resistors R25 to R27 serve as 0 Ω assembly links in the CS, SWCLK, and PSOC_RESET signal paths. The optional header J2 is not populated (DNI). If assembled, it provides access to +3.3 V_ISO, OBD_TCK, OBD_TMS, OBD_PORST, and GND_ISO.

These assembly links and the optional header are not user-configurable jumpers. Modifying them requires assembly-level rework and is not a user-adjustable configuration option.

Signal direction varies by function. Therefore, follow the isolator-channel implementation rather than inferring signal direction from connector names. SWD routes through U8 with U9 steering, reset routes through U12 with U13 buffering, and UART and CAN-control signals route through dual-channel isolators U10 and U11, respectively.

The Isolated interfaces section describes these isolator devices from the target-side perspective and identifies the destination buffer and target-side ground domain associated with each channel.

The source documentation defines only the verified net connections for these paths. It does not provide protocol-level behavior beyond the connections summarized in Table 10.

**Table 10 XMC4200 I/O destinations**

| Function | U2-side net/group | Link/device | Destination | Population |
|---|---|---|---|---|
| SWD | OBD_TCK/OBD_TMS path | R25/R26; U8/U9 | Target SWD routing | Fitted |
| Reset | PSOC_RESET | R27; U12/U13 | XRES_L path | Fitted |

**(table continues...)**

**Table 10 (continued) XMC4200 I/O destinations**

| Function | U2-side net/group | Link/device | Destination | Population |
|---|---|---|---|---|
| UART | UART control pair | U10 | Target UART path | Fitted |
| CAN control | CAN logic pair | U11 | U5/target CAN logic | Fitted |
| Optional OBD | TCK/TMS/PORST | J2 | External access | DNI |

Figure 24 shows each U2 control signal routed to its corresponding assembly link, optional header, or isolation-device interface.

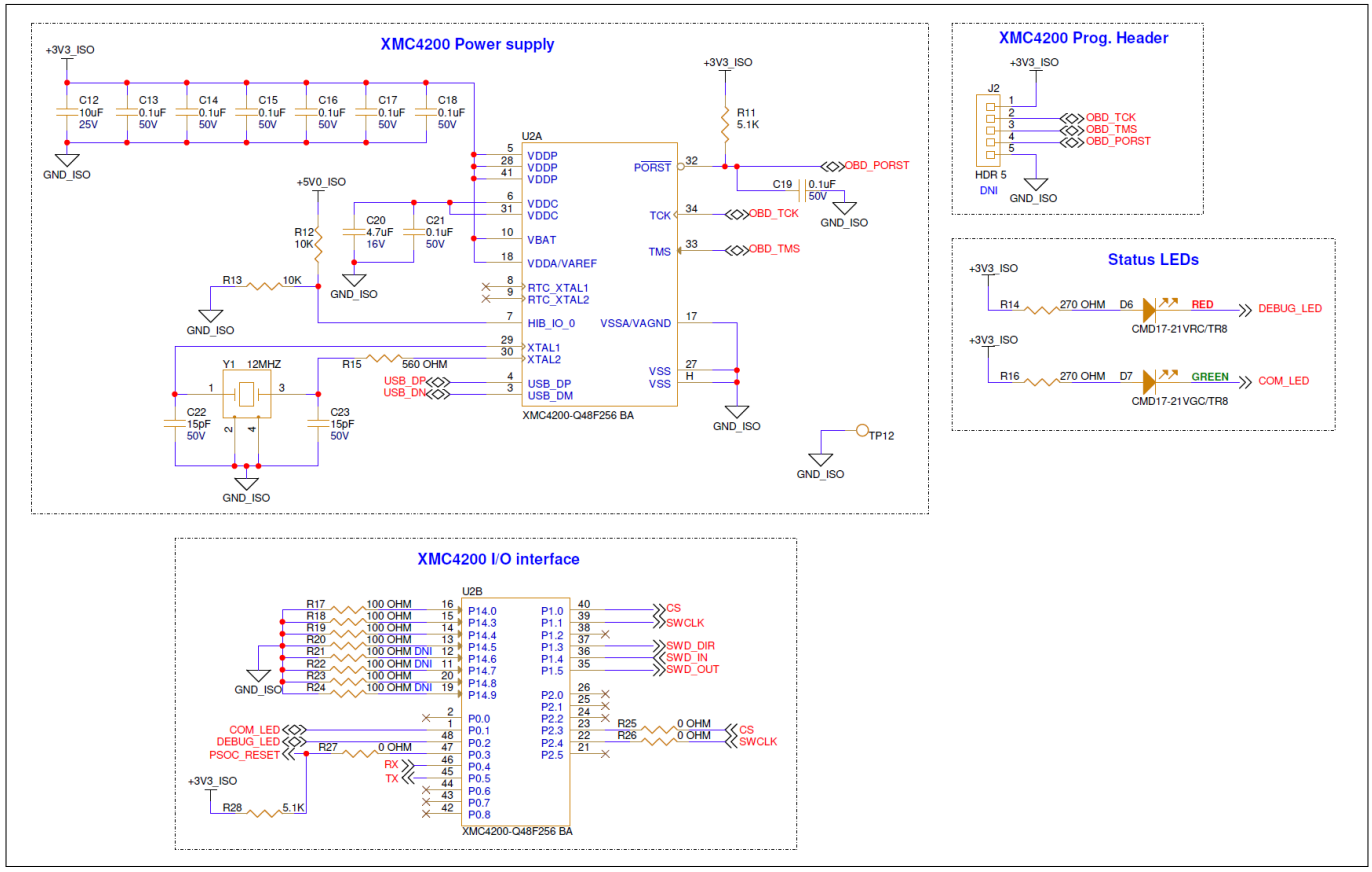



**Figure 24 XMC4200 I/O connections**

## 3.1.2.4 Clock architecture

The programmer clock circuit supplies the XMC4200 crystal reference.

By default, crystal Y1 operates at 12 MHz and uses 15 pF capacitors C22 and C23 connected to the XMC4200 clock pins. No alternate clock population option is shown for this subsystem.

Y1 is local to U2 and is independent of the target WCO and ECO networks described for the PSC3M6 MCU.

***Note**: Removing or replacing these components requires assembly rework and is not a documented user configuration. No fitted/DNI alternative pair is provided for this clock circuit.*

Table 11 summarizes the programmer clock components and their associated block.

**Table 11 Programmer clock components**

| Reference | Function/value | Population | Connected block |
|---|---|---|---|
| Y1 | 12 MHz crystal | Fitted | XMC4200 oscillator |
| C22, C23 | 15 pF load capacitors | Fitted | Y1 network |

Figure 25 shows Y1 and C22/C23 connected between the XMC4200 oscillator pins.

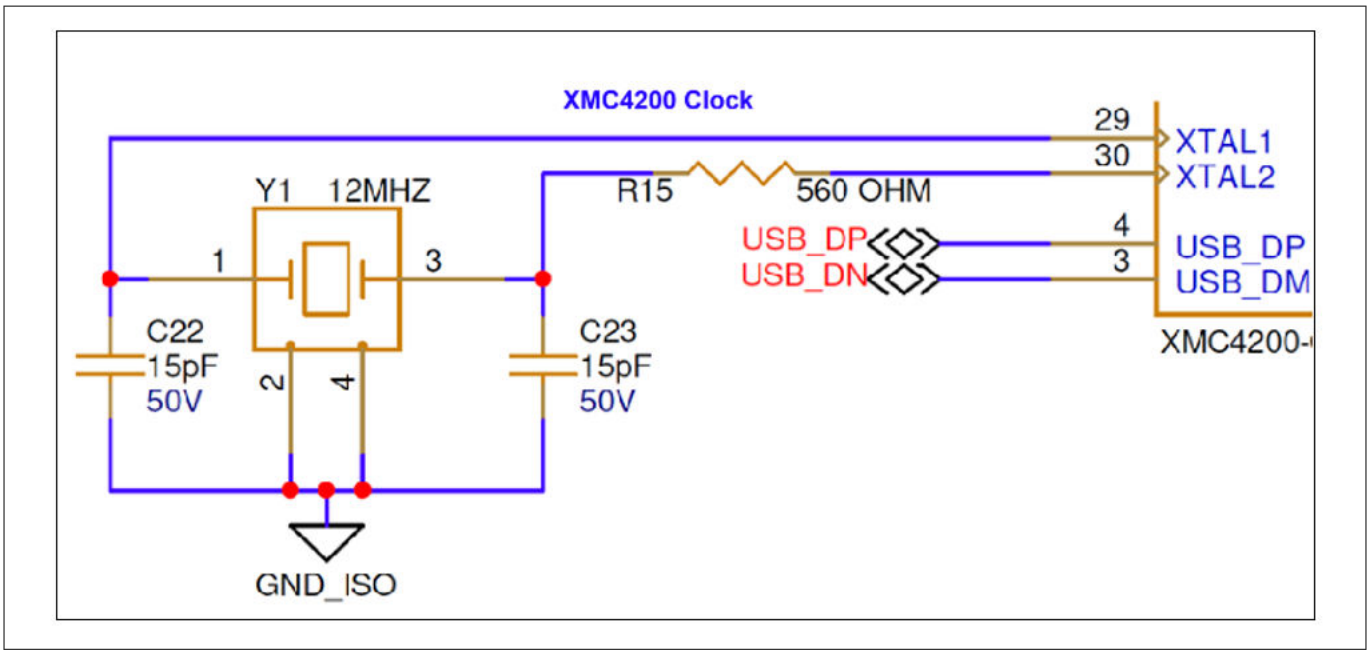



**Figure 25 XMC4200 clock network**

### 3.1.2.5 LEDs

The programmer LEDs provide two hardware-controlled visual indicators in the isolated domain.

By default, D6 is a red LED connected in series with the 270 Ω resistor R14 on the DEBUG_LED net, and D7 is a green LED connected in series with the 270 Ω resistor R16 on the COM_LED net. These LEDs indicate the licensing and connection status of the XMC4200, as defined by the firmware.

For each LED path, current flows from +3V3_ISO through the series resistor and LED to the U2-controlled signal. Both LEDs return to GND_ISO, along with the rest of the isolated domain.

Table 12 summarizes each LED's color, series resistor, supply domain, and control signal.

***Note**: LED-state definitions are firmware-dependent and are not determined by the hardware.*

**Table 12 Programmer LED circuits**

| LED | Color | Series resistor | Supply/domain | Control net | Population |
|---|---|---|---|---|---|
| D6 | Red | R14, 270 Ω | +3V3_ISO/ GND_ISO | DEBUG_LED | Fitted |
| D7 | Green | R16, 270 Ω | +3V3_ISO/ GND_ISO | COM_LED | Fitted |

Figure 26 shows current flowing from +3V3_ISO through each 270 Ω resistor and LED to its corresponding U2-controlled net.

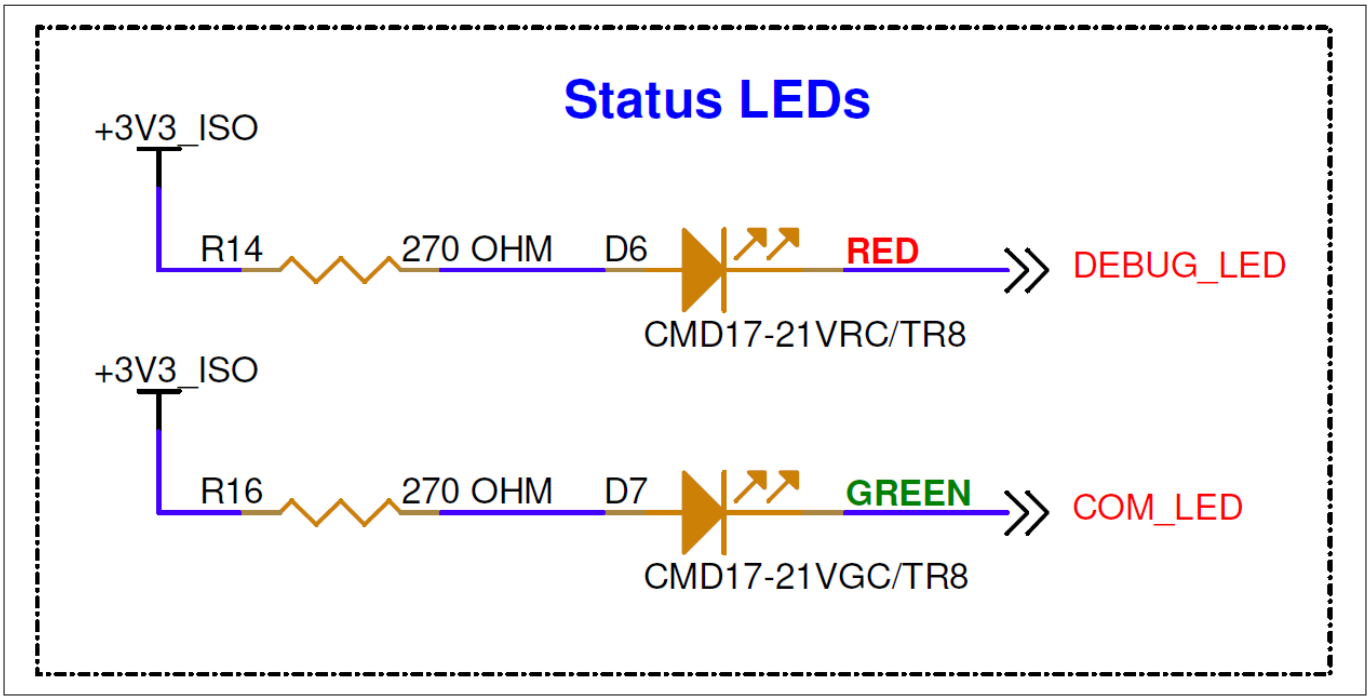



**Figure 26 XMC4200 LED circuits**

### 3.1.3 PSC3M6 MCU

The PSC3P6xx and PSC3M6xx devices are based on the Arm® Cortex®-M33 processor and operate at frequencies of up to 180 MHz with DSP and FPU capabilities. In addition to the CPU subsystem, the devices include advanced real-time control peripherals, such as a high-performance programmable analog subsystem with ADCs, DACs, opamps, and comparators, as well as advanced timers with high-resolution capabilities. The devices support one Active mode and five low-power modes to help manage and reduce power consumption based on application requirements.

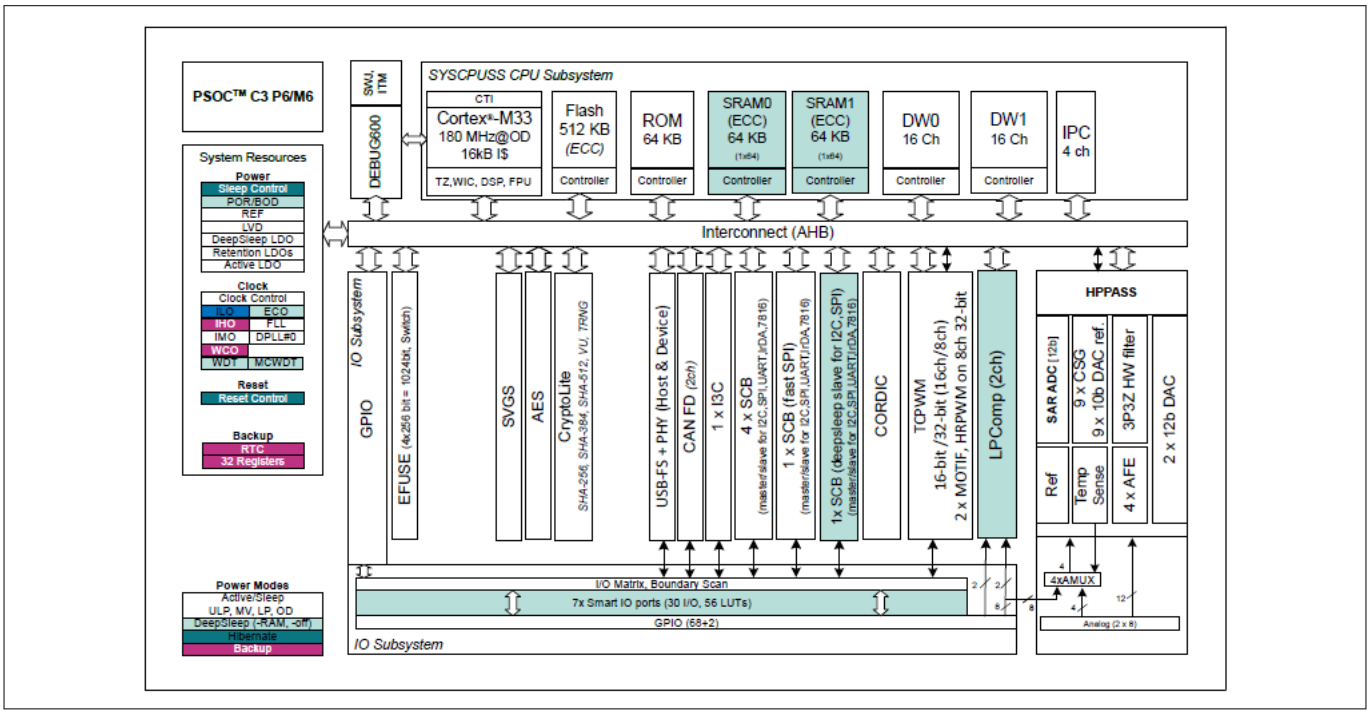



**Figure 27 PSC3M6 MCU architecture**

**PSC3M6xx device features**: PSC3M6GES3AHQ1 (E-LQFP-100), PSC3M6GES3ACQ1 (ELQFP-64)

- Low-power operation from 1.71 V to 3.63 V with six power modes
- 180 MHz 32-bit Arm® Cortex®-M33 CPU
- DSP, FPU, MPU, and 16 KB I-cache
- Two DMA controllers with 16 channels each
- PSA Level 3-certified security
- Up to 512 KB flash memory with ECC support and RWW capability, and 64 KB ROM for boot code
- 128 KB SRAM with ECC support
- Clocking subsystem with an 8 MHz IMO that supports Deep Sleep operation and provides ±2% accuracy
- Serial communication blocks for interfaces such as UART, I2C, and SPI
- Fast SPI support of up to 50 MHz
- Two CAN FD channels in a single instance, supporting data rates of up to 8 Mbps
- USB Full-Speed host and device support
- I3C with OVT I/O support
- Programmable analog subsystem with ADCs and analog comparators
- 12-bit, 9 Msps SAR ADC blocks
- 16 sample-and-hold circuits
- CORDIC support for solving trigonometric and hyperbolic functions
- 16 TCPWM timers with 16-bit support
- Eight 32-bit TCPWM channels supporting HRPWM outputs
- Smart I/O block
- Debug interfaces such as SWD, JTAG, and ETM (Trace)
- 16 dedicated analog input pins
- Up to 68 digital GPIO pins

For more details, refer to the device datasheet.

The target MCU subsystem serves as the central endpoint for digital I/O, analog inputs, clocks, USB, debug, communication interfaces, reset, and the edge connector. All other control-card functions described in this guide are defined relative to this subsystem.

#### 3.1.3.1 Architecture

The PSC3P6xx and PSC3M6xx devices are part of the PSOC™ Control C3 MCU family and are designed for real-time control, enhanced sensing, secure operation, and low-power applications. Typical target applications for these microcontrollers include:

- Industrial motor controllers
- Power-stage converters
- Home appliances
- Automation devices
- Low-power sensors

The PSC3M6 MCU design is divided into power, digital I/O, and analog I/O subsystems and distinguishes the populated U1 package from the DNI U3 alternative.

U1, with the value PSC3M6GES3AHQ1, is the populated 100-pin LQFP implementation. U3, with the value PSC3M6GES3ACQ1, is a DNI 64-pin LQFP alternative. Therefore, only U1 is present on the released assembly.

The schematic divides the target MCU subsystem into power, digital-I/O, and analog-I/O blocks and connects them to the routing matrix, crystal oscillators, USB interface, debug interface, reset circuitry, status LED, and J8.

PSC3M6 MCU through Interfaces describe these blocks as architecture, power supply, digital I/O, analog I/O, clock architecture, and interfaces.

***Note**: The control card provides a dual-footprint option that allows the populated 100-pin LQFP package to be replaced with a 64-pin LQFP package, if required.*

The power subsystem includes VDDUSB, VDDIO, VDDD, VDDA, VCCD, VAREF_EXT, VBACKUP, GND, and AGND connections. The source of each rail is described in the Power supply system section.

The digital-I/O subsystem includes port groups P0 through P13, along with USB, debug, and clock functions. The routing matrix described in the Digital I/O subsystem section routes these signals either to onboard functions or to J8.

The analog-I/O subsystem receives AN_A0 through AN_A7 and AN_B0 through AN_B7 through the filter networks described in the Analog I/O subsystem section.

These subsystems describe board-level connectivity only and do not define CPU-core functionality, memory features, ADC specifications, or device pin limitations.

**Table 13 Target MCU schematic groups**

| Group | Verified contents | External endpoints |
|---|---|---|
| Power | VDDUSB, VDDIO, VDDD, VDDA, VCCD, reference, backup | +3V3 and optional J8 rails |
| Digital I/O | P0-P13, USB, debug, clocks, reset | Onboard functions, headers, J8 |
| Analog I/O | AN_A0-A7 and AN_B0-B7 | Filters and J8/interface headers |
| Package option | U1 100-pin drawing; U3 64-pin drawing | U1 fitted; U3 DNI |

Figure 28 shows the schematic-unit boundaries that separate MCU power, digital I/O, and analog I/O connections, matching the groups summarized in Table 13.

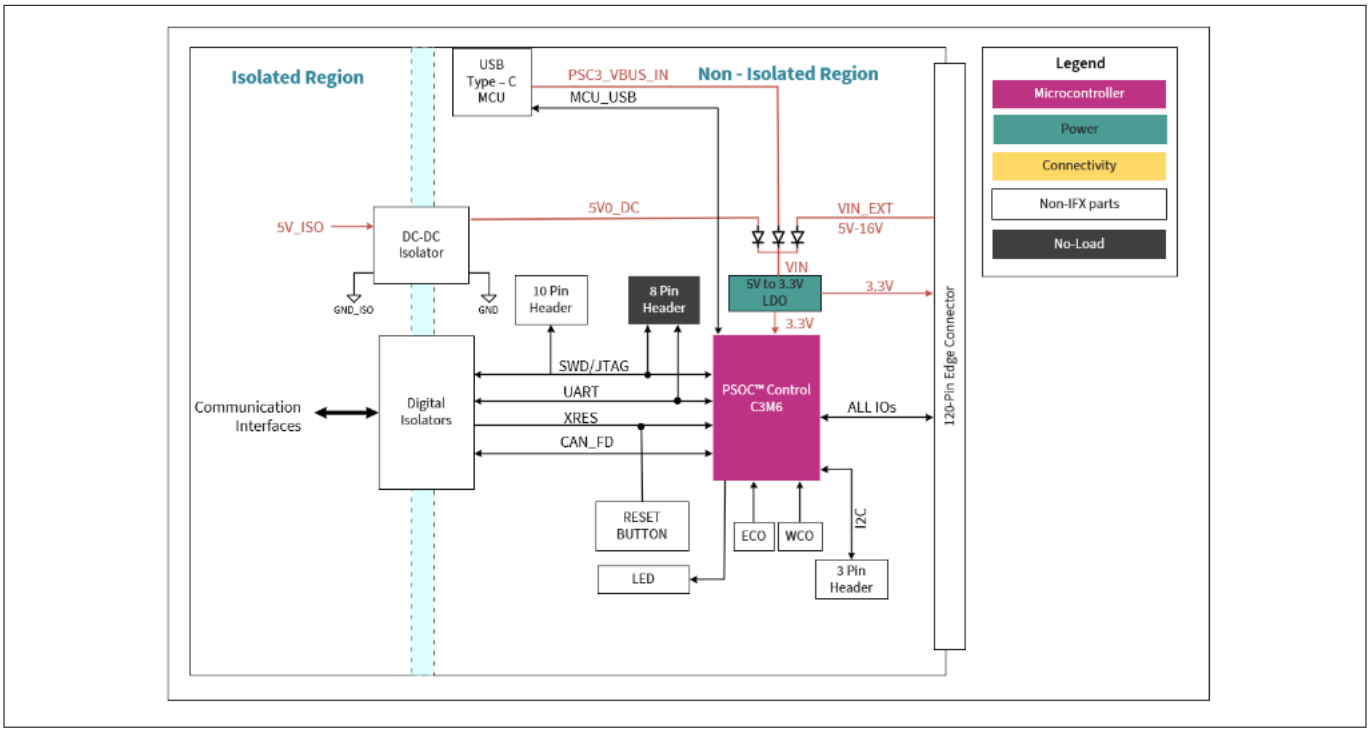



**Figure 28 PSC3M6 MCU board level architecture**

### 3.1.3.2 Power supply system

The PSC3M6 MCU offers multiple features for managing and reducing power consumption. The available power modes include Active, Sleep, Deep Sleep, and Hibernate. Deep Sleep has three variations based on SRAM retention.

The device operates from a single regulated VDDD supply in the range of 1.71 V to 3.63 V. In addition, an optional VBACKUP supply can be used, with a range of 1.4 V to 3.63 V. A linear regulator powers the core logic at four voltage levels: 0.9 V, 1.0 V, 1.1 V, and 1.2 V. Voltage-level switching is implemented by writing to the power-control registers.

The power supplies for the PSC3M6 MCU are as follows:

- **VDDD (core power)**: 1.71 V to 3.63 V
- **VDDIO (digital I/O power)**: 1.71 V to 3.63 V
- **VDDA (analog I/O power)**: 1.71 V to 3.63 V
- **VBACKUP**: 1.71 V to 3.63 V from VDDD, or 1.4 V to 3.63 V from a backup source
- **VDDUSB**: 1.71 V to 3.63 V (GPIO) or 3.0 V to 3.63 V (USB)
- **VAREF_EXT**: 1.71 V to VDDA
- **VCCD**: 0.9 V to 1.2 V (internally generated)

By default, R64 and R65 feed VDDUSB and VDDIO directly from +3V3. FB5 feeds VDDD, and FB6 feeds VDDA. FB3 and R66 select +3V3 for VAREF_EXT and VBACKUP, respectively.

***Note**: FB4, FB7, and R67 provide external alternatives and require removal of the corresponding default components before use. VCCD capacitors and local decoupling components support the controller pins connected to U1.*

AGND and GND are identified separately around the MCU and the analog-input filters. The analog and digital grounds are connected through 0 Ω resistors.

***Note**: The reference and backup rework options described in the Rework section section depend on the same +3V3 distribution. Cross-check any change to one domain against the others before performing rework. Table 14 summarizes the default source and alternate source for each MCU supply domain.*

***Warning**: Never install an external-source option before removing its paired +3V3 default link.*

The resulting default configuration uses a single +3V3-derived set of MCU domains, with filtering or zero-ohm isolation provided by the listed components. External inputs are available at J8 but remain disconnected through DNI components. The alternate nets VDDA_C, VAREF_EXT_C, and VBACKUP_C connect to the MCU only after their corresponding default components are depopulated.

**Table 14 MCU rail-source view**

| MCU domain | Fitted source | DNI alternative | Related rework |
|---|---|---|---|
| VDDUSB | +3V3 through R64 | None shown | None |
| VDDIO | +3V3 through R65 | None shown | None |
| VDDD | +3V3 through FB5 | None shown | None |
| VDDA | +3V3 through FB6 | VDDA_C through FB7 | 3.3.5 |
| VAREF_EXT | +3V3 through FB3 | VAREF_EXT_C through FB4 | 3.3.5 |
| VBACKUP | +3V3 through R66 | VBACKUP_C through R67 | 3.3.5 |

Figure 29 shows the power-supply connections for the PSC3M6 MCU in both the E-LQFP-100 and E-LQFP-64 pin packages.

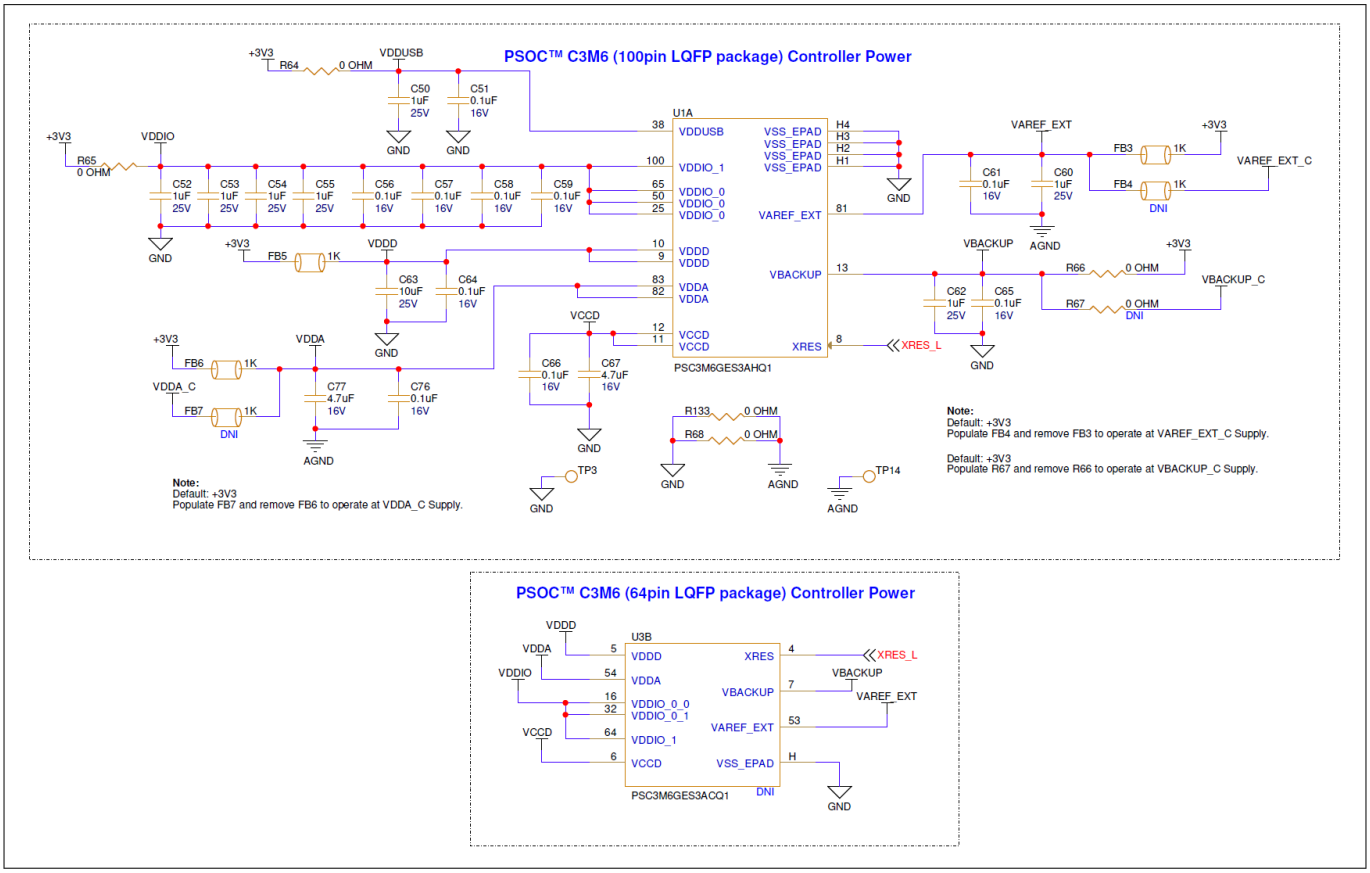



**Figure 29 Target MCU rail-source configuration**

## 3.1.3.3 Digital I/O subsystem

The digital I/O subsystem connects MCU pins to either onboard functions or the edge connector through a fitted/DNI resistor-routing matrix.

Clock pins default to onboard crystals. UART and CAN pins default to isolated onboard paths. $I^2C$ pins default to J8, and USB pins default to target USB connector J6 through fitted 22 Ω resistors. TDI and TDO use fitted links. Therefore, the signal name printed for J8 identifies an available edge-connector net and does not necessarily indicate the fitted destination of the MCU pin. Rework sections - Rework for MCU clock through Rework for E-LQFP-64 pin PSC3M6 MCU describe the paired changes. Table 15 lists one representative pin pair for each routed function rather than every MCU pin.

CAN and UART connections are established across the isolated, non-isolated, and external sections through the digital-isolator and edge-connector network.

The paired resistors represent physical assembly options rather than run-time multiplexers. Changing a route changes which external circuit can drive or monitor the MCU pin and can disconnect an onboard function. USB differs from the 0 ohm resistor groups because both the fitted and alternate links use 22 Ω series resistors. This configuration reflects a series-termination function rather than simple link selection.

**Table 15 Default digital routing**

| Function/pins | Onboard endpoint | Edge endpoint | Fitted link | DNI alternate |
|---|---|---|---|---|
| WCO P0.0/P0.1 | Y2 network | J8 clock nets | R85/R90 | R87/R92 |

**(table continues...)**

**Table 15 (continued) Default digital routing**

| Function/pins | Onboard endpoint | Edge endpoint | Fitted link | DNI alternate |
|---|---|---|---|---|
| ECO P1.0/P1.1 | Y3 network | J8 clock nets | R94/R97 | R96/R99 |
| UART P5.3/P5.2 | Isolated UART | J8 UART nets | R101/R104 | R103/R106 |
| CAN P6.2/P6.3 | Isolated CAN | J8 CAN nets | R93/R98 | R95/R100 |
| I2C P7.0/P7.1 | J4 nets | J8 I2C nets | R86/R89 edge | R88/R91 local |
| USB P11.1/P11.0 | J6 USB | J8 USB nets | R107/R109, 22 ohm | R108/R110, 22 ohm |

Figure 30 shows representative MCU pins routed through the routing matrix to onboard functions for the PSC3M6 MCU in both the E-LQFP-100 and E-LQFP-64 pin packages.

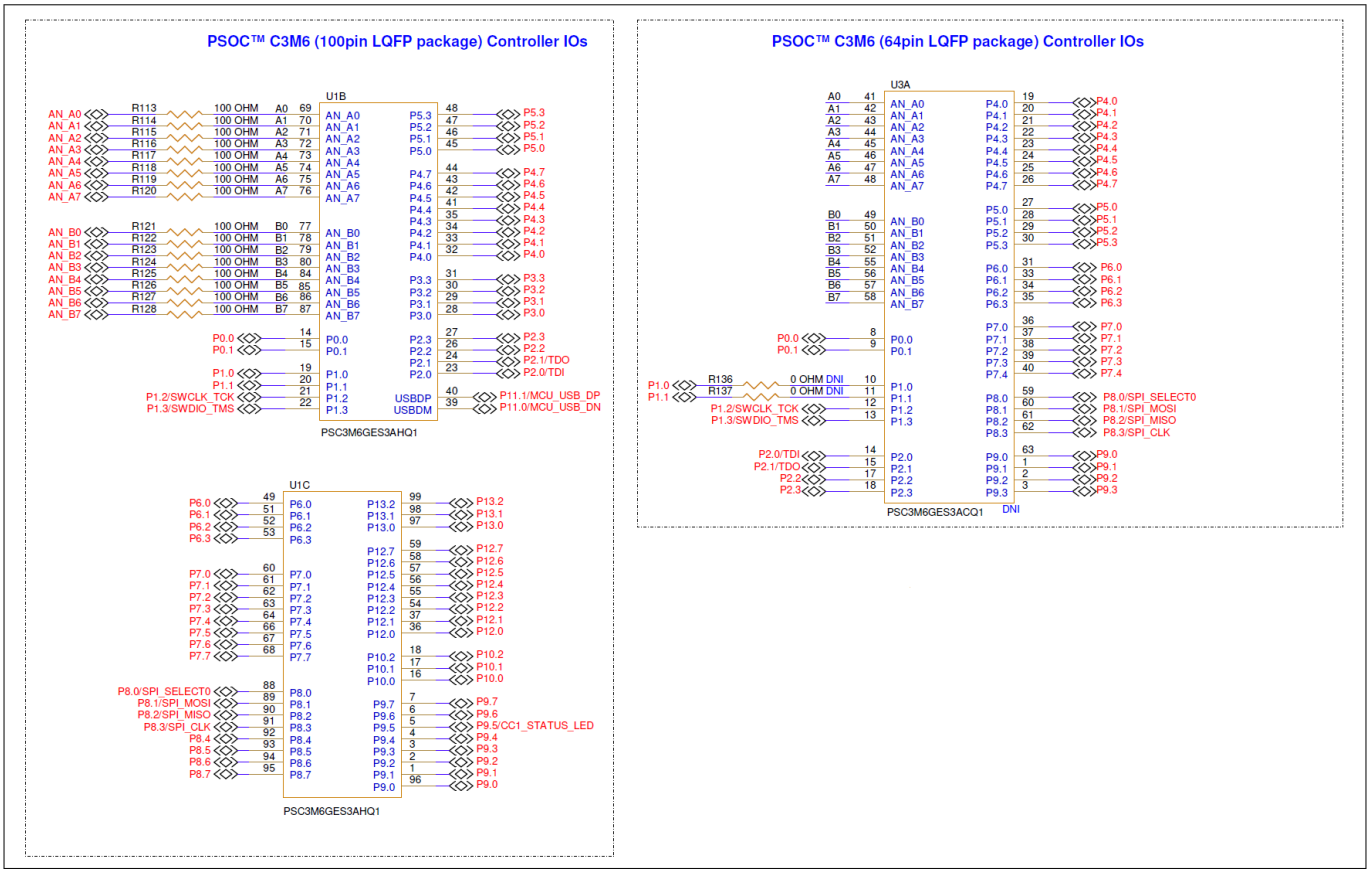



**Figure 30 Target digital I/O connections**

## 3.1.3.4 Analog I/O subsystem

The analog I/O subsystem routes sixteen named channels, `AN_A0` to `AN_A7` and `AN_B0` to `AN_B7`, to the MCU through identical resistor-capacitor input networks arranged as two eight-channel banks in the E-LQFP-100 and E-LQFP-64 pin packages.

In addition to these channels, port pins P7.4 to P7.7 and P8.0 to P8.5 provide analog functionality in the E-LQFP-100 pin package. In the E-LQFP-64 pin package, only P7.4 supports analog functionality.

**Note:** In this design, P8.0 to P8.4 are dedicated to SPI functionality.

Each named channel connects through a 100 Ω resistor (R113 to R128) and includes a 100 pF capacitor (C81 to C96) connected to AGND before reaching U1. This repeated network is implemented across both eight-channel

banks and forms a simple low-pass filter ahead of the MCU analog pins. Both banks are also accessible through J8, as summarized in the Interfaces section.

This section documents the filtering topology only. The schematic and BOM do not provide sufficient information to specify input-voltage range, source impedance, conversion accuracy, bandwidth, settling characteristics, or calibration requirements.

***Note**: Analog-input range, accuracy, bandwidth, source-impedance limits, and calibration requirements are not available.*

**Table 16 Analog input filter groups**

| Channels | Series resistors | Shunt capacitors | Return | Population |
|---|---|---|---|---|
| AN_A0-AN_A7 | R113-R120, 100 Ω | C81-C88, 100 pF | AGND | Fitted |
| AN_B0-AN_B7 | R121-R128, 100 Ω | C89-C96, 100 pF | AGND | Fitted |

Figure 31 shows the analog-signal connections for the PSC3M6 MCU in both the E-LQFP-100 and E-LQFP-64 pin packages.

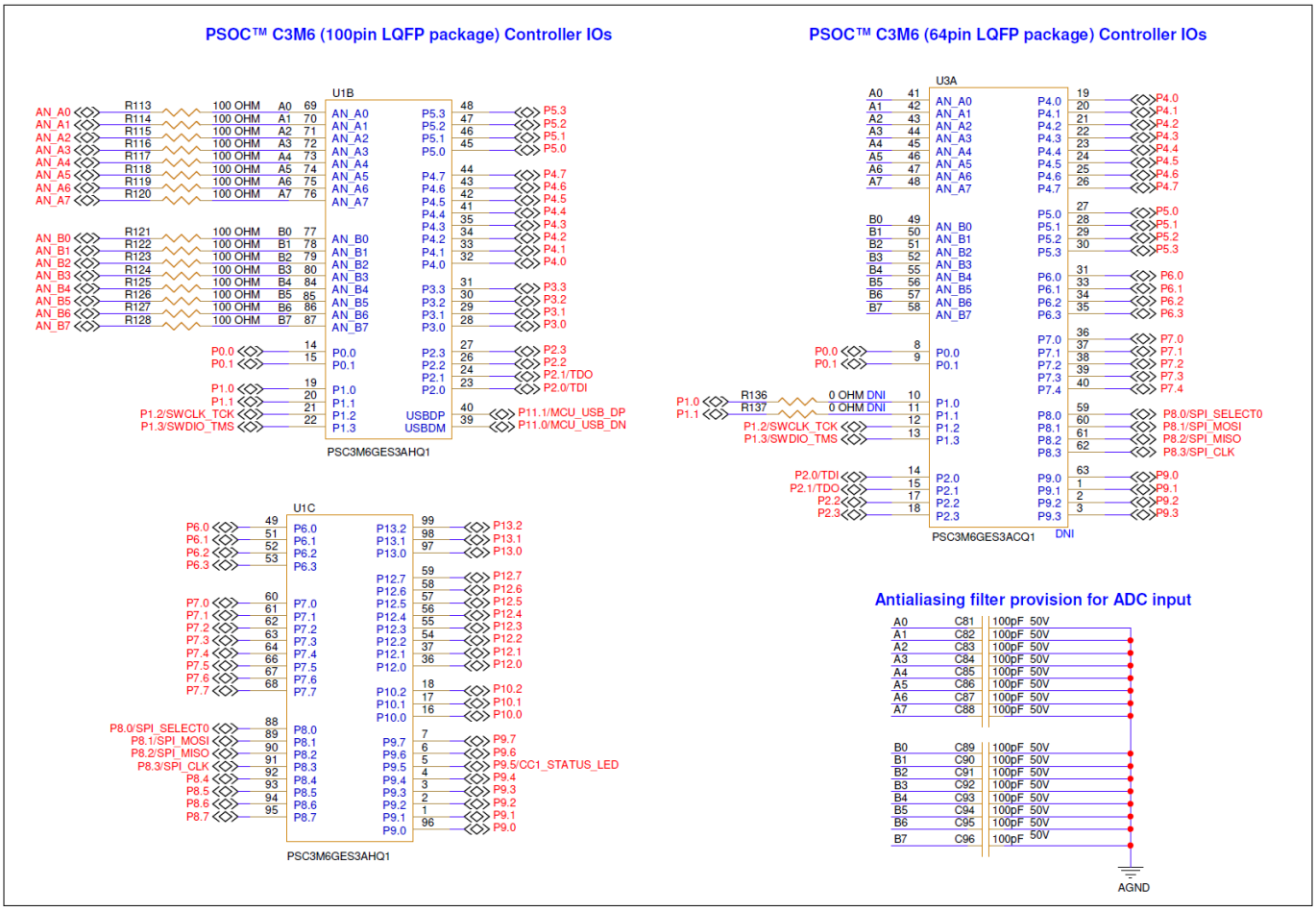



**Figure 31 Target MCU analog I/O connections**

## 3.1.3.5 Clock architecture

The PSOC™ Control C3 clock system provides clocks to all clock-dependent subsystems and switches between clock sources without glitches. The clock system also prevents metastable conditions.

In addition, a clock-supervision (CSV) circuit is implemented for each `clk_hf` domain. The CSV circuit detects a stopped clock or an abnormal frequency on the monitored clock.

The following clock sources are available:

- **Internal main oscillator (IMO)**: 8 MHz ±2%, fast wake-up, low jitter
- **Internal high-speed oscillator (IHO)**: 48 MHz ±1%
- **Internal low-speed oscillator (ILO)**: 32 kHz ±10%; also serves as a wake-up source for the RTC
- **External crystal oscillator (ECO)**: 4 MHz to 36 MHz
- **External watch-crystal oscillator (WCO)**: 32.768 kHz
- **External clock (EXTCLK)**: Maximum frequency of 80 MHz
- **One frequency-locked loop (FLL)1**: Output-frequency range of 24 MHz to 100 MHz
- **One digital phase-locked loop (DPLL#0)**: Output-frequency range of 25 MHz to 180 MHz

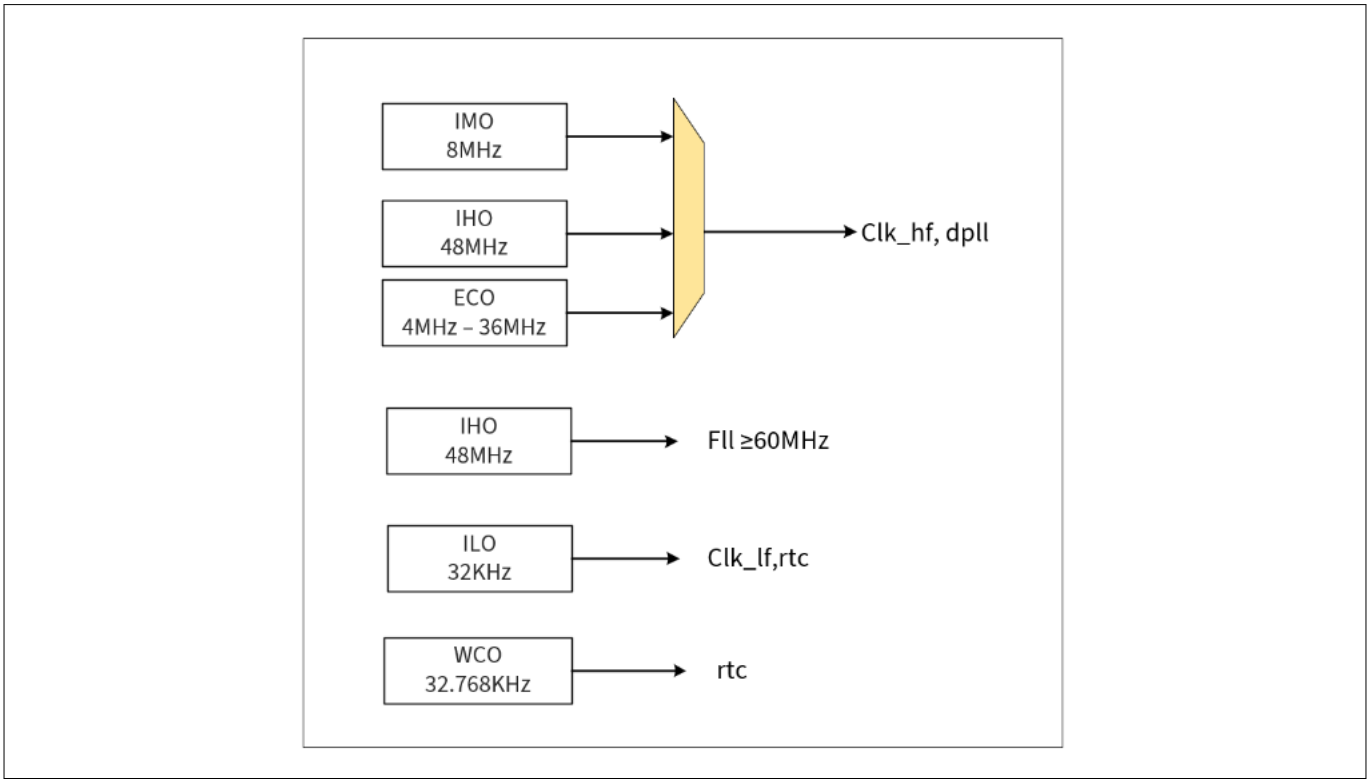



**Figure 32 PSC3M6 MCU clock architecture**

The target clock subsystem provides two primary clock sources: a low-frequency WCO path and a high-frequency ECO crystal path. DNI alternatives are available for edge-routed clock pins. In this design, the P0.0/P0.1 and P1.0/P1.1 pin pairs connect to the external crystals by default.

The WCO uses a 32.768 kHz crystal (Y2) with an 18 pF load capacitance. The ECO uses a 16 MHz crystal (Y3) with an 8 pF load capacitance. In addition to the external crystals, an alternative edge-routed clock source is available. This source becomes active only after the corresponding default resistor pair is removed and the alternate resistor pair is installed.

Rework for MCU clock documents the route-selection changes without calculating load capacitance or clock accuracy. The schematic and BOM identify the crystal, capacitor, and resistor values listed in the table, but they do not provide sufficient information to determine clock start-up time, frequency tolerance, or MCU internal clock-tree behavior.

**Table 17 Target clock configuration**

| Clock | Source | Capacitors/link | MCU pins | Default route | DNI edge route |
|---|---|---|---|---|---|
| WCO | Y2, 32.768 kHz | C47/C48 18 pF; R61 | P0.0/P0.1 | R85/R90 | R87/R92 |
| ECO | Y3, 16 MHz | C46/C49 8 pF; R62 | P1.0/P1.1 | R94/R97 | R96/R99 |

Figure 33 shows the WCO and ECO crystal networks side by side and traces their default fitted routes to the MCU pins.

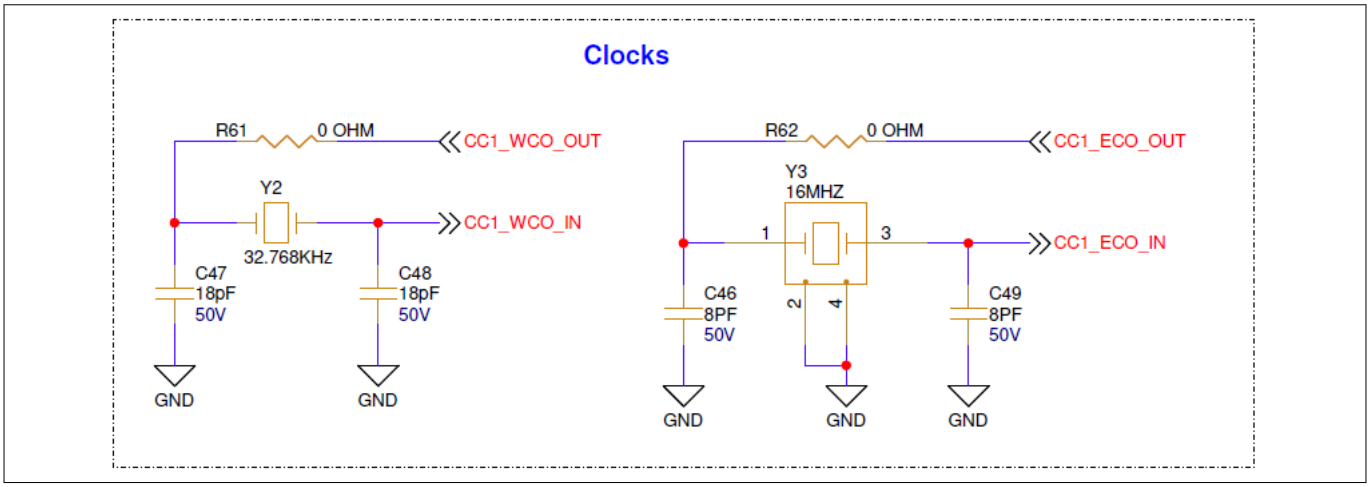



**Figure 33 Target WCO and ECO clock networks**

### 3.1.3.6 Interfaces

The target interface network exposes USB, debug, UART, I²C, CAN, GPIO, analog, and edge-connector signals through multiple endpoints. This section consolidates the endpoint overview introduced in Architecture through Interfaces.

J6 provides the target USB interface with TVS protection and 22 ohm MCU signal routes. J5 is the target SWD/JTAG header, and J7 is a DNI SWD/UART header. J4 carries I²C signals, but its pull-up resistors and local MCU routes are DNI in the documented population.

CAN signals reach the physical J3 interface through U11 and U5, crossing from the isolated region to the target region. J8 provides access to GPIO, analog, clock, power, USB, and debug signals. SPI and the remaining GPIO groups do not have dedicated onboard headers and are accessible only through J8.

These interfaces do not use a common protection scheme. USB includes local TVS protection and series resistors. Onboard CAN includes isolation, a transceiver, and bus protection. I²C does not include fitted local pull-up resistors, and J8 primarily provides direct signal access.

Connector pinouts are documented in Connectors and the interface-board topics to avoid implying identical electrical conditioning across all interfaces. CAN and isolated UART signals also cross the GND/GND_ISO boundary described in Isolated interfaces.

**Table 18 Target interface summary**

| Interface | Endpoint | Protection/ isolation | Default route/ population | Alternative |
|---|---|---|---|---|
| USB | J6 | D17; R107/R109 | Fitted to P11.1/ P11.0 | J8 links R108/R110 DNI |
| SWD/JTAG | J5 | U8/U9 for onboard path | J5 fitted; SW2 fitted | J7 DNI |
| UART | Isolated path | U10 | R101/R104 fitted | J8 R103/R106 DNI |
| I2C | J8 by default; J4 present | No fitted J4 pull-ups | R86/R89 fitted | R88/R91 and R57/R59 DNI |
| CAN | J3 through U5 | U11 isolation; line protection | R93/R98 fitted | J8 R95/R100 DNI |
| Edge I/O | J8 | Depends on signal path | 120-pin electrical map | Mechanical naming unresolved |

Figure 34, Figure 35, and Figure 36 shows the USB, debug, I²C, CAN, UART, and edge-connector interfaces and traces the signal paths to the points where isolation, protection, or DNI routing is applied.

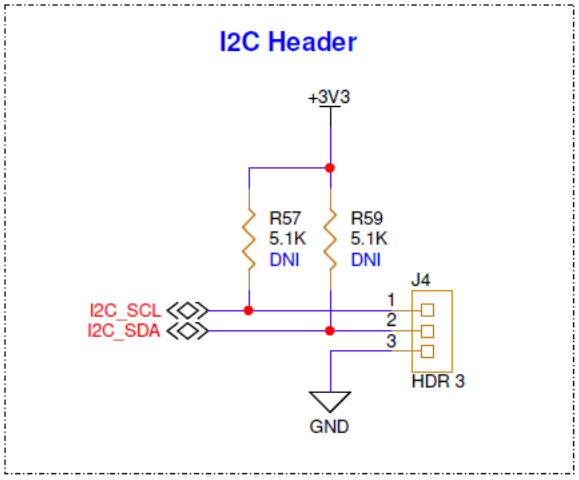



**Figure 34 Target MCU - I²C header**

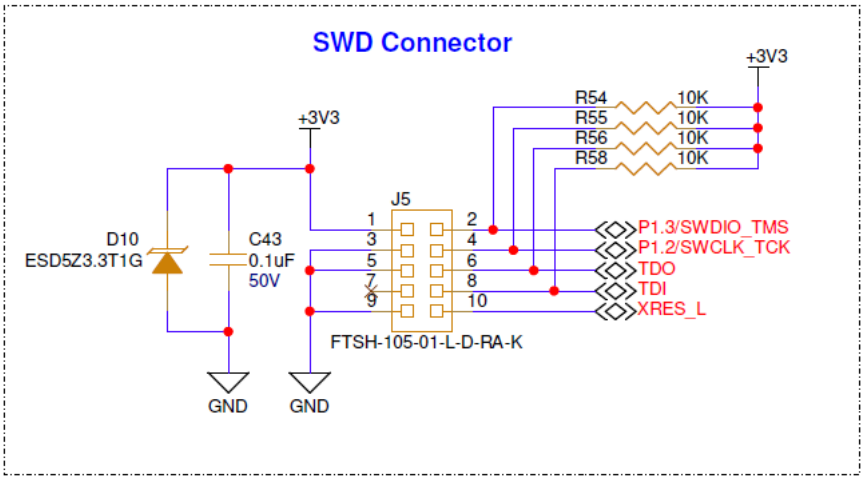



**Figure 35** **Target MCU - SWD header**

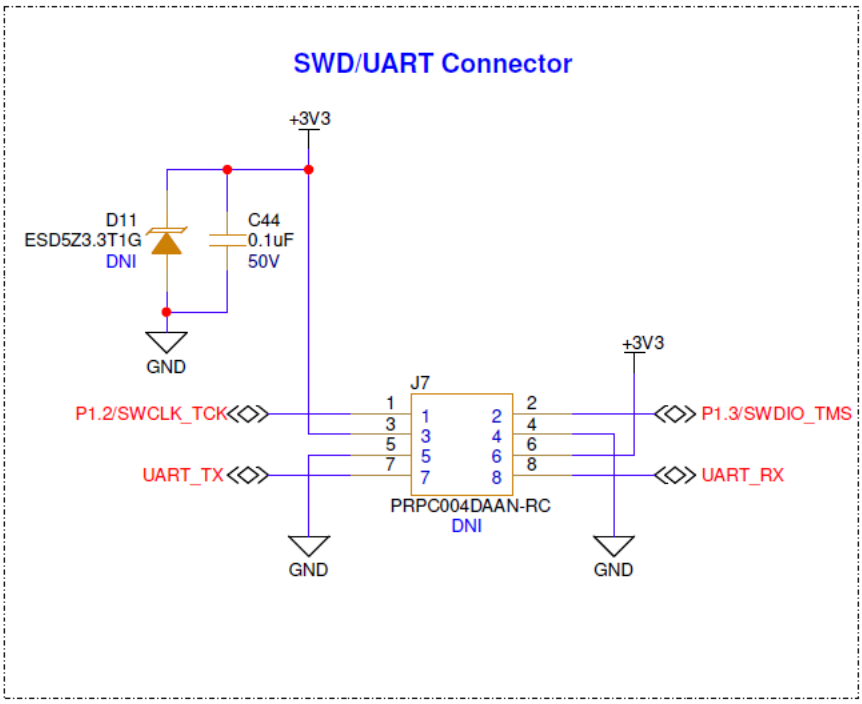



**Figure 36** **Target MCU - SWD/UART header**

## 3.1.4 CAN subsystem

The CAN subsystem converts target-side CAN logic into an isolated physical CAN interface at J3 while maintaining separation between the target GND domain and the CAN bus-side GND_ISO domain.

CAN_TX and CAN_RX signals pass between the PSC3M6 MCU and the digital isolator across the isolation boundary. On the isolated side, the CAN transceiver converts the logic-level signals to CAN_H and CAN_L.

Diodes D13 and D14 provide line protection, while R111 and R112 (60.4 Ω each) together with C80 (4700 pF) form the termination network ahead of the CAN header (J3). Pin 2 of J3 is connected to GND_ISO.

The transmit path starts at the MCU and passes through the logic routing, digital isolator (U11), and CAN transceiver (U5) before reaching the terminated CAN interface at J3. The receive path follows the same route in the opposite direction, from J3 back to the MCU

**Table 19 CAN signal path**

| Stage | Signals | Implementation | Domain | Population |
|---|---|---|---|---|
| MCU logic | CAN_TX/CAN_RX | U1 through R98/R93 | Target GND | Fitted |
| Isolation | CAN logic pair | U11 ISO6721BQDRQ1 | GND to GND_ISO | Fitted |
| Transceiver | Logic to CAN_H/ CAN_L | U5 TLE9351BVSJXTMA1 | GND_ISO | Fitted |
| Protection/network | CAN_H/CAN_L | D13/D14; R111/ R112; C80 | GND_ISO | Fitted |
| Connector | CAN_L, GND_ISO, CAN_H | J3 pins 1, 2, 3 | GND_ISO | Fitted |

Figure 37 and Figure 38 shows the CAN signal connections.

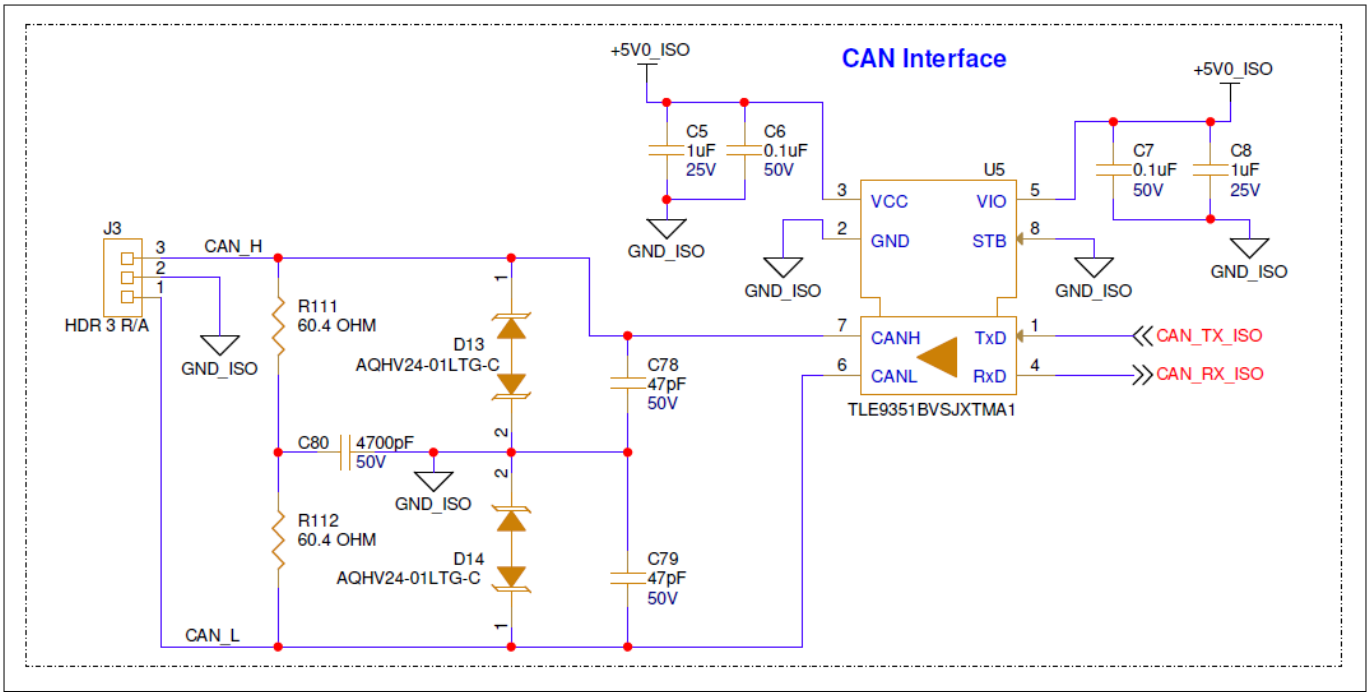



**Figure 37 CAN transceiver connection**

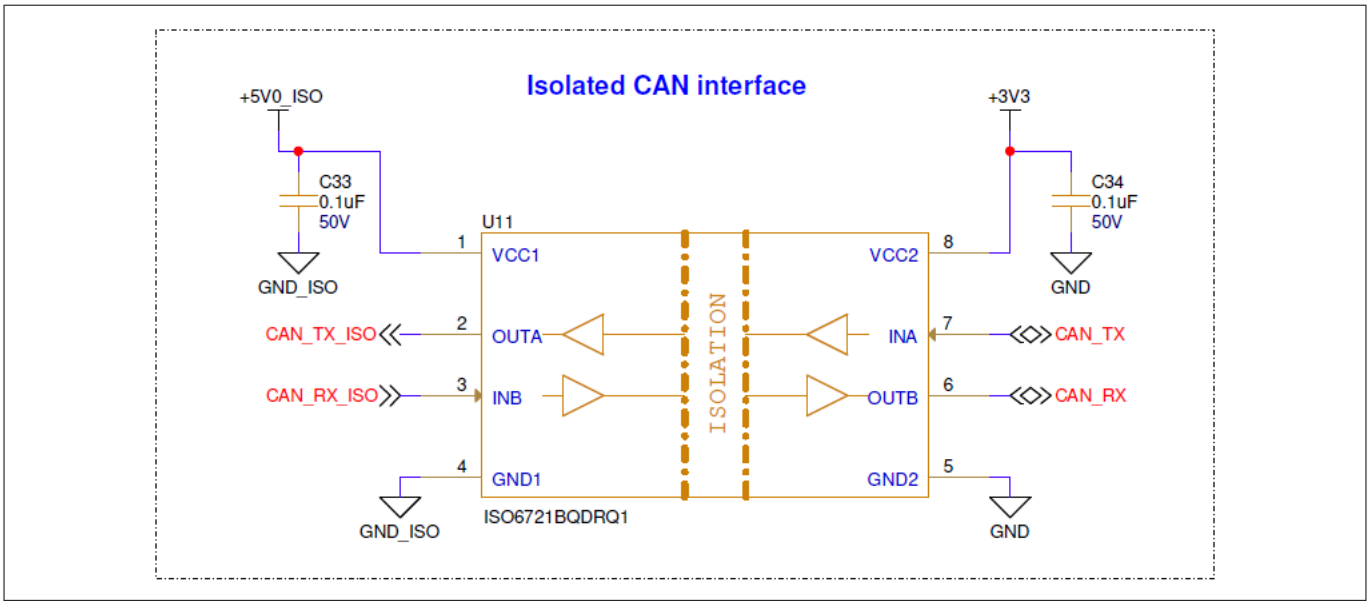



**Figure 38 Isolated CAN interface**

## 3.1.5 Isolated interfaces

The control card features an onboard XMC4200-based J-Link debugger. All interface signals between the XMC4200 and the PSC3M6 device are isolated using digital isolators that provide up to 2.5 kVrms capacitive isolation.

The isolation subsystem uses four digital isolators that transfer SWD, UART, CAN, and reset signals between `GND_ISO` and the target GND, while preserving the schematic domain boundary.

U8 is the fitted SWD isolator, and U9 provides target-side steering and buffering. U10 transfers UART signals, U11 transfers CAN signals, and U12 and U13 transfer and buffer reset signals. Programmer-side channels reference `GND_ISO`, while target-side channels reference GND.

Each channel listed in the table below uses a dedicated isolator device. Therefore, the four functions are not multiplexed through a shared isolation path.

The isolators are fitted in the documented assembly. Therefore, the default onboard programmer and control paths use these isolators without requiring resistor rework. Alternate edge routing for UART and CAN can bypass the onboard isolated destination through the MCU routing matrix, but this does not remove the isolator components.

**Table 20 Isolation-channel summary**

| Function | Isolator | Target buffer | Programmer/ isolated side | Target destination | Signals | Population/BOM description |
|---|---|---|---|---|---|---|
| SWD | U8 SI8641BB-B-IS1R | U9 | XMC4200/GND_ISO | SWD routing/GND | SWCLK/TCK, SWDIO/TMS | Fitted; 2.5 kVrms component description |
| UART | U10 ISO6721BQDRQ1 | None shown | XMC4200/GND_ISO | UART routing/GND | UART_TX, UART_RX | Fitted; 3 kVrms component description |

**(table continues...)**

**Table 20 (continued) Isolation-channel summary**

| Function | Isolator | Target buffer | Programmer/ isolated side | Target destination | Signals | Population/BOM description |
|---|---|---|---|---|---|---|
| CAN | U11 ISO6721BQDRQ1 | None shown | U5/GND_ISO | MCU CAN logic/GND | CAN_TX, CAN_RX | Fitted; 3 kVrms component description |
| Reset | U12 ISO6721BQDRQ1 | U13 | XMC4200/GND_ISO | XRES_L/GND | XRES_L | Fitted; 3 kVrms component description |

***Note**: When the debugger section is removed, the control card no longer provides signal or power isolation.*

Figure 39 and Figure 40 shows each channel crossing the isolation boundary and identifies the points where additional target-side buffering is provided by U9 or U13.

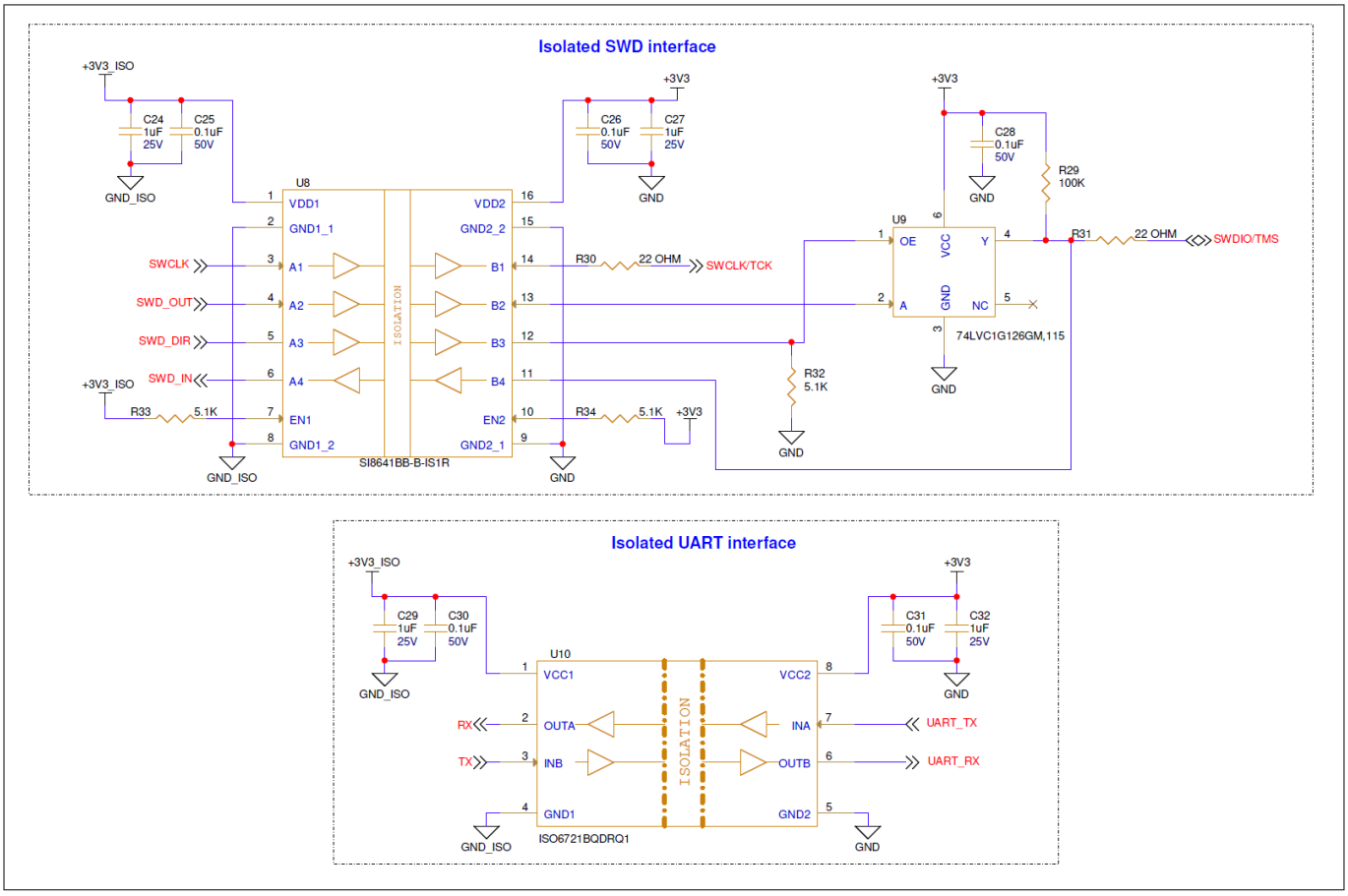



**Figure 39 SWD and UART isolation channels**

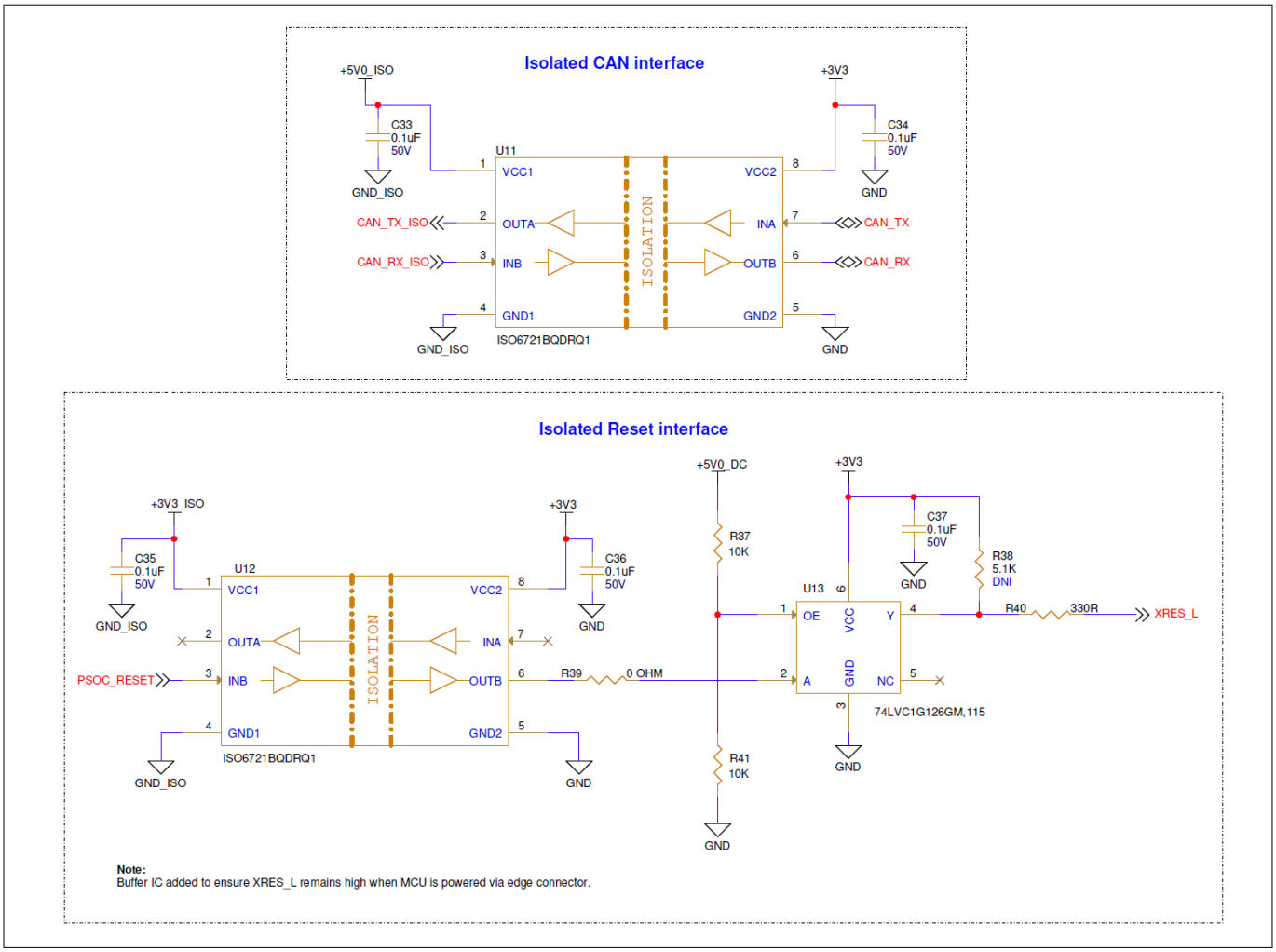



**Figure 40 CAN and reset isolation channels**

## 3.1.6 User LED

The user LED provides a target-domain visual indicator connected to the MCU status-LED signal, giving the board a single fitted indicator that is separate from the programmer-side LEDs.

The fitted green LED D8 and resistor R63 (270 Ω) form a series path from +3V3 to P9.5/CC1_STATUS_LED. The GPIO-controlled pin therefore completes or interrupts the LED current path according to its electrical state. Because D8 is controlled by a GPIO signal, the PSC3M6 MCU can configure the LED state

***Note**: The E-LQFP-64 package does not support pin P9.5. Therefore, user-LED functionality is available only on the E-LQFP-100 package of the PSC3M6 MCU.*

**Table 21 User LED connection**

| Reference | Color | Supply | Series element | MCU net | Population |
|---|---|---|---|---|---|
| D8 | Green | +3V3 | R63, 270 Ω | P9.5/ CC1_STATUS_LED | Fitted |

Figure 41 shows the user LED connection.

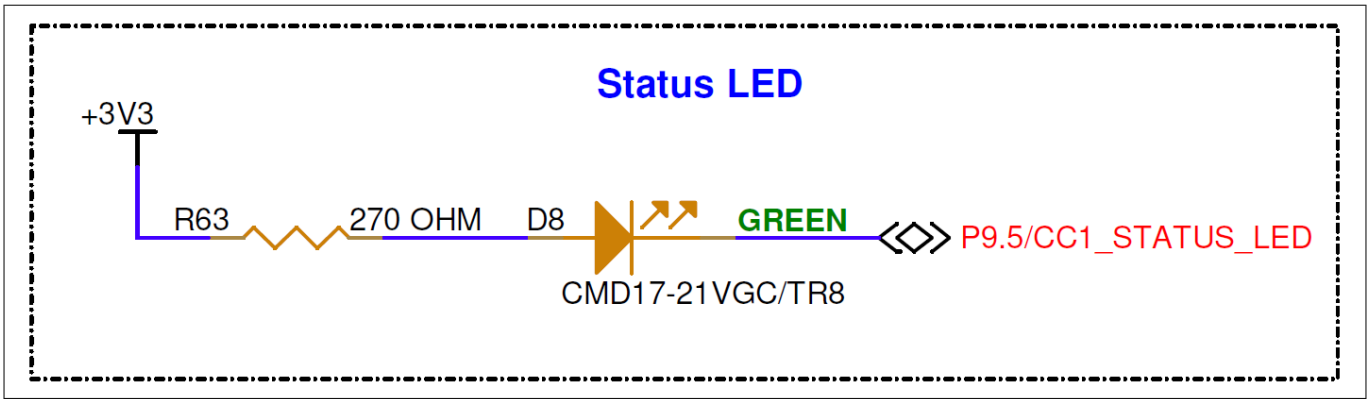



**Figure 41** **User LED connection**

### 3.1.7 Reset button

The reset circuit provides local hardware control that asserts the target XRES_L net, giving the board a manual reset path independent of the isolated reset channel described in Isolated interfaces.

In the default released state, R60 pulls XRES_L high toward +3V3, and C45 connects the net to GND. Pressing the normally open reset button (SW1) connects XRES_L directly to GND, generating a reset signal for the MCU.

Releasing SW1 removes the direct connection to GND, and the pull network restores the default high state.

To ensure that the reset line remains high by default when the isolation section is removed through the breakaway tabs and the MCU is powered from the 120-pin edge connector, the design includes a tri-state buffer circuit. The buffer circuit senses the removal of the isolated region through its enable pin and maintains the reset line in the default high state.

***Note**: The reset line must remain high by default because XRES_L is an active-low signal.*

**Table 22** **Reset signal states**

| Condition | SW1 | R60 | C45 | XRES_L result |
|---|---|---|---|---|
| Not pressed | Open | 5.1 kΩ pull-up to +3V3 | 0.1 uF to GND | Not directly grounded, default high state |
| Pressed | Closed to GND | Remains fitted | Remains fitted | Asserted low, Reset state |

shows the XRES_L signal path, including the pull-up resistor R60, capacitor C45, and the ground connection established when SW1 is pressed.

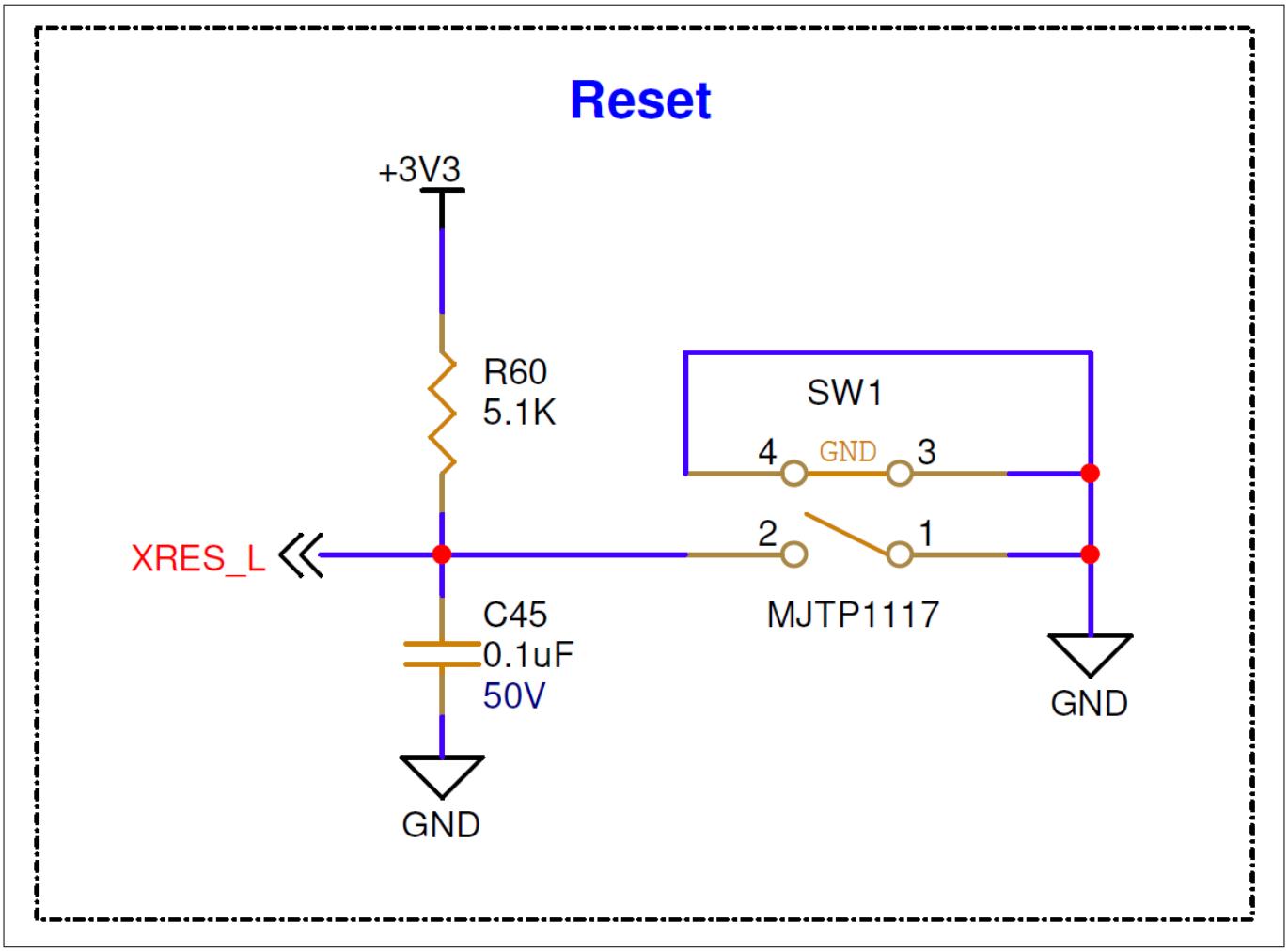



**Figure 42 Target reset connection**

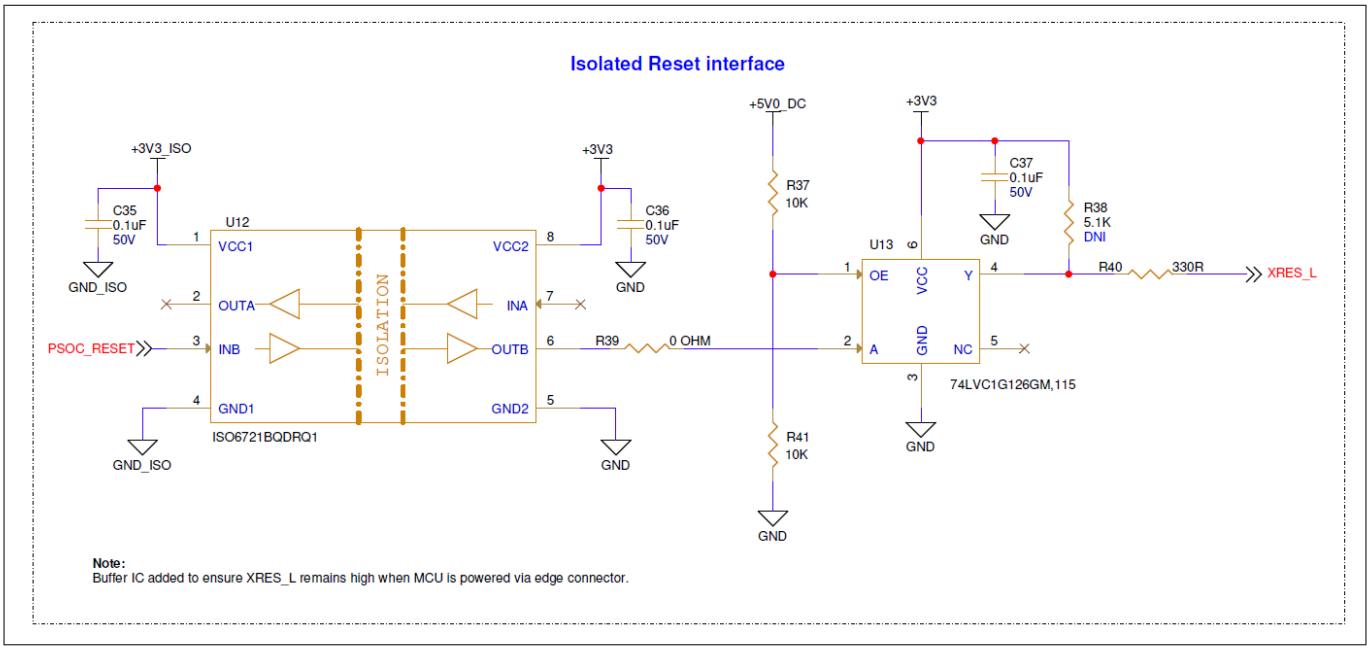



**Figure 43 Target reset buffer connection**

### 3.1.8 Connectors

The control-card connectors provide USB power and data, CAN, I²C, target debug, optional debug/UART, and the complete board-edge interface.

J1 and J6 are USB Type-C receptacles in the isolated and target domains, respectively. J3, J4, and J5 are CAN, I²C, and target-debug headers. J2 and J7 are DNI optional headers. J8 is the 120-contact edge interface. Each table below is preceded by the relevant domain, population, conditioning, and routing information.

**CAN header**: J3 is a three-pin, isolated-domain CAN header. U11 and U5 provide isolation and CAN transceiver conversion. D13, D14, and the split-termination network condition the bus-side path. The default routing reaches J3 through fitted MCU-to-isolator links.

**Table 23 Control J3 - Isolated CAN**

| Pin | Signal |
|---|---|
| 1 | CAN_L |
| 2 | GND_ISO |
| 3 | CAN_H |

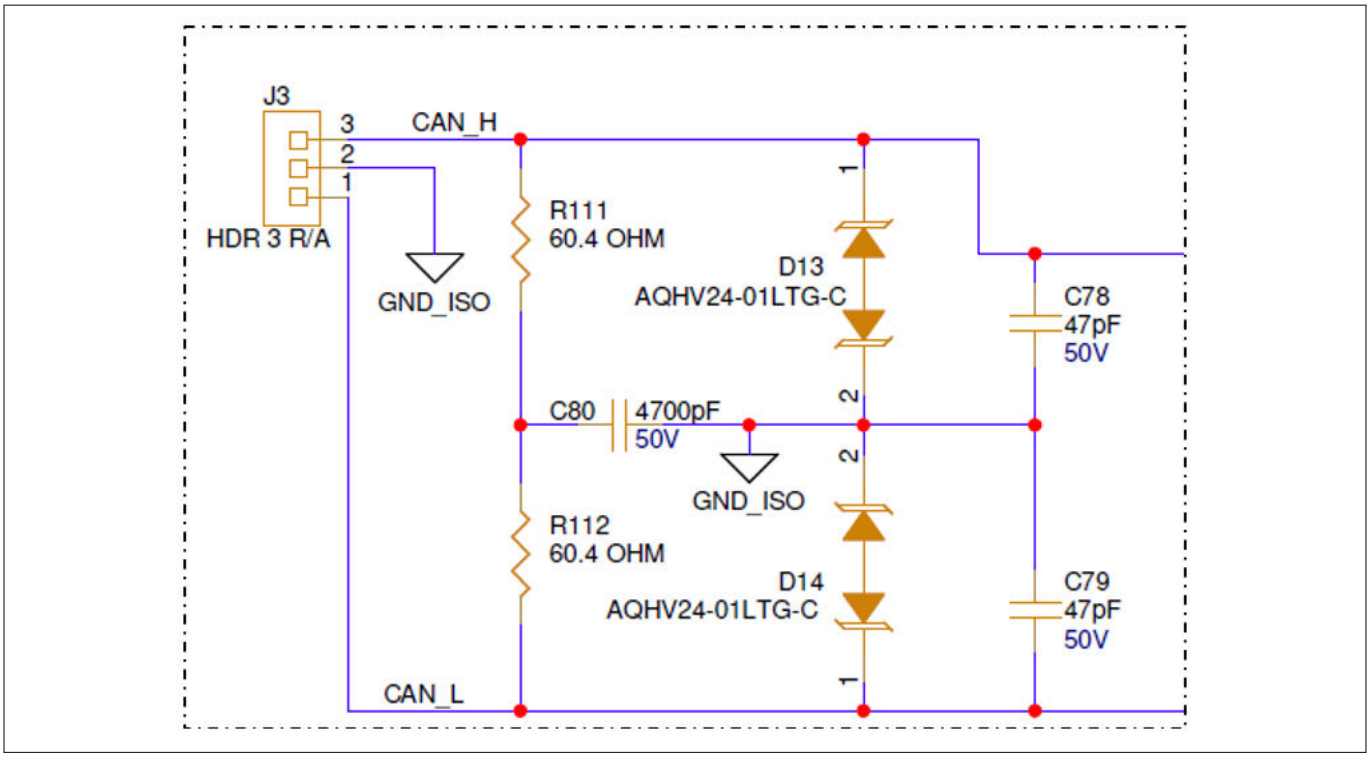



**Figure 44 CAN header**

**I2C header**: J4 is a three-pin target-domain I²C header. It does not provide isolation or level translation. Pull-up resistors R57 and R59, along with local MCU routing links R88 and R91, are DNI. Therefore, in the documented population, J4 is not directly connected to the MCU I²C pins.

**Table 24 Control J4 - I²C header**

| Pin | Signal |
|---|---|
| 1 | I2C_SCL |
| 2 | I2C_SDA |
| 3 | GND |

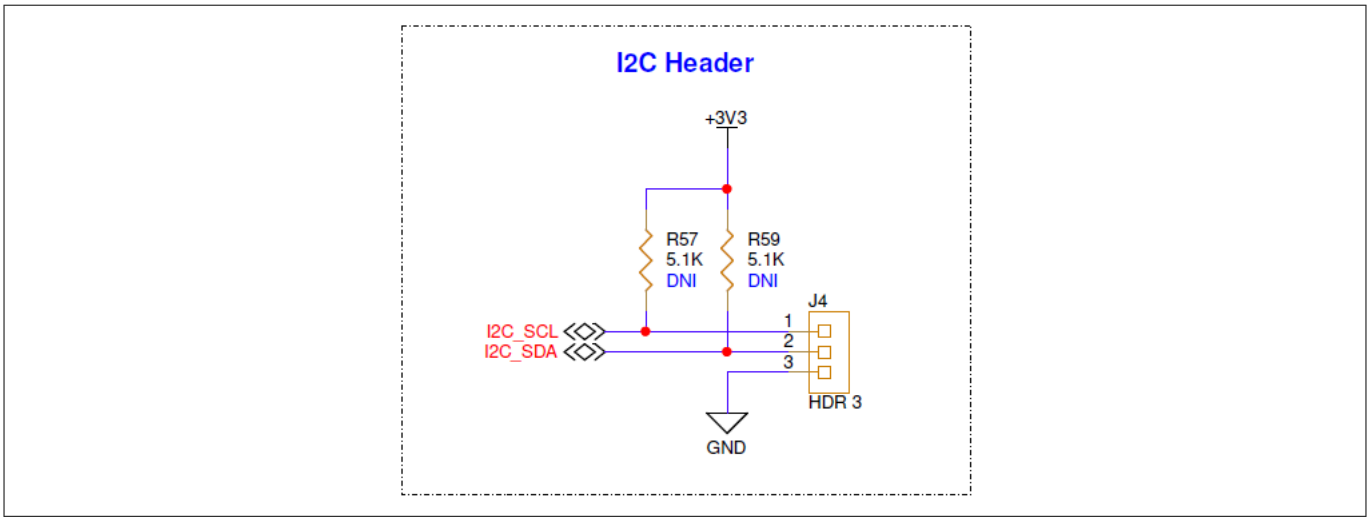



**Figure 45 I²C header**

**SWD header**: J5 is a 10-pin target-domain debug header referenced to +3V3 and GND. It exposes SWD/JTAG signals and XRES_L without providing connector-specific protection. SW2 and the associated routing determine how the header interacts with the onboard isolated programmer.

**Table 25 Control J5 - Target SWD/JTAG**

| Pin | Signal |
|---|---|
| 1 | +3V3 |
| 2 | P1.3/SWDIO_TMS |
| 3 | GND |
| 4 | P1.2/SWCLK_TCK |
| 5 | GND |
| 6 | P2.1/TDO |
| 7 | NC |
| 8 | P2.0/TDI |
| 9 | GND |
| 10 | XRES_L |

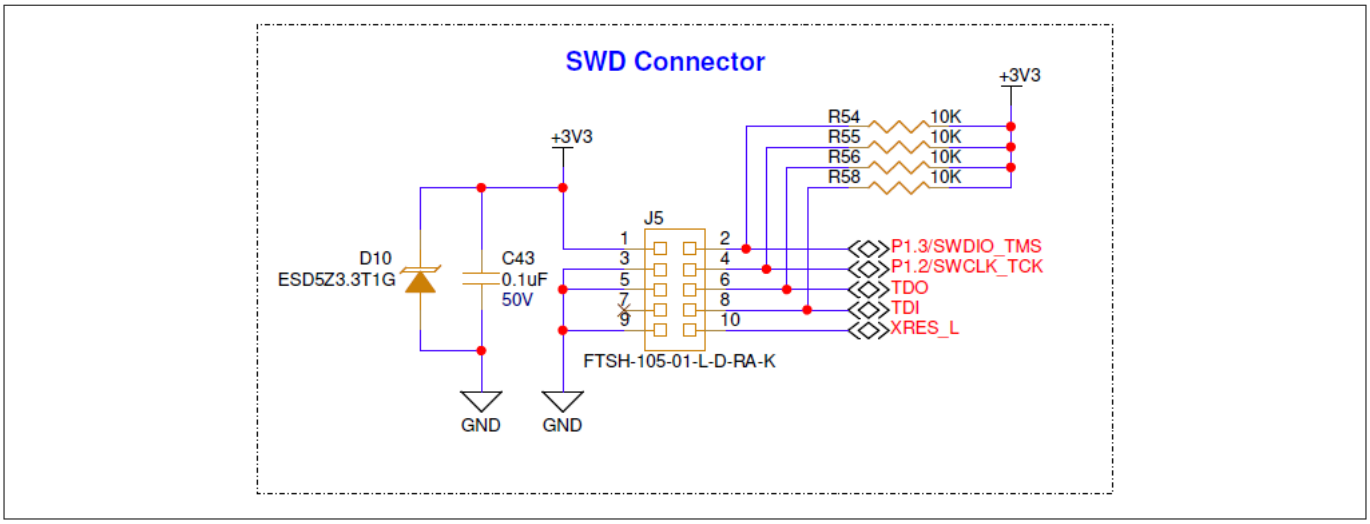



**Figure 46 SWD header**

**SWD/UART header**: J7 is a DNI eight-pin target-domain SWD/UART header. Its signals are referenced to +3V3 and GND and are not isolated at the header. Because the connector is not fitted, these signals are unavailable in the released BOM unless the assembly is modified.

**Table 26 Control J7 - Optional SWD/UART (DNI)**

| Pin | Signal |
|---|---|
| 1 | P1.2/SWCLK_TCK |
| 2 | P1.3/SWDIO_TMS |
| 3 | +3V3 |
| 4 | GND |
| 5 | GND |
| 6 | +3V3 |
| 7 | UART_TX |
| 8 | UART_RX |

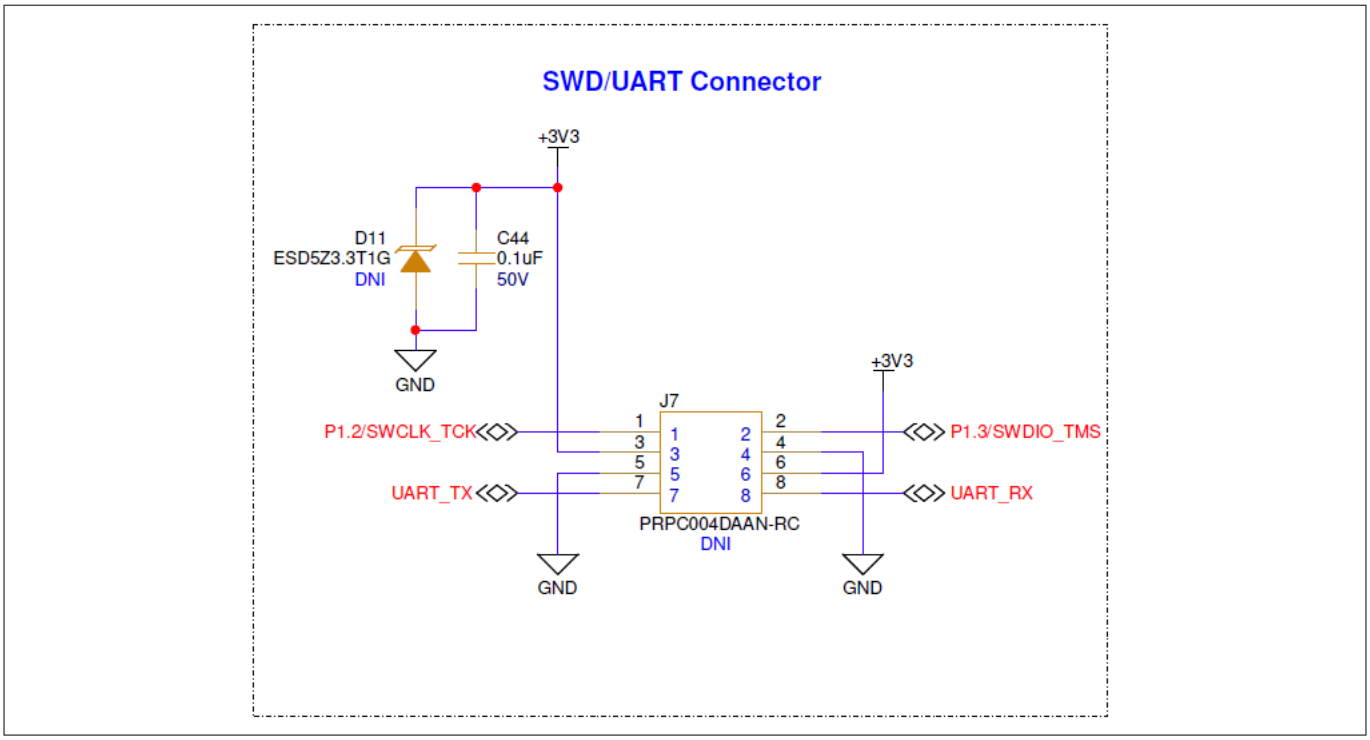



**Figure 47 SWD/UART header**

**120-pin edge connector**: J8 is the control card's 120-contact edge interface and carries power, ground, GPIO, analog, clock, USB, debug, reference, and backup nets. This connector mates with the HTEC8-160-01-L-DV-A-BL connector on the interface board. All I/O signals of the PSC3M6 device are exposed through this 120-pin edge connector.

**Table 27 Control-card J8 120-pin edge mapping**

| Odd pin | Signal | Even pin | Signal |
|---|---|---|---|
| 1 | +3V3 | 2 | XRES_L |
| 3 | P3.0 | 4 | P9.1 |
| 5 | P4.4 | 6 | P3.1 |
| 7 | P4.5 | 8 | P9.3 |
| 9 | GND | 10 | VIN_CON |
| 11 | P4.6 | 12 | P12.0 |
| 13 | P4.7 | 14 | P9.0 |
| 15 | P7.0/I2C_SCL | 16 | P12.1 |
| 17 | P7.1/I2C_SDA | 18 | P12.2 |
| 19 | P7.2 | 20 | P12.3 |
| 21 | P7.3 | 22 | P5.1 |
| 23 | GND | 24 | VIN_CON |
| 25 | P4.0 | 26 | P12.4 |
| 27 | P4.1 | 28 | P0.0/CC1_WCO_OUT |

**(table continues...)**

**Table 27 (continued) Control-card J8 120-pin edge mapping**

| Odd pin | Signal | Even pin | Signal |
|---|---|---|---|
| 29 | P4.2 | 30 | P0.1/CC1_WCO_IN |
| 31 | P4.3 | 32 | P1.0/CC1_ECO_IN |
| 33 | P6.0 | 34 | P1.1/CC1_ECO_OUT |
| 35 | P6.1 | 36 | P12.5 |
| 37 | GND | 38 | VIN_CON |
| 39 | P9.4 | 40 | P12.6 |
| 41 | P9.2 | 42 | P2.2 |
| 43 | P10.0 | 44 | P2.3 |
| 45 | P10.1 | 46 | P12.7 |
| 47 | P10.2 | 48 | P9.6 |
| 49 | P6.2/CAN_RX | 50 | P3.2 |
| 51 | P6.3/CAN_TX | 52 | P3.3 |
| 53 | P9.5/CC1_STATUS_LED | 54 | P5.2/UART_RX |
| 55 | GND | 56 | P5.3/UART_TX |
| 57 | P8.0/SPI_SELECT0 | 58 | P5.0 |
| 59 | P8.1/SPI_MOSI | 60 | P13.0 |
| 61 | P8.2/SPI_MISO | 62 | P13.1 |
| 63 | P8.3/SPI_CLK | 64 | P13.2 |
| 65 | AN_A0 | 66 | VDDA_C |
| 67 | AN_A1 | 68 | AN_A7 |
| 69 | AN_A5 | 70 | AN_A6 |
| 71 | AN_A3 | 72 | AN_B4 |
| 73 | AGND | 74 | AGND |
| 75 | AN_A4 | 76 | AN_B5 |
| 77 | VAREF_EXT_C | 78 | AN_B2 |
| 79 | AN_A2 | 80 | AN_B3 |
| 81 | AN_B0 | 82 | AN_B6 |
| 83 | AN_B1 | 84 | AN_B7 |
| 85 | NC | 86 | NC |
| 87 | AGND | 88 | AGND |
| 89 | NC | 90 | P8.4 |
| 91 | NC | 92 | P8.5 |
| 93 | NC | 94 | NC |

**(table continues...)**

**Table 27 (continued) Control-card J8 120-pin edge mapping**

| Odd pin | Signal | Even pin | Signal |
|---|---|---|---|
| 95 | P7.7 | 96 | NC |
| 97 | P7.6 | 98 | NC |
| 99 | P7.5 | 100 | P8.6 |
| 101 | P7.4 | 102 | NC |
| 103 | NC | 104 | P8.7 |
| 105 | NC | 106 | NC |
| 107 | NC | 108 | P11.1/USB_DP |
| 109 | NC | 110 | P11.0/USB_DN |
| 111 | P9.7 | 112 | GND |
| 113 | GND | 114 | P2.0/TDI |
| 115 | P1.2/SWCLK_TCK | 116 | P2.1/TDO |
| 117 | P1.3/SWDIO_TMS | 118 | VBACKUP_C |
| 119 | +3V3 | 120 | +3V3 |

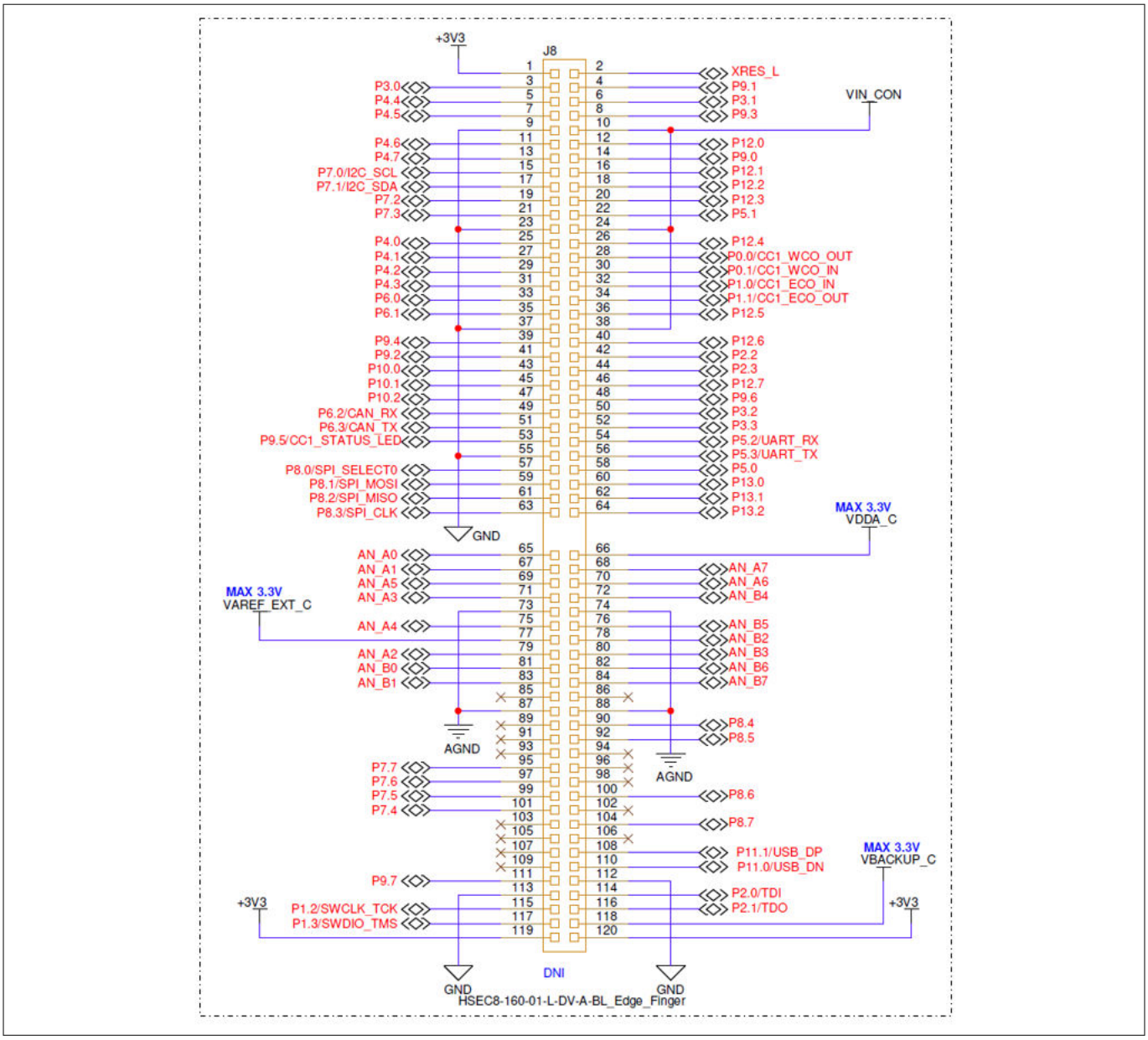



**Figure 48 120-pin edge connector**

## 3.1.9 Removal of onboard programmer

The programmer-routing hardware determines how target SWD signals reach the MCU and provides a fitted external-debug header. It does not implement a physical break-off or programmer-removal mechanism. The routing options described in this section interact with the isolation channels and debug connectors.

SWD switch SW2 routes `SWCLK/TCK` and `SWDIO/TMS` between the onboard isolated path and the target-side routing associated with SWD header J5.

SWD header J5 is fitted and provides +3V3, GND, SWD/JTAG signals, and `XRES_L`. SWD/UART header J7 is DNI and provides SWD/UART access only when assembled.

Using J5 changes the debugger attachment point but does not, by itself, disconnect power from the onboard programmer, programmer power supply, DC-DC isolator, or isolated-domain circuitry.

***Warning:*** ***External debug equipment can alter the isolation and grounding arrangement. Review the ground connection before attaching external debug equipment.***

**Table 28 Programmer and external-debug routing**

| Element/path | Population | Domain | Verified role | User consequence |
|---|---|---|---|---|
| SW2 | Fitted | Target signal routing | Steers SWCLK/TCK and SWDIO/TMS | Position names/ default not documented |
| Onboard SWD path | Fitted isolator path | GND_ISO to GND | Connects XMC4200 path to target routing | Uses board isolation circuitry |
| J5 | Fitted | Target +3V3/GND | 10-pin SWD/JTAG and reset access | External debugger endpoint |
| J7 | DNI | Target +3V3/GND | Optional SWD/UART access | Unavailable unless assembled |
| Physical removal of isolated region | Breakaway tabs | Isolated domain | Physical breakaway tab assembly | Once broken, permanently disconnect |

Figure 49 shows the switch positions used to select either the onboard debugger or an external programmer.

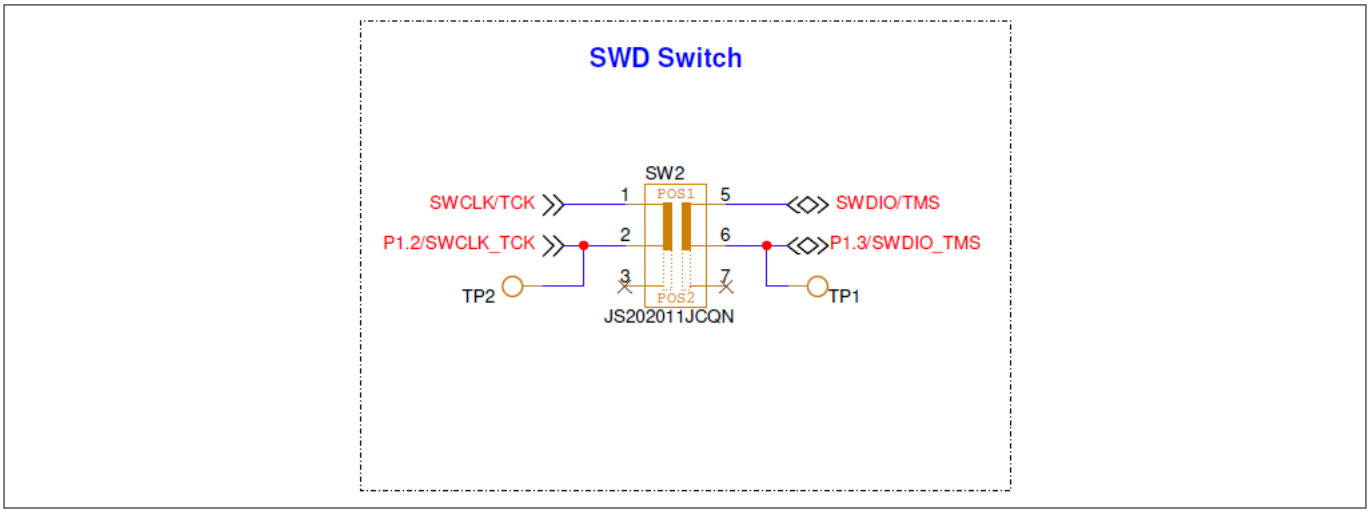



**Figure 49 SWD routing switch**

Figure 50 shows the breakaway tabs used to physically remove the isolated region.

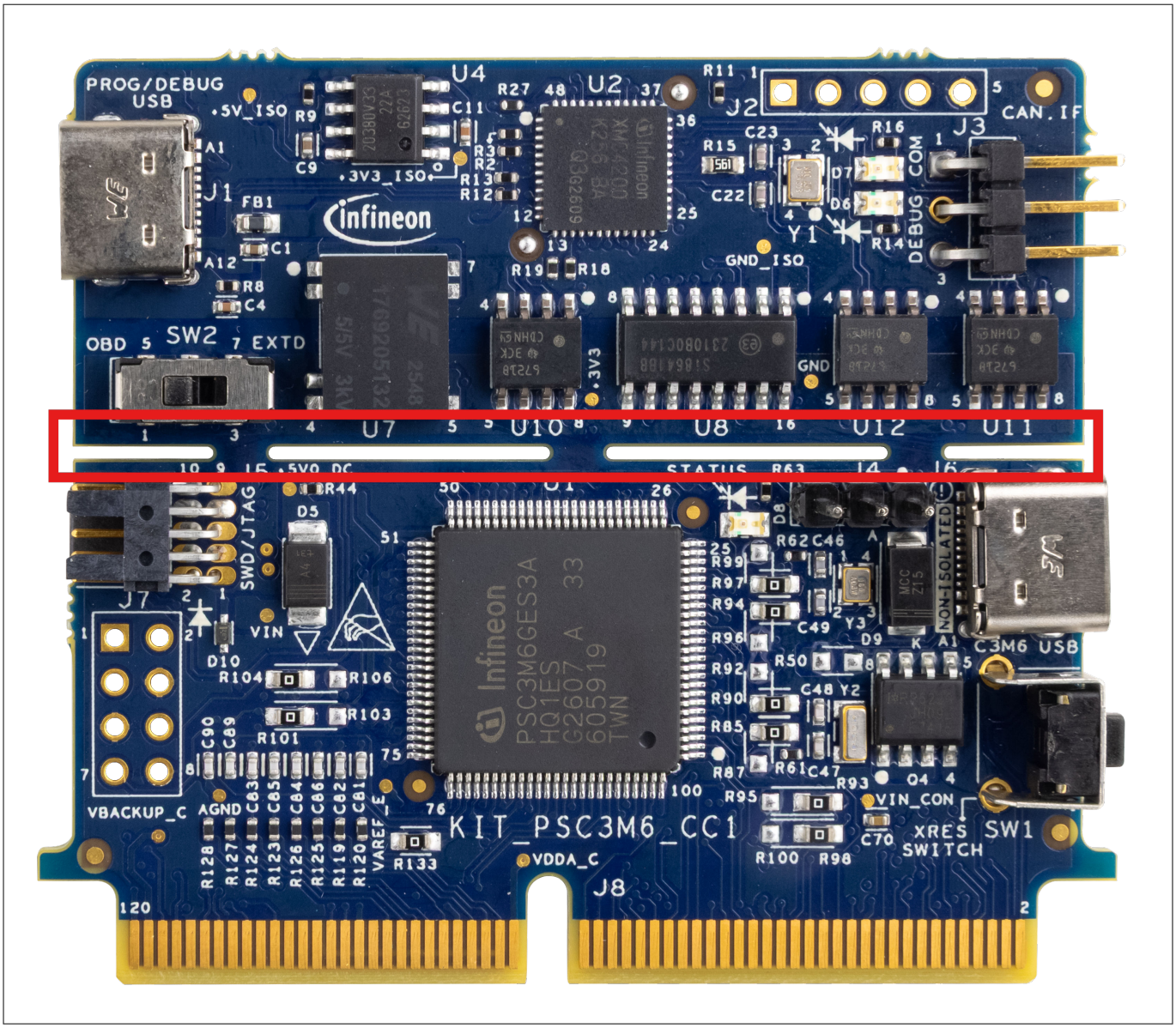



**Figure 50** **Breakaway tabs**

## 3.2 Interface board

The interface board is a passive fan-out card that connects to the control card through J1 and distributes the resulting control-card nets to the accessible digital and analog headers J2-J7. It provides only limited decoupling, two fixed-voltage straps, and a single ground link between the AGND and GND_SIGNAL domains. It does not introduce any additional circuit functionality.

It mainly comprises the following components:

- 120-pin edge connector (HTEC8-160-01-L-DV-A-BL)
- Four 2.54 mm, 18-pin (9 × 2) headers
- Two 2.54 mm, 16-pin (8 × 2) headers

Signals enter the board through the fitted J1 connector and fan out directly to the fitted J2-J7 connectors without modification. Populated C3 and C4 provide local decoupling at the connector. DNI components C1, C2, C5, and C6 are unpopulated alternate footprints for the same function. R1 is a 0 Ω link that joins the AGND and GND_SIGNAL domains, while fitted R2 and R3 establish the two fixed strap levels available on J5.

Because no active interface device is populated on this board, it provides no regulation, level translation, transceiver, USB protection, or isolation functions. Every net is a direct pass-through from J1.

Table 29 groups these elements into the board's functional blocks and lists the implementation, population status, and effect of each block.

**Table 29 Interface-board functional blocks**

| Block | Implementation | Population | Effect |
|---|---|---|---|
| Board-to-board input | J1, 120-position | Fitted | Receives all control-card nets |
| Digital fan-out | J2-J5 | Fitted | Direct digital/power routing |
| Analog fan-out | J6-J7 | Fitted | Direct analog/GPIO/ ground routing |
| Ground link | R1, 0 Ω | Fitted | Joins AGND and GND_SIGNAL |
| Fixed straps | R2 pull-up; R3 pull-down | Fitted | Sets J5.2 high and J5.4 low |
| Optional decoupling | C1/C2/C5/C6 | DNI | No effect in released population |

Figure 51 shows the interface board's passive fan-out architecture, tracing the direct signal routes from J1 to J2 through J7 and identifying the locations of the decoupling, ground-link, and strap components.

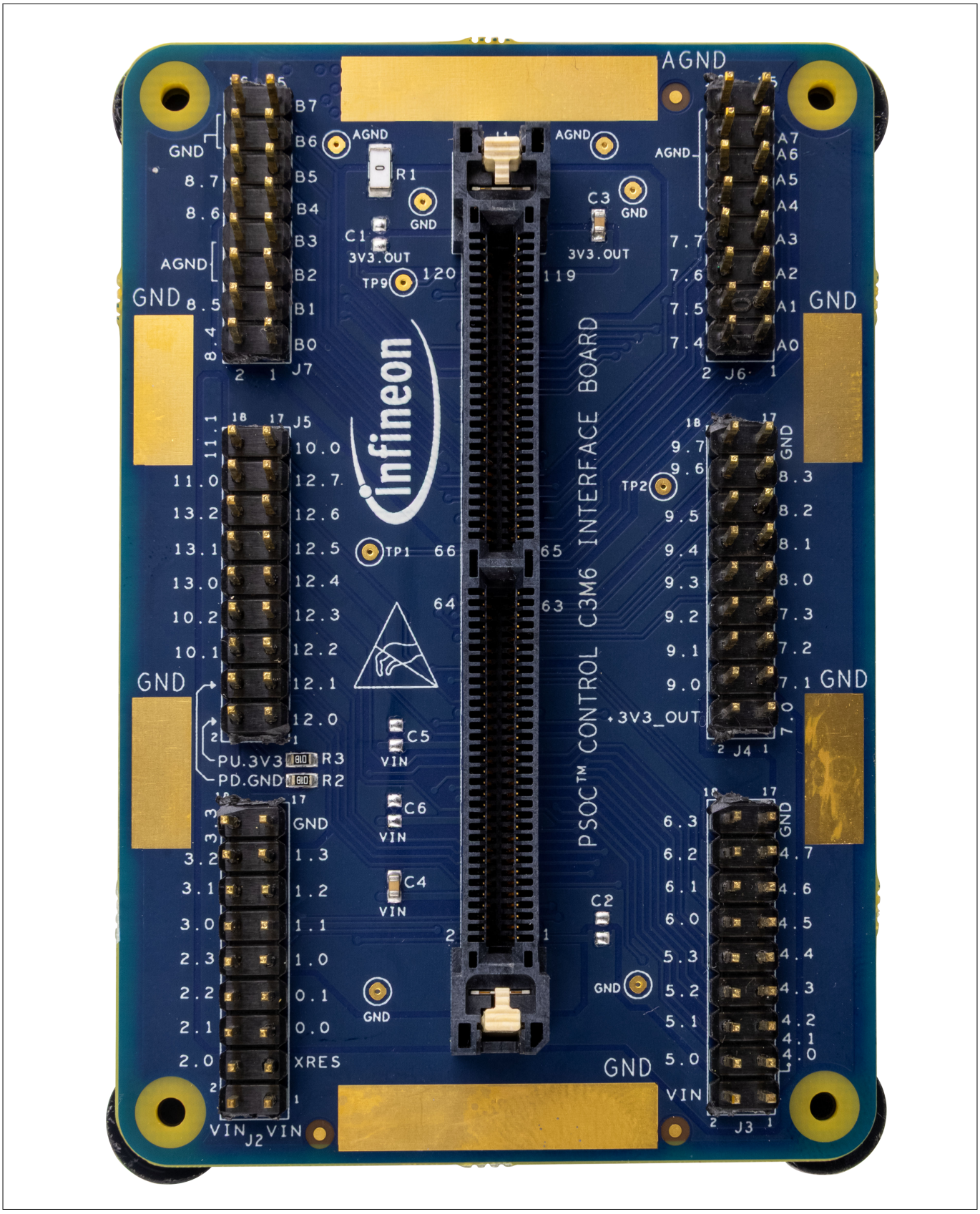



**Figure 51** **Interface-board architecture**

### 3.2.1 120-pin interface connector

Interface-board J1 is the single board-to-board connector that carries all signal, power, ground, debug, clock, USB, and analog connections between the interface board and the control card.

J1 is a 120-position, 0.8 mm female connector. It routes the +3V3_OUT and VIN power rails, the GND_SIGNAL and AGND return paths, and the GPIO, analog, USB, debug, clock, reference, and backup nets to J2-J7 or to the test pads. Shield contacts SH1 and SH2 connect to GND_SIGNAL.

Note that each NC pin listed in the pin mapping is individually unused. Do not treat these pins as a common signal or connect them together.

J1 is fitted and serves as the sole mechanical and electrical connection between the passive interface board and the control-card edge interface. It carries both power domains used on the interface board, the direct signal fan-out, and the shield contacts connected to GND_SIGNAL. It provides no isolation, level translation, or protection functions, and the NC contacts remain individually unused.

Table 30 lists the complete J1 pin mapping, pairing each odd-numbered pin with its corresponding even-numbered pin and associated function.

**Table 30 Interface-board J1 120-pin mapping**

| Odd pin | Function | Even pin | Function |
|---|---|---|---|
| 1 | +3V3_OUT | 2 | XRES_L |
| 3 | P3.0 | 4 | P9.1 |
| 5 | P4.4 | 6 | P3.1 |
| 7 | P4.5 | 8 | P9.3 |
| 9 | GND_SIGNAL | 10 | VIN |
| 11 | P4.6 | 12 | P12.0 |
| 13 | P4.7 | 14 | P9.0 |
| 15 | P7.0/I2C_SCL | 16 | P12.1 |
| 17 | P7.1/I2C_SDA | 18 | P12.2 |
| 19 | P7.2 | 20 | P12.3 |
| 21 | P7.3 | 22 | P5.1 |
| 23 | GND_SIGNAL | 24 | VIN |
| 25 | P4.0 | 26 | P12.4 |
| 27 | P4.1 | 28 | P0.0/CC1_WCO_OUT |
| 29 | P4.2 | 30 | P0.1/CC1_WCO_IN |
| 31 | P4.3 | 32 | P1.0/CC1_ECO_IN |
| 33 | P6.0 | 34 | P1.1/CC1_ECO_OUT |
| 35 | P6.1 | 36 | P12.5 |
| 37 | GND_SIGNAL | 38 | VIN |
| 39 | P9.4 | 40 | P12.6 |
| 41 | P9.2 | 42 | P2.2 |
| 43 | P10.0 | 44 | P2.3 |

**(table continues...)**

**Table 30 (continued) Interface-board J1 120-pin mapping**

| Odd pin | Function | Even pin | Function |
|---|---|---|---|
| 45 | P10.1 | 46 | P12.7 |
| 47 | P10.2 | 48 | P9.6 |
| 49 | P6.2/CAN_RX | 50 | P3.2 |
| 51 | P6.3/CAN_TX | 52 | P3.3 |
| 53 | P9.5/CC1_STATUS_LED | 54 | P5.2/UART_RX |
| 55 | GND_SIGNAL | 56 | P5.3/UART_TX |
| 57 | P8.0/SPI_SELECT0 | 58 | P5.0 |
| 59 | P8.1/SPI_MOSI | 60 | P13.0 |
| 61 | P8.2/SPI_MISO | 62 | P13.1 |
| 63 | P8.3/SPI_CLK | 64 | P13.2 |
| 65 | AN_A0 | 66 | VDDA_C |
| 67 | AN_A1 | 68 | AN_A7 |
| 69 | AN_A5 | 70 | AN_A6 |
| 71 | AN_A3 | 72 | AN_B4 |
| 73 | AGND | 74 | AGND |
| 75 | AN_A4 | 76 | AN_B5 |
| 77 | VAREF_EXT_C | 78 | AN_B2 |
| 79 | AN_A2 | 80 | AN_B3 |
| 81 | AN_B0 | 82 | AN_B6 |
| 83 | AN_B1 | 84 | AN_B7 |
| 85 | NC | 86 | NC |
| 87 | AGND | 88 | AGND |
| 89 | NC | 90 | P8.4 |
| 91 | NC | 92 | P8.5 |
| 93 | NC | 94 | NC |
| 95 | P7.7 | 96 | NC |
| 97 | P7.6 | 98 | NC |
| 99 | P7.5 | 100 | P8.6 |
| 101 | P7.4 | 102 | NC |
| 103 | NC | 104 | P8.7 |
| 105 | NC | 106 | NC |
| 107 | NC | 108 | P11.1/USB_DP |
| 109 | NC | 110 | P11.0/USB_DN |

**(table continues...)**

**Table 30 (continued) Interface-board J1 120-pin mapping**

| Odd pin | Function | Even pin | Function |
|---|---|---|---|
| 111 | P9.7 | 112 | GND_SIGNAL |
| 113 | GND_SIGNAL | 114 | P2.0/TDI |
| 115 | P1.2/SWCLK_TCK | 116 | P2.1/TDO |
| 117 | P1.3/SWDIO_TMS | 118 | VBACKUP_C |
| 119 | +3V3_OUT | 120 | +3V3_OUT |

Figure 52 shows the complete J1 signal mapping. It groups the power, digital, analog, USB, debug, and clock pins while preserving the numbered-pin order defined in Table 30.

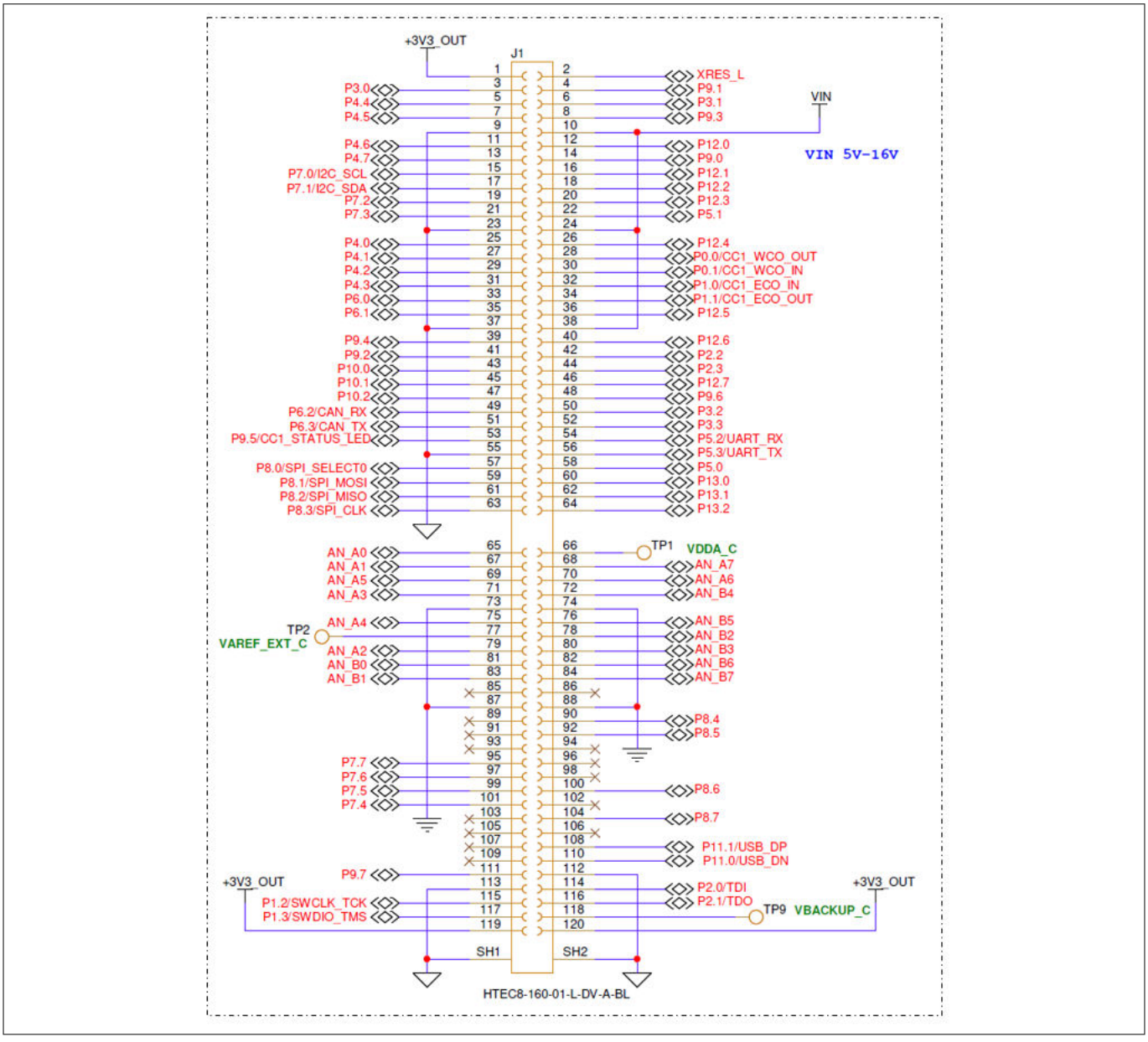



**Figure 52 Interface-board J1 signal mapping**

### 3.2.2 Expansion header

Headers J2 through J7 are the interface-board expansion connectors. Each header exposes a subset of the J1 nets as one of four digital groups or one of two analog or mixed-signal groups.

J2 provides reset, clock, debug, P2/P3 GPIO, VIN, and GND signals. J3 provides P4 through P6 GPIO, along with the UART and CAN logic signals. J4 provides I2C, SPI, P7/P9 GPIO, +3V3_OUT, and GND. J5 provides P10 through P13 GPIO, USB signals, and the two fitted straps. J6 and J7 provide the AN_A and AN_B analog banks, together with selected GPIO signals and ground-return connections.

All six headers are fitted and connect directly to J1 unless stated otherwise.

***Warning:*** ***The interface board is passive and does not make exposed signals tolerant of unspecified voltages or bus conditions.***

#### Detailed description of expansion headers

J2 is an 18-position digital header that provides VIN, the reset net, the WCO/ECO clock pins, the SWD/JTAG debug pins, P2/P3 GPIO, and GND_SIGNAL. The signals connect directly from J1. This header does not include active protection, isolation, or level translation. Table 31 lists the complete J2 pin assignment.

**Table 31 Interface J2**

| Pin | Function |
|---|---|
| 1 | VIN |
| 2 | VIN |
| 3 | XRES_L |
| 4 | P2.0/TDI |
| 5 | P0.0/CC1_WCO_OUT |
| 6 | P2.1/TDO |
| 7 | P0.1/CC1_WCO_IN |
| 8 | P2.2 |
| 9 | P1.0/CC1_ECO_IN |
| 10 | P2.3 |
| 11 | P1.1/CC1_ECO_OUT |
| 12 | P3.0 |
| 13 | P1.2/SWCLK_TCK |
| 14 | P3.1 |
| 15 | P1.3/SWDIO_TMS |
| 16 | P3.2 |
| 17 | GND_SIGNAL |
| 18 | P3.3 |

J3 is an 18-position digital header that carries VIN, P4-P6 GPIO signals, the UART_RX/UART_TX pair, the CAN_RX/CAN_TX logic pair, and GND_SIGNAL.

Note that CAN_RX and CAN_TX are logic-level signals, not CAN_H or CAN_L bus signals. The interface board does not include a CAN transceiver.

Table 32 lists the complete J3 pin assignment.

**Table 32 Interface J3**

| Pin | Function |
|---|---|
| 1 | P4.0 |
| 2 | VIN |
| 3 | P4.1 |
| 4 | P5.0 |
| 5 | P4.2 |
| 6 | P5.1 |
| 7 | P4.3 |
| 8 | P5.2/UART_RX |
| 9 | P4.4 |
| 10 | P5.3/UART_TX |
| 11 | P4.5 |
| 12 | P6.0 |
| 13 | P4.6 |
| 14 | P6.1 |
| 15 | P4.7 |
| 16 | P6.2/CAN_RX |
| 17 | GND_SIGNAL |
| 18 | P6.3/CAN_TX |

J4 is an 18-position digital header that carries +3V3_OUT, the I2C signal pair, SPI signals, P7 and P9 GPIO signals, the status-LED-labeled net, and GND_SIGNAL.

Routing is direct from J1. Note that this board does not provide $I^2C$ pull-ups, buffers, or level-translation functions.

Table 33 lists the complete J4 pin assignment.

**Table 33 Interface J4**

| Pin | Function |
|---|---|
| 1 | P7.0/I2C_SCL |
| 2 | +3V3_OUT |
| 3 | P7.1/I2C_SDA |
| 4 | P9.0 |
| 5 | P7.2 |
| 6 | P9.1 |
| 7 | P7.3 |
| 8 | P9.2 |

**(table continues...)**

**Table 33 (continued) Interface J4**

| Pin | Function |
|---|---|
| 9 | P8.0/SPI_SELECT0 |
| 10 | P9.3 |
| 11 | P8.1/SPI_MOSI |
| 12 | P9.4 |
| 13 | P8.2/SPI_MISO |
| 14 | P9.5/CC1_STATUS_LED |
| 15 | P8.3/SPI_CLK |
| 16 | P9.6 |
| 17 | GND_SIGNAL |
| 18 | P9.7 |

J5 is an 18-position digital header that carries P10-P13 GPIO signals, the USB_D+/USB_D– pair, and two fixed-strap pins. By default, R2 pulls pin 2 toward +3V3_OUT, and R3 pulls pin 4 toward GND_SIGNAL.

Note that this board does not provide a USB connector, ESD protection array, or series-termination components.

Table 34 lists the complete J5 pin assignment.

**Table 34 Interface J5**

| Pin | Function |
|---|---|
| 1 | P12.0 |
| 2 | 1 kΩ pull-up to +3V3_OUT through R2 |
| 3 | P12.1 |
| 4 | 1 kΩ pull-down to GND_SIGNAL through R3 |
| 5 | P12.2 |
| 6 | P10.1 |
| 7 | P12.3 |
| 8 | P10.2 |
| 9 | P12.4 |
| 10 | P13.0 |
| 11 | P12.5 |
| 12 | P13.1 |
| 13 | P12.6 |
| 14 | P13.2 |
| 15 | P12.7 |
| 16 | P11.0/USB_DN |
| 17 | P10.0 |

**(table continues...)**

**Table 34 (continued) Interface J5**

| Pin | Function |
|---|---|
| 18 | P11.1/USB_DP |

J6 is a 16-position analog and mixed-signal header that carries the AN_A0-AN_A7 channels, P7.4-P7.7 GPIO signals, and AGND.

These channels fan out directly from J1. Note that the interface board does not provide an analog front end, scaling network, or protection circuitry.

Table 35 lists the complete J6 pin assignment.

**Table 35 Interface J6**

| Pin | Function |
|---|---|
| 1 | AN_A0 |
| 2 | P7.4 |
| 3 | AN_A1 |
| 4 | P7.5 |
| 5 | AN_A2 |
| 6 | P7.6 |
| 7 | AN_A3 |
| 8 | P7.7 |
| 9 | AN_A4 |
| 10 | AGND |
| 11 | AN_A5 |
| 12 | AGND |
| 13 | AN_A6 |
| 14 | AGND |
| 15 | AN_A7 |
| 16 | AGND |

J7 is a 16-position analog and mixed-signal header that carries the AN_B0-AN_B7 channels, P8.4-P8.7 GPIO signals, AGND, and GND_SIGNAL.

These signals fan out directly from J1. Note that the interface board does not define the analog input range, filtering, or calibration for these channels.

Table 36 lists the complete J7 pin assignment.

**Table 36 Interface J7**

| Pin | Function |
|---|---|
| 1 | AN_B0 |
| 2 | P8.4 |
| 3 | AN_B1 |

**(table continues...)**

**Table 36 (continued) Interface J7**

| Pin | Function |
|---|---|
| 4 | P8.5 |
| 5 | AN_B2 |
| 6 | AGND |
| 7 | AN_B3 |
| 8 | AGND |
| 9 | AN_B4 |
| 10 | P8.6 |
| 11 | AN_B5 |
| 12 | P8.7 |
| 13 | AN_B6 |
| 14 | GND_SIGNAL |
| 15 | AN_B7 |
| 16 | GND_SIGNAL |

Figure 53 shows the expansion-header fan-out. It maps each J2-J7 header group directly to J1 and identifies the locations of the J5 strap pins and ground-return connections.

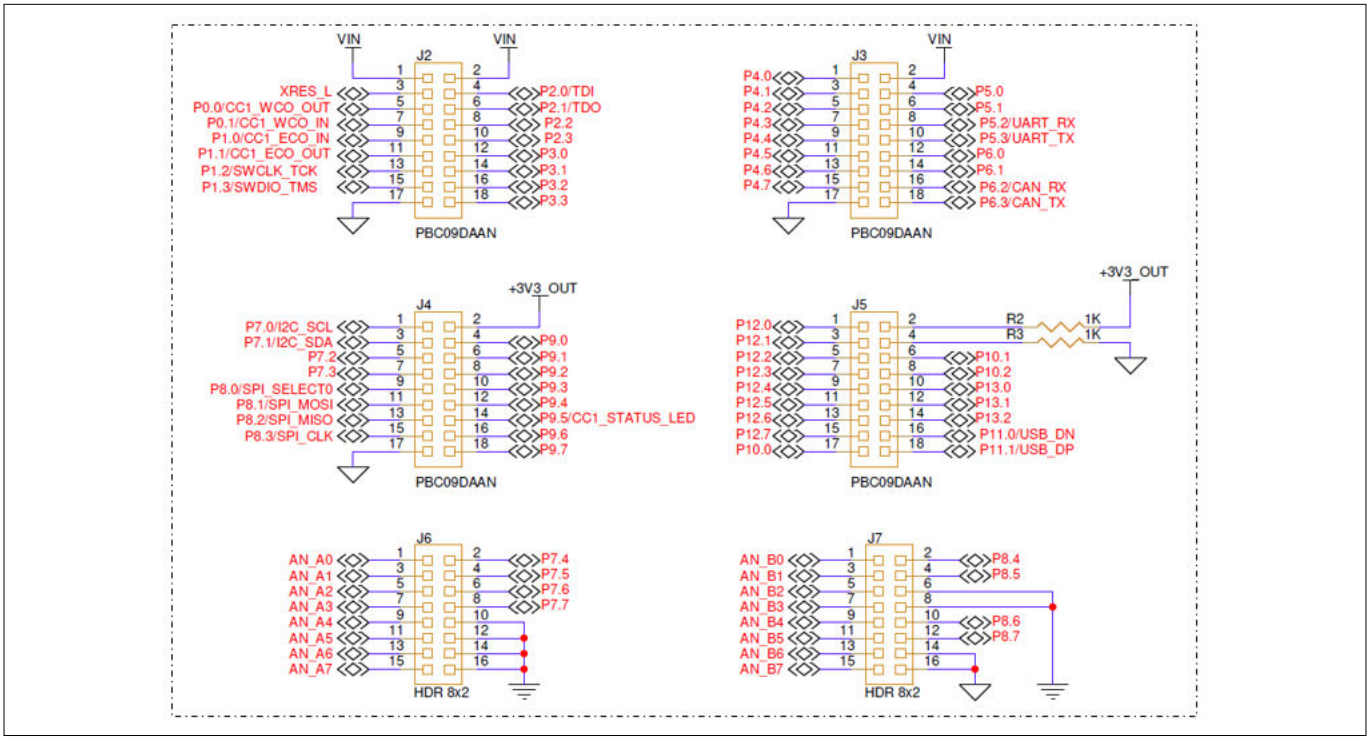



**Figure 53 Interface-board expansion-header connections**

## 3.3 Rework section

The rework section documents six evidence-backed assembly alternatives that redirect signal routing, select an alternate supply source, or replace the fitted MCU package on the control card. Each alternative is documented alongside its default population in the associated schematic and BOM references.

Every option in this section is implemented through solder rework of the default bill of materials. None of the six alternatives uses a user-removable jumper. Before modifying any component, remove all power from the board, apply ESD controls, confirm which alternative is fitted, and follow the released rework instructions rather than relying solely on this summary.

Because each rework option pairs a default 0 Ω link with a corresponding DNI alternative, treat the two paths in a given pair as mutually exclusive unless separate engineering evidence confirms that both components may be populated simultaneously.

Table 37 links each of the six rework topics to its default assembly, alternate configuration, and the detailed subsection that documents the affected circuit.

***Warning:*** ***Remove all power from the board before performing any solder rework. Apply ESD controls throughout the procedure and follow the released assembly instructions for the specific option being modified.***

.

**Table 37 Rework-topic index**

| Section | Outcome | Default assembly | Alternative |
|---|---|---|---|
| Rework for MCU clock | Clock routing | Onboard WCO/ECO | J8 clock nets |
| Rework for UART signals | UART routing | Isolated onboard UART | J8 UART nets |
| Rework for CAN signals | CAN routing | Isolated CAN transceiver path | J8 CAN logic nets |
| Rework for $I^2C$ signals | $I^2C$ routing | J8 $I^2C$ | Local J4 plus optional pull-ups |
| Rework for MCU power supply | Supply selection | +3V3 defaults | External VDDA/reference/ backup |
| Rework for E-LQFP-64 pin PSC3M6 MCU | MCU assembly | U1 100-pin drawing | U3 64-pin drawing |

### 3.3.1 Rework for MCU clock

Clock rework determines whether the MCU WCO and ECO clock pins remain connected to the fitted onboard crystal networks, Y2 and Y3 are exposed through the corresponding clock-labeled J8 edge routes. This section documents the resistor pairs used to select each configuration.

All routing resistors used for this option are 0 Ω, 0603 components. To expose a clock pin through J8 instead of routing it to its onboard crystal network, remove the fitted onboard-route resistor and install the corresponding DNI edge-route resistor. After this change, the MCU pin no longer follows the onboard crystal path and is instead routed to the J8 edge connector.

Because the WCO and ECO networks each use a coordinated resistor pair, perform both WCO changes together or both ECO changes together. Do not change only one resistor in either pair.

After completing the rework, verify the intended resistor pair through population inspection and continuity testing before applying power to the board. The available documentation does not define an energized adjustment procedure for this option.

**Table 38 Rework configuration**

| Outcome | Default path | Remove | Fit | Result | Side effects | Value/MPN |
|---|---|---|---|---|---|---|
| Route WCO through J8 | R85/R90 fitted to Y2 | R85, R90 | R87, R92 | P0.0/P0.1 use J8 clock nets | Onboard WCO disconnected | 0 ohm 0603 |
| Route ECO through J8 | R94/R97 fitted to Y3 | R94, R97 | R96, R99 | P1.0/P1.1 use J8 clock nets | Onboard ECO disconnected | 0 ohm 0603 |

Trace each resistor pair in Figure 54 between the onboard clock net, the associated MCU pin, and the corresponding J8-labeled alternate net to verify which route is fitted before rework.

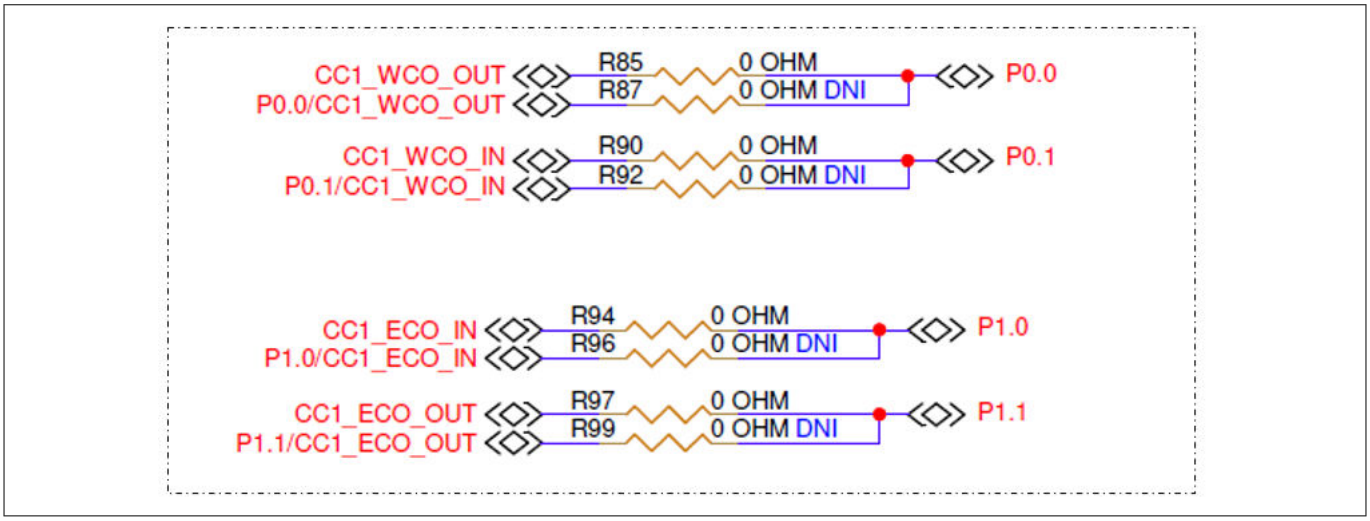



**Figure 54 Clock signal alternate resistor pairs circuit**

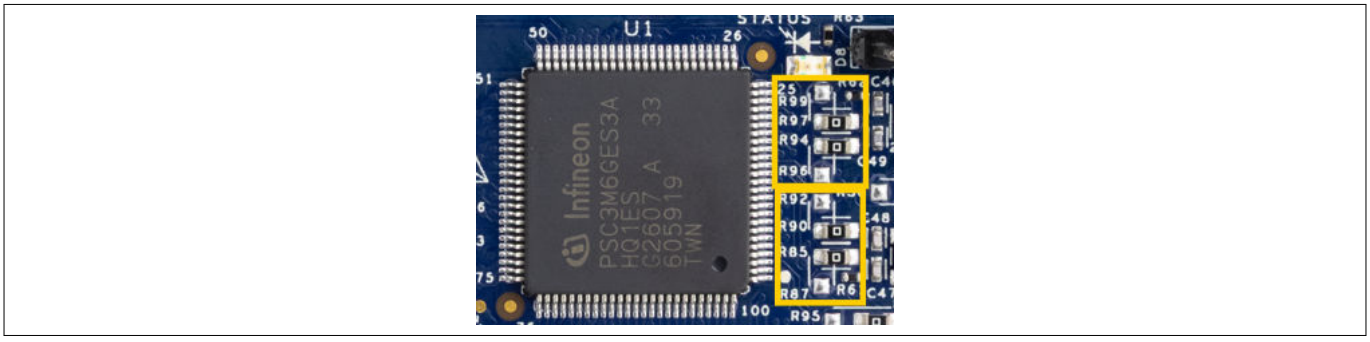



**Figure 55 Clock signals alternate resistor pairs location**

## 3.3.2 Rework for UART signals

UART rework determines whether MCU pins P5.3 and P5.2 remain connected to the isolated onboard UART path or are routed to the corresponding J8 UART-labeled edge signals.

R101 and R104 are the fitted 0 ohm links that provide the default isolated UART path. R103 and R106 are the DNI 0 Ω links that provide the alternate J8 edge route. To select the edge route, remove both fitted links (R101 and R104) and install both alternate links (R103 and R106). This change disconnects the MCU UART signal pair from the onboard isolated path and reconnects it to the J8-labeled edge signals.

Do not populate both the onboard and edge-routing paths simultaneously unless an approved contention analysis has been completed.

**Table 39 Rework configuration**

| Outcome | Default path | Remove | Fit | Result | Side effects | Value/MPN |
|---|---|---|---|---|---|---|
| Route UART through J8 | R101/R104 fitted to isolated UART | R101, R104 | R103, R106 | P5.3/P5.2 use J8 UART nets | Isolated onboard UART path disconnected | 0 ohm 0603 |

Figure 56 shows the fitted isolated UART path and the alternate J8 UART path for MCU pins P5.3 and P5.2.

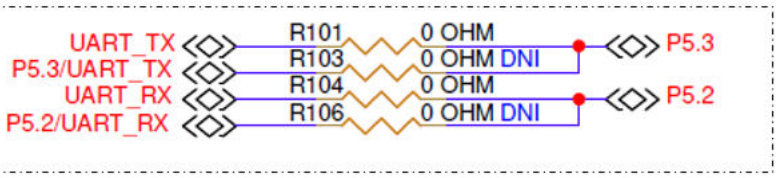



**Figure 56 UART signals alternate resistor pairs circuit**

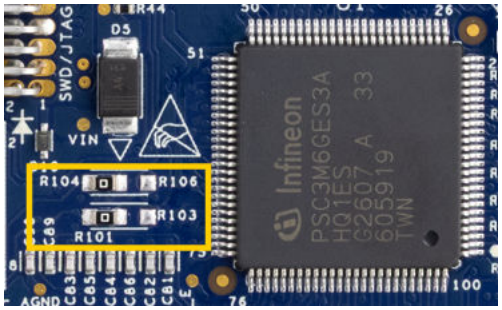



**Figure 57 UART signals alternate resistor pairs location**

## 3.3.3 Rework for CAN signals

CAN rework determines whether MCU pins P6.2 and P6.3 remain connected to the isolated transceiver-side CAN logic path or are routed to the corresponding CAN-labeled J8 edge signals.

R93 and R98 are the fitted 0 Ω links that implement the default isolated CAN logic path. R95 and R100 are the DNI 0 Ω links that implement the J8 edge route. To enable edge routing, remove both fitted links, R93 and R98, and install both alternate links, R95 and R100.

After this change, the MCU no longer connects to the U11/U5 isolator and transceiver pair through the default path. As a result, the physical CAN connection available at J3 is no longer provided through that route. Do not enable both destinations simultaneously.

***Warning:*** ***Do not populate the onboard and edge CAN routes simultaneously unless an approved contention analysis confirms that both routes can be used together.***

**Table 40 Rework configuration**

| Outcome | Default path | Remove | Fit | Result | Side effects | Value/MPN |
|---|---|---|---|---|---|---|
| Route CAN logic through J8 | R93/R98 fitted to U11/U5 path | R93, R98 | R95, R100 | P6.2/P6.3 use J8 CAN logic nets | J3 physical CAN path no longer reached by default route | 0 ohm 0603 |

Figure 58 shows the default isolated CAN logic path and the alternate J8 CAN path for MCU pins P6.2 and P6.3.

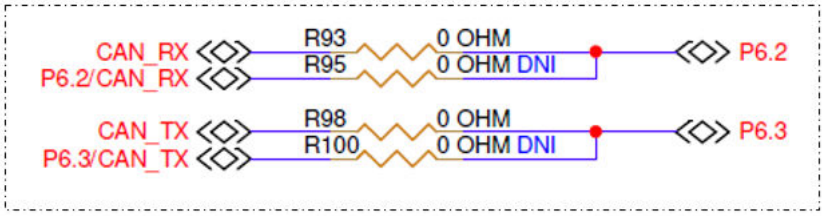



**Figure 58 CAN signals alternate resistor pairs circuit**

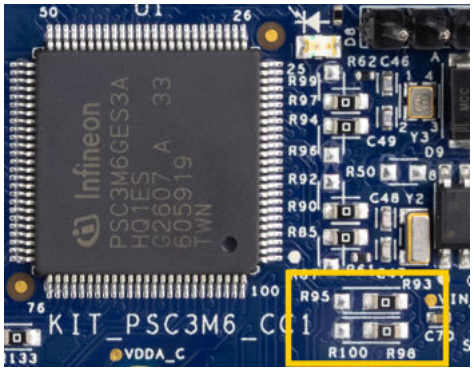



**Figure 59 CAN signals alternate resistor pairs location**

## 3.3.4 Rework for I²C signals

I²C rework determines whether MCU pins P7.0 and P7.1 remain connected to the default J8 route or are connected to the local J4 route. It also determines whether the local pull-up resistor footprints are populated.

R86 and R89 are the fitted 0 Ω links that connect the MCU to J8 by default. R88 and R91 are the DNI 0 Ω links that connect the local J4 nets instead. To select the local J4 route, remove both fitted links, R86 and R89, and install both alternate links, R88 and R91.

Pull-up resistors R57 and R59 form a separate pair of DNI 5.1 kΩ, 0402 components that operate independently of the route selection. Populate these resistors only when required by the intended bus design. The available documentation does not demonstrate I²C bus operation with any specific external pull-up configuration.

***Note**: Populating the local pull-up resistors alone does not guarantee I2C bus operation in a particular external system.*

**Table 41 Rework configuration**

| Outcome | Default path | Remove | Fit | Result | Side effects | Value/MPN |
|---|---|---|---|---|---|---|
| Route I2C through local J4 | R86/R89 fitted to J8 | R86, R89 | R88, R91 | P7.0/P7.1 connect to J4 nets | J8 I2C route disconnected | 0 ohm 0603 |
| Add local J4 pull-ups | R57/R59 DNI | None | R57, R59 | SCL/SDA pulled toward +3V3 as drawn | External bus pull-up interaction must be reviewed | 5.1 KΩ 0402 |

Trace both the J8 and local J4 SCL/SDA routes to MCU pins P7.0 and P7.1, then locate the separate DNI pull-up resistor footprints, R57 and R59, adjacent to the bus nets.

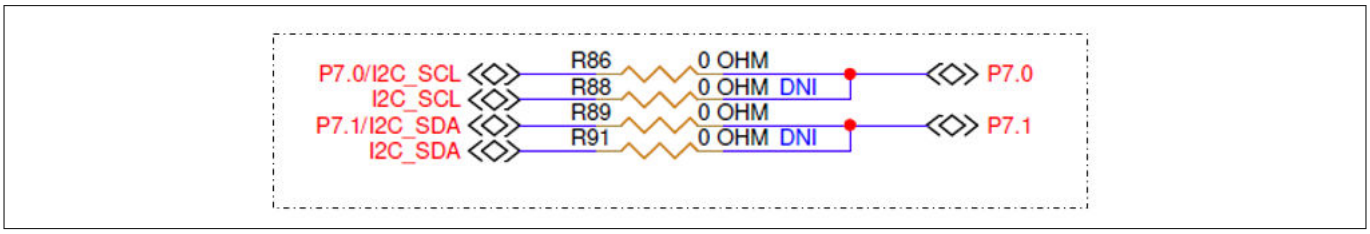



**Figure 60 I²C signals alternate resistor pairs circuit**

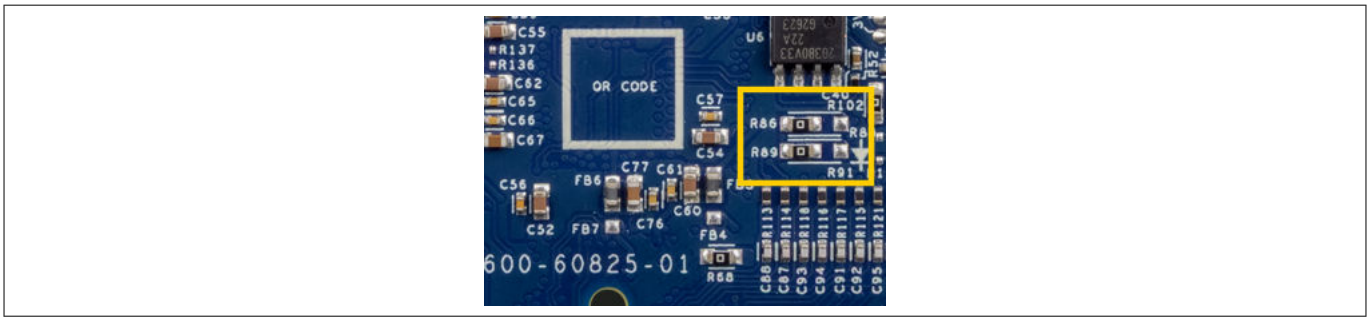



**Figure 61 I²C signals alternate resistor pairs location**

## 3.3.5 Rework for MCU power supply

Supply rework determines, independently for each of three domains, whether the MCU receives the default +3V3-derived supply or an externally supplied input from VDDA_C, VAREF_EXT_C, or VBACKUP_C.

FB6, FB3, and R66 are the fitted default links that source VDDA, VAREF_EXT, and VBACKUP, respectively, from +3V3. FB7, FB4, and R67 are the corresponding DNI external-source alternatives. For each domain, remove the fitted default link before installing the corresponding alternate link. This prevents the +3V3-derived source and the external source from being connected to the same net.

FB3, FB4, FB6, and FB7 are ferrite-bead links. R66 and R67 are 0 Ω links. The available documentation does not specify the voltage, tolerance, or power-sequencing requirements for the external inputs.

***Warning:*** ***Remove the fitted default source link before installing the corresponding external-source link. Never connect both sources to the same supply domain simultaneously.***

**Table 42 Rework configuration**

| Outcome | Default path | Remove | Fit | Result | Side effects | Value/MPN |
|---|---|---|---|---|---|---|
| Externally source VDDA | FB6 fitted from +3V3 | FB6 | FB7 | VDDA supplied from VDDA_C | External limits/ sequencing unavailable | 1 kΩ ferrite |
| Externally source VAREF_EXT | FB3 fitted from +3V3 | FB3 | FB4 | VAREF_EXT supplied from VAREF_EXT_C | External limits/ sequencing unavailable | 1 kΩ ferrite |
| Externally source VBACKUP | R66 fitted from +3V3 | R66 | R67 | VBACKUP supplied from VBACKUP_C | External limits/ sequencing unavailable | 0 Ω 0603 |

Trace each +3V3 default-source link and its mutually exclusive external-input alternative to identify which supply source powers the corresponding MCU domain.

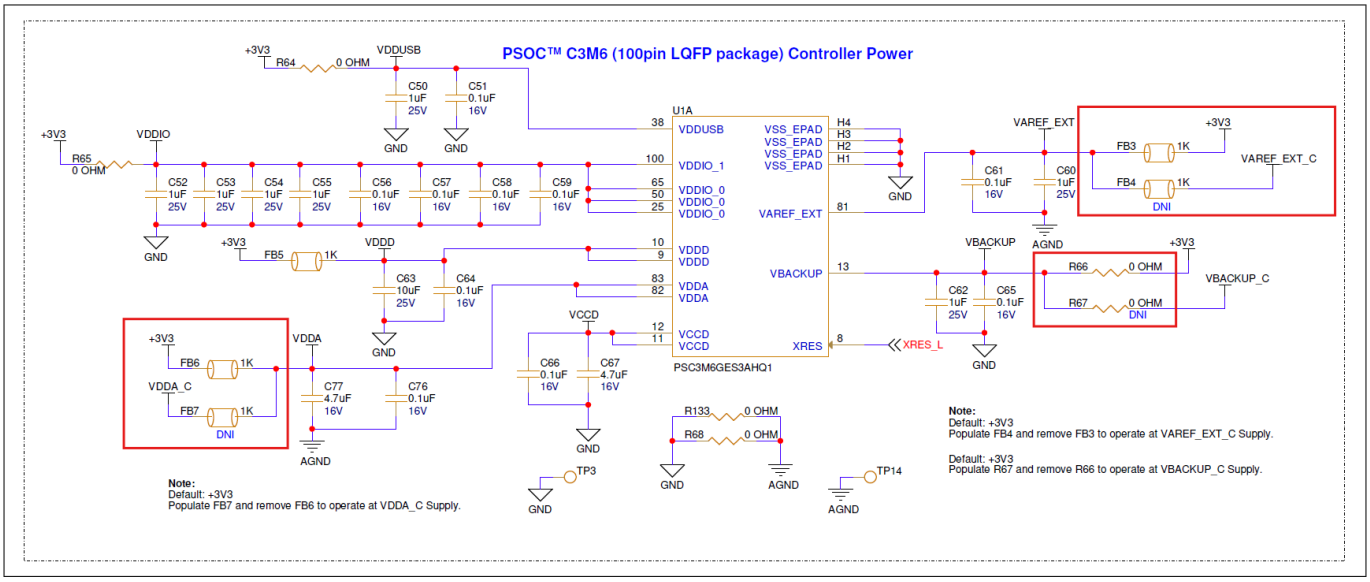



**Figure 62 VDDA, reference, and backup supply selections circuit**

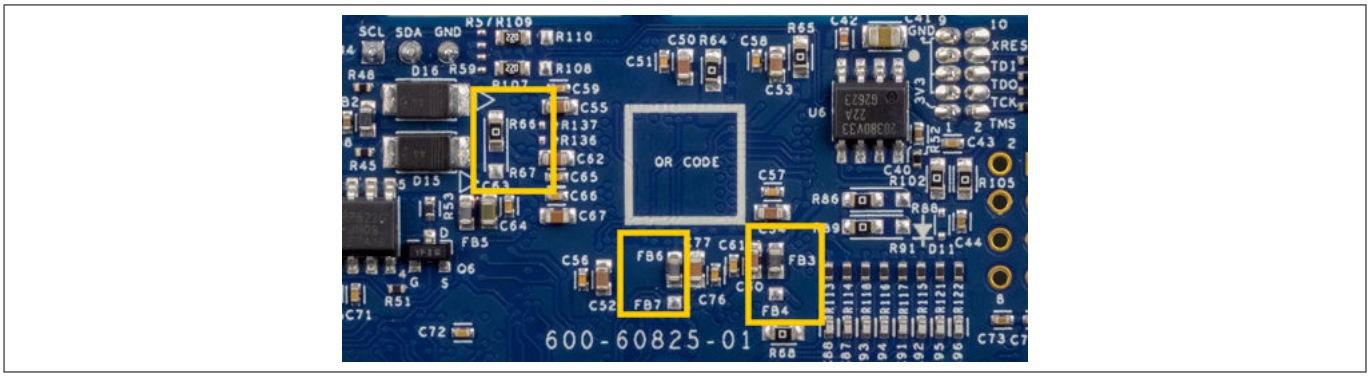



**Figure 63 VDDA, reference, and backup supply selections location**

### 3.3.6 Rework for E-LQFP-64 pin PSC3M6 MCU

The alternate MCU option describes a manufacturing assembly variant that substitutes the DNI U3 footprint for the fitted U1 footprint, together with its associated component population.

In the default assembly, U1 is fitted, while U3, R136, and R137 remain DNI. The alternate assembly option uses U3 and populates the associated 0 Ω links as required.

Because the control card supports dual-footprint package assembly, the digital I/O, analog I/O, and communication interfaces are routed to support both package variants.

***Note**: The alternate MCU option is a manufacturing assembly variant and is not intended as a field-replacement procedure. USB is not supported by the E-LQFP-64 package. Therefore, the target USB connector (J6) signals are not connected to this MCU variant.*

**Table 43 Rework configuration**

| Outcome | Default path | Remove | Fit | Result | Side effects | Value/MPN |
|---|---|---|---|---|---|---|
| Assemble alternate MCU package | U1 PSC3M6GES3AHQ1(E-LQFP-100) fitted | U1 and U1-specific population per released instructions | U3 PSC3M6GES3ACQ1(E-LQFP-64); R136/R137 as required | Uses 64-pin alternate schematic option | Not field-swappable; compatibility verified | R136/R137: 0 Ω 0402 |

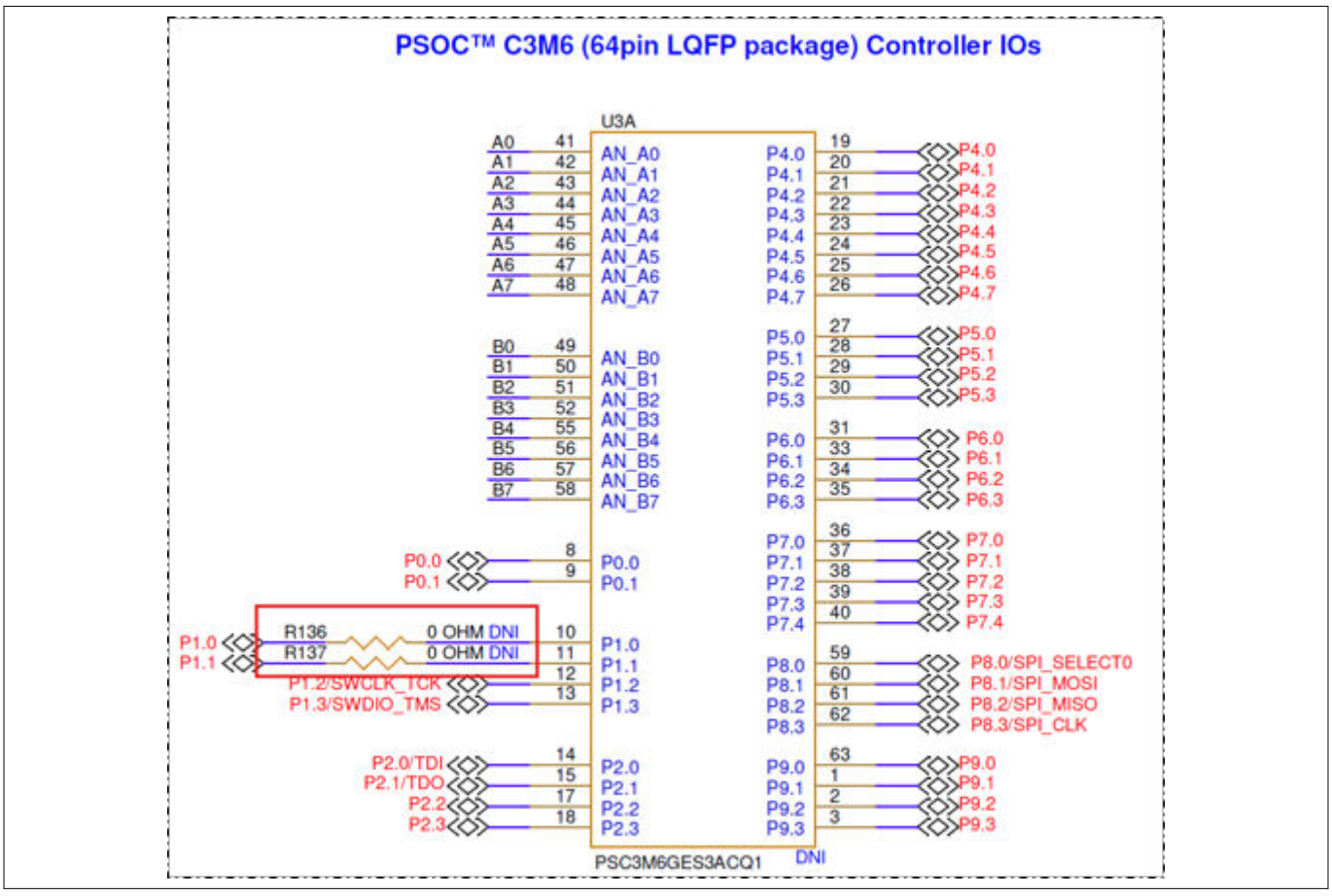



**Figure 64 Target MCU E-LQFP-64 resistor circuit**

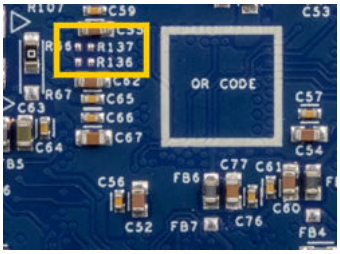



**Figure 65** **Target MCU E-LQFP-64 resistor location**

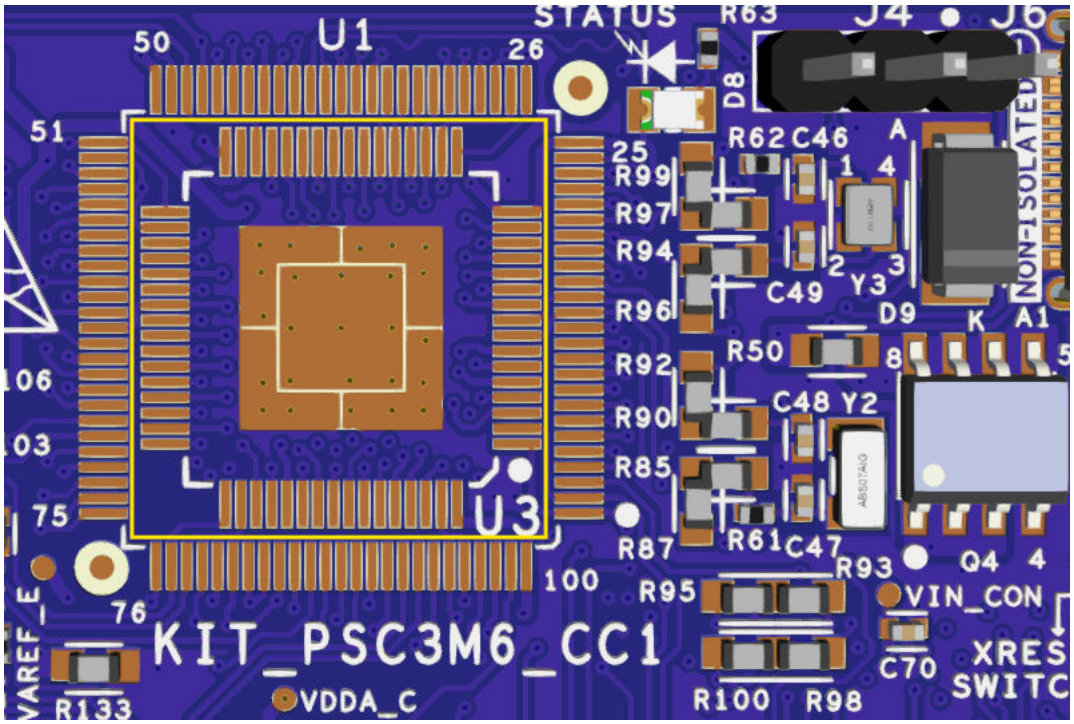



**Figure 66** **Target MCU E-LQFP-64 IC location**

## 3.4 Bill of materials (BoM)

This section provides a selective key-parts index derived from the control-card and interface-board designs, together with references to the two authoritative BOM source files. It is not intended to serve as a complete production BOM.

The summary focuses on active devices, isolation and conversion components, connectors, switches, and clock components used across both boards. It intentionally excludes most passive components and does not replace assembly instructions, approved purchasing data, placement data, or manufacturing test requirements. The population status shown in Table 44 follows the source BOM files.

***Note**:* *This key-parts table does not indicate production readiness, AVL approval, or manufacturing release status.*

**Table 44 Key active and connectivity items**

| Board | Function | Reference | Part/value | Population | Source/status |
|---|---|---|---|---|---|
| Control card | Target MCU | U1 | PSC3M6GES3AHQ1 | Fitted | Control BOM |
| Control card | Alternate target MCU | U3 | PSC3M6GES3ACQ1 | DNI | Control BOM |
| Control card | Programmer MCU | U2 | XMC4200-Q48F256 BA | Fitted | Control BOM |
| Control card | 3.3 V regulators | U4, U6 | TLS203B0EJV33XUMA1 | Fitted | Control BOM |
| Control card | CAN transceiver | U5 | TLE9351BVSJXTMA1 | Fitted | Control BOM |
| Control card | Isolated DC/DC | U7 | 1769205132 | Fitted | Control BOM |
| Control card | SWD isolator | U8 | SI8641BB-B-IS1R | Fitted | Control BOM |
| Control card | UART/CAN/reset isolators | U10-U12 | ISO6721BQDRQ1 | Fitted | Control BOM |
| Control card | Logic buffers | U9, U13 | 74LVC1G126GM,115 | Fitted | Control BOM |
| Control card | USB Type-C receptacles | J1, J6 | 629722000214 | Fitted | Control BOM |
| Control card | Control CAN header | J3 | TSW-103-08-F-S-RA | Fitted | Control BOM |
| Control card | Control I2C header | J4 | PREC003SAAN-RC | Fitted | Control BOM |
| Control card | Control debug header | J5 | FTSH-105-01-L-D-RA-K | Fitted | Control BOM |
| Control card | Control optional header | J7 | PRPC004DAAN-RC | DNI | Control BOM |
| Control card | Control edge fingers | J8 | HSEC8-160-01-L-DV-A-BL_Edge_Finger | DNI | Control BOM |
| Interface board | Interface board connector | J1 | HTEC8-160-01-L-DV-A-BL | Fitted | Interface BOM |
| Interface board | Interface digital headers | J2-J5 | PBC09DAAN | Fitted | Interface BOM |
| Interface board | Interface analog headers | J6-J7 | PBC08DAAN | Fitted | Interface BOM |
| Control card | Reset switch | SW1 | MJTP1117 | Fitted | Control BOM |
| Control card | SWD routing switch | SW2 | JS202011JCQN | Fitted | Control BOM |

**(table continues...)**

**Table 44 (continued) Key active and connectivity items**

| Board | Function | Reference | Part/value | Population | Source/status |
|---|---|---|---|---|---|
| Control card | Target crystal | Y2 | ABS07AIG-32.768 KHZ-6-T | Fitted | Control BOM |
| Control card | Target crystal | Y3 | ABM11W-16.000 0MHZ-6-K1Z-T3 | Fitted | Control BOM |

# Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| ** | 2026-09-08 | Initial release |
| *A | 2026-10-28 | Updated Theory of operation section. |

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Customer shall not touch the Evaluation Board during operation and keep a safe distance.
Customer shall not touch the Evaluation Board after disconnecting the power supply, several components may still store electrical voltage and can discharge through physical contact. Several parts, like heat sinks and transformers, may still be very hot. Allow the components to cool before touching or servicing.
The electrical installation must be completed in accordance with the appropriate safety requirements.