ferApplication Note

EiceDRIVER™ gate driver 1EDI302xAS, 1EDI303xAS (x=5,6,8)

About this document

Scope and purpose

This is an application note for the EiceDRIVER™ gate driver 1EDI3035AS, 1EDI3025AS, 1EDI3026AS, 1EDI3028AS and 1EDI3038AS family of devices. This document is intended to give user of the product hints for the usage in the application. For more details on product specification please refer to the datasheet.

It is the responsibility of the integrator to ensure that the EiceDRIVER™ gate driver complies with the appropriate application standards.

Intended audience

This application note is inteded for engineers who are using the EiceDRIVER™ gate driver in their application.

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1 Product selection and features

There is a total of five different devices in this product family: 1EDI3035AS, 1EDI3025AS, 1EDI3026AS and 1EDI3028AS. Each family member implements a slightly different feature-set and is optimized to target different power switch technologies, whereas the power stage and safety concept is shared between all members.

Table 1 shows the key product features per variant in order to ease the slection process. The user can distinguish the following feature sets:

- External active Miller clamp – AMCLP
- External softoff pin – SOFTOFF
- Overcurrent protection – OCP
- Desaturation protection – DESAT
- VEE2 OVLO monitoring – OVLO3

Table 1 Overview of product variants

Type	AMCLP	SOFTOFF	OCP	DESAT	OVLO3	ADC	Output stage rated current	Power switch target
1EDI3025AS		x		x	x	x	15 A	IGBT
1EDI3026AS		x	x		x			IGBT
1EDI3028AS		x		x			10 A	IGBT
1EDI3035AS		x		x	x		15 A	SiC
1EDI3038AS		x		x			10 A	SiC

Note: 1EDI3028AS has the current source on the ADC disabled

The 1EDI3028AS variant is optimized for EESM application, with a disabled ADC current source for NTC measurement optimization, no OVLO3 and a lower output stage current.

The 1EDI3038AS variant is prepared for OBC and DC/DC applications, with no ADC or OVLO3 and lower output stage current.

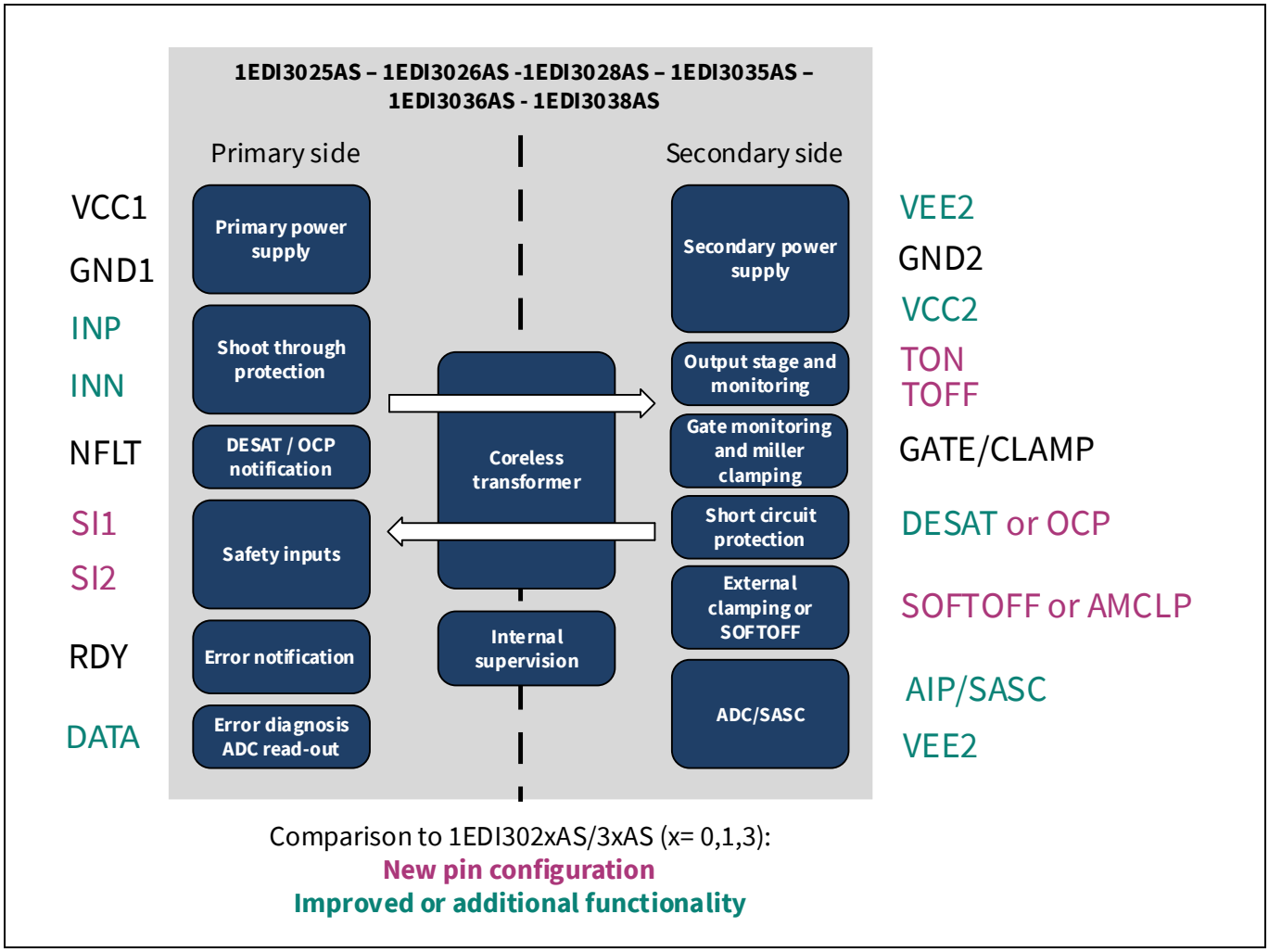


Figure 1 Block diagram including comparison to the legacy driver

Figure 1 combines Table 1 into a graphical block representation of the device. For users of the previous driver family 1EDI302xAS/3xAS (x = 0,1,3) also a comparison is given.

Most noticeable are the following upgrades to this family:

- Split output stage TON/TOFF allowing separate turn-on and turn-off gate resistors
- Primary side safety input SI1/SI2 for clearing errors and controlling ASCP
- SOFTOFF pin or AMCLP functionality
- ADC combined with SASC simultaneously
- Increased diagnosis coverage in DATA stream
- Shoot through protection with additional keep-state timer
- DESAT/OCP built-in selftest
- Adaptive VEE2 UVLO/OVLO monitoring
- Reduced minimum input pulse width of 150 ns to support active discharge applications
- Shorter DESAT/OCP blanking and detection and reaction times

2 Gate driver fundamentals

2.1 Switching behavior

The EiceDRIVER™ gate driver implements a powerful, low ohmic output stage which is prepared for driving current generation IGBT and SiC power modules and discretes with sufficient thermal margin. The configuration of the output stage is shown in Figure 2. TOFF is driven by a low ohmic n-MOSFET with a maximum Rds-on of 350 mΩ over process variation and temperature. TON is driven by the same low ohmic n-MOSFET but supported by a 1 Ω p-MOSFET.

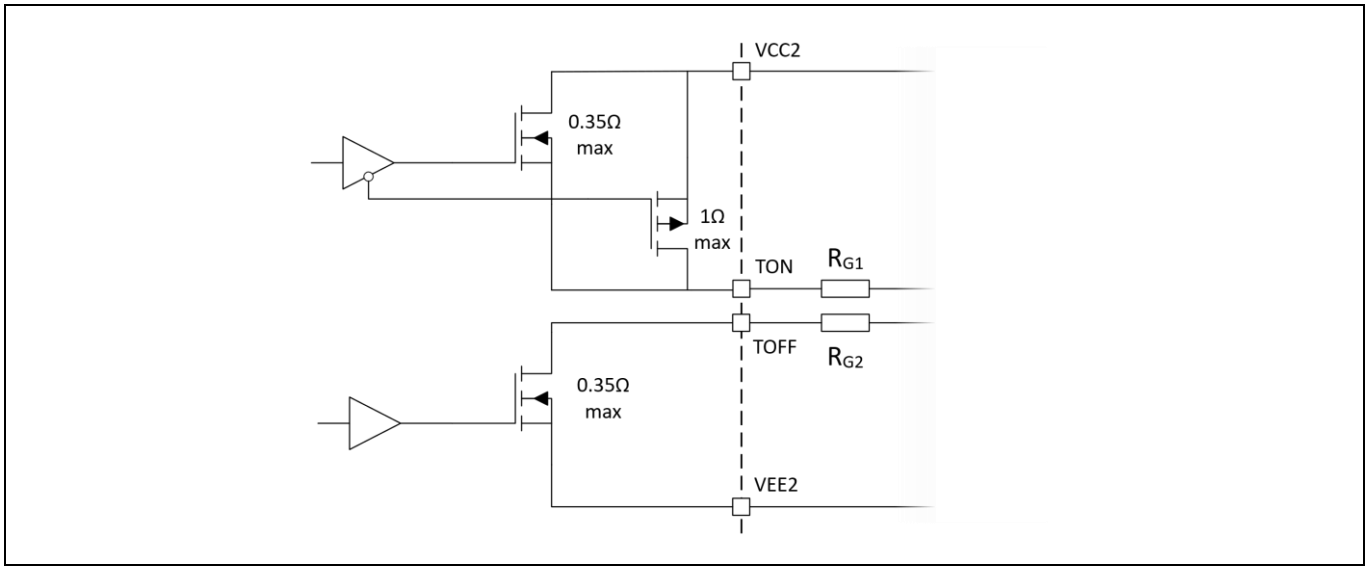


Figure 2 Output stage configuration

When turning on TON, the high-side n-MOSFET increases the output current to the peak to ensure a rapid turn-on of the driven IGBT or SiC power module. The p-MOSFET takes over once TON reaches close to the VCC2 rail.

A typical turn-on and turn-off waveform is shown in Figure 3. The waveforms show the output stage driving a 300 nF capacitor load. For this test TON and TOFF where connected together and to the load with a 1.8 Ω gate resistor.

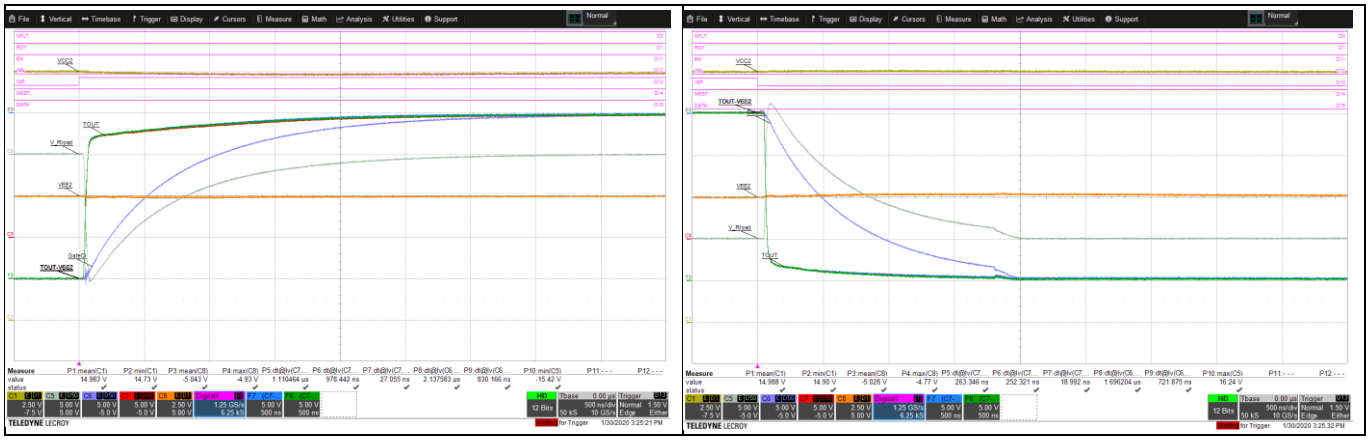


Figure 3 Left: turn-on; right: turn-off example waveform

2.2 Common mode transient immunity

With the establishment of modern SiC and GaN MOSFET technologies higher inverter efficiencies become a possibility to increase xEV range inexpensively. In order to decrease switching loss, shorter switching times are one key parameter for inverter optimization. Shorter switching times imply that the two galvanically isolated GND systems of the low voltage and the high voltage domain experience a higher “dV/dt”. Since the EiceDRIVER™ gate driver is bridging the two GND systems, this “dV/dt” will be applied to the internal isolation barrier in the form of a common-mode excitation.

2.2.1 Definition of common mode transient immunity - CMTI

The CMTI is the maximum tolerable rise and fall rate of the voltage between the two galvanically isolated grounds of the EiceDRIVER™ gate driver up to a defined peak voltage V_{cm}. It is often given in the units of [V/ns] or [kV/µs] The measurement principle is shown in Figure 4.

The figure shows two coreless transformer paths:

One is used to transmit the PWM switching signal from low voltage side to the high voltage side, while the other is used for transmitting a digitally encoded datastream in the other direction. For the family of drivers described in this application note, this information contains for example the ADC data as well as supervision information about the secondary side. Gate drivers can make use of additional coreless transformers, for example when programmability of the secondary side is required.

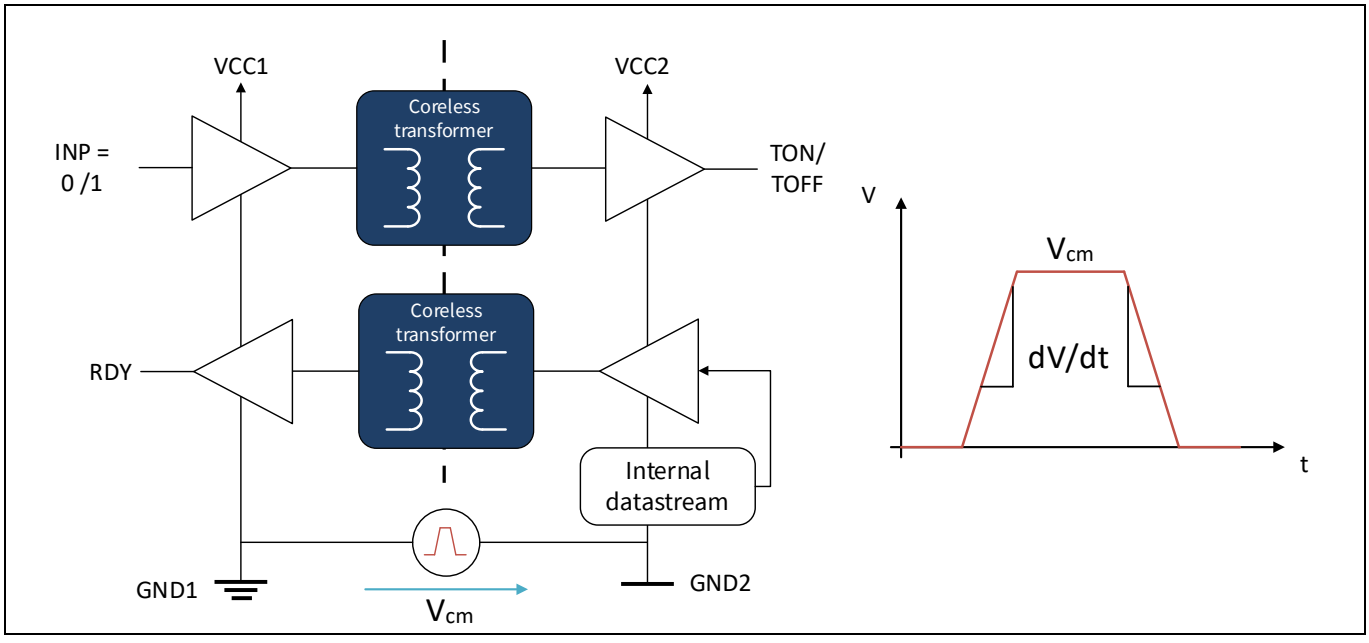


Figure 4 Verification setup of the CMTI measurement

CMTI performance is verified on each transmition path. For the PWM transmission path the input INP is kept statically low or high while the CMTI pulse is applied through a high-frequency stabilization network repeadetly. Over the curse of several thousand pulses the output of the driver is observed (TON and TOFF are connected). The failure criteria is met when the output signal deviates by 20% from either VCC2 or VEE2 in on and off-state.

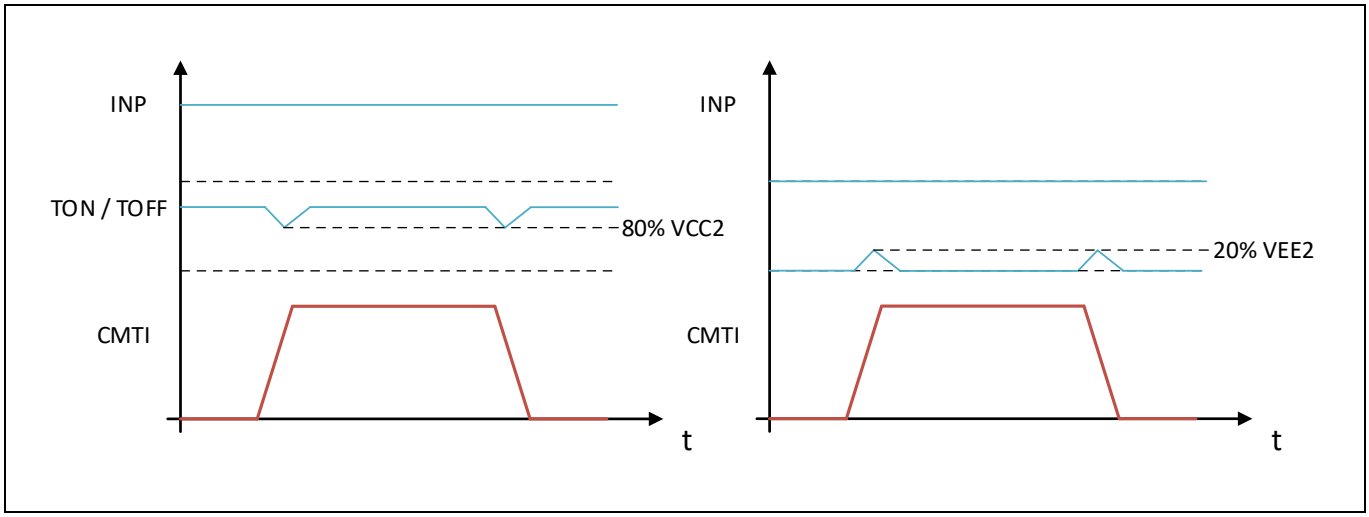


Figure 5 CMTI measurement illustration on PWM path

For the data transmission path from the secondary side to the primary side the RDY pin is observed. Here the measurement cycles can reach up to several hundred thousand cycles in order to achieve a statiscal correlation to the digital information passed through the coreless transformer. The failure criteria is met when RDY is pulled to low.

The EiceDRIVER™ gate driver family CMTI performance is concluded from the performance of both transmission paths. It excels with a best in-class CMTI rating of up to 150 V/ns. For more information please refer to the datasheet.

2.3 Thermal considerations

With ever increasing power densities in the application, thermal management is a key task to get the maximum performance out of the EiceDRIVER™ gate driver.

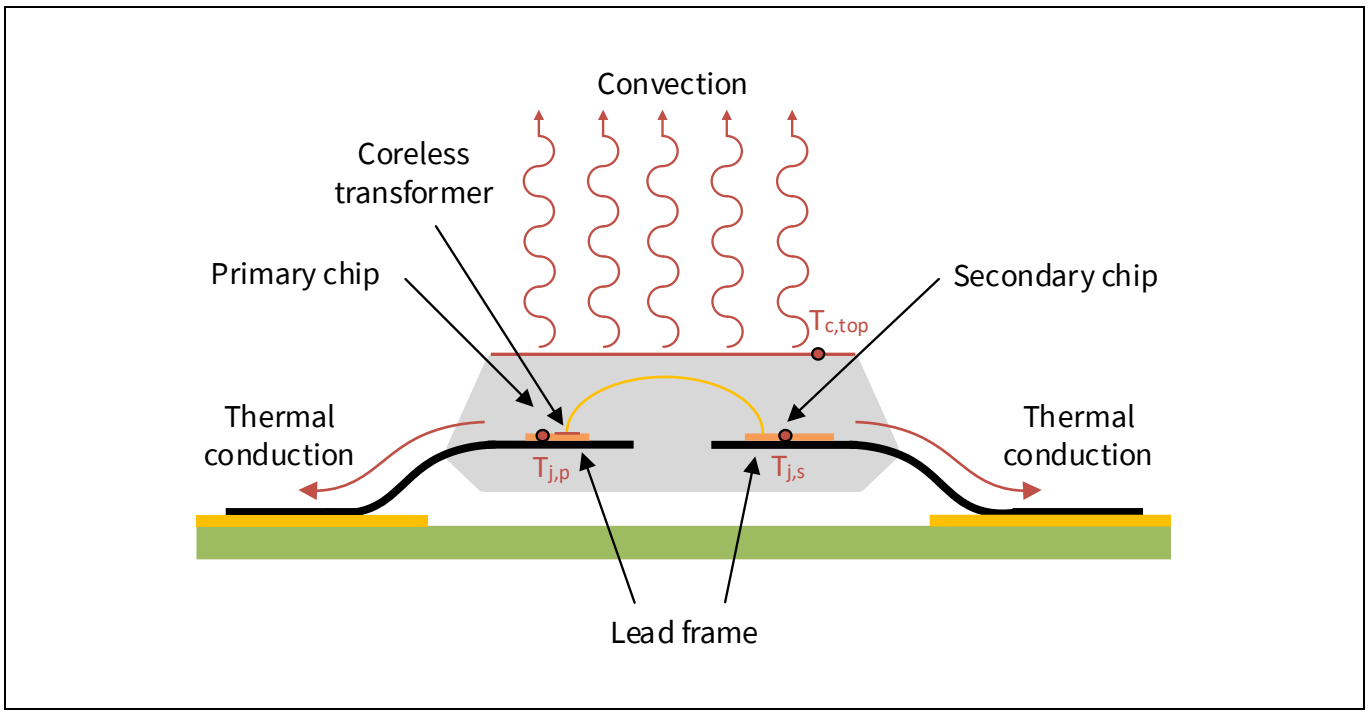


Figure 6 EiceDRIVER™ gate driver thermal dissipation paths

Figure 6 shows a simplified cross-section of the gate driver to illustrate the various ways thermal energy may dissipate into ambient:

- Thermal convection through the package surface
- Thermal radiation in the IR spectrum
- Thermal conduction through the leads

It is also most noticeable that the driver inherits two silicon dies. One on the primary side and one on the secondary side. The secondary die is usually bigger in area than the primary one, since it incorporates the output stage from Figure 2. Given this configuration, there are also two junction temperatures to be distinguished between those two chips $T_{j,p}$ and $T_{j,s}$. The system integrator shall choose the gate driver's load condition and thermal interface in a way such that the conditions $T_{j,p}$ < 150°C "and" $T_{j,s}$< 150°C are fulfilled over all operating points.

2.3.1 Deriving the thermal resistance

The thermal coupling and self-heating of both dies can be easily modeled using the following relationship to determine the increase in junction temperature to

$$\begin{pmatrix} T_{j,p} \\ T_{j,s} \end{pmatrix} = \begin{pmatrix} R_{11,\mathrm{ja}} & R_{12,\mathrm{ja}} \\ R_{21,\mathrm{ja}} & R_{22,\mathrm{ja}} \end{pmatrix} \begin{pmatrix} P_{v,p} \\ P_{v,s} \end{pmatrix} + T_{amb} = \boldsymbol{R} \cdot \vec{\boldsymbol{P}} + T_{amb} \qquad (2\text{-}1)$$

. The matrix of thermal resistances has no physical equivalence, it is determined through 3D finite element simulation by successive model excitation with either $P_{v,p} = 0$ or $P_{v,s} = 0$. Note that due to symmetry reciprocity applies and $R_{12,\mathrm{ja}} = R_{21,\mathrm{ja}}$ holds true. $R_{12,\mathrm{ja}}, R_{21,\mathrm{ja}}$ describe the thermal coupling between both dies through the mold compound and bond wires.

The thermal resistance matrix **R** is also a function of temperature. With increasing temperature the black body characteristic of the package contributes to increase dissipation by thermal radiation in the IR spectrum. Therefore the thermal resistances in the datasheet are usually specified for two ambient temperatures: 25°C and 125°C.

For the system integrator the resistance matrix delivers insights into the physical background of a two-die thermal system.

In the datasheet of EiceDRIVER™ gate driver there is only one thermal resistance $R_{\mathrm{th,ja}}$ given. This thermal resistance is formed from (*2-1*) under the following assumptions:

- Primary chip exhibits 40 mW losses – corresponds to ~50% duty cycle on INP, VCC1 = 5 V
- Higher Tj always present on secondary die

The result is a single $R_{\mathrm{th,ja}}$

$$R_{\mathrm{th,ja}} = \frac{T_{j,s} - T_{amb}}{P_{v,p} + P_{v,s}} \qquad (2\text{-}2)$$

.

2.3.2 Pseudo thermal resistance

In section “Deriving the thermal resistance” the relationship between secondary side losses and junction temperature was established. This relationship proves handy when estimating the junction temperature from calculation but it is missing a reference surface temperature in order to indirectly measure T_j.

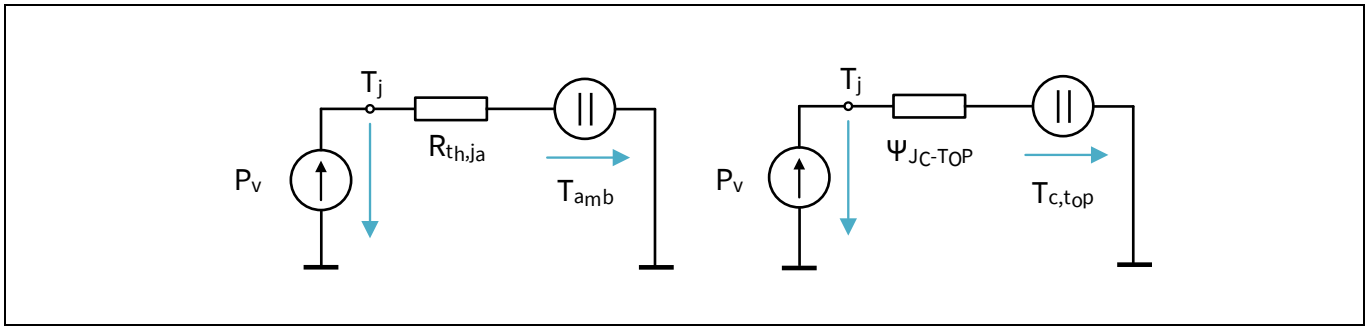


Figure 7 Thermal equivalent networks

This task can be covered by the introduction of the pseudo thermal resistance, that is usually given by the Greek letter Ψ. The pseudo thermal resistance establishes a relationship between a reference point on the IC surface

and the junction temperature. For the EiceDRIVER™ gate driver the reference point is on the top of the package as shown in Figure 6, since it is most accessible and due to the assembly structure closely coupled to the junction.

Note: For other Infineon products the reference point can be defined differently. For example, for exposed pad packages the reference is often on the exposed pad, since it is thermally best connected to the die.

The relationship between T_j and case top temperature is given by

$$T_j = \Psi_{\mathrm{JC-TOP}} \cdot P_V + T_{c,top} \qquad (2\text{-}3)$$

. This relationship can be used to estimate the junction temperature experimentally from measurement of the package top temperature.

The precision of this estimation is increased over (*2-2*), since the $R_{th,ja}$ is more dependent on the mounting situation and footprint. It is therefore recommended to use $\Psi_{\mathrm{JC-TOP}}$ to validate the gate driver thermal performance and guarantee the absolute maximum ratings are valued.

2.3.3 Thermal simulation conditions

The thermal performance parameters given in the datasheet are derived by simulation. The simulation is conducted considering the footprint and board layer stack as shown in Figure 8.

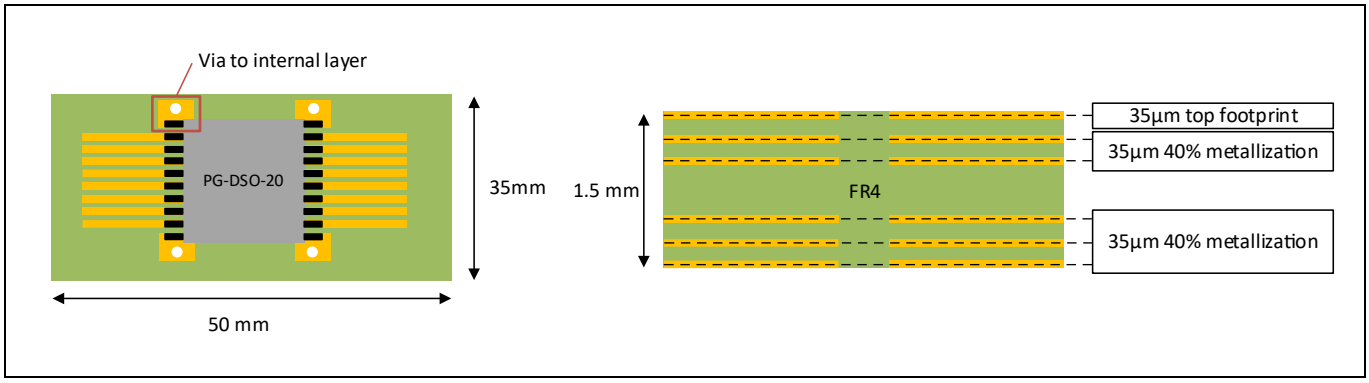


Figure 8 Footprint and PCB for thermal simulation

A 6-layer board with split copper layers is used to mimic the application conditions. On the gate driver all the pins except the corner pins are faned out. The corner pins are connected with a via to an internal copper layer to reflect the usual method of power distribution.

2.3.4 Switching loss calculation

In the previous chapters insights on the thermal modeling of the EiceDRIVER™ gate driver were given. To complete the thermal performance calculation, the internal losses of the gate driver need to be known.

There are two kinds of loss contributors:

- Static losses P_{static}
- Dynamic switching losses $P_{switch} = P_{rds,on} + P_{rds,off}$

The static losses can easily be calculated by referring to the chapter “Electrical characteristics power supply current consumption” in the datasheet. Note that on the primary side the current consumption on VCC1 is also given for the conditions of TON = high and TON = low, to accommodate for the additional consumption of the coreless transformer that transmits the PWM signal.

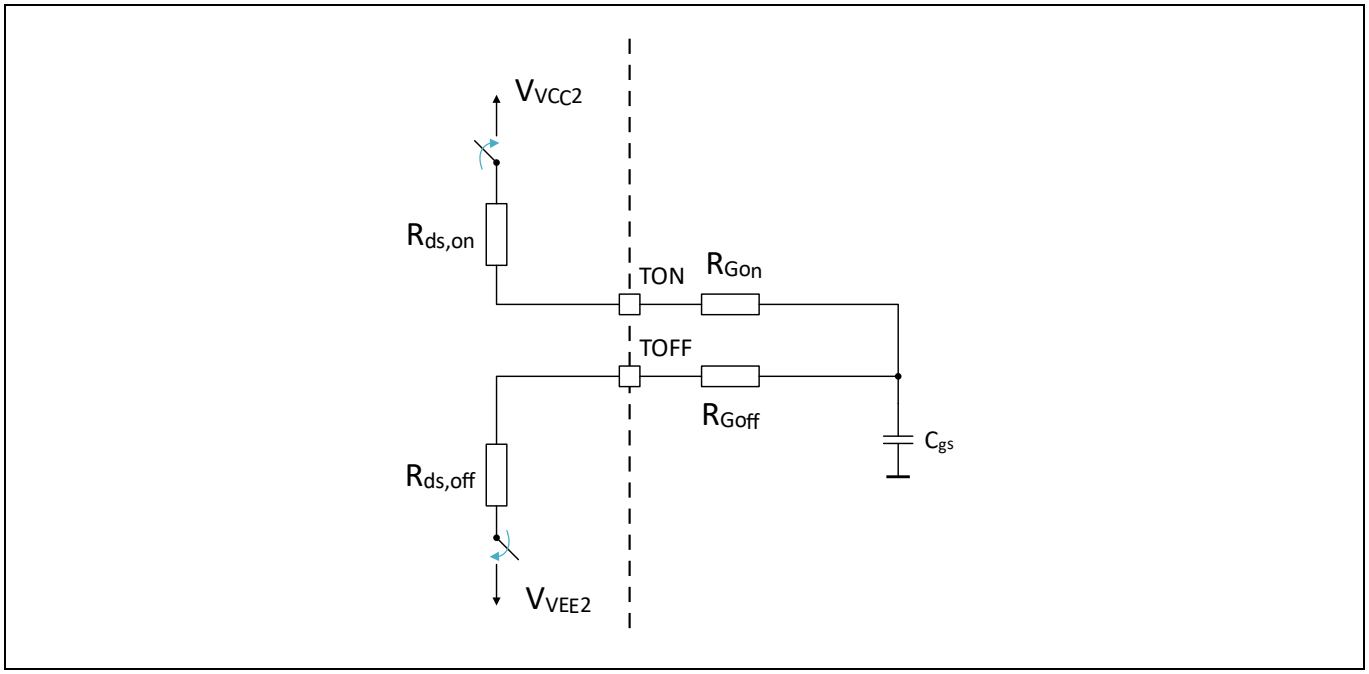


Figure 9 Electrical model for loss calculation in the output stage

The dynamic switching losses are traded-off between the gate driver power stage and the external gate resistors. A formula for the internal switching losses can be found in the Laplace-domain, due to the impulsive nature of the gate currents.

$$P_{rds,on} = \frac{1}{2} f_s C_{gs} (V_{VCC2} - V_{VEE2})^2 \frac{R_{ds,on}}{R_{ds,on} + R_{g,on}}$$
$$P_{rds,off} = \frac{1}{2} f_s C_{gs} (V_{VCC2} - V_{VEE2})^2 \frac{R_{dsoff}}{R_{ds,off} + R_{g,off}} \quad (2\text{-}4)$$

It is often more convenient to rewrite the formula to accommodate for the gate charge:

$$P_{rds,on} = \frac{1}{2} f_s Q_{gs} (V_{VCC2} - V_{VEE2}) \frac{R_{ds,on}}{R_{ds,on} + R_{g,on}}$$
$$P_{rds,off} = \frac{1}{2} f_s Q_{gs} (V_{VCC2} - V_{VEE2}) \frac{R_{dsoff}}{R_{ds,off} + R_{g,off}} \quad (2\text{-}5)$$

The losses in the output stage increase with switching frequency and the applied voltage difference.

For a worst-case calculation insert the combined resistance of the TON RDSON for $R_{ds,on}$ and the TOFF RDSON for $R_{ds,off}$.

The total losses, consisting of the sum of P_{static} and P_{switch} can then be used to estimate device self-heating according to (*2-3*).

2.3.5 Miller clamping losses

The calculation of this loss contributor varies between which driver variant is used. For all variants with an internal active Miller clamp the RMS current into the GATE/CLAMP needs to be measured and then used with the Miller clamping resistor to calculate the losses

$$P_{clamp,internal} = \left(I_{CLAMPL,rms}\right)^2 \cdot R_{DSON-CLAMP} \quad (2\text{-}6)$$

.

2.3.6 Transient thermal behavior

Novel inverters implement the so called Active Discharge functionality that uses the inverter full bridge to conduct either a regular or even emergency discharge of the DC link capacitor when hazardous voltages need to be avoided. Various strategies exist to implement Active Discharge, which are out of scope for this application note. The thermal implications will however be described in this chapter.

During Active Discharge the switching frequency of the gate driver can increase above the regular inverter operating switching frequency for a very limited time duration. Typical Active Discharge scenarios last from one to a couple of seconds. This increased switching frequency causes elevated losses. Since the thermal inertia of the gate driver spans into this range of the “Active Discharge” duration a calculation of this scenario with the static thermal resistances of chapter 2.3.1 would lead to a significant over estimation of gate driver self heating. A more precise result can be obtained by calculating the response from the transient model.

The transient thermal impedance $Z_{th,ja}$ must be used instead. The $Z_{th,ja}$ characteristic is derived by applying the measurement principle shown in Figure 10.

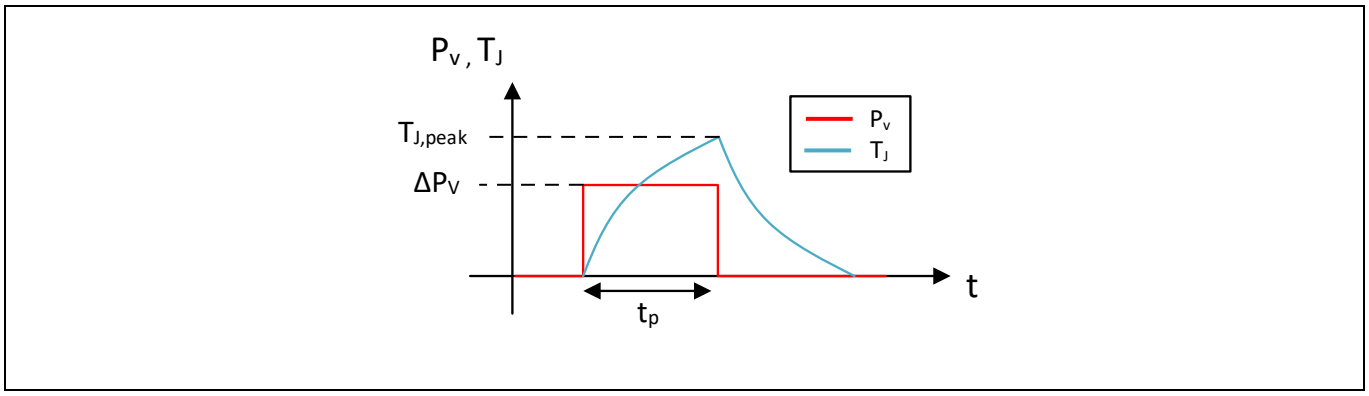


Figure 10 Measurement of the transient thermal impedance

The power source is turned on for the pulse duration t_p and the peak junction temperature $T_{j,peak}$ is determined. The transient thermal impedance is then given as

$$Z_{\mathrm{th,ja}}(t_p) = \frac{T_{\mathrm{j,peak}}(t_p)}{\Delta P_V} \qquad (2\text{-}7)$$

. The simulation result of a complete pulse sweep is given in Figure 11. Note that for high pulse durations the transient thermal impedance converges to the static $R_{th,ja}$ value which is also given in the datasheet.

$$R_{\mathrm{th,ja}} = \lim_{t_p \to \infty} Z_{\mathrm{th,ja}}(t_p) \qquad (2\text{-}8)$$

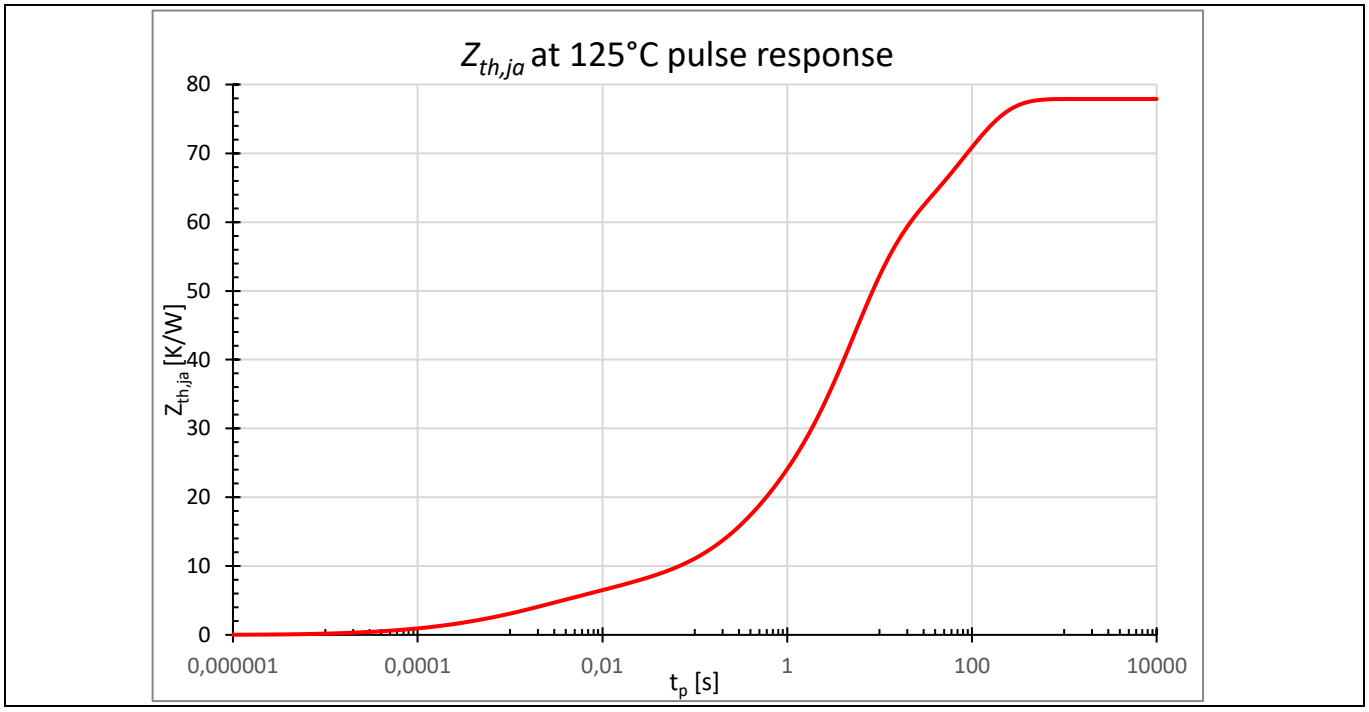


Figure 11 Transient thermal impedance response for 1EDI303xAS, 1EDI302xAS series

2.3.6.1 Calculation example

The following example shows how to use the data from Figure 11 to calculate the maximum junction temperature during an Active Discharge scenario.

The following power profile is assumed:

- Total gate driver losses during normal switching operation $P_{v,norm}$ = 600mW
- Totel gate driver losses during active discharge operation $P_{v,discharge}$ = 1W
- Active discharge duration 3 seconds
- Ambient temperature T_a = 80°C

The scenario is also shown in Figure 12.

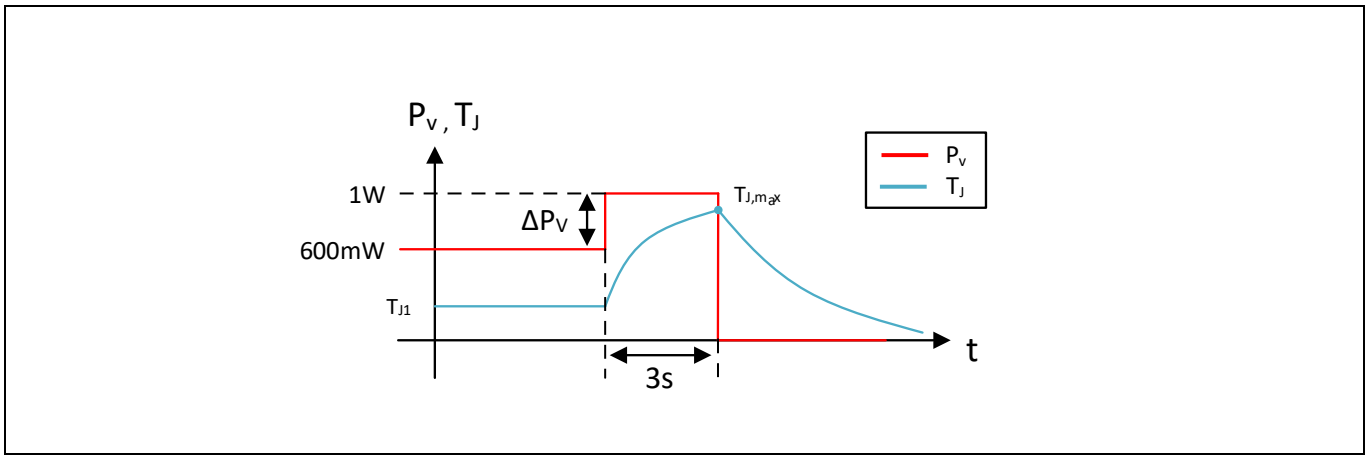


Figure 12 Power and temperature profile example

The initial gate driver temperature T_{J1} can be calculated from the static $Z_{th,ja}$ value which is identical to the $R_{th,ja}$ as

$$T_{j,1} = 600\text{mW} \cdot R_{th,ja} = 600\text{mW} \cdot 78\frac{°C}{W} + 80°C = 126°C \quad (2\text{-}9)$$

. The first step for calculating the peak junction temperature T_{J1} is to determine the corresponding $Z_{th,ja}$. According to Figure 11 the thermal impedance associated with a 3s pulse is approximately 35 K/W. This yields

$$T_{j,max} = 400\text{mW} \cdot 35\frac{°C}{W} + T_{j,1} = 400\text{mW} \cdot 35\frac{°C}{W} + 126°C = 140°C \quad (2\text{-}10)$$

. The result shows that the maximum junction temperature will remain below the permissible absolute maximum temperature of 150°C. Note that the result of a calculation using only the static $R_{th,ja}$ would yield a junction temperature of 158°C and therefore violate the absolute maximum ratings.

It is therefore emphasized that for transient loads the usage of the transient thermal impedance is imperative to obtain precise results.

2.4 Electrical insulation

It is a key feature of the EiceDRIVER™ gate driver to provide galvanic insulation between the primary low-voltage and secondary high-voltage side.

This insulation is first of all required from a **functional perspective**, to allow switching the driver when the secondary GND is floating up and down versus the primary GND due to switching operation.

From a **safety perspective** the insulation is required to prevent exposure of the user from hazardous voltages.

Disclaimer: information provided in this chapter must not be seen as guidance for the system integrator in any means. Please consult proper parties for high voltage safety coordination when in doubt.

2.4.1 Insulation component standard IEC 60747-17 (VDE 0884-17):2021 -10

This newly released standard summarizes the terminology, ratings and measurement methods as well as the principles and requirements of insulation and isolation characteristics applied to magnetic couplers. The EiceDRIVER™ gate driver 1EDI3025AS, 1EDI3026AS and 1EDI3035AS family states the compliance to this standard in the datasheet and delivers the mandatory electrical parameters in the form of a table.

Electrical insulation is basically dealing with two key topics in various combinations:

- Applied voltage waveforms
- Time scale and repetition rate

Important to keep in mind

This standard is not specifically automotive, it is therefore written in a more general form and under the assumption that the insulating coupler may also be connected to the mains.

This implies that the insulating coupler needs to withstand voltage irregularities associated with the mains, such as:

- Temporary overvoltage
- Lightning induced power surges

In particular the standard refers only to AC voltages, whereas it is assumed that any form of DC voltage or “chopped” DC voltage is covered by AC.

2.4.1.1 Reinforced and basic insulation

The most common terms used in conjunction with the word insulation are most likely “**reinforced** and **basic**”. Both types of insulation provide a safeguard against electric shock.

The difference is that reinforced insulation is more stringent than basic insulation, since reinforced insulation “provides a degree of protection against electric shock equivalent to double insulation”. The term double insulation is referenced from IEC 60664-1, whereas it is described as a form of basic insulation combined with supplementary insulation. Supplementary insulation is another **independent** insulation applied in addition to basic insulation. The key word here is “**independent**”, which implies also that both “layers” of insulation in supplementary insulation are independently testable from each other. This can be easily achieved in most home appliances, such as for example an electrical hedge drimmer or electric drill.

For integrated magnetic or capacitive couplers however this is no longer applicable, since the assembly is intertwined through various passivation layers and the package mold compound. Therefore, the term “**reinforced insulation**” was introduced and test procedures are described on how to achieve this rating. The

test and qualification flows are identical to "**basic insulation**" but tougher targets need to be achieved. For example in the form of higher testing voltages or higher life-time margin and stricter derating factors.

2.4.1.2 Voltage definitions

Several voltrage rating are defined in the standard, that the system integrator needs to map to their application conditions. This section summarizes their definition:

Table 2 Overview of rated voltages

Symbol	Extended description	Justification
V_{IORM}	"Maximum rated repetitive peak isolation voltage" Peak value of an AC sinusoid	Withstand voltage over entire product life-time from TDDB test – see standard for details
V_{IOTM}	"Maximum rated transient isolation voltage" Peak value of an AC sinusoid	Withstand voltage for 60 s , 100% of voltage rating during sample test, 120% of voltage rating during production test but for 1 s
V_{IOSM}	"Maximum surge insulation voltage" Peak value of a defined surge pulse waveform – see standard for details	50 discharges with different polarity – see standard, tested in oil to prevent flash-over
V_{IMP}	"Maximum impulse voltage" Peak value of a desfine surge pulse waveform – see standard for details	Highest allowable voltage without flash-over or internal break-down. Derived from V_{IOTM} and V_{IOSM}

The voltages depicted in Table 2 cover the isolation characteristic over a remarkable time-span of 14 magnitudes. This time-span is ranging from microseconds up to multiple decades and are shown in Figure 13.

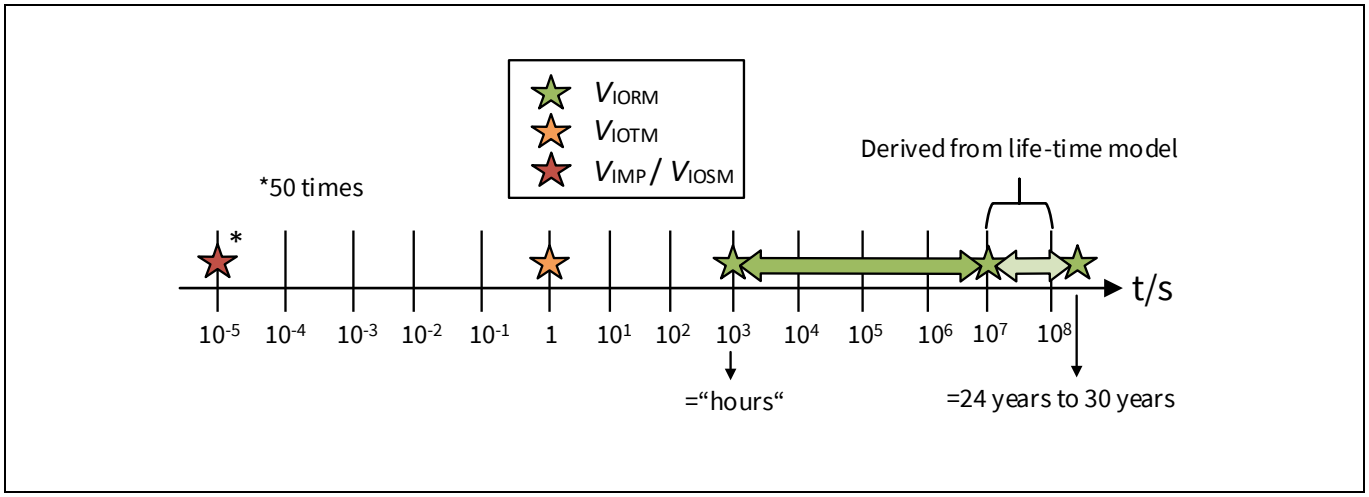


Figure 13 Illustration of the applicable time-scale to the rated voltages

While V_{IOSM} and V_{IOTM} can be completely covered by direct measurement, due to their instantaneous definition, V_{IORM} covers the complete life-time of the isolation barrier. This life-time, according to the standard, is **24 years for basic insulation** and **30 years for reinforced insulation**. Since it is not feasible to conduct a measurement for this long, a TDDB model (Time Dependent Dielectric Breakdown) is created in order to prove the expected

isolation barrier lifetime. The model is based on “end of life” data that is collected from a couple of hundred device’s that are exposed to an AC sinusoid voltage of varying magnitude. The rules for model creation are strictly stated in the standard. The model has to include a data-point where the device life-time is proven to be higher than 10^7 s, together with a ppm rate of either 1 ppm (reinforced) or 1000 ppm (basic). Life-time beyond this point is based on interpolation together with a number of derating factors to ensure coverage for V_{IORM}.

2.4.2 Insulation component standard UL1577

This standard was mainly created for opto-coupler based isolators. When applied to products employing magnetic insulation principles, such as the EiceDRIVER™ gate driver, a single test has to be carried out:

- Dielectric voltage-withstand test

For the dielectric voltage-withstand test a couple of devices with thermal or humidity preconditioning are exposed to the rated AC rms voltage for 60 seconds plus an additional ramp-down and ramp-up time. This test procedure is similar to the procedure applicable to V_{IOTM} in IEC 60747-17. Both UL1577 and IEC 60747-17 require a production test for this voltage. It can be carried out for 1 s when 120% of the rated voltage is applied.

2.4.3 Advantages of IEC 60747-17 over UL1577

While both insulation standards are popular internationally, it has to be outlined that there is a substantial difference between them. Namely, IEC 60747-17 specifically accounts for additional parameters to satisfy higher system level standards such as IEC 60664-1. It also incorporates learnings about the physical break-down of insulation barriers due to aging effects and demands these effects to be accounted for in the TDDB model. A further advantage is the strict definition of production test methods for defect screening, such as partial discharge testing.

Table 3 Comparison of UL1577 to IEC60747-17

	UL1577	IEC 60747-17
Temporary overvoltage	X	X
Surge	—	X
Isolation resistance	—	X
Partial discharge	—	X
Life-time at withstand voltage	—	X
Creepage and clearance	—	X
CTI	—	X
Periodic monitoring	—	X
Production test	(X) only for overvoltage	X combining partial discharge and overvoltage

For the system integrator it is therefore advantegous to consider IEC 60747-17 as a “must have” on the requirement list, especially with regards to high-voltage safety in xEVs.

2.5 Implications of primary and secondary chip concept

The EiceDRIVER™ gate driver is actually two products in one package. The gate driver is comprised of two separate chips. One on the primary side and one on the secondary. This concept is implied from the insulation requirements described in chapter 2.4 to enable a galvanic separation between the high voltage and low voltage domain.

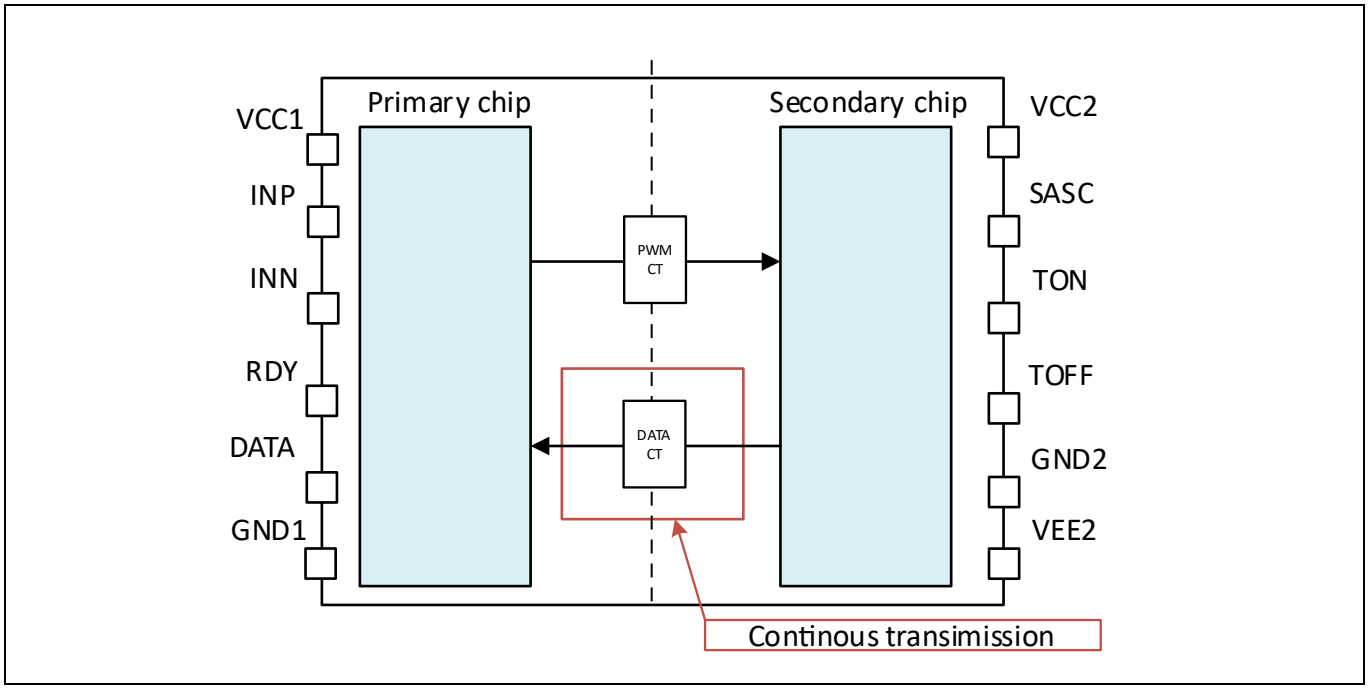


Figure 14 EiceDRIVER™ gate driver – internal chips and CTs

Each of the two chips is supplied separately and independently:

- VCC1, GND1 on the primary chip
- VCC2, VEE2, GND2 on the secondary chip

The communication between both chips is done through coreless transformers (CTs). There is one CT for PWM signal transmission from the primary to the secondary chip. A second CT is used for digital DATA transmission from the secondary to the primary chip.

Through the DATA transmission the primary chip is able to read the status of the secondary chip, but not the other way round. In case the primary chip fails or powers down, the PWM CT transmission is simply deactivated and the the output stage turns-off on the secondary.

The triggering of a protection mechanism on the secondary chip is reported to the primary and then reflected in the state of the following pins for immediate feedback:

- NFLT – mapped to OCP or DESAT event
- RDY – mapped to
    - Output stage errors: OSM error, GATEMON error
    - Power supply monitoring: UVLO1, UVLO2, OVLO2, UVLO3, OVLO3
    - Internal supervision: primary and secondary
    - Life sign error
    - STP keep error

Despite all events being reported to the primary, the reaction to these events mostly takes place on the secondary chip and will therefore also be carried out when the primary is unpowered.

Only the following events are handled on the primary chip:

- UVLO1
- Shoot through protection
- Life sign error
- Internal supervision primary

The “life sign error” is a special error also leading to “RDY going low”. The DATA transmission through the digital CT also carries information that enables the primary chip to identify whether the transmitted data is valid or not. Should the data be indentified to be corrupted for a certain number of frames or even no frame be received within a specific time period the primary chip raises the so called “life sign error”.

This error can be understood as the last resort to a lost connection from the secondary chip. With the raising of a life sign error the PWM CT is automatically turned off. A permanent loss of life sign is also visible in the external DATA interface, since the “no life sign established” bit will be set to 0.

Since the communication link from the secondary is broken during a “life sign error” it also means that the events reflected in the DATA interface are possibly outdated or incomplete.

This makes the recovery on system level somewhat tricky. In order to clear the life sign error, like any other error, the gate driver needs to be transitioned from “PWM disable” into “PWM enable” as explained in chapter 3.9.1. Should the “life sing error” be persistent the clear will not be successful and RDY will stay “low”. There will however not be any updated information in the external DATA interface, since the connection to the secondary chip is still not established.

Life sign errors may also occur when the PCB design is not optimized to reduce EMC induced noise. While the CT transmission is extremely robust due to its extremely small coil loops, the secondary chip may pick-up noise that results in a corrupted or missing internal DATA frame. For tips on how to improve noise performance refer to chapter 5 “Layout optimization”.

2.5.1 Power-up and initilization

When powering-up the EiceDRIVER™ gate driver the voltage on the secondary side is usually not precisely known. It is imperative to understand that the gate driver will not be able to enter PWM Enable and assert RDY = “high” unless there is no pending error on the secondary chip, such as a power supply monitoring errors.

To ensure a correct intilization the following power-up strategy is recommended:

- Apply VCC1, VCC2, VEE2
- Check VCC1 > UVLO1 by monitoring DATA output – if no output then device is in Primary_Init
- In the DATA diagnostics frame check whether “bipolar detection warning” is expected to be set or not after the maximum VCC2 and VEE2 ramp-up time – this is only applicable for variants 1EDI3025AS, 1EDI3026AS, 1EDI3035AS
- Try to transition into PWM_Enable mode
- Observe RDY pin – if RDY pin goes “high” the device is properly powered up
- If RDY pin stays “low” check whether any error or warning bit is set in DATA
- If the “no life sign established” bit is set the secondary side could not be supplied at all

3 Specific product features

3.1 Operating modes

The EiceDRIVER™ gate driver implements a state-machine to distinguish between several different operating modes. An example of all the operating modes in this state-machine is shown in Figure 15.

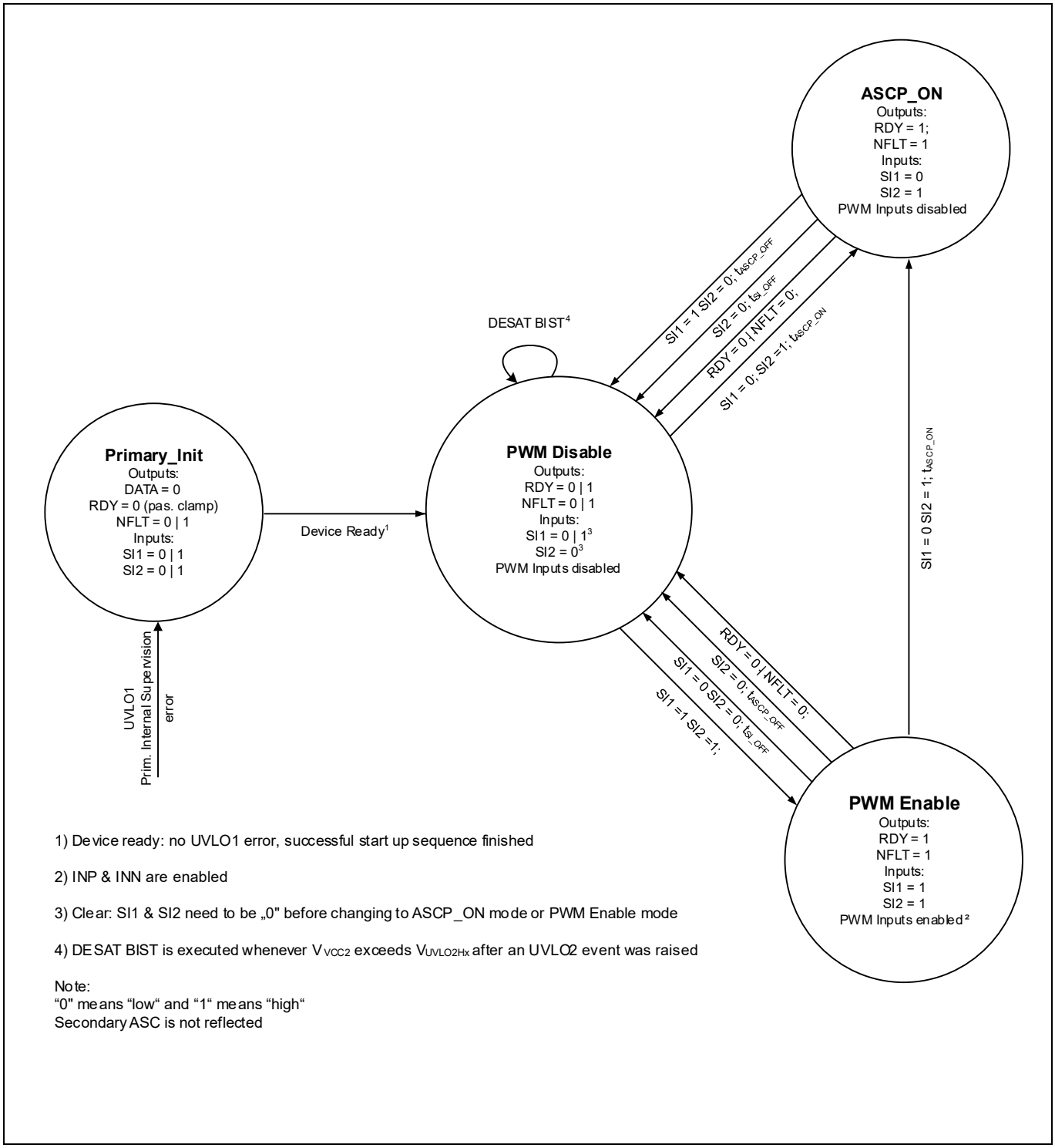


Figure 15 Operating mode example of 1EDI3035AS

A transition between states can be caused by the system integrator or by an external event:

- Actuation of the SI1, SI2 pins
- Error event that causes RDY or NFLT to go low – see datasheet for a complete list of these events
- Undervoltage event on the primar or secondary side

For details about operating mode transitions through SI1 and SI2 see chapter 3.9.1.1.

3.2 DATA read-out via PWM coding

Intrusive diagnostics and ADC readback functionality is provided on the DATA pin. The binary data is coded in the duty cycles of repeating unique identifiable pattern. An attached microcontroller, such as the AURIX™, can measure the duty cycle by the means of two timers in “capture and compare” mode. The pattern is shown in Figure 16.

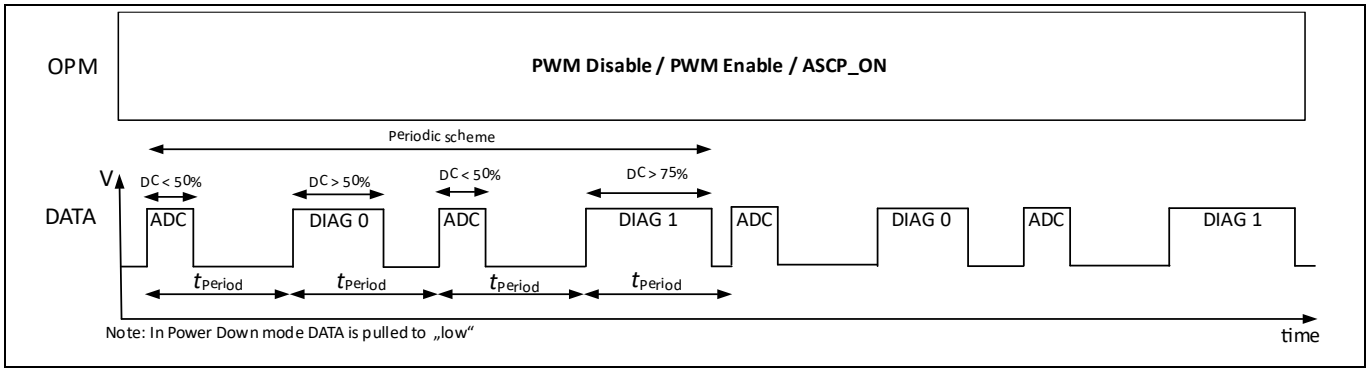


Figure 16 Alternating DATA read-out pattern

There is a total of three different frame types:

- DIAG0
- DIAG1
- ADC

Each frame can be uniquely distinguished based on the possible duty cycle range. The ADC frame’s duty cycle is always smaller or equal to 50%. Whereas DIAG0 is always greater than 50% but smaller than 75% and DIAG1 is always greater than 75%.

The two diagnosis frames are shown in Table 4 and Table 5 respectively. For a diagnosis frame bit 12 is always set. Bit 11 is either 0 for DIAG0 or 1 for DIAG1.

Table 4 DIAG0 frame

bit	12	11	10	9	8	7	6	5	4	3	2	1	0
Description	1 = DIAGx	0 = DIAG0	SASC activation warning	Bipolar detection warning 1)	UVLO3 error	OVLO3 error 1)	UVLO2 error	OVLO2 error	No life sign established	1	0	0	0

1) “0” for 1EDI3038AS and 1EDI3028AS

Table 5 DIAG1 frame

bit	12	11	10	9	8	7	6	5	4	3	2	1	0
Description	1 = DIAGx	1 = DIAG0	SASC activation warning	No Desaturation BIST warning	Desaturation detection error	Gate monitoring error	Output stage monitoring error	STP keep error	Dead time warning	1	0	0	0

Table 6 ADC frame

bit	12	11	10	9	8	7	6	5	4	3	2	1	0
Description	0 = ADC	ADC MSB	x	x	x	x	x	x	x	x	x	x	ADC LSB

The ADC resolution is 12 bits (bits 0 to 11). This means that in the ADC frame bit 12 is always zero. Table 7 shows the decimal and duty cycle ranges of the DIAG1, DIAG0 and ADC frame as they are resulting from the previous bit patterns. Given these ranges, it is at any time possible for a microcontroller to distinguish and identify each individual frame in the pattern by applying the following logic:

- A DIAG1 frame's duty cycle is always greater than 75%
- After a DIAG1 frame, there is an ADC frame
- After the ADC frame "after" the DIAG1 frame there is a DIAG0 frame

Table 7 Frame decimal range

frame	DIAG1	DIAG0	ADC
range	6152 … 8184	4104 … 6136	0 … 4095
normalization	$2^{13} = 8192$		
Duty-Cycle range	75% … 99.8 %	50% …74.8%	0 … 49.99%

The equivalent time of one LSB is given by the "ADC DATA period" and can be calculated as 204 µs/2^13 ~ 25 ns. In order to distinguish DIAG0 from DIAG1, according to Table 7 it is necessary to detect a difference of 17 LSBs between them under worst-case conditions. This is equivalent to a time difference of 16 LSBs * 25 ns = 400 ns.

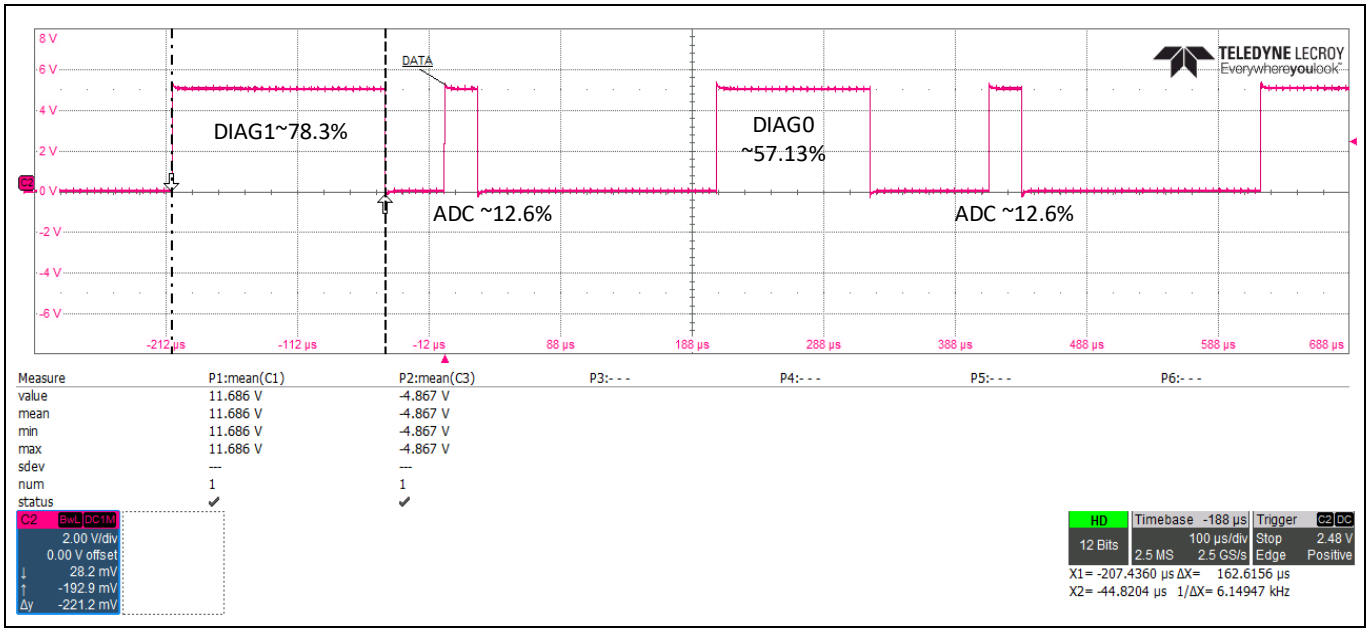


Figure 17 DATA frame output example

An example waveform of the DATA frame was captured in Figure 17. The duty cycles can be measured by freezing the waveform to a single trigger and by measuring the timings with the cursors. The procedure is straight-forward but also prone to errors since the cursors need to be manually placed, which can easily lead to reading errors in the lower bits (= less numeric significance).

From the example in Figure 17 the driver status can be determined as follows:

- DIAG1 = 78.3% * 2^13 = 6414d = 1100100001110b
- DIAG0 = 57.13% * 2^13 = 4680d = 1001001001000b
- ADC = 12.6% * 2^13 = 1032d
- Vadc ~ 12.6% * 3.5 V * 2 = 0.882 V

The lower 4 bits are assumed to be do not care due to the inaccuracy in reading the width from the oscilloscope.

Comparing DIAG1 with Table 5 shows that Bit8 = desaturation detection error is set.

Comparing DIAG0 with Table 4 reveals Bits 9 and 6 are set, indicating that “bipolar detection warning” is active and an “OVLO2” error occurred.

3.2.1 Differentiating error and warning bits

The datasheet classifies the bits in the DATA output into the following categories:

- Warning bits
- Error bits
- No life sign established bit

The “no life sign established bit” is actually neither a warning nor an error bit. It shows the instantaneous status of the life sign. More information about the concept of life sign and its implications are given in chapter 2.5 “Implications of primary and secondary chip concept”.

Error bits are reflecting events that cause the gate driver to transition into “PWM Disable” mode. The full list of events and reactions are summarized in the datasheet. Error bits are considered to be “sticky”. They can only be cleared by a transition from “PWM Disable” to “PWM Enable” using SI1 and SI2 pins and given that the cause of error is gone. For more information see chapter Operating modes.

Warning bits are reflecting events that give additional status information to the system integrator. These events do not imply a status change in the gate driver’s operating mode. **Warning bits** are “non sticky”. They clear themselves automatically when the cause of the warning is cleared. When a warning bit is set, the DATA frame is always output at least once to ensure observability for events that are shorter than a DATA cycle period.

3.2.2 System considerations on DATA signal readout

The DATA signal is output from a fast I/O pad and achieves rise- and fall-times in the range of 13 ns. An attached microcontroller samples the DATA signal and calculates the duty cycle thereafter. The effectively sampled pulse width differs from the externally applied signal, due to the micrcontrollers receiver characteristic.

This situation is depicted in Figure 18. The figure shows that whenever the DATA signal's rise and fall times t_{rise} and t_{fall} are similar, the idealized DATA output can be recovered by sampling the signal at a 50% threshold.

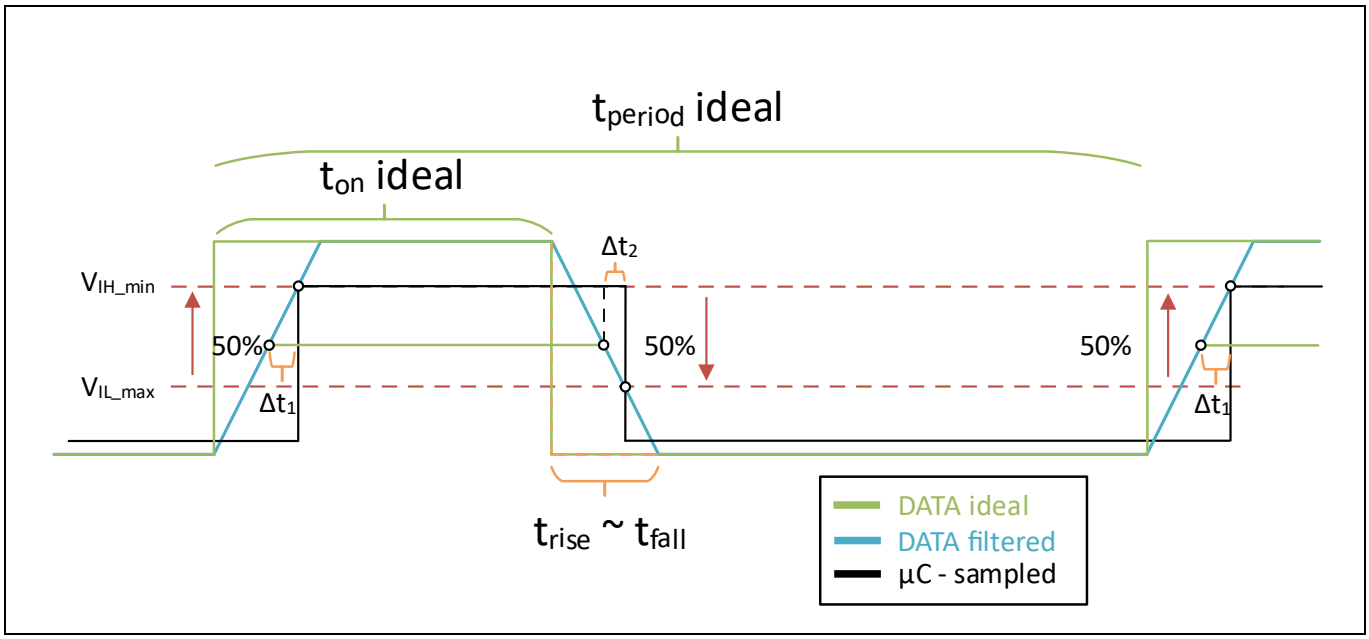


Figure 18 DATA signal and signal samples by microcontroller comparison

A typical microcontroller receiver is however not achieving this sampling threshold, especially because there is a hysteresis added to the receiver. For a first worst-case assumption the logic level V_{IH_MIN} and V_{IL_MAX} are assumed for the calculation.

For the following example TTL logic levels are given as:

- V_{IH_min} = 2.0 V
- V_{IL_max} = 0.8 V
- 5 V peak voltage

The timing diviations from the ideal sampled signal can be calculated as

$$\Delta t_1 = \frac{(50\% \cdot 5\,V - V_{IH_MIN})}{5\,V} t_{rise}, \qquad \Delta t_2 = \frac{(50\% \cdot 5\,V - V_{IL_MAX})}{5\,V} t_{fall} \tag{3-1}$$

. The DATA signal rise and fall time can be measured and is given to be approximately 13 ns. Using the formula yields

$$\Delta t_1 = \frac{(2\,V - 50\% \cdot 5\,V)}{5\,V} 13\text{ ns} = +1.3\text{ ns},\ \Delta t_2 = \frac{(50\% \cdot 5\,V - 0.8\,V)}{5\,V} 13\text{ ns} = +0.42\text{ ns} \tag{3-2}$$

This means that the total deviation from the ideal DATA signal on-time is given as 1.72 ns. The positive sign indicates that the samples DATA signal appears to be extended by 1.72 ns for the microcontroller versus the idealized DATA output. The DATA period appears to be extended by two times Δt_1. The “total” timing error can therefore be given as approximately 2*1.3 ns + 1.72 ns ~ 5 ns. The timing difference between “1 LSB” in the DATA signal is given as t_{period} / 2^13 ~25 ns.

This calculation shows that the DATA interface is perfectly suitable to provide 12 bit resolution for the ADC data. When in the application it is required to filter the DATA signal, formulas (3-1) and (3-2) can be used to calculate the impact on the signal resolution. The parameters t_{rise} and t_{fall} have to be adjusted accordingly.

3.3 Power supply monitoring

The EiceDRIVER™ gate driver implements an advanced voltage monitoring feature for the primary and secondary supply voltages VCC1, VCC2 and VEE2 according to Table 1.

The voltages are monitored by the means of comparators that are configured as Schmitt triggers.

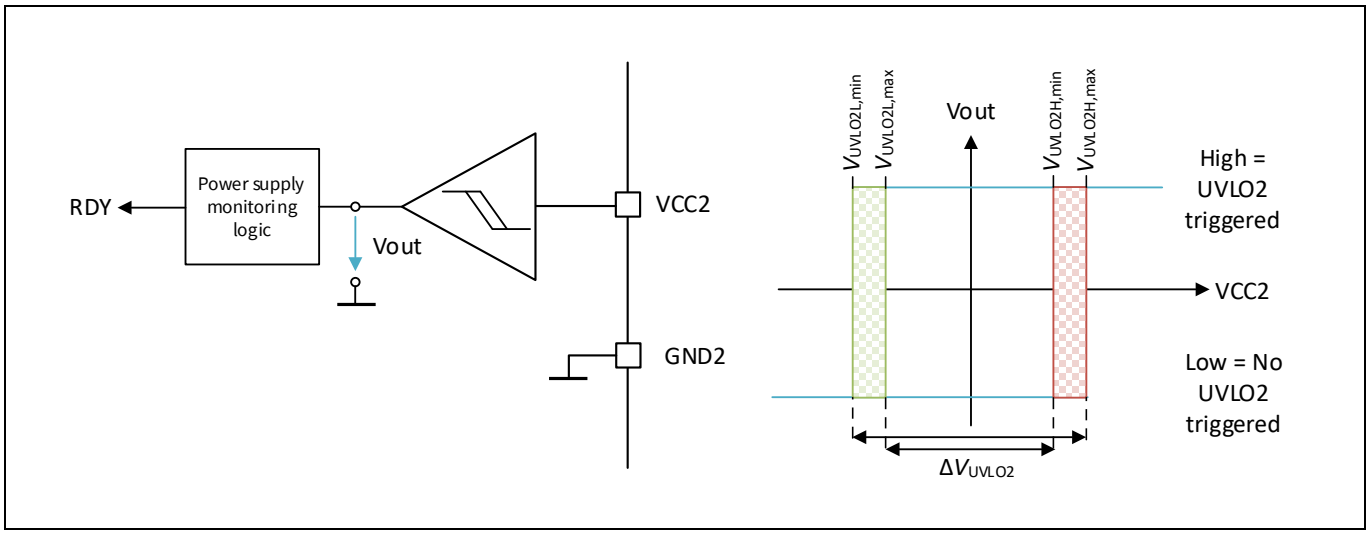


Figure 19 UVLO2 monitor on VCC2 example

Figure 19 illustrates how the datasheet voltage thresholds are mapped to the functionality of a Schmitt trigger. For the output of the monitor to flip, the input needs to cross the respective maximum or minimum thresholds V_{UVLO2H} or V_{UVLO2L}. Note that the hysteresis ΔV_{UVLO2H} is not given in the datasheet but if necessary it can be calculated by hand from the threshold values.

For UVLO1 monitoring the $V_{UVLO1H,min}$ and $V_{UVLO1L,max}$ voltages may even overlap, which is not a contradiction. The reason for the overlap is the tolerance adders from temperature drift and production testing guard-band. In the application the system integrator needs to interpret the values as follows:

- On power-up VCC1 needs to rise above $V_{UVLO1H,max}$ for the primary side to leave UVLO1 = active state
- During normal operating VCC1 shall not reach $V_{UVLO1L,max}$ to prevent an accidental UVLO1 trigger

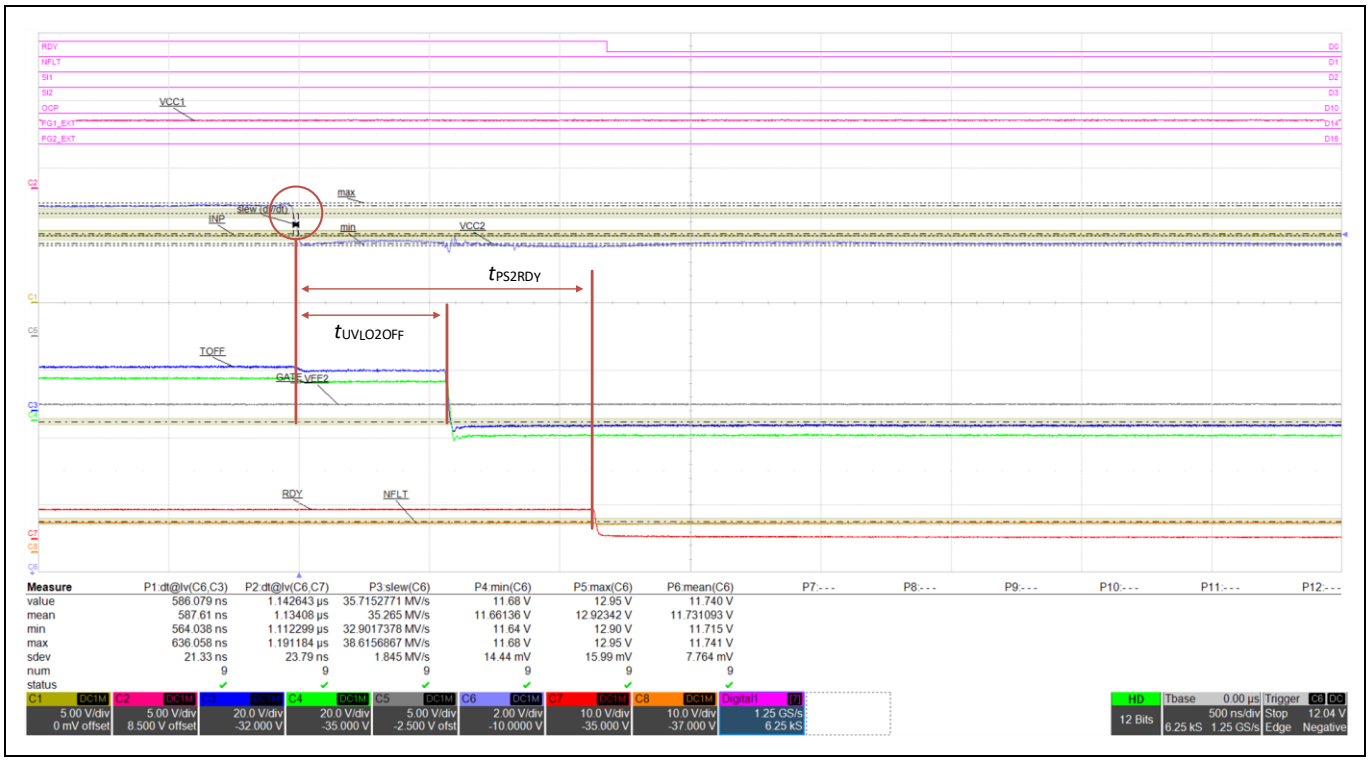


Figure 20 UVLO2 reaction measurement example

For device characterization a step function is generated on the respective supply voltage and the gate driver reaction is observed. An example is shown in Figure 20 where the output stage turns off due to a UVLO2 event.

The “detection and reaction times” for every power supply monitor are given in the datasheet. This time is basically a characterization of the delay of the Schmitt trigger. Note that the conditions state a certain slew-rate and voltage overdrive value since these values impact the timing result. There is no deglitching or filtering added to the power supply monitoring since it directly impacts the time until gate driver turn-off and the indication on the primary side through the RDY pin.

3.3.1 Self learning OVLO3 monitoring

Several products of the EiceDRIVER™ gate driver family implement overvoltage monitoring on the VEE2 voltage rail. For a detailed mapping to enabled variants see Table 1. The OVLO3 monitoring is a self learning feature and prepared to accommodate for both unipolar and bipolar switching applications. Everytime the secondary chip is powered down the OVLO3 monitoring is deactivated by default.

For the monitoring to be activated the V_{UVLO3L} threshold needs to be crossed for the time of $t_{VLO,active}$ for the feature to activate and react accordingly once V_{OVLO3H} is crossed at a later point in time. This principle is shown in Figure 21.

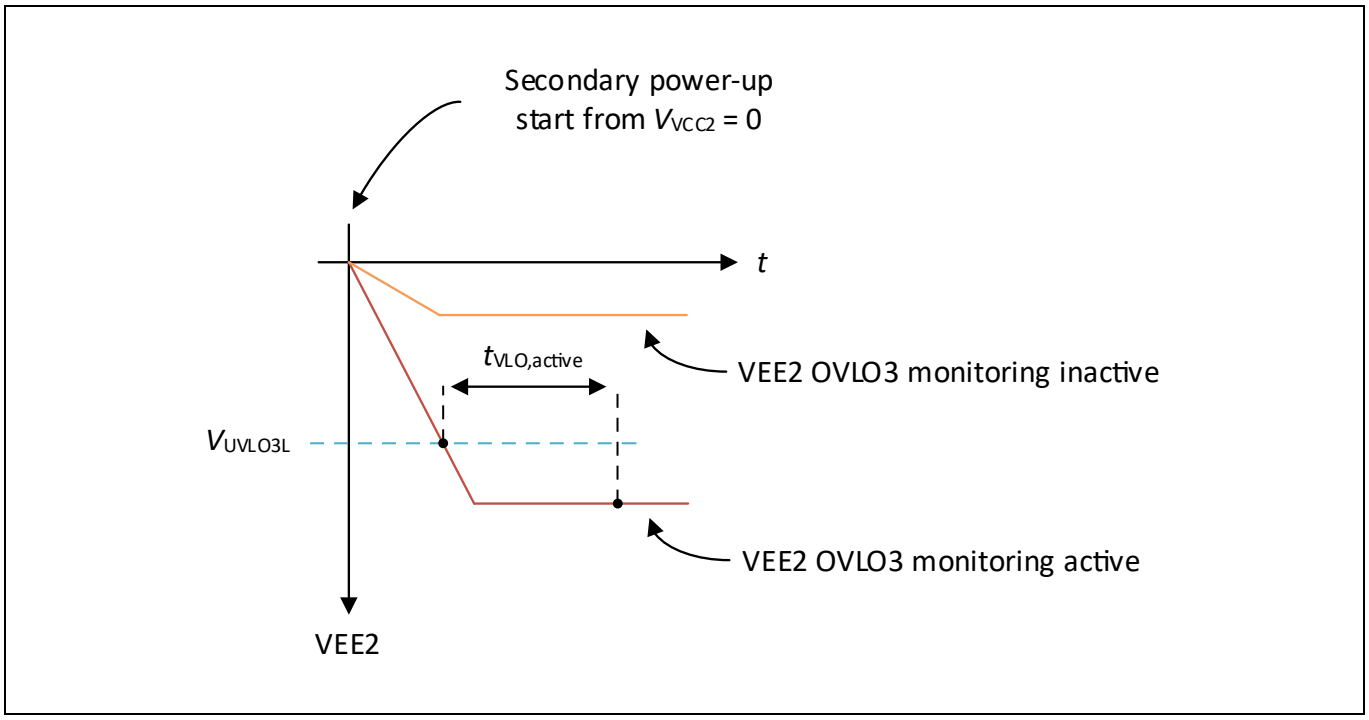


Figure 21 Activation of OVLO3 monitoring illustration

The status of the OVLO3 monitor can be read from the DATA stream through the “Bipolar detection warning bit” in Table 4. The bit is set once the OVLO3 monitor is activated, indicating the presence of a bipolar supply voltage.

3.4 DESAT and OCP protection

The EiceDRIVER™ gate driver family implements an exceptionally fast DESAT and OCP concept with improved detection and reaction times. The basic internal circuit together with a typical external configuration is shown in Figure 22 and Figure 23.

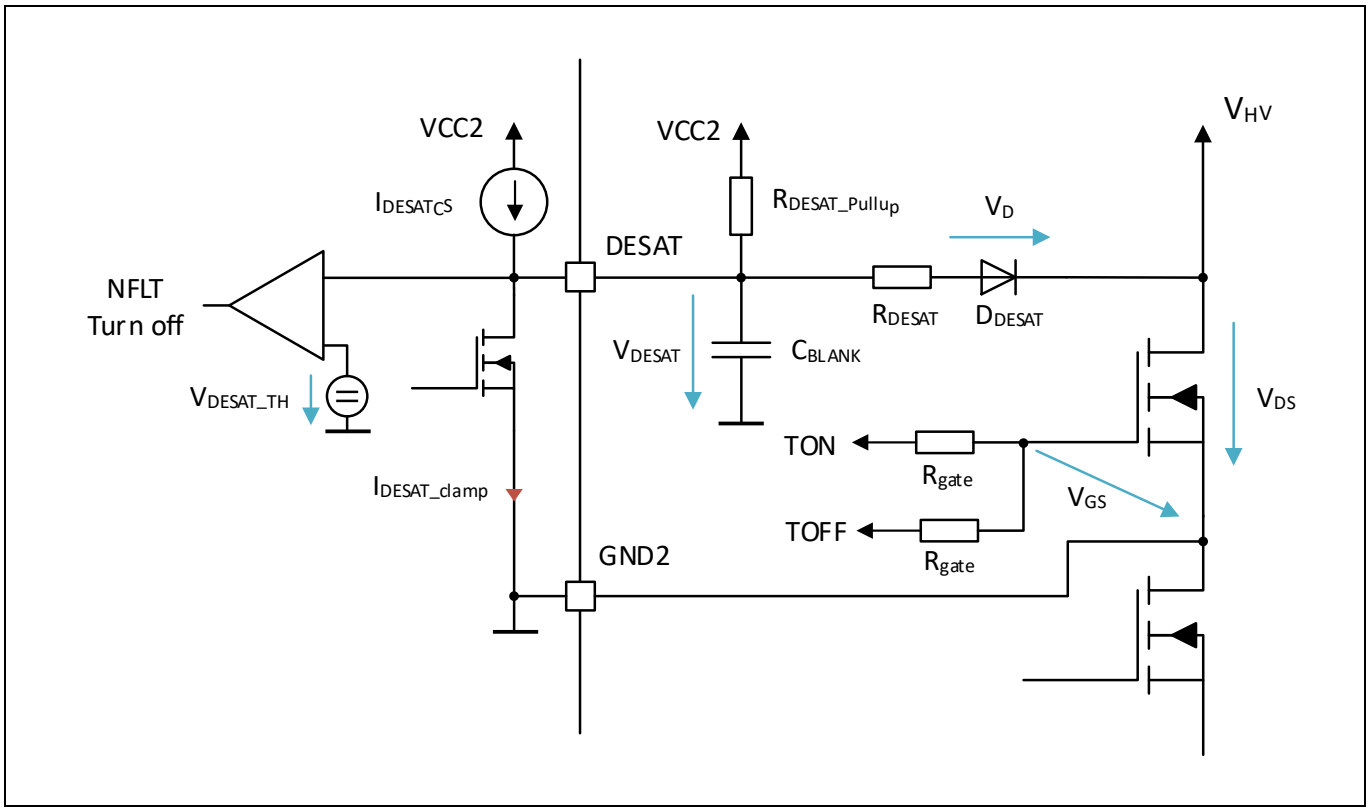


Figure 22 DESAT concept with external components

The DESAT/OCP feature internally consists of the following parts:

- DESAT/OCP current source
- DESAT/OCP clamping transistor
- DESAT/OCP comparator

As long as the received PWM signal on the secondary side is “low”, the clamping transistor is activated and keeps the DESAT/OCP pin node discharged. Upon a transition of this signal from “low” to “high”, the clamp is released after the blanking time t_{OCPBT} or $t_{DESATBT}$ is elapsed.

The DESAT/OCP current source then charges the capacitor C_{DESAT} until an equilibrium is reached together with the external excitation. Under regular switching conditions, the DESAT/OCP comparator is not tripped. In case of a short circuit condition, the DESAT/OCP comparator detects the rising voltage and issues a safe turn-off (1EDI3035AS, 1EDI3025AS, 1EDI3026AS) depending on the product variant. See section Product selection and features for more details.

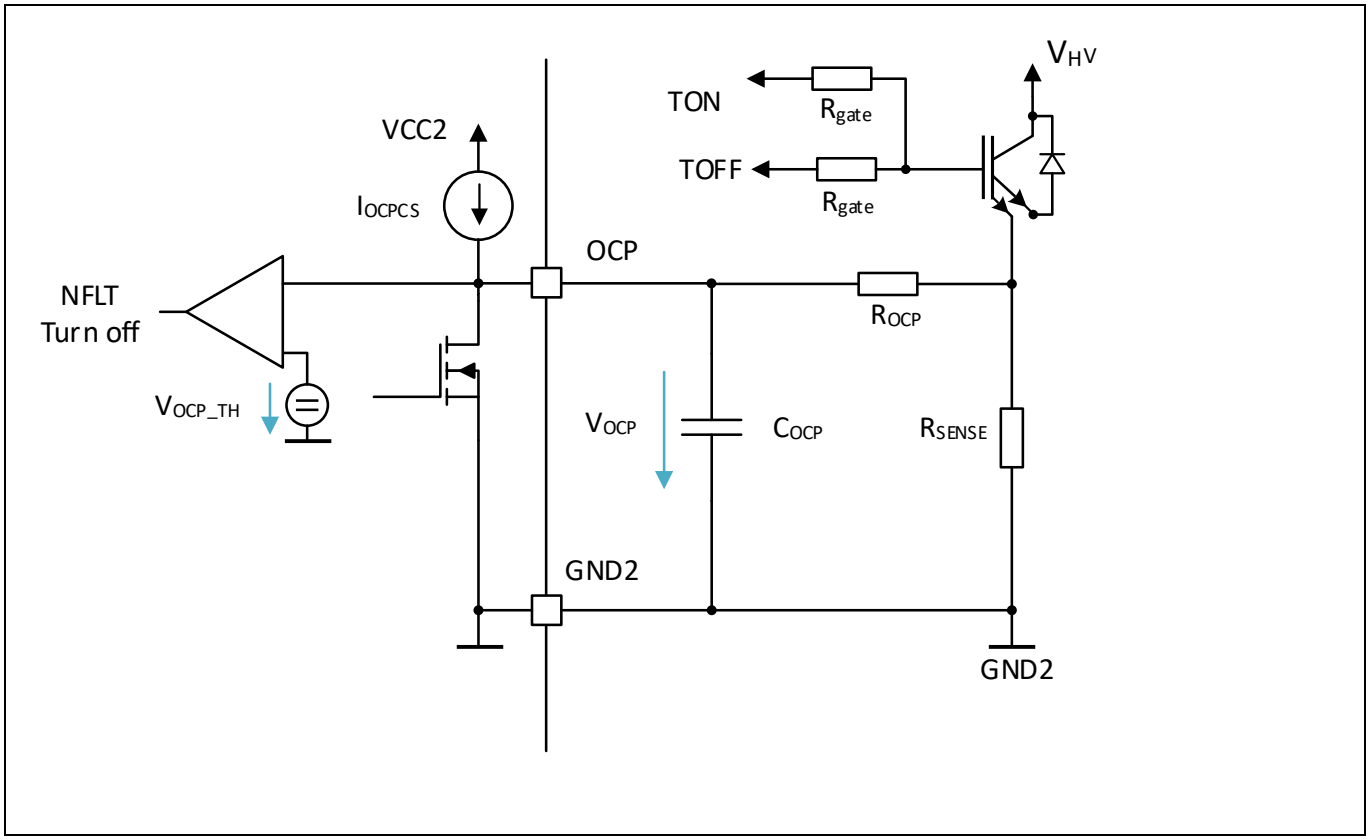


Figure 23 OCP concept with external components

Despite the OCP pin being completely biased by the external current mirror of the IGBT, an additional current source is present inside the gate-driver. It serves the purpose of detecting an “open pin” on OCP by intentionally pulling up OCP voltage and triggering the OCP reaction.

3.4.1 DESAT timing and component calculation

The two possible DESAT timing schemes are shown in Figure 24 and respectively. An overview of all product variants is given in Table 1.

In case a device with soft turn-off capability is used, the complete cycle time from turn-on to device turn-off is given by:

$$t_{\mathrm{on2off}} = \underbrace{t_{\mathrm{DESATBT}}}_{\text{Gate driver}} + \underbrace{t_{\mathrm{filter}}}_{\text{System integrator}} + \underbrace{t_{\mathrm{DESAT2SOFTOFF}}}_{\text{Gate driver}} + \underbrace{t_{\mathrm{SOFTOFF}}}_{\text{System integrator}} \quad (3\text{-}3)$$

. The calculation can be formulated for the OCP protection in a similar fashion. The contribution of the filter time t_{filter} depends on the external circuit and component values. For the DESAT circuit with an external pull-up resistor to VCC2 as shown in Figure 22 it is given by

$$t_{\mathrm{filter}} = C_{\mathrm{DESAT}} R_{\mathrm{DESAT_Pullup}} \cdot \ln\left(\frac{R_{\mathrm{DESAT_Pullup}} \cdot I_{\mathrm{DESATCS}} + V_{VCC2}}{V_{\mathrm{VCC2}} - V_{\mathrm{DESAT_TH}} + R_{\mathrm{DESAT_Pullup}} \cdot I_{\mathrm{DESATCS}}}\right) \quad (3\text{-}4)$$

. When no $R_{\mathrm{DESAT_Pullup}}$ is used (3-5) simplifies to

$$t_{\mathrm{filter}} = \frac{V_{\mathrm{DESAT_TH}} \cdot C_{\mathrm{DESAT}}}{I_{\mathrm{DESATCS}}} \quad (3\text{-}5)$$

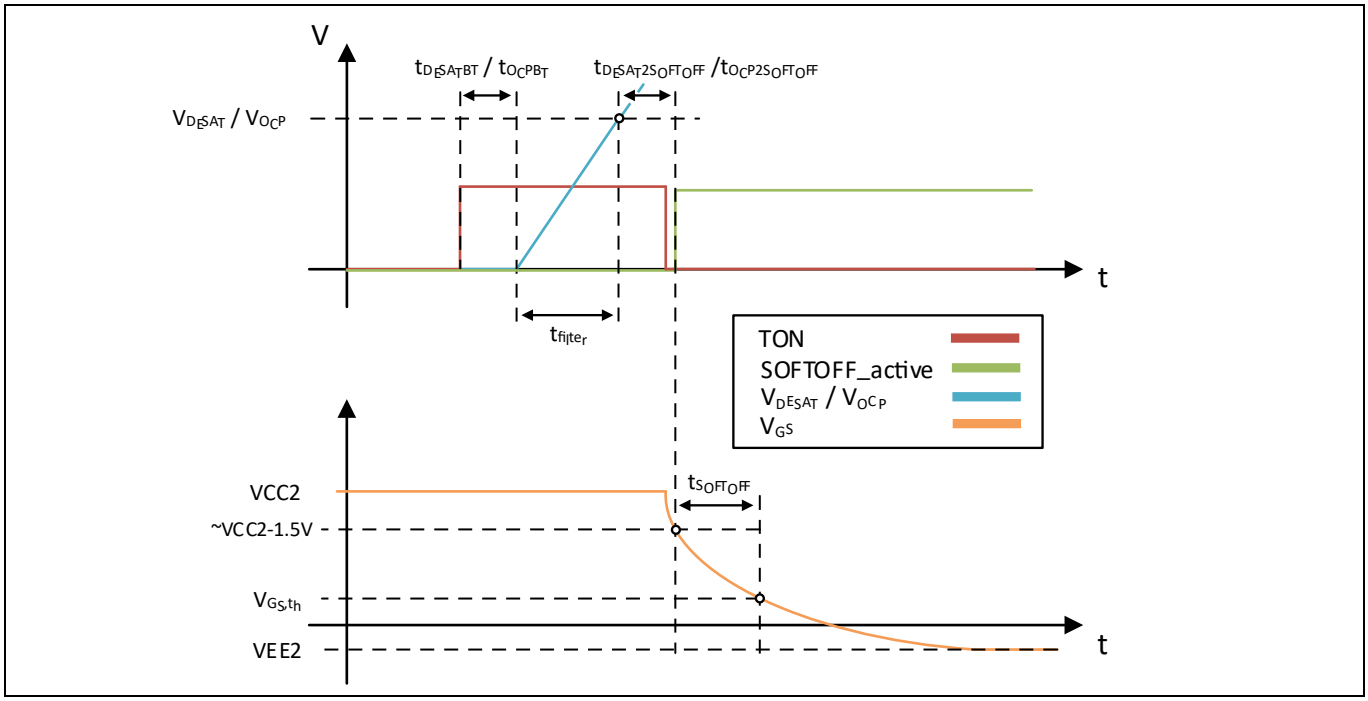


Figure 24 Soft turn-off timing with DESAT or OCP protection

The pull-up resistor R_{DESAT_pullup} also influences the DESAT triggering threshold. The resulting voltage on the DESAT pin V_{DESAT} in steady-state turn-on an be calculated by applying the superposition theorem to be

$$V_{\mathrm{DESAT}} = \frac{1}{R_{\mathrm{DESAT_Pullup}} + R_{\mathrm{DESAT}}} \left[R_{\mathrm{DESAT}} \left(V_{\mathrm{VCC2}} + R_{\mathrm{DESAT_Pullup}} \cdot I_{\mathrm{DESATCS}} \right) + R_{\mathrm{DESAT_Pullup}} \left(V_D + V_{DS} \right) \right] \quad (3\text{-}6)$$

.

According to equation (3-7) the DESAT voltage increases with lower pull-up resistance R_{DESAT_Pullup}, thus when using the circuit configuration of Figure 22 the DESAT triggering threshold decreases. In order to increase the DESAT triggering threshold a more sophisticated circuit as shown in chapter 3.4.2 is required.

Note that R_{DESAT_pullup} also contributes to the current through the internal clamping transistor shown in Figure 22 and to the thermal power dissipation in the gate driver. The capability of this clamping transistor is given by the sink current in the “DESAT low voltage” requirement in the datasheet. This requirement can also be used to estimate the internal losses by applying Ohm’s law for estimating the clamping transistor’s Rdson.

The following example illustrates the impact on the steady-state V_{DESAT} with the following input values:

- R_{DESAT_Pullup} = 10 kΩ
- R_{DESAT} = 1 kΩ
- V_D = 1.1 V
- V_{DS} = 1.7 V
- V_{VCC2} = 18 V

Yields

$$V_{\mathrm{DESAT,pull-up}} = 4.6\ V, V_{\mathrm{DESAT,wo-pull-up}} = 3.6\ V \quad (3\text{-}7)$$

. The voltage is increased by 1 V, which needs to be considered together with DESAT threshold. The provided charging current to filter capacitor is however increased by ~3 times.

3.4.2 Advanced DESAT circuit for arbitrary threshold adjustment

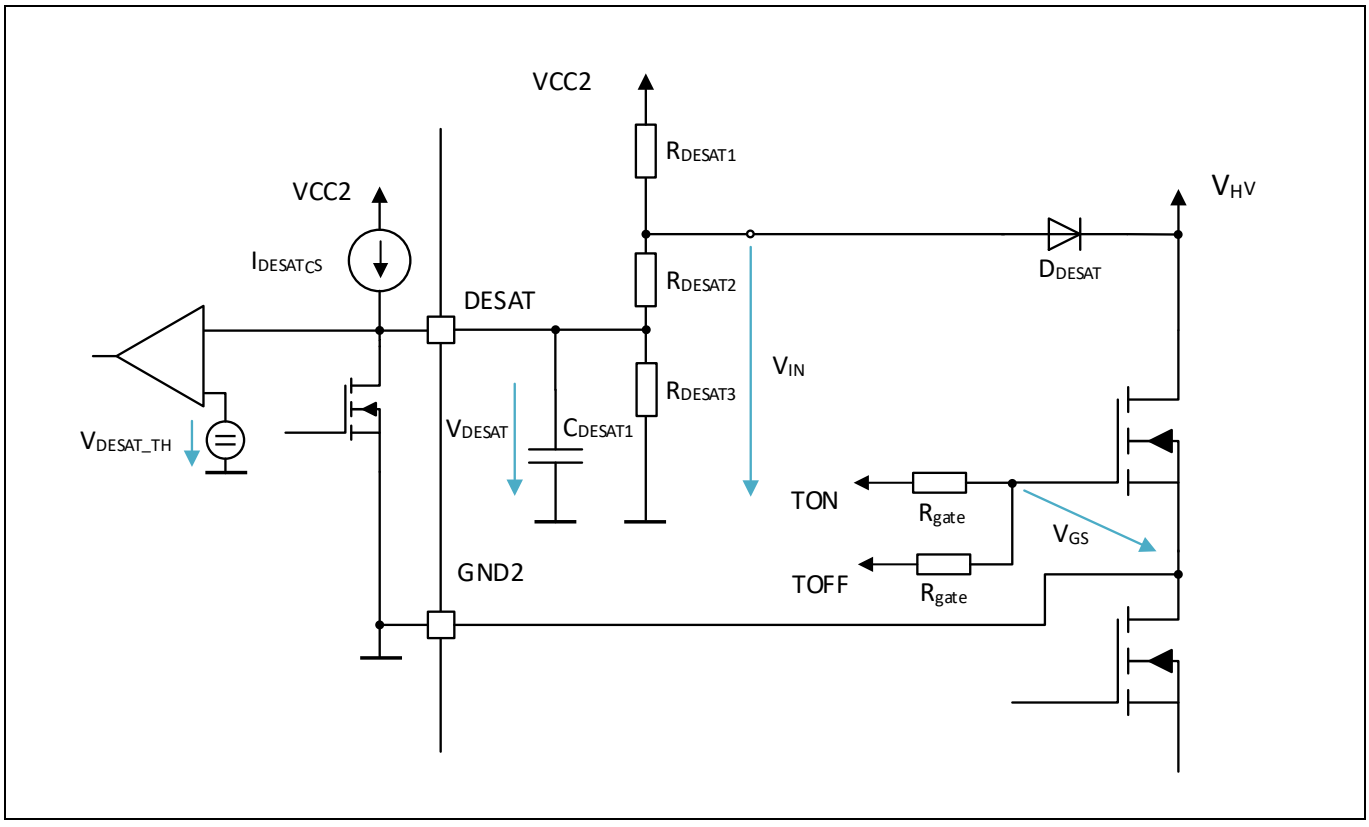


Figure 25 Circuit for arbitrary adjustment of DESAT threshold example

In case a higher DESAT threshold is needed an additional resistor divider can be introduced as shown in Figure 25.

3.4.2.1 Circuit description

In normal operation when the power tranistor is turned on, the steady state voltage on the DESAT pin is given by

$$V_{\mathrm{DESAT}} = \frac{R_{\mathrm{DESAT3}}}{R_{\mathrm{DESAT2}} + R_{\mathrm{DESAT3}}} \left(R_{\mathrm{DESAT2}} I_{\mathrm{DESATCS}} + V_{IN}\right) \quad (3\text{-}8)$$

Note that the voltage “Vin” combines the forward voltage drop of the diode D_{DESAT} and the voltage drop over the power transistor.

During short circuit the diode D_{DESAT} is blocking and the transient voltage on the DESAT pin is given by

$$V_{\mathrm{DESAT}}(t) = \frac{I_{\mathrm{DESATCS}} R_{\mathrm{DESAT3}} (R_{\mathrm{DESAT1}} + R_{\mathrm{DESAT2}})}{R_{\mathrm{DESAT1}} + R_{\mathrm{DESAT2}} + R_{\mathrm{DESAT3}}} \left(1 - e^{\frac{-t(R_{\mathrm{DESAT1}} + R_{\mathrm{DESAT2}} + R_{\mathrm{DESAT3}})}{C_{\mathrm{DESAT1}} R_{\mathrm{DESAT3}} (R_{\mathrm{DESAT1}} + R_{\mathrm{DESAT2}})}}\right) + \frac{V_{VCC2} R_{\mathrm{DESAT3}}}{R_{\mathrm{DESAT1}} + R_{\mathrm{DESAT2}} + R_{\mathrm{DESAT3}}} \left(1 - e^{\frac{-t(R_{\mathrm{DESAT1}} + R_{\mathrm{DESAT2}} + R_{\mathrm{DESAT3}})}{C_{\mathrm{DESAT1}} R_{\mathrm{DESAT3}} (R_{\mathrm{DESAT1}} + R_{\mathrm{DESAT2}})}}\right) \quad (3\text{-}9)$$

The equations allow several degrees of freedom in choosing R_{DESAT1}, R_{DESAT2}, R_{DESAT3} and C_{DESAT1}.

3.4.2.2 Optimizing the circuit

One approach to design the components in Figure 24 is to start by constraining the maximum current to be drawn from the supply voltage VCC2. The maximum pull-up current flows when the power transistor is steady on. The resistor R_{DESAT1} can then be calculated as

$$R_{\mathrm{DESAT1}} = \frac{\left(V_{VCC2} - V_{IN,min}\right)}{I_{VCC2,max}} \quad (3\text{-}10)$$

.

Due to the non-linear nature of the transient voltage, the next step in calculation requires the usage of an interative procedure. The flow is depicted in Figure 26.

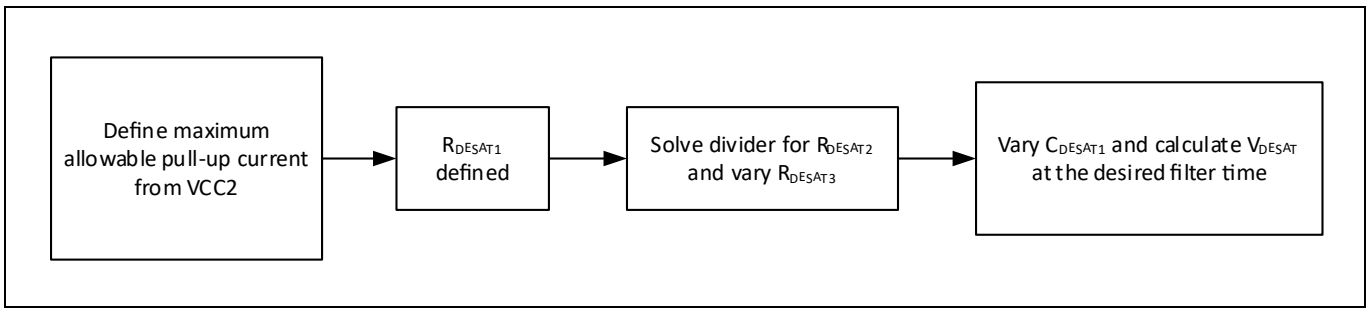


Figure 26 Proposed flow for finding the circuit parameters

After defining R_{DESAT1} the two remaining parameters R_{DESAT3} and C_{DESAT1} are varied to reveal the resulting filter time during short-circuit. Refactoring equation of (3-9) yields

$$R_{\mathrm{DESAT2}} = \frac{R_{\mathrm{DESAT3}}}{V_{DESAT_TH} - R_{\mathrm{DESAT3}} I_{\mathrm{DESATCS}}} \left(V_{IN,trigger} - V_{DESAT_TH}\right) \quad (3\text{-}11)$$

. Where V_{DESAT_TH} is the internal DESAT trigger threshold and $V_{IN,trigger}$ is the combined input voltage where DESAT shall trigger.

Using the voltage at the DESAT pin can now be evaluated for a variation of R_{DESAT3} and C_{DESAT1}. At the desired filter time the voltage on the DESAT pin needs to be equal to the DESATS threshold voltage.

$$V_{\mathrm{DESAT}}(t_{filt}) = V_{DESAT_TH} \quad (3\text{-}12)$$

An example of the procedure is show in Figure 27, for a desired filter time of 700ns. The voltage on the DESAT pin at 700ns is plotted for various filter capacitors and permissible pull-up currents.

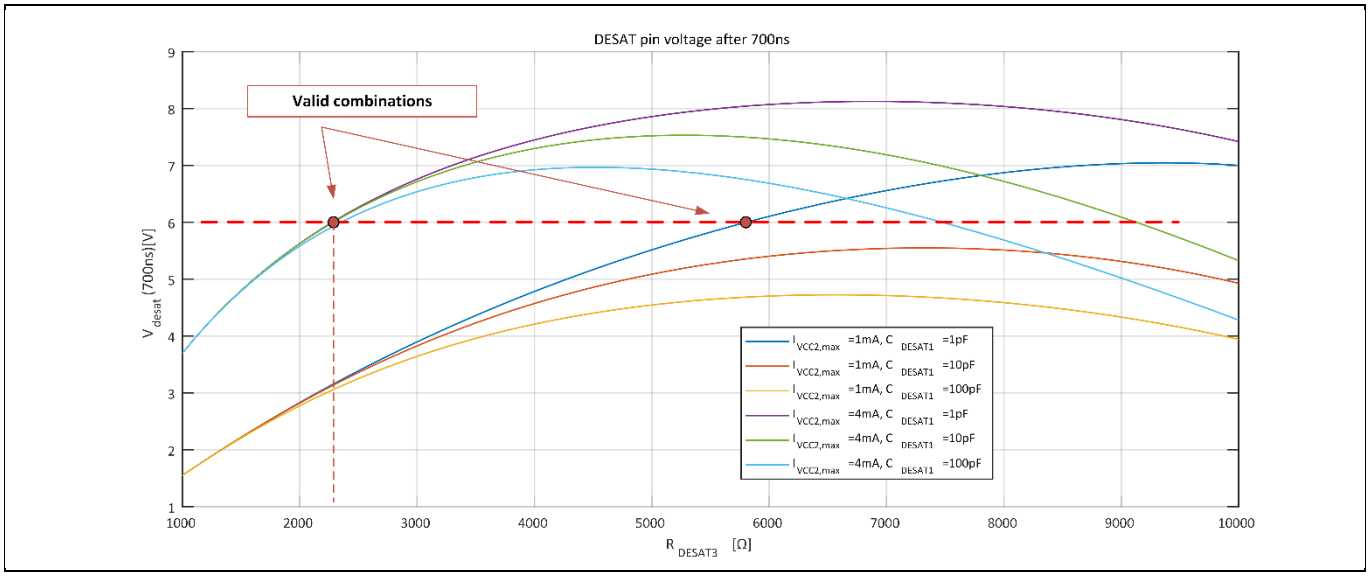


Figure 27 Calculation of the DESAT pin voltage at the desired filter time

The following conclusions can be drawn from Figure 27:

- The DESAT pin voltages rise with R_{DESAT3} and reaches a peak before dropping
- A higher pull-up current helps to reach the DESAT threshold even with lower values of R_{DESAT3}
- Higher values of filter capacitance C_{DESAT1} increase the filter time
- Higher values of filter capacitance require higher pull-up currents

The fact that there is a peak in Figure 27 is on first sight remarkable but follows an inituitive explanation. The higher the resistor R_{DESAT3}, the higher ohmic the voltage divider including R_{DESAT2} will be (see equation 3-12). At the same time the voltage-drop on the DESAT pin due to the current source $I_{DESATCS}$ driving into the resistors increases, too. The charging of the the filter capacitor C_{DESAT1} will however take longer, due to the smaller contribution to charge the capacitor through VCC2 caused by higher values of R_{DESAT2} and R_{DESAT3}.

3.4.3 Negative DESAT voltage protection

When driving an inductive load in a full bridge phases of reverse conduction through the body diode of the power switch occur naturally. This scenario is depicted in Figure 28.

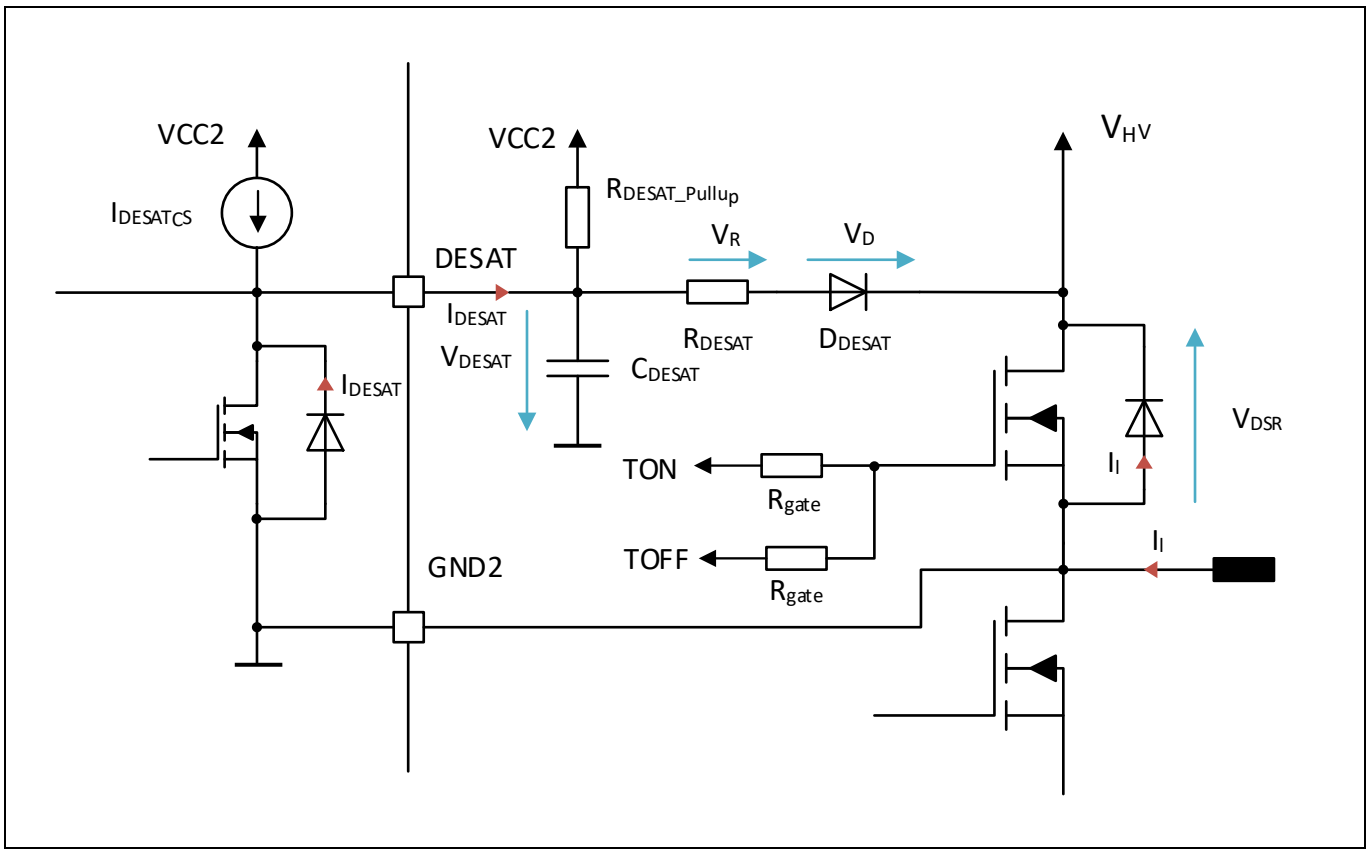


Figure 28 DESAT current during body diode reverse conduction

The voltage V_{DSR} is caused by the free-wheeling current I_l from the motor winding inductance. The diode D_{DESAT} is forward biased and the voltage on the DESAT pin V_{DESAT} becomes negative resulting in the current I_{DESAT} . The EiceDRIVER™ gate driver integrates a guarded body diode on the DESAT clamping transistor to allow for this operation mode without the need for further external clamping structures.

The reverse current capability is given in the datasheet by the “DESAT negative transient current”. To estimate the static current flow the following formula can be used

$$I_{\mathrm{DESAT}} = \frac{V_{\mathrm{DSR}} - V_{\mathrm{D}}}{R_{\mathrm{DESAT}}} \qquad (3\text{-}13)$$

. Note that the “DESAT negative transient current” is given with an additional timing and repetition frequency constraint.

Hint: in case the peak of the actual measured negative transient current is within the specified range in the datasheet but the pulse duration is extended or a different switching frequency is used then the gate drive capability can also be judged by calculating the equivalent energy

$$E_{\mathrm{DESAT,eq}} \sim t_{DESATNTC} \cdot f_s \qquad (3\text{-}14)$$

under the assumption that the unknown forward voltage drop on the internal diode is identical. For the application then simply

$$t_{DESATNTC,\text{actual}} \cdot f_{s,\text{actual}} \leq t_{DESATNTC} \cdot f_s \quad (3\text{-}15)$$

needs to be statisfied. Where $t_{DESATNTC}$ and f_s are the rated values in the “DESAT negative transient current” inside the datasheet.

3.4.4 SOFTOFF feature

The SOFTOFF feature provides the highest degree of flexibility to control the turn-off of the power switch during a DESAT or OCP event. It is available on 1EDI3035AS, 1EDI3038AS, 1EDI3025AS, 1EDI3026S and 1EDI3028AS. The turn-off time is controlled arbitaritly by $R_{SOFTOFF}$ and is up to the system integrator. This enables a seamingless trade-off between turn-off time and inductive induced overvoltage on the power switch. An overview of the SOFTOFF feature together with DESAT protection is shown in Figure 29. When OCP protection is used, the pattern is identical.

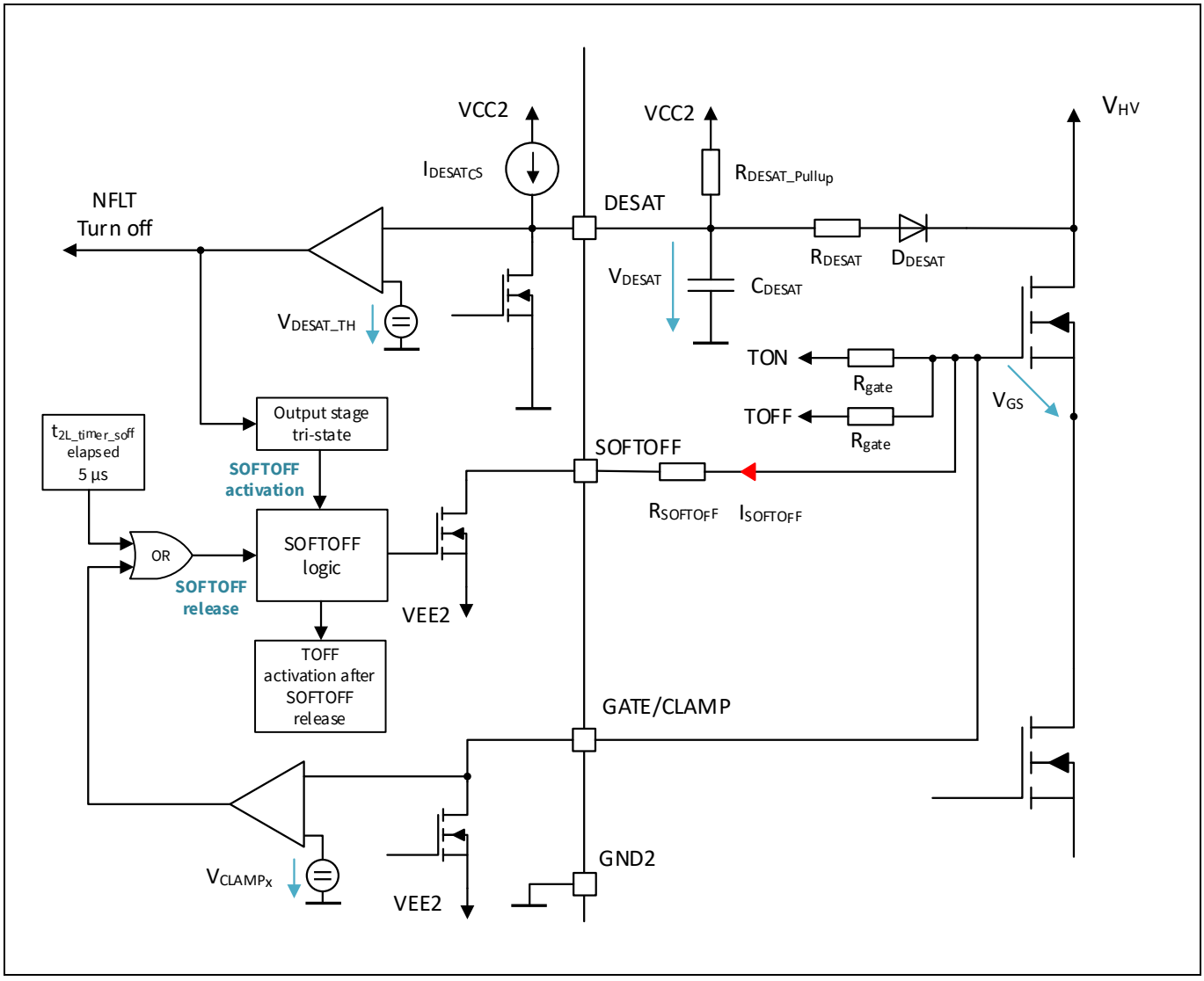


Figure 29 SOFTOFF block diagram

SOFTOFF activates a pull-down transistor to VEE2 after a DESAT or OCP event happened and when the output stage of the gate driver was tri-stated. SOFTOFF turns off the power device gate with the means of $R_{SOFTOFF}$. When the GATE/CLAMP pin reaches the active Miller clamp threshold V_{CLAMPx}, the SOFTOFF logic deactivates the SOFTOFF pull-down transistor and activates the output stage TOFF turn-off as well as the active Miller clamp GATE/CLAMP.

This sequence in the turn-off procedure can be nicely observed in the measurement shown in Figure 22. CH3 shows the SOFTOFF pin going low after a DESAT event was triggered. The gate is discharged through $R_{SOFTOFF}$ until GATE/CLAMP on CH4 reaches the active Miller clamping threshold voltage V_{clamp2} (1EDI3025AS, 1EDI3026AS), the SOFTOFF is released and TOFF is reactivated together with the internal active Miller clamp.

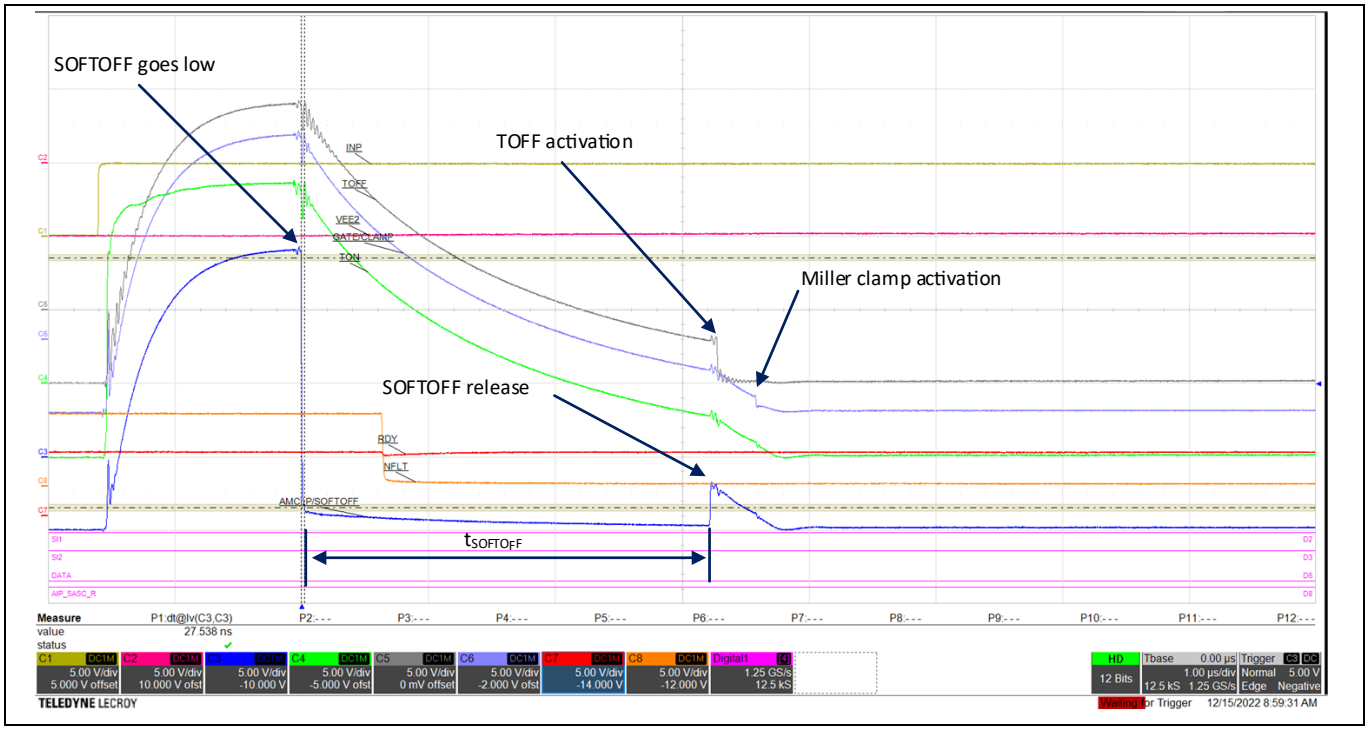


Figure 30 SOFTOFF example with $R_{SOFTOFF}$ = 5 Ohm, C_{gs} = 68 nF

When a crossing of the Miller clamp threshold voltage is not detected within $t_{2l_timer_soff}$ as shown in Figure 29, SOFTOFF is force released and TOFF activated.

3.5 DESAT and SOFTOFF performance measurement

In order to illustrate the DESAT and SOFTOFF concept benefits a short circuit measurement was conducted using the 1EDI3035AS evaluation kit together with a FF06MR12A04MA2 HybridPACK™ DSC module. The set-up is shown in Figure 31.

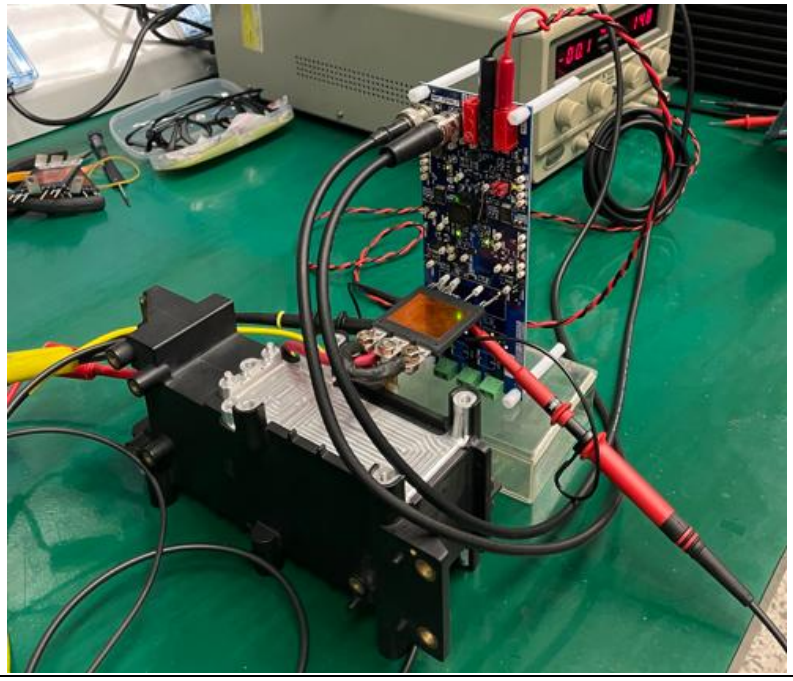


Figure 31 Measurement set-up for type 1 short circuit characterization

The high side switch is permanently on and the low-side switch is turned on into the short circuit created by the high-side. During this event the drain current, gate voltage and drain source voltage of the low-side switch are recorded.

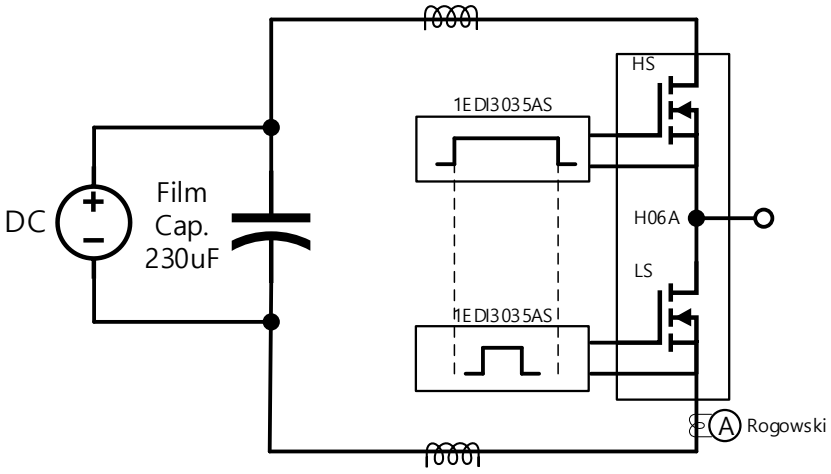


Figure 32 Short circuit type 1 principle schematic

For the first short circuit test an initial value has to be chosen for C_{DESAT} and $R_{SOFTOFF}$. While all the formulas are presented in section 3.4.1 they don't give a hint about with which values to start with. For a first switching test it

is adviseable to mount no C_{DESAT} capacitor at all to provoque the shortest possible filter time t_{filter}. Later C_{DESAT} is added again to increase the noise robustness and prevent false triggering during normal inverter operation.

The initial value for $R_{SOFTOFF}$ is more tricky to predict. For Infineon's second generation SiC technology a factor of "2x" to "3x" the recommended regular turn-off gate resistor is a good starting point.

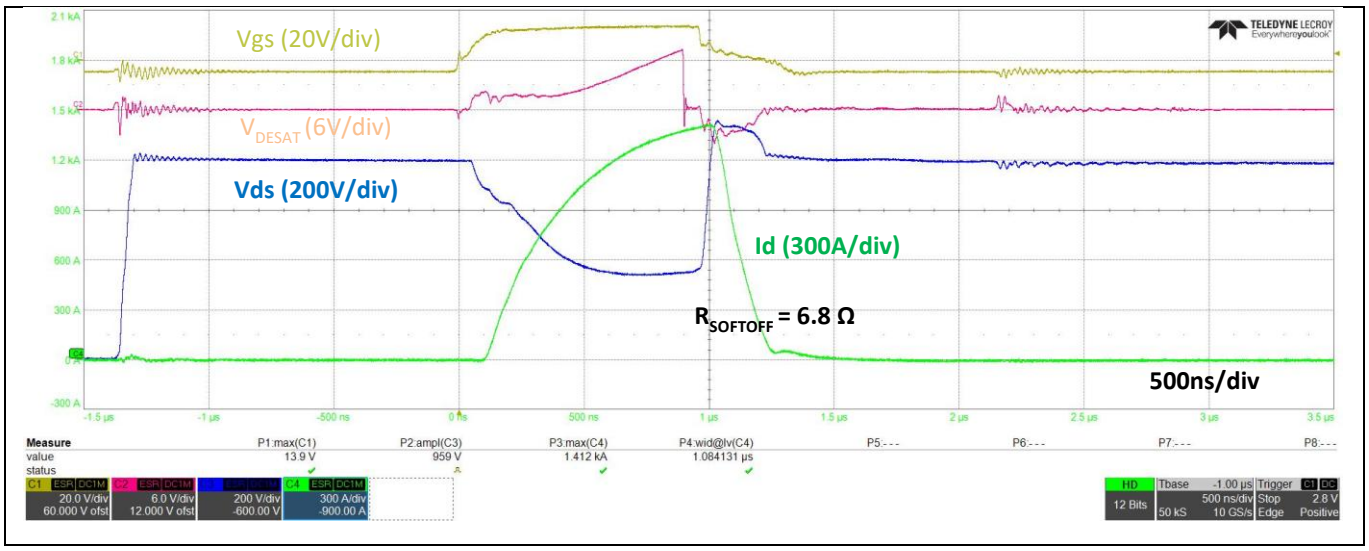


Figure 33 Example waveform for a short circuit turn-off event

In Figure 33 a waveform was recorded. It is visible how the drain current rises to a peak value of almost 1500A until SOFTOFF is activated. Along with the current there is also an increase in the voltage on the DESAT pin V_{DESAT} which leads to the tripping of the DESAT protection.

For all measurements no pull-up resistor on DESAT R_{DESAT_pullup} was used.

3.5.1 Influence of varying C_{DESAT}

The value of the DESAT filter capacitor directly influences the filter time that is applied before the detection of the short circuit event on the DESAT pin. In Figure 34 it is visible how the length of the V_{gs} pulse is reduced with lower capacitor values. Note that the relationship between the pulse length and the capacitor value is indeed linear.

Another noticeable phenomenom is shown in the V_{ds} peak voltage. The overshoot remains constant. This is due to the fact that the overshoot is caused by the change in drain current "dI_{ds}/dt" rather than the drain current absolute value. This emphasizes the impact of the resistor $R_{SOFTOFF}$ as shown in 3.5.2.

In the application it is important to choose the filter time together with C_{DESAT} to prevent false triggering of the DESAT due to noise induced from switching in the inverter. The minimum permissible value for the filter time can only be determined in system tests.

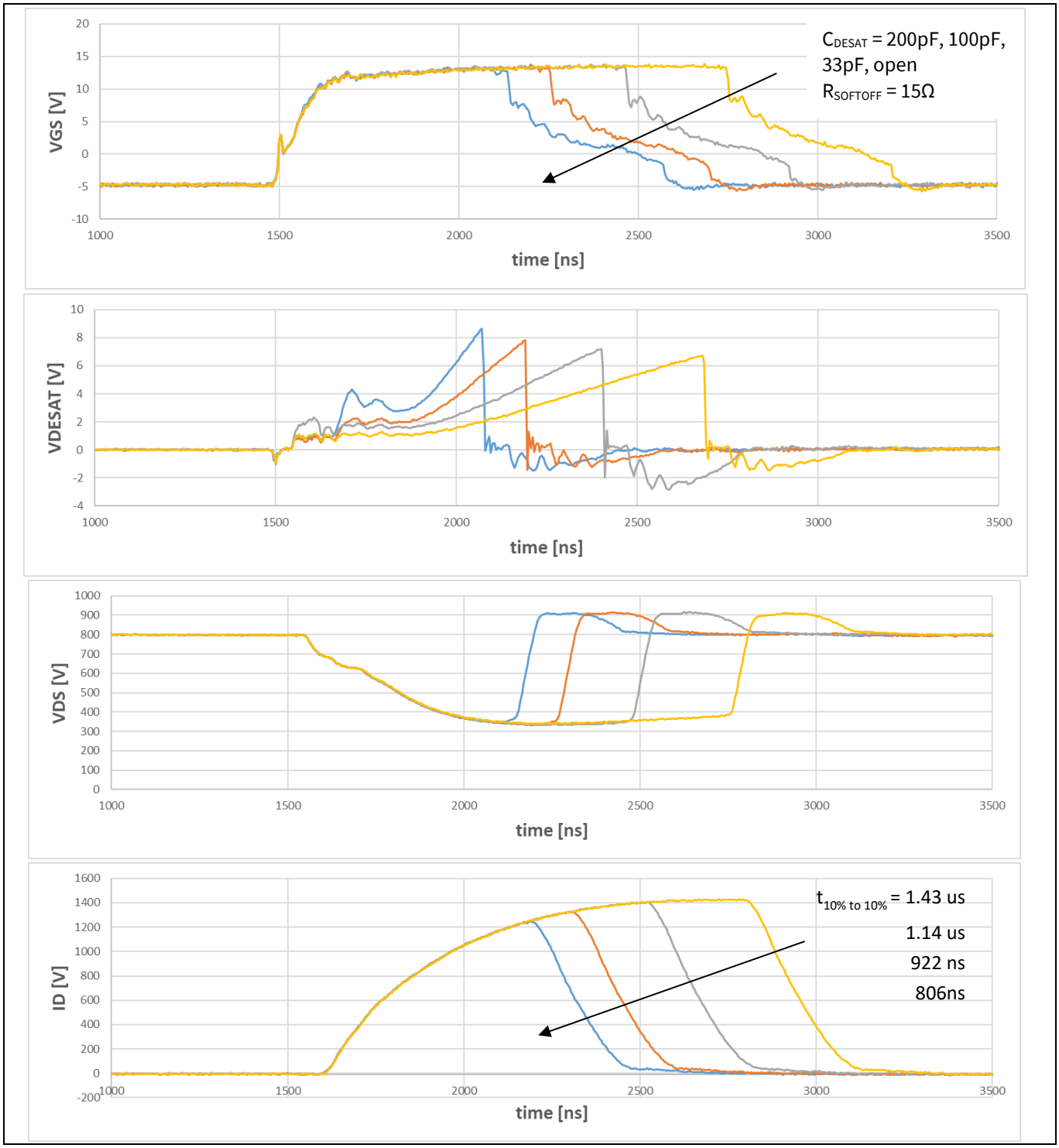


Figure 34 Short circuit waveforms for different C_{DESAT} values

3.5.2 Influence of varying $R_{SOFTOFF}$

Figure 35 shows that a reduction in the value of $R_{SOFTOFF}$ has no impact on the time until the short circuit event is detected. The value instead influences the change in the drain current "dI_{ds}/dt" during turn-off and the total turn-off time. Hence, the resistor value controls the V_{ds} overshoot peak voltage.

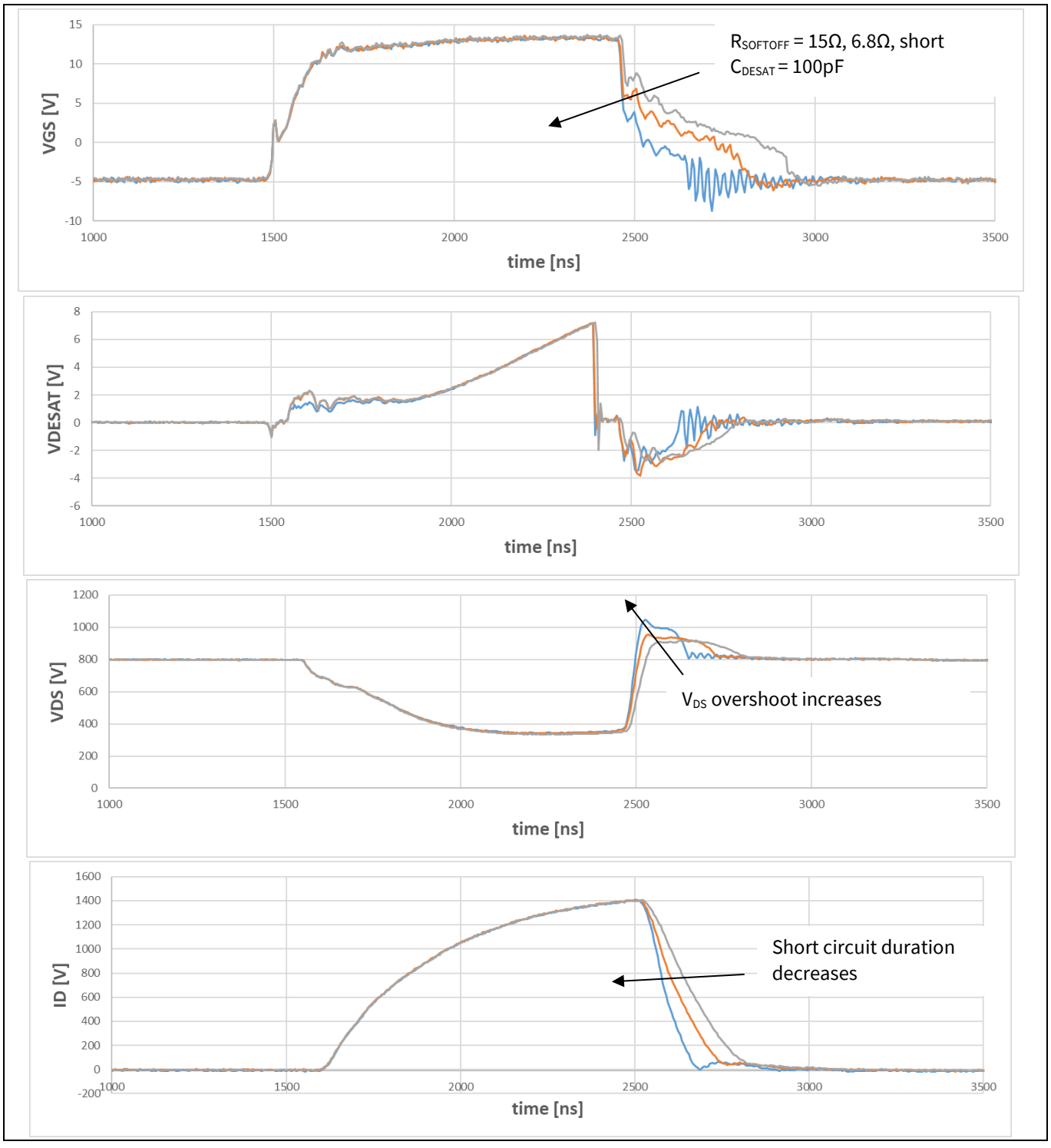


Figure 35 Short circuit waveforms for different $R_{SOFTOFF}$ values

3.5.3 Influence of varying V_{VCC2}

Increasing the gate driver positive supply voltage leads to an increase in the V_{gs} target voltage during turn-on. As a consequence, the resistance of the SiC device reduces and the peak short circuit current increases. The increase in the short circuit current leads to an earlier triggering of the DESAT protection and thus the total turn-off time is further decreased. See Figure 36 for reference.

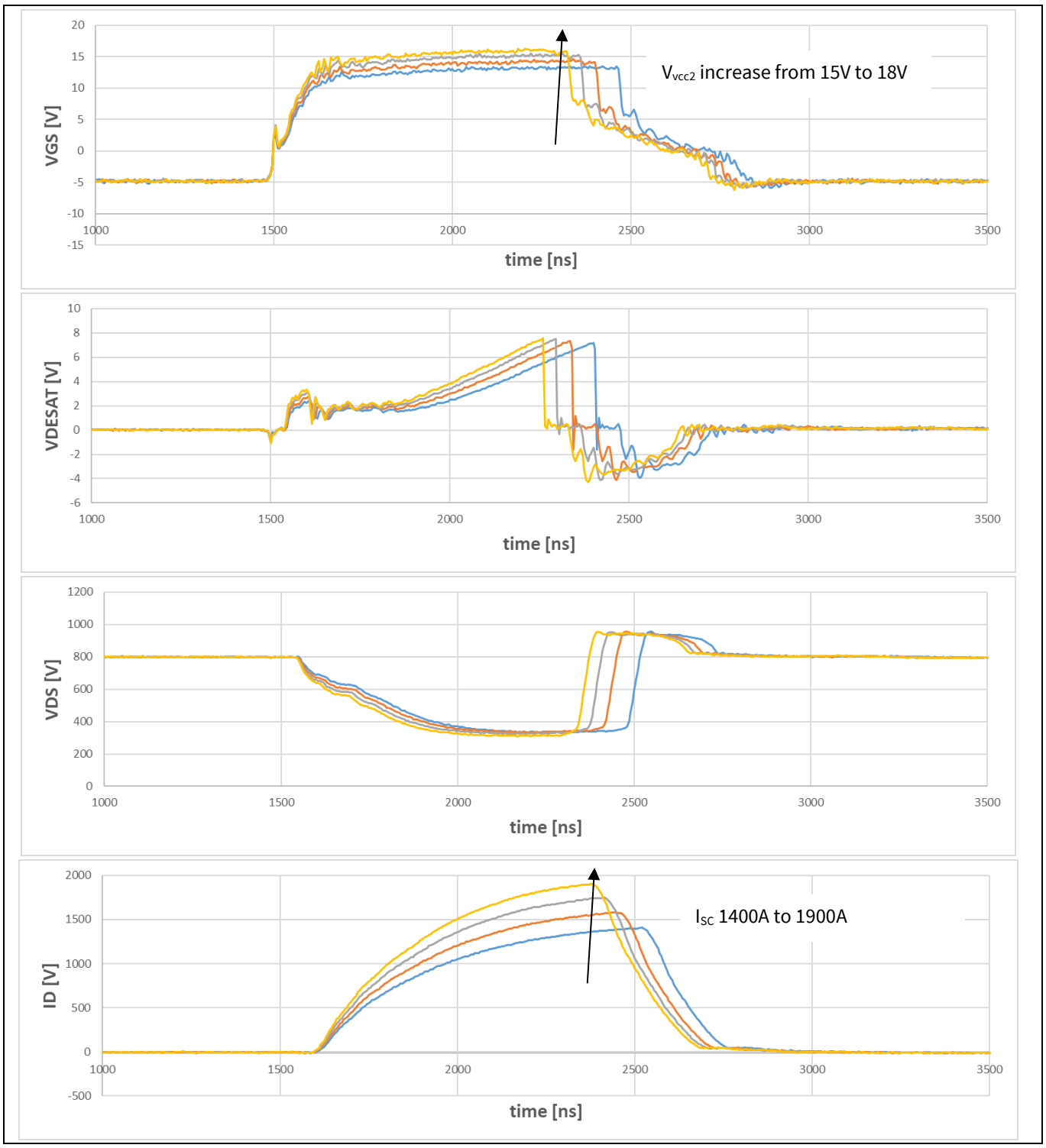


Figure 36 Short circuit waveforms for increasing V_{VCC2} voltage

3.5.4 Summary and additional hints

Determining the values of C_{DESAT} and $R_{SOFTOFF}$ can be achieved with the following steps:

- Start the first mueasrement with no C_{DESAT} and $R_{SOFTOFF}$ ~ 3* $R_{g,off}$
- Reduce or increase $R_{SOFTOFF}$ until V_{ds} overshoot is within specification
- Add C_{DESAT} until no false triggering of DESAT is observed in the application
- Or remove C_{DESAT} until required short circuit time is achieved
- In case too much C_{DESAT} capacitance has to be added consider boosting the charging current by adding a pull-up resistor R_{DESAT_pullup}

As observed in Figure 34 the DESAT SOFTOFF concept of the EiceDRIVER™ gate driver family achieves outstanding short circuit turn-off performance, resulting in short circuit turn-off times around or below 1µs.

3.6 DESAT and OCP built-in selftest

The EiceDRIVER™ gate driver family implements an automatic selftest for latent fault checking on the DESAT and OCP feature. Note that for each product either DESAT or OCP is available according to Table 1. The input structure is very similar but the implementation of built-in selftest is different and explained hereafter

3.6.1 DESAT built-in selftest sequence

Figure 37 shows the DESAT feature including the following sub-components:

- Clamping transistor that keeps DESAT low in case TON = off
- Comparator that compares DESAT to the DESAT threshold
- Current source that charges the DESAT node

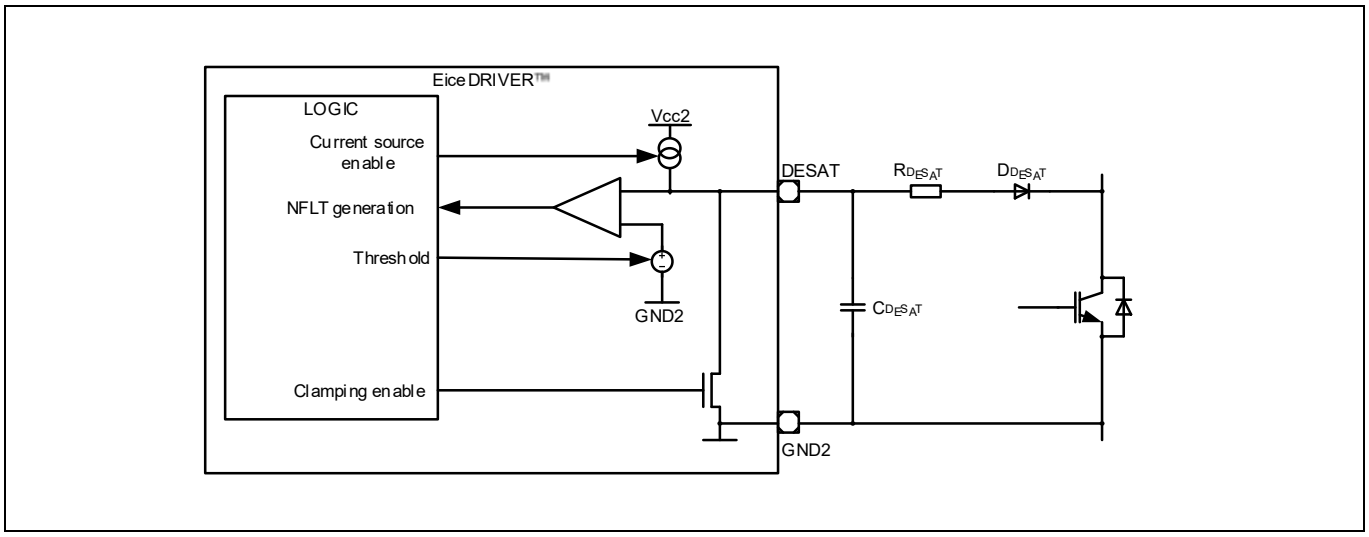


Figure 37 DESAT feature description

The behavior of the DESAT built-in selftest is depicted in the flow chart shown in Figure 38.

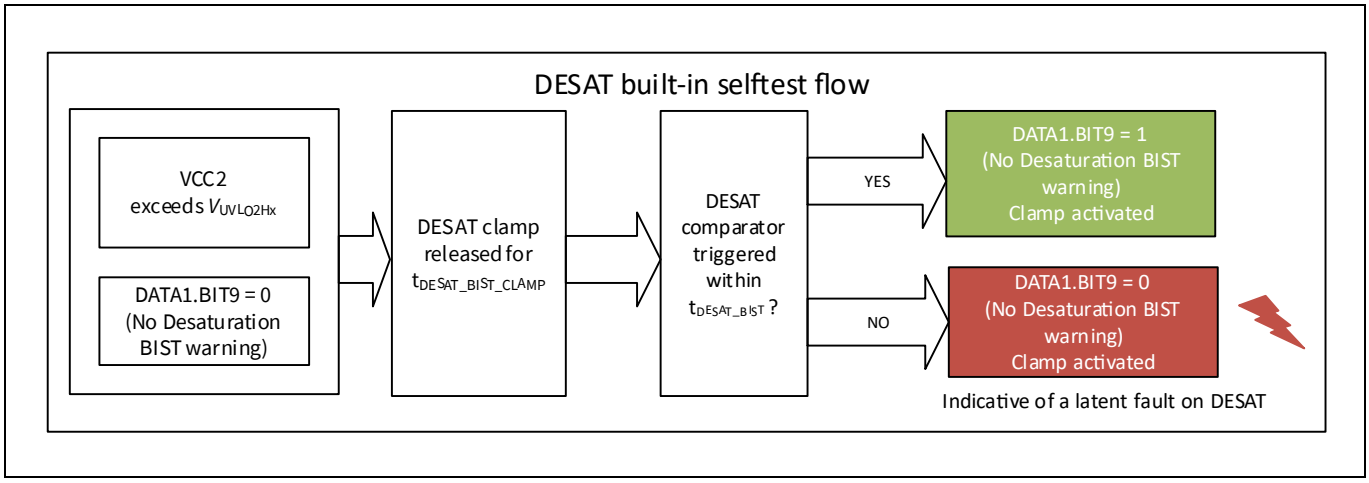


Figure 38 DESAT built-in selftest flow chart

The condition for a selftest start is that the VCC2 voltage exceeds the higher UVLO2 limit $V_{UVLO2Hx}$. This condition is usually fulfilled when the gate driver is being powered-up. For the selftest the clamping transistor is intentionally released for $t_{DESAT_BIST_CLAMP}$ and the voltage on the DESATpin voltages rises because the node is pulled up by the internal current source.

The gate driver detects a successful selftest when the DESAT comparator is tripped within t_{DESAT_BIST}. Whenever a selftest is triggered, BIT9 in the second DATA frame is cleared. Upon a successfully completed selftest the bit is set to one. It remains zero otherwise.

3.6.2 OCP built-in selftest sequence

The OCP feature internal structure is identical to DESAT besides the different OCP triggering threshold and a slightly altered OCP built-in selftest sequence.

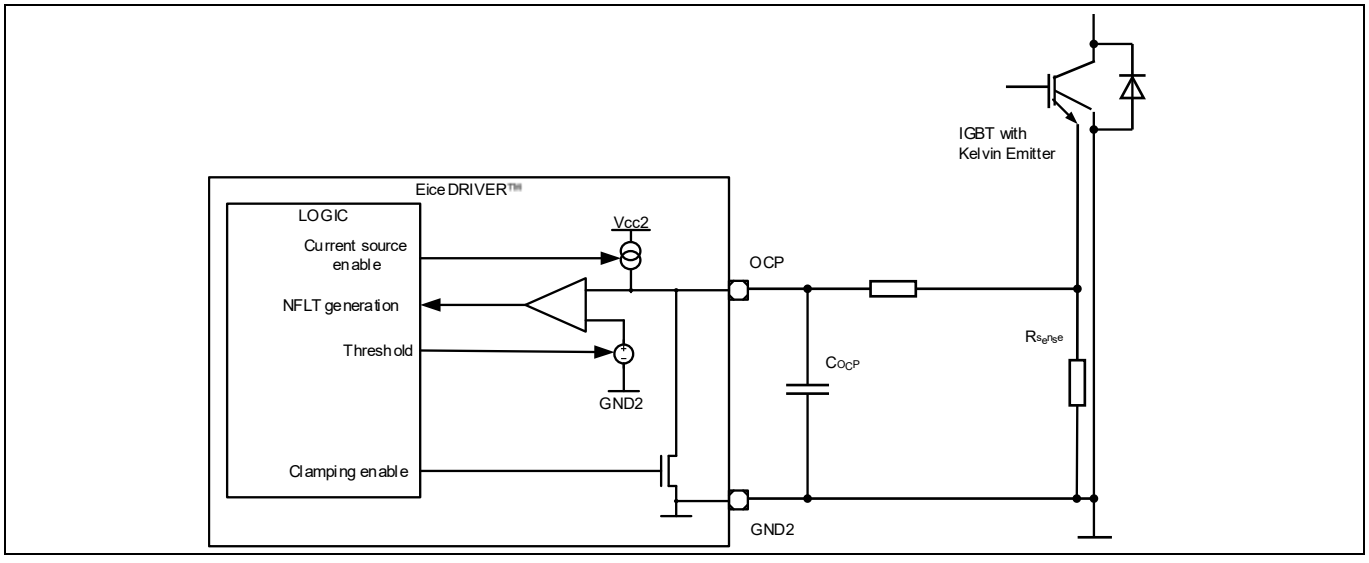


Figure 39 OCP feature description

The OCP built-in selftest differs slightly from the DESAT variant. The reason is that the external circuit connected to the OCP pin is by nature low ohmic. As shown in Figure 39 typically a shunt resistor is used to translate the mirrored fraction of the IGBT drain current into a voltage.

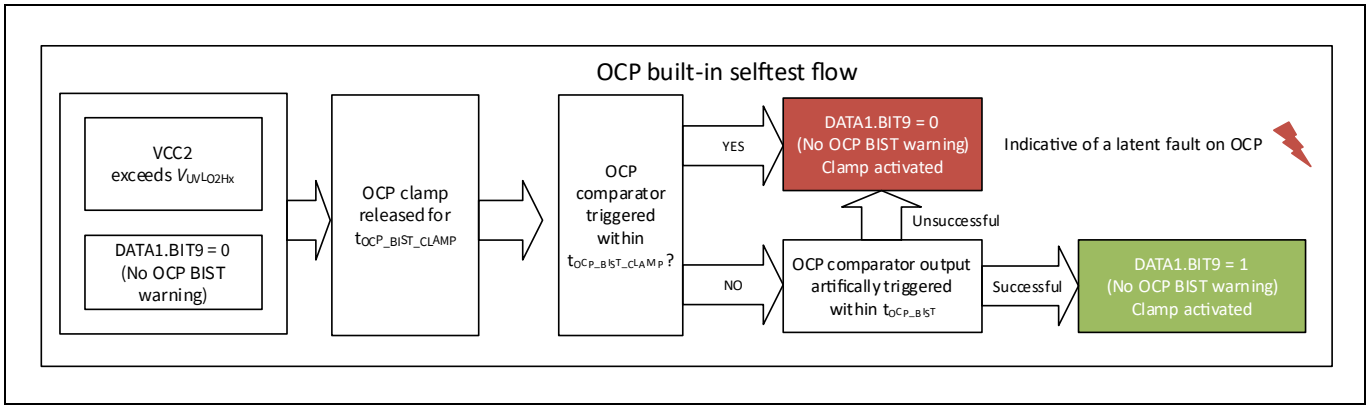


Figure 40 OCP built-in selftest flow chart

The OCP BIST starts like the DESAT BIST by releasing the clamp transistor. The OCP BIST is then expecting that the OCP threshold is not reached within $t_{OCP_BIST_CLAMP}$, since the external shunt effectively shorts the OCP current source. Only in case of a pin-open the voltage on the OCP pin would rise and trigger the comparator.

If the first phase of the OCP BIST was successful the second phase will be processed internally. In this phase the OCP comparator output is triggered artificially and the logic checks whether the OCP event is correctly processed.

In case both phases are successful BIT9 in the second DATA frame is cleared within t_{OCP_BIST}.

Hints for the system integrator:

- Upon system power-up observe BIT9 in the DATA1 frame = “NO desaturation/OCP BIST warning”
- In the microcontroller set a counter based on the maximum permissible ramp-up time of the secondary supply voltages VCC2, VEE2
- After the ramp-up time has elapsed, try initializing the driver by setting SI1 = SI2 = 1 simultanously
- The driver will only transition to “PWM Enable” state when there is no pending error active and RDY will go high
- After RDY goes high wait at least for t_{DESAT_BIST}/t_{OCP_BIST} to ensure that the selftest has finished
- Wait for a new DIAG1 frame on the DATA pin to ensure that the outcome of the selftest is updated in the DATA frame

For more details look at the comprehensive guide on start-up behavior that is given in chapter 2.5.1.

Note: A failed selftest of DESAT/OCP will not prevent the driver from transitioning into PWM Enable and RDY will still go high. It is up to the system integrator to react accordingly to the selftest result.

Figure 41 shows a measurement example from the evaluation board. In the screenshot VCC2 rises slowly and is therefore almost a flat line. In this example VCC2 just crossed $V_{UVLO2Hx}$ at ~12.3 V and the DESAT clamp is released. The DESAT voltage crosses V_{DESAT2} after less than 1 µs. The clamp is activated again and DESAT is pulled to GND2.

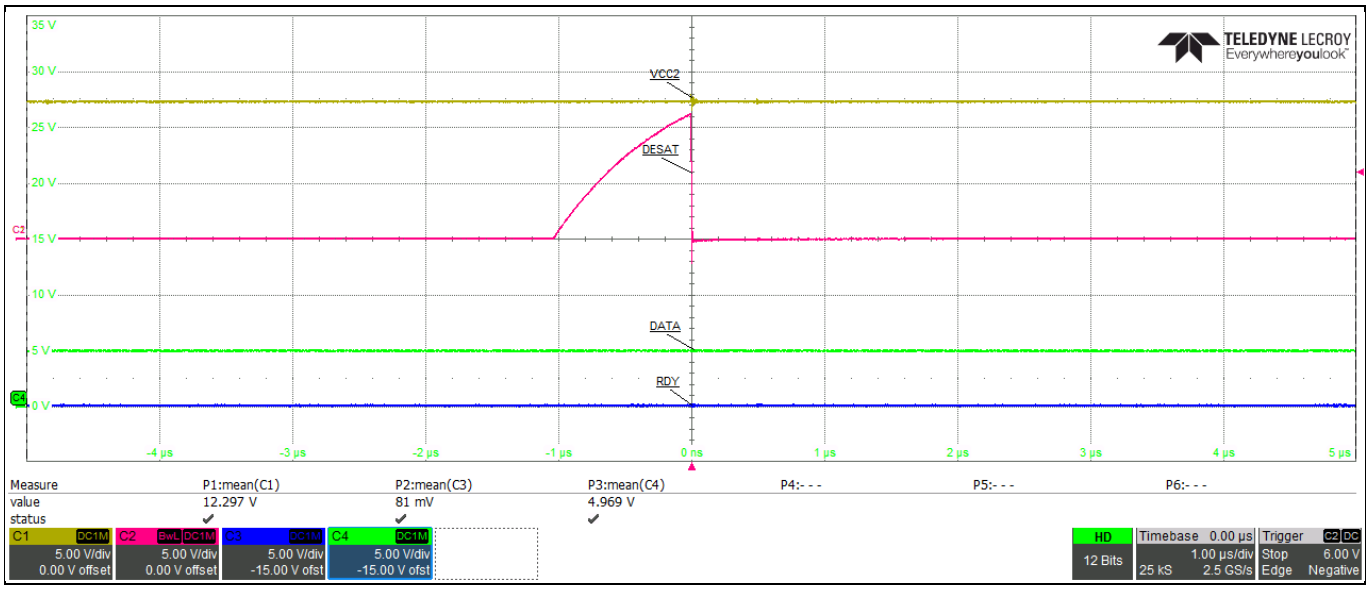


Figure 41 DESAT selftest example on the evaluation board

Since the DATA frame period t_{period} is several magnitudes longer than the actual DESAT triggering time, the reaction of the DATA output can only be meaningfully depicted on other time scale. Figure 42 shows a capture of the DATA output reaction after a successful DESAT built-in selftest.

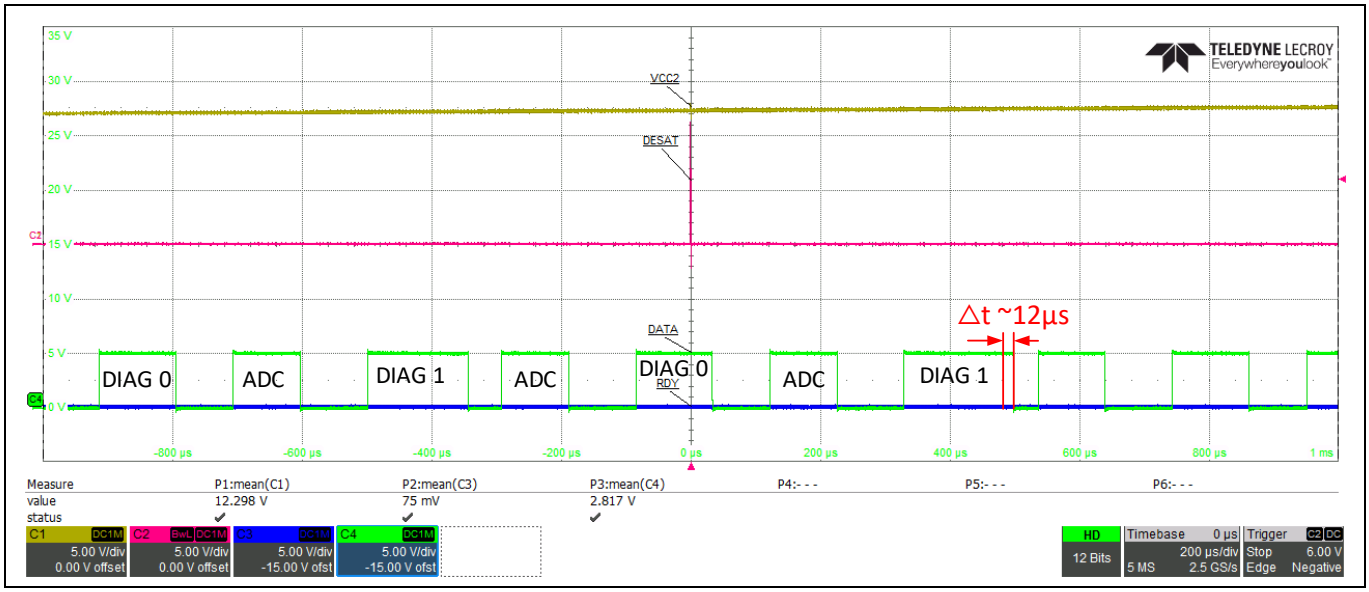


Figure 42 DATA output reaction to a successful selftest

The DIAG1 frame duration increases by around 12 µs in the above example. This is approximately 6.25% of the frame period of 200 µs. According to the datasheet, this corresponds to BIT9 – “No desaturation BIST warning”. It can therefore be concluded that in the shown example the successful completion of the DESAT built-in selftest is signaled by setting BIT9.

3.7 Short input pulses

The EiceDRIVER™ gate driver is capable to propagate short pulses. Features like the output stage monitor, gate monitoring, DESAT/OCP incorporate an intentional blanking time that can easily be longer than the propagated pulse.

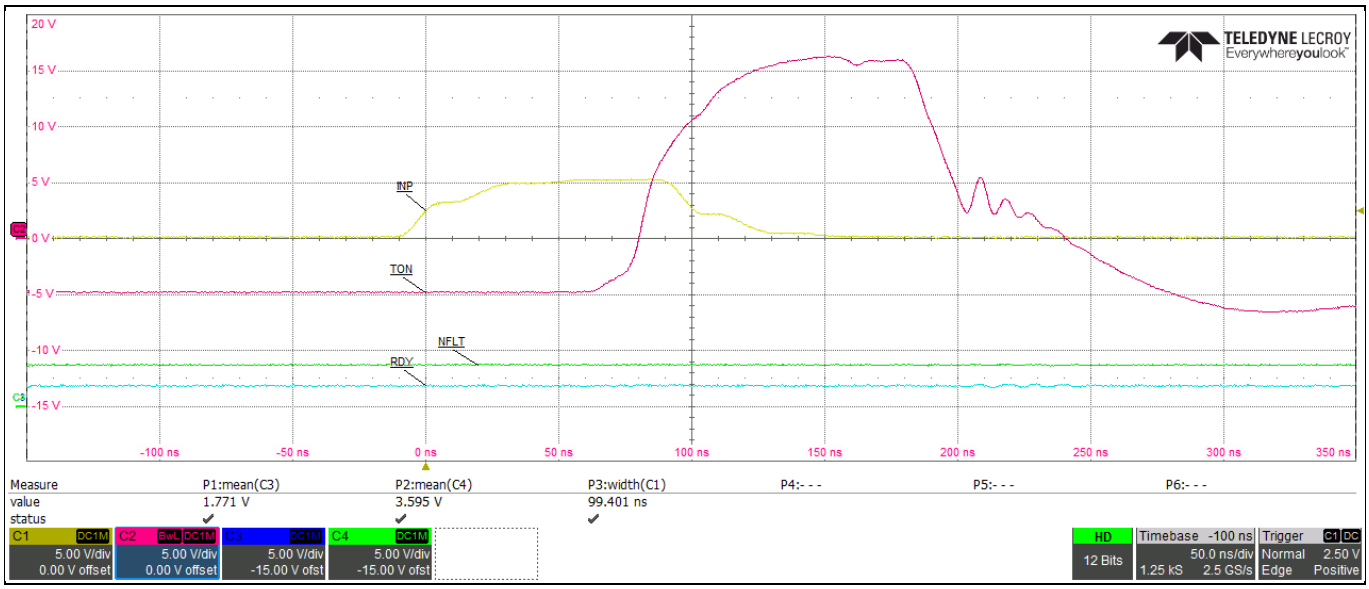


Figure 43 Gate driver output for a 100 ns input pulse

In such a condition the monitoring features follow the moving target given by the received PWM signal on the secondary chip.

3.8 Analog to Digital Converter

The EiceDRIVER™ gate driver family implementes a 12bit delta-sigma analog to digital converter (ADC) which is prepared for temperature measurement together with an NTC or temperature sense diodes. The ADC continuously samples the secondary side voltage on the AIP pin. Note that the AIP pin also shares the functionality of SASC, for further information see 0.

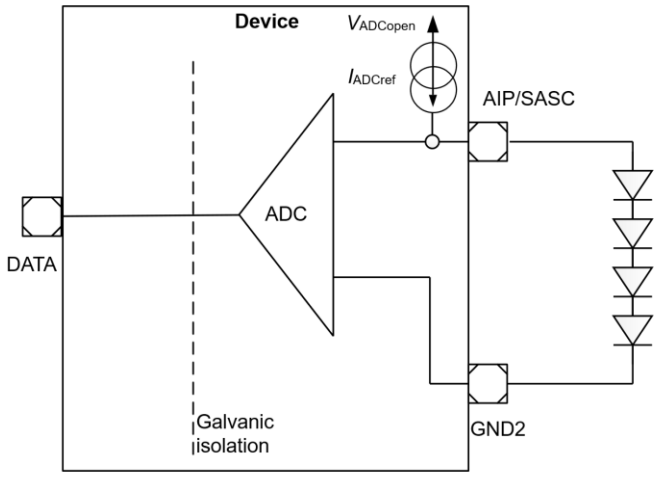


Figure 44 ADC feature inside the EiceDRIVER™ gate driver

The ADC result is encoded into a duty cycle and provided on the DATA pin to be captured by a microcontroller. The ADC offset is trimmed in production at an input voltage level of 2 V, which is optimized for the measurement of external thermal diodes.

3.8.1 Signal transfer characteristic

There is a linear relationship between the ADC input voltage and the duty cycle of the respective frame on the DATA pin as shown in Figure 45. The ADC duty cycle is limited within $D_{ADC,min}$ and $D_{ADC,max}$, therefore the usable voltage range is limited at the boundaries of the quantization range. The output duty cycle “clips” at these limits when the ADC input voltage exceeds them. Note that this range is further restricted by the ADC error, which is calculated in section 3.8.3.

The ADC sample rate is synchronized to the DATA output. It is exactly half of the DATA output frequency, since every second frame in the DATA interface represents the ADC voltage. For further details see chapter 3.2.

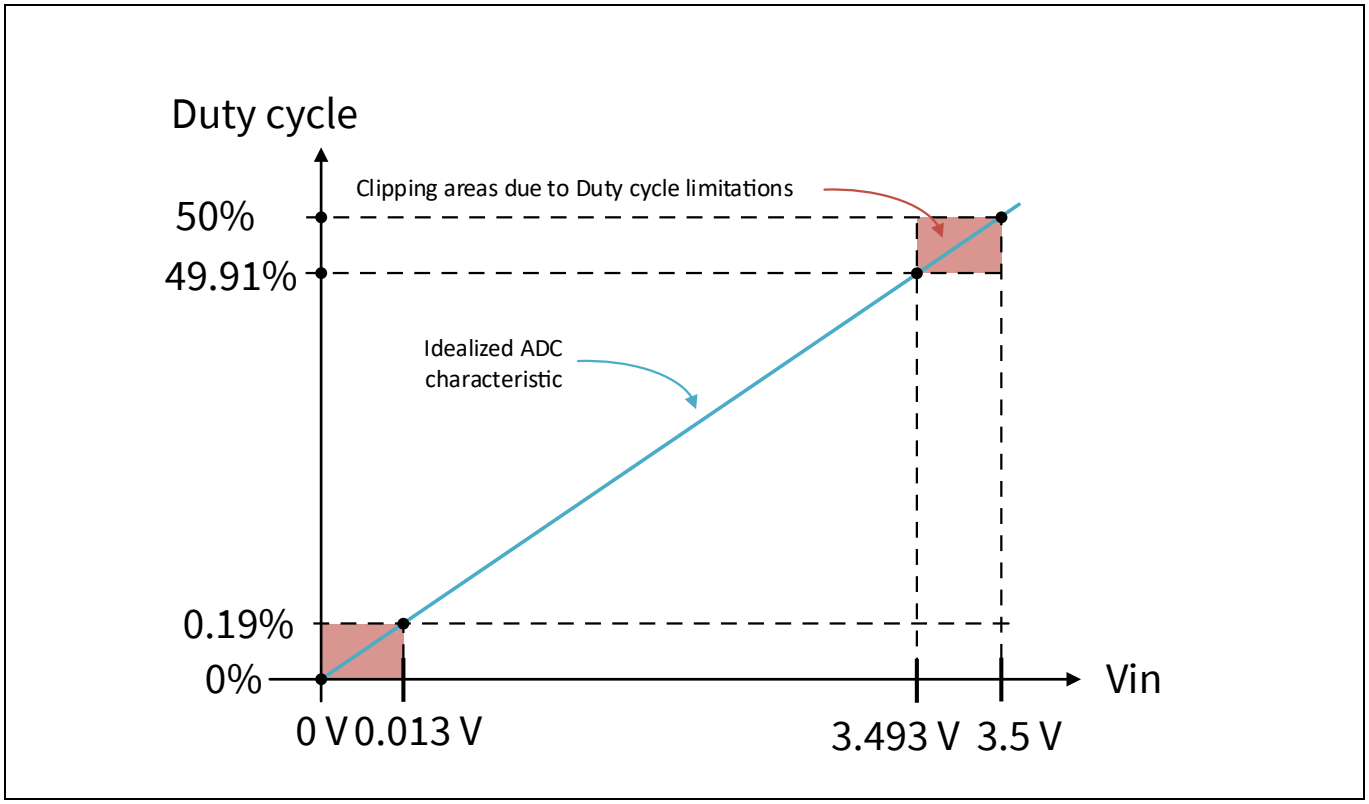


Figure 45 Input voltage vs. output duty cycle on DATA

3.8.2 Frequency characteristic

A first order CIC decimation filter is used to generate the output values from the delta-sigma bit stream. The modulation frequency f_{mod} equals 10 MHz. A decimation filter is used to generate the digital output signal from the modulator bit stream, resulting in a output sample rate of f_{sample} as depicted in Figure 46.

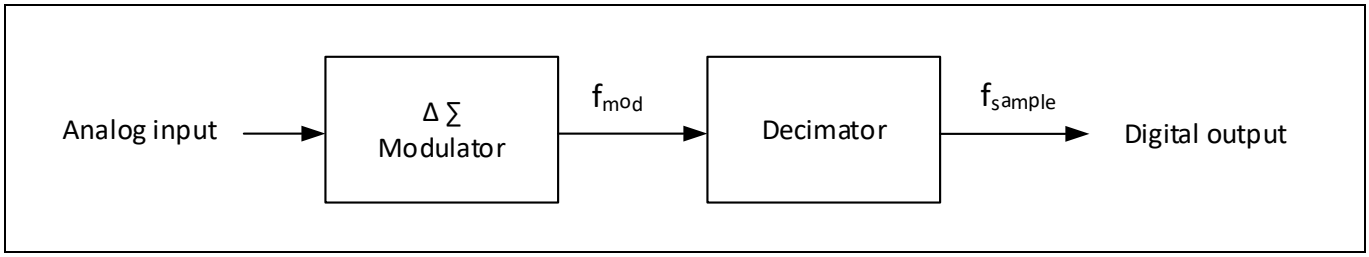


Figure 46 Delta sigma modulator flow chart

The transfer function of the decimation filter is given in the discrete domain as

$$H(z) = \frac{1}{D}\frac{1 - z^{-D}}{1 - z^{-1}} \quad (3\text{-}16)$$

, where the decimation rate is given as

$$D = \frac{f_{mod}}{f_{sample}} = 2^{12} \quad (3\text{-}17)$$

.

Conducting a bliniear transform with $z = e^{j\omega/f_s}$ the filter can be expressed in the fourier transform as

$$H\left(e^{j\frac{\omega}{f_{mod}}}\right) = \frac{1}{D}\frac{1-e^{-\frac{j\omega D}{f_{mod}}}}{1-e^{-\frac{j\omega}{f_{mod}}}} = \frac{1}{D}\frac{e^{j\omega/2f_{mod}}}{e^{j\omega D/2f_{mod}}}\frac{e^{j\omega D/2f_{mod}}-e^{-j\omega D/2f_{mod}}}{e^{j\omega/2f_{mod}}-e^{-j\omega/2f_{mod}}}$$
$$= \frac{1}{D}e^{\frac{j\omega}{2f_{mod}}(1-D)}\frac{\sin\left(\frac{\omega D}{2f_{mod}}\right)}{\sin\left(\frac{\omega}{2f_{mod}}\right)} \quad (3\text{-}18)$$

. Where the magnitude is given by

$$|H(f)| = \frac{1}{D}\left|\frac{\sin\left(\frac{\omega D}{2f_{mod}}\right)}{\sin\left(\frac{\omega}{2f_{mod}}\right)}\right| = \frac{1}{D}\left|\frac{\sin\left(\frac{\pi f D}{f_{mod}}\right)}{\sin\left(\frac{\pi f}{f_{mod}}\right)}\right| = \frac{1}{D}\left|\frac{\sin\left(\frac{\pi f}{f_{sample}}\right)}{\sin\left(\frac{\pi f}{f_{mod}}\right)}\right| \quad (3\text{-}19)$$

. The transfer function is plotted in Figure 47.

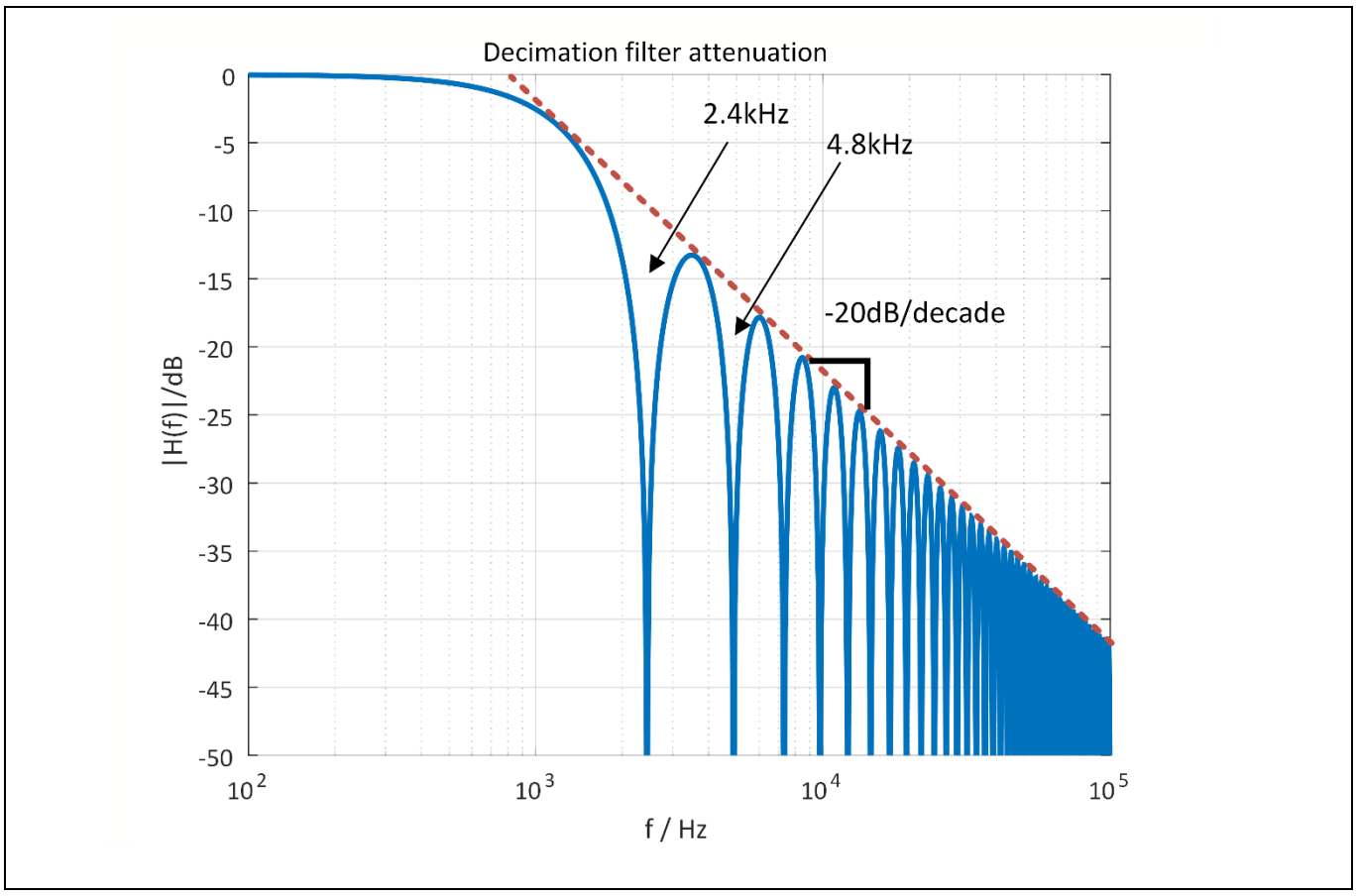


Figure 47 Delta sigma frequency characteristic is given by the decimation filter

The filter applies a 20dB per decade as is shown by the envelope function. Notches with additional attenuation appear at

$$f = n \cdot f_{sample} \quad (3\text{-}20)$$

with n = 1, 2, 3,….

The following key takeaways shall be highlighted:

- The delta sigma ADC frequency characteristic is given by the decimation filter
- Above ~1kHz the attenuation increases with 20 dB/decade
- Additional notches suppress frequencies at the multiple of the output sampling frequency f_{sample}
- The delta sigma ADC is especially suitable for slow changing but noise prone signals – such as properties that reflect the temperature of a component or system

3.8.3 Conversion and error calculation

The idealized relationship between output duty cycle and input voltage is given by

$$V_{\mathrm{AIP,ideal}} = DC \cdot 2 \cdot V_{\mathrm{IADC}} \quad (3\text{-}21)$$

. The factor of “2” is added because the ADC output voltage is mapped to half the duty cycle range as stated in Table 7.

The total unadjusted error with respect to the full-scale range can be easily calculated by using the datasheet parameters for “ADC gain error”, “ADC offset error”, “ADC INL” and “ADC DNL”

$$TUE_{\mathrm{FSR}} = \sqrt{ER_{\mathrm{GAIN}}{}^2 + ER_{\mathrm{OFF}}{}^2 + INL^2 + DNL^2} \quad (3\text{-}22)$$

. Since the datasheet parameters are all given in “percentage to full scale range” the conversion to an absolute voltage is obtained by

$$TUE = V_{\mathrm{IADC}} TUE_{\mathrm{FSR}} \quad (3\text{-}23)$$

. The total unadjusted error on a single device is characterized in Figure 48. Note that this characteristic was recorded on an ADC with a slightly higher full scale range, nevertheless the theory and results remain the same.

The error is minimized around the trim voltage but increases with higher input voltage. This contribution is due to the gain error, whereas the offset error, INL and DNL can be assumed constant in magnitude.

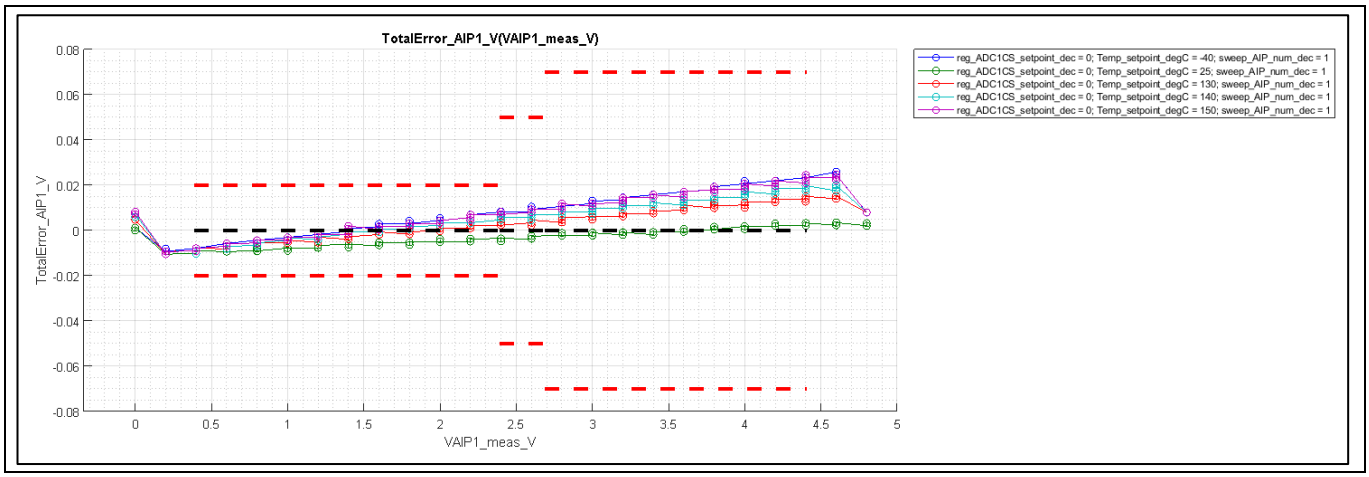


Figure 48 Total unadjusted error versus input voltage

When estimating the measurement error in the application it is therefore meaningful to scale the gain error with the applied input voltage in relation to the full scale range as

$$ER_{\mathrm{GAIN}}(V_{\mathrm{IADC}}) = \frac{V_{\mathrm{AIP}}}{V_{\mathrm{IADC}}} \cdot ER_{\mathrm{GAIN}} \qquad (3\text{-}24)$$

.

3.8.4 End of line calibration

The ADC offset is trimmed in Infineon's production at an input voltage of 2V. A gain calibration is not performed.

In case it is desired to further decrease the total unadjusted error in the application two methods arise:

- Offset trimming in the microcontroller at a different input voltage
- Gain calibration at one or various measurement points

The end of line test capability is often limited to room temperature measurement. This means that an additional temperature dependency of the error quantities must be taken into account to estimate the effectiveness of end of line calibration.

The data shown in Figure 49 and Figure 50 shows the temperature characterization of gain and offset error with respect to the temperature for a typical device and can help to estimate the magnitude of the remaining error after nullifying at a given temperature.

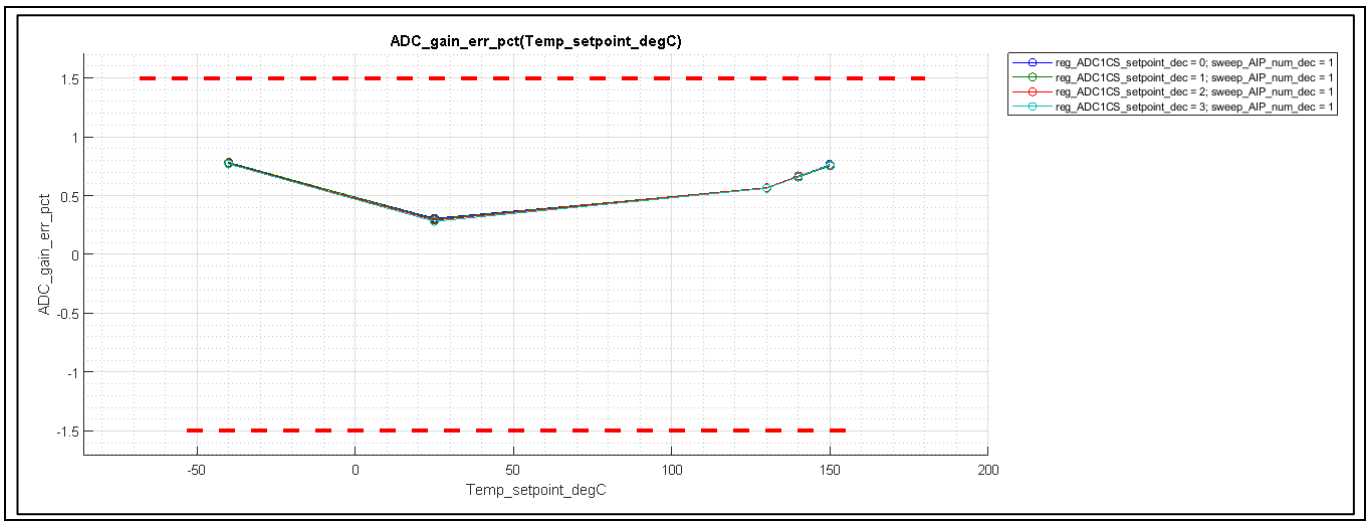


Figure 49 ADC gain error versus temperature

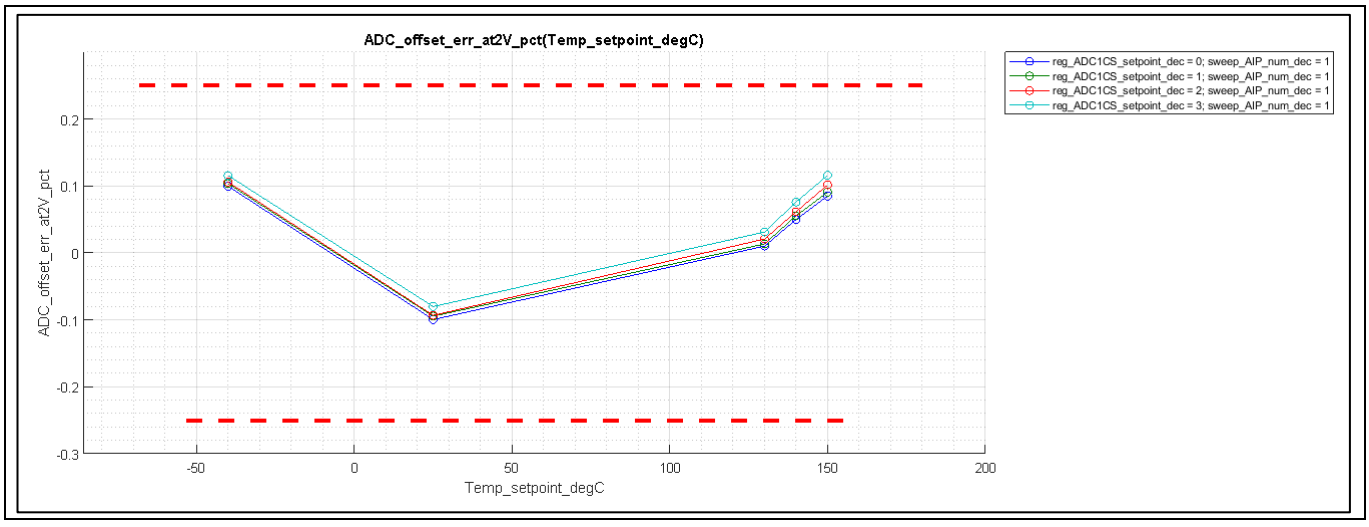


Figure 50 ADC offset error versus temperature

3.8.5 Temperature sensing diode driven measurement

Enabling temperature measurement with on chip sensing diodes on modules such has Infineon HybridPACK™ FS1150R08A8P3 is straight forward. The voltage drop on the diode for a constant current bias is given in the module datasheet. For the EiceDRIVER™ gate driver family a 200µA current source is driven out of the AIP/SASC pin. The ADC ideal measurement range of 3.5V is specifically tailed to the sense diode. Hence for correlating the DATA output of the ADC to the actual chip temperature all required information is given in Figure 51.

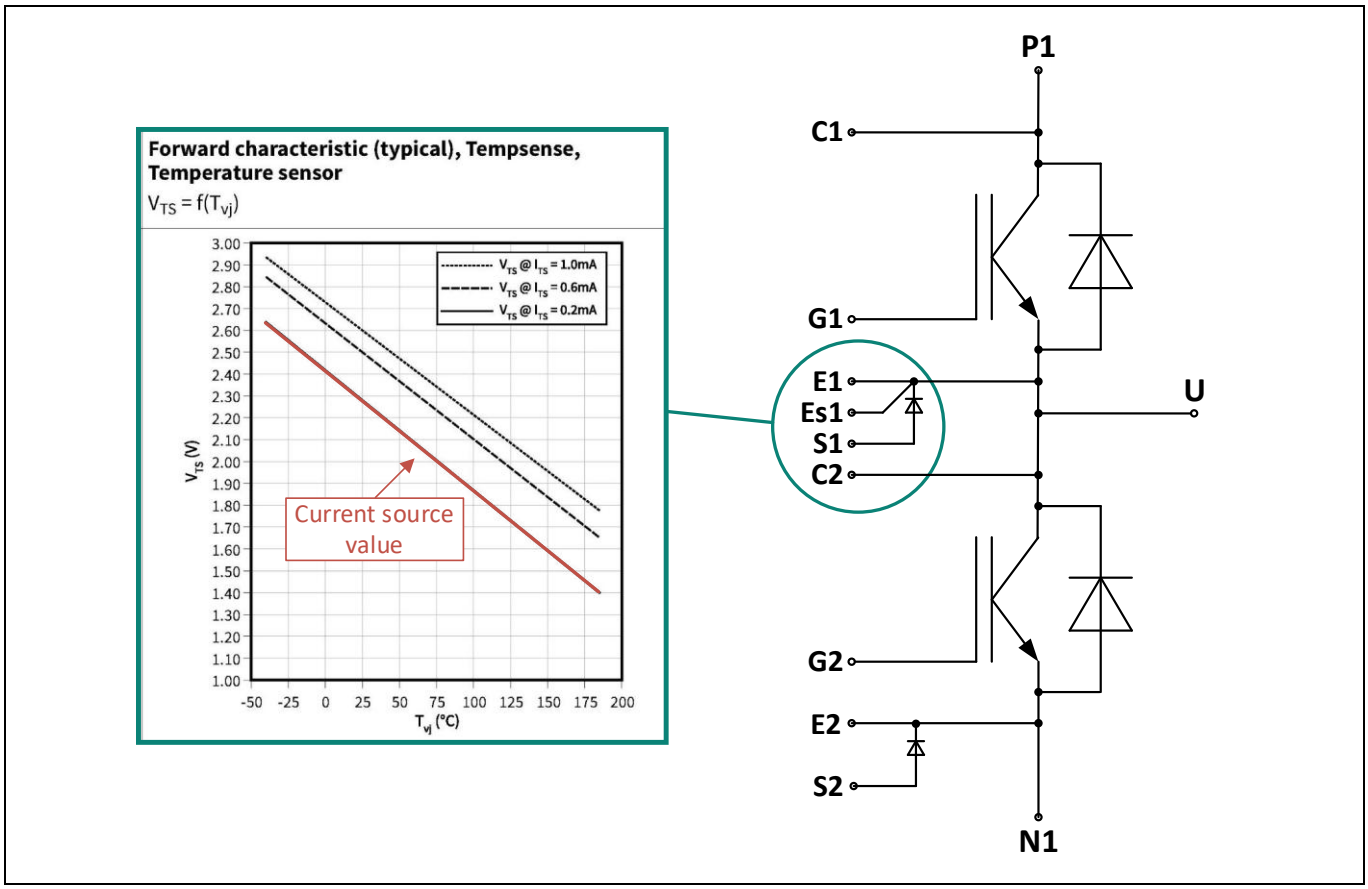


Figure 51 Temperature diode characteristic of FS1150R08A8P3

The on-chip temperature sensing yields the benefit of a defacto delayless real time temperature measurement with a high correlation towards the actual die junction temperature. For more details on this technology please refer to the application note “HybridPACK™ Drive G2 power module Application Hints for the On-Chip Temperature Sensor” (AN-G2-TEMPSENSE).

3.8.5.1 Transient response and signal filter

During switching operation the output voltage V_{ts} on the temperature sensing diode gets disturbed. The duration of the disturbance is given by the IGBT switching time. The magnitude is proportional to the switched current. Therefore, the worst case can easily be identified. An example waveform is given Figure 52, together with the equivalent circuit of Figure 54.

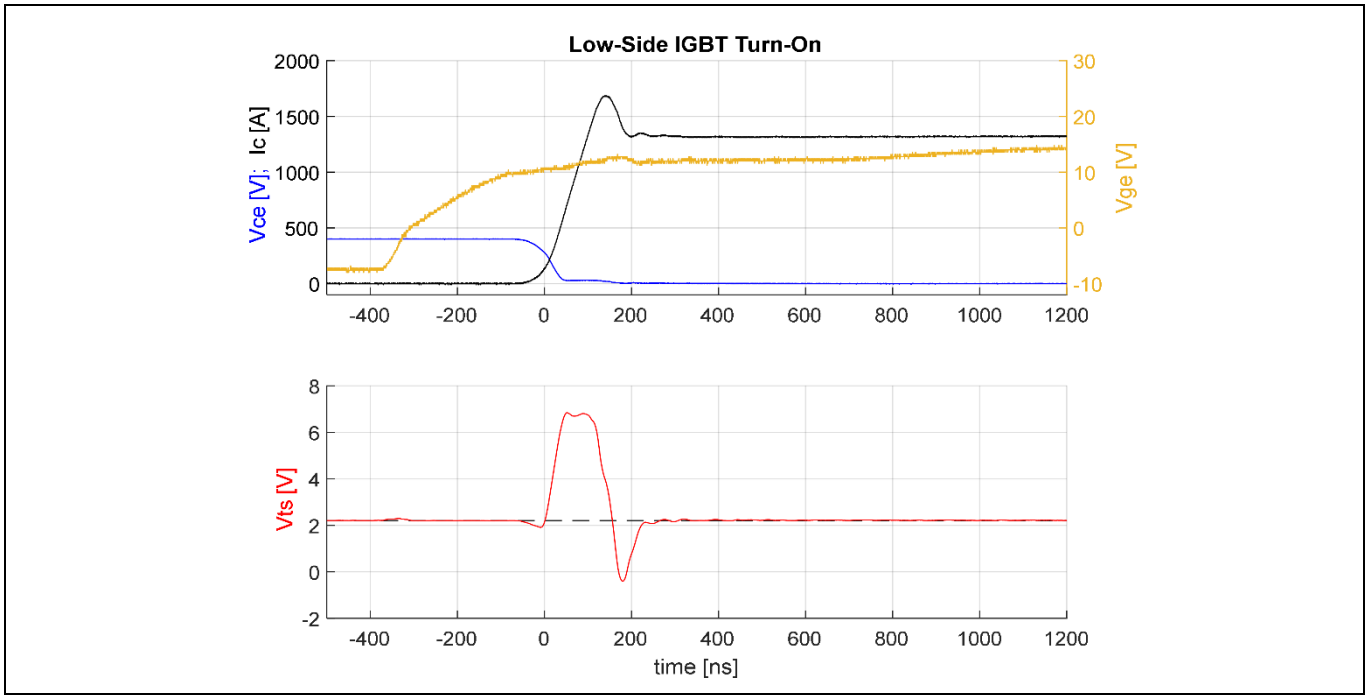


Figure 52 Temperature diode response during switching transient

The peak of V_{ts} must be suppressed to ensure that the voltage can not trigger the SASC functionality which is shared with the AIP pin. This means the following condition must be fulfilled by the filter circuit of Figure 53:

$$V_{\mathrm{AIP,max}} < V_{\mathrm{SASCL,max}} \quad (3\text{-}25)$$

Since the shape of V_{ts} is almost rectangular, the peak voltage on the AIP pin can determined as

$$V_{\mathrm{AIP,peak}} = V_{\mathrm{ts,max}}\left(1 - e^{\frac{-t_{\mathrm{width}}}{R_{AIP}C_{AIP}}}\right) \quad (3\text{-}26)$$

where t_{width} is the duration of the pulse.
Using the example in Figure 52 with the assumption of t_{width} = 200ns and $V_{ts,max}$ = 7V the results can be plotted in Figure 53. When choosing a filter constant of 200ns the peak voltage will remain below 5V.

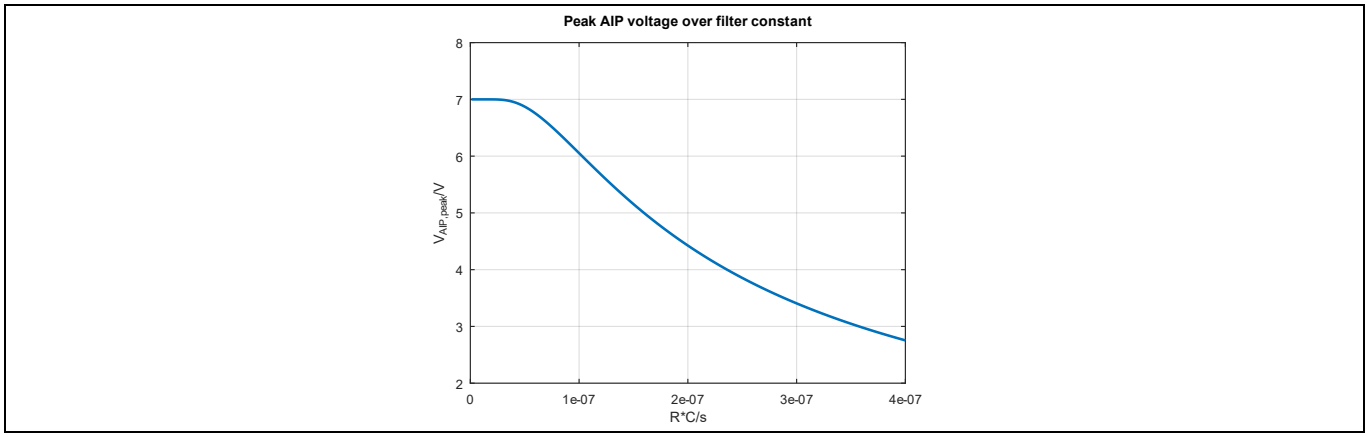


Figure 53 Peak voltage on AIP pin versus filter time constant

The filter constant can for example be achieved with R_{AIP} = 200 Ω resistor value and a C_{AIP} = 1nF capacitor.

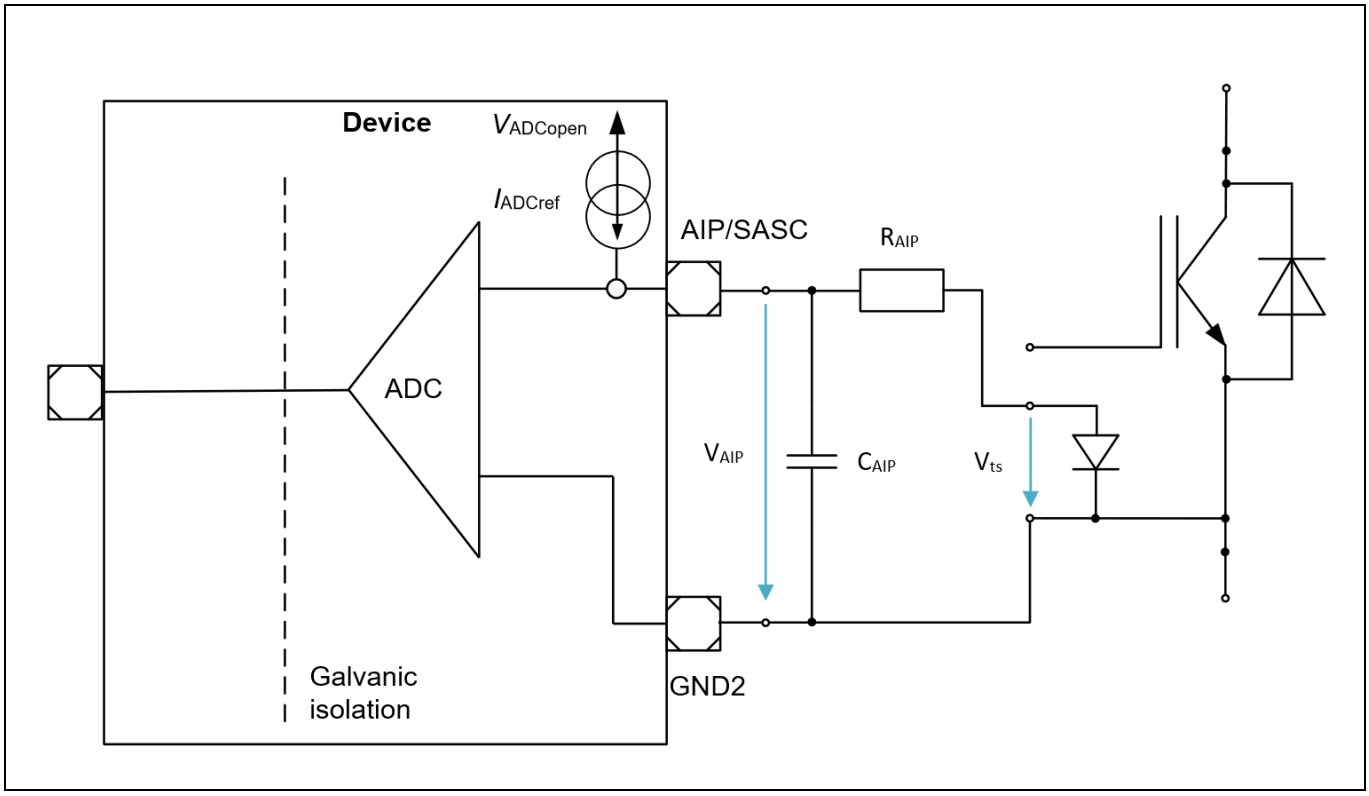


Figure 54 Recommended filter circuit and connection to temperature sensor

Note that the error introduced by the switching transient can be neglected, since it is averaged out over the sampling cycle of ~410µs of the ADC.

3.8.6 NTC driven temperature measurement

To measure the temperature with an NTC two additional resistors are required to set the NTC operating point, see Figure 56:

- R_{PU} to bias the NTC
- R_{PD} to limit the maximum voltage on AIP/SASC for low temperatures to prevent SASC activation

The modelling equation for the NTC resistor temperature dependence is usually given by

$$R_{NTC}(T) = R_{25} e^{B_{25/100}\left(\frac{1}{T+273.15\,K} - \frac{1}{298.15\,K}\right)} \quad (3\text{-}27)$$

. As the name “negative temperature coefficient” already states the resistance reduces over temperature. Typical values for the material constant “B” are in the range of 3000 Kelvin to 4000 Kelvin und usually defined between two temperature reference points. In Figure 55 the NTC characteristic for HybridPACK™ FS03MR12A6MA1LB is plotted as an example.

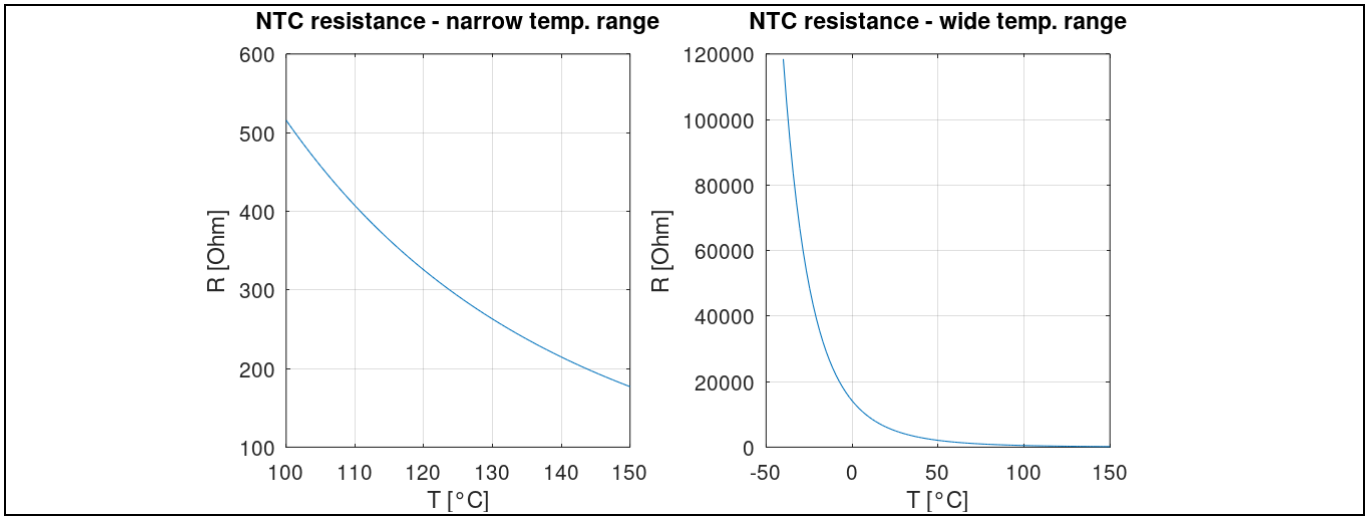


Figure 55 NTC resistance over different temperature ranges

The range of interest is around the absolute maximum rating of the power module at hot. For FS03MR12A6MA1LB this is up to 150°C. This is also the range where the NTC resistance is more linear versus the temperature, as can be seen in Figure 55.

The resulting parallel resistance between R_{NTC} and R_{PD} is then given by

$$R_{\mathrm{PAR}}(T) = \frac{R_{NTC}(T)R_{PD}}{R_{NTC}(T) + R_{PD}} \qquad (3\text{-}28)$$

.

At cold temperatures the NTC resistances rises by several magnitudes.

This can be used for simplification of the calculation procedure:

- At cold the R_{PAR} is given by R_{PD}, since $R_{PD} << R_{NTC}$

For the temperature measurement a usage range needs to be defined, it is hereafter referred to as T_{min} and T_{max}.

The boundary conditions for the calculation are as follows:

- At the lowest system temperature $V_{AIP/SASC}$ may not rise above $V_{SASCH,min}$
- The measurement range T_{min}, T_{max} shall be within the ADC quantization range
- At T_{min} the full scale range of the ADC V_{IADC} shall be used

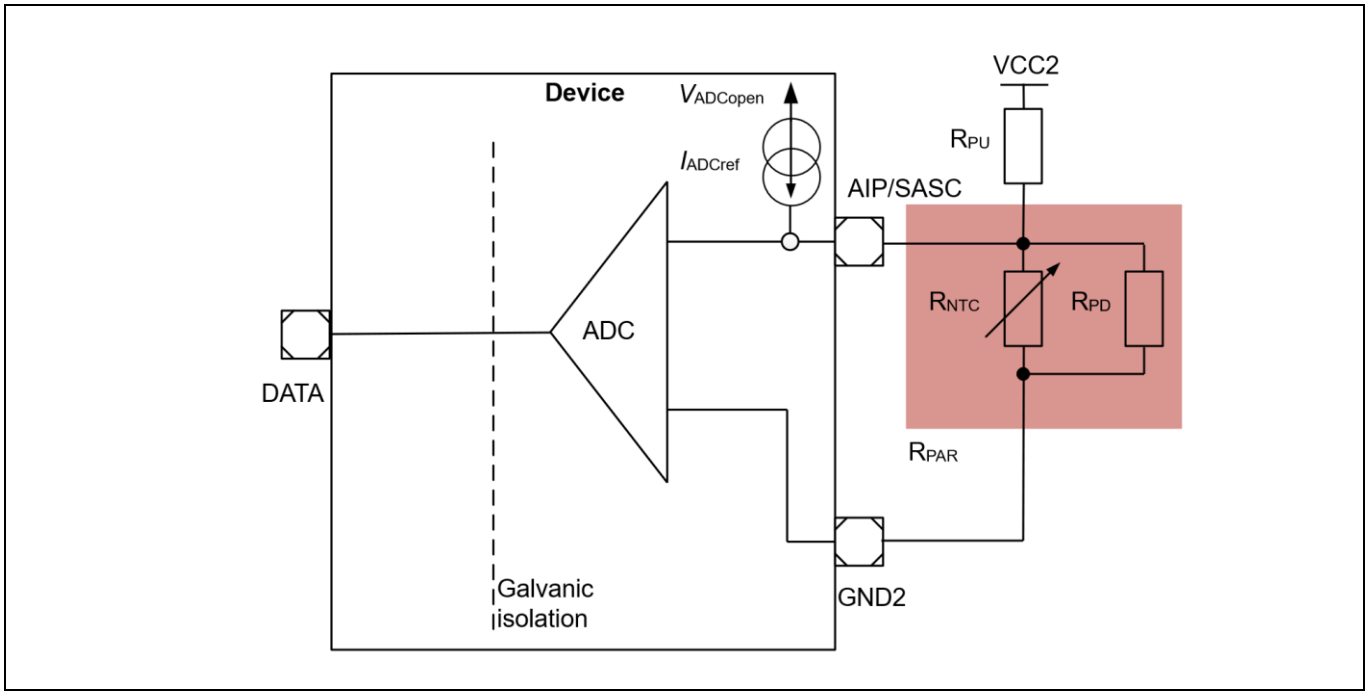


Figure 56 ADC configuration for NTC driven temperature measurement

The first equation is given by the voltage divider for very low temperature, where R_{PAR} is given by R_{PD}

$$V_{\mathrm{SASCH,min}} = V_{\mathrm{VCC2}} \frac{R_{PD}}{R_{PU} + R_{PD}} \quad (3\text{-}29)$$

. The second equation introduces the constraint that at T_{min} the ideal ADC full scale range voltage V_{IADC} shall be applied to the input of the ADC. For any temperature higher than T_{min} the resistance of R_{NTC} decreases and the voltage on the ADC input will be lower.

$$V_{\mathrm{IADC}} = V_{\mathrm{VCC2}} \frac{R_{\mathrm{PAR}}(T_{min})}{R_{\mathrm{PAR}}(T_{min}) + R_{PU}} \quad (3\text{-}30)$$

Inserting and refactoring yields

$$R_{\mathrm{PU}} = \frac{V_{\mathrm{VCC2}}}{V_{\mathrm{SASCH,min}} V_{\mathrm{IADC}}} R_{NTC}(T_{min}) \left(V_{\mathrm{SASCH,min}} - V_{\mathrm{IADC}}\right) \quad (3\text{-}31)$$

and

$$R_{\mathrm{PD}} = \frac{R_{\mathrm{PU}} V_{\mathrm{SASCH,min}}}{V_{\mathrm{VCC2}} - V_{\mathrm{SASCH,min}}} \quad (3\text{-}32)$$

. The resulting transfer function is then given by

$$V_{\mathrm{AIP}} = \frac{R_{\mathrm{NTC}} R_{\mathrm{PD}}}{R_{\mathrm{PU}} R_{\mathrm{NTC}} + R_{\mathrm{PU}} R_{\mathrm{PD}} + R_{\mathrm{NTC}} R_{\mathrm{PD}}} \left(R_{\mathrm{PU}} I_{\mathrm{ADCref}} + V_{\mathrm{VCC2}}\right) \quad (3\text{-}33)$$

For a given ADC input voltage, the measured temperature can be derived in two steps. First step is to calculate the R_{NTC} based on the measured ADC voltage to be

$$R_{\mathrm{NTC}} = \frac{V_{\mathrm{AIP}} R_{\mathrm{PU}} R_{\mathrm{PD}}}{R_{\mathrm{PU}} R_{\mathrm{PD}} I_{\mathrm{ADCref}} + V_{\mathrm{VCC2}} R_{\mathrm{PD}} - V_{\mathrm{AIP}} (R_{\mathrm{PU}} + R_{\mathrm{PD}})} \quad (3\text{-}34)$$

. Then the temperature can be derived from

$$T = \frac{1}{\ln\left(\frac{R_{\mathrm{NTC}}}{R_{25}}\right)\frac{1}{B_{25/100}} + \frac{1}{298.15\ \mathrm{K}}} - 273.15\ \mathrm{K} \quad (3\text{-}35)$$

.

3.8.6.1 Component calculation example

The inputs

- V_{VCC2} = 18 V
- T_{min} = 120 °C, T_{max} =150°C
- $V_{SASCH,min}$ = 6.3 V
- $R_{ntc}(T_{min})$ = 320 Ohm
- V_{IADC} = 3.5 V

Yield the following results

- R_{pu} = 731 Ohm , R_{pd} = 392 Ohm

3.8.6.2 Measurement error calculation example

The error calculation is performed based on the NTC design of 3.8.6.1. Since the employed equations are non-linear Matlab is used to model the statistical variation in the following quantities: V_{VCC2}, R_{pu}, R_{pd}, $I_{adc,ref}$. For the ADC error calculation, the formulas of chapter 3.8.3 are used.

The NTC data is taken from Infineon's first generation SiC HybridPACK™ module like the FS03 series:

- B = 3411 K
- R_{25} = 5 kΩ

The following values are used for the ADC error calculation relative to the full scale range V_{IADC}:

- INL = 0.073%
- DNL = 0.025%
- ER_{GAIN} = 1.5%
- ER_{OFF} = 0.25%
- V_{IADC} = 3.5V

Note that this error calculation is not exhaustive since the NTC is assumed to be ideal.

In order to obtain the plots shown in Figure 57 and Figure 58 the following computation steps are carried out:

1. Sweep the ideal measured ADC voltage in n steps, hereafter referred to as "$V_{adc,ideal}$"
2. Calculate the ideal NTC resistance by using equation (3-30)
3. Calculate the ideal NTC temperature by using the result from (2) in equation (3-31)
4. Calculate the maximum deviation in the ADC voltage "ΔV_{adc}" at the "n-th" step by using equation (3-18)
5. Repeat steps 1 to 3 with the result from step 4 and vary the quantities V_{VCC2}, R_{pu}, R_{pd}, $I_{adc,ref}$ statistically within a given tolerance to obtain the maximum and minimum temperature estimator

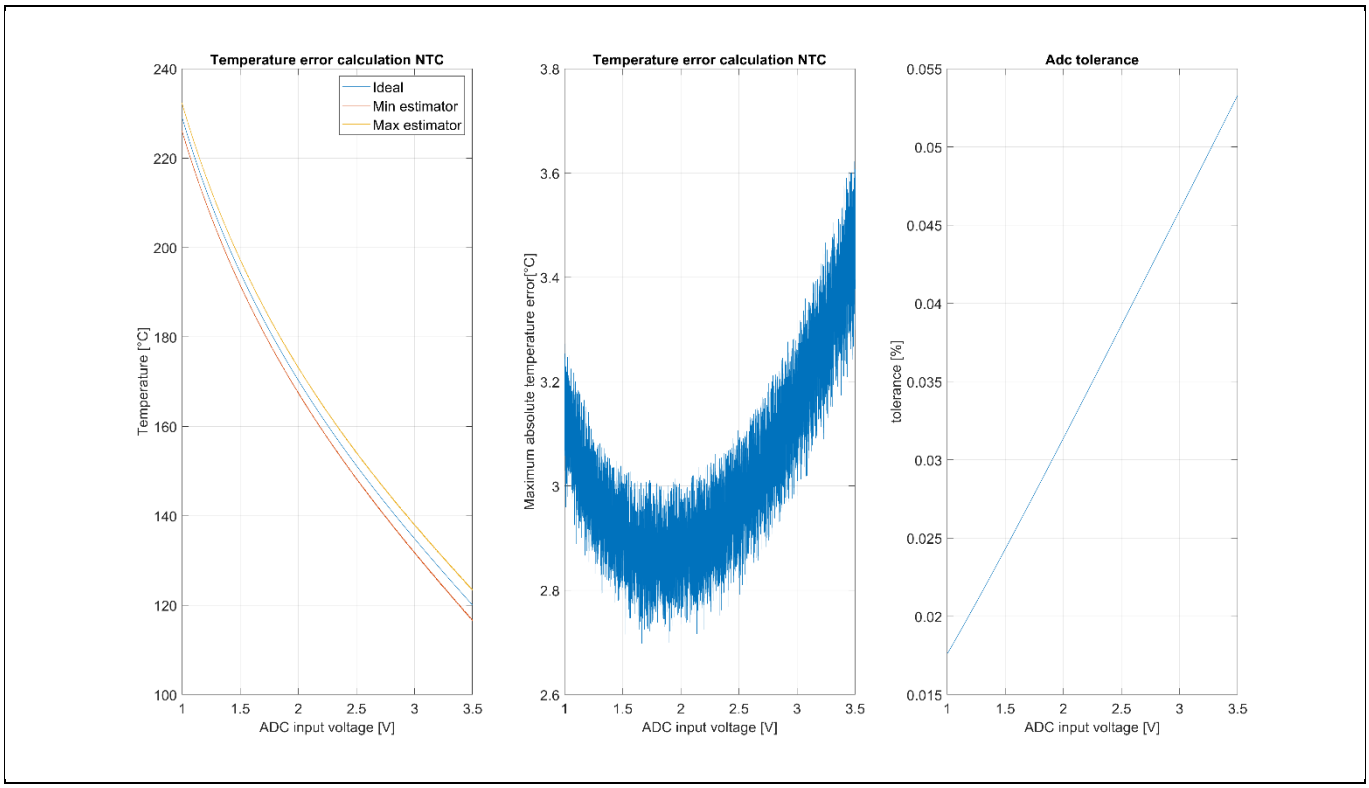


Figure 57 Error estimation assuming a 1% tolerance on V_{VCC2}, R_{pu}, R_{pd}, $I_{adc,ref}$

The measurement error is increasing with the input voltage because of the gain error that is scaled with the ADC input voltage according to equation (3-20).

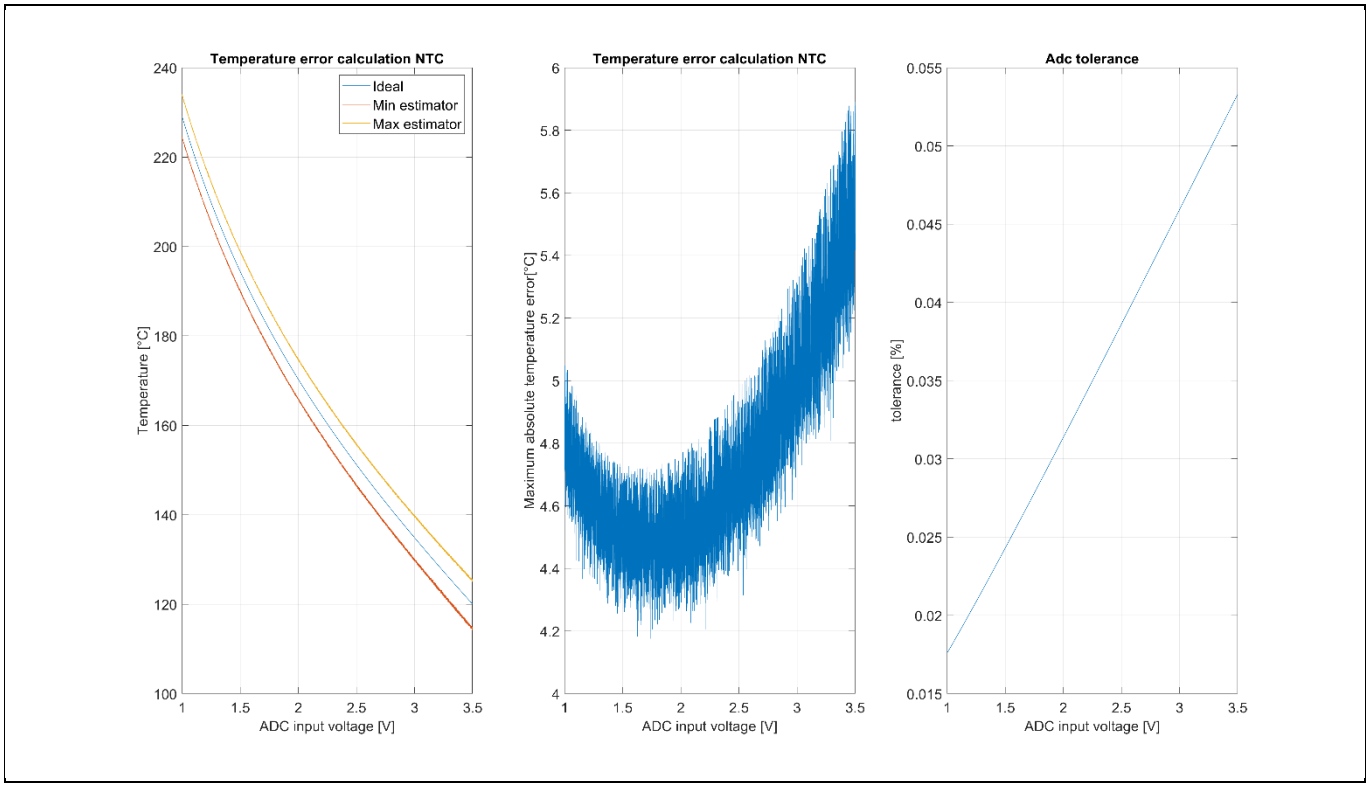


Figure 58 Error estimation assuming a 2% tolerance on V_{VCC2}, R_{pu}, R_{pd}, $I_{adc,ref}$

3.9 Safety controls

The EiceDRIVER™ gate driver implements a primary and secondary side safety feature to allow a transition into the system safe state by the control of an external safety logic should the microcontroller fail. The safe state transition is associated with either a turn-on or turn-off of the gate driver output stage.

The output stage can be controlled through the following inputs:

- INP/INN – PWM input pins, can beconnected to a microcontroller
- SI1/SI2 – primary side safety input pins, can be connected a primary side safety logic
- SASC – secondary side safety input pin, can be connected to a secondary side safety logic

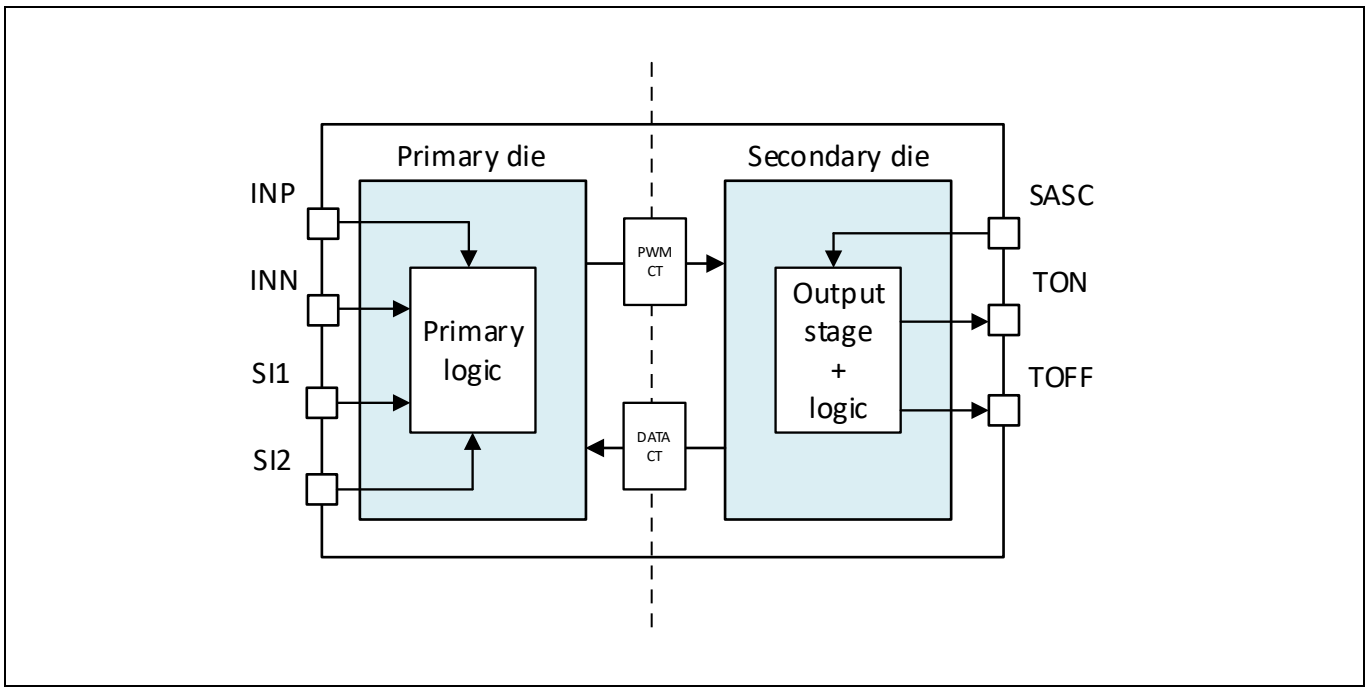


Figure 59 Illustration of output stage control through PWM and safety inputs

There is distinct priority for how each individual path controls the output stage:

1. *= highest : SASC turn-on*
2. *: SI1/SI2 turn-on = ASCP_ON and turn-off = PWM_DISABLE*
3. *: INP/INN turn-on and turn-off only during PWM_ENABLE*

Note that SASC may only be used to force turn-on the gate driver from the secondary, it can not be used for force turn-off in contrast to the SI1 and SI2 pins. Fore detailed information about the safey use case please refer to the safety manual for this device.

3.9.1 Primary side safety control

The SI1 and SI2 pin serve multiple functions:

- Transition into ASCP_ON mode to turn-on the output stage – ingnore INP/INN input
- Transition into PWM_Enable
- Transition into PWM_Disable
- Clear sticky errors

In the application the SI1 and SI2 pins of two gate drivers in a half-bridge configuration are meant to be connected crossed over as depicted in Figure 60.

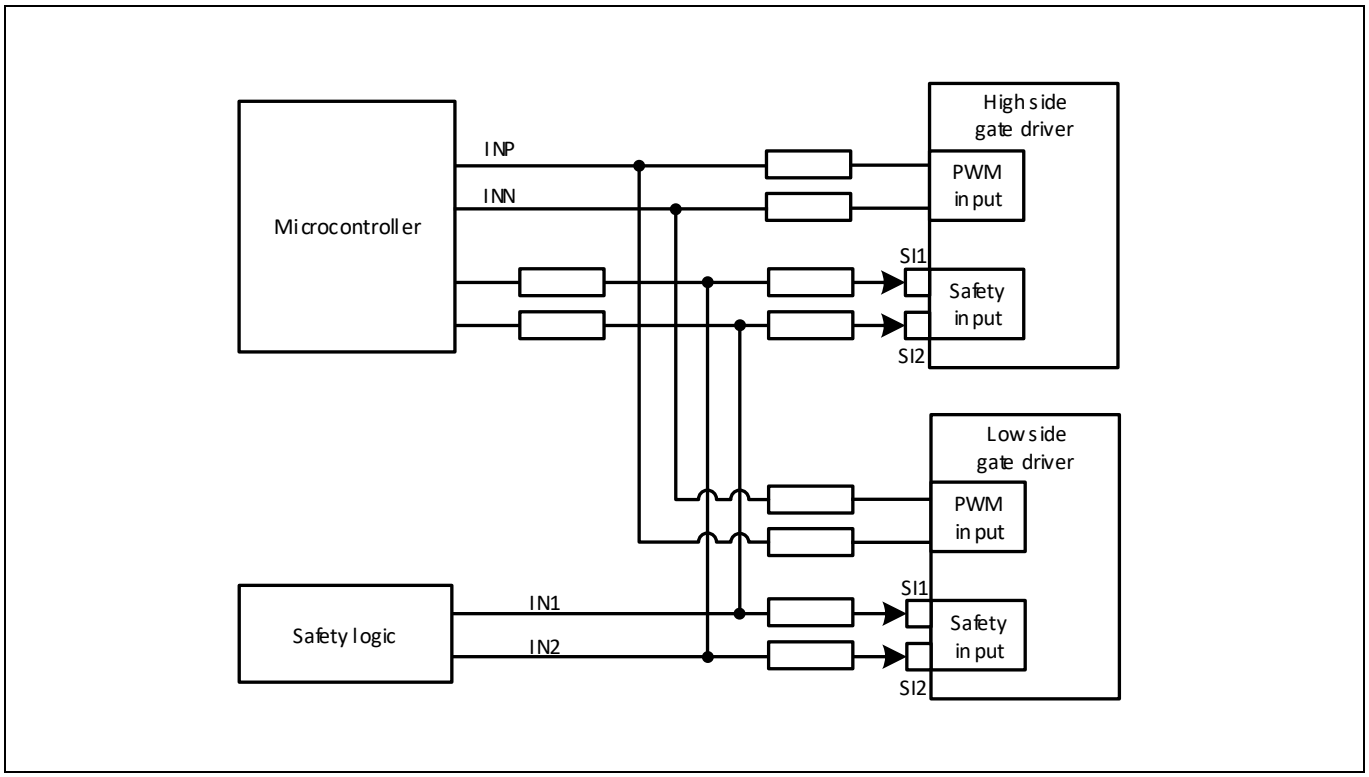


Figure 60 Connection of safety pins in a half bridge topology

This connection ensures by the simplicity of its concept that when ASCP is activated on one gate driver the other driver is automatically in PWM_Disable mode. This fact is further depicted in Table 8 with the assumed configuration of Figure 60.

Table 8 Driver operating mode in half bridge configuration

IN1	IN2	High side driver	Low side driver
0	0	PWM_Disable	PWM_Disable
0	1	PWM_Disable	ASCP_ON
1	0	ASCP_ON	PWM_Disable
1	1	PWM_Enable	PWM_Enable

Note that a direct transition from ASCP_ON back to PWM_Enable is not possible. It is only possible to transition back into PWM_Enable by entering PWM_Disable first. This is because timings have to be respected to ensure that the gate driver in ASCP_ON had time to turn-off the output before resuming PWM operation.

3.9.1.1 Operating mode transitioning

The SI1 and SI2 pins also control the regular operating mode transitioning and clear functionality. The mechanism of changing the operating mode is implemented by a “safety transition timer” t_{safety}. This timer is reset whenever SI1 or SI2 change their logic state. Only when the time reaches t_{safety} the status of SI1 and SI2 is captured and assumed for the next state transition. A small deglitching filter time $t_{SIglitch}$ is added internally, too.

This transition mode is introduced to allow a direct state transition from SI1 = SI2 = 0 to SI1 = SI2 = 1 without an intermediate transition to SI1 = 1 and SI2 = 0 or SI1 = 0 and SI2 = 1. A detailed timing diagram and example is provided in the datasheet.

Additional delays are introduced between the operating mode transitions. These delays are visible in Figure 15 but are also summarized in Figure 61 for simplicity.

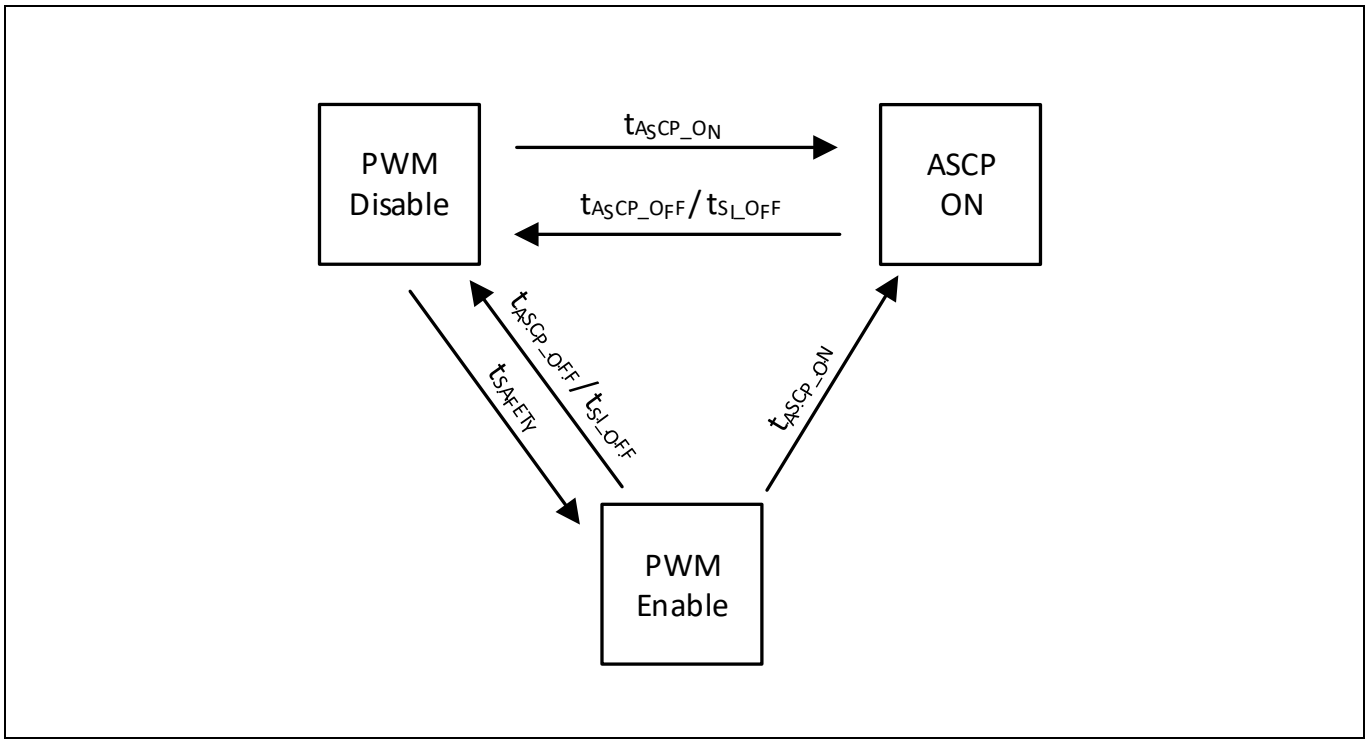


Figure 61 Delays between mode transitions

The delay t_{ASCP_ON} is around 3 to 4 times the value of t_{ASCP_ON} / t_{SI_OFF}. This way in the half bridge configuration of Figure 60 during ASCP_ON activation of one driver the opposite gate driver will have enough time to turn-off the power transistor.

With the introduction of these timings inside the gate driver the need for the external safety logic to implement delays becomes ASC related delays becomes obsolete.

Note that a transition from PWM Disable to PWM Enable is also associated with the attempt to clear any previous error event.

3.9.1.2 Restrcited transitions

A direct transition from ASCP_ON to PWM Enable is not possible. The driver will remain in ASCP_ON otherwise. This transition is suppressed due to the implications of Table 8 to ensure that the gate driver in ASCP_ON has sufficient time to turn-off the output before the other gate driver is in PWM Enable mode. Otherwise an unintended OCP or DESAT event could be triggered.

The transition from PWM Disable to PWM Enable is only possible when a direct transition of SI1 = SI2 = 0 to SI1 = SI2 = 1 takes place for the same reason as previously explained.

3.9.1.3 Priority of ASCP_ON in case of an error event

As shown in Figure 59 the primary side safety control is interfacing with the primary side logic. It is relying on the same CT transmission path as the regular PWM switching signal.

3.9.2 Secondary side active short circuit SASC

The EiceDRIVER™ gate driver family hosts the functionality to force turn-on the gate driver output through the secondary side SASC pin. The SASC feature is a means to initate the system safe state from the secondary side. It is applicable when the inverter is driving PMSMs (permanent magnet synchronous machines), where due to the back EMF voltage the motor windings need to be actively shorted during free-wheeling. This may prevent an unintended voltage build up at the DC-link capacitor and component level damage. For details about the safety use case please refer to the safety manual.

3.9.2.1 Priority of SASC in case of an error event

The SASC feature can be used to force turn-on the output stage even during numerous error events. There are only three cases during which SASC will be inhibited or overruled:

- DESAT or OCP error event
- Gate monitoring event
- Output stage monitoring event

During these events the output stage will perform the corresponding safe transition, such as a safe turn-off or tristate. For details please refer to the datasheet.

SASC can be reapplied after the error event was processed. There is a minimum retry time t_{SASC_retry} required for which SASC needs to stay “low” before attempting another turn-on. On the rising edge of SASC the internal logic tries to clear any previous errors.

This retry scheme is common, since when entering the active short circuit state in the inverter excessive currents may cause a false triggering of DESAT or OCP.

An example scenario for the priority of DESAT over SASC is shown in Figure 62.

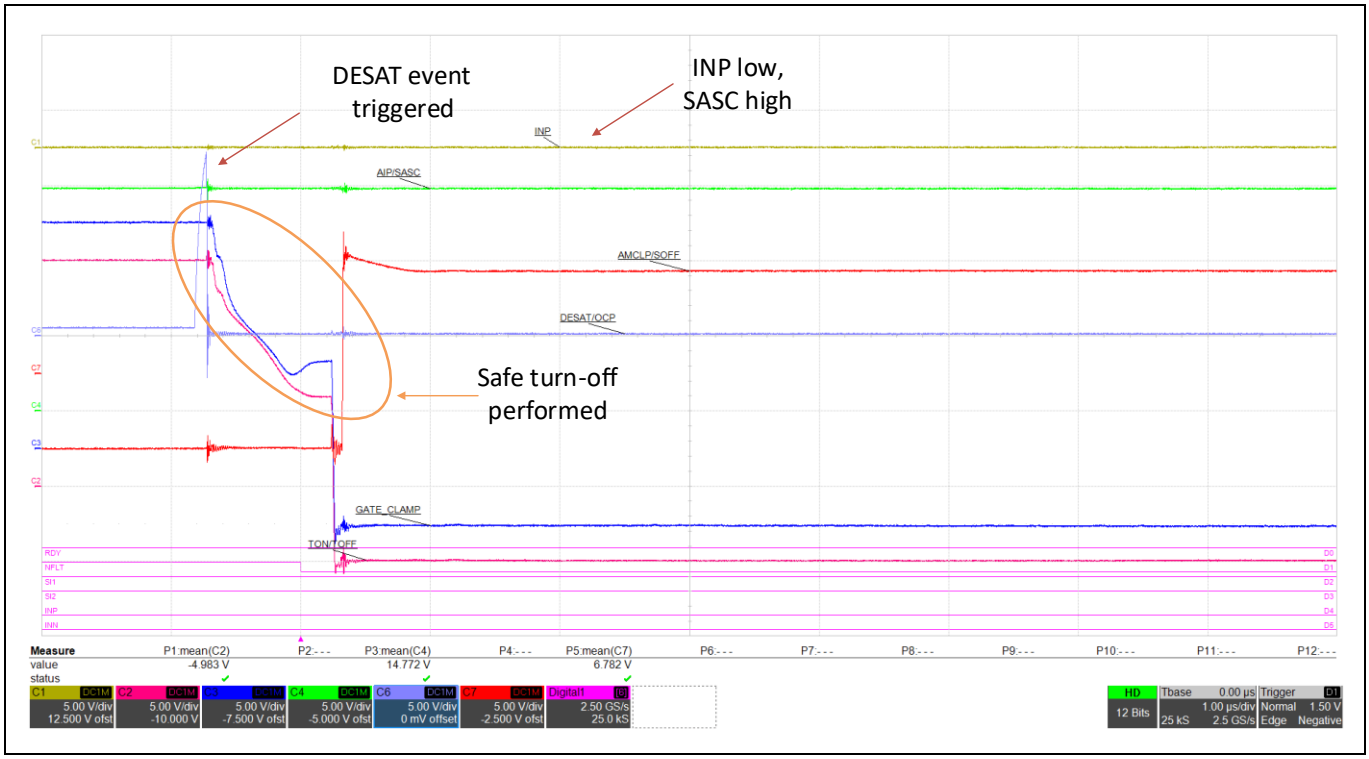


Figure 62 DESAT event during SASC activation

3.9.2.2 Actuating the SASC from a logic level

The SASC functionality is triggered by pulling the voltage on the AIP/SASC pin above V_{SASCH}. The input voltage range on the AIP/SASC is up to V_{VCC2}. In order to apply the required voltage level it is recommended to use an external discrete level-shifter circuit. An example schematic is shown in Figure 63.

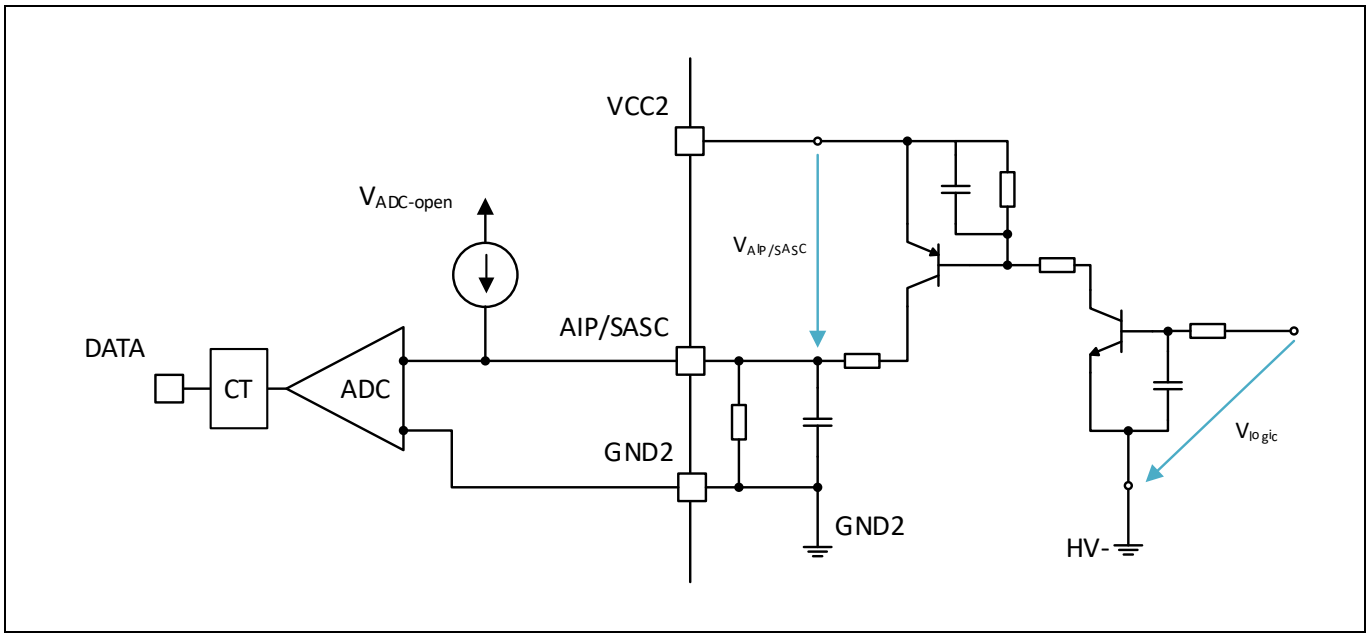


Figure 63 SASC actuation from logic level with a level shifter

The input voltage V_{logic} can be driven from a 3.3 V or 5 V logic. It is then level-shifted and the AIP/SASC pin is pulled up to VCC2 to activate the SASC function. When SASC is not activated an external pull-down resistor pulls the voltage on AIP/SASC to GND2.

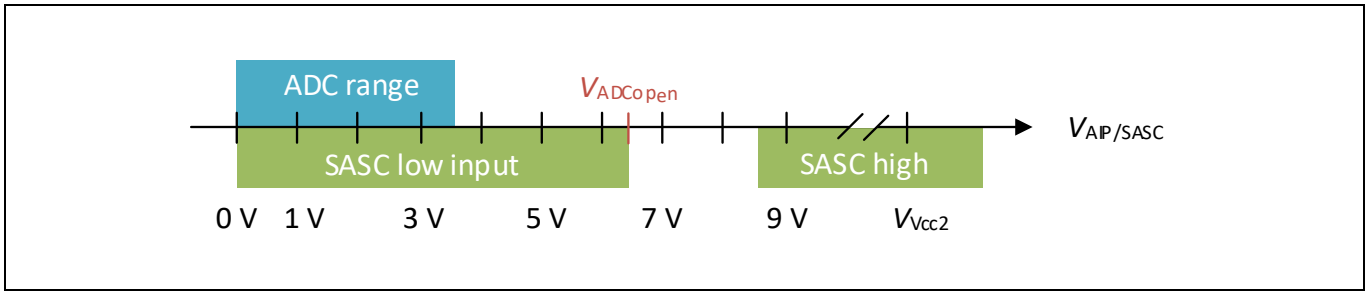


Figure 64 Illustration of ADC and SASC range

In case of a pin open failure on the AIP/SASC pin the internal current source will pull-up the AIP/SASC pin voltage to a maximum of $V_{ADCopen}$ to ensure that SASC is not activated unintentionally.

3.9.2.3 SASC detection on primary side

Upon the activation of the SASC logic on the secondary side there is a means of detecting the activation from the primary. The “SASC activation warning” bit will be set in the DATA signal. Note that also any other error event occurring due to SASC activation will be correctly reflected in the DATA stream as described in chapter DATA read-out via PWM coding.

3.10 Shoot Through Protection

The EiceDRIVER™ gate driver family 1EDI3035AS, 1EDI3038AS, 1EDI3025AS, 1EDI3026AS and 1EDI3028AS implements an active shoot-through protection (STP) function to prevent both highside and lowside switches to be activated simultaneously. If the device is in ASCP_ON mode or in a valid transition to ASCP_ON mode, the shoot-through protection functionality is overruled and RDY switches to “high”, see chapter 3.1. This also holds true when activating the secondary side active short circuit.

The STP function consists of the following sub features, all contributing to the prevention of unintended cross current:

- Dead time monitor with dead time extension
- Inhibit of turn-on when INN = high
- Keep sate protection

For the correct function of the STP protection the PWM signals from the high side and low side are cross coupled on the primary side as shown in Figure 65. The PWM signal of one gate driver is fed to the other gate driver’s inverting PWM input pin INN.

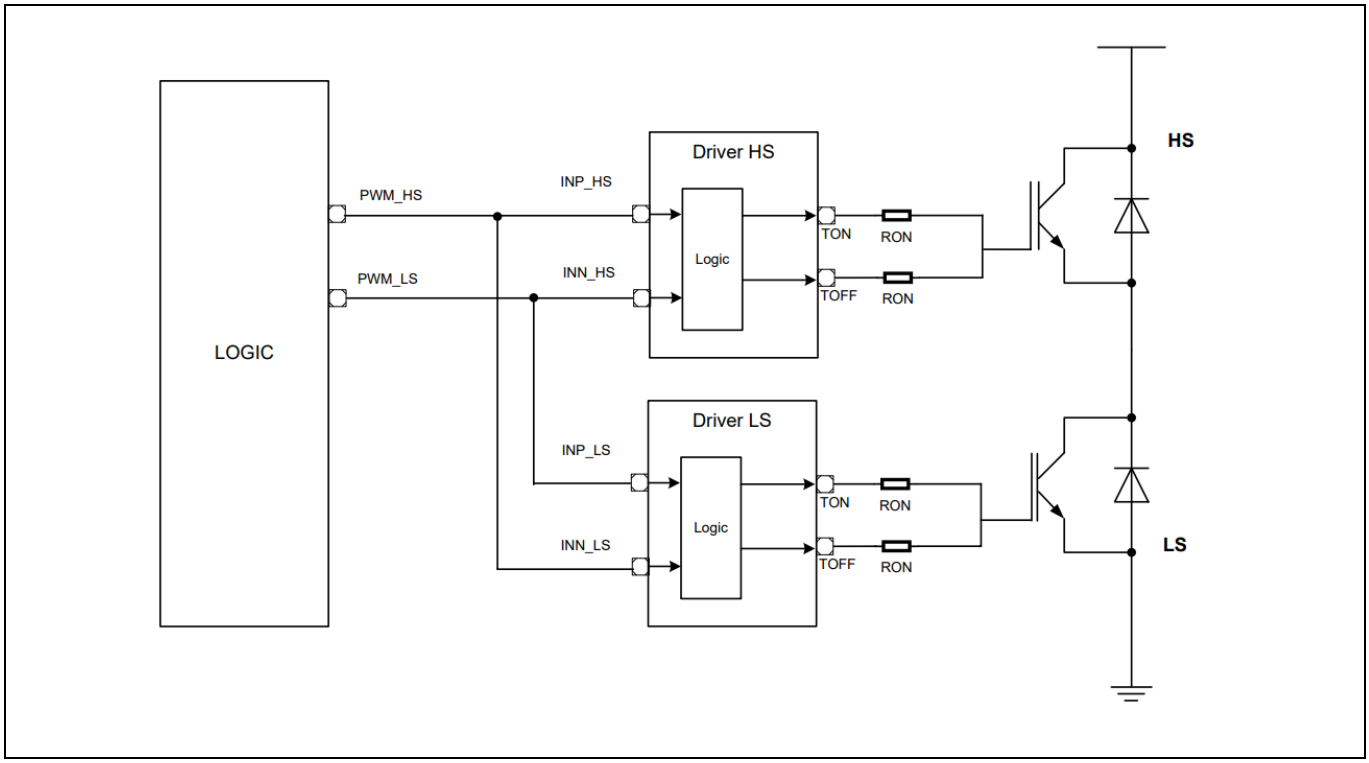


Figure 65 Shoot-though protection feature description

3.10.1 Dead time supervision

When the absolute value of the time between the falling edge of INN and the rising edge of INP are below t_{DEAD}, the deadtime is internally increased to t_{DEAD} at the output stage. The deadtime warning Bit BIT4 in DATA1 frame is also set to “high” and is reported at least once to observe the violation. Since it is a warning bit, it self clears as soon as the condition for warning is gone.

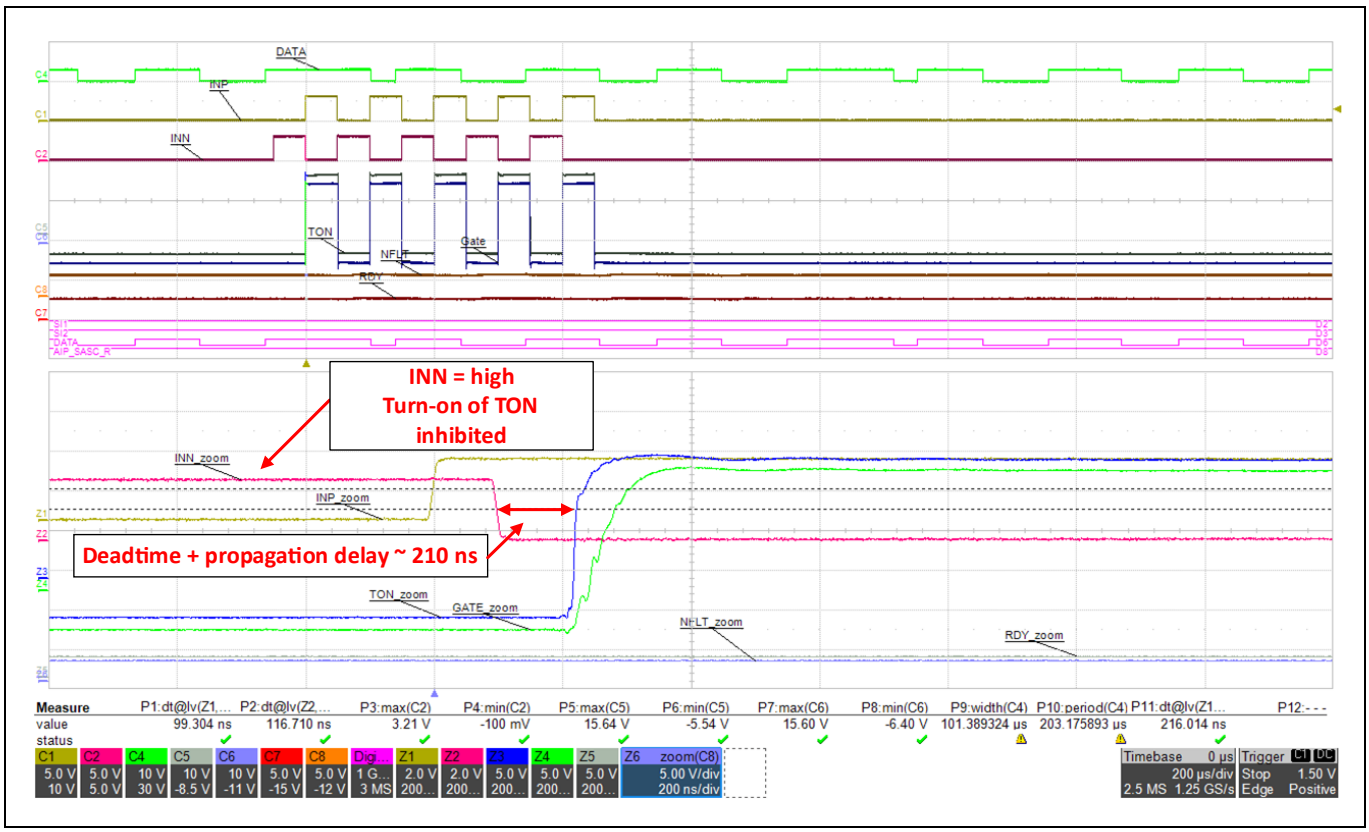


Figure 66 Example of dead time violation and automated dead time extension

In Figure 66 a measurement example shows the principle of the dead time supervision. In this case the rising edge of INP is preceding INN. The turn-on of TON is delayed by t_{DEAD0} + t_{PDON} starting at the falling edge of INN.

The dead time supervision is implemented by the means of a simple counter. The counter is started upon the falling edge of INN and inhibits INP until it has reached t_{DEAD}. Since the the STP function is implemented on the primary chip the output stage will always react with an additional delay of t_{PDON}.

It is important to note that, when the gate driver extends the deadtime, it implies that there is a fault in the microcontroller. The dead time supervision must not be used to generate the dead time during regular switching operation.

3.10.2 Keep state and STP keep error

When INP (or INN) goes “high” when INN (or INP) is already “high”, the gate driver enters into keep state mode. During keep state the output stage remains high. A timer is started on the rising edge of INN. When the timer exceeds $t_{keepstate,max}$ the “STP keep error” reaction is initated and the output turns off. RDY is set to “low”. The STP keep error bit in BIT5 DATA1 frame is set to “high” and the “deadtime warning” bit BIT4 in DATA1 frame is also set to “high”.

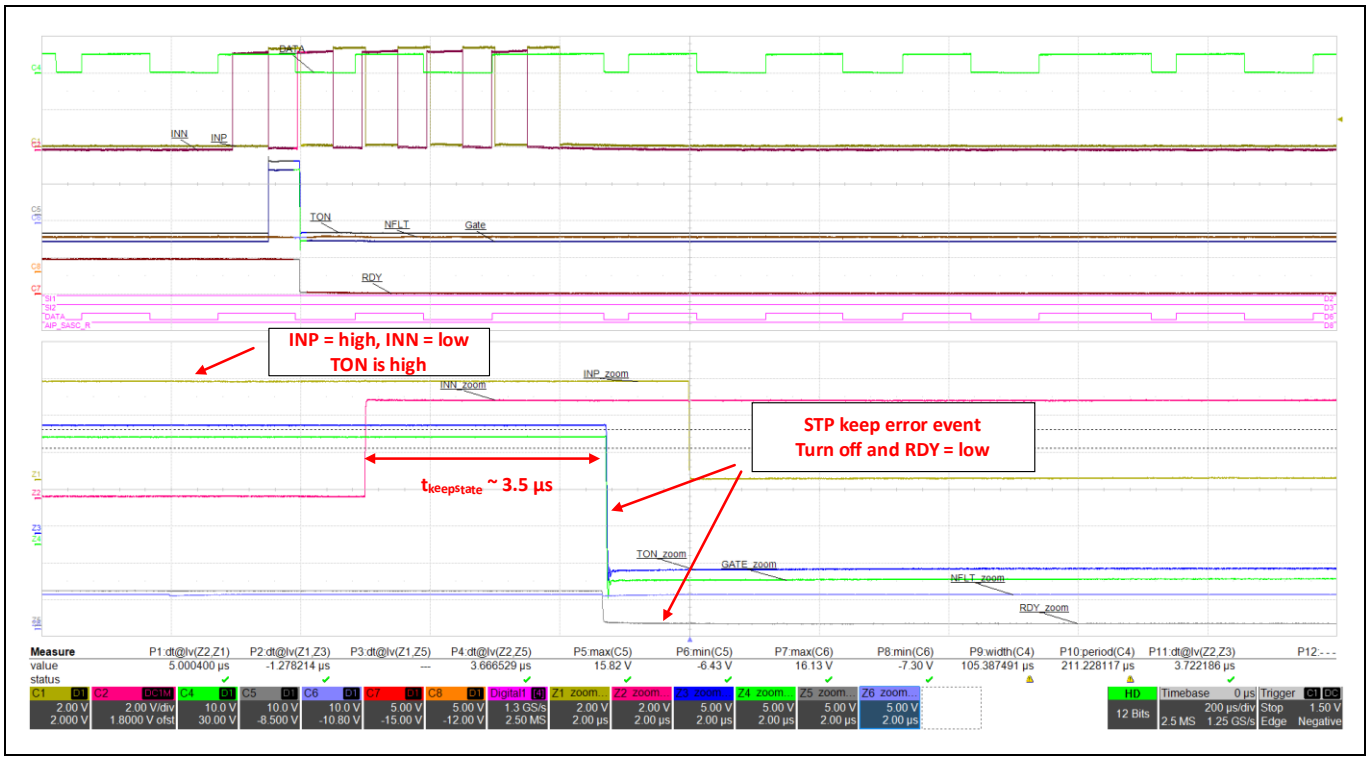


Figure 67 Keep state example with error reaction

The example given in Figure 67 demonstrates the intentional triggering of keep state, followed by an “STP keep error event” that leads to a turn-off of the output stage and RDY goes low.

The keep state feature is implemented to:

- Increase the system robustness against injected noise or short spikes
- Remove the need for pulse suppression filtering on INP/INN to enable the highest timing accuracy
- Enable advanced system diagnostic capabilities during start-up, see chapter 4

3.10.3 Filter on INP and INN

It is recommended to use filter capacitances C_{INP} and C_{INN} in combination with R_{INP} and R_{INN} as shown in Figure 68. The values of the filter capacitances C_{INP} and C_{INN} are to be chosen such that the PWM signal to INP is at least 1 ns delayed after the PWM signal to INN. This is recommended to prevent any inadvertent bridge shorts, for example should the PWM signals from the microcontroller be shorted and rise simultaneously.

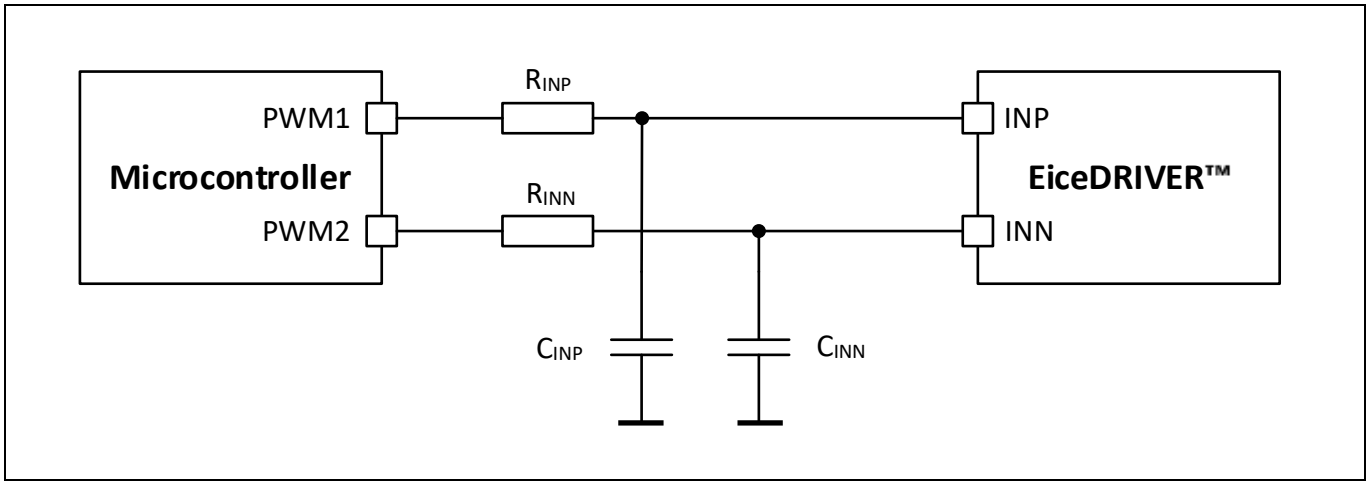


Figure 68 Input filter capacitance configuration on INN and INP

When no external filter capacitances are used or when the dimensioning is not following the previously given advice then during the event of INN and INP going high at the same time a race condition applies.

Depending on which input receiver is faster, the following two scenarios may occur:

- Case 1: INP is registered first and the output stage turns-on but enters keep state, see 3.10.2
- Case 2: INN is registered first and the turn-on through INP is inhibited

In the extremely unlikely situation when the counterpart gate driver in a half-bridge configuration has an opposite effect of propagation delays on its INP and INN pins, it can also enter into a keep state where its output is also “high”. This can result in a bridge short. Hence to avoid a bridge short, it is recommended to use different filter capacitances on INN and INP as suggested above. It is also pointed out that DESAT and OCP will still be active under this condition and can be used to detect a bridge short.

These cases are further elaborated below. Intentional delays between INP and INN are introduced to show the behavior of the keep state.

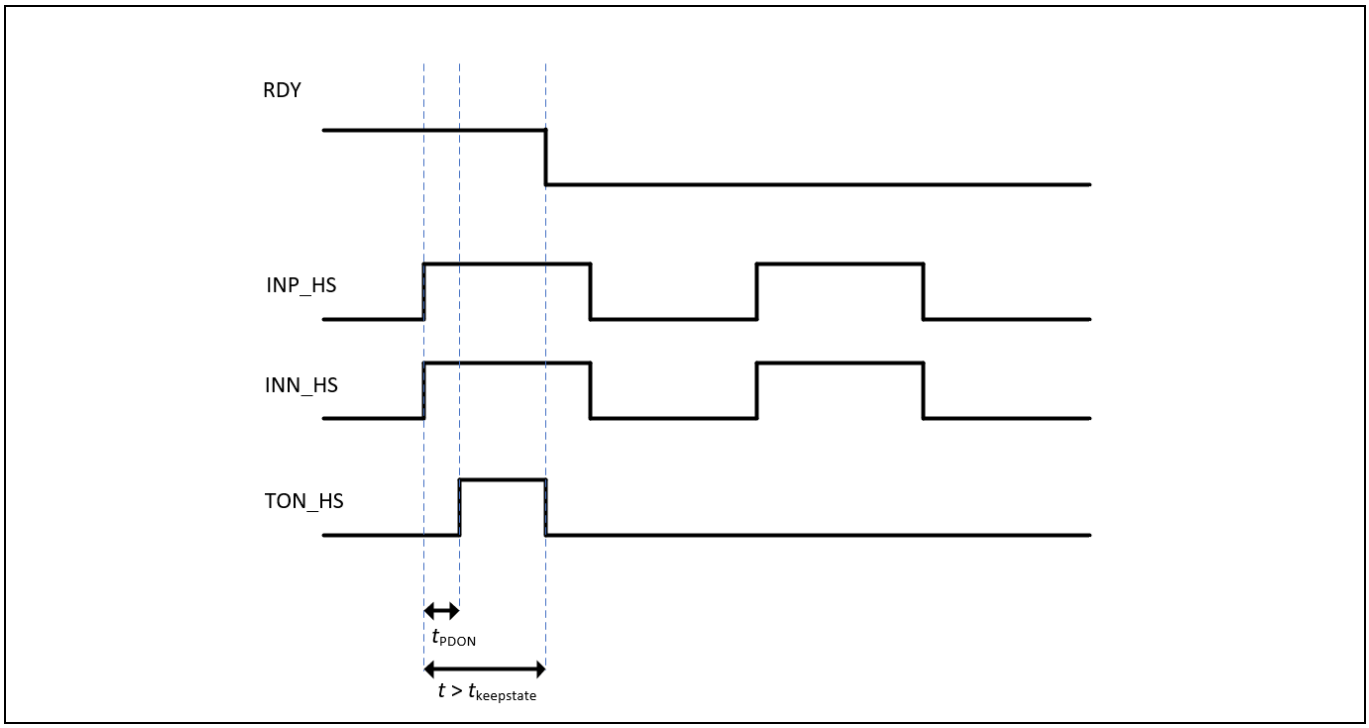


Figure 69 Case 1: INP_HS rising edge is sensed before INN_HS rising edge and $t > t_{keepstate}$

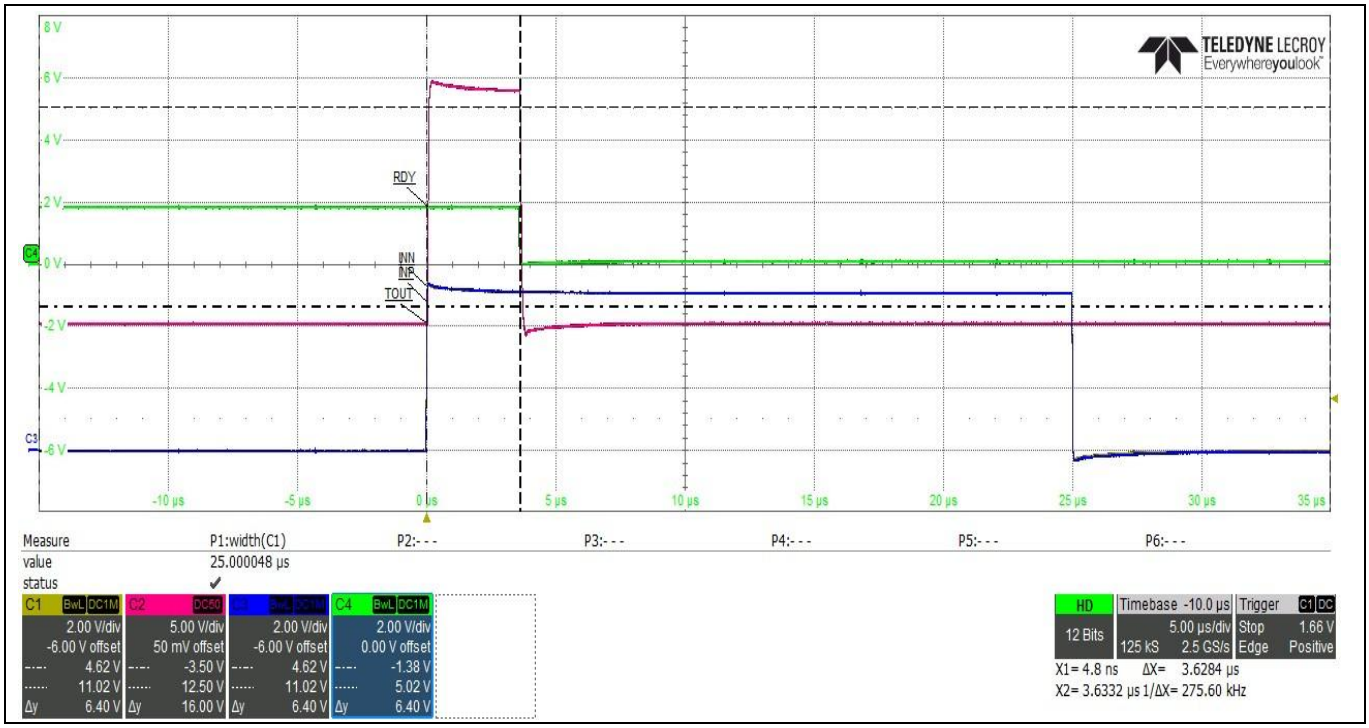


Figure 70 Case 1: output pulse for duration $t_{keepstate}$ seen when INP turns ON 1.3 ns before INN

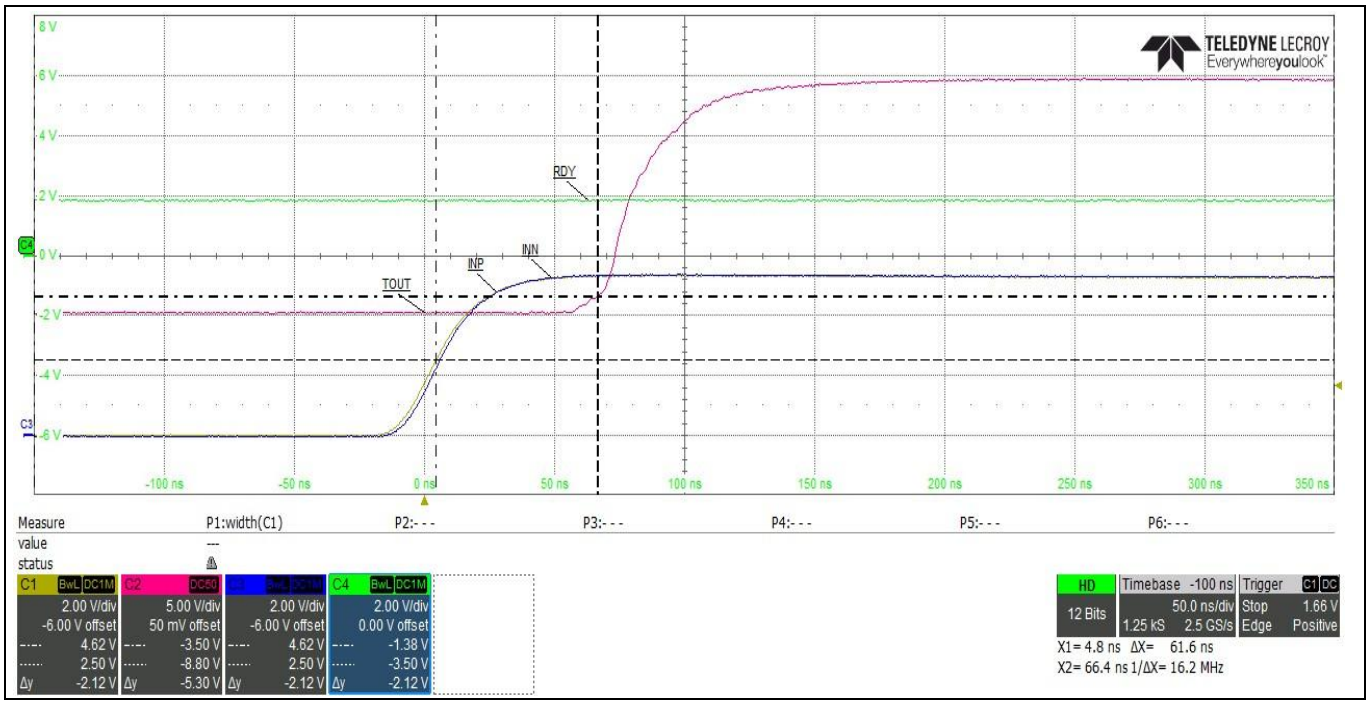


Figure 71 Case 1: t_{PDON} and output pulse seen when INP turns ON 1.3 ns before INN

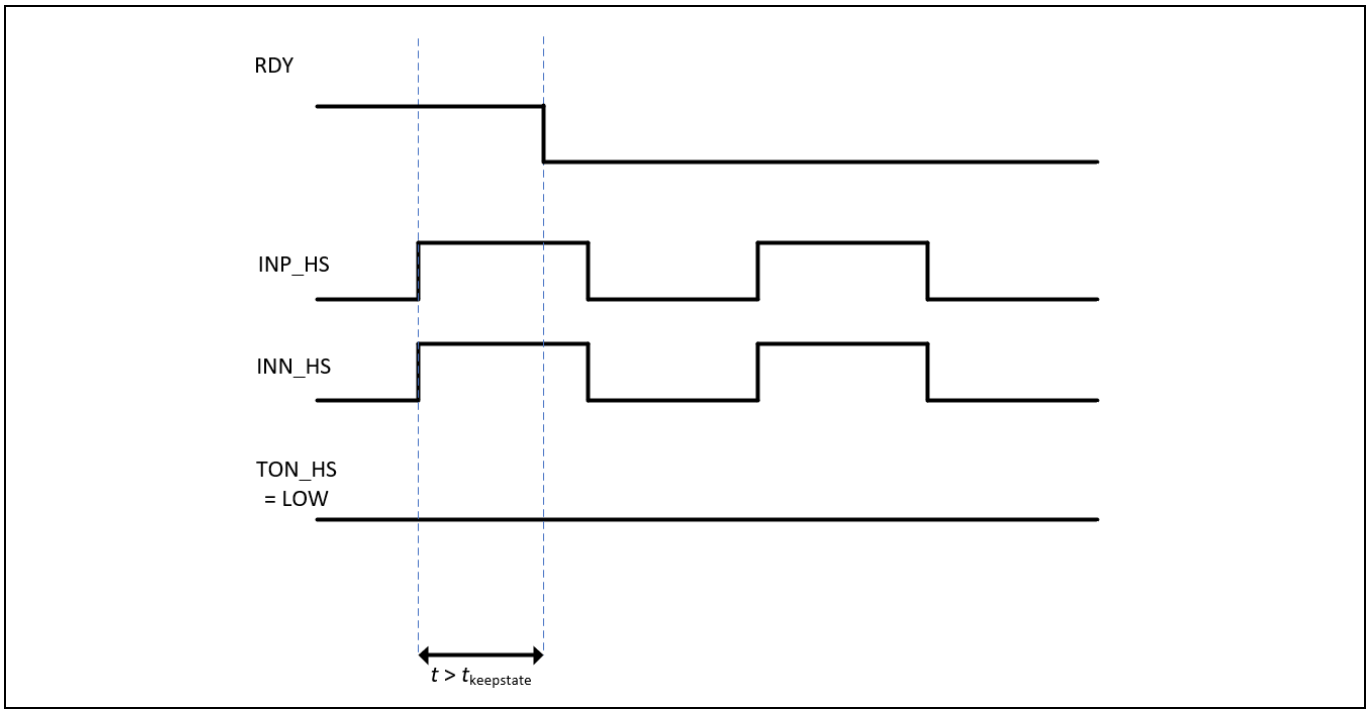


Figure 72 Case 2: INN_HS rising edge is sensed before INP_HS rising edge and $t > t_{keepstate}$

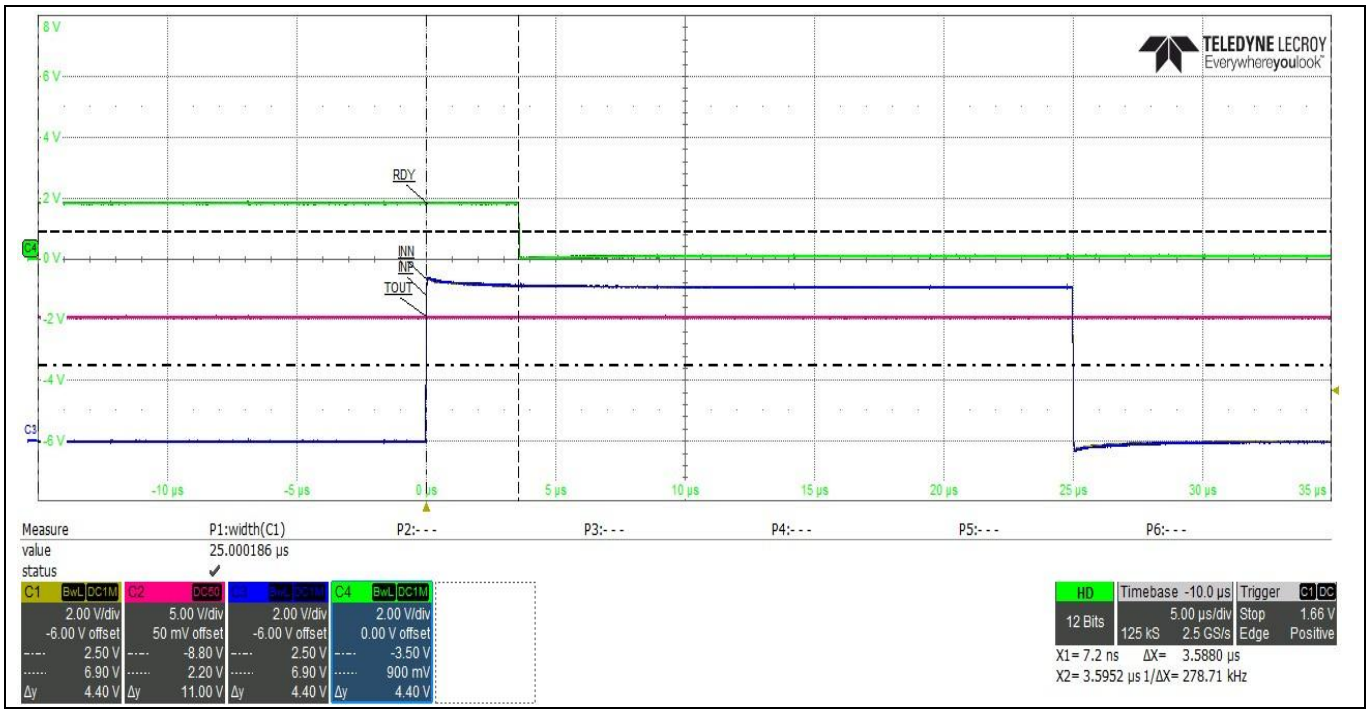


Figure 73 Case 2: no output pulse seen when INN turns ON 1.3 ns before INP

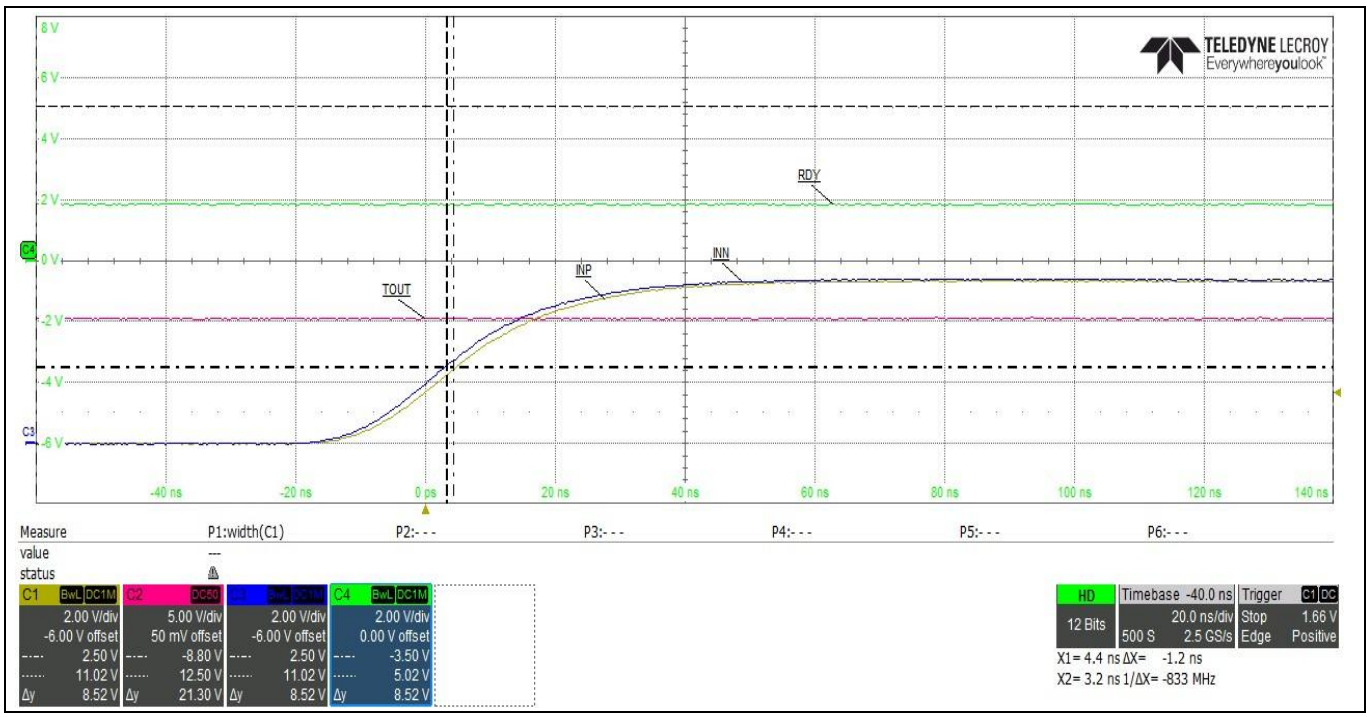


Figure 74 Case 2: no output pulse seen when INN turns ON 1.3 ns before INP

3.11 Active Miller clamping

The EiceDRIVER™ gate driver family is equipped with an active Miller clamping feature. The active Miller clamping provides a low ohmic path to the power transistor gate once the gate driver is turned off. When a switching transition happens in the half-bridge the active Miller clamp sinks the current that is injected into the gate by the Miller capacitor and prevents an unintended turn-on, see Figure 75. There are two different variants of active Miller clamping available, depending on which product variant is chosen from Table 1. Both variants are explained hereafter.

3.11.1 Internal active Miller clamp

This feature is available on the product variants 1EDI3025AS, 1EDI3026AS, 1EDI3035AS and 1EDI3038AS. The internal active Miller clamp is released upon a turn-on request and reactivated after the voltage on the **GATE/CLAMP** pin sinks below the threshold V_{CLAMPx}. Note that the threshold is different between the IGBT and SiC gate driver variant. For the SiC gate driver variants it is referenced to GND2, which leads to an earlier activation. For the IGBT variants it is referenced to VEE2.

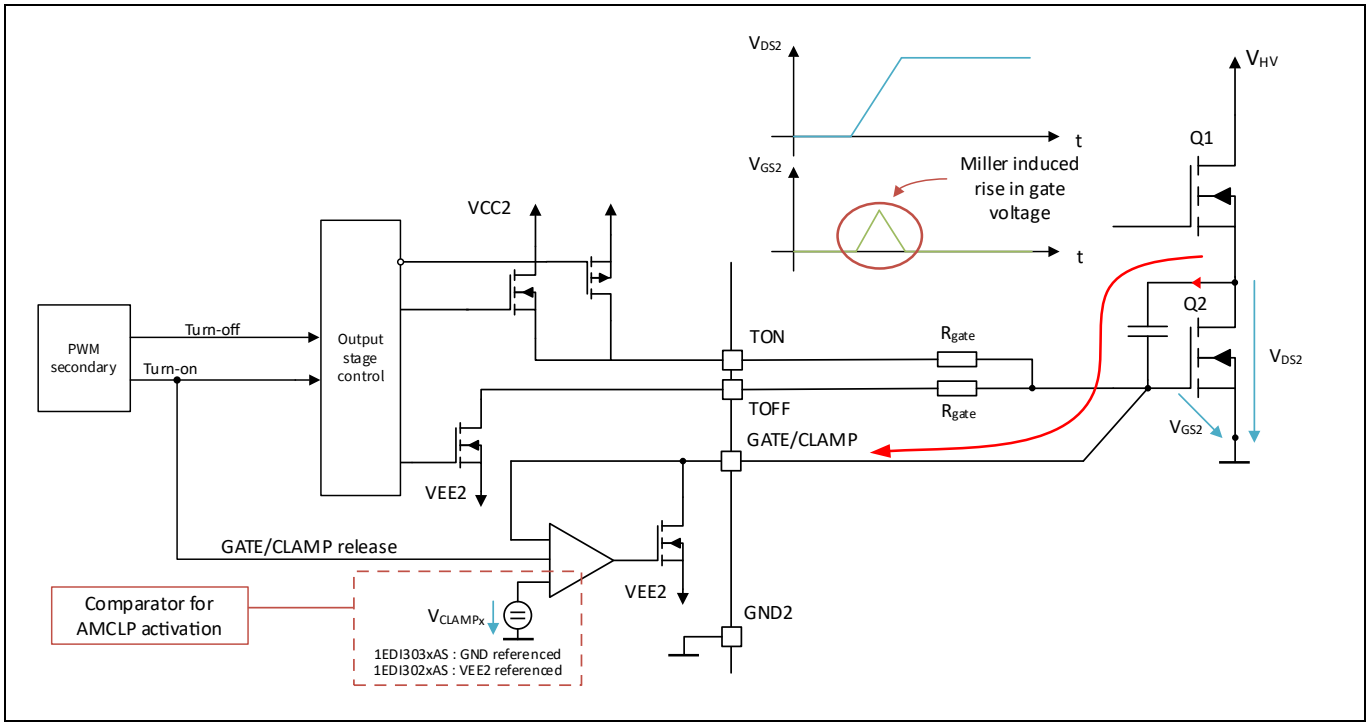


Figure 75 Block diagram of internal active Miller clamping

The GATE/CLAMP connection to the power transistor gate should be as short as possible to reduce the effective series inductance in the path.

3.11.1.1 Loop inductance and compensation

During the gate driver turn-off transition through TOFF the AMCLP output is low. The transient turn-off current flows through the output stage transistor and exits the gate driver through the VEE2 pin to return back to the VEE2 voltage source.

The package pins are connected to the die through a bond-wire. Together with the PCB trace, the pin and the bond-wire an inductance L_{AMCLP} is formed. The equivalent circuit is shown in Figure 76. Through this inductance a coupling between the AMCLP circuit and the TOFF loop occurs, since the AMCLP is referenced to the internal VEE2 available on the die. The coupled voltage is of positive polarity vs. the VEE2 voltage rail and therefore increases the voltage on the external AMLCP transistor.

This chapter derives the required equations and shows how to use them for dimensioning the AMCLP circuit components in the application in order to prevent a parasitic turn-on event on the AMCLP transistor.

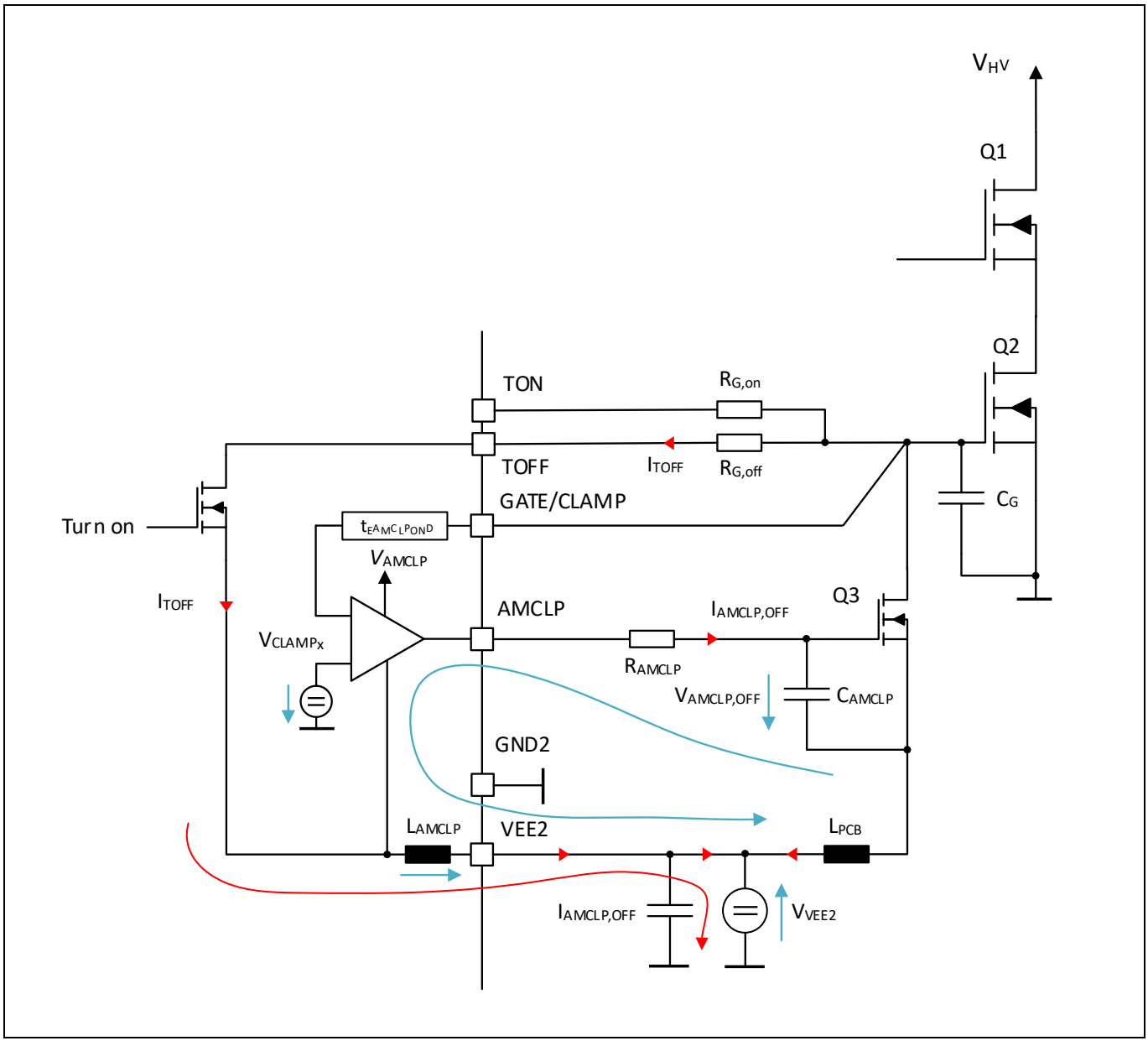


Figure 76 AMCLP in off state together with induced voltage from the gate loop

The discharge current of the transistor Q2 through the TOFF pin can be modeled as an RLC series resonant circuit with the following parameters

$$\delta = \frac{R_{Goff}}{2 \cdot L_{AMCLP}}, \omega_0 = \frac{1}{\sqrt{L_{AMCLP} \cdot C_G}}, \kappa = \sqrt{\delta^2 - {\omega_0}^2}, \tau = R_{AMCLP} \cdot C_{AMCLP} \quad (3\text{-}36)$$

. In physical terms the resonant circuit is usually overdamped, since

$$\delta \gg \omega_0 \quad (3\text{-}37)$$

holds true. It is imperative to ensure this condition in the application where a resonance in the switching loop is anyhow not desired.

The current through the inductance L_{AMCLP} during TOFF activation can then be determined as

$$I_{TOFF}(t) = \frac{V_{VCC2} + V_{VEE2}}{L_{AMCLP} \cdot \kappa} e^{-\delta \cdot t} \sinh(\kappa \cdot t) \quad (3\text{-}38)$$

. In the next step it is assumed that the AMCLP circuit is not significantly loading the gate loop, which is justified since typically the effective gate capacitance C_G is magnitudes larger than C_{AMCLP} and the result will represent a “worst-case” approximation.

The resulting voltage on the AMCLP capacitor can be determined as the rather undhandy expression of

$$\begin{aligned} V_{AMCLP,OFF}(t) = {} & V_{VCC2} + V_{VEE2} \\ & \cdot \left\{ \frac{(-\delta - \kappa)}{2\kappa(\delta \cdot \tau + \kappa \cdot \tau - 1)} \cdot e^{-t(\delta+\kappa)} + \frac{(\kappa - \delta)}{2\kappa(-\delta \cdot \tau + \kappa \cdot \tau + 1)} \cdot e^{-t(\delta-\kappa)} \right. \\ & \left. - \frac{1}{(\delta \cdot \tau + \kappa \cdot \tau - 1)(\delta \cdot \tau - \kappa \cdot \tau - 1)} \cdot e^{-\frac{t}{\tau}} \right\} \end{aligned} \quad (3\text{-}39)$$

, where it is introduced that

$$\tau = R_{AMCLP} \cdot C_{AMCLP} \quad (3\text{-}40)$$

. Unfortunately, it is not possible to find a closed solution for the global extremum of this function.

The function can be plotted to show the dependencies of the time constant τ.

The following parameters are assumed in the example:

- C_g = 47nF
- R_g = 4Ω
- L_{AMCLP} = 1.5nH
- V_{VCC2} = 18V, V_{VEE2} = -3V

The results are plotted in Figure 77 and Figure 78 respectively. Note that the minimum gate threshold voltage of the typical MOSFETS applied on the AMCLP pin is around 1V to 1.5V, while the input capacitance is usually far below 1nF. Looking at Figure 78 and considering a 20% margin a reasonable time constant is 6ns. This time constant can be achieved with

- R_{AMCLP} = 4.7 Ω
- C_{amclp} = 1.3 nF

which implies that an additional discrete capacitance must be added to the external AMCLP MOSFET.

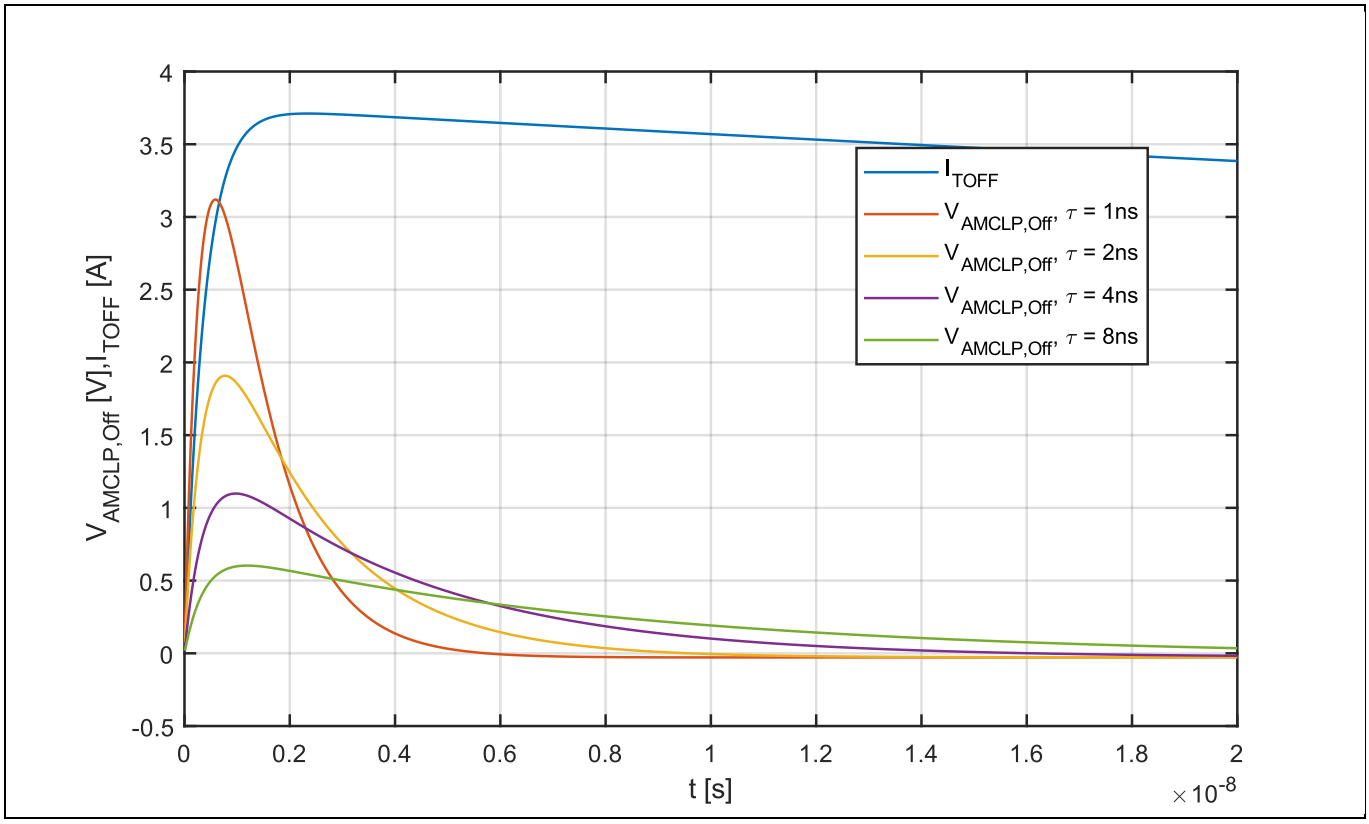


Figure 77 Plot of current and resulting AMCLP voltage for different time constants

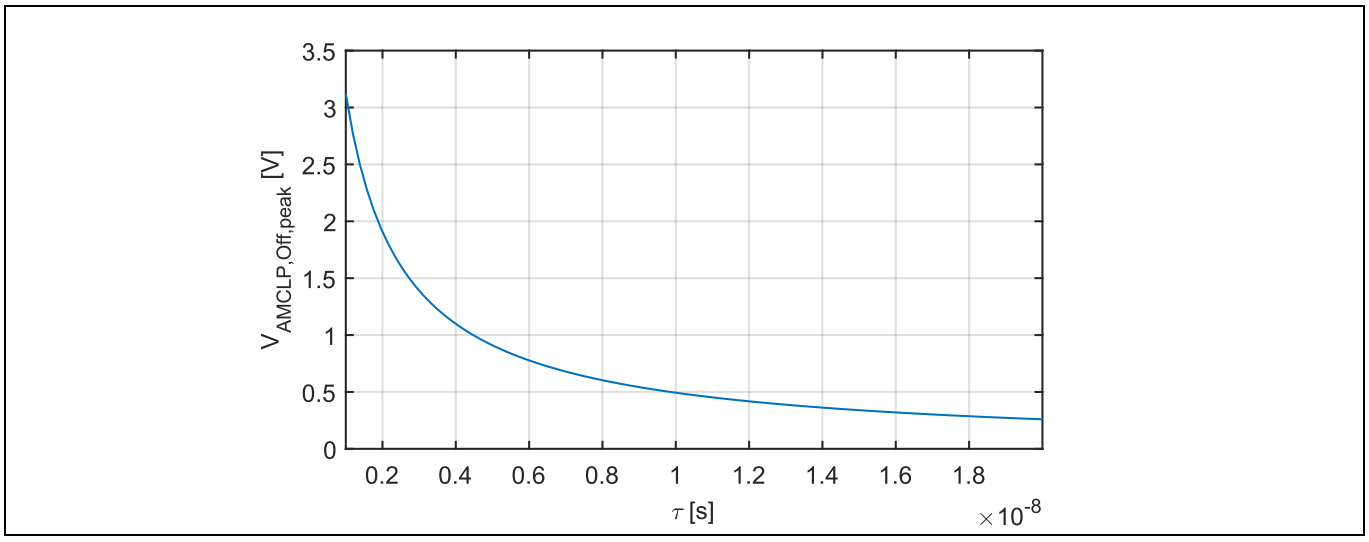


Figure 78 AMCLP voltage peak versus time constant

3.11.1.2 Connecting the AMCLP transistor to VEE2

As shown in chapter 3.11.1.1 the loop inductance of the AMCLP circuit plays an important role in the overall AMCLP performance. The inductance can be split into an internal contributor of L_{AMCLP} and an external contributor L_{PCB} as shown in Figure 76. While the internal inductance is just given and can only be compensated by an external capacitor on the AMCLP transistor, the external inductance is governed by the PCB layout. In the layout it must be prevented that L_{PCB} is excited by the VEE2 return current, since this would add further voltage to the AMCLP gate on TOFF activation.

Therefore the following approach is recommended:

- Connect the AMCLP transistor VEE2 through a Kelvin connection to VEE2
- Ideally connect directly to both gate driver corner pins

This guideline is implemented on the evaluation board. The layout examples are shown in Figure 79 and Figure 80 respectively. An inproper connection may require higher external compensation capacitance on the transistor.

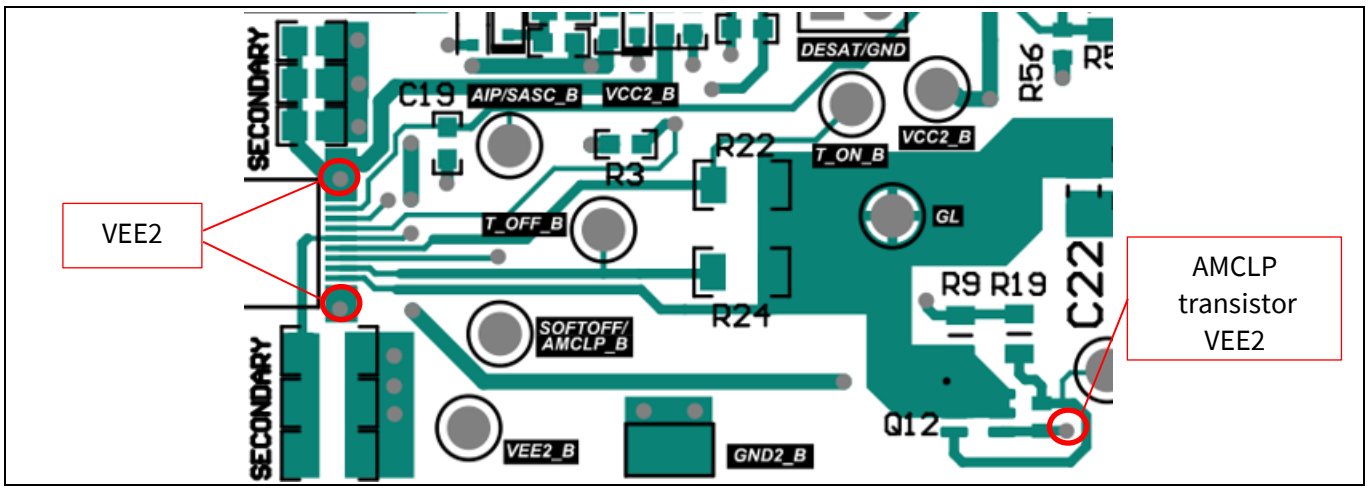


Figure 79 Evaluation board AMCLP connection – TOP layer

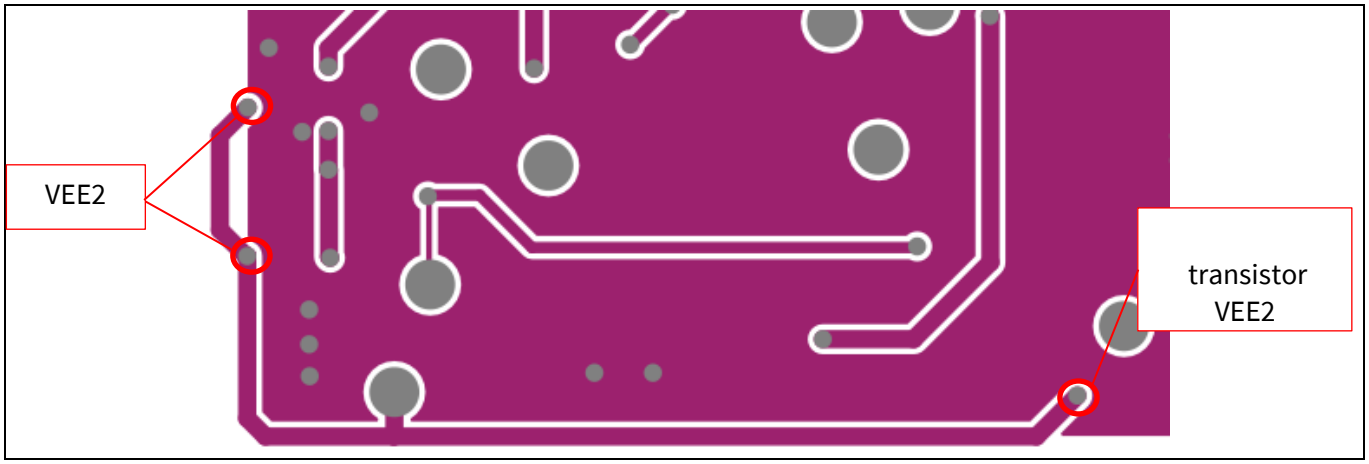


Figure 80 Evaluation board AMCLP connection – BOTTOM layer

3.11.2 Passive gate clamp

When the gate driver is unpowered the passive gate clamp structure inside the GATE/CLAMP can sink current and pull-down the gate to VEE2. The detailed electrical characteristic is given in the datasheet. The characteristic of the passive gate clamp for a single device is shown in Figure 81.

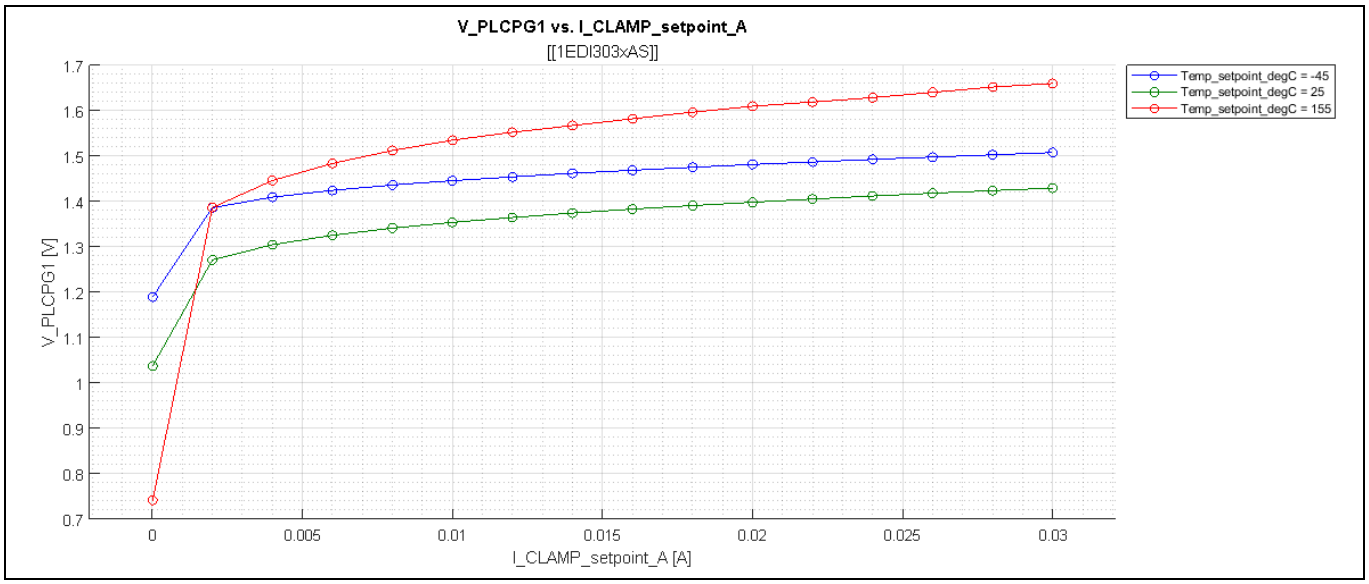


Figure 81 Voltage rise above VEE2 versus injected clamp current

3.12 Short circuit clamping

During a short circuit event modern IGBT technologies may experience charge injection back into the gate. This charge causes the gate voltage to rise. The EiceDRIVER™ gate driver family implements a novel short circuit clamping feature to remove the need for an external clamping diode. Characteristics are given in the datasheet.

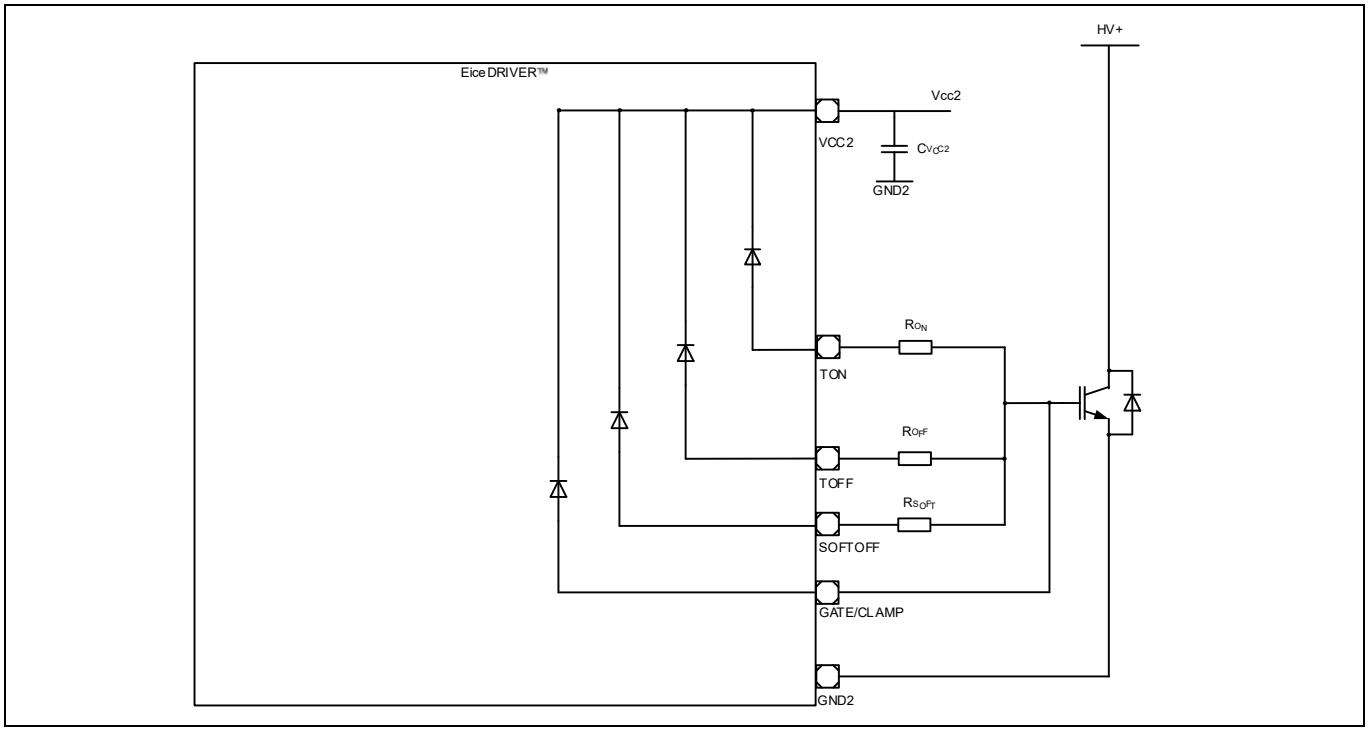


Figure 82 Short circuit clamping on 1EDI3025AS, 1EDI3026AS, 1EDI3028AS, 1EDI3035AS and 1EDI3038AS

4 Implementing system level advanced diagnostics

Due to the advanced feature set and the implemented DATA interface the EiceDRIVER™ gate driver allows to perform beneficial diagnostics after power-up to reduce the number of latent faults. One substantial contributor is the DESAT/OCP built-in selftest that is executed everytime UVLO2 is cleared, for mor details see chapter 3.6.

Additional diagnostic opportunities arise from the shoot through protection feature. This feature is also active in PWM_Disable mode.

4.1 Primary PWM switching path health check

The entire PWM path on the primary can be checked for stuck or shorted pins by following the procedure shown in Figure 83. SI1 and SI2 are low during this check to ensure that the gate driver remains in PWM_Disable mode and that the output stage remains inactive.

- Force a dead time warning on the low side gate driver
- Observe the “dead time warning bit” to be set once and then cleared on the low side DATA interface
- Force a dead time warning on the high side gate driver
- Observe the “dead time warning bit” to be set once and then cleared on the high side DATA interface

If the outcome of this procedure is positive, then any failures on the pins in the path can be excluded, such as:

- Short to VCC1 or GND1
- Short to neighbor
- Pin open

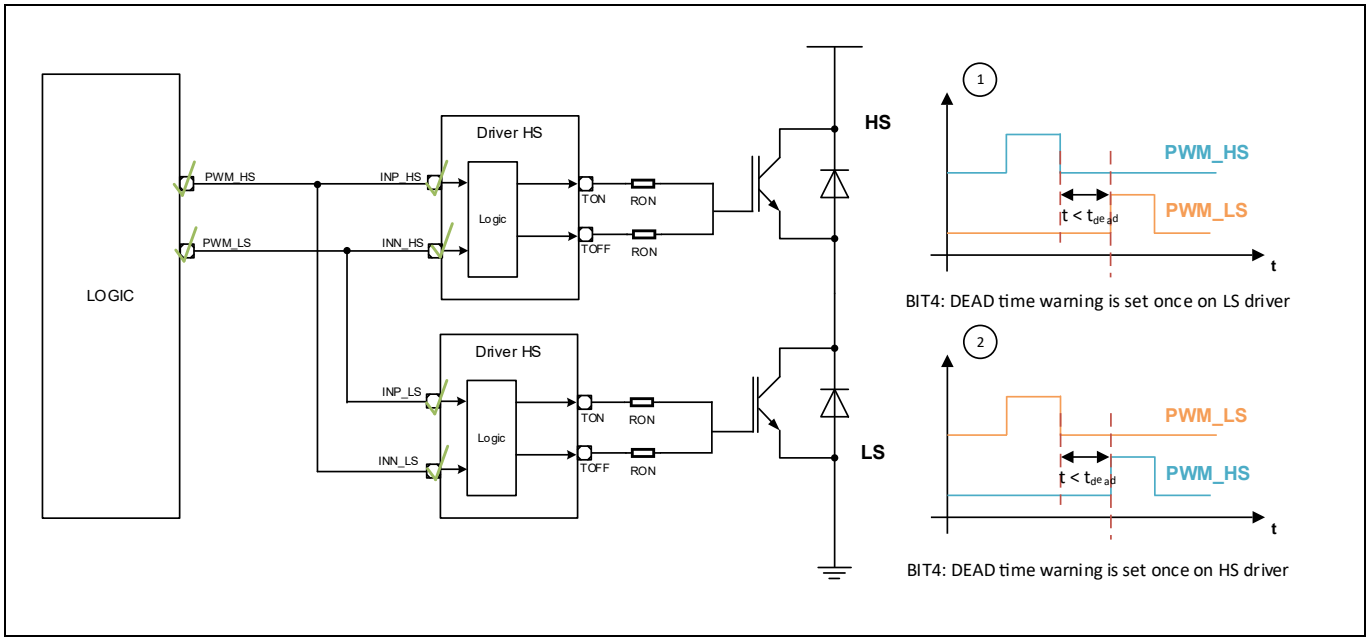


Figure 83 Procedure for checking all PWM pin connections

4.2 Secondary side switching path health check

The output stage can also be activated through the AIP/SASC pin. More details about this functionality are given in 3.9.2. After power-up the SASC functionality can be checked by turning on one power switch one at a time. Once the SASC is activated, the “SASC activation warning” bit will be set in the DATA interface and can be read from the primary. A potential connection issue to the power transistor gate will result in raising an “output stage monitoring error” or a “gate monitoring error”.

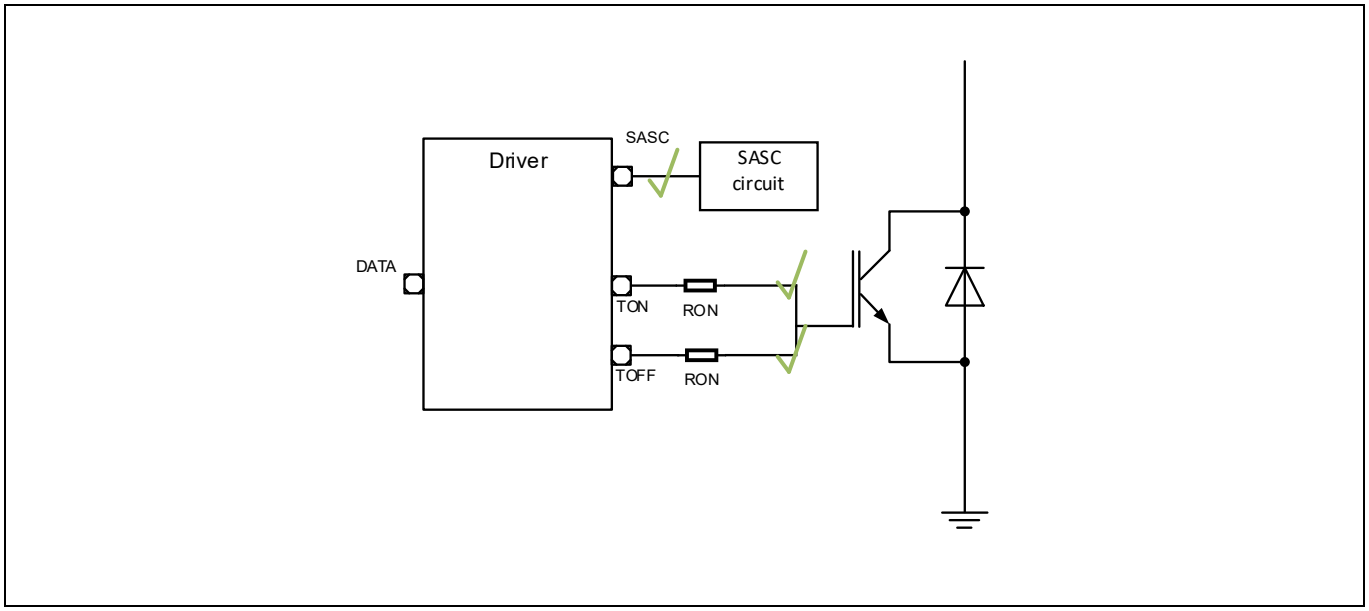


Figure 84 Checking the SASC functionality

Likewise, the primary side safety interface can be used to conduct an identical check by transitioning in ASCP_ON mode.

5 Layout optimization

Based on the application information in the datasheet, a minimum number of components is recommended in order to enable all driver features. An exemplary schematic for the 1EDI3035AS and layout is shown in Figure 85 and Figure 86 respectively.

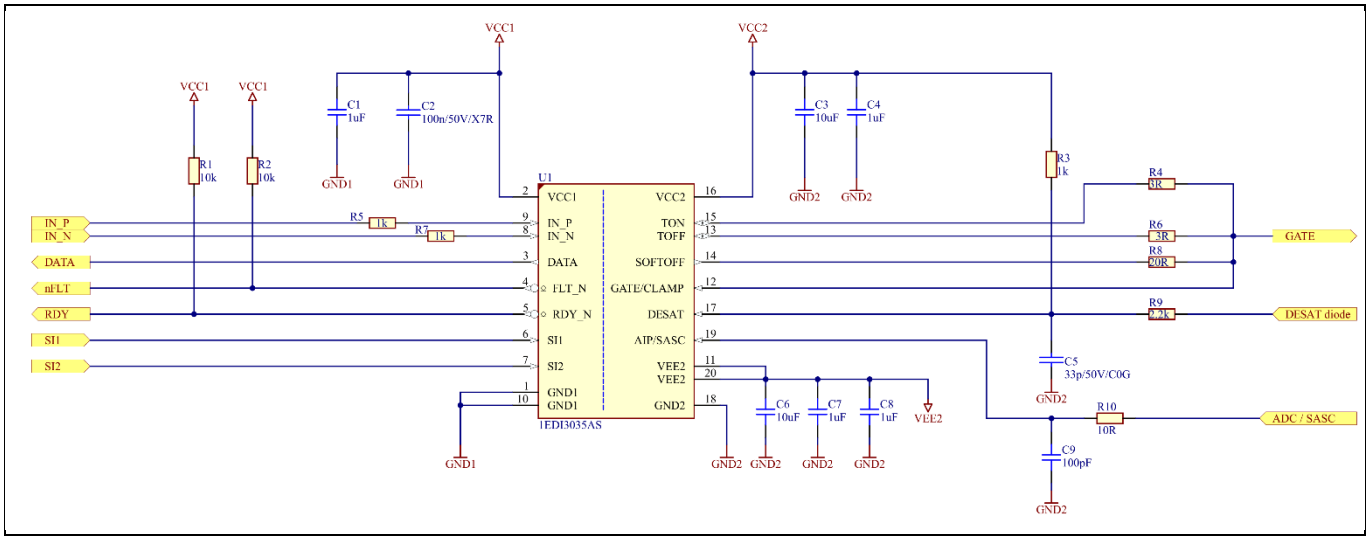


Figure 85 Driver schematic including local components

When layouting the driver schematic the following design rules help to maximize system performance:

- Place the decoupling capacitors C1, C2, C3, C4, C6, C7 and C8 as close to the respective supply pins as possible
- Connect the supply pins directly with a via to the power plane first, see Figure 86
- Place additional vias at the decoupling capacitors to reduce the series inductance further
- On the secondary side there are two VEE2 pins. Decoupling on VEE2 can be further improved by splitting the capacitors between both pins. If splitting is not possible, the capacitors should be placed near to pin 11, since pin 11 is internally connected with a lower impedance to the chip than pin 20
- The DESAT filter capacitance C5 and filter resistor R9 should be placed close to the DESAT pin to prevent noise pick-up
- The GATE loop, consisting of R6, R4 and R8 should be optimized for a low loop inductance. This can be achived by keeping the distance of the driver to the power device low and by maintaining and providing an uninterrupted return path for the GATE currents through the GND2 plane
- The GATE/CLAMP pin should be connected by the shortest possible distance to the power device GATE or external clamping transistor to provide a low-inductance clamping path. In the example layout this achieved by routing pin 12 on another layer to the GATE – see Figure 87

For some supply concepts the supply lines have to be routed below the gate driver. Due to the high dV/dt that naturally occurs in SiC applications between the driver and the supply lines, noise can be picked up by the gate driver through the back metallization of the internal lead-frame. To improve noise immunity of the gate driver it is recommended to extend the internal GND1 and GND2 planes slightly below the gate driver, which is also shown in Figure 86. This allows noise to be shielded from the gate driver.

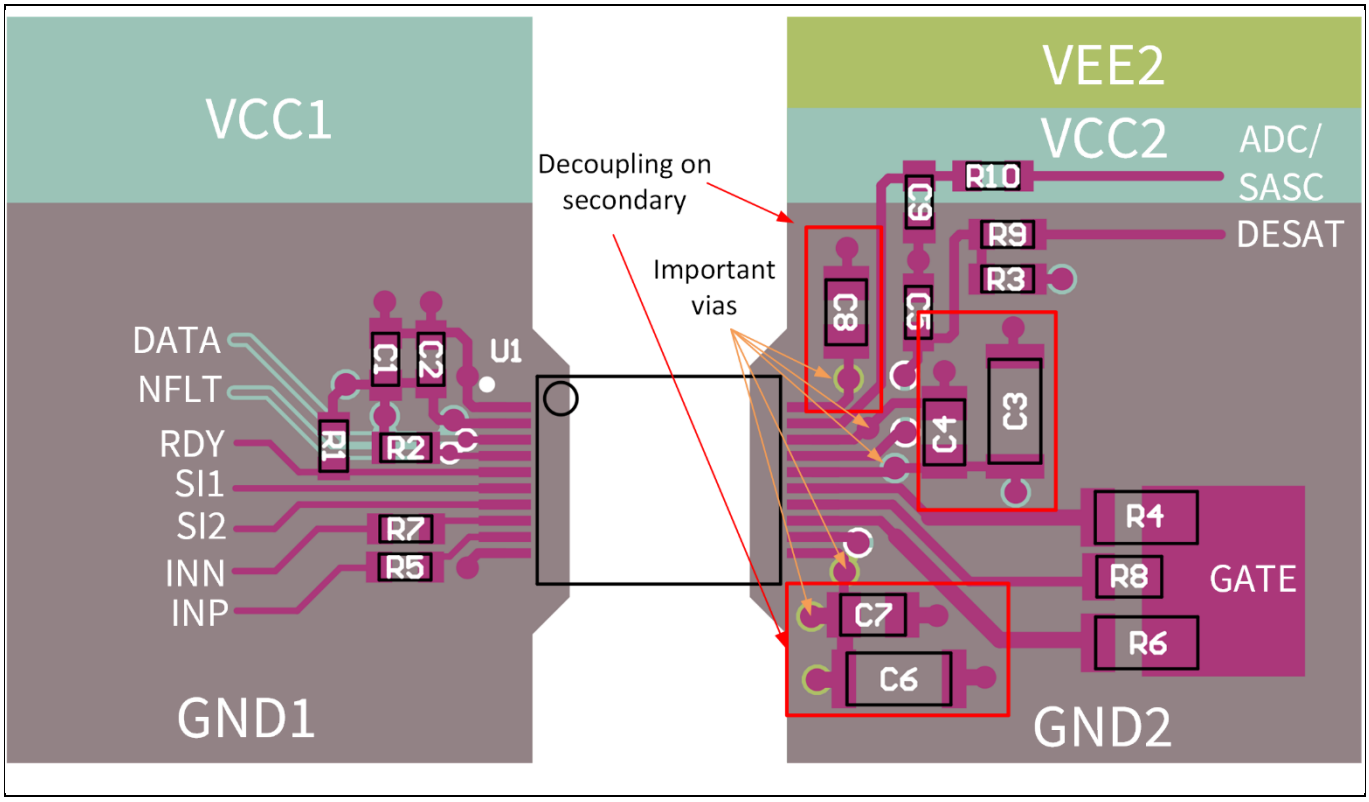


Figure 86 Layout example with external components and noise improvement

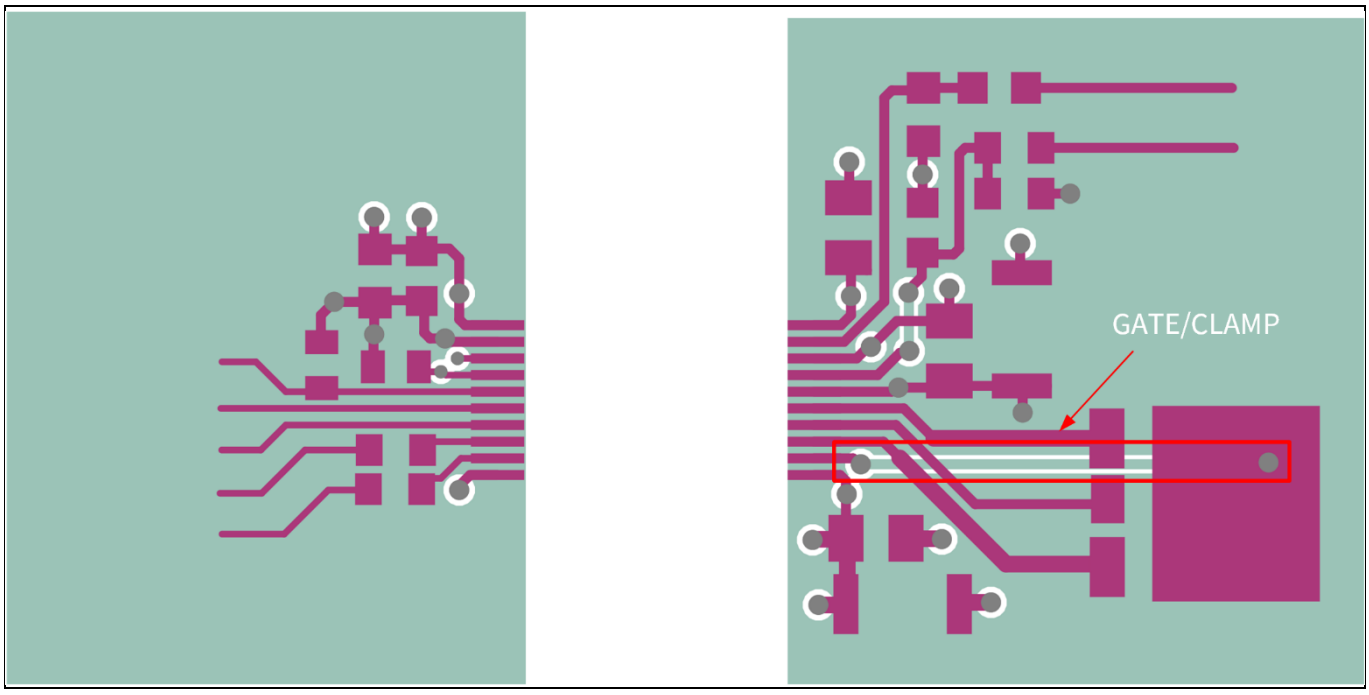


Figure 87 Top and inner layer showing GATE/CLAMP or AMCLP routing

6 Revision history

Document version	Date of release	Description of changes
1.0	2023-09-27	Initial release
1.1	2024-01-08	Chapter 3.4.1 • Formula (3-6) corrected Chapter 3.4.2 “Advanced DESAT circuit for arbitarty threshold adjustement” added Chapter 3.5 “DESAT and SOFTOFF performance measurement” added Chapter 3.11.2 “External active Miller clamp” revised Chapter 3.8.2 “Frequency characteristic” added Chapter 3.8.2 “Conversion and error calculation” revised Chapter 3.8.4 “End of line calibration” added Chapter 3.8.5 “Temperature sensing” added Chapter 3.8.6.2 “Measurement error calculation example” added
1.2	2024-02-21	Formula (3-14) corrected Chapter 2.3.6 “Transient thermal behavior” added Chapter 3.5.3 “Influence of varying VCC2” added
1.3	2024-03-12	Chapter 3.11.2.1 “Loop inductance and compensation” added Chapter 3.11.2.2 “Connecting the AMCLP transistor to VEE2” added
1.4	2024-07-25	Removed 1EDI3036AS variant from all chapters
1.5	2024-12-20	Chapter 3.4.2 “Advanced DESAT circuit for arbitrary threshold adjustment” expanded with sub chapters an detailed calculations
1.6	2026-08-05	Chapter 3.4.1 Linking issue resolved

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