Hardware design guidelines for AIROC™ CYW55310 Bluetooth® & Bluetooth® LE device WLBGA package

About this document

Scope and purpose

This document provides PCB layout guidelines for board designs using the AIROC™ CYW55310 Bluetooth® & Bluetooth® Low Energy chip in flip chip ball grid array (WLBGA) package, based on the reference schematics and layout files [1].

Intended audience

This document is intended for hardware engineers creating PCB layout designs with AIROC™ CYW55310 Bluetooth® & Bluetooth® LE-WLBGA chipset.

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1 Introduction

This document provides examples, guidelines, and requirements to help board designers to:

- Enable optimal board routing and chip performance
- Address noise coupling, electromagnetic interference (EMI), current-flow capability, and power management unit (PMU) performance
- Identify the comparative differences of various components (footprint and rating trade-offs) and the impact on the overall PMU functionality and performance

1.1 Acronyms and abbreviations

In most cases, acronyms and abbreviations are defined on first use. For a comprehensive list of acronyms and other terms, see the Glossary.

1.2 IoT resources

The wealth of data available here will help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. You can access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. You can acquire technical documentation and software from the Infineon Developer Community.

1.3 Device description

This section contains a subset of information about the AIROC™ CYW55310 Bluetooth® chip. For more information, see the AIROC™ CYW55310 device datasheet [2].

The AIROC™ CYW55310 is a single chip Bluetooth®, Low Energy qualified against Bluetooth® Core 6.1-compliant, supporting basic rate, enhanced data rate (EDR), Bluetooth® Low Energy 2 Mbps, Bluetooth® Low Energy 1 Mbps, long-range (LR), and Low Energy Coded PHY with advertising coding selection. It provides a small form-factor solution with minimal external components to drive down cost and allows for platform design flexibility in size, form, and function.

Figure 1 shows the AIROC™ CYW55310 device architecture block diagram with a simplified view of interconnection between subsystems and blocks.

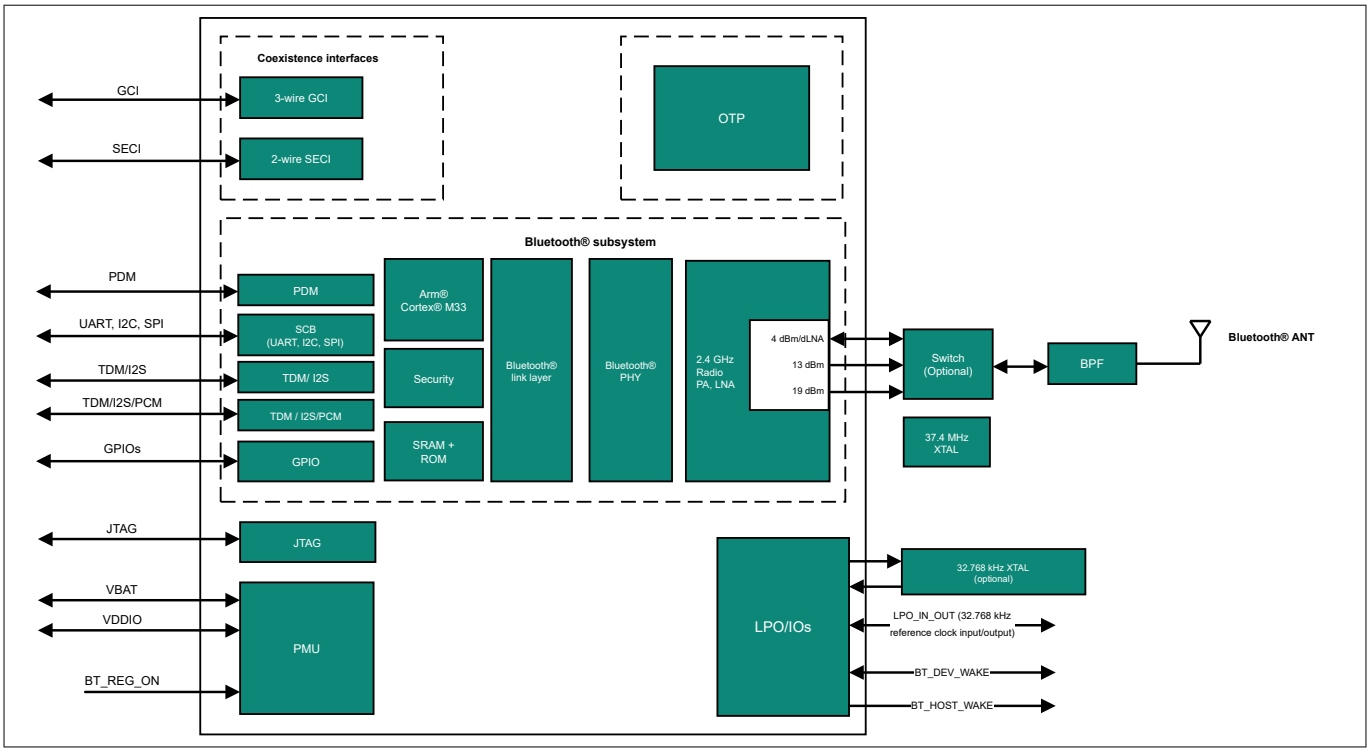

Figure 1 Functional block diagram

1.4 AIROC™ CYW55310 device WLBGA package ball map

Figure 2 shows the AIROC™ CYW55310 device WLBGA package ball map.

	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
10	RSVD	RF_GND	RF_GND	RF_VDD_1P12	RF_GND	NC7	RFSW_CTRL7	VDDIO_RFSW	GPIO_0	GPIO_4	VDDOUT_RF3P3	BTLDO_VDDBAT	BTLDO_VDDBAT	ASR_VDDBAT	ASR_VLX	10
9	RSVD	RF_GND	BTRF_GPAIO				RFSW_CTRL6	VSSC	GPIO_2	GPIO_6	PMU_VDD1P8	NC10	VDDOUT_BT3P3	VDDOUT_CLDO	PVSSA	9
8	RF_GND	NC11	RF_GND	RF_VDD_3P3	RF_GND	NC8	RFSW_CTRL5	VDDC	GPIO_3	GPIO_5	MIC_P	PMU_AVSS	BTREG_ON	ASR_VDD1P12	VSSC	8
7	RSVD	RF_GND	RF_GND	RF_VDD_3P3	RF_VDD_1P12	RFSW_CTRL4	LHL_XTALI	LHL_XTALO	BT_UART_RTS_N	BT_UART_TXD	VSSC	BT_GPIO_5	NC	NC	NC	7
6	RSVD	RF_GND	NC6	RF_GND	RF_VDD_1P12	RFSW_CTRL3	VDDC	LHL_GPIO_2	BT_UART_RXD	BT_UART_CTS_N	BT_GPIO_6	VDDIO	NC	NC	NC	6
5	BTRF_RF_OP	BTRF_VSS	BTRF_IF_VSS	RF_VDD_1P8	RF_GND	RFSW_CTRL2	LPO_IN_OUT	LHL_GPIO_3	AVDD_BBPLL	BT_GPIO_4	BT_GPIO_3	VDDC	SMIF_SPHB_DQ3	SMIF_SPHB_DQ2	SMIF_SPHB_CK	5
4	BTRF_VSS	BTRF_TEST	BTRF_PLL_VSS	BTRF_RX_DVSS	RFSW_CTRL1	RFSW_CTRL0	VSSC	LHL_GPIO_4	VSSC	BT_VDDO	BT_GPIO_2	TDM1_DI	SMIF_SPHB_CS0_N	SMIF_SPHB_DQ1	SMIF_SPHB_DQ0	4
3	BTRF_13DBM_OP	BTRF_VCO_VSS		BTRF_LDO_VDD_1P12		JTAG_SEL	BT_DEV_WAKE	LHL_GPIO_5	SMIF_SPHB_CS1_N	TDM1_DO	TDM1_SCK	TDM1_WS	BT_GPIO_17	BT_GPIO_16	BT_GPIO_7	3
2		BTRF_PA_VSS	BTRF_TX_VSS	BTRF_TX_DVSS	XTAL_GND	VDD_XTAL	VSSC	VDDC	LHL_GPIO_8	BT_HOST_WAKE	TDM1_MCK	TDM2_DI	VSSC	VDDC	TDM2_WS	2
1	BTRF_20DBM_OP	BTRF_PA_VSS	BTRF_PA_VDD_3P3	BTRF_TXIF_VSS	XTAL_XON	XTAL_XOP		LHL_GPIO_9	LHL_GPIO_6	BT_GPIO_0	DMIC_DQ	DMIC_CK	TDM2_DO	TDM2_MCK	TDM2_SCK	1
	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Figure 2 AIROC™ CYW55310 device WLBGA package ball map

1.5 Power topology

As shown in Figure 3, one buck regulator, multiple LDO regulators, and a PMU are integrated into the AIROC™ CYW55310 device. These blocks simplify power supply design for Bluetooth®. The AIROC™ CYW55310 device only requires two power supplies; VBAT and VDDIO to be provided with all additional voltages being generated by on-chip regulators.

1 Introduction

The control signal *BT_REG_ON* is used to power-up the regulators and take the section out of reset. The core buck regulator *ABUCK* powers up when *BT_REG_ON* is asserted. All regulators, buck, and LDO are powered down when *BT_REG_ON* is de-asserted.

The AIROC™ CYW55310 device allows for an extremely low power-consumption mode by completely shutting down the *ABUCK* regulator.

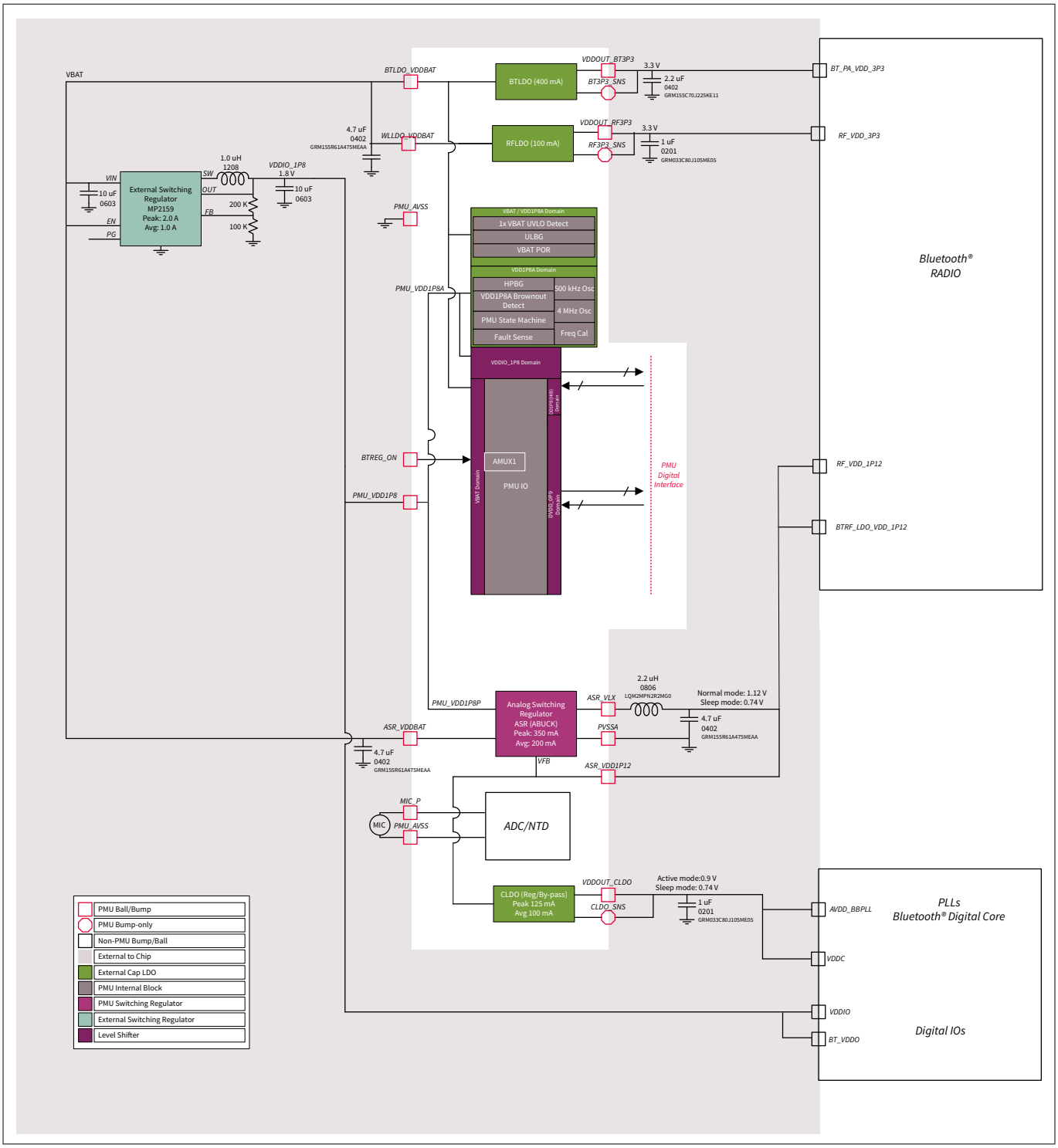

Figure 3 Typical power topology

2 Reference design board

2.1 Block diagram

***Note**: Contact Infineon support for the schematic and the Allegro layout file (*.brd). In this document, excerpts from the layout file are provided to show various areas of importance.*

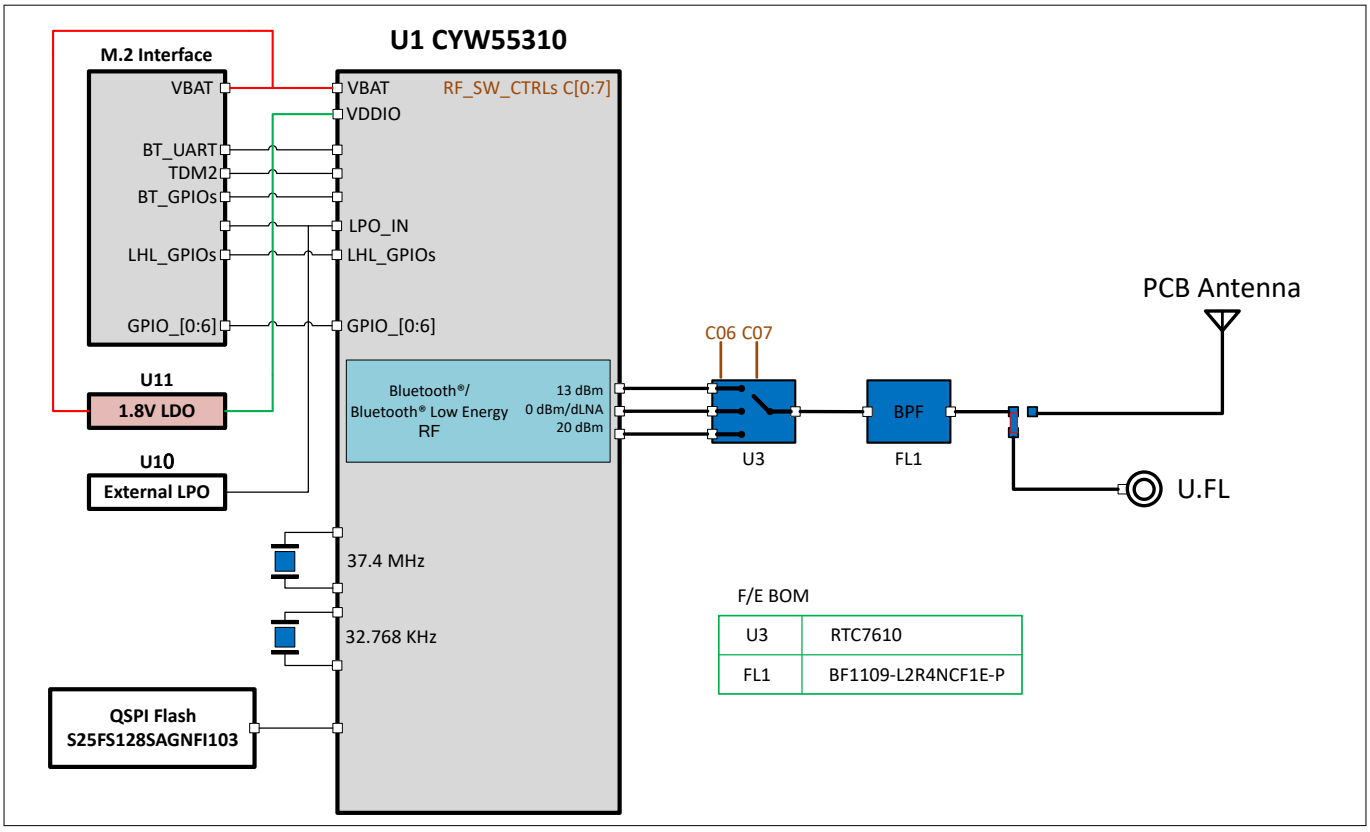

Figure 4 Functional block diagram

2.2 Major components in reference design

Table 1 Major reference design components

Reference design component designation	Description	Value
C2	ASR VDDBAT capacitor	4.7 µF
C5	BTLDO VDDBAT capacitor	4.7 µF
C1	BTLDO VDDBT capacitor	4.7 µF
C14	VDDOUT_BT3P3 capacitor	2.2 µF
C3	ABUCK capacitor	4.7 µF
L1	ABUCK inductor	2.2 µH

2.3 Board layers

***Note**: The figures in the following sections are from the reference design layout.*

Table 2 Board layers

Layer	Description
1	Component placement, RF signals, and wide power traces
2	Ground plane. Includes ground cut for RF traces and antenna connector
3	Power/signal plane. A few of the power rails are routed at this plane
4	Ground/signal plane. A few of the digital signal traces and some power rails are routed at this plane
5	Ground plane
6	Component placement, signals, and wide power traces

2.3.1 Layer 1 (component placement)

Regulators are sensitive to routing parasitics that can cause instability, power efficiency losses, and in extreme cases, loss of voltage regulation. Extreme parasitics due to long and thin traces can create large switching voltage spikes leading to long-term chip reliability problems.

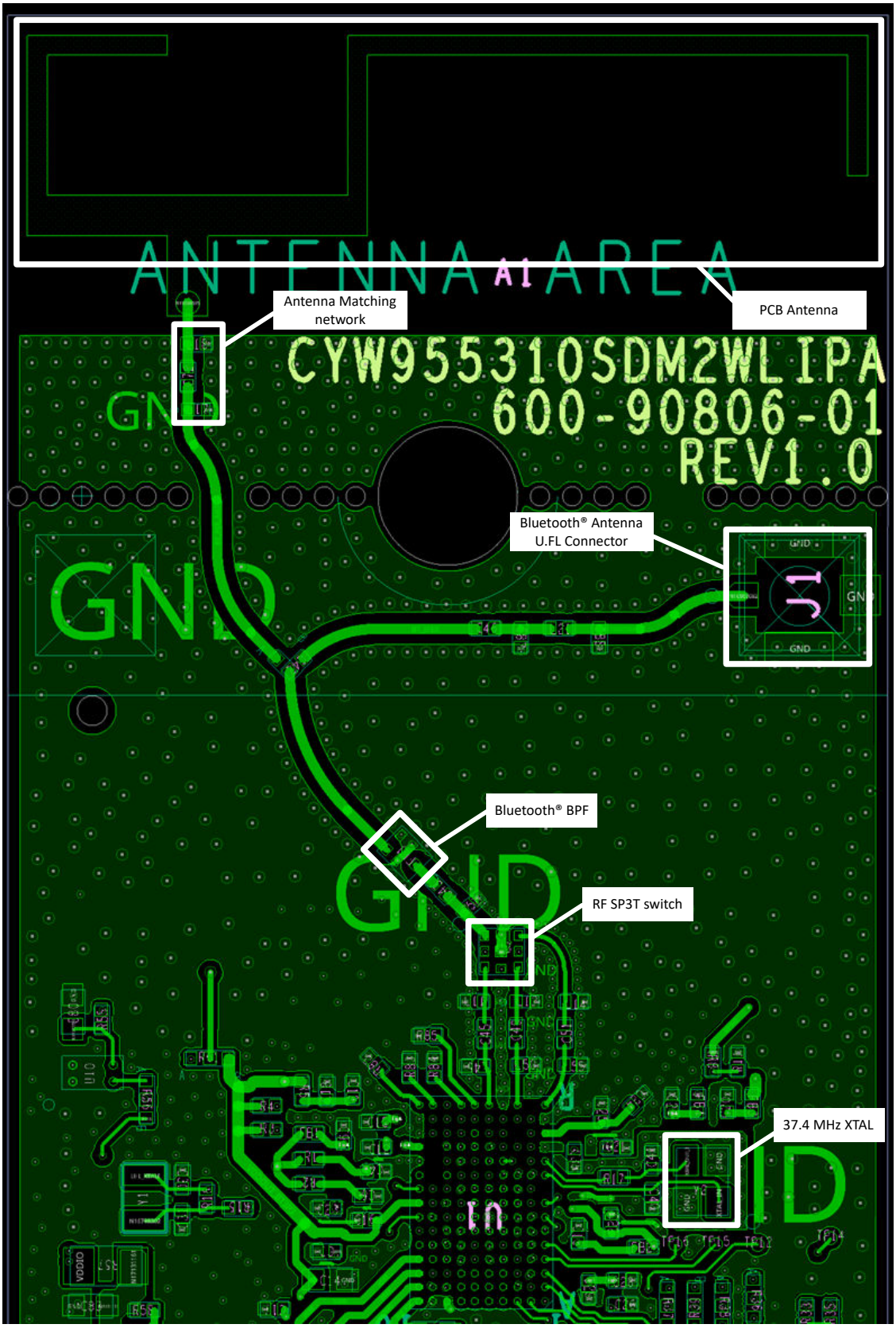

Figure 5 Reference design board layer 1 (component placement 1 of 2)

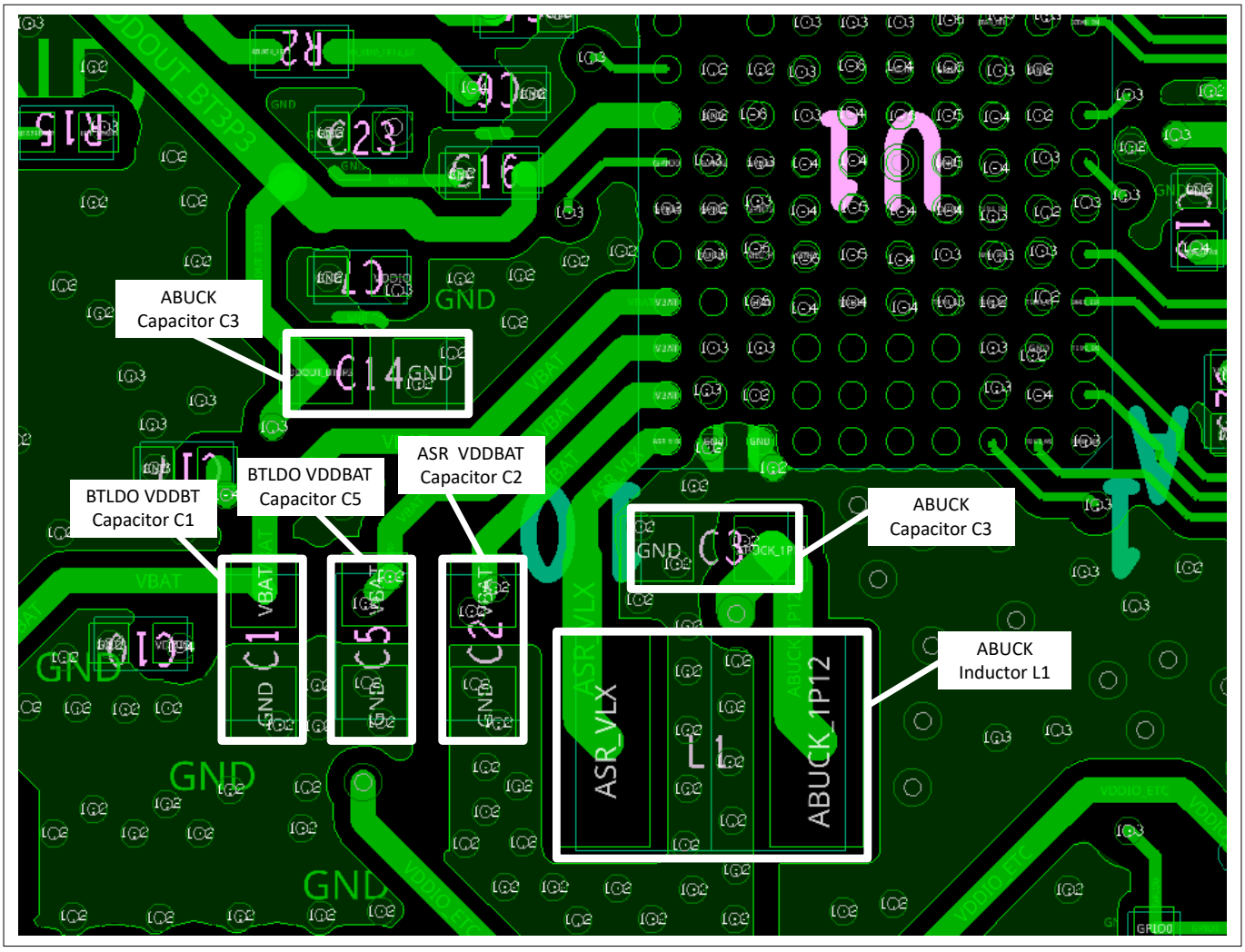

Figure 6 Reference design board layer 1 (component placement 2 of 2)

2.3.2 Layer 2 (ground plane)

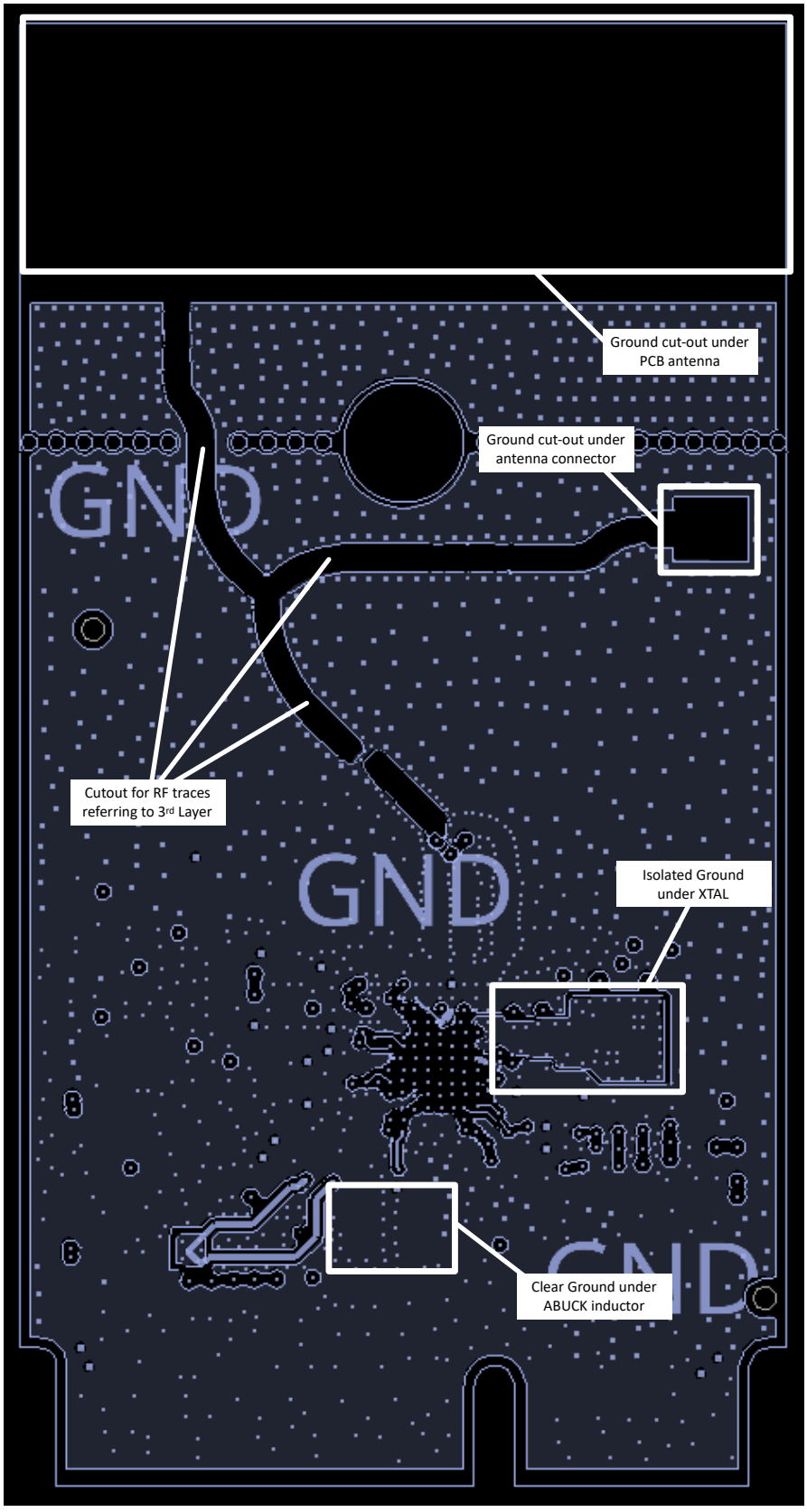

Figure 7 Reference design board layer 2 (ground plane)

2.3.3 Layer 3 (power/signal plane)

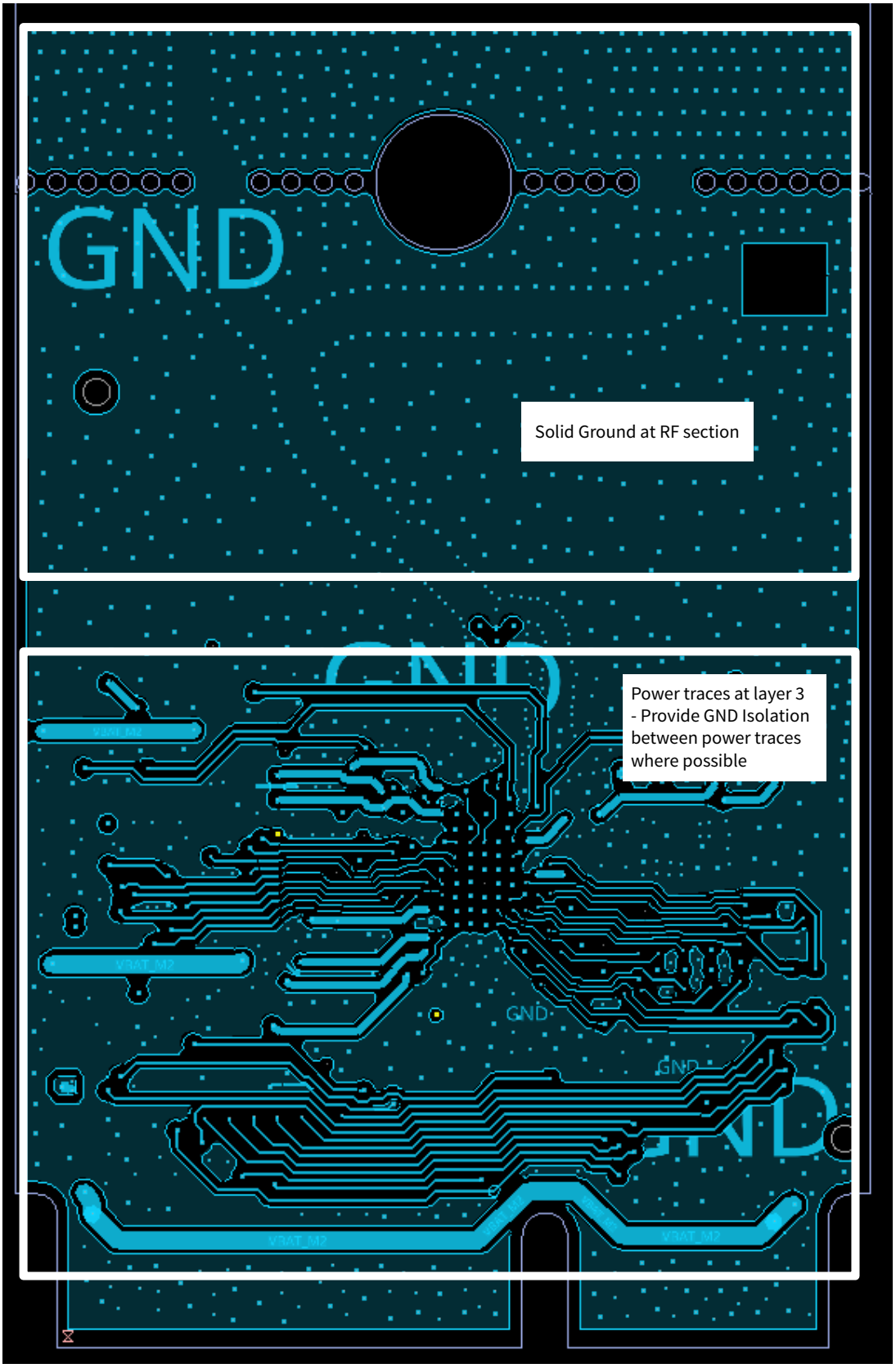

Figure 8 Reference design board layer 3

2.3.4 Layer 4 (ground/signal plane)



Figure 9 Reference design board layer 4

2.3.5 Layer 5 (ground plane)

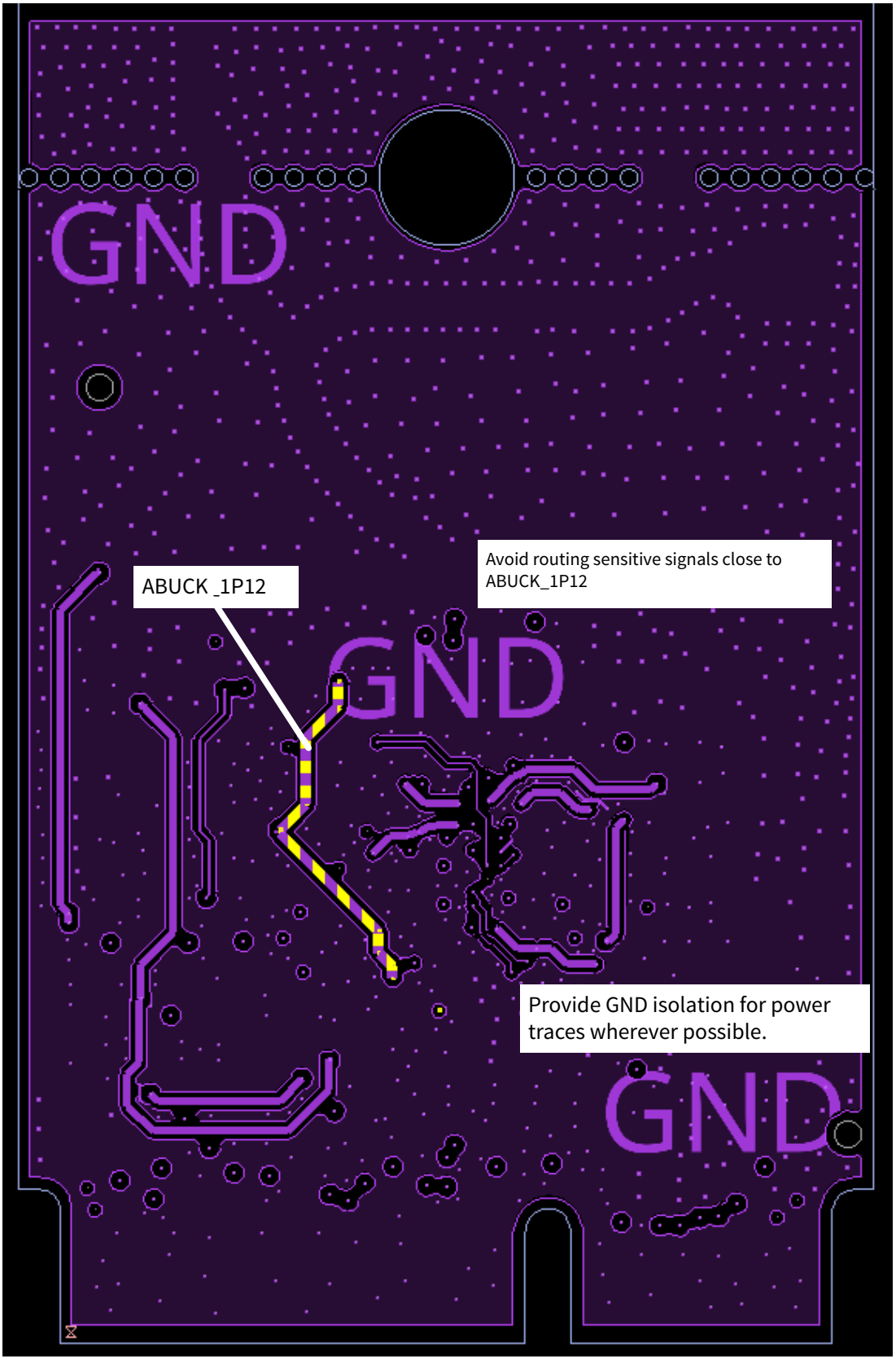

Figure 10 Reference design board layer 5

2.3.6 Layer 6 (component placement/signal plane)

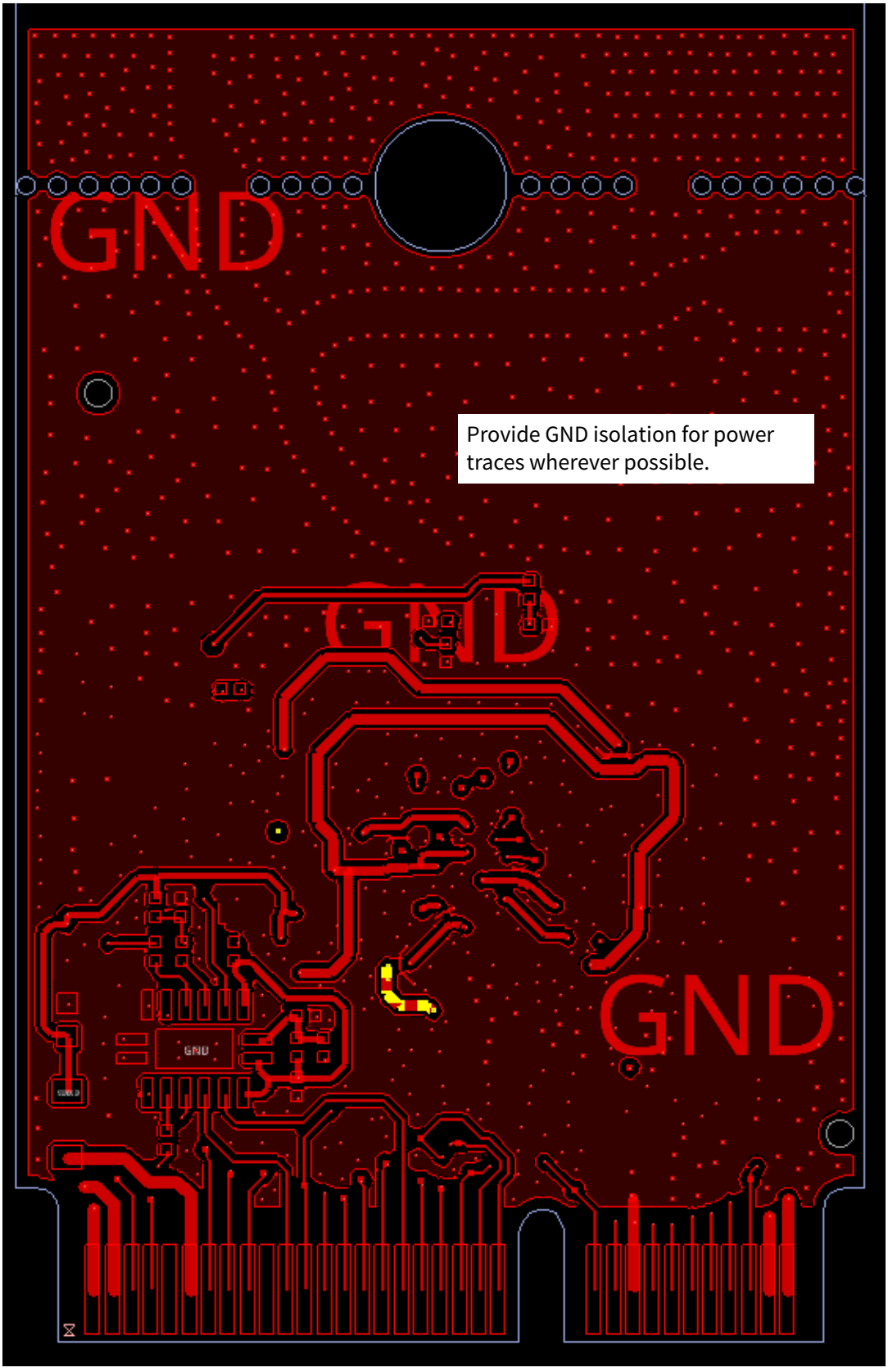

Figure 11 Reference design board layer 6

3 Component selection

This section provides component selection guidance for optimizing the performance of the following power rails:

- VBAT (ASR_VDDBAT, BTLDO_VDDBAT)
- ABUCK (ASR_VLX)
- VDDOUT_RF3P3
- VDDOUT_BT3P3
- Front end

3.1 External components selection

The selection of inductor depends on the DC resistance (DCR), AC resistance (ACR), saturation currents, temperature rise criteria, and footprint/height. The use of smaller components may negatively impact overall efficiency performance. Ensure that the effective capacitance does not drop by more than 69% of the nominal value at 3.6 V.

3.2 ABUCK inductance

The nominal inductor value is 2.2 µH.

Table 3 Recommended inductors

Vendor	Part #	L (µH)	Tol (%)	DCRmax (mW)	DCRAVG (mW)	Current rating (A)	Size (in)	Purpose
Murata	DFE201610E_2R2M	2.2	±20	140	117	1.7	0806	ASR output inductor
Murata	LQM2MPN2R2MG0	2.2	±20	138	110	1.2	0806	
Murata	WIP201610S-2R2ML	2.2	±20	140	117	2.0	0806	

Table 4 ASR (ABUCK) generic inductor specifications

Requirement	Value
Typical value	2.2 µH
PWM switching frequency	4 MHz
Tolerance	±20%
DCR nominal	0.11 Ω to 0.15 Ω
ACR at 4 MHz	≤ 1.2 Ω at no-load
Maximum rated current (40°C rise)	1600 mA
Inductance vs. DC bias-current profile	2.0 µH at 200 mA 1.9 µH at 400 mA 1.2 µH at 600 mA 0.9 µH at 800 mA 0.7 µH at 1000 mA

The inductor characteristics listed in the following table must be known to determine the suitability with the ASR (ABUCK).

Table 5 ASR (ABUCK) inductor requirements

Criteria	Value
Inductor tolerance	No greater than ±20%
DCR	DCR versus temperature
ACR	• ACR vs. frequency under no-load, mid-load, and maximum load conditions • ACR vs. frequency under minimum, typical, and maximum operating temperatures, at maximum load • ACR vs. 4 MHz ripple current amplitude under no load and maximum load conditions
I_{SAT}	Saturation current based on (nominal inductance of 30%)
I_{TEMP}	• Temperature saturation current is specified when the self-heating temperature of the inductor is raised +40°C • Inductance under ITEMP versus operating temperature range

3.2.1 Inductor comparative criteria

DC resistance

The DC resistance (DCR) contributes to the conduction power losses of the ABUCK. Excessive DCR can cause power losses up to 5%.

Saturation current (I_{SAT})

The saturation current (I_{SAT}) is defined as the load current that causes the inductance to drop by 30% of the nominal value. Typically, datasheets of multilayered inductors do not explicitly present the saturation current information because of the lower current level.

An excessive drop in inductance can lead to additional inductor losses because of increased inductor ripple current through the ACR. Increased inductor ripple current can also lead to greater switching-current injection into the ground.

For pulse-width modulation (PWM) loop stability, effective inductance at a 600 mA load should be at least 1.2 µH across all parts (tolerance included). For optimal peak PWM efficiency at a 200 mA load, the effective inductance should be at least 1.9 µH.

Temperature saturation current (I_{TEMP})

The temperature saturation current (I_{TEMP}) is the current that causes the inductor to self-heat above +40°C. Typically, I_{TEMP} is provided in the datasheets and is usually higher than the saturation current (I_{SAT}). I_{TEMP} should be at least 1000 mA.

Inductance under I_{TEMP} vs. operating temperature range

Consider the following for an inductance under I_{TEMP} over the entire operating temperature range:

- Characterize the inductance assuming temperature saturation current (I_{TEMP}) across the full operating temperature range of the inductor
- The recommended operating temperature range is from –40°C to +125°C, including the rise in temperature due to inductor self-heating (+40°C)
- The inductor operating temperature (up to +125°C including inductor self-heating of +40°C) corresponds to the customer product temperature maximum of 85°C. The inductance should not vary by more than ±4%

3.3 External bypass capacitance

Table 6 Capacitor recommendations

Vendor	Part	C (µF)	Tol. (%)	Voltage (V)	Temp rating	Size (in)	Purpose
Murata	GRM033R61A104KE15	0.1	±10	10	X5R	0201	PMU input bypass
Murata	GRM033R60J105MEA2	1.0	±20	6.3	X5R	0201	CLDO output
Murata	GRM033C80J105ME05	1.0	±20	6.3	X6S	0201	
Murata	GRM155C70J225KE11	2.2	±10	6.3	X7S	0402	BTLDO output
Murata	GRM155R61C225KE11	2.2	±10	16	X5R	0402	
Murata	GRM155R61A475MEAA	4.7	±20	10	X5R	0402	ASR, PMU input bypass
Murata	GRM188R60J475ME84	4.7	±20	6.3	X5R	0603	
Murata	GRM188R60J475KE19	4.7	±10	6.3	X5R	0603	
Murata	GRM188R61C106KAAL	10	±10	16	X5R	0603	

Critical parts used on the Bluetooth® front end are RF switch and band-pass filters.

4 Routing guidelines

4.1 General PCB design guidelines

- Keep noisy lines and crystal trace away from RF traces and place ground vias along RF traces
- Do not use ground cuts under RF traces
- Properly ground RF switches using vias
- Do not place noisy supply lines (such as VBAT and VDDIO) or noisy digital lines (UART and flash) over sensitive supply traces like radio power rails
- Minimize the coupling of noisy signals to crystal traces
- Avoid different power traces on adjacent layer overlap
- Separate different power traces on the same layer as far as possible
- Add ground side shielding to improve isolation to different neighboring power traces
- Avoid placing crystal-trace vias close to noisy signals on other layers
- Use a solid ground layer under the ABUCK regulator
- Use power supply traces wide enough to support the required currents. For example, 10 mils, ½ oz. copper trace can handle 500 mA (at 10°C). The width must be increased to 25 mils for 900 mA. The current-carrying capacity goes up to 700 mA for 10 mils and 1.5 A for 25 mils at 30°C for the same ½ oz. copper weight
- When trace routing jumps layers, use multiple vias if the trace needs to support a high current

***Note**: In figures throughout this section, an asterisk symbol is used to indicate a star connection. A star connection is formed at a decoupling capacitor that attaches to more than one circuit element.*

4.2 Routing the VBAT and ABUCK networks

The main power supply (VBAT) coming directly from the platform battery and the switching regulator (ABUCK) network generating 1.12 V are shown in Figure 12 and Figure 13.

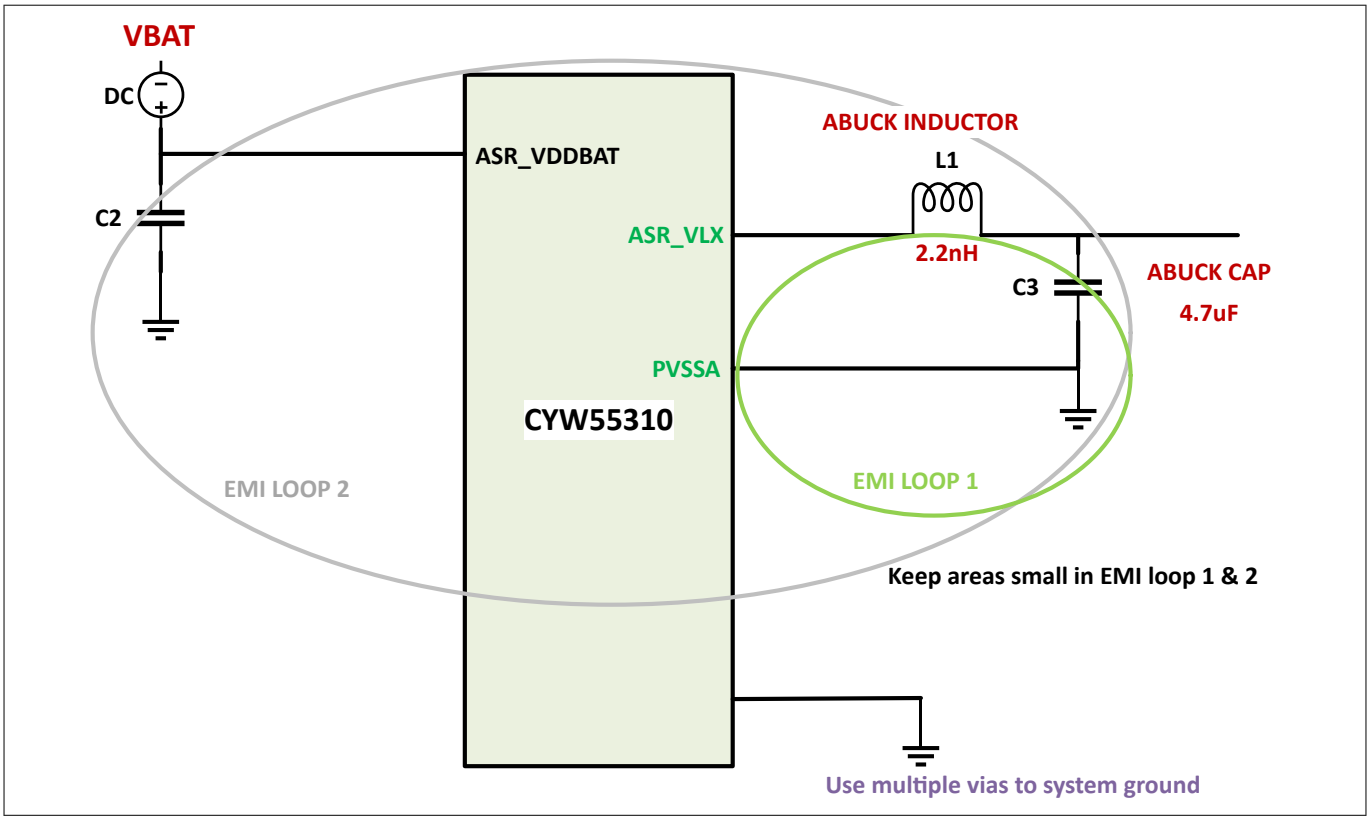

Figure 12 VBAT and ABUCK power networks

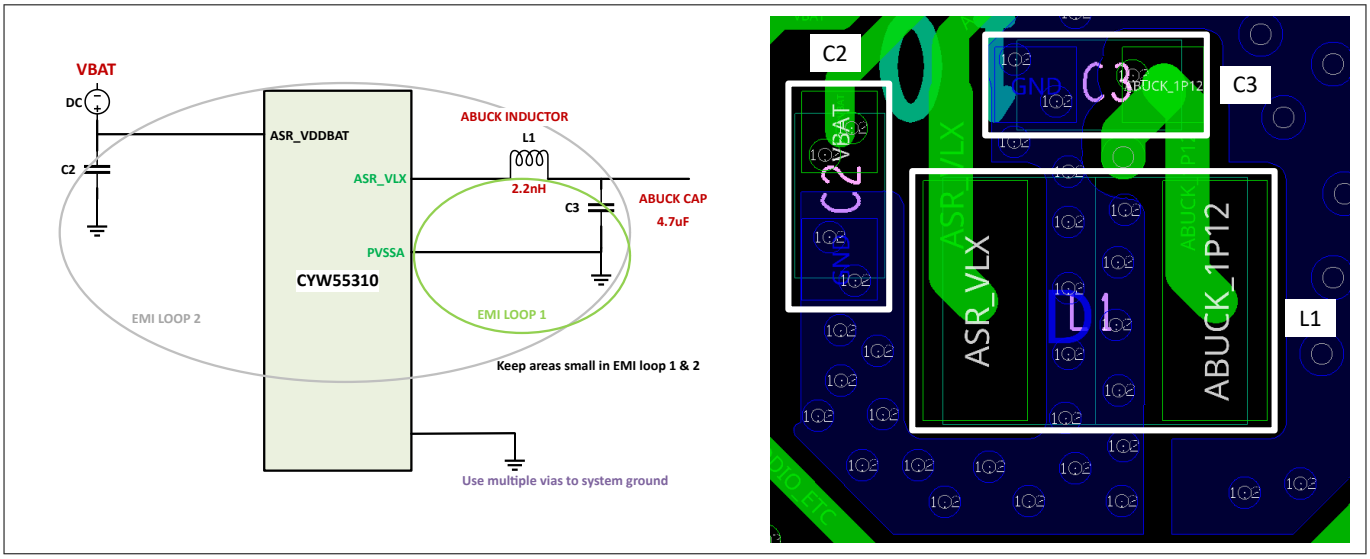

Figure 13 VBAT and ABUCK power supply networks (detailed view)

The following routing and placement guidelines apply to the VBAT capacitor, the ABUCK capacitor, the ABUCK inductor, and their associated traces:

- Place all components on the top layer close to pins A9, A10, and B10
- To handle the large currents between the previously mentioned components and pins, use traces that are as thick as possible

- Use multiple vias to the second layer to reduce the area of EMI loops 1 and 2
- To prevent ABUCK circuit transients from coupling onto lower-layer traces, use a solid (layer 2) ground under the ABUCK inductor. See Figure 14 for the ground used under the ABUCK inductor in the reference design

***Note**: The peak current flowing through the ABUCK inductor and capacitor is 400 mA. To avoid large switching-voltage spikes that lead to power efficiency losses, long-term chip reliability problems, or both, do not use thin and long traces to these components.*

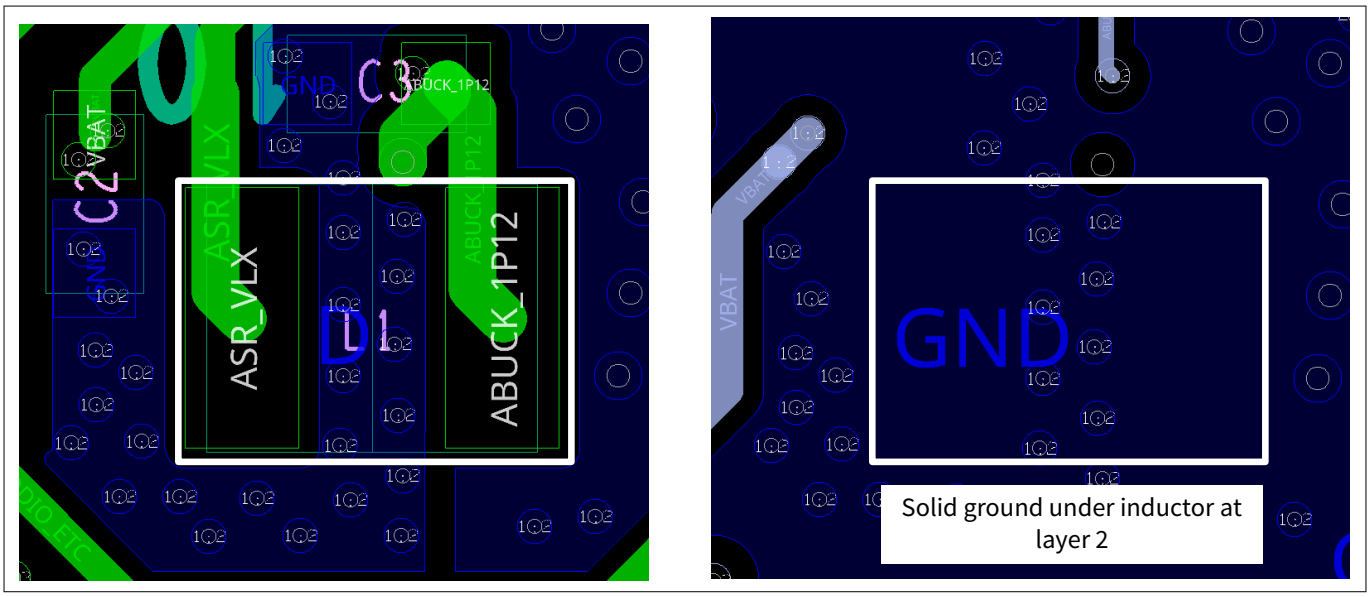

Figure 14 ABUCK inductor (and capacitor) ground plane

Figure 15 shows the EMI loops in the ABUCK switching regulator. Sensitive signals should not be routed through the areas bounded by the two loops that go through the power MOSFET switches of the ABUCK. Each loop starts at a capacitor and ends at its associated ground terminal. The area within each loop is proportional to the EMI.

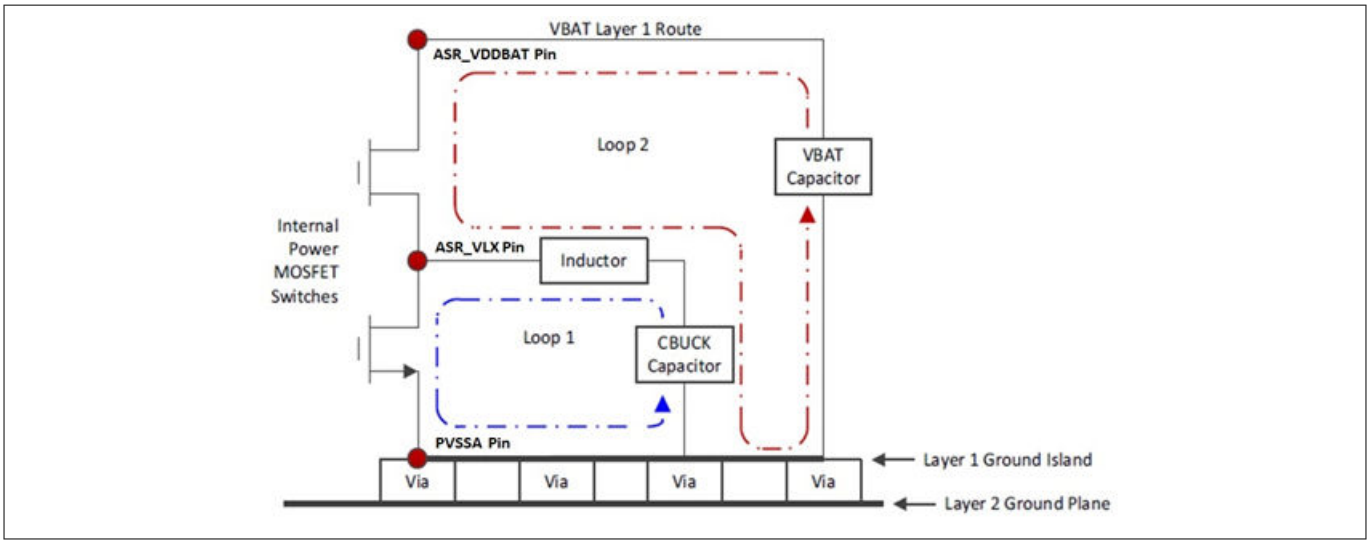

Figure 15 EMI loops in buck switching regulator

When addressing EMI, consider the following:

- Avoid routing sensitive signals through the areas bounded by these two loops

- The VBAT and ABUCK capacitors sit on a top-layer ground island directly connected to the PVSSA pin
- Multiple vias are used to connect the ground island on layer 1 to the ground plane on layer 2
- The ground plane on layer 2 also acts as a shield over the two EMI loops to prevent noise radiation from reaching the adjacent layers

Additional considerations:

- Bypass capacitors on VBAT and ABUCK should have as many ground vias as possible
- Isolate the ground plane around ABUCK to avoid noise coupling
- Use at least two vias for the bypass capacitor
- Minimize the area enclosed by the following loops to reduce EMI in the forward and return paths:
  - ASR_VLX to inductor and capacitor to PVSSA
  - ASR_VDDBAT to supply bypass capacitors to PVSSA

4.3 Routing the ABUCK_1P12 network

***Notes**:*

1. *Power traces are routed as a star configuration*

2. *A few power rails have two decoupling capacitors: If your design allows the component to be placed at the bottom, place the decoupling capacitor at the bottom close to the power input pin so that the decoupling capacitor is more effective. Place the smaller value capacitor closer to the AIROC™ CYW55310 chip*

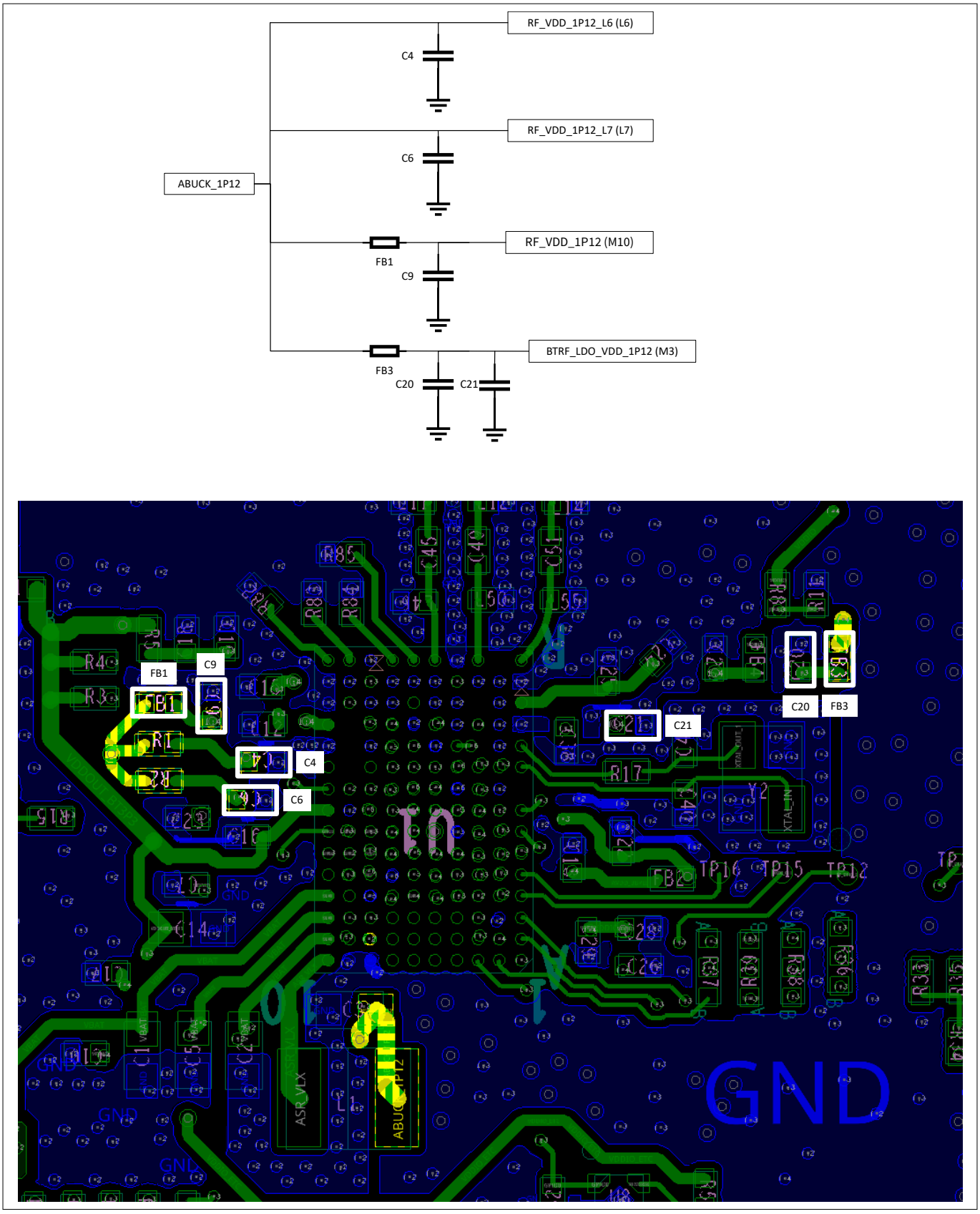

Figure 16 ABUCK_1P12 network (top layer)

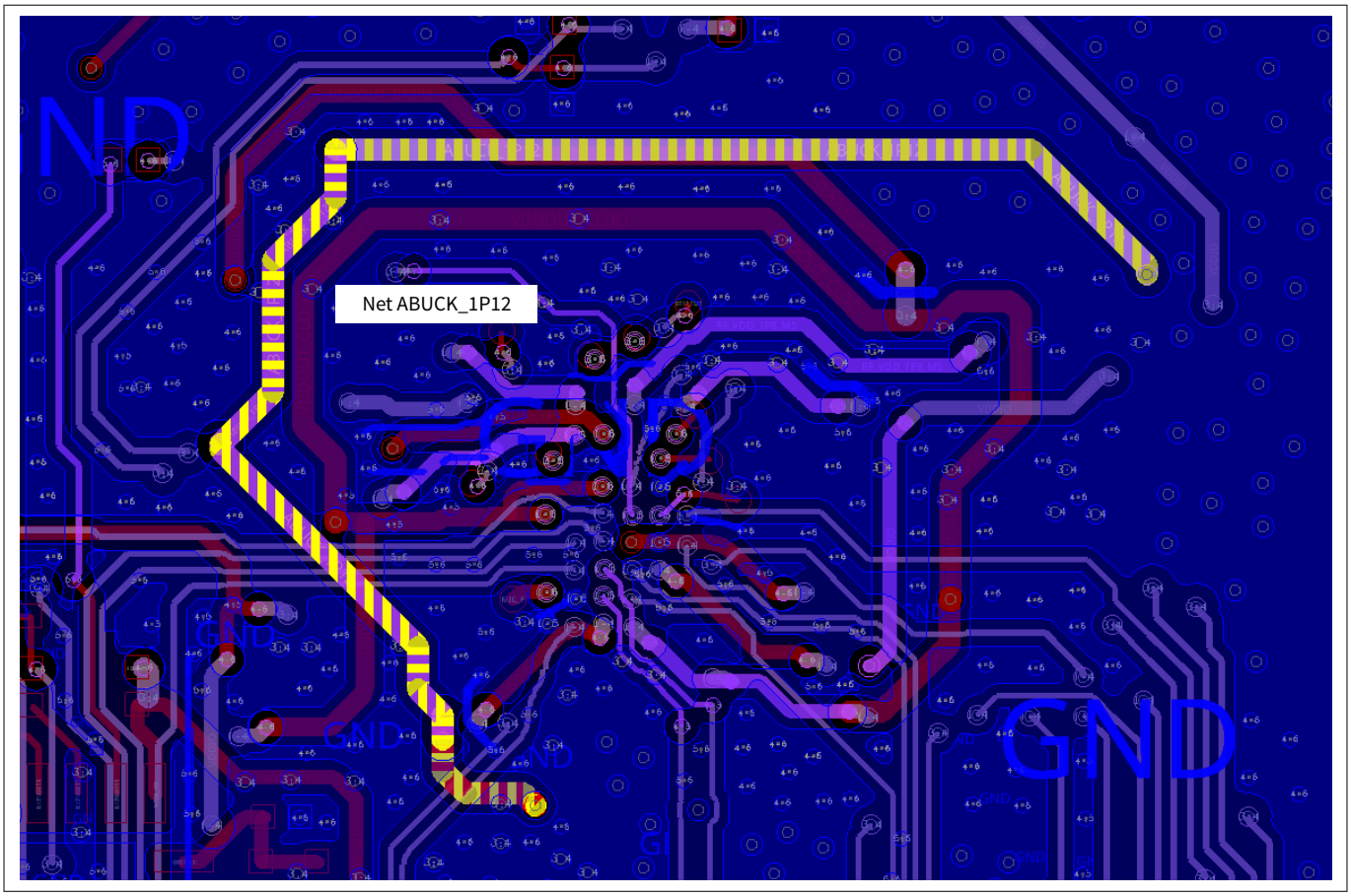

Figure 17 ABUCK_1P12 network (layers 4, 5 and 6)

4.4 Routing the VDDOUT_BT3P3 trace

***Notes**:*

1. *Power traces are routed as a star configuration*
2. *A few power rails have two decoupling capacitors: If your design allows the component to be placed at the bottom, place the decoupling capacitor at the bottom close to the power input pin so that the decoupling capacitor is more effective. Place the smaller value capacitor closer to the AIROC™ CYW55310 chip*
3. *BTRF_PA_VDD_3P3 has two decoupling capacitors, but C24 is not installed by default. If PCB space is limited, omit C24*

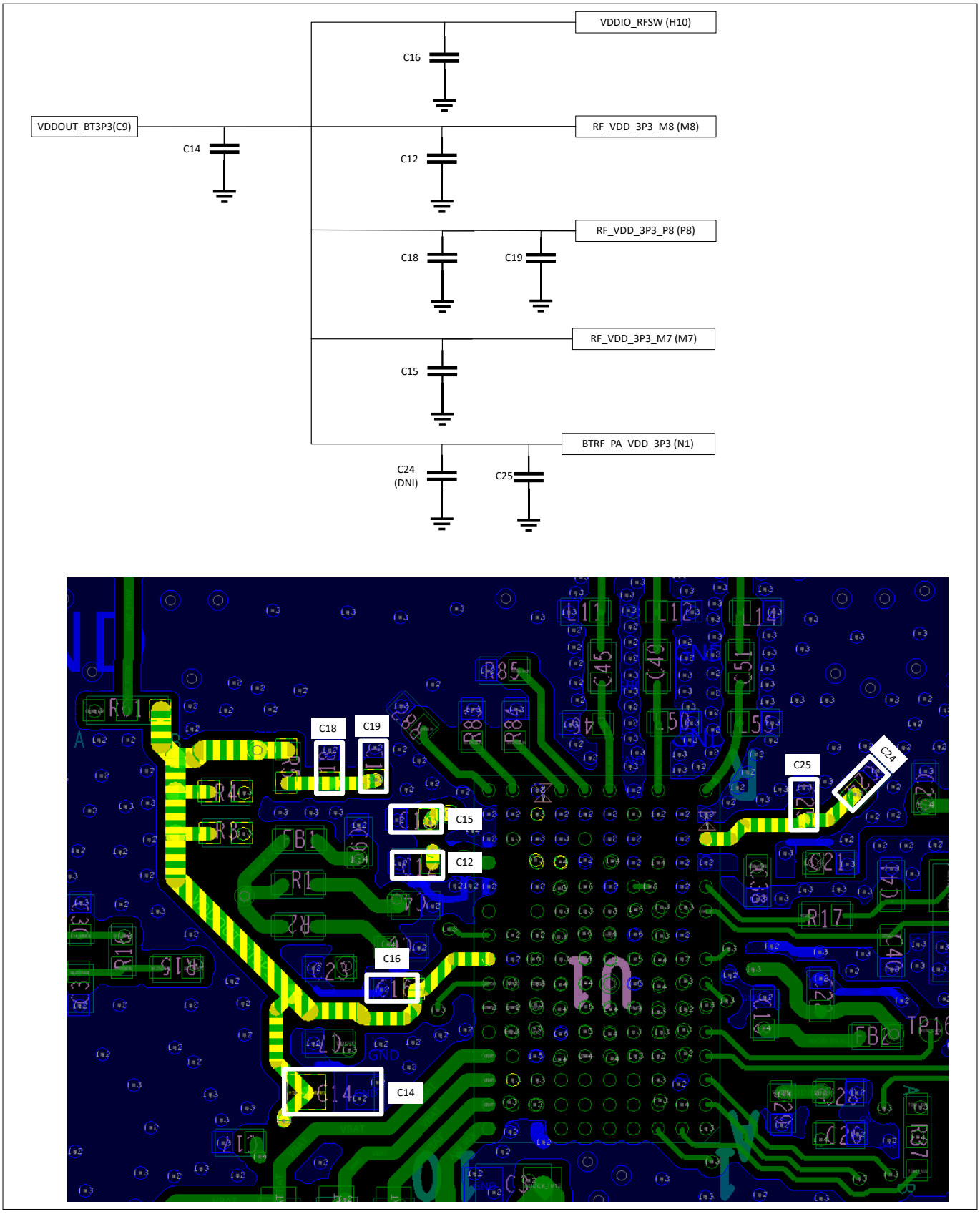

Figure 18 VDDOUT_BT3P3 routing (top layer)

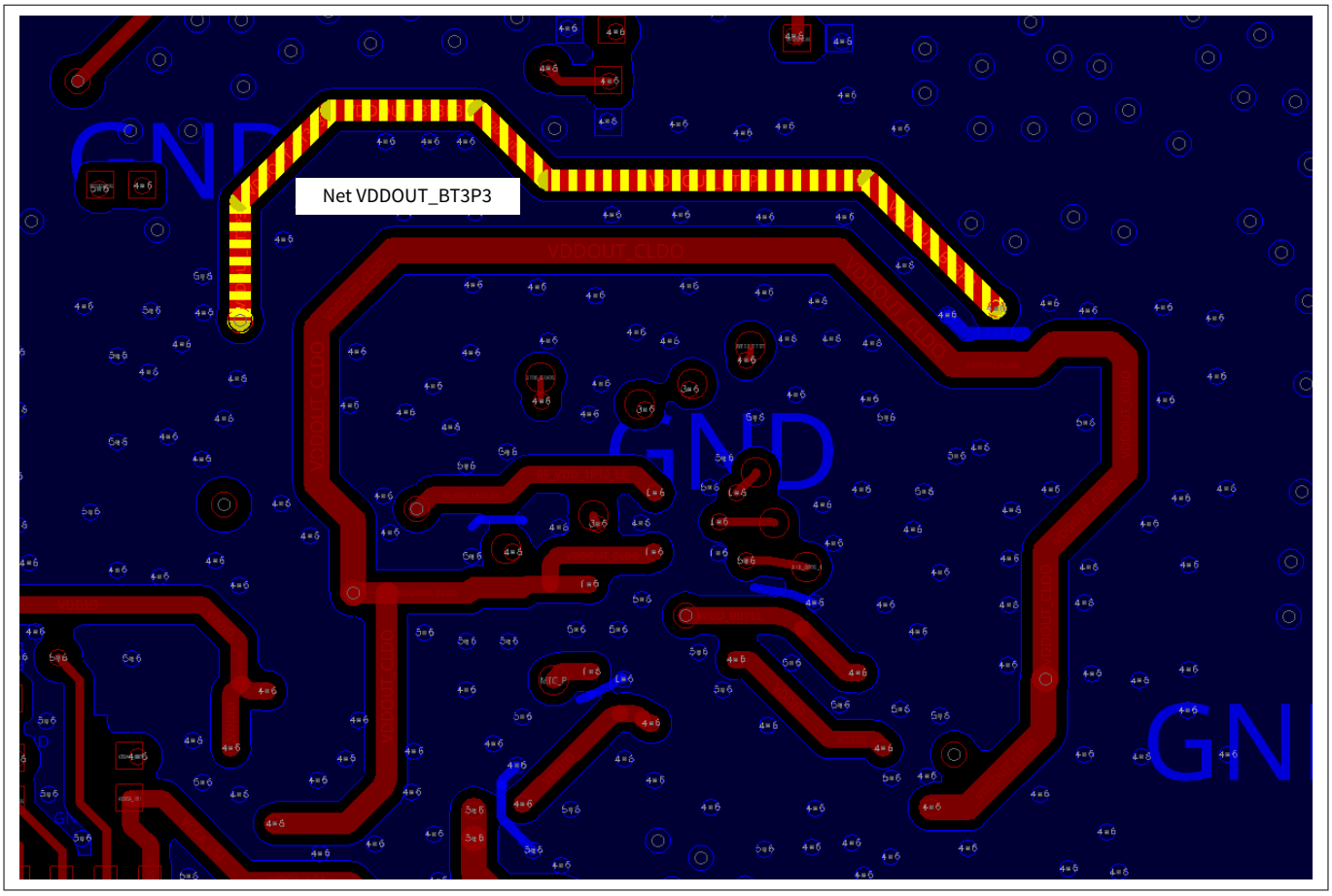

Figure 19 VDDOUT_BT3P3 routing (bottom layer)

4.5 Routing the VDDOUT_CLDO traces

***Notes**:*

1. *Power traces are routed as a star configuration*
2. *A few power rails have two decoupling capacitors: If your design allows the component to be placed at the bottom, place the decoupling capacitor at the bottom close to the power input pin so that the decoupling capacitor is more effective. Place the smaller value capacitor closer to the AIROC™ CYW55310 chip*

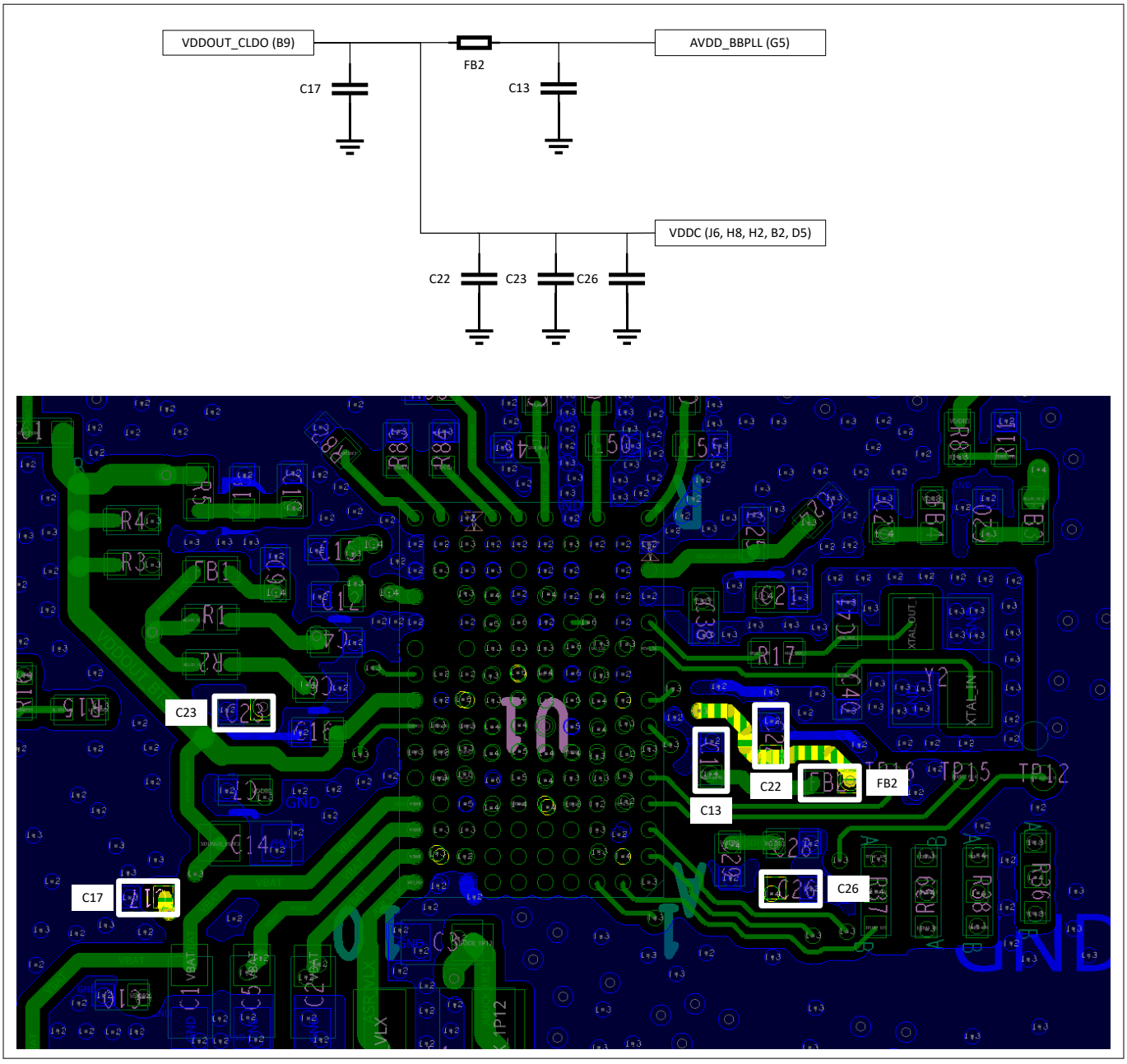

Figure 20 VDDOUT_CLDO routing (top layer)

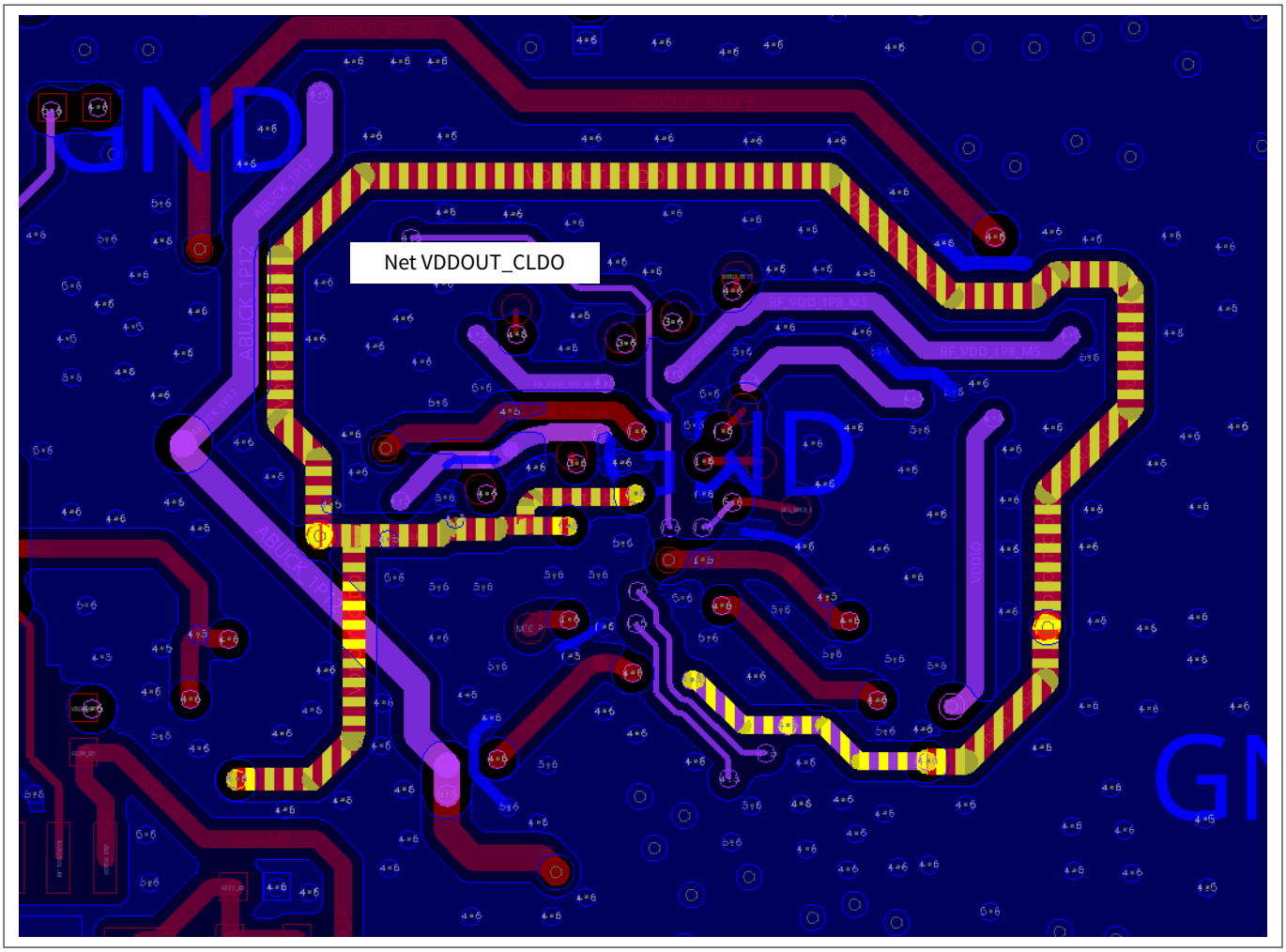

Figure 21 VDDOUT_CLDO routing (layers 5 and 6)

4.6 Routing the crystal traces

When routing the crystal (XTAL) traces, consider the following:

- Ensure that XTAL_IN and XTAL_OUT traces do not overlap
- Isolate ground as XTAL ground at layer 1 and layer 2, and connect XTAL ground directly to XTAL_GND pins
- Ensure that the XTAL ground plane has direct vias to the reference ground plane

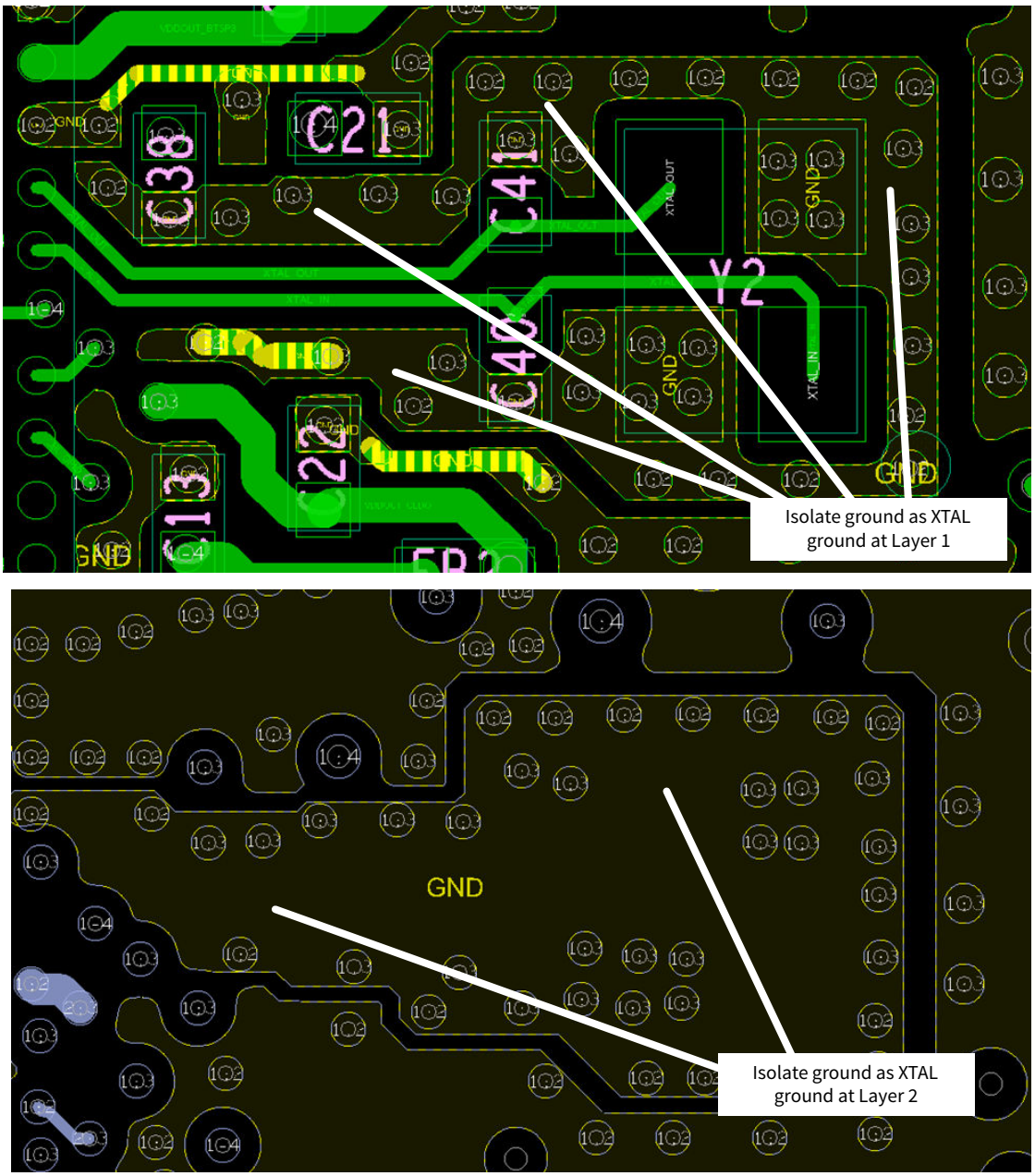

Figure 22 XTAL ground

4.7 Routing the RF traces

When routing the RF traces, consider the following:

- Keep the RF traces on the component layer to avoid using vias
- Add ground stitches around the RF traces
- Ensure that adequate isolation and spacing are provided for each RF trace
- Ensure that the RF traces and stack-up are properly designed so that the RF trace impedance is controlled to 50 Ω
- Make sure that the front-end matching components are placed close to the chip pin

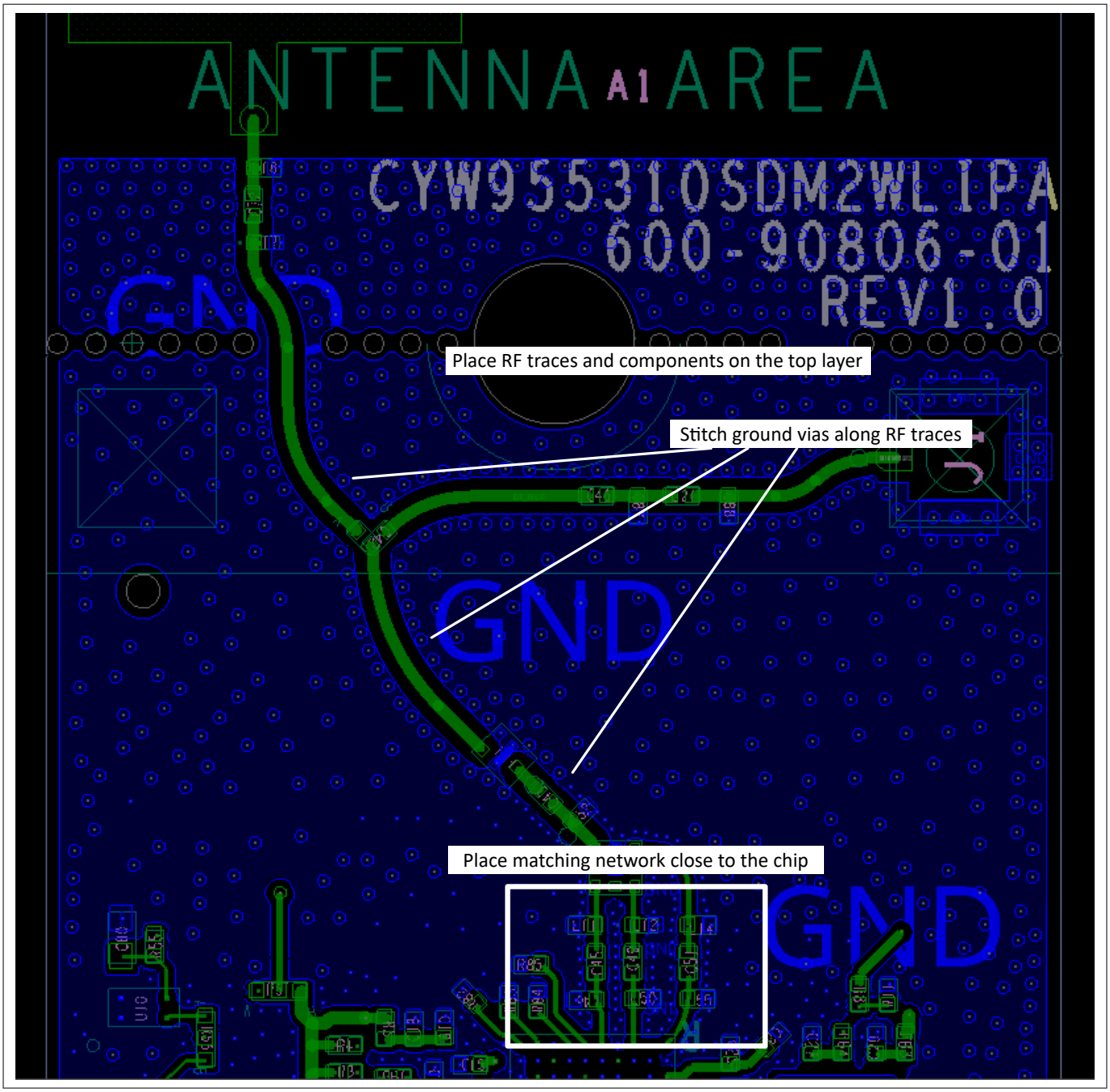

Figure 23 RF component placement and RF trace routing

4.8 RF front end area

Attention: Do not route any traces in the RF front end area on layers 2 and possibly on layer 3.

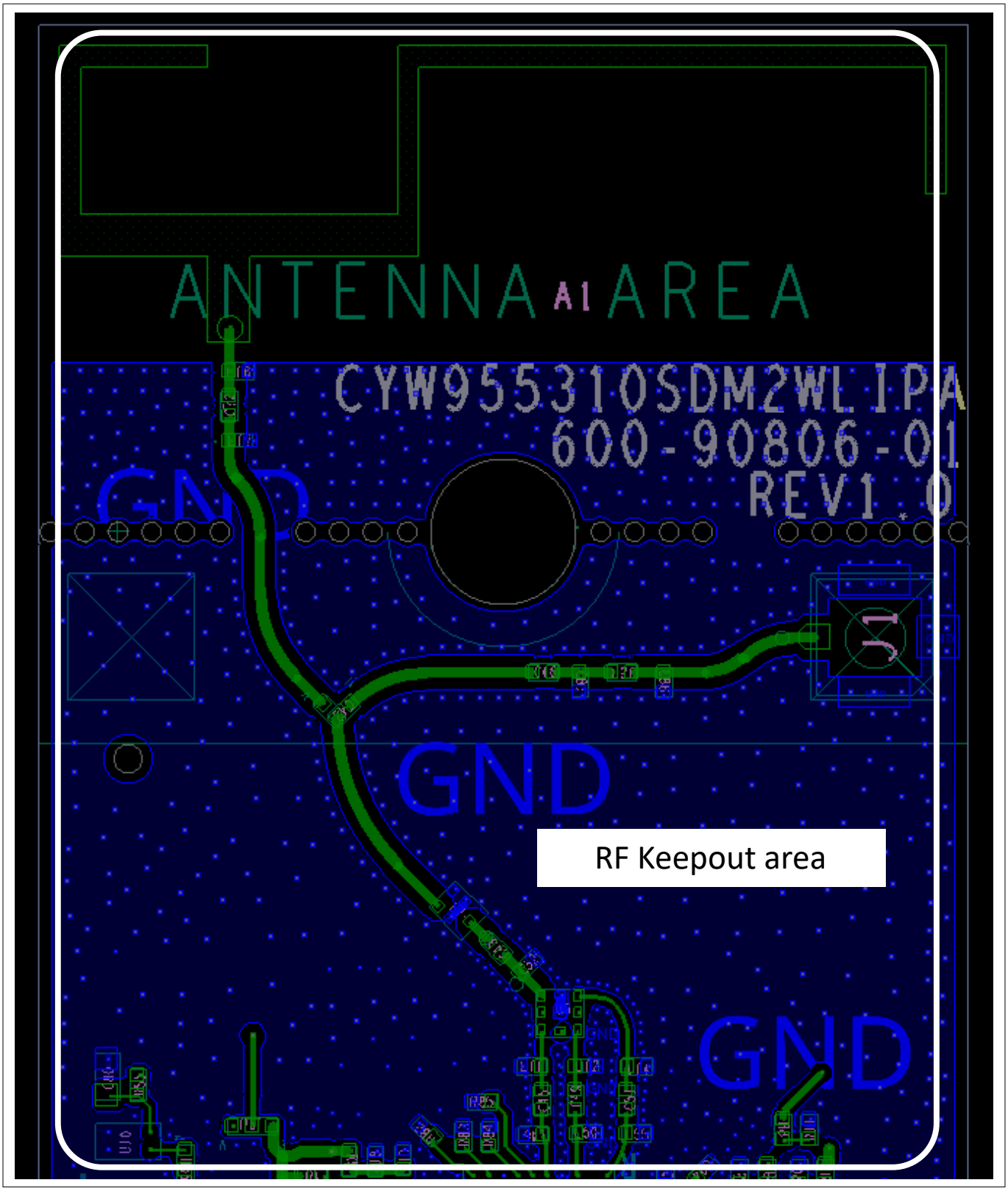

Figure 24 RF area routing keepout

References

[1] Infineon Technologies AG: *CYW955310SDM2WLIPA design pack*
[2] Infineon Technologies AG: *AIROC™ CYW55310 Bluetooth® & Bluetooth® LE webpage*; Available online

***Note**: Contact Infineon support to access technical documentation and software.*

Revision history

Document revision	Date	Description of changes
**	2026-07-13	Initial release

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