Hardware design guidelines for PSOC™ Control C3M/P8, C3M/P7 MCUs

About this document

Scope and purpose

This application note describes how to set up a hardware environment for the PSC3M/P8, PSC3M/P7 MCUs. It provides the hardware design considerations, including package selection, power, clocking, reset, I/O usage, programming/debugging, and PCB layout guidelines.

Intended audience

This application note is intended for hardware designers.

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1 Introduction

The PSC3M/P8, PSC3M/P7 MCUs are designed for real-time control, enhanced sensing, secure, and low-power operations. A few target applications include:

- Digital power applications with switching frequencies up to 2 MHz, used in power supplies for AI servers, telecom, EV chargers, and solar systems
- High-switching-frequency wide-bandgap technologies, such as silicon carbide (SiC) and gallium nitride (GaN), enabling power conversion, and motor control applications
- Motor control application devices for appliances, light electric vehicles, robots, and drones

2 Package selection

Device package selection is one of the first crucial decisions for the PCB design. Several considerations drive this decision, including the number of I/O pins required, PCB and product size, PCB design rules, and thermal and mechanical stresses. The PSC3M/P8, PSC3M/P7 devices have a large selection of packages to match the application requirements with an efficient and cost-effective solution. Package offerings include the compact VQFN package and the E-LQFP package, which is easier to layout on lower layer counts and low-cost PCBs.

Table 1 Packages

Package	Pins
VQFN	48-pin
	64-pin
E-LQFP	64-pin
	80-pin
	100-pin

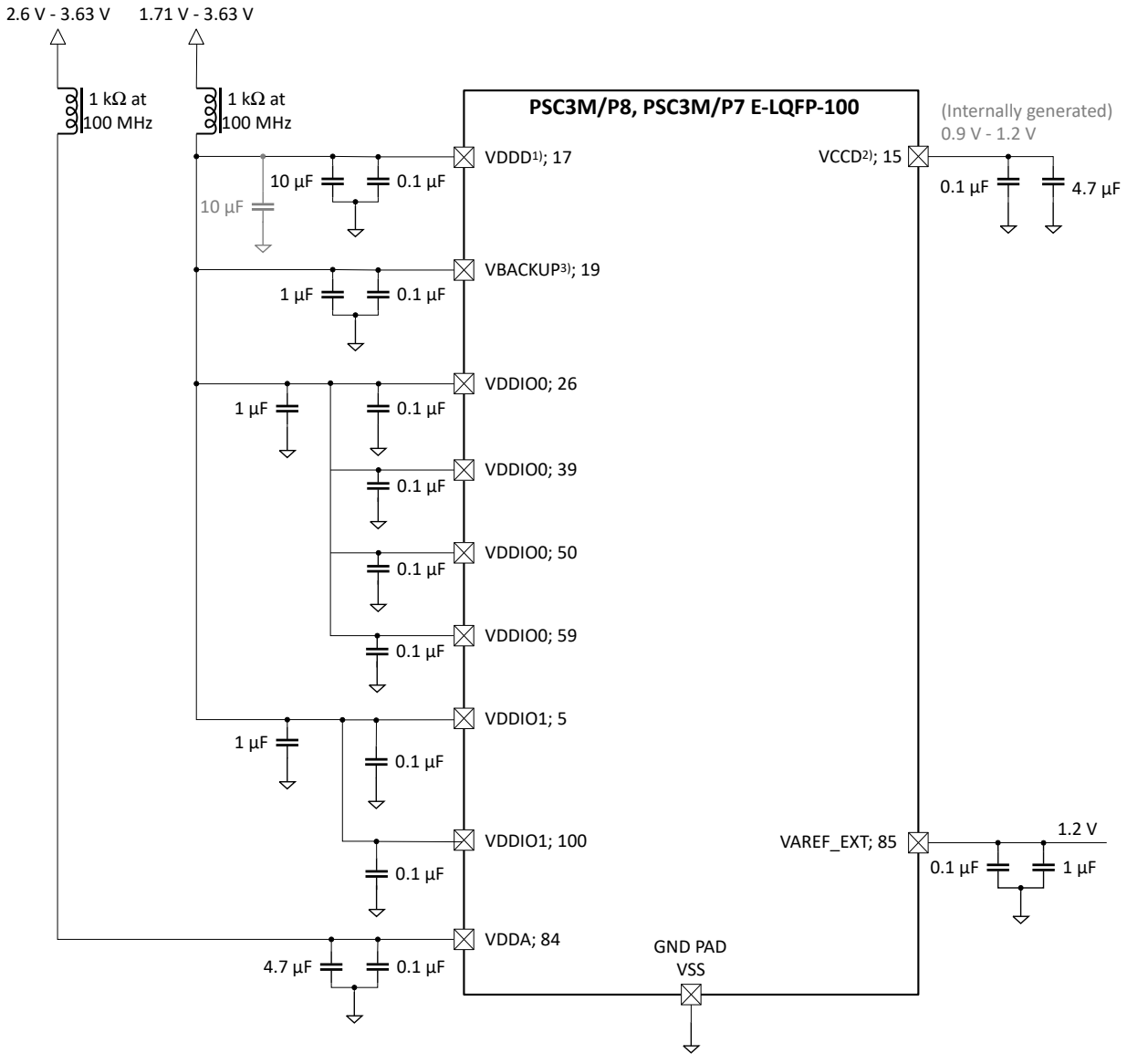
3 Power

The power system for the PSC3M/P8, PSC3M/P7 MCUs is based on separate analog and digital supplies as listed in Table 2. The VDDA supply voltage must be maintained between 2.6 V to 3.63 V while the rest of the system can be powered using a supply voltage ranging from 1.71 V to 3.63 V. The device can be either powered by a single supply voltage range, from 2.6 V to 3.63 V or two separate supplies:

- 2.6 V to 3.63 V for VDDA
- 1.71 V to 3.63 V for the digital power supplies (VDDD, VDDIO0, VDDIO1, and VBACKUP)

Depending on the application requirement, connect VBACKUP to a dedicated coin cell with a supply voltage between 1.4 V to 3.63 V.

The external analog reference voltage (VAREF_EXT) requires a 1.2 V reference. It is recommended to use a 1.2 V precision reference voltage generator for high accuracy and low noise.



1) A 10 µF capacitor on VDDD supports full operating voltage range for Active/Hibernate modes and Deep Sleep with VDDD ≥ 2.3 V. Use 2x10 µF capacitors or a single 22 µF capacitor for Deep Sleep operation down to 1.71 V.
2) VCCD is internally generated. It is only used to connect external bypass capacitors for the internal LDO. Do not use it to power external circuits.
3) VBACKUP can be connected to a coin cell (1.4 V to 3.63 V) or a supercapacitor depending on the application. If not used, connect it to VDDD.

Figure 1 Typical power supply connections for the PSC3M/P8, PSC3M/P7 MCUs (E-LQFP-100)

Figure 1 shows a typical powering scheme for the 100-pin LQFP package. See the device datasheet for details about other pin packages. Details of connections to the power pins are described in the Power pin connections section.

3.1 Power domains

Table 2 Power domains

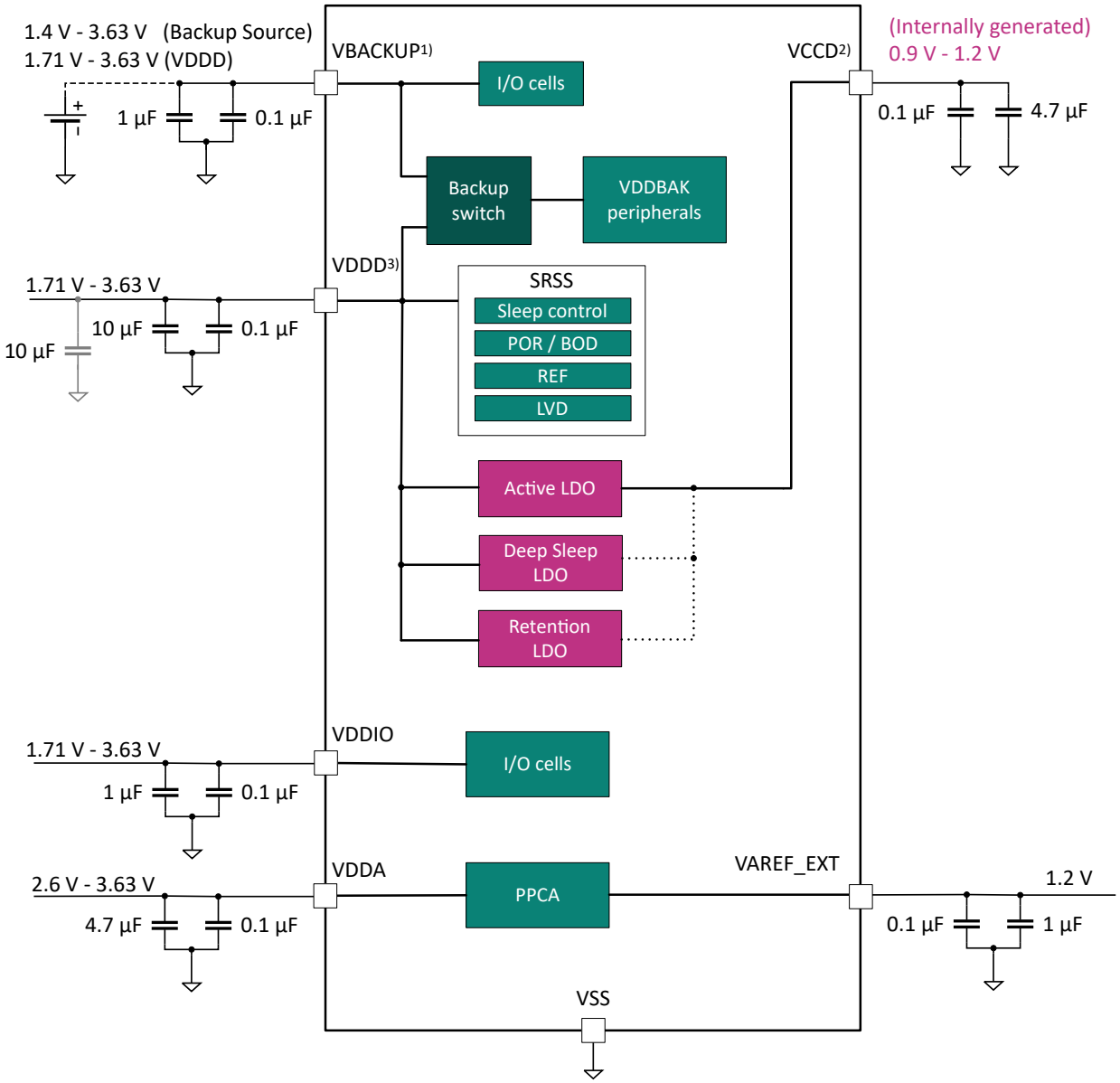
Power domain	Associated pins
Analog	VDDA
Digital	VCCD
I/O	VDDIO0, VDDIO1
Shared digital and I/O	VDDD, VBACKUP

Table 3 Power supply pin description

Pin name	Function	Nominal power domain voltage range
VDDD	Shared power supply pin for internal voltage regulators, internal logic, I/O domain, and debug interface	1.71 V to 3.63 V
VCCD	Only used to connect an external bypass capacitor for the integrated core logic supply LDO outputs ***Note**: Do not connect any external supply or use this pin to power external components*	0.9 V to 1.2 V
VBACKUP	Backup domain power supply including the backup domain I/O cells. Connect to a coin cell or a super capacitor depending on the application. If not used, it should be connected to VDDD	1.4 V to 3.63 V
VDDA	Powers the analog domain circuits	2.6 V to 3.63 V
VDDIO0, VDDIO1	Power supply for the I/O cells	1.71 V to 3.63 V

3.2 Power pin connections

Figure 2 shows the power pin connections and the routing block diagram. All the power pins can be connected together to a single regulated supply between 2.6 V to 3.63 V. When using a single supply source, place the ferrite beads for minimizing the noise interference between the analog and digital supply inputs. Alternatively, use independent regulated supplies for all power input pins within their valid operating voltage range. For device-specific details including pin information, see the device datasheet.



1) VBACKUP can be connected to a coin cell (1.4 V to 3.63 V) or a supercapacitor, depending on the application. If not used, it should be connected to VDDD.
2) VCCD is internally generated. It is only used to connect external bypass capacitors for the internal LDO. Do not use it to power external circuits.
3) A 10 µF capacitor on VDDD supports full operating voltage range for Active/Hibernate modes and Deep Sleep with VDDD ≥ 2.3 V. Use 2x10 µF capacitors or a single 22 µF capacitor for Deep Sleep operation down to 1.71 V.

Figure 2 Power distribution and domains

3.3 Core regulators

The device features multiple low-dropout (LDO) regulators that are responsible for powering the device in the supported power modes. All the core regulators draw power from the VDDD supply and generate a voltage ranging between 0.9 V to 1.2 V. The VDDD supply needs to be a stable voltage ranging between 1.71 V to 3.63 V and bypassed with capacitors as per the values specified in the Power pin connections section. Bypass capacitors should be placed as close as possible to the device supply pins.

The LDO output is connected to the VCCD pin with the sole purpose of connecting an external bypass capacitor. Do not use this pin to supply power to any external circuits.

***Note**: The bypass capacitors should be of X5R type or better.*

3.4 Power ramp-up considerations

The device has no special power-on and ramp-up considerations. The power-on reset (POR) circuit on the VDDD and internal VCCD supply ensures that the device has a stable power supply before deasserting the reset. If backup functionality is not used, connect VBACKUP to VDDD. Other pins used for I/O and analog supply can be left unconnected if the associated sections are not used in the application. The device enters Active mode by default after power-on.

***Note**: VDDIO supply on/off state change is only allowed in Active, Sleep, and Deep Sleep modes. It should not be changed in Hibernate mode.*

4 Clocking

The device supports the following clock sources:

- **Internal oscillators:**
  - **Internal main oscillator (IMO):** 8 MHz ±2%, fast wake-up, low jitter
  - **Internal high-speed oscillator (IHO):** 48 MHz ±1%
  - **Internal low-speed oscillator (ILO):** 32 kHz ±10%, also used as a wake-up source for the RTC
- **External crystal oscillators (ECO and WCO):**
  - **External crystal oscillator (ECO):** 4 MHz to 35 MHz
  - **External watch crystal oscillator (WCO):** 32.768 kHz
  - **External clock (EXTCLK):** Maximum frequency up to 100 MHz
- **Frequency locked loop (FLL):** Output range of 25 MHz to 100 MHz with ±1% accuracy
- **Two digital phase-locked loops (DPLL#0 and DPLL#1):** Output range of 50 MHz to 200 MHz, used for the main CPU, PPCA blocks, SCB, and TCPWM (outside the PPCA)

Use the recommended clock source for the respective CLK_HF domains.

Table 4 Clock distribution and Active mode performance parameters

CLK_HF	Peripherals	Recommend source	Max permitted clock frequency [1]			
			OD (1.2 V)	LP (1.1 V)	MF (1.0 V)	ULP (0.9 V)
CLK_HF0	AES, CPU, PERI, SRSS, SVGS, Peri clock group 0 (Debug trace), Peri clock group 1 (CRYPTO)	DPPL0	180 MHz	150 MHz	70 MHz	50 MHz
CLK_HF1	IOSS, LPCOMP, Peri clock group 2 (TCPWM[0])	DPLL0	180 MHz	150 MHz	70 MHz	50 MHz
CLK_HF2	Peri clock group 3 (CAN, SCB[0:4])	FLL	100 MHz	100 MHz	25 MHz	25 MHz
CLK_HF3	PPCA	DPLL1	200 MHz	150 MHz	70 MHz	50 MHz
CLK_HF4	Peri clock group 5 (SCB[5-6])	DPLL1 (For fast SPI)	200 MHz	150 MHz	70 MHz	50 MHz
		FLL (For UART/I^2C)	100 MHz	100 MHz	25 MHz	25 MHz
CLK_HF5	EXT_CLK_OUT	All	80 MHz	80 MHz	80 MHz	50 MHz
CLK_HF6	CSV	All	8 MHz	8 MHz	8 MHz	8 MHz

1) Maximum clock frequency after the corresponding clock source (DPLL/FLL + dividers). All internal tolerances and affects are covered by these frequencies.

4.1 External crystal oscillator (ECO)

The device can be clocked using the external crystal oscillator (ECO). A crystal of 4 MHz to 35 MHz connected to the ECO_IN (P1.0) and ECO_OUT (P1.1) pins of the device is used to generate the clock. When using the ECO, enable it using Device Configurator in ModusToolbox™. To minimize the stray capacitance, the crystal along with associated components should be placed on the same layer as the MCU and close to the device pins.

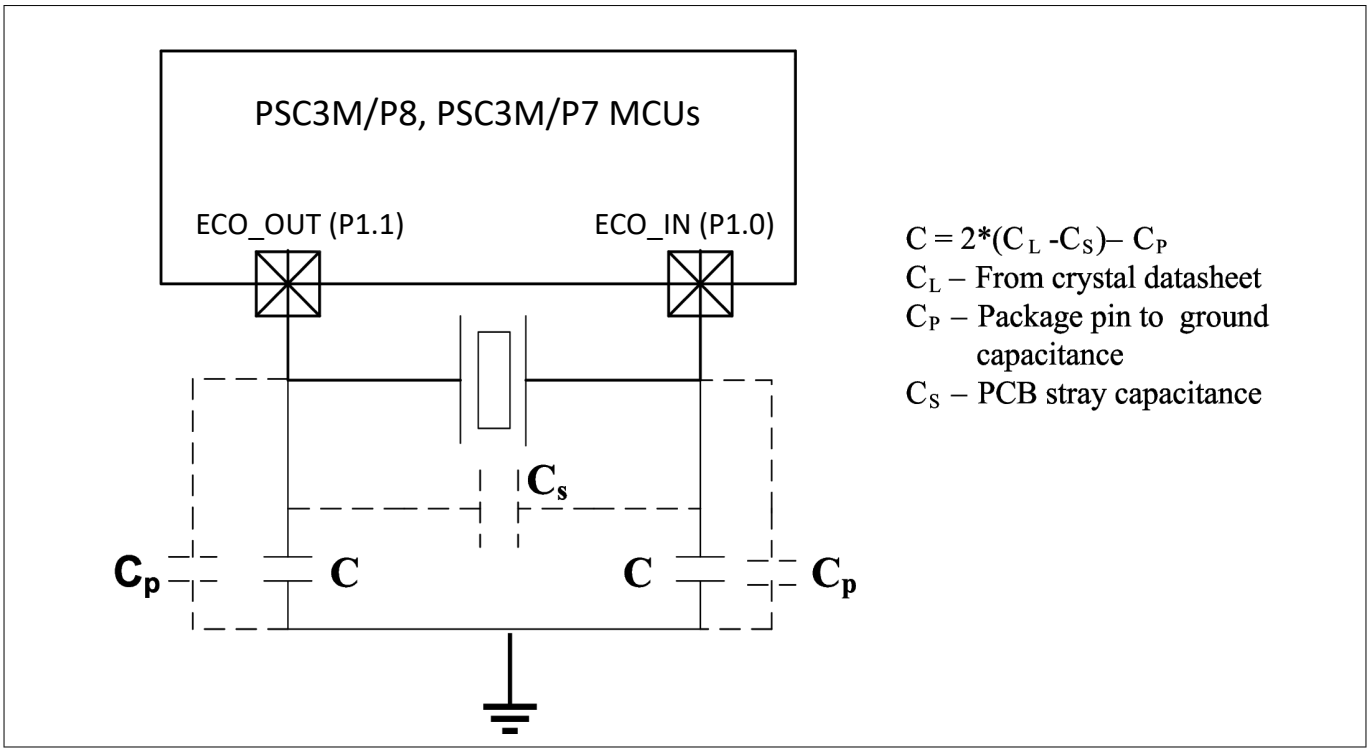


Figure 3 ECO connections

The external load capacitors for the ECO are calculated as:

$$C = 2 \times (C_L - C_S) - C_P \quad (1)$$

Where,

- **C_L:** Crystal load capacitor as per the crystal datasheet
- **C_S:** PCB stray capacitance. A well-designed PCB minimizes the stray capacitance and includes a grounded copper trace between the crystal input and output wires
- **C_P:** Package pin-to-ground parasitic capacitance (see the device datasheet for more details on pin parasitic capacitance)

4.2 Watch crystal oscillator (WCO)

The watch crystal oscillator (WCO) block requires an external 32.768 kHz crystal connected between WCO_IN (P0.1) and WCO_OUT (P0.0) along with input and output load capacitors for proper operation.

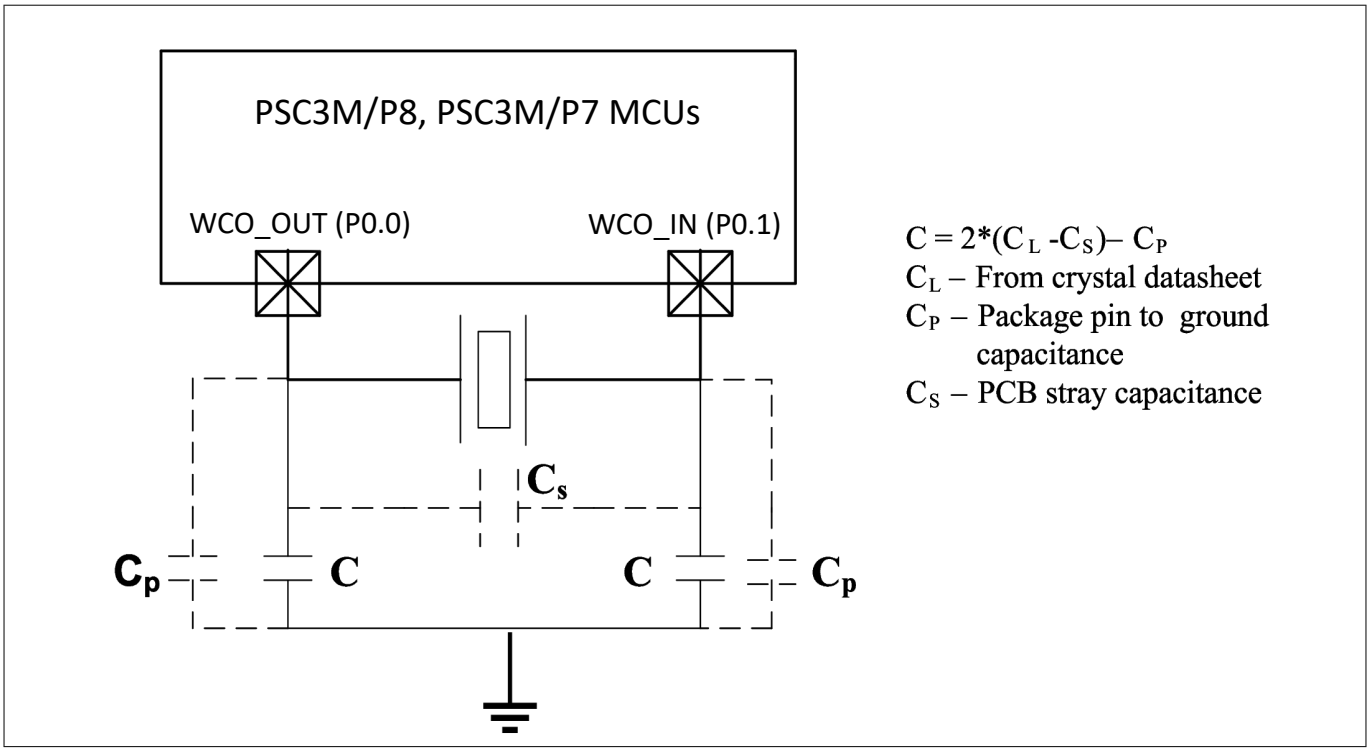


Figure 4 WCO connections

The external load capacitors for the WCO are calculated as:

$$C = 2 \times (C_L - C_S) - C_P \quad (2)$$

Where,

- **C_L:** Crystal load capacitor as per the crystal datasheet
- **C_S:** PCB stray capacitance. A well-designed PCB minimizes the stray capacitance and includes a grounded copper trace between the crystal input and output wires
- **C_P:** Package pin-to-ground parasitic capacitance (See the device datasheet for more details on pin parasitic capacitance)

4.3 External clock

The external clock is a 0.001 MHz to 100 MHz range clock that can be sourced from a signal on pin P7.2 or P8.3. This clock can be used as the source clock for either the DPLL or FLL, or can be used directly by the high-frequency clocks.

4.4 Clock supervisor output

A clock supervision (CSV) circuit is implemented for each clk_hf domain. The CSV circuit detects a stopped clock or an abnormal frequency of the monitored clock. There are clock counters for both the monitored clock and the reference clock. Parameters for each counter define the frequency of the reference clock and the upper and lower limit for the frequency of the monitored clock.

If the dedicated frequency range comparator detects a stopped clock or a clock outside the specified frequency range, an abnormal state is signaled. Depending on the register settings and how the monitored clock is used on the device, either a reset or an interrupt is generated.

5 Reset

5.1 Reset pin (XRES)

The device has a reset pin (XRES) that is active $\overline{\text{LOW}}$. XRES should be externally pulled up to VDDD via a 4.7 kΩ resistor, which will ensure that the XRES pin is not left floating in the design and that the device can function properly. It is recommended to connect a capacitor (typically 0.1 µF) to the XRES pin to filter out glitches and give the reset signal better noise immunity. Optionally, if the device is controlled by an external host, the XRES pin can be directly driven by the host.

5.2 Power supply monitoring

Ensure that the MCU is not running outside the valid operating conditions, a broad range of power monitor circuits are provided within the MCU. See the device architecture reference manual and datasheet for more details.

5.2.1 Power-on reset (POR)

Power-on reset (POR) circuits provide a reset pulse during the initial power ramp. At the system level, only the VDDD power supply rail is observed.

5.2.2 Brown-out detection (BOD)

The brown-out detection (BOD) circuit protects the operating or retaining logic from possibly unsafe supply conditions by applying reset to the device. The BOD circuits for the power supply rails VDDD and VCCD are provided. A reset is generated when an out-of-range condition is detected on the monitored voltages. This circuit is required to detect a sneaking voltage drop of the battery power supply.

5.2.3 Low-voltage detection (LVD)

Before the BOD level threshold generates a reset, it is possible to get a low-voltage detection (LVD) warning by the configurable circuit. The LVD trip point can be configured by writing to the PWR_LVD_CTL register. When the trip threshold is triggered, LVD generates a CPU interrupt for possible safety measures. By default, LVD is disabled because it consumes power; it must be enabled if used by the application.

5.3 Watchdog reset

An internal watchdog timer (WDT) and a multi-counter watchdog timer (MCWDT) support a wide range of capabilities, which can be configured to reset the device in case of software faults that halt code execution.

6 GPIO pins

The device provides flexible GPIO pins. All GPIO pins can be controlled by the firmware. Most of them also have alternative connections to the device peripherals. Different peripherals have different dedicated or fixed pins for their terminals. The best performance is achieved when a peripheral is connected to its own dedicated pin or pins. However, for flexibility, the peripheral can be connected to other pins using the high-speed I/O matrix (HSIOM). The flexibility of the devices and the capability of its I/O to route signals to most pins greatly simplify the circuit design and board layout. If a peripheral has fixed pins, it can be connected to those pins only. For more information on the pin-out and the pin alternate functionality, see the device datasheet.

Some I/O pins are overvoltage tolerant (OVT). These pins implement an alternate scheme without clamping diodes connected to the supply lines, thereby limiting the leakage current when the corresponding VDDIO voltage is lower than the external voltage applied on the pin; for example, when the device is powered down (VDDIO = 0 V while connected to an active bus). It is recommended to use these pins for PMBus®/SMBus interface and they do not support operation with external logic voltages higher than the pin input/output voltage range specifications. See the device datasheet for details.

6.1 I/O pin selection

When a hardware system is designed based on the PSC3M/P8, PSC3M/P7 devices, the GPIO pins should be assigned in sequence as shown in Table 5. See the device datasheet to determine whether the listed peripheral block is supported by the device.

Table 5 I/O pin selection guide

Block	Pin name	Port#[Pin#]	Remarks
System function pins			
Run-time debug	–	–	If you need run-time debugging or trace support, select the appropriate setting in the System settings. The selection will automatically lock the required I/Os for the purpose
External crystal oscillator (ECO)	ECO_IN	P1.0	External crystal frequency range: (4 MHz to 35 MHz)
	ECO_OUT	P1.1	
Watch crystal oscillator (WCO)	WCO_IN	P0.1	If you need a highly accurate and low-frequency clock for RTC or Deep Sleep wakeup purpose, use the WCO block with an external 32.768 kHz crystal or clock. Note that the WCO block is present in the device's backup domain and it is available, even when the VDDD of the device is removed (VBACKUP supply shall be present)
	WCO_OUT	P0.0	
Wakeup (Hibernate)	HIB_WAKEUP	P2.1 or P7.0	The Hibernate wakeup pin is used to wake the device from Hibernate mode
External clock	EXT_CLK	P7.2 or P8.3	Configure the pin as an input (high impedance digital) for receiving the external clock
Analog pins			

(table continues...)

Table 5 (continued) I/O pin selection guide

Block	Pin name	Port#[Pin#]	Remarks
System function pins			
Low-power comparator	LPCOMP0_IN+, LPCOMP1_IN+	P6.5, P6.3	Non-inverting [+] and inverting [-] inputs for the two low-power comparators
	LPCOMP0_IN-, LPCOMP1_IN-	P6.4, P6.2	
ADC analog input pins	Analog inputs directly connected to dedicated samplers	AN_A0 to AN-A7 and AN_B0 to AN_B3	Pins supporting ADC functionality
	Analog inputs connected through AMUX	B4 to B7, P8.0, P8.2	
Digital pins			
Timer/counter pulse-width modulator (TCPWM)	TCPWM pins	See the device datasheet	The device has multiple TCPWM blocks inside the PPCA cores and outside. All the output signals can be routed to any GPIO pin by either using the alternate functionality or by using peri.tr_io_output via the HSIOM
Serial communication block (SCB)	SCB pins	See the device datasheet	The devices have up to seven SCBs out of which one SCB is capable of working in Deep Sleep mode for SPI and I2C, up to two SCBs are Fast-SPI capable and two SCBs are connected to OVT pins, which can protect the I/Os in MCU power down state when connected to an active bus (PMBus®/ SMBus use case). See the device datasheet for the device-specific capabilities

6.2 Unused pin connections

During and after a POR, by default, the I/O pins are in a high-impedance (High-Z) analog state with disabled input buffers. The advantage of leaving unused I/O pins open is that the current consumption of the MCU is lower when compared to the use of a terminal resistor; this also reduces the bill of materials (BOM) cost. PCB designers need to ensure that the trace length of the unused pins is short to avoid the unused trace from acting like an antenna and picking up noise. If any pin is routed for future expansion options, it is recommended to place a 0 Ω resistor close to the pin and keep it unmounted as long as the pin is not in use.

Internal pull-up can be enabled for unused I/O pins to ensure that they have a stable state and are not impacted by external noise. If the high-impedance state of any unused I/O pins after POR is not acceptable, the specific pins can be terminated to GND or pulled-up to VDDD using a resistor ranging between 4.7 kΩ to 10 kΩ.

6.3 Direct connection to GND or power supply

The I/O pins should not be connected directly to GND or to power supply because the power supply traces can take effect as an antenna to the pin and the captured noise can cause a latch-up effect.

7 Programming and debugging

The device program and debug interface provides a communication gateway for an external device to perform programming or debugging. The external device can be an Infineon-supplied programmer and debugger or a third-party device that supports programming and debugging. The Serial-Wire Debug (SWD) or the JTAG interface can be used as the program/debug protocol between the external device and the MCU. In addition, the device supports Arm® Embedded Trace Macrocell (ETM) on the Cortex®-M33 CPUs.

7.1 Serial Wire Debug (SWD)

For SWD programming or debugging, you can use the onboard programmer/debugger in the MCU kits when available or connect the device to an external debugger, such as CY8CKIT-005-A MiniProg4 via any connector supported by the debugger. MiniProg4 supports a 10-pin and a 5-pin connector for SWD programming and debugging. The *VTREF* voltage should be connected to the same voltage as the VDDIO voltage of the SWD interface pins. This voltage is used by the onboard or external debugger to set the logic voltage level for the SWD signals.

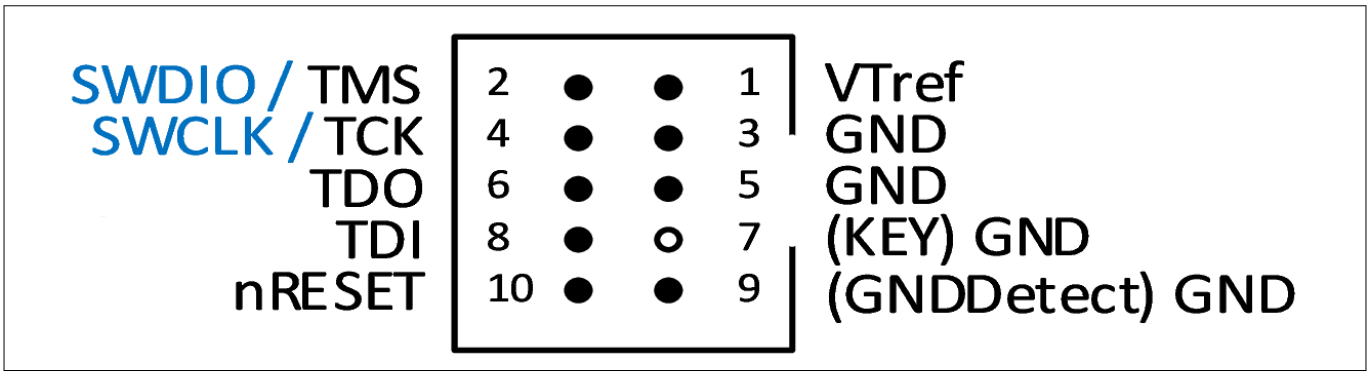


Figure 5 10-pin Cortex® debug connector

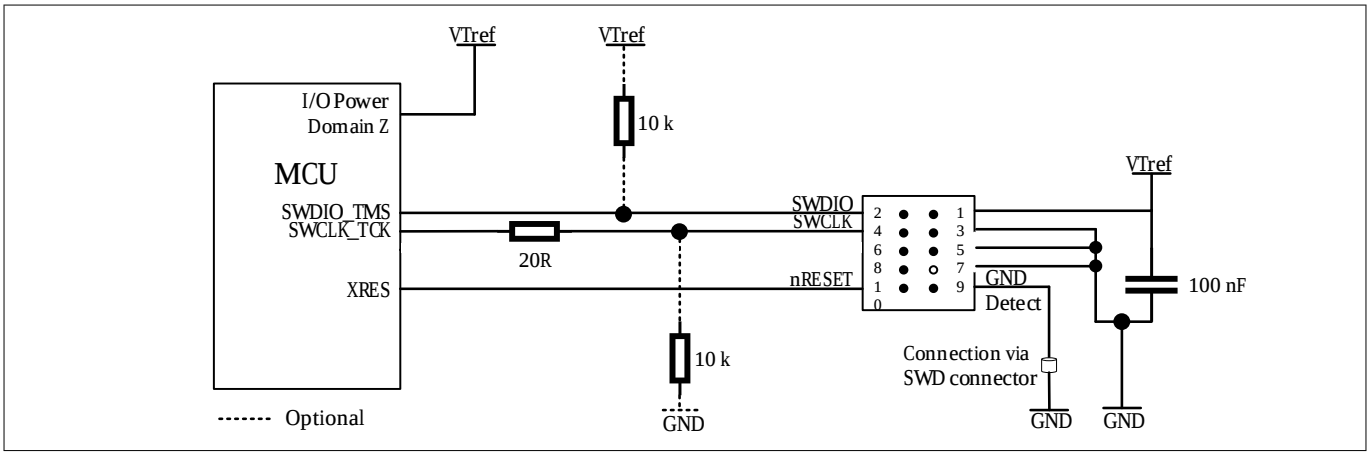


Figure 6 SWD debug connection to the MCU with 10-pin MIPI SWD debug connector

From Figure 5, it can be observed that the minimum of four connections (two SWD pins, *GND*, and *VTREF*) are needed from the target board to the debugger in SWD mode. XRES connection to *NRESET* is used by external programmers/debuggers for hardware reset during programming and debugging operations. This connection is optional if the programmer/debugger supports connecting under software reset.

XRES connection to the program/debug interface is recommended to ensure wider compatibility.

7.2 JTAG

For JTAG programming and debugging, external debuggers like MiniProg3 or J-Link can be used. Both 4-wire and 5-wire JTAG programming is supported.

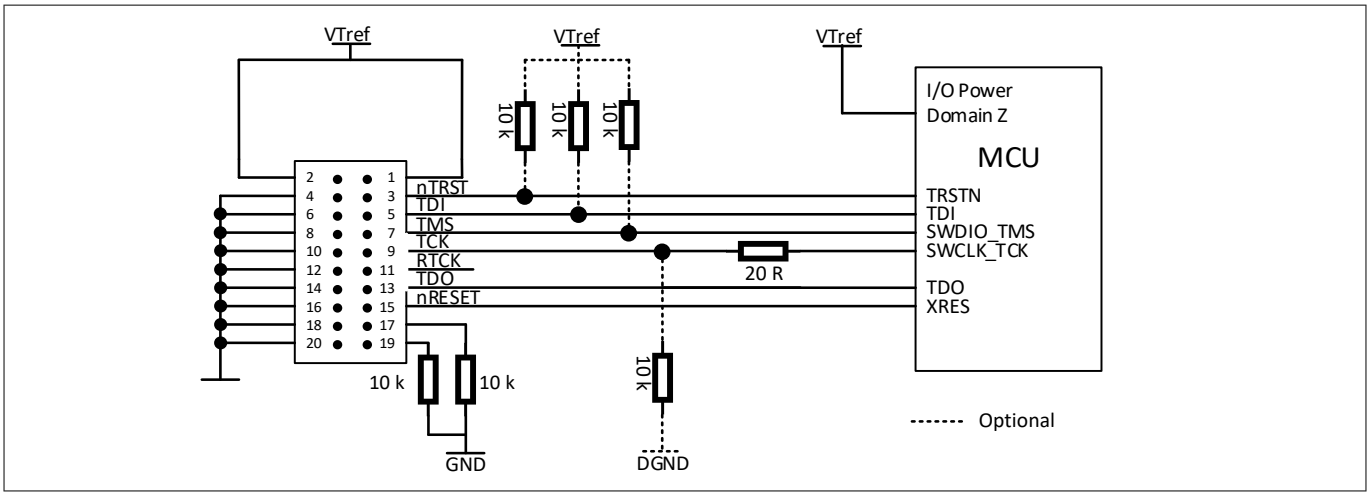


Figure 7 JTAG connection to the MCU with 20-pin IDC connector

7.3 Embedded Trace Macrocell (ETM)

The Cortex®-M33 CPUs in the device supports parallel trace mode with 1, 2, and 4 data lines.

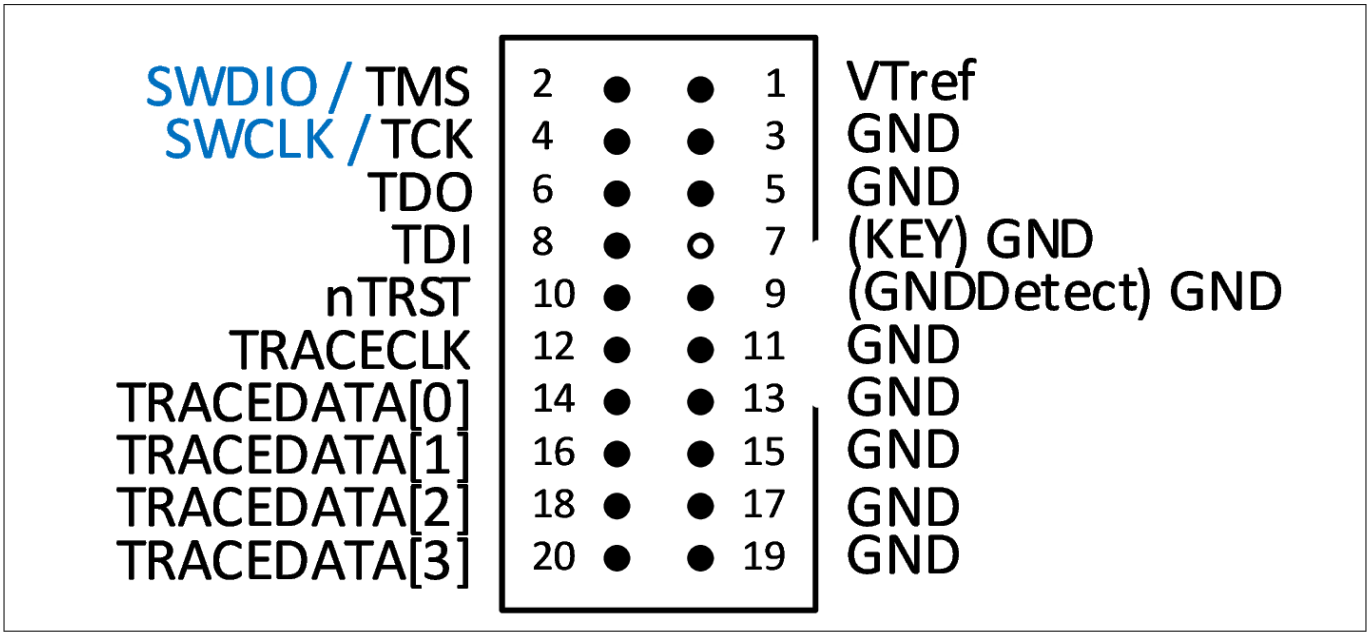


Figure 8 20-pin Cortex® debug + ETM connector

Table 6 20-pin Cortex® debug + ETM header pinout

Pin	Pin name	Functionality
1	*VTREF*	Target reference voltage. Used by the external debugger/trace tool to set the logic voltage level for communication
2	*SWDIO/TMS*	SWD interface data pin/JTAG TMS pin

(table continues...)

Table 6 (continued) 20-pin Cortex® debug + ETM header pinout

Pin	Pin name	Functionality
3	*GND*	Ground
4	*SWCLK/TCK*	SWD clock/JTAG clock
5	*GND*	Ground
6	*TDO*	JTAG TDO pin
7	*(KEY) GND*	No pin on the header. Connected to the ground
8	*TDI*	JTAG TDI pin
9	*(GNDDETECT) GND*	GND connection on the debugger/trace tool side. Can be used to disable the onboard debugger
10	*NTRST*	Used by an external debugger/trace tool to reset the target MCU. Connect to MCU XRES pin
11	*GND*	Ground
12	*TRACECLK*	Trace clock pin
13	*GND*	Ground
14	*TRACEDATA[0]*	Parallel trace data bit 0 pin. Used in 1-bit, 2-bit, and 4-bit mode
15	*GND*	Ground
16	*TRACEDATA[1]*	Parallel trace data bit 1 pin. Used in 2-bit and 4-bit mode
17	*GND*	Ground
18	*TRACEDATA[2]*	Parallel trace data bit 2 pin. Used in 4-bit mode
19	*GND*	Ground
20	*TRACEDATA[3]*	Parallel trace data bit 3 pin. Used in 4-bit mode

7.4 Device Firmware Update (DFU)

The immutable BootROM includes a built-in DFU protocol that enables secure and reliable firmware upgrades through a serial interface. By default, the DFU functionality is disabled and must be explicitly enabled in the OEM policy. The device must also be provisioned before DFU can be used. For more details, contact Infineon Support.

Table 7 DFU mode and serial communication pins

Pin	UART
P8.0	UART - Rx
P8.1	UART - Tx
P8.2	DFU enable (VSS)/DFU disable (VDDIO_1/High-Z)

When DFU is enabled in the OEM policy, P8.2 can either be left floating or pulled-up to the port VDDIO_1 supply voltage to disable the DFU entry after reset. The pull-up or pull-down resistors should be 1 kΩ or less. The arrangement shown in Figure 9 requires only four wires for UART TX/RX and to enable DFU by pulling-down P8.2 to VSS.

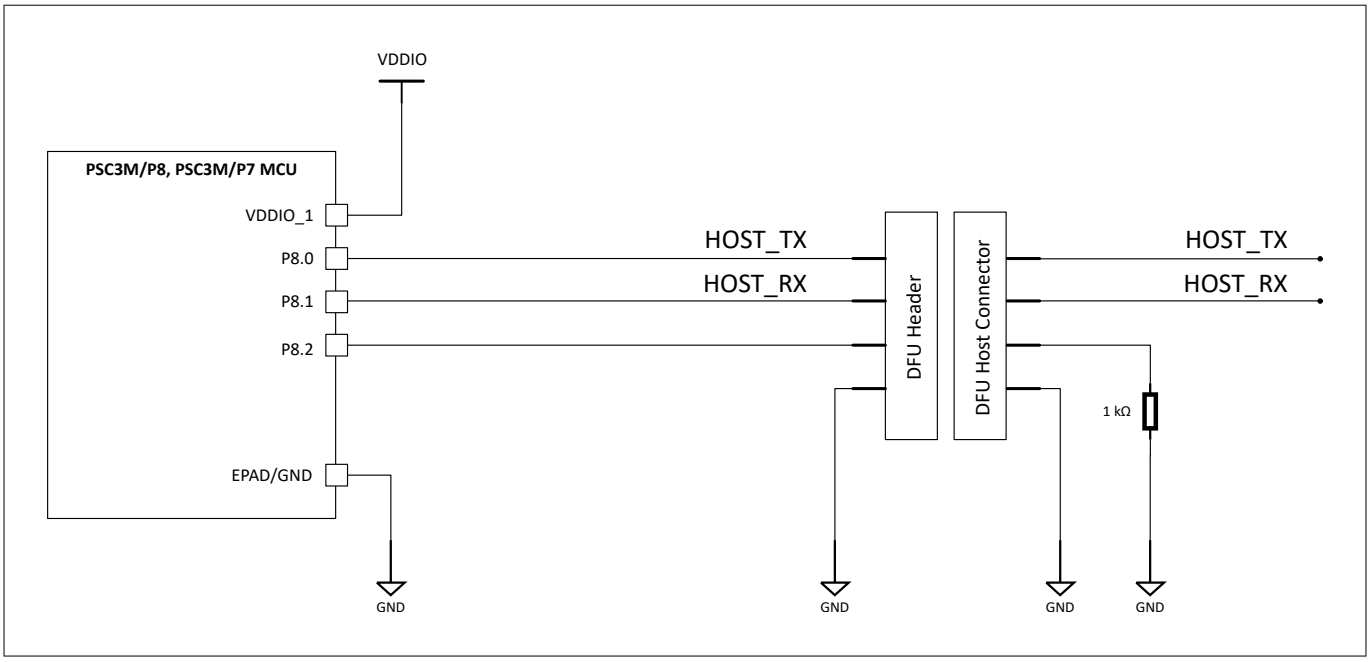


Figure 9 DFU UART connection diagram

***Note**: When the DFU feature is enabled:*

- *During normal operation, the DFU enable pin should not be pulled down or driven $\overline{LOW}$ when the MCU is powered on to avoid entering DFU mode unintentionally*
- *DFU enable pin internal pull-up and pull-down resistors are enabled for a short duration during the power on boot up sequence. If the DFU enable pin is used in the application circuit, ensure that this startup behavior does not cause any malfunction. See the device datasheet for the internal pull-up/pull-down resistor values*
- *DFU enable pin is only used during the boot code execution for DFU entry. It can be used in the application with above considerations*

8 Analog subsystem design

8.1 SAR ADC

The device has up to three 12-bit ADCs with a sampling rate of up to 25 Msps. It features multiple dedicated analog input pins. Some dedicated analog pins have a direct path to dedicated samplers while other dedicated analog/analog capable GPIO pins are connected through multiplexers. See the device datasheet for details.

The direct path for the dedicated analog input pins without multiplexing minimizes parasitic capacitance and internal path resistance. The SAR ADC utilizes a 1.2 V external voltage reference connected to the *VAREF_EXT* pin. Although the device provides an internal 1.2 V reference, it is recommended to connect the *VAREF_EXT* pin to an external precision voltage reference for better accuracy and lower noise.

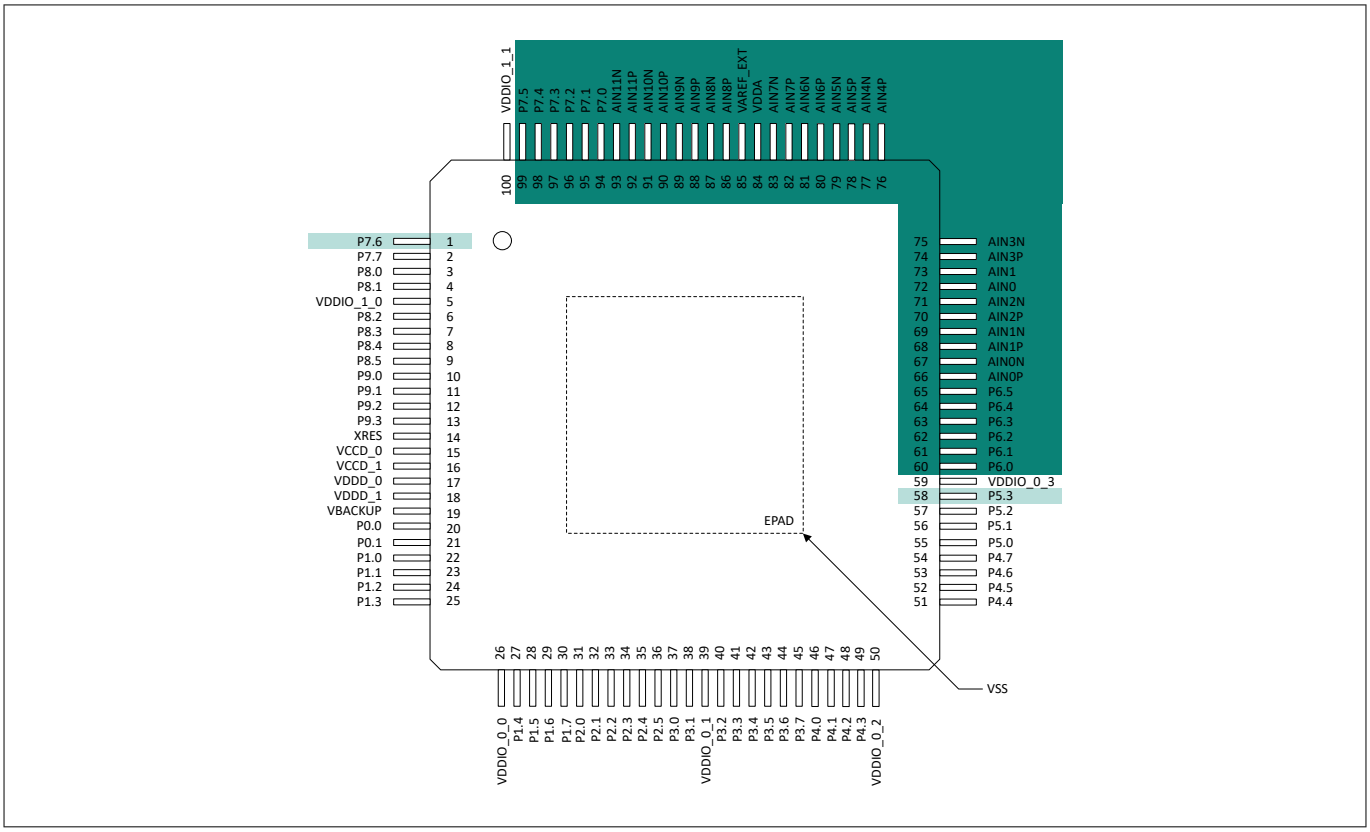


Figure 10 Analog pins in the PSC3M/P8, PSC3M/P7 MCUs (E-LQFP-100 package)

Figure 10 shows that all the dedicated analog, analog capable GPIO, and the analog supply/reference pins are located together in the LQFP-100 package. It is also applicable for other smaller pin count packages. This allows the analog and the digital sections of the design to be segregated on the PCB. While selecting the pin-outs and placing the components on the PCB, ensure that all the analog components are placed on the analog side and all the digital components are placed on the digital side of the MCU. P5.3 is only available in 100-pin and 80-pin packages while P7.6 is only available in 100-pin package, which can be used as additional analog inputs if required.

8.2 Active comparators

See the device datasheet for information about the pinouts supported for the active comparators.

Analog inputs may be impacted by digital noise, which must be considered during pin assignment and board design.

8.3 Low-power comparators

In addition to the active comparators, the device features two low-power comparators that can operate even in Deep Sleep and Hibernate power modes. These comparators can be used to wake up the MCU. Both the inverting and non-inverting comparator inputs are available on fixed GPIO pins. See the device datasheet for the low-power comparator input pin mapping. Both the low-power comparators can compare two external voltages or compare an external voltage with an internal reference voltage.

9 PCB layout recommendations

There are many classic techniques for designing PCBs for low noise and EMC. A few of these techniques are covered in the subsequent subsections.

9.1 General PCB design guidelines

- **Multiple layers:** Although they are more expensive, it is best to use a multilayer PCB with separate layers dedicated to the VSS and VDD supplies. This gives good decoupling and shielding effects. Separate fills on these layers should be provided for VSSA, VSSD, VDDA, VDDIO, and VDDD. To reduce cost, a two-layer or even a single-layer PCB can be used. In that case, you must have a good layout for all VSS and VDD
- **Ground and power supply:** There should be a single point for gathering all ground returns. Avoid ground loops, or minimize their surface area. All component-free surfaces of the PCB should be filled with additional grounding to create a shield, especially when using two-layer or single-layer PCBs. The power supply should be close to the ground line to minimize the area of the supply loop. The supply loop can act as an antenna and can be a major emitter or receiver of EMI
- **Decoupling:** The standard decoupler for power domains is a 10 µF capacitor. Supplementary 0.1 µF capacitors should be placed as close as possible to the VSS and VDD pins of the device to reduce high-frequency power supply ripple. Generally, you should decouple all sensitive or noisy signals to improve the EMC performance. Decoupling can be both capacitive and inductive
- **Component position:** Separate the circuits on the PCB according to their EMI contribution. This will help reduce cross-coupling on the PCB. For example, separate noisy high-current circuits, low-voltage circuits, and digital components. If an external switching regulator is used to generate the MCU supply, the decoupling capacitors and the inductor (buck inductor) should be placed as close as possible to the external regulator pins with minimum trace resistance
- **Signal routing:** When designing an application, the following areas should be closely observed to improve the EMC performance:
  - Noisy signals; for example, signals with fast transition times
  - Sensitive and high-impedance signals
  - Signals that capture events, such as interrupts and strobe signals

To improve the EMC performance, keep the trace lengths as short as possible and isolate the traces with VSS traces. To avoid crosstalk, do not route them near to or parallel to other noisy and sensitive traces.

9.2 Power supply decoupling

Decoupling capacitors should be placed as close as possible to the supply pins on the same layer as the MCU. If two capacitors are placed on the same supply line, the one with a smaller value should be placed closer followed by the larger value capacitor. The supply decoupling capacitors should be of the X5R or X7R type with a suitable voltage rating as per the operating voltage.

For single or two-layer PCBs, decoupling capacitors for the power supply must be placed within the current flow. The power traces or vias from power and GND planes should first connect to the decoupling capacitor and then the capacitor pads are connected to the MCU supply pins. On the other hand, if there is a direct connection to the MCU power pins which then also goes to the decoupling capacitor, it is not within the current flow path, thereby making it less effective.

For multilayer PCBs with dedicated GND and power planes, place the capacitor close to the MCU pins and connect the capacitor directly to the GND and power planes using vias; it reduces the impedance of the supply planes. Instead of connecting the MCU supply pins to the capacitor pads, connect them to the GND and power planes directly using vias; it provides the minimum possible impedance for the MCU power and GND connections.

9.3 Quartz crystals

Quartz crystals along with the load capacitors should be placed close to the ECO and WCO pins. Using short traces and isolating the two crystal pin traces using a GND trace or grounded copper pour helps minimize stray capacitance. Placing the crystal and the load capacitors on the same layer as the MCU also helps in reducing the stray capacitance.

9.4 PCB design

While it is possible to design a two-layer PCB with good performance, a four-layer or six-layer PCB with dedicated GND and power planes will potentially result in better performance. The final choice may depend on the cost vs. performance constraints.

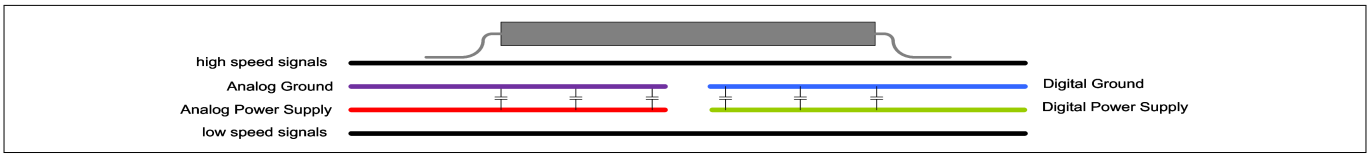


Figure 11 Example of a good PCB layer stack

Figure 11 shows an example of a good PCB layer stack. Segregating the analog and digital GND/power planes can help minimize noise propagation from the digital domains into the analog side. The MCU EPAD ground can be made the star ground point where the two ground planes meet. In few cases, using a single GND plane while ensuring that the digital and analog components are placed according to the respective MCU sections.

9.5 Component placement

Component should be segregated and placed as per their respective sections and proximity to the MCU pins to avoid crossing of signals as far as possible. Analog and high-impedance paths are more prone to noise and should be placed away from high-speed/high-current traces. The flexibility offered by the MCU alternate function mapping and extended routing capabilities using the high-speed I/O matrix (HSIOM) enables further optimization of component placement. For example, it is possible to bring any TCPWM output/complementary output signals to any MCU I/O pin.

9.6 Signal routing

If only a two-layer PCB is used, one layer can be used for routing traces vertically while the other layer can be used to route traces horizontally. This can minimize crosstalk and also minimizes the possibility of creating discontinuity in the GND planes.

For four-layer or six-layer PCBs, use dedicated layers for signal routing (analog and high-speed digital on the same layer as the MCU as far as possible and auxiliary signals on other layers).

9.7 Analog signals

Analog signals are more prone to noise compared to digital signals. The impact of noise may manifest as unwanted variations in the converted ADC value or lead to false triggering in case of comparator inputs. Routing for critical analog signals should be prioritized. Try to route the analog signals away from high speed and high current switching signal.

9.8 Discrete RC filters

RC low-pass filters can be added to the ADC inputs to reduce RF noise. The RC time constant should be selected as per the expected signal bandwidth. The RC should be placed close to the analog input pin with the capacitor placed closer to the pin followed by the resistor. The signal trace is connected to the far end of the resistor (away from the MCU pin). The closer resistor pad (to the MCU pin) is connected to the capacitor pad and then the capacitor pad trace is connected to the analog input pin.

10 Schematic checklist

The following checklists help ensure that the important design elements are not overlooked. The answer to each of the entries should be Yes (Y), No (N), or Not Applicable (NA). This checklist does not guarantee 100% coverage of all use cases/scenarios. However, it can be used as a starting point and customized/enhanced further as per individual design requirements.

10.1 Power checklist

Table 8 Power checklist

Item	Y/N/NA	Remarks
Are the power pin connections made in accordance with Power pin connections?		
Are decoupling capacitors placed as per recommended values on VDDD, VDDIO, and VDDA?		
Are the voltages (including ripples) at the VDDD and VDDA pins in the range of 1.71 V to 3.63 V?		
Is the VCCD pin connected to a 4.7 µF capacitor?		
Is the VBACKUP pin connected to an appropriate supply (VDDD or the 1.4 V to 3.63 V source)?		

10.2 Clocking checklist

Table 9 Clocking checklist

Item	Y/N/NA	Remarks
Is the external clock connected to the *EXT_CLK* pin?		
Is the external clock's frequency less than or equal to 100 MHz (including tolerance)?		
Is the external crystal connected to the ECO pins for ECO operation (4 MHz to 35 MHz)? Are the ECO load capacitors connected?		
Is the 32.768 kHz crystal connected to the WCO for RTC operation? Are the WCO load capacitors connected?		

10.3 Reset checklist

Table 10 Reset checklist

Item	Y/N/NA	Remarks
Is the reset pin connection made in accordance with Reset pin (XRES)?		
Is the reset button connected between XRES and GND?		

10.4 Programming and debugging checklist

Table 11 Programming and debugging checklist

Item	Y/N/NA	Remarks
Are SWD signals connected as described in Serial Wire Debug (SWD)?		
Are JTAG signals connected as described in JTAG?		
Are ETM signals connected as described in Embedded Trace Macrocell (ETM)?		
If DFU is intended to be used in the application, are DFU signals connected as described in Device Firmware Update (DFU)?		
DFU enable pin constrains described in Notes are taken into account?		

10.5 GPIO pins checklist

Table 12 GPIO pins checklist

Item	Y/N/NA	Remarks
Is the assignment of your GPIO pins done in the sequence described in I/O pin selection?		

10.6 SCB and CAN checklist

Table 13 SCB and CAN checklist

Item	Y/N/NA	Remarks
Is the assignment of the SCB's fixed pins in accordance with the device datasheet for the following SCBs:		
SCB0?		
SCB1?		
SCB2?		
SCB3?		
SCB4?		
SCB5?		
SCB6?		
Is the assignment of the CAN fixed pins in accordance with the device datasheet?		

10.7 ADC checklist

Table 14 ADC checklist

Item	Y/N/NA	Remarks
Is the *VAREF_EXT* pin connected externally to a 1.2 V source/precision reference voltage generator?		
Is the *VAREF_EXT* pin connected to a 1 µF capacitor?		
Is the connection to ADC analog input pins done as per the device datasheet specified pinout?		

11 Summary

The PSC3M/P8, PSC3M/P7 devices provide a flexible solution for designing digital and analog applications including, but not limited to, real-time control applications. This application note documents the considerations that need to be considered when building a hardware system around these devices.

References

[1] Infineon Technologies AG: *002-39793: PSOC™ Control C3 - PSC3P7xx, PSC3M7xx, PSC3P8xx, PSC3M8xx*; Available online

[2] Infineon Technologies AG: *002-42141: PSOC™ Control C3 (PSC3P7xx, PSC3M7xx, PSC3P8xx, PSC3M8xx) architecture reference manual*; Available online

***Note**: For more documents related to PSC3M/P8, PSC3M/P7 MCUs, see PSOC™ Control C3 Performance Line webpage.*

Revision history

Document revision	Date	Description of changes
**	2026-04-01	Initial release
*A	2026-09-18	Release to web

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