Product Qualification Report (PQR)

SmartLEWIS™ RX+ TDA5240

Package: PG0-TSSOP-28

All reliability stress tests according to AEC Q100 rev. H (Grade 1) are assessed as PASS. The data outlined in this document may reference existing qualification results of similar products.

Table 1 Reliability stress tests.

#	Test Description	Abbr.	Condition	Duration	Min. # of Lots × Sample Size	Result
Test Group A – Accelerated Environment Stress Tests						
A1	**Preconditioning** *JEDEC JESD22-A113, J-STD-20 (MSL)*	PC	MSL 3	3 × reflow 260°C	before A2, A3, A4	pass
A2	**Temperature Humidity Bias** *JEDEC JESD22-A101*	THB	85°C 85% RH Vcc = 5,5 V	1000 h	3 x 77	pass
A3	**Autoclave** *JEDEC JESD22-A102*	AC	121°C 100% RH	264 h	3 × 77	pass
A4	**Temperature Cycling** *JEDEC JESD22-A104*	TC	-55°C to 150°C	1000×	3 × 77	pass
A6	**High Temperature Storage Life** *JEDEC JESD22-A103*	HTSL	125°C	1000 h	1 × 45	pass
Test Group B – Accelerated Lifetime Simulation Tests						
B1	**High Temperature Operating Life** *JEDEC JESD22-A108*	HTOL	125°C Vcc max	1000 h	3 × 77	pass

#	Test Description	Abbr.	Comment	Result
Test Group C – Package Assembly Integrity Tests				
C1	**Wire Bond Shear** *AEC Q100-001, AEC Q003*	WBS	covered by package platform qualification and production monitoring	pass
C2	**Wire Bond Pull** *MIL-STD883 Method 2011, AEC Q003*	WBP	covered by package platform qualification and production monitoring	pass
C3	**Solderability** *JEDEC J-STD-002*	SD	covered by package platform qualification and production monitoring	pass
C4	**Physical Dimensions** *JEDEC JESD22-B100 and AEC Q003*	PD	covered by package platform qualification and production monitoring	pass
C5	**Solder Ball Shear** *AEC Q100-010, AEC Q003*	SBS	for solder Ball Surface Mount Package only	n.a.
C6	**Lead Integrity** *JEDEC JESD22-B105*	LI	for through-hole devices only	n.a.
C7	**Bump Shear Test** *JEDEC JESD22-B117, AEC-Q003*	BST	for flip-chip technology only	n.a.
Test Group D – Die Fabrication Reliability Tests				
Die Fabrication Reliability Tests like EM, TDDB, HCI, BTI, SM are covered by wafer technology qualification				pass
Test Group E – Electrical Verification Tests				
E1	**Pre- and Post-Stress Function Parameter**	TEST	performed for all qualification parts	pass
E2	**ESD Human Body Model** *AEC Q100-002*	ESD HBM	Class 2 (2000 V to < 4000 V)	pass

#	Test Description	Abbr.	Comment	Result
E3	**ESD Charged Device Model**[1)] *AEC Q100-011*	ESD CDM	Class C2a (500 V to < 750 V, corner pins = 750 V)	pass
E4	**Latch-Up** *AEC Q100-004*	LU	Class II	pass
E5	**Electrical Distributions** *AEC Q100-009, AEC Q003*	ED	test at room, hot, cold temperature	pass
E6	**Fault Grading** *AEC Q100-007*	FG	implemented in production test	pass
E10	**Short Circuit Characterization** *AEC Q100-012*	SC	for smart power devices only	n.a.
E12	**Lead (Pb) Free** *AEC Q005*	LF	covered by package platform qualification	pass
Test Group F – Defect Screening Tests				
F1	**Process Average Testing** *AEC Q001*	PAT	implemented in production test	pass
F2	**Statistical Bin / Yield Analysis** *AEC Q002*	SBA	implemented in production test	pass
Test group G – cavity package integrity tests				
Cavity package integrity tests like MS, VFV, CA, GFL, DROP, LT, DS, IWV apply for hermetic packages only				n.a.

[1)] voltage refers to test condition (TC) mentioned in the standard

For further information and documentation please refer to the product homepage:
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