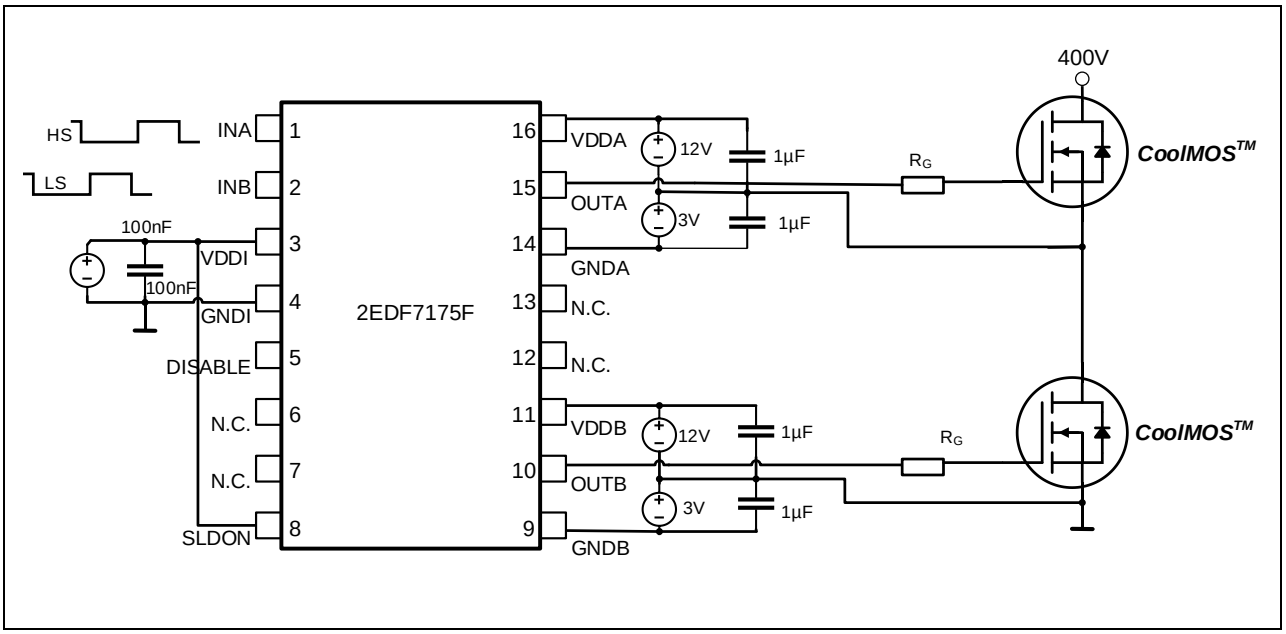
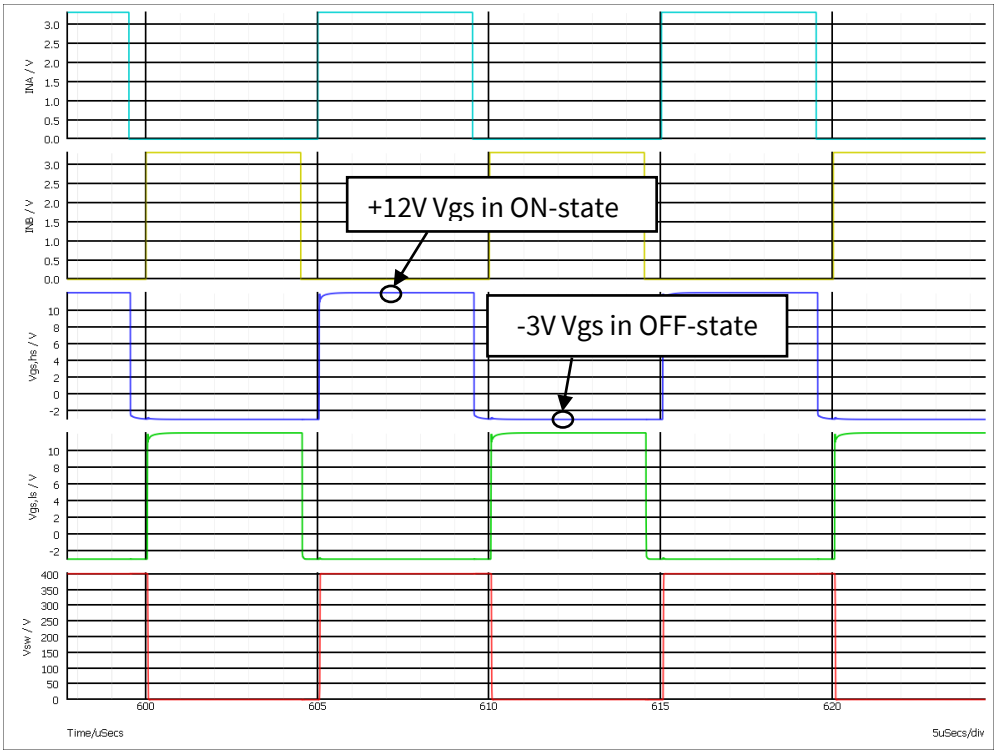
2EDi does not accept a negative voltage (negative when referred to the driven MOSFET source) on the output channels grounds (GNDA, GNDB). However, if the goal is to generate a bipolar gate voltage (to avoid for example Miller return-on) you can do it also with the 2EDi products and with non-negative voltage on pins GNDA, GNDB; just consider one among the three proposed methods below.

Method 1



For each output channel, use two split bypass capacitors with the middle node connected to the source of the driving MOSFET. Supply each capacitance with an isolated aux supply; the two voltage sources must be selected according to the gate-to-source voltage (Vgs) levels you want to get in ON and OFF state (for example 12V and -3V as in figure).

The upper capacitance supplies current during turn-on and the lower capacitance supplies current during turn-off. With this simple circuit the driver output GNDA, GNDB are still supplied with a non-negative voltage (referred to the driven MOSFET source); however, a bipolar Vgs (+12V, -3V) is obtained on the MOSFET as visible in the simulation results (0Ω R_G, IPA60R280C6 CoolMOS™) below.

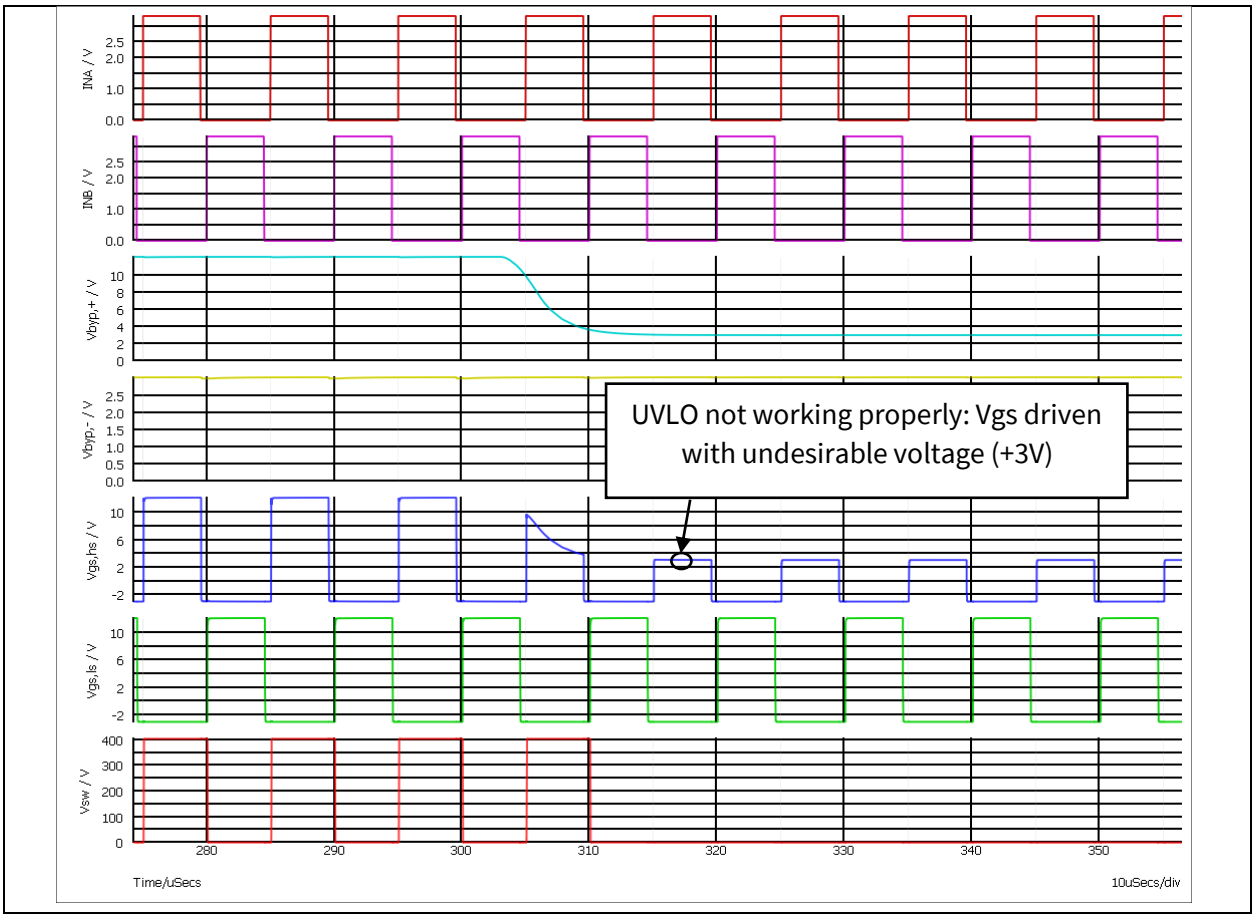


Same value for the two capacitors is recommended to get the same ripple on both positive and negative supply; the ripple is, in fact, caused by the driving charge and this is the same in both turn-on and turn-off. If you care more about the accuracy of the positive Vgs you can select a bigger value for the upper capacitor.

This method requires two isolated auxiliary supplies for each output channel and, then, four isolated auxiliary supplies to drive an half-bridge. It is, then, a valid option only in systems integrating, e.g., flyback auxiliary circuits; in this case, the different auxiliary voltages can be just obtained playing with the windings ratio of the output coils.

The limitation of this method is the shift in the UVLO level functionality. A 4V UVLO is integrated in the 2EDFx to block MOSFET driving with Vgs below 4V; purpose is avoiding that the MOSFET runs in linear region with consequent high thermal stress. The UVLO level refers to the voltage difference (VDDA–GNDA) or (VDDB-GNDB).

In this circuit, only part of the overall driver supply (12V) is replicated on the positive Vgs level. As consequence, if the upper auxiliary source drops (from 12V to 3V e.g.) with the lower auxiliary supply constant (3V e.g.) the driver does not react (see simulation result below) since the voltage VDDA-GNDA (3V+3V) is still above the 4V UVLO level; the MOSFET is, then, driven with undesirable Vgs voltage (3V in this example) in ON-state.

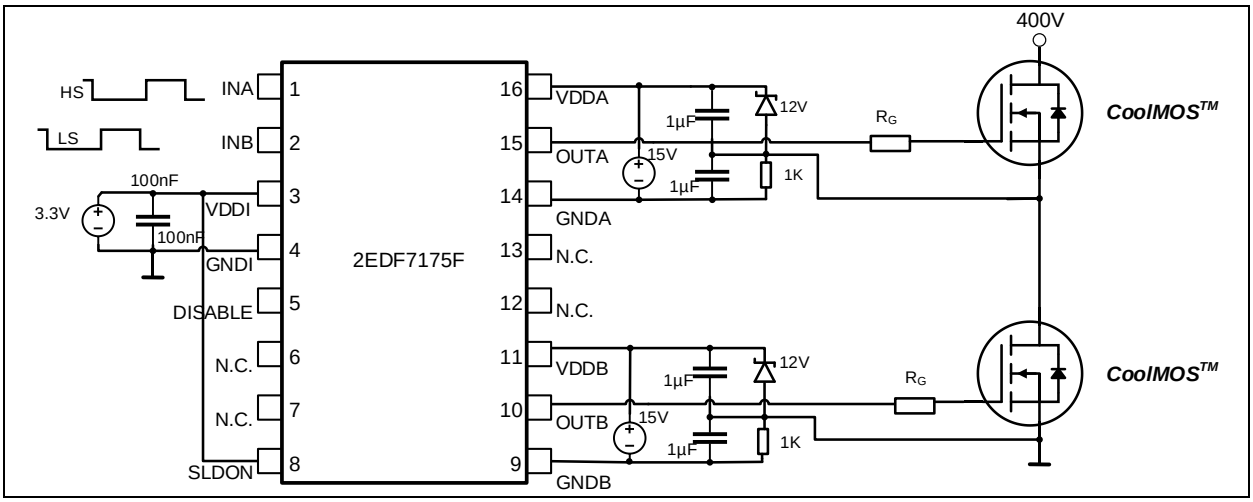


To conclude, with this method the effective UVLO level seen by the MOSFET is shifted; the shift is given by the negative voltage source value (3V in figure). If strong noise is existing in your design, I suggest you to avoid this method and considering the next options.

Method 2

Using method 1 with a single auxiliary supply (in this case the two capacitances must be selected with proper value ratio to give the desired voltages) is not possible since any leakage current (for example the capacitors intrinsic ones) would change the capacitors voltage ratio over the time. You can just simulate this situation adding in series to each capacitance the leakage resistance.

This problem can be solved by adding a Zener diode as below. If the resistance R_Z in series to the Zener diode is properly dimensioned, the Zener diode absorbs any leakage current from the capacitors.



Same value for the capacitance can be selected to guarantee same ripple on the positive and negative supply; the voltage ratio in steady state is just given by the zener diode. In figure a 12V zener diode is used and, with 15V aux supply, steady-state voltages of 12V (V_{Pos}) and 3V (V_{Neg}) establishes on the upper and lower capacitors. The driver then replicates those voltages as positive and negative Vgs on the MOSFET.

The resistance R_Z must be selected to provide enough current to run the Zener diode with 12V voltage; some current margin has to be considered since the Zener diode must also absorb leakage currents.

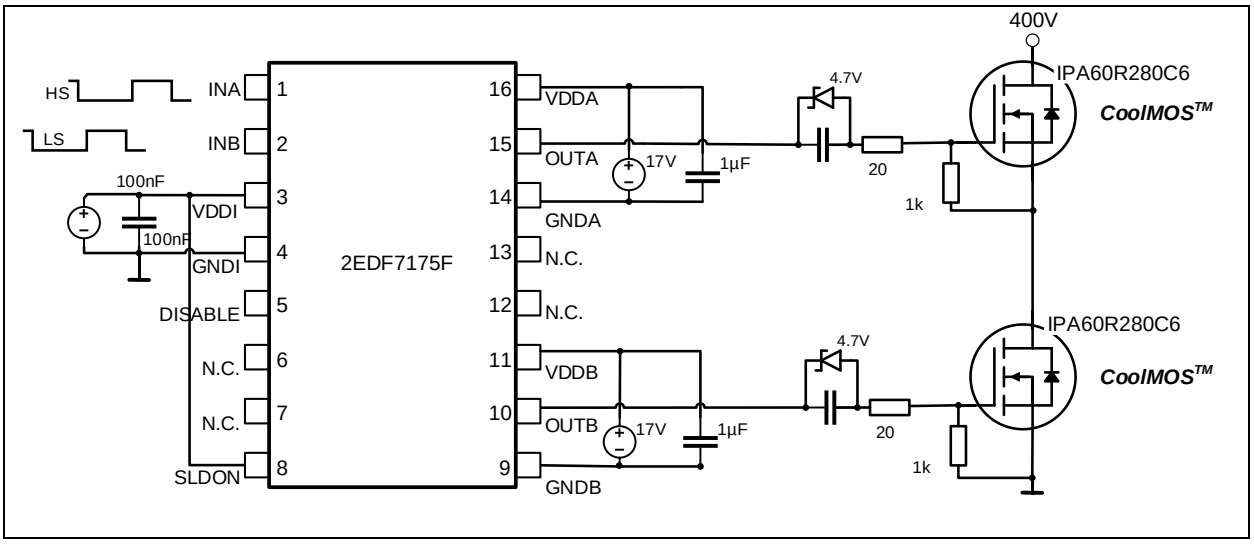
$I_{ZENER} = V_{Neg} / R_Z > I_Z \sim 10\mu A$

Considering some margin, with 3V negative supply, 60kΩ R_Z is a good choice. However, 1 kΩ has been used just to speed up the simulation. I suggest you to use a resistance as close as possible to this value to reduce the static power dissipation on it.

Method 2 does not suffer of UVLO interpretation problems since only one aux supply is used. This solution is very simple, low-cost and compact but bootstrap can not be used.

Method 3

The bigger advantage of this solution is the possibility to use the boostrap in half-bridge driving. However, it requires a proper dimensioning of the gate cap according to the selected MOSFET. Moreover, if negative voltage is needed from the beginning, as in start-up, or in “first pulse condition” (burst-mode) as when using CoolGAN, then method 2 is recommended.



Below you find the simulation result for the reference circuit above.

