Scenario:

Some isolated gate drivers manufacturers specify the time needed from the UVLO to activate after the supply has reached the UVLO threshold; during this time, any PWM on the input is not replicated on the output of the driver. One company is e.g. stating 50us for the UVLO activation and is suggesting to the user to apply the PWMs only after this time. I looked in the 2EDi datasheet but I did not find any similar information. Could you please advice on this?

Solution:

If my understanding is correct, you are interested in the start-up behavior of the driver itself, how long the 2EDi takes to activate after the input or output supply has reached the UVLO turn-on threshold; just for common understanding, let's refer to this interval as "start-up time'' and let's consider the 2EDSx products (with 8V $UVLO_{ON}$, 7V $UVLO_{OFF}$).

You are right; the datasheet does not provide info on start-up time over temperature and production spread. However, internal measurements have been done on a single sample in the following conditions (Cond A and Cond B):

- 3.3V constant INA input on ChA;
- Input-side supply (VDDI) rising and output-side supply (VDDA) fixed at 12V in Cond A;
- Input-side supply (VDDI) fixed at 3.3V and output-side supply (VDDA) rising in Cond B.

The start-up time needed from the driver to react and generate a high-state signal on the output OUTA (according to the input INA) has been measured in both conditions.

For Cond A, the start-up time (measured from the typ. input-side supply $UVLO_{ON}$ threshold of 2.85V) is in the range [5us; 7.5us].

For Cond B, the start-up time (measured from the typ. output supply $UVLO_{ON}$ threshold of 8V) is in the range [2us; 4.5us].

The exact start-up value depends on the supply rising speed/time. For more information, please have a look to the complementary information provided below.

For more information:

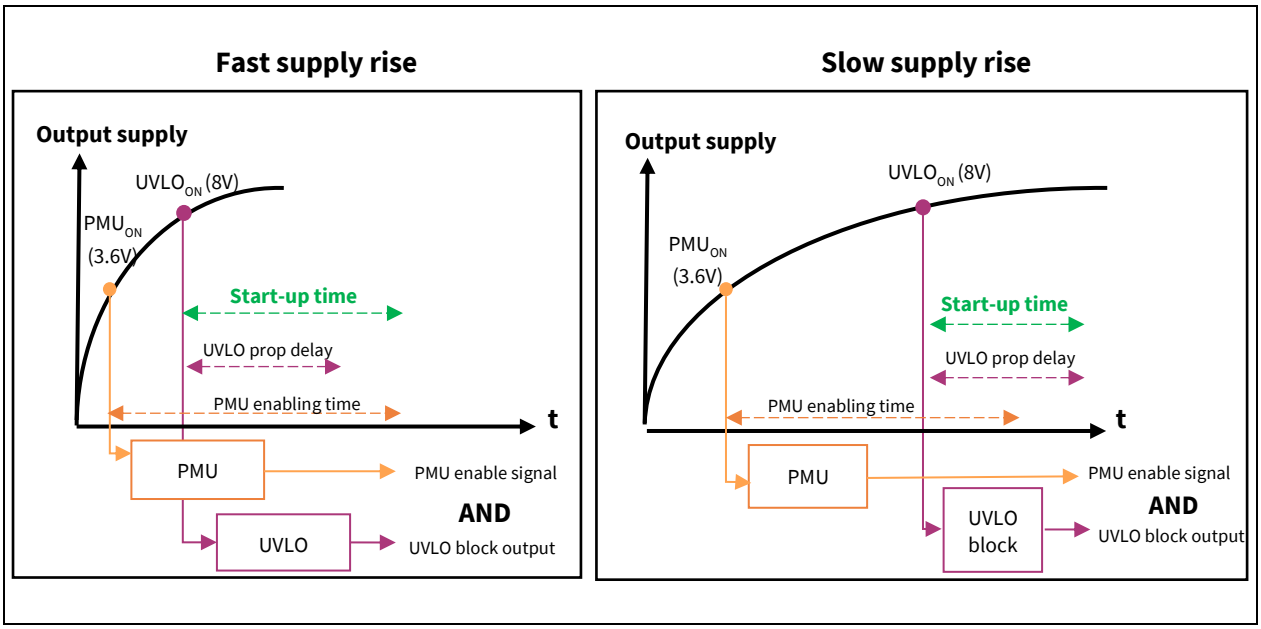
Let's consider CondB for simplicity.

During start-up, the output supply rises from 0V to the end voltage (12V in the example). While rising, it approaches first the PMU (Power Management Unit) activation voltage (PMU_{ON}, 3.6V) and after the UVLO block activation voltage ($UVLO_{ON}$, 8V in datasheet for 2EDS).

After activation, the PMU chain takes a while to provide the "output enable signal" that goes in AND with the UVLO block output. Let's refer to this time as "PMU enabling time".

The UVLO block takes a while to provide the output after it has been activated. In a simplified view, you can just consider the propagation delay of the UVLO block as the delays of a comparator comparing the supply with the $UVLO_{ON}$ threshold.

Since the UVLO block output and the “output enable signal” are in AND, the real time of reaction of the driver depends on the last signal that comes.



The PMU enabling time is ~4us.

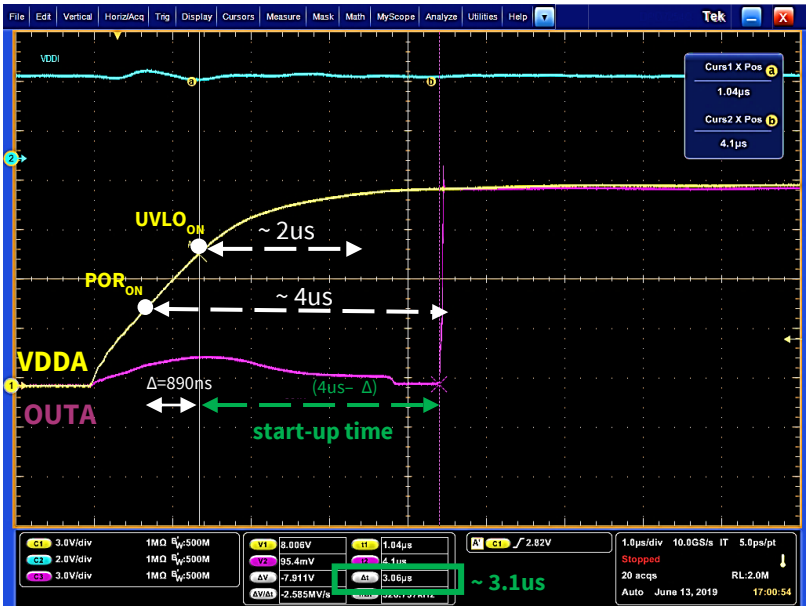
The UVLO block propagation delays is ~2us.

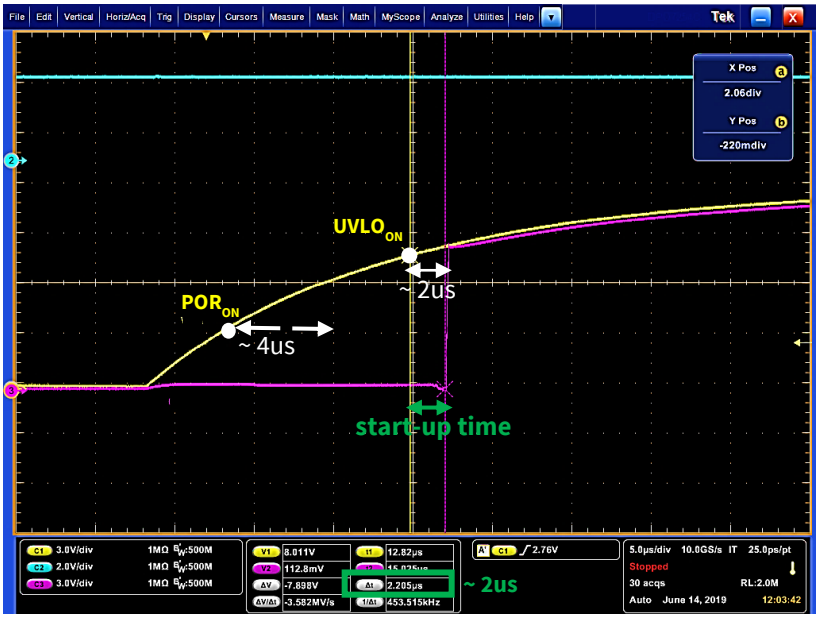
As visible in picture, the total start-up time is dependent on the VDDO rise time and can go from a minimum of 2us (slow supply rising, >us range) to a maximum of 4us (fast supply rising, <us range).

In the 1st case (left end-side picture), when the UVLO block is activated the PMU has already provided the PMU enable signal; the UVLO block propagation delay is, then, completely dominating the driver reaction time.

In the 2nd case (right end-side picture), the timing distance between PUM_{ON} and $UVLO_{ON}$ is very short and the PMU enabling time is completely dominating the driver reaction time.

For all intermediate case, the start-up time just assumes an intermediate value. Below you find two measurements with ~3us and ~15us for the VDDO supply rise time confirming the theory.





Same concept is valid for CondA, just in this case input chip values have to be considered (2.5V PMUON, 2.8 UVLOON, 7.5µs input-chip PMU enabling time, 5µs input-chip UVLO block prop delay).

Start-up time is longer in Cond A mainly because of the “driver configuration reading” phase, which happens in the input chip when the input-side supply has reached the PMUON threshold. During this phase, configuration parameters are read from input chip fuses and stored into the on-chip memory. In Cond B, this operation is not taken in

account (input side-supply fixed and driver reading already concluded when the output-side supply is rising).