

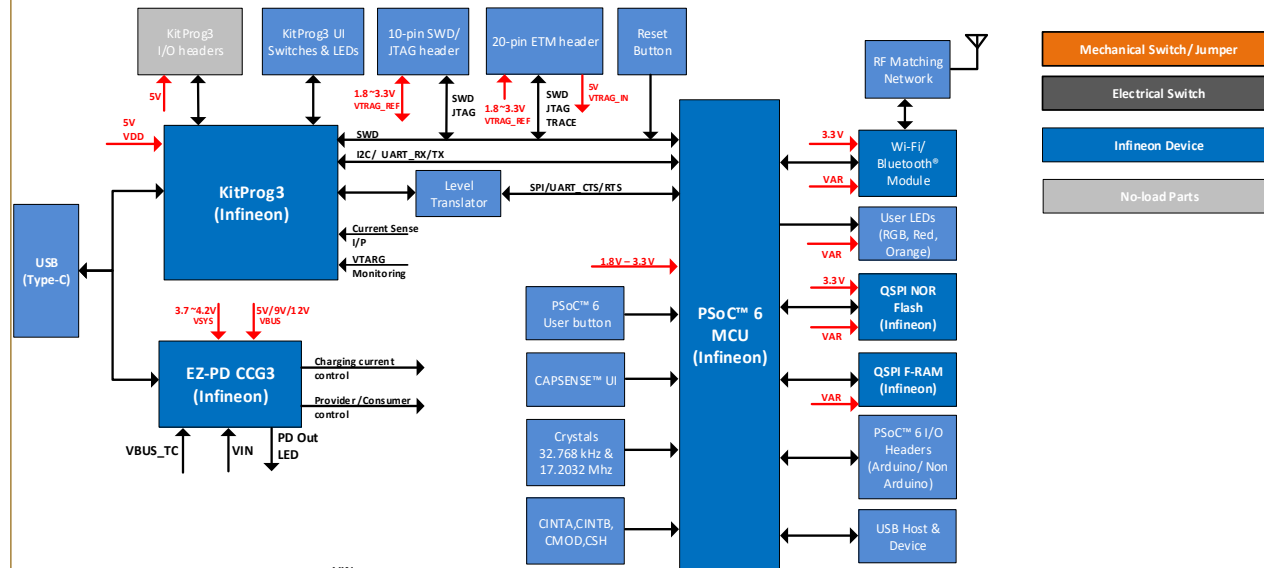
## CY8CKIT-062-WiFi-BT PSoC™ 6 Wi-Fi-Bluetooth® Pioneer Kit

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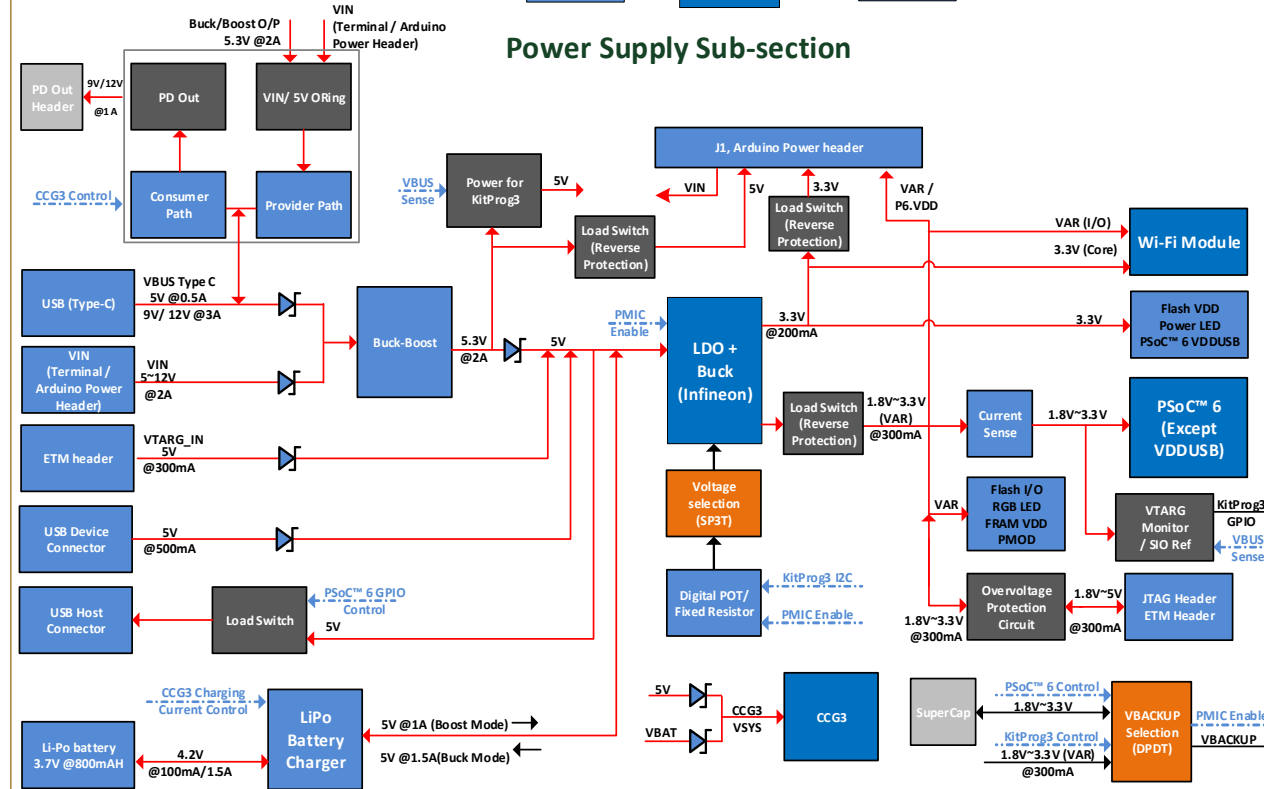
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| PCB             | 600-60435-01 |
| FAB DRW         | 610-60435-01 |
| ASSY DRW        | 620-60435-01 |
| SCH DRW         | 630-60435-01 |

|                                                                                       |                                        |                                                                                            |                            |  |  |
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| <b>Page Title : Title Page</b>                                                        |                                        |                                                                                            |                            |  |  |
| Size<br>A4                                                                            | Document Number<br><b>630-60435-01</b> | Drawn By<br><b>AARA, TAVA</b>                                                              | Approved By<br><b>RKAD</b> |  |  |
| Date:<br>Friday, December 22, 2023                                                    | Sheet<br><b>1</b> of <b>16</b>         |                                                                                            | Rev<br><b>05</b>           |  |  |

# CY8CKIT-062-WiFi-BT Architecture Block Diagram



## Power Supply Sub-section





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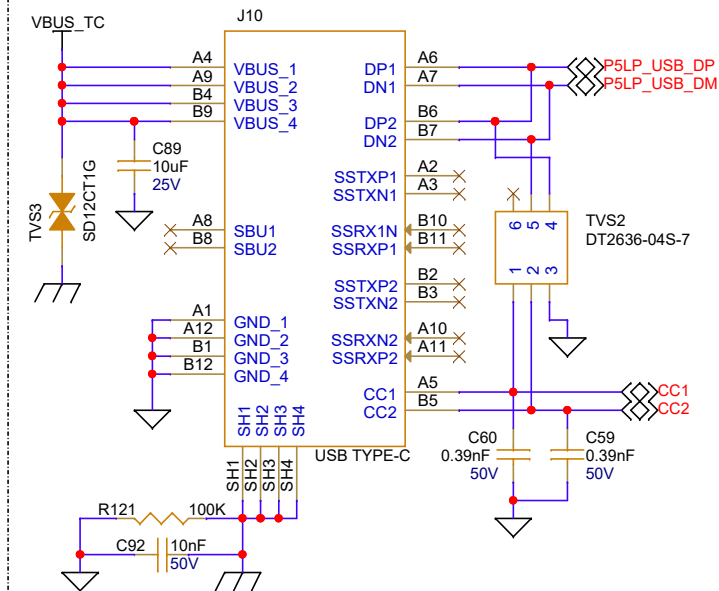
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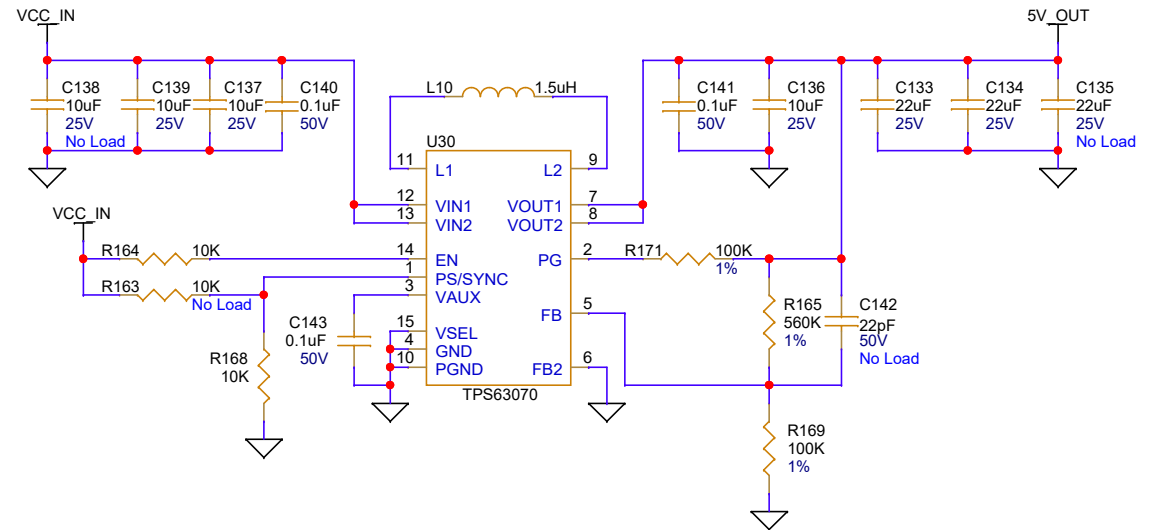
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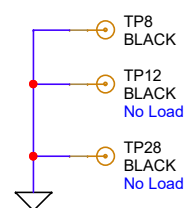
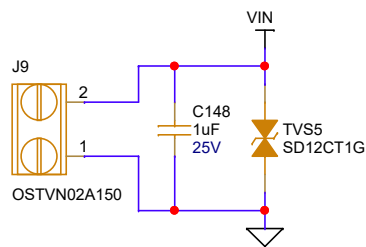
## KitProg3 USB Type-C Connector



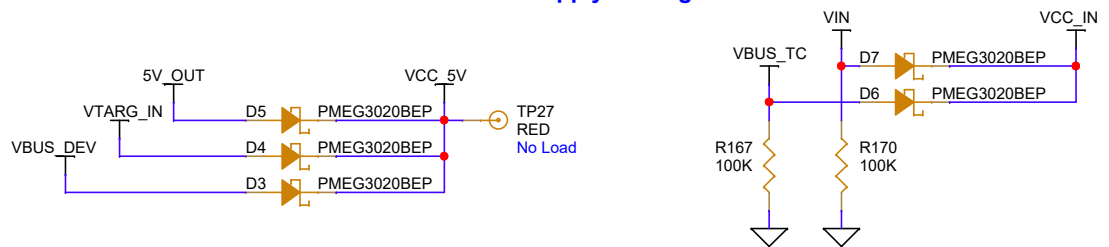
## 5V Buck-Boost Regulator



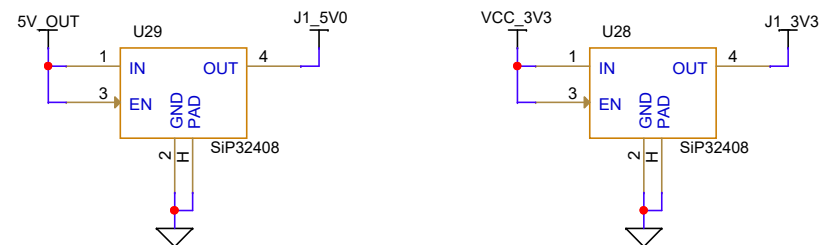
## VIN Header



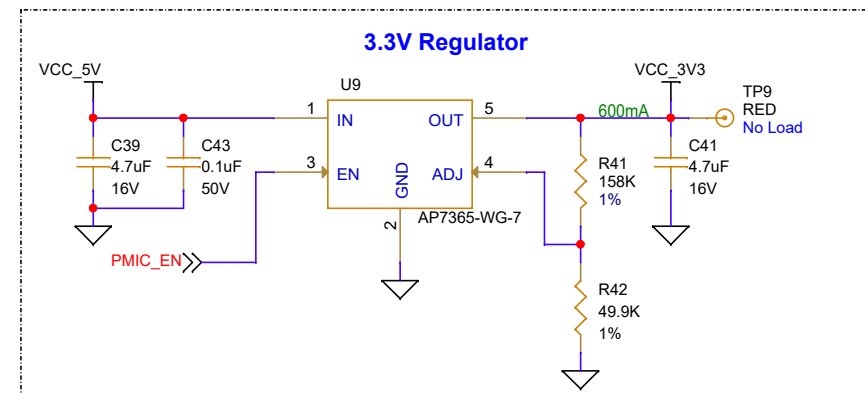
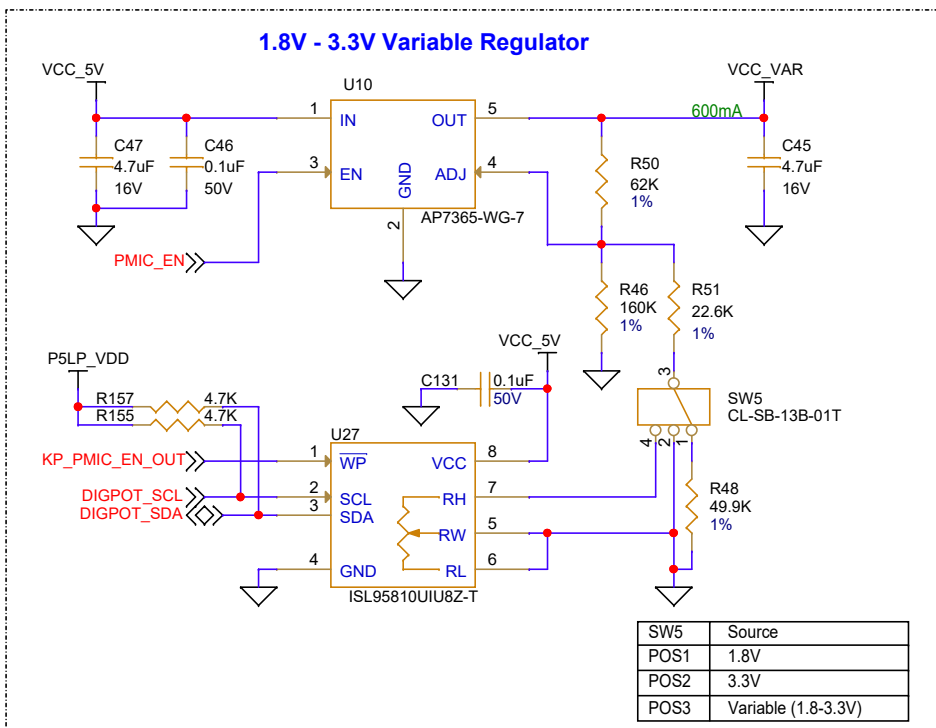
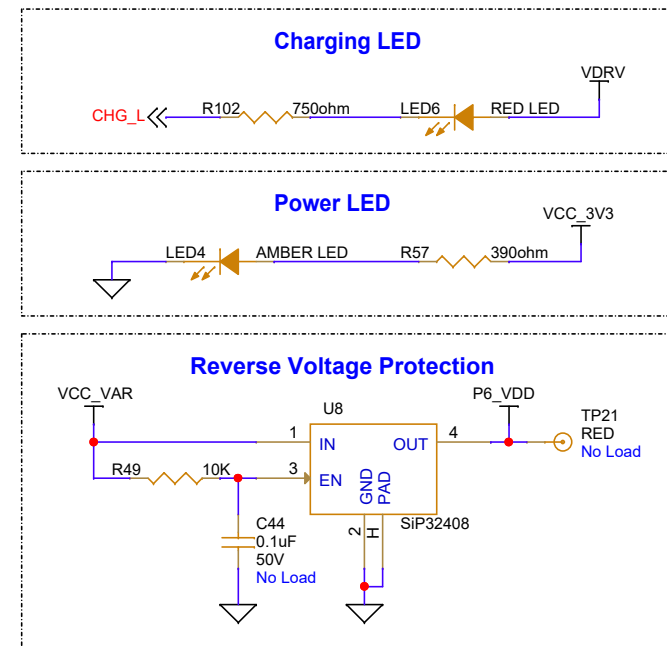
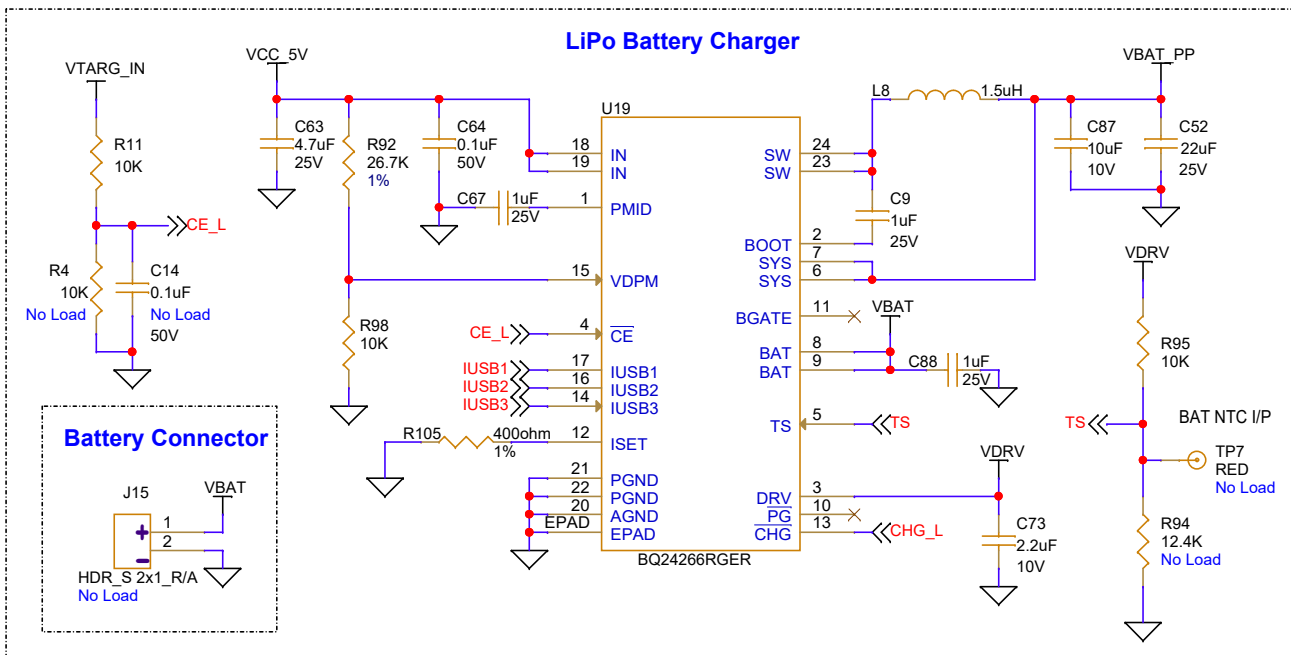
## Power Supply 'OR'ing



## Arduino Header O/P



|                                                                                                                                                                                  |                                        |
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| <b>Page Title : 5V Buck/Boost Regulator</b>                                                                                                                                      |                                        |
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| Drawn By<br><b>AARA, TAVA</b>                                                                                                                                                    | Approved By<br><b>RKAD</b>             |
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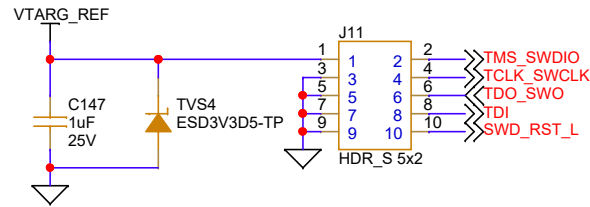
**Page Title : Variable Regulator, Charger**

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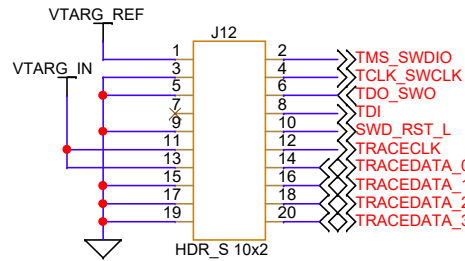
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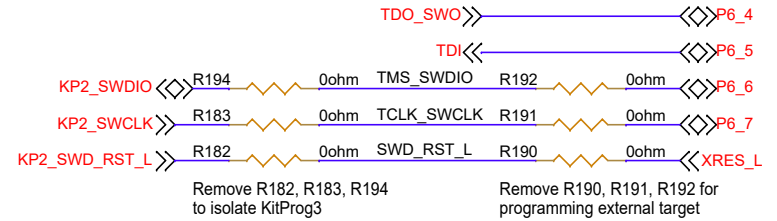
## Target PSoC Program/Debug Header



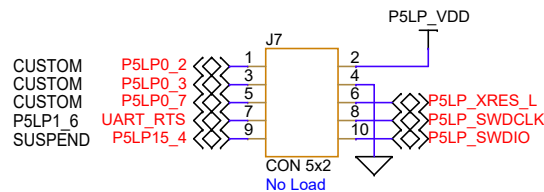
## ETM Header



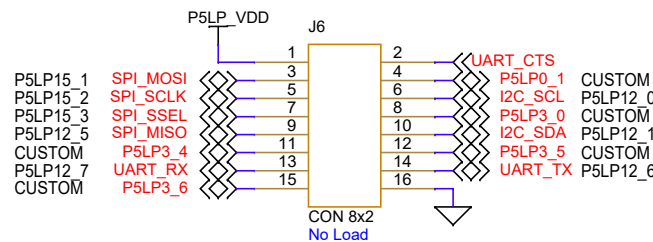
## PSoC 6 SWD/JTAG Interface



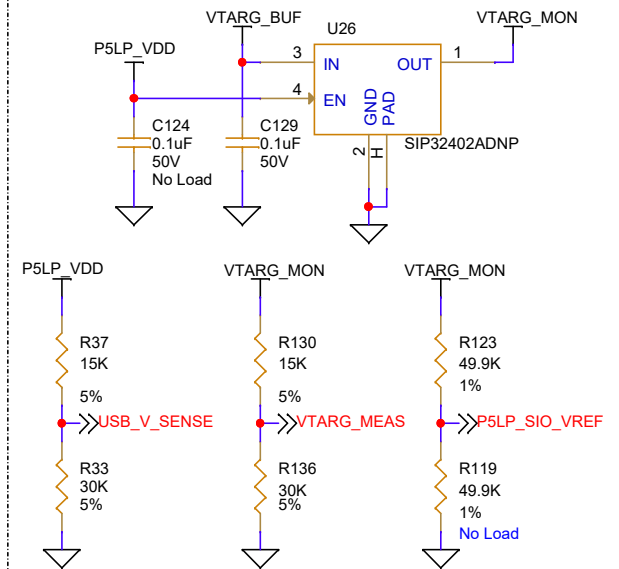
## PSoC 5LP Custom Application Header



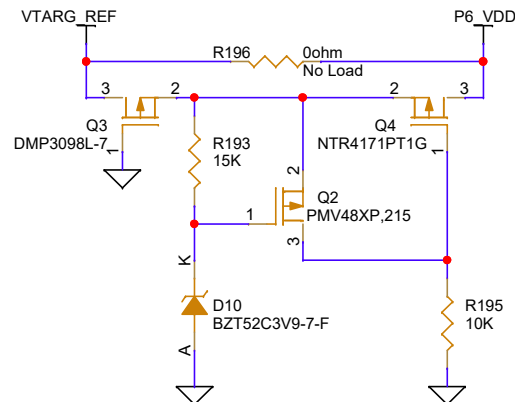
## PSoC 5LP GPIO Expansion Header



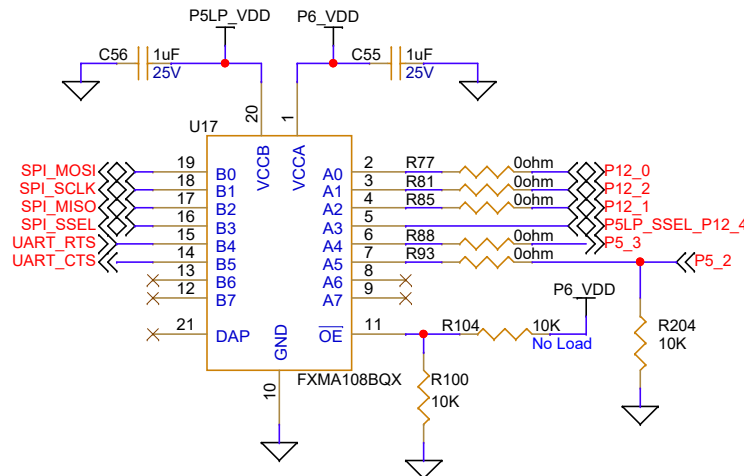
## Voltage Monitoring



## Program/Debug Overvoltage Protection



## Level Translator for SPI and UART flow control



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SCH Title : PSoC™ 6 Wi-Fi Bluetooth® Pioneer Kit

Page Title : Kitprog3 Power & Headers

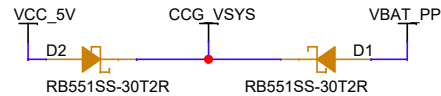
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| A4   | 630-60435-01    | AARA, TAVA | RKAD        | 05  |

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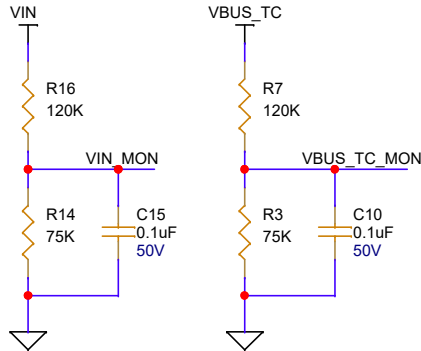
### CCG3 Supply Selection

The diagram illustrates the CCG3 supply selection circuit. It shows a power path starting from VCC\_5V, passing through diode D2 (RB551SS-30T2R) to CCG\_VSYS, and then through diode D1 (RB551SS-30T2R) to VBAT\_PP. The CCG\_VSYS pin is highlighted with a red dot, indicating it is the selected supply source.

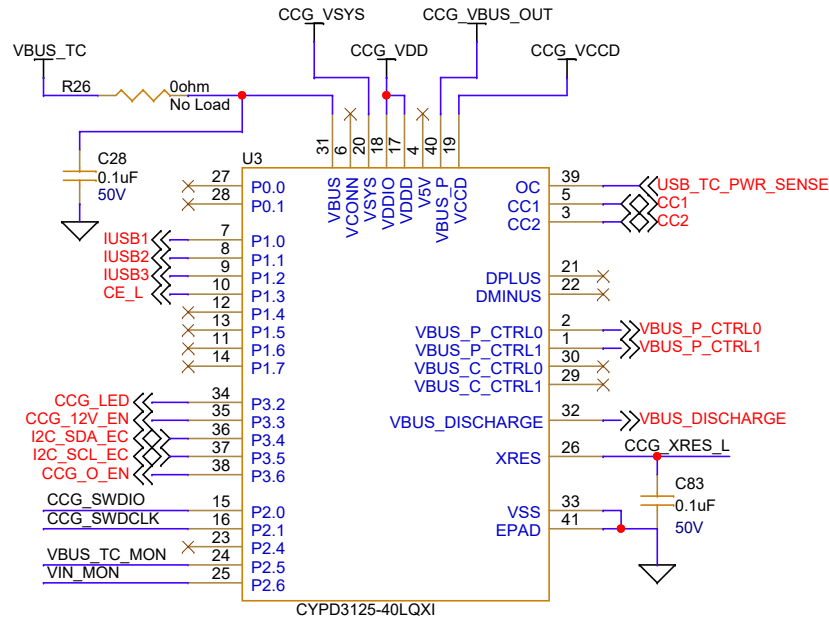
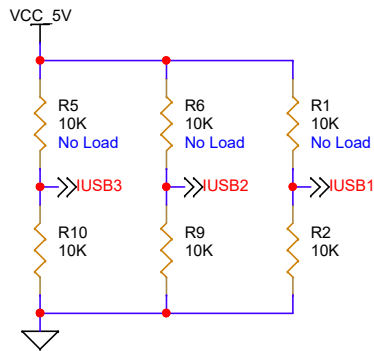


## VBUS & VIN Voltage Monitoring

The diagram illustrates two voltage monitoring circuits. The left circuit monitors VIN through a 120K resistor (R16) to a monitoring point (MON). The right circuit monitors VBUS\_TC through a 120K resistor (R7) to a monitoring point (MON). Both monitoring points are connected to a 75K resistor (R14 or R3) leading to ground and a 0.1uF capacitor (C15 or C10) to ground. The capacitors are rated for 50V.



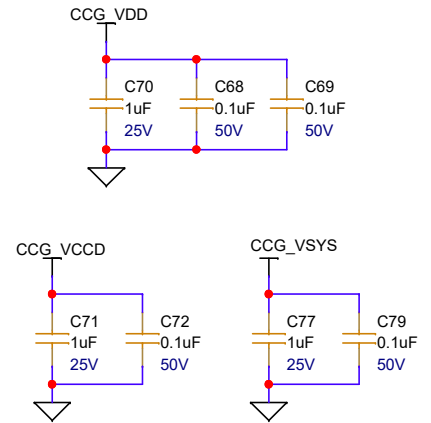
The diagram illustrates a circuit for pulling up the USB D+ lines (USB3, USB2, USB1) to a 5V supply (VCC\_5V) using 10K resistors (R5, R6, R1). Each USB port is connected to ground through a 10K resistor (R10, R9, R2). The USB ports are labeled 'No Load'.



## Decoupling Capacitors

The diagrams illustrate the placement of decoupling capacitors for three different power supply lines:

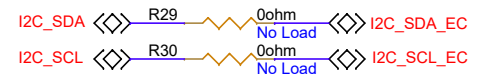
- CCG\_VDD:** A power supply line connected to a series of capacitors (C70, C78, C69) connected to ground. The capacitors are labeled with their values and voltages: C70 (1uF, 25V), C78 (0.1uF, 50V), and C69 (0.1uF, 50V).
- CCG\_VCCD:** A power supply line connected to a series of capacitors (C71, C72) connected to ground. The capacitors are labeled with their values and voltages: C71 (1uF, 25V) and C72 (0.1uF, 50V).
- CCG\_VSYS:** A power supply line connected to a series of capacitors (C77, C79) connected to ground. The capacitors are labeled with their values and voltages: C77 (1uF, 25V) and C79 (0.1uF, 50V).



### I2C Bootloader



The diagram shows the I2C Bootloader circuit. It features two I2C lines, I2C\_SDA and I2C\_SCL, each connected to a pull-up resistor (R29 and R30) and a 0ohm resistor. The I2C\_SDA line is connected to the I2C\_SDA\_EC pin, and the I2C\_SCL line is connected to the I2C\_SCL\_EC pin. The pull-up resistors are labeled R29 and R30, and the 0ohm resistors are labeled 0ohm. The I2C\_SDA line is also labeled I2C\_SDA and the I2C\_SCL line is also labeled I2C\_SCL.



**Output Indication**

CCG\_LED << LED7 <> GREEN\_LED R75 750ohm CCG\_VSYS



## CCG3 Programming

CCG3 Programming

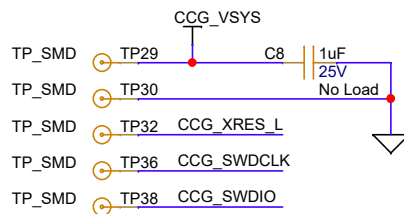
TP\_SMD TP29 CCG\_VSYS

TP\_SMD TP30 1uF 25V No Load

TP\_SMD TP32 CCG\_XRES\_L

TP\_SMD TP36 CCG\_SWDCCLK

TP\_SMD TP38 CCG\_SWDIO



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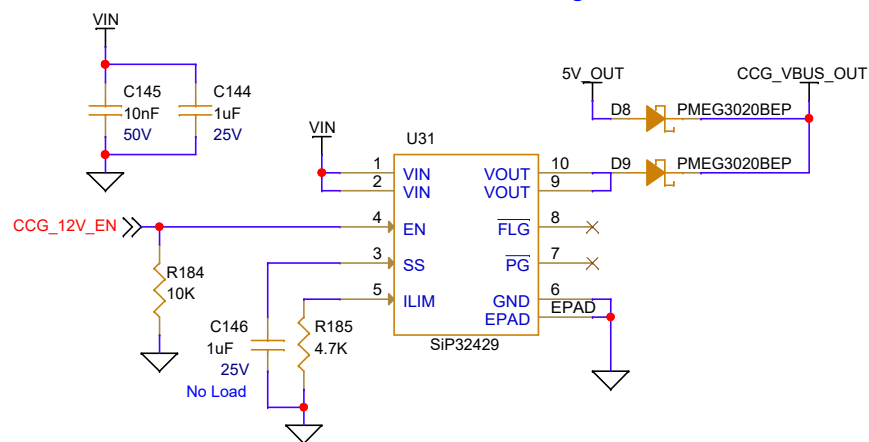
Page Title : Type-C Controller

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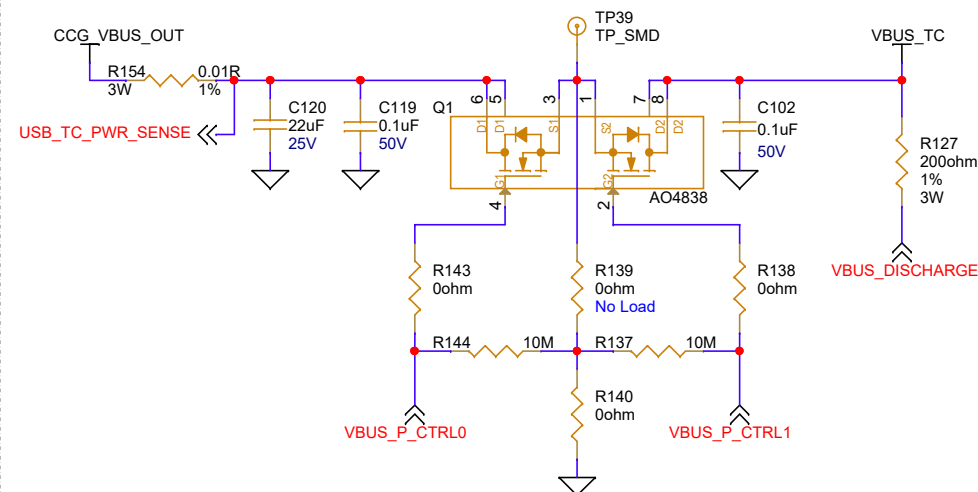
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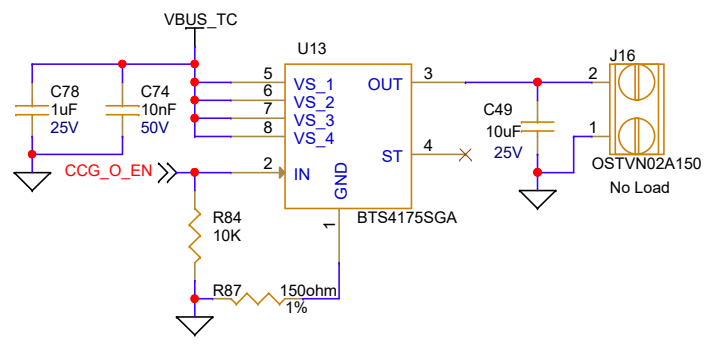
### CCG3 Provider Path 'OR'ing



### VBUS Provider Path



### CCG3 Consumer Path





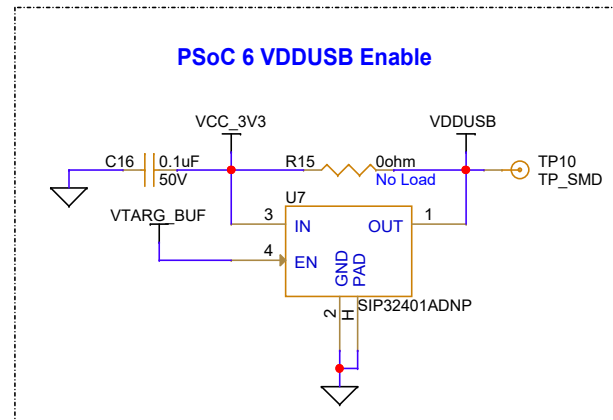
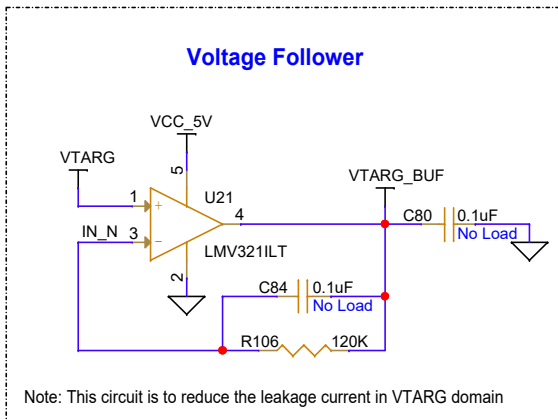
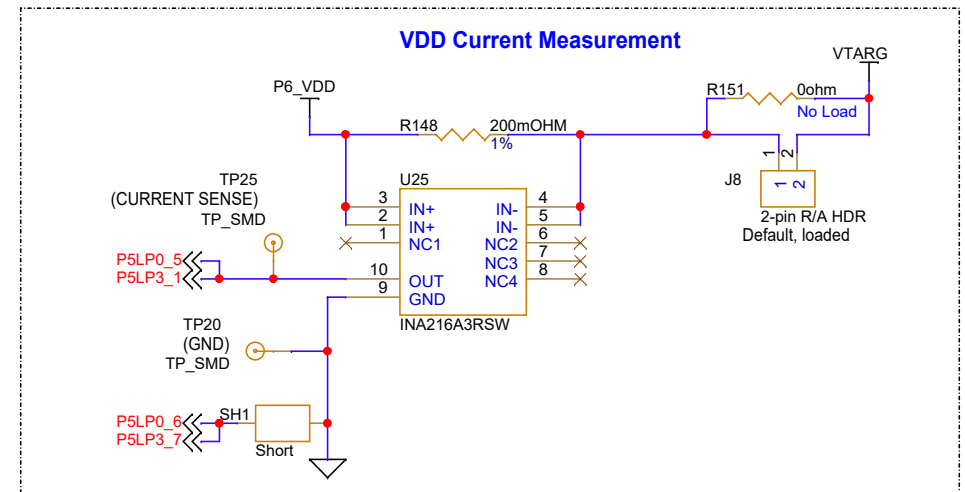
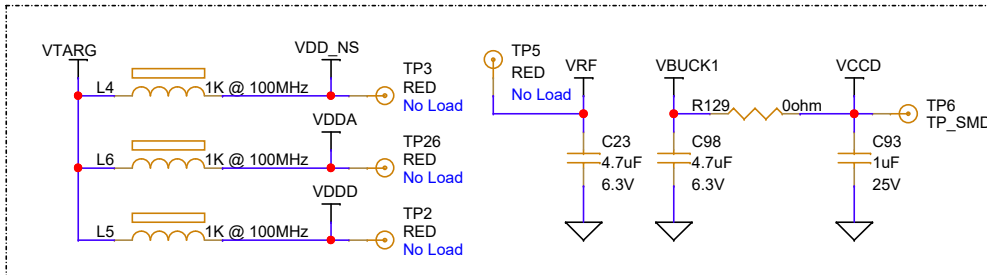
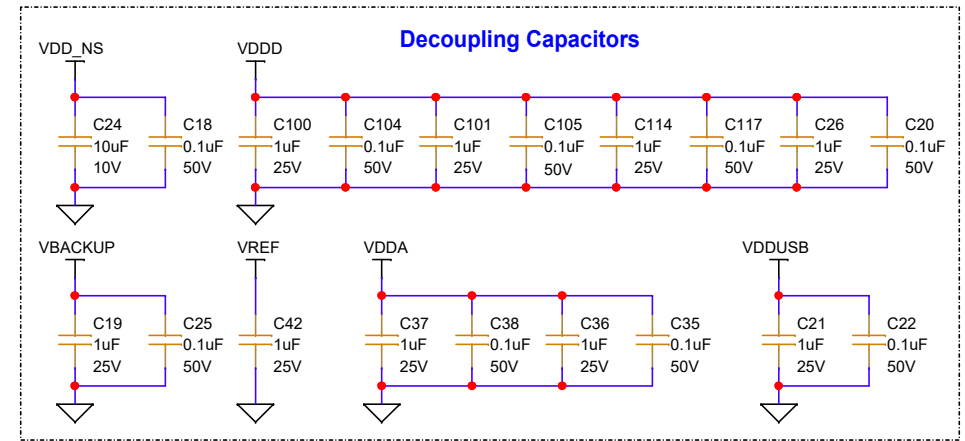
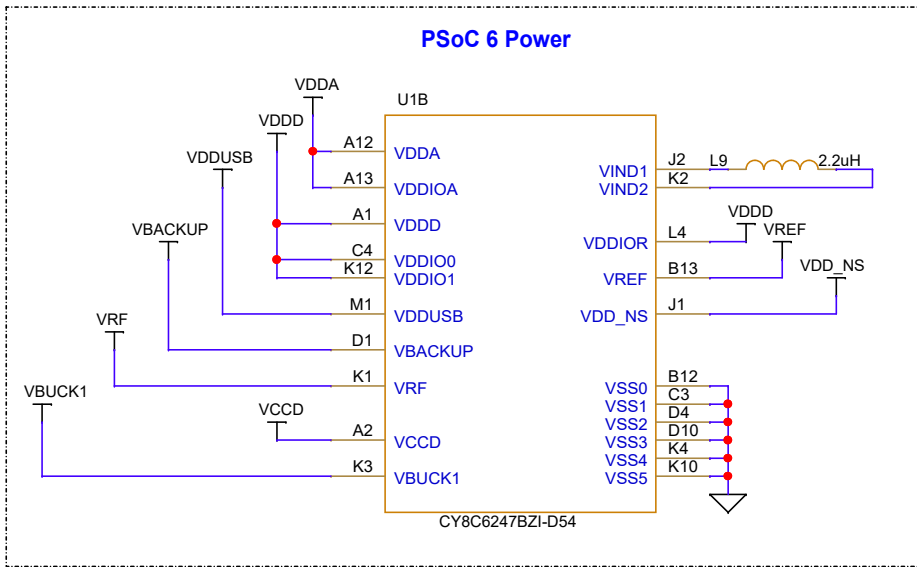
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**Page Title : Type-C Power Path**

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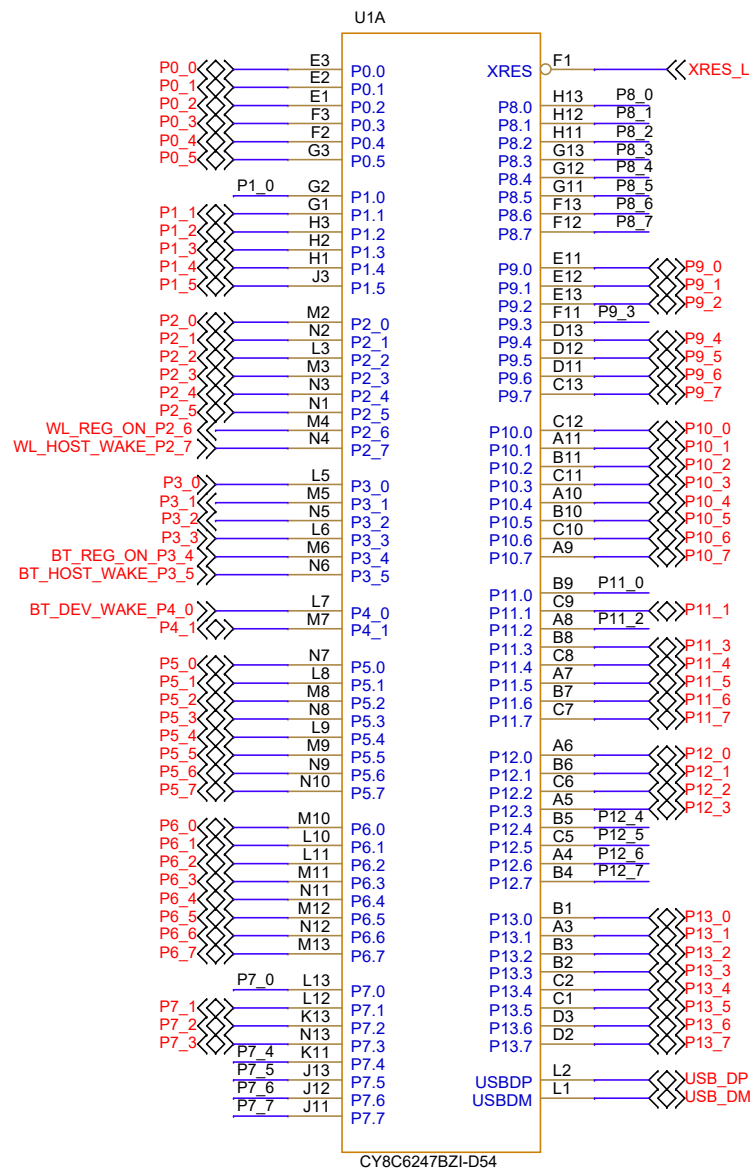
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**Page Title : PSoC 6 Power**

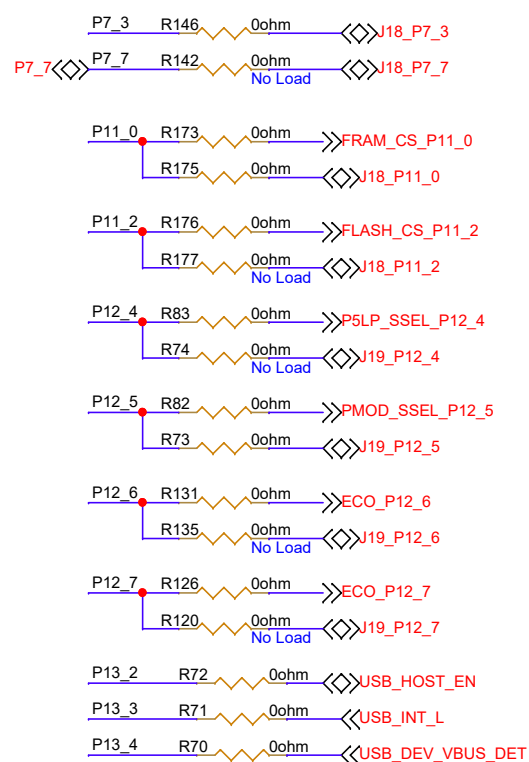
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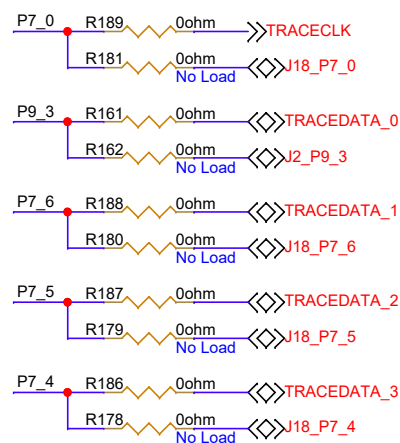
## PSoC 6 Signals



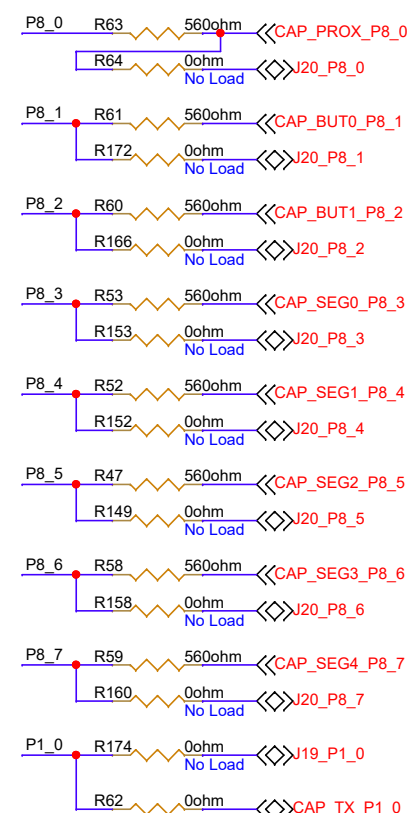
## Additional Multiplexed Pins



## TRACE Multiplexed Pins



## CapSense Multiplexed Pins



WL\_HOST\_WAKE\_P2\_7 >> R133 >> 0ohm >> No Load >> P0\_4

Note: Option for WLAN to wake PSoC 6 from Hibernate



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**Page Title : PSoC 6 Signals**

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### Arduino & Extended Headers

The diagrams illustrate the following connections:

- Diagram 1:** J18 and J1 headers. J18 pins 8-1 are connected to J1 pins 8-1. J1 pin 8 is connected to P6\_VDD. J1 pin 7 is connected to J1\_3V3. J1 pin 6 is connected to SWD\_RST\_L. J1 pin 5 is connected to VIN. J1 pin 4 is connected to J1\_5V0. J1 pin 3 is connected to ground. J1 pin 2 is connected to ground. J1 pin 1 is connected to ground.
- Diagram 2:** J3 and J19 headers. J3 pins 10-1 are connected to J19 pins 10-1. J3 pin 10 is connected to VREF. J3 pin 9 is connected to P6\_0. J3 pin 8 is connected to P6\_1. J3 pin 7 is connected to P12\_2. J3 pin 6 is connected to P12\_1. J3 pin 5 is connected to P12\_0. J3 pin 4 is connected to P12\_3. J3 pin 3 is connected to P13\_1. J3 pin 2 is connected to P13\_0. J3 pin 1 is connected to J19\_P12\_4. J3 pin 10 is connected to J19\_P12\_5. J3 pin 9 is connected to J19\_P12\_6. J3 pin 8 is connected to J19\_P12\_7.
- Diagram 3:** J2 header. J2 pins 1-19 are connected to P10\_0/P10\_1/P10\_2/P10\_3/P10\_4/P10\_5/P10\_6/P6\_2/P6\_3/P13\_6. J2 pins 2-20 are connected to P9\_0/P9\_1/P9\_2/J2\_P9\_3/P9\_4/P9\_5/P9\_6/P9\_7/P13\_7.
- Diagram 4:** J4 and J20 headers. J4 pins 8-1 are connected to J20 pins 8-1. J4 pin 8 is connected to P0\_2. J4 pin 7 is connected to P0\_6. J4 pin 6 is connected to P5\_5. J4 pin 5 is connected to P5\_4. J4 pin 4 is connected to P5\_3. J4 pin 3 is connected to P5\_2. J4 pin 2 is connected to P5\_1. J4 pin 1 is connected to P5\_0. J4 pin 8 is connected to J20\_P8\_7. J4 pin 7 is connected to J20\_P8\_6. J4 pin 6 is connected to J20\_P8\_5. J4 pin 5 is connected to J20\_P8\_4. J4 pin 4 is connected to J20\_P8\_3. J4 pin 3 is connected to J20\_P8\_2. J4 pin 2 is connected to J20\_P8\_1. J4 pin 1 is connected to J20\_P8\_0. J20 pin 8 is connected to J20\_P8\_7. J20 pin 7 is connected to J20\_P8\_6. J20 pin 6 is connected to J20\_P8\_5. J20 pin 5 is connected to J20\_P8\_4. J20 pin 4 is connected to J20\_P8\_3. J20 pin 3 is connected to J20\_P8\_2. J20 pin 2 is connected to J20\_P8\_1. J20 pin 1 is connected to J20\_P8\_0. J21 pin 1 is connected to P4\_1. J21 pin 2 is connected to P5\_7. J21 pin 3 is connected to P10\_7. J21 pin 4 is connected to P13\_2. J21 pin 5 is connected to P13\_3. J21 pin 6 is connected to P13\_4. J21 pin 7 is connected to P13\_5.

The diagram shows a 6-pin header labeled J14. The pins are numbered 1 through 6. The connections are as follows:

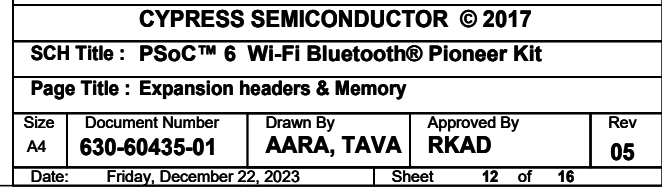
- Pin 1: Connected to P12\_0
- Pin 2: Connected to P12\_1
- Pin 3: Connected to P12\_2
- Pin 4: Connected to P12\_2
- Pin 5: Connected to P6\_VDD
- Pin 6: Connected to P6\_VDD

Labels in the diagram include: PMOD Header, J14, 1, 2, 3, 4, 5, 6, P12\_0, P12\_1, P12\_2, P6\_VDD, CON 6x1, and No Load.

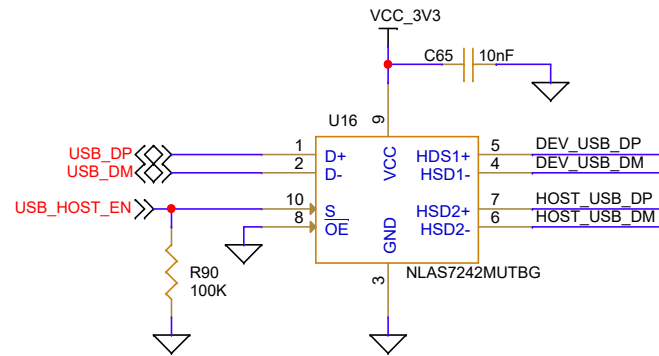
The diagram shows the ICSP Header J5 with the following connections:

- Pin 1: P12\_1
- Pin 2: P12\_0
- Pin 3: P12\_2
- Pin 4: P12\_0
- Pin 5: SWD\_RST\_L
- Pin 6: P12\_0

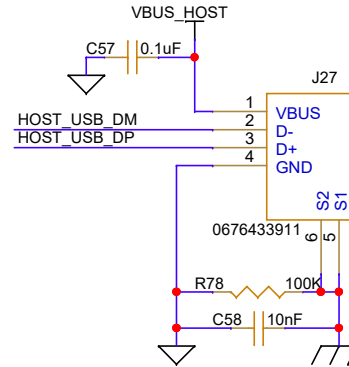
The header is labeled "HDR 3x2" and "No Load".

[illegible][illegible]

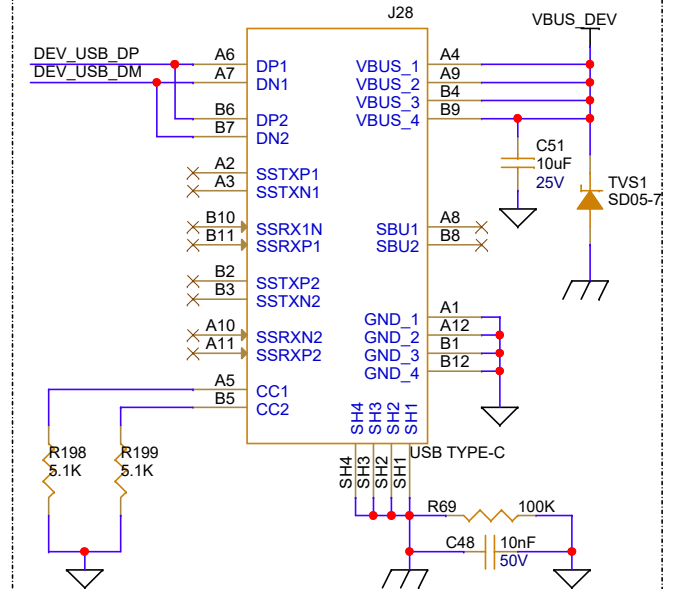
### USB Multiplexer



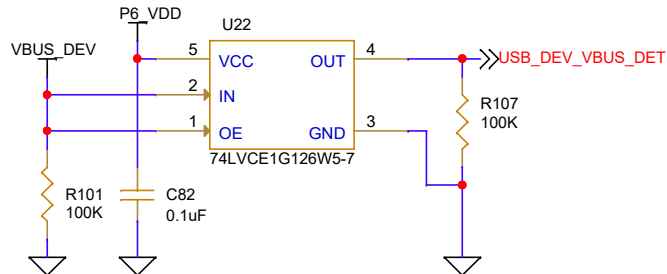
### USB Type-A Receptacle (Host)



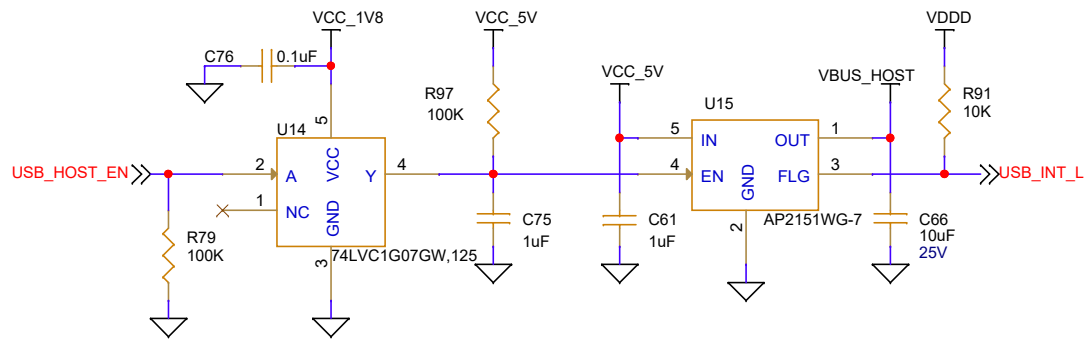
### USB Type-C Connector (Device)



### USB Device Port VBUS Detect



### USB Host VBUS Enable





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**Page Title : USB Host & Device Interface**

|            |                                        |                               |                            |                  |
|------------|----------------------------------------|-------------------------------|----------------------------|------------------|
| Size<br>A4 | Document Number<br><b>630-60435-01</b> | Drawn By<br><b>AARA, TAVA</b> | Approved By<br><b>RKAD</b> | Rev<br><b>05</b> |
|------------|----------------------------------------|-------------------------------|----------------------------|------------------|

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## Accessories

### Cylindrical Bumper

SJ61A4

SJ61A4



SJ61A4

SJ61A4



### Acrylic Overlay

Acrylic Overlay

Color: Clear, Transparent  
Finish: Matt

40 x 34 x  
1mm

### Jumper Shunt

SPC02SYAN



### USB Type-C Connector Brackets

298 SV001



298 SV001



### PCBA label

LBL PCA Label



LBL QR Code



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## REVISION HISTORY

| REV | DESCRIPTION OF CHANGE                   | DATE       |
|-----|-----------------------------------------|------------|
| 01  | Internal Release                        | 2017/03/13 |
| 02  | Internal Release                        | 2017/09/01 |
| 03  | Initial Release                         | 2017/10/20 |
| 04  | Changed WCO load capacitors C85 and C86 | 2020/01/29 |
| 05  | Removed C103 (SuperCap) from assembly   | 2023/12/22 |

|                                                                                       |                                        |                                                                                            |                            |
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| <b>Page Title : Internal Revision History</b>                                         |                                        |                                                                                            |                            |
| Size<br>A4                                                                            | Document Number<br><b>630-60435-01</b> | Drawn By<br><b>AARA, TAVA</b>                                                              | Approved By<br><b>RKAD</b> |
| Date:<br>Friday, December 22, 2023                                                    | Sheet<br><b>16</b> of <b>16</b>        |                                                                                            | Rev<br><b>05</b>           |