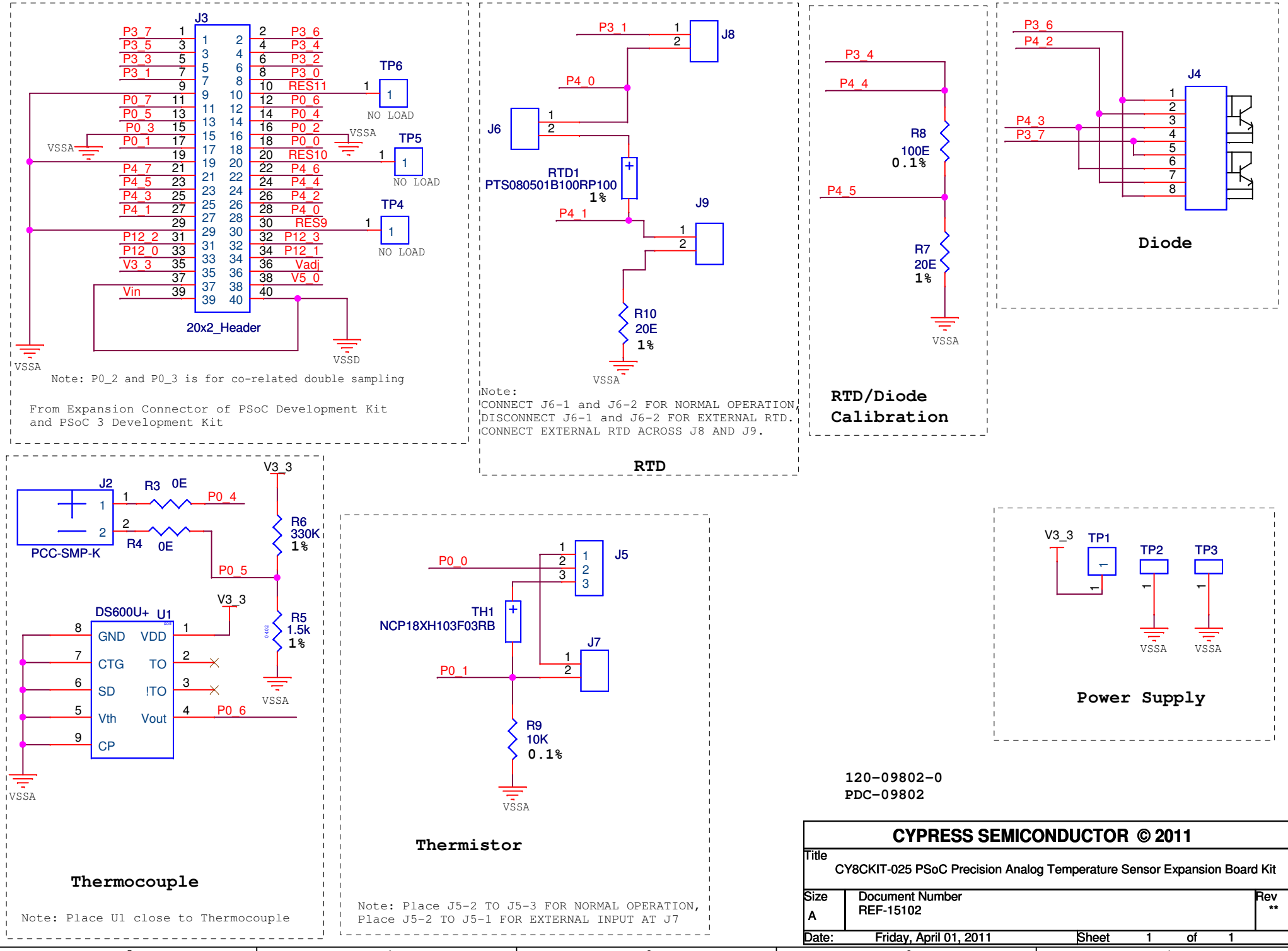

J3
20x2_Header
TP6
TP5
TP4
NO LOAD
VSSA
VSSD
Note: P0_2 and P0_3 is for co-related double sampling
From Expansion Connector of PSoC Development Kit
and PSoC 3 Development Kit
J8
J6
J9
RTD1
PTS080501B100RP100
1%
R10
20E
1%
Note:
CONNECT J6-1 and J6-2 FOR NORMAL OPERATION.
DISCONNECT J6-1 and J6-2 FOR EXTERNAL RTD.
CONNECT EXTERNAL RTD ACROSS J8 AND J9.
RTD
R8
100E
0.1%
R7
20E
1%
RTD/Diode
Calibration
J4
Diode
J2
PCC-SMP-K
R3 0E
R4 0E
R6
330K
1%
R5
1.5k
1%
V3_3
DS600U+ U1
GND
VDD
CTG
TO
SD
!TO
Vth
Vout
CP
Thermocouple
Note: Place U1 close to Thermocouple
J5
TH1
NCP18XH103F03RB
J7
R9
10K
0.1%
Thermistor
Note: Place J5-2 TO J5-3 FOR NORMAL OPERATION,
Place J5-2 TO J5-1 FOR EXTERNAL INPUT AT J7
TP1
TP2
TP3
Power Supply
120-09802-0
PDC-09802
CYPRESS SEMICONDUCTOR © 2011
Title
CY8CKIT-025 PSoC Precision Analog Temperature Sensor Expansion Board Kit
Size
A
Document Number
REF-15102
Rev
**
Date: Friday, April 01, 2011
Sheet 1 of 1