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PSoC 4100M/4200M Family

PSoC® 4 Registers Technical Reference Manual (TRM)

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Book 2 of 2

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Register Mapping

The Register Mapping section discusses the registers and lists all the registers in mapping tables, in address order. For Architecture details, refer to PSoC 4100M/4200M Architecture TRM.

Register General Conventions

The register conventions specific to this section and the Register Reference chapter are listed in this table.

Convention	Description	Explanation
RW	Read / Write	These bits can be both read and written.
R	Read only	These bits can only be read. Writing has no effect on the bit value.
W	Write only	These bits can only be written. Reading the bit returns the reset value.
RW1C	Read / Write '1' to clear	These bits can be read as well as cleared by writing '1'. Writing '0' has no effect on the bit value.
RW0C	Read / Write '0' to clear	These bits can be read as well as cleared by writing '0'. Writing '1' has no effect on the bit value.
RW1S	Read / Write '1' to set	These bits can be read as well as set by writing '1'. Writing '0' has no effect on the bit value.
None / Reserved	Reserved bits	Keep these bits at the default value
'x' in a register /bit field name	Multiple instances	Multiple instances/address ranges of the same register/bit field

Acronyms

This table lists the acronyms used in this document

Table 3-1. Acronyms

Symbol	Unit of Measure
ABUS	analog output bus
AC	alternating current
ADC	analog-to-digital converter
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
API	application programming interface
APOR	analog power-on reset
BC	broadcast clock
BOM	bill of materials
BR	bit rate
BRA	bus request acknowledge
BRQ	bus request
CAN	controller area network
CI	carry in
CMP	compare
CO	carry out
CPU	central processing unit
CRC	cyclic redundancy check

Table 3-1. Acronyms

Symbol	Unit of Measure
CSD	CapSense sigma delta
CT	continuous time
CTBm	continuous time block - mini
DAC	digital-to-analog converter
DC	direct current
DI	digital or data input
DMA	direct memory access
DNL	differential nonlinearity
DO	digital or data output
DSI	digital signal interface
DSM	deep-sleep mode
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read only memory
EMIF	external memory interface
FB	feedback
FIFO	first in first out
FSR	full scale range
GPIO	general purpose I/O
HCI	host-controller interface
HFCLK	high-frequency clock
I^2C	inter-integrated circuit
IDE	integrated development environment
ILO	internal low-speed oscillator
IMO	internal main oscillator
INL	integral nonlinearity
I/O	input/output
IOR	I/O read
IOW	I/O write
IRES	initial power on reset
IRA	interrupt request acknowledge
IRQ	interrupt request
ISR	interrupt service routine
IVR	interrupt vector read
L2CAP	logical link control and adaptation protocol
LPCOMP	low-power comparator
LRb	last received bit
LRB	last received byte
LSb	least significant bit
LSB	least significant byte
LUT	lookup table
MISO	master-in-slave-out
MMIO	memory mapped input/output
MOSI	master-out-slave-in
MSb	most significant bit

Table 3-1. Acronyms

Symbol	Unit of Measure
MSB	most significant byte
PC	program counter
PCH	program counter high
PCL	program counter low
PD	power down
PGA	programmable gain amplifier
PM	power management
PMA	PSoC memory arbiter
POR	power-on reset
PPOR	precision power-on reset
PRS	pseudo random sequence
PSoC®	Programmable System-on-Chip
PSRR	power supply rejection ratio
PSSDC	power system sleep duty cycle
PWM	pulse width modulator
RAM	random-access memory
RETI	return from interrupt
RF	radio frequency
ROM	read only memory
RW	read/write
SAR	successive approximation register
SC	switched capacitor
SCB	serial communication block
SIE	serial interface engine
SIO	special I/O
SE0	single-ended zero
SNR	signal-to-noise ratio
SOF	start of frame
SOI	start of instruction
SP	stack pointer
SPD	sequential phase detector
SPI	serial peripheral interconnect
SPIM	serial peripheral interconnect master
SPIS	serial peripheral interconnect slave
SRAM	static random-access memory
SROM	supervisory read only memory
SRSS	system resources sub-system
SSADC	single slope ADC
SSC	supervisory system call
SYSCLK	system clock
SWD	single wire debug
TC	terminal count
TD	transaction descriptors
UART	universal asynchronous receiver/transmitter

Table 3-1. Acronyms

Symbol	Unit of Measure
UDB	universal digital block
USB	universal serial bus
USBIO	USB I/O
WCO	watch crystal oscillator
WDT	watchdog timer
WDR	watchdog reset
XRES	external reset
XRES_N	external reset, active low

1 UDB Array Bank Control (BCTL) Registers

This section discusses the BCTL registers. It lists all the registers in mapping tables, in address order.

1.1 Register Details

Register Name	Address
UDB_BCTL0_DRV	0x400F6000
UDB_BCTL0_MDCLK_EN	0x400F6001
UDB_BCTL0_MBCLK_EN	0x400F6002
UDB_BCTL0_BOTSEL_L	0x400F6008
UDB_BCTL0_BOTSEL_U	0x400F6009
UDB_BCTL0_TOPSEL_L	0x400F600A
UDB_BCTL0_TOPSEL_U	0x400F600B
UDB_BCTL0_QCLK_EN0	0x400F6010
UDB_BCTL0_QCLK_EN1	0x400F6012
UDB_BCTL0_QCLK_EN2	0x400F6014
UDB_BCTL0_QCLK_EN3	0x400F6016

1.1.1 UDB_BCTL0_DRV

Master Digital Clock Drive Register

Address: 0x400F6000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DRV [7:0]							

Bits	Name	Description
7 : 0	DRV	Master digital clock drive enable for the digital clock that matches the index. Default Value: 0 **0x0: DISABLE:** Enabled drive from array bottom, top drive disabled. **0x1: ENABLE:** Disabled drive from array bottom, top drive enabled.

1.1.2 UDB_BCTL0_MDCLK_EN

Master Digital Clock Enable Register

Address: 0x400F6001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DCEN [7:0]							

Bits	Name	Description
7 : 0	DCEN	Master digital clock enable for the digital clock that matches the index. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

1.1.3 UDB_BCTL0_MBCLK_EN

Master Bus Clock Enable Register

Address: 0x400F6002

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							BCEN

Bits	Name	Description
0	BCEN	Bank Clock Enable Control Default Value: 0 **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

1.1.4 UDB_BCTL0_BOTSEL_L

Lower Nibble Bottom Digital Clock Select Register

Address: 0x400F6008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CLK_SEL3 [7:6]		CLK_SEL2 [5:4]		CLK_SEL1 [3:2]		CLK_SEL0 [1:0]	

Bits	Name	Description
7 : 6	CLK_SEL3	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
5 : 4	CLK_SEL2	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
3 : 2	CLK_SEL1	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
1 : 0	CLK_SEL0	Clock selection control for digital clock Default Value: 0

1.1.4 UDB_BCTL0_BOTSEL_L (continued)

0x0: EDGE_ENABLES:
clock generated from edge enables from clock distribution block

0x1: PORT_INPUT:
Port input

0x2: DSI_OUTPUT:
DSI output

0x3: SYNC_DSI_OUTPUT:
synchronized DSI output

1.1.5 UDB_BCTL0_BOTSEL_U

Upper Nibble Bottom Digital Clock Select Register

Address: 0x400F6009

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CLK_SEL7 [7:6]		CLK_SEL6 [5:4]		CLK_SEL5 [3:2]		CLK_SEL4 [1:0]	

Bits	Name	Description
7 : 6	CLK_SEL7	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
5 : 4	CLK_SEL6	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
3 : 2	CLK_SEL5	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
1 : 0	CLK_SEL4	Clock selection control for digital clock Default Value: 0

1.1.5 UDB_BCTL0_BOTSEL_U (continued)

0x0: EDGE_ENABLES:
clock generated from edge enables from clock distribution block

0x1: PORT_INPUT:
Port input

0x2: DSI_OUTPUT:
DSI output

0x3: SYNC_DSI_OUTPUT:
synchronized DSI output

1.1.6 UDB_BCTL0_TOPSEL_L

Lower Nibble Top Digital Clock Select Register

Address: 0x400F600A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CLK_SEL3 [7:6]		CLK_SEL2 [5:4]		CLK_SEL1 [3:2]		CLK_SEL0 [1:0]	

Bits	Name	Description
7 : 6	CLK_SEL3	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
5 : 4	CLK_SEL2	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
3 : 2	CLK_SEL1	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
1 : 0	CLK_SEL0	Clock selection control for digital clock Default Value: 0

1.1.6 UDB_BCTL0_TOPSEL_L (continued)

0x0: EDGE_ENABLES:
clock generated from edge enables from clock distribution block

0x1: PORT_INPUT:
Port input

0x2: DSI_OUTPUT:
DSI output

0x3: SYNC_DSI_OUTPUT:
synchronized DSI output

1.1.7 UDB_BCTL0_TOPSEL_U

Upper Nibble Top Digital Clock Select Register

Address: 0x400F600B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CLK_SEL7 [7:6]		CLK_SEL6 [5:4]		CLK_SEL5 [3:2]		CLK_SEL4 [1:0]	

Bits	Name	Description
7 : 6	CLK_SEL7	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
5 : 4	CLK_SEL6	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
3 : 2	CLK_SEL5	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
1 : 0	CLK_SEL4	Clock selection control for digital clock Default Value: 0

1.1.7 UDB_BCTL0_TOPSEL_U (continued)

0x0: EDGE_ENABLES:
clock generated from edge enables from clock distribution block

0x1: PORT_INPUT:
Port input

0x2: DSI_OUTPUT:
DSI output

0x3: SYNC_DSI_OUTPUT:
synchronized DSI output

1.1.8 UDB_BCTL0_QCLK_EN0

Quadrant Digital Clock Enable Registers

Address: 0x400F6010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DCEN_Q [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SLEEP_TEST	NC0	WR_CFG_OPT	GLB_DSI_WR	DISABLE_ROUTE	GCH_WR_HI	GCH_WR_LO	BCEN_Q

Bits	Name	Description
15	SLEEP_TEST	Reserved
14	NC0	Spare register bit Default Value: 0
13	WR_CFG_OPT	Select 1/2 clock cycle or full clock cycle generation for bus_last_strobe used in generating write strobes for latches within the UDB. Only one BCLK_ENx register per bank has an active bit. BCTL0_BCLK_EN0 controls this bit for Bank 0. The WR_CFG_OPT bits in the other BCTLx_BCLK_ENy registers are not used. Default Value: 0 **0x0: FULL_CYCLE_STB:** bus_last_strobe is generated for the full final bus_clk cycle of a bus transaction. **0x1: HALF_CYCLE_STB:** bus_last_strobe is generated during the last 1/2 clock cycle of a bus transaction on the negative edge of bus_clk.
12	GLB_DSI_WR	Enable global write operation for the DSI routing channels. When this bit is set, the DSI ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Control is split top and bottom. BCTL0_BCLK_EN0 controls DSI blocks 0-3. BCTL0_BCLK_EN3 controls DSI blocks 4-7. The GLB_DSI_WR bits in the other BCTLx_BCLK_ENy registers are not used. Default Value: 0 **0x0: DISABLE:** Global DSI channel configuration write is disabled. **0x1: ENABLE:** Global DSI channel configuration write is enabled.
11	DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. Default Value: 0

1.1.8 UDB_BCTL0_QCLK_EN0 (continued)

		0x0: DISABLE: The routing in this quadrant can be enabled with the bank route enable bit. (default) **0x1: ENABLE:** The routing in this quadrant is disabled and held in a benign state.
10	GCH_WR_HI	Enable global write operation for the routing channel with the higher address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for higher order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for higher order address is enabled.
9	GCH_WR_LO	Enable global write operation for the routing channel with the lower address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for lower order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for lower order address is enabled.
8	BCEN_Q	Bank Clock Enable Control Default Value: 0 **0x0: DISABLE:** Digital Global clock is disabled. **0x1: ENABLE:** Digital Global clock is enabled.
7 : 0	DCEN_Q	Digital clock enable for indexed digital clock for the associated quadrant. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

1.1.9 UDB_BCTL0_QCLK_EN1

Quadrant Digital Clock Enable Registers

Address: 0x400F6012

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DCEN_Q [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SLEEP_TEST	NC0	WR_CFG_OPT	GLB_DSI_WR	DISABLE_ROUTE	GCH_WR_HI	GCH_WR_LO	BCEN_Q

Bits	Name	Description
15	SLEEP_TEST	Reserved
14	NC0	Spare register bit Default Value: 0
13	WR_CFG_OPT	Select 1/2 clock cycle or full clock cycle generation for bus_last_strobe used in generating write strobes for latches within the UDB. Only one BCLK_ENx register per bank has an active bit. BCTL0_BCLK_EN0 controls this bit for Bank 0. The WR_CFG_OPT bits in the other BCTLx_BCLK_ENy registers are not used. Default Value: 0 **0x0: FULL_CYCLE_STB:** bus_last_strobe is generated for the full final bus_clk cycle of a bus transaction. **0x1: HALF_CYCLE_STB:** bus_last_strobe is generated during the last 1/2 clock cycle of a bus transaction on the negative edge of bus_clk.
12	GLB_DSI_WR	Enable global write operation for the DSI routing channels. When this bit is set, the DSI ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Control is split top and bottom. BCTL0_BCLK_EN0 controls DSI blocks 0-3. BCTL0_BCLK_EN3 controls DSI blocks 4-7. The GLB_DSI_WR bits in the other BCTLx_BCLK_ENy registers are not used. Default Value: 0 **0x0: DISABLE:** Global DSI channel configuration write is disabled. **0x1: ENABLE:** Global DSI channel configuration write is enabled.
11	DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. Default Value: 0

1.1.9 UDB_BCTL0_QCLK_EN1 (continued)

		0x0: DISABLE: The routing in this quadrant can be enabled with the bank route enable bit. (default) **0x1: ENABLE:** The routing in this quadrant is disabled and held in a benign state.
10	GCH_WR_HI	Enable global write operation for the routing channel with the higher address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for higher order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for higher order address is enabled.
9	GCH_WR_LO	Enable global write operation for the routing channel with the lower address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for lower order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for lower order address is enabled.
8	BCEN_Q	Bank Clock Enable Control Default Value: 0 **0x0: DISABLE:** Digital Global clock is disabled. **0x1: ENABLE:** Digital Global clock is enabled.
7 : 0	DCEN_Q	Digital clock enable for indexed digital clock for the associated quadrant. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

1.1.10 UDB_BCTL0_QCLK_EN2

Quadrant Digital Clock Enable Registers

Address: 0x400F6014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DCEN_Q [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SLEEP_TEST	NC0	WR_CFG_OPT	GLB_DSI_WR	DISABLE_ROUTE	GCH_WR_HI	GCH_WR_LO	BCEN_Q

Bits	Name	Description
15	SLEEP_TEST	Reserved
14	NC0	Spare register bit Default Value: 0
13	WR_CFG_OPT	Select 1/2 clock cycle or full clock cycle generation for bus_last_strobe used in generating write strobes for latches within the UDB. Only one BCLK_ENx register per bank has an active bit. BCTL0_BCLK_EN0 controls this bit for Bank 0. The WR_CFG_OPT bits in the other BCTLx_BCLK_ENy registers are not used. Default Value: 0 **0x0: FULL_CYCLE_STB:** bus_last_strobe is generated for the full final bus_clk cycle of a bus transaction. **0x1: HALF_CYCLE_STB:** bus_last_strobe is generated during the last 1/2 clock cycle of a bus transaction on the negative edge of bus_clk.
12	GLB_DSI_WR	Enable global write operation for the DSI routing channels. When this bit is set, the DSI ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Control is split top and bottom. BCTL0_BCLK_EN0 controls DSI blocks 0-3. BCTL0_BCLK_EN3 controls DSI blocks 4-7. The GLB_DSI_WR bits in the other BCTLx_BCLK_ENy registers are not used. Default Value: 0 **0x0: DISABLE:** Global DSI channel configuration write is disabled. **0x1: ENABLE:** Global DSI channel configuration write is enabled.
11	DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. Default Value: 0

1.1.10 UDB_BCTL0_QCLK_EN2 (continued)

		0x0: DISABLE: The routing in this quadrant can be enabled with the bank route enable bit. (default) **0x1: ENABLE:** The routing in this quadrant is disabled and held in a benign state.
10	GCH_WR_HI	Enable global write operation for the routing channel with the higher address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for higher order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for higher order address is enabled.
9	GCH_WR_LO	Enable global write operation for the routing channel with the lower address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for lower order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for lower order address is enabled.
8	BCEN_Q	Bank Clock Enable Control Default Value: 0 **0x0: DISABLE:** Digital Global clock is disabled. **0x1: ENABLE:** Digital Global clock is enabled.
7 : 0	DCEN_Q	Digital clock enable for indexed digital clock for the associated quadrant. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

1.1.11 UDB_BCTL0_QCLK_EN3

Quadrant Digital Clock Enable Registers

Address: 0x400F6016

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DCEN_Q [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SLEEP_TEST	NC0	WR_CFG_OPT	GLB_DSI_WR	DISABLE_ROUTE	GCH_WR_HI	GCH_WR_LO	BCEN_Q

Bits	Name	Description
15	SLEEP_TEST	Reserved
14	NC0	Spare register bit Default Value: 0
13	WR_CFG_OPT	Select 1/2 clock cycle or full clock cycle generation for bus_last_strobe used in generating write strobes for latches within the UDB. Only one BCLK_ENx register per bank has an active bit. BCTL0_BCLK_EN0 controls this bit for Bank 0. The WR_CFG_OPT bits in the other BCTLx_BCLK_ENy registers are not used. Default Value: 0 **0x0: FULL_CYCLE_STB:** bus_last_strobe is generated for the full final bus_clk cycle of a bus transaction. **0x1: HALF_CYCLE_STB:** bus_last_strobe is generated during the last 1/2 clock cycle of a bus transaction on the negative edge of bus_clk.
12	GLB_DSI_WR	Enable global write operation for the DSI routing channels. When this bit is set, the DSI ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Control is split top and bottom. BCTL0_BCLK_EN0 controls DSI blocks 0-3. BCTL0_BCLK_EN3 controls DSI blocks 4-7. The GLB_DSI_WR bits in the other BCTLx_BCLK_ENy registers are not used. Default Value: 0 **0x0: DISABLE:** Global DSI channel configuration write is disabled. **0x1: ENABLE:** Global DSI channel configuration write is enabled.
11	DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. Default Value: 0

1.1.11 UDB_BCTL0_QCLK_EN3 (continued)

		0x0: DISABLE: The routing in this quadrant can be enabled with the bank route enable bit. (default) **0x1: ENABLE:** The routing in this quadrant is disabled and held in a benign state.
10	GCH_WR_HI	Enable global write operation for the routing channel with the higher address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for higher order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for higher order address is enabled.
9	GCH_WR_LO	Enable global write operation for the routing channel with the lower address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for lower order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for lower order address is enabled.
8	BCEN_Q	Bank Clock Enable Control Default Value: 0 **0x0: DISABLE:** Digital Global clock is disabled. **0x1: ENABLE:** Digital Global clock is enabled.
7 : 0	DCEN_Q	Digital clock enable for indexed digital clock for the associated quadrant. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

2 CAN Registers

This section discusses the CAN registers. It lists all the registers in mapping tables, in address order.

2.1 Register Details

Register Name	Address
CAN0_INT_STATUS	0x402E0000
CAN0_INT_EBL	0x402E0004
CAN0_BUFFER_STATUS	0x402E0008
CAN0_ERROR_STATUS	0x402E000C
CAN0_COMMAND	0x402E0010
CAN0_CONFIG	0x402E0014
CAN0_ECR	0x402E0018
CAN0_CNTL	0x402E0400
CAN0_TTCAN_COUNTER	0x402E0404
CAN0_TTCAN_COMPARE	0x402E0408
CAN0_TTCAN_CAPTURE	0x402E040C
CAN0_TTCAN_TIMING	0x402E0410
CAN0_INTR_CAN	0x402E0414
CAN0_INTR_CAN_SET	0x402E0418
CAN0_INTR_CAN_MASK	0x402E041C
CAN0_INTR_CAN_MASKED	0x402E0420
CAN1_INT_STATUS	0x402F0000
CAN1_INT_EBL	0x402F0004
CAN1_BUFFER_STATUS	0x402F0008
CAN1_ERROR_STATUS	0x402F000C
CAN1_COMMAND	0x402F0010
CAN1_CONFIG	0x402F0014
CAN1_ECR	0x402F0018
CAN1_CNTL	0x402F0400
CAN1_TTCAN_COUNTER	0x402F0404
CAN1_TTCAN_COMPARE	0x402F0408
CAN1_TTCAN_CAPTURE	0x402F040C

Register Name	Address
CAN1_TTCAN_TIMING	0x402F0410
CAN1_INTR_CAN	0x402F0414
CAN1_INTR_CAN_SET	0x402F0418
CAN1_INTR_CAN_MASK	0x402F041C
CAN1_INTR_CAN_MASKED	0x402F0420

2.1.1 CAN0_INT_STATUS

Interrupt Status

Address: 0x402E0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	None	
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	None	
Name	FORM_ERR	ACK_ERR	STUFF_ERR	BIT_ERR	OVR_LOAD	ARB_LOSS	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	SST_FAILURE	STUCK_AT_0	RTR_MSG	RX_MSG	TX_MSG	RX_MSG_LOSS	BUS_OFF	CRC_ERR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	SST_FAILURE	Single shot transmission failure 0: Normal operation 1: A buffer set for single shot transmission experienced an arbitration loss or a bus error during transmission The sst_failure interrupt is set as well when the CAN controller is being stopped while an SST message is in the transmit buffer. Default Value: 0
14	STUCK_AT_0	Stuck at dominant error 0: Normal Operation 1: Indicates if the rx input remains stuack at 0 (dominant level) for more than 11 consecutive bit times. The "stuck at 0" condition is checked, only when COMMAND.RUN is set Default Value: 0
13	RTR_MSG	RTR auto-reply message sent 0: Normal operation 1: Indicates that a RTR auto-reply message was sent Default Value: 0

2.1.1 CAN0_INT_STATUS (continued)

12	RX_MSG	Indicates that a message was received 0: Normal operation 1: A new message was successfully received and stored in a receive buffer which has its RxIntEBL flag asserted. Default Value: 0
11	TX_MSG	Indicates that a message was sent 0: Normal operation 1: A message was successfully sent from a transmit buffer which has its TxIntEbl flag asserted. Default Value: 0
10	RX_MSG_LOSS	Is set when a new message arrives but the RxMessage flag MsgAv is set Default Value: 0
9	BUS_OFF	The CAN has reached the bus off state Default Value: 0
8	CRC_ERR	A CAN CRC error was detected Default Value: 0
7	FORM_ERR	A CAN message format error was detected Default Value: 0
6	ACK_ERR	An CAN message acknowledge error was detected Default Value: 0
5	STUFF_ERR	A bit stuffing error was detected Default Value: 0
4	BIT_ERR	A bit error was detected Default Value: 0
3	OVR_LOAD	An overload frame was received, or reactive overload frame condition is detected (ISO-11898-1 section 10.11) Default Value: 0
2	ARB_LOSS	The arbitration was lost while sending a message Default Value: 0

2.1.2 CAN0_INT_EBL

Interrupt Enable

Address: 0x402E0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	None	RW
HW Access	R	R	R	R	R	R	None	R
Name	FORM_ERR_ENBL	ACK_ERR_ENBL	STUFF_ERR_ENBL	BIT_ERR_ENBL	OVR_LOAD_ENBL	ARB_LOSS_ENBL	None	GLOBAL_INT_ENBL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SST_FAILURE_ENBL	STUCK_AT_0_ENBL	RTR_MSG_ENBL	RX_MSG_ENBl	TX_MSG_ENBL	RX_MSG_LOSS	BUS_OFF_ENBL	CRC_ERR_ENBL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	SST_FAILURE_ENBL	See description in INT_STATUS Default Value: 0
14	STUCK_AT_0_ENBL	See description in INT_STATUS Default Value: 0
13	RTR_MSG_ENBL	See description in INT_STATUS Default Value: 0
12	RX_MSG_ENBl	See description in INT_STATUS Default Value: 0
11	TX_MSG_ENBL	See description in INT_STATUS Default Value: 0
10	RX_MSG_LOSS	See description in INT_STATUS Default Value: 0
9	BUS_OFF_ENBL	See description in INT_STATUS Default Value: 0

2.1.2 CAN0_INT_EBL (continued)

8	CRC_ERR_ENBL	See description in INT_STATUS Default Value: 0
7	FORM_ERR_ENBL	See description in INT_STATUS Default Value: 0
6	ACK_ERR_ENBL	See description in INT_STATUS Default Value: 0
5	STUFF_ERR_ENBL	See description in INT_STATUS Default Value: 0
4	BIT_ERR_ENBL	See description in INT_STATUS Default Value: 0
3	OVR_LOAD_ENBL	See description in INT_STATUS Default Value: 0
2	ARB_LOSS_ENBL	See description in INT_STATUS Default Value: 0
0	GLOBAL_INT_ENBL	global interrupt enable flag ¡®0¡¯: All interrupts are disabled ¡®1¡¯: Enabled interrupt sources are available Default Value: 0

2.1.3 CAN0_BUFFER_STATUS

RxMessage and TxMessage Buffer Status

Address: 0x402E0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	RX7_MSG_AV	RX6_MSG_AV	RX5_MSG_AV	RX4_MSG_AV	RX3_MSG_AV	RX2_MSG_AV	RX1_MSG_AV	RX0_MSG_AV

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	RX15_MSG_AV	RX14_MSG_AV	RX13_MSG_AV	RX12_MSG_AV	RX11_MSG_AV	RX10_MSG_AV	RX9_MSG_AV	RX8_MSG_AV

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	TX7_REQ_PEND	TX6_REQ_PEND	TX5_REQ_PEND	TX4_REQ_PEND	TX3_REQ_PEND	TX2_REQ_PEND	TX1_REQ_PEND	TX0_REQ_PEND

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	TX7_REQ_PEND	TxMessage Buffer Status Default Value: 0
22	TX6_REQ_PEND	TxMessage Buffer Status Default Value: 0
21	TX5_REQ_PEND	TxMessage Buffer Status Default Value: 0
20	TX4_REQ_PEND	TxMessage Buffer Status Default Value: 0
19	TX3_REQ_PEND	TxMessage Buffer Status Default Value: 0
18	TX2_REQ_PEND	TxMessage Buffer Status Default Value: 0
17	TX1_REQ_PEND	TxMessage Buffer Status Default Value: 0

2.1.3 CAN0_BUFFER_STATUS (continued)

16	TX0_REQ_PEND	TxMessage Buffer Status Default Value: 0
15	RX15_MSG_AV	RxMessage Buffer Status Default Value: 0
14	RX14_MSG_AV	RxMessage Buffer Status Default Value: 0
13	RX13_MSG_AV	RxMessage Buffer Status Default Value: 0
12	RX12_MSG_AV	RxMessage Buffer Status Default Value: 0
11	RX11_MSG_AV	RxMessage Buffer Status Default Value: 0
10	RX10_MSG_AV	RxMessage Buffer Status Default Value: 0
9	RX9_MSG_AV	RxMessage Buffer Status Default Value: 0
8	RX8_MSG_AV	RxMessage Buffer Status Default Value: 0
7	RX7_MSG_AV	RxMessage Buffer Status Default Value: 0
6	RX6_MSG_AV	RxMessage Buffer Status Default Value: 0
5	RX5_MSG_AV	RxMessage Buffer Status Default Value: 0
4	RX4_MSG_AV	RxMessage Buffer Status Default Value: 0
3	RX3_MSG_AV	RxMessage Buffer Status Default Value: 0
2	RX2_MSG_AV	RxMessage Buffer Status Default Value: 0
1	RX1_MSG_AV	RxMessage Buffer Status Default Value: 0
0	RX0_MSG_AV	RxMessage Buffer Status Default Value: 0

2.1.4 CAN0_ERROR_STATUS

CAN Error Status

Address: 0x402E000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TX_ERR_CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RX_ERR_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R	R	R	
HW Access	None				RW	RW	RW	
Name	None [23:20]				RXGTE96	TXGTE96	ERROR_STATE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	RXGTE96	The Rx error counter is greater or equal 96 Default Value: 0
18	TXGTE96	The Tx error counter is greater or equal 96 Default Value: 0
17 : 16	ERROR_STATE	The error state of the CAN node: 00: error active (normal operation) 01: error passive 1x: bus off Default Value: 0
15 : 8	RX_ERR_CNT	The receive error counter according to the CAN 2.0 specification. When in bus-off state, this counter is used to count 128 groups of 11 recessive bits. it is fixed at 255 Default Value: 0

2.1.4 CAN0_ERROR_STATUS (continued)

7 : 0	TX_ERR_CNT	The transmitter error counter according to the CAN standard. When it is greater than 255, it is fixed at 255 Default Value: 0

2.1.5 CAN0_COMMAND

CAN Command Register

Address: 0x402E0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				SRAM_TEST	LOOPBACK_TEST	LISTEN	RUN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	IP_REV_NUMBER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	R				R			
Name	IP_MAJOR_VERSION [31:28]				IP_MINOR_VERSION [27:24]			

Bits	Name	Description
31 : 28	IP_MAJOR_VERSION	IP Major Version Number Default Value: 3
27 : 24	IP_MINOR_VERSION	IP Minor Version Number Default Value: 0
23 : 16	IP_REV_NUMBER	IP Revision Number Default Value: 0
3	SRAM_TEST	Reserved
2	LOOPBACK_TEST	Reserved
1	LISTEN	Reserved
0	RUN	Reserved

2.1.6 CAN0_CONFIG

CAN Configuration

Address: 0x402E0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW	RW		RW	RW
HW Access	R			R	R		R	R
Name	CFG_TSEG2 [7:5]			AUTO_RESTART	CFG_SJW [3:2]		SAMPLING_MODE	EDGE_MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW	RW	RW			
HW Access	None	R	R	R	R			
Name	None	ECR_MODE	SWAP_ENDIAN	CFG_ARBITER	CFG_TSEG1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CFG_BITRATE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	CFG_BITRATE [30:24]						

Bits	Name	Description
30 : 16	CFG_BITRATE	Prescaler for generating the time quantum which defines the TQ: 0: One time quantum equals 1 clock cycle 1: One time quantum equals 2 clock cycles ... 32767: One time quantum equals 32768 clock cycles Default Value: 0
14	ECR_MODE	Error Capture mode 0: Free running: The ECR register shows the current bit position within the CAN frame 1: Capture mode: The ecr register shows the bit position and type of the last captured CAN error. Default Value: 0
13	SWAP_ENDIAN	Swap Endian - the byte position of the CAN receive and transmit data fields can be modified to match the endian setting of the processor or the used CAN protocol 0: CAN data byte position is not swapped (big endian) 1: CAN data byte position is swapped (little endian) Default Value: 0

2.1.6 CAN0_CONFIG (continued)

12	CFG_ARBITER	Transmit buffer arbiter ¡®0¡¯: Round robin arbitration ¡®1¡¯: Fixed priority arbitration Default Value: 0
11 : 8	CFG_TSEG1	Time segment 1 Length of the first time segment: tseg1 = cfg_tseg1 + 1 Time segment 1 includes the propagation time. cfg_tseg1=0 and cfg_tseg1=1 are not allowed. Default Value: 0
7 : 5	CFG_TSEG2	Time segment 2 Length of the second time segment: tseg2 = cfg_tseg2 + 1 cfg_tseg2=0 is not allowed; cfg_tseg2=1 is only allowed in direct sampling mode. Default Value: 0
4	AUTO_RESTART	¡®0¡¯: After bus-off, the CAN core must be restarted by setting COMMAND.RUN register. This is the recommended setting. ¡®1¡¯: After bus-off, the CAN core is restarting automatically after 128 groups of 11 recessive bits Default Value: 0
3 : 2	CFG_SJW	Synchronization jump width - 1 sjw ¡Ü tseg1 and sjw ¡Ü tseg2 Default Value: 0
1	SAMPLING_MODE	CAN bus bit sampling ¡®0¡¯: One sampling point is used in the receiver path ¡®1¡¯: 3 sampling points with majority decision are used Default Value: 0
0	EDGE_MODE	CAN bus synchronization logic ¡®0¡¯: Edge from ¡®R¡¯ to ¡®D¡¯ is used for synchronization ¡®1¡¯: Both edges are used Note, only ¡®R¡¯ to ¡®D¡¯ edge shall be used for synchronization per ISO-11898-1 spec, so this bit should always be set 0 (by default) Default Value: 0

2.1.7 CAN0_ECR

Error Capture Register

Address: 0x402E0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R	R	R			RW
HW Access	RW		RW	RW	RW			RW
Name	BIT [7:6]		TX_MODE	RX_MODE	ERROR_TYPE [3:1]			ECR_STATUS

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	Field [15:12]				BIT [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							RW
Name	None [23:17]							Field

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

2.1.7 CAN0_ECR (continued)

16 : 12	Field	Field - 0x00 : Stopped 0x01 : Synchronize 0x05 : Interframe 0x06 : Bus Idle 0x07 : Start of Frame 0x08 : Arbitration 0x09 : Control 0x0A : Data 0x0B : CRC 0x0C : ACK 0x0D : End of frame 0x10 : Error flag 0x11 : Error echo 0x12 : Error delimiter 0x18 : Overload flag 0x19 : Overload echo 0x1A : Overload delimiter Others : N/A Default Value: 0
11 : 6	BIT	Bit number inside of Field Default Value: 0
5	TX_MODE	TX Mode - 0: No status 1: CAN Controller is transmitter Default Value: 0
4	RX_MODE	RX Mode - 0: No status 1: CAN Controller is receiver Default Value: 0
3 : 1	ERROR_TYPE	Error type - 000 : Arbitration loss 001 : Bit Error 010 : Bit Stuffing Error 011 : Acknowledge Error 100 : Form Error 101 : CRC Error Others : N/A Default Value: 0
0	ECR_STATUS	ECR STATUS - 0: ECR register captured an error, or it is in free running mode 1: ECR register is armed Default Value: 0

2.1.8 CAN0_CNTL

Control

Address: 0x402E0400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TT_ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	IP_ENABLE	None [30:24]						

Bits	Name	Description
31	IP_ENABLE	IP Enable/Disable 0=IP is disabled/reset 1=IP is enabled/running Default Value: 0
0	TT_ENABLE	TTCAN enable/disable 0=TTCAN is disabled; Interrupt_can is sourced from 3PIP. INT_EBL.GLOBAL_INT_ENBL & (INT_EBL[i] & INT_STATUS[i]) 1=TTCAN is enabled; Interrupt_can is sourced from INTR_CAN_MASKED. Default Value: 0

2.1.9 CAN0_TTCAN_COUNTER

TTCAN Level1 16-Bit local time counter

Address: 0x402E0404

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	LOCAL_TIME [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	LOCAL_TIME [31:24]							

Bits	Name	Description
31 : 16	LOCAL_TIME	Bit time counter in TTCAN level 1 Default Value: 0

2.1.10 CAN0_TTCAN_COMPARE

TTCAN Level1 compare configuration

Address: 0x402E0408

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TIME_MARK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TIME_MARK [31:24]							

Bits	Name	Description
31 : 16	TIME_MARK	compare target, when TTCAN_COUNTER.LOCAL_TIME counts to TT_COMPARE, INTR_CAN.TT_COMPARE will be set Default Value: 65535

2.1.11 CAN0_TTCAN_CAPTURE

TTCAN Level1 capture configuration

Address: 0x402E040C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SYNC_MARK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SYNC_MARK [31:24]							

Bits	Name	Description
31 : 16	SYNC_MARK	copy TTCAN_COUNTER.LOCAL_TIME to TTCAN_CAPTURE.SYNC_MARK, when SOF detected. when new event triggers, new LOCAL_TIME value will overwrite previous SYNC_MARK value Default Value: 0

2.1.12 CAN0_TTCAN_TIMING

TTCAN Level1 timing configuration, duplicate of CONFIG fields

Address: 0x402E0410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			None			RW	None
HW Access	R			None			R	None
Name	CFG_TSEG2 [7:5]			None [4:2]			SAMPLING _MODE	None

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				CFG_TSEG1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CFG_BITRATE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	CFG_BITRATE [30:24]						

Bits	Name	Description
30 : 16	CFG_BITRATE	Prescaler for generating the time quantum which defines the TQ: 0: One time quantum equals 1 clock cycle 1: One time quantum equals 2 clock cycles ... 32767: One time quantum equals 32768 clock cycles Default Value: 0
11 : 8	CFG_TSEG1	Time segment 1 Length of the first time segment: tseg1 = cfg_tseg1 + 1 Time segment 1 includes the propagation time. cfg_tseg1=0 and cfg_tseg1=1 are not allowed. Default Value: 0

2.1.12 CAN0_TTCAN_TIMING (continued)

7 : 5	CFG_TSEG2	Time segment 2 Length of the second time segment: tseg2 = cfg_tseg2 + 1 cfg_tseg2=0 is not allowed; cfg_tseg2=1 is only allowed in direct sampling mode. Default Value: 0
1	SAMPLING_MODE	CAN bus bit sampling ¡®0¡¯: One sampling point is used in the receiver path ¡®1¡¯: 3 sampling points with majority decision are used Default Value: 0

2.1.13 CAN0_INTR_CAN

CAN Interrupt Cause (TTCAN + INT_STATUS Or)

Address: 0x402E0414

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [7:3]					TT_CAPTURE	TT_COMPARE	INT_STATUS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	TT_CAPTURE	Triggers when LOCAL_TIME is saved to TT_CAPTURE, on SOF detection Default Value: 0
1	TT_COMPARE	Triggers when LOCAL_TIME is equal to TT_COMPARE Default Value: 0
0	INT_STATUS	Triggers when any enabled (INT_EBL) interrupt are set in INT_STATUS Default Value: 0

2.1.14 CAN0_INTR_CAN_SET

CAN Interrupt Set (TTCAN + INT_STATUS Or)

Address: 0x402E0418

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					TT_CAPTURE	TT_COMPARE	INT_STATUS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	TT_CAPTURE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	TT_COMPARE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	INT_STATUS	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

2.1.15 CAN0_INTR_CAN_MASK

CAN Interrupt Mask (TTCAN + INT_STATUS Or)

Address: 0x402E041C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					TT_CAPTURE	TT_COMPARE	INT_STATUS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	TT_CAPTURE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	TT_COMPARE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	INT_STATUS	Mask bit for corresponding bit in interrupt request register. Default Value: 0

2.1.16 CAN0_INTR_CAN_MASKED

Can Interrupt Masked (TTCAN + INT_STATUS Or)

Address: 0x402E0420

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					TT_CAPTURE	TT_COMPARE	INT_STATUS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	TT_CAPTURE	Logical and of corresponding request and mask bits. Default Value: 0
1	TT_COMPARE	Logical and of corresponding request and mask bits. Default Value: 0
0	INT_STATUS	Logical and of corresponding request and mask bits. Default Value: 0

2.1.17 CAN1_INT_STATUS

Interrupt Status

Address: 0x402F0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	None	
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	None	
Name	FORM_ERR	ACK_ERR	STUFF_ERR	BIT_ERR	OVR_LOAD	ARB_LOSS	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	SST_FAILURE	STUCK_AT_0	RTR_MSG	RX_MSG	TX_MSG	RX_MSG_LOSS	BUS_OFF	CRC_ERR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	SST_FAILURE	Single shot transmission failure 0: Normal operation 1: A buffer set for single shot transmission experienced an arbitration loss or a bus error during transmission The sst_failure interrupt is set as well when the CAN controller is being stopped while an SST message is in the transmit buffer. Default Value: 0
14	STUCK_AT_0	Stuck at dominant error 0: Normal Operation 1: Indicates if the rx input remains stuack at 0 (dominant level) for more than 11 consecutive bit times. The "stuck at 0" condition is checked, only when COMMAND.RUN is set Default Value: 0
13	RTR_MSG	RTR auto-reply message sent 0: Normal operation 1: Indicates that a RTR auto-reply message was sent Default Value: 0

2.1.17 CAN1_INT_STATUS (continued)

12	RX_MSG	Indicates that a message was received 0: Normal operation 1: A new message was successfully received and stored in a receive buffer which has its RxIntEBL flag asserted. Default Value: 0
11	TX_MSG	Indicates that a message was sent 0: Normal operation 1: A message was successfully sent from a transmit buffer which has its TxIntEbl flag asserted. Default Value: 0
10	RX_MSG_LOSS	Is set when a new message arrives but the RxMessage flag MsgAv is set Default Value: 0
9	BUS_OFF	The CAN has reached the bus off state Default Value: 0
8	CRC_ERR	A CAN CRC error was detected Default Value: 0
7	FORM_ERR	A CAN message format error was detected Default Value: 0
6	ACK_ERR	An CAN message acknowledge error was detected Default Value: 0
5	STUFF_ERR	A bit stuffing error was detected Default Value: 0
4	BIT_ERR	A bit error was detected Default Value: 0
3	OVR_LOAD	An overload frame was received, or reactive overload frame condition is detected (ISO-11898-1 section 10.11) Default Value: 0
2	ARB_LOSS	The arbitration was lost while sending a message Default Value: 0

2.1.18 CAN1_INT_EBL

Interrupt Enable

Address: 0x402F0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	None	RW
HW Access	R	R	R	R	R	R	None	R
Name	FORM_ERR_ENBL	ACK_ERR_ENBL	STUFF_ERR_ENBL	BIT_ERR_ENBL	OVR_LOAD_ENBL	ARB_LOSS_ENBL	None	GLOBAL_INT_ENBL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SST_FAILURE_ENBL	STUCK_AT_0_ENBL	RTR_MSG_ENBL	RX_MSG_ENBl	TX_MSG_ENBL	RX_MSG_LOSS	BUS_OFF_ENBL	CRC_ERR_ENBL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	SST_FAILURE_ENBL	See description in INT_STATUS Default Value: 0
14	STUCK_AT_0_ENBL	See description in INT_STATUS Default Value: 0
13	RTR_MSG_ENBL	See description in INT_STATUS Default Value: 0
12	RX_MSG_ENBl	See description in INT_STATUS Default Value: 0
11	TX_MSG_ENBL	See description in INT_STATUS Default Value: 0
10	RX_MSG_LOSS	See description in INT_STATUS Default Value: 0
9	BUS_OFF_ENBL	See description in INT_STATUS Default Value: 0

2.1.18 CAN1_INT_EBL (continued)

8	CRC_ERR_ENBL	See description in INT_STATUS Default Value: 0
7	FORM_ERR_ENBL	See description in INT_STATUS Default Value: 0
6	ACK_ERR_ENBL	See description in INT_STATUS Default Value: 0
5	STUFF_ERR_ENBL	See description in INT_STATUS Default Value: 0
4	BIT_ERR_ENBL	See description in INT_STATUS Default Value: 0
3	OVR_LOAD_ENBL	See description in INT_STATUS Default Value: 0
2	ARB_LOSS_ENBL	See description in INT_STATUS Default Value: 0
0	GLOBAL_INT_ENBL	global interrupt enable flag ¡®0¡¯: All interrupts are disabled ¡®1¡¯: Enabled interrupt sources are available Default Value: 0

2.1.19 CAN1_BUFFER_STATUS

RxMessage and TxMessage Buffer Status

Address: 0x402F0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	RX7_MSG_AV	RX6_MSG_AV	RX5_MSG_AV	RX4_MSG_AV	RX3_MSG_AV	RX2_MSG_AV	RX1_MSG_AV	RX0_MSG_AV

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	RX15_MSG_AV	RX14_MSG_AV	RX13_MSG_AV	RX12_MSG_AV	RX11_MSG_AV	RX10_MSG_AV	RX9_MSG_AV	RX8_MSG_AV

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	TX7_REQ_PEND	TX6_REQ_PEND	TX5_REQ_PEND	TX4_REQ_PEND	TX3_REQ_PEND	TX2_REQ_PEND	TX1_REQ_PEND	TX0_REQ_PEND

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	TX7_REQ_PEND	TxMessage Buffer Status Default Value: 0
22	TX6_REQ_PEND	TxMessage Buffer Status Default Value: 0
21	TX5_REQ_PEND	TxMessage Buffer Status Default Value: 0
20	TX4_REQ_PEND	TxMessage Buffer Status Default Value: 0
19	TX3_REQ_PEND	TxMessage Buffer Status Default Value: 0
18	TX2_REQ_PEND	TxMessage Buffer Status Default Value: 0
17	TX1_REQ_PEND	TxMessage Buffer Status Default Value: 0

2.1.19 CAN1_BUFFER_STATUS (continued)

16	TX0_REQ_PEND	TxMessage Buffer Status Default Value: 0
15	RX15_MSG_AV	RxMessage Buffer Status Default Value: 0
14	RX14_MSG_AV	RxMessage Buffer Status Default Value: 0
13	RX13_MSG_AV	RxMessage Buffer Status Default Value: 0
12	RX12_MSG_AV	RxMessage Buffer Status Default Value: 0
11	RX11_MSG_AV	RxMessage Buffer Status Default Value: 0
10	RX10_MSG_AV	RxMessage Buffer Status Default Value: 0
9	RX9_MSG_AV	RxMessage Buffer Status Default Value: 0
8	RX8_MSG_AV	RxMessage Buffer Status Default Value: 0
7	RX7_MSG_AV	RxMessage Buffer Status Default Value: 0
6	RX6_MSG_AV	RxMessage Buffer Status Default Value: 0
5	RX5_MSG_AV	RxMessage Buffer Status Default Value: 0
4	RX4_MSG_AV	RxMessage Buffer Status Default Value: 0
3	RX3_MSG_AV	RxMessage Buffer Status Default Value: 0
2	RX2_MSG_AV	RxMessage Buffer Status Default Value: 0
1	RX1_MSG_AV	RxMessage Buffer Status Default Value: 0
0	RX0_MSG_AV	RxMessage Buffer Status Default Value: 0

2.1.20 CAN1_ERROR_STATUS

CAN Error Status

Address: 0x402F000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TX_ERR_CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RX_ERR_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R	R	R	
HW Access	None				RW	RW	RW	
Name	None [23:20]				RXGTE96	TXGTE96	ERROR_STATE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	RXGTE96	The Rx error counter is greater or equal 96 Default Value: 0
18	TXGTE96	The Tx error counter is greater or equal 96 Default Value: 0
17 : 16	ERROR_STATE	The error state of the CAN node: 00: error active (normal operation) 01: error passive 1x: bus off Default Value: 0
15 : 8	RX_ERR_CNT	The receive error counter according to the CAN 2.0 specification. When in bus-off state, this counter is used to count 128 groups of 11 recessive bits. it is fixed at 255 Default Value: 0

2.1.20 CAN1_ERROR_STATUS (continued)

7 : 0	TX_ERR_CNT	The transmitter error counter according to the CAN standard. When it is greater than 255, it is fixed at 255 Default Value: 0

2.1.21 CAN1_COMMAND

CAN Command Register

Address: 0x402F0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				SRAM_TEST	LOOPBACK_TEST	LISTEN	RUN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	IP_REV_NUMBER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	R				R			
Name	IP_MAJOR_VERSION [31:28]				IP_MINOR_VERSION [27:24]			

Bits	Name	Description
31 : 28	IP_MAJOR_VERSION	IP Major Version Number Default Value: 3
27 : 24	IP_MINOR_VERSION	IP Minor Version Number Default Value: 0
23 : 16	IP_REV_NUMBER	IP Revision Number Default Value: 0
3	SRAM_TEST	Reserved
2	LOOPBACK_TEST	Reserved
1	LISTEN	TEST_MODE[1] Default Value: 0
0	RUN	Reserved

2.1.22 CAN1_CONFIG

CAN Configuration

Address: 0x402F0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW	RW		RW	RW
HW Access	R			R	R		R	R
Name	CFG_TSEG2 [7:5]			AUTO_RESTART	CFG_SJW [3:2]		SAMPLING_MODE	EDGE_MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW	RW	RW			
HW Access	None	R	R	R	R			
Name	None	ECR_MODE	SWAP_ENDIAN	CFG_ARBITER	CFG_TSEG1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CFG_BITRATE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	CFG_BITRATE [30:24]						

Bits	Name	Description
30 : 16	CFG_BITRATE	Prescaler for generating the time quantum which defines the TQ: 0: One time quantum equals 1 clock cycle 1: One time quantum equals 2 clock cycles ... 32767: One time quantum equals 32768 clock cycles Default Value: 0
14	ECR_MODE	Error Capture mode 0: Free running: The ECR register shows the current bit position within the CAN frame 1: Capture mode: The ecr register shows the bit position and type of the last captured CAN error. Default Value: 0
13	SWAP_ENDIAN	Swap Endian - the byte position of the CAN receive and transmit data fields can be modified to match the endian setting of the processor or the used CAN protocol 0: CAN data byte position is not swapped (big endian) 1: CAN data byte position is swapped (little endian) Default Value: 0

2.1.22 CAN1_CONFIG (continued)

12	CFG_ARBITER	Transmit buffer arbiter ¡®0¡¯: Round robin arbitration ¡®1¡¯: Fixed priority arbitration Default Value: 0
11 : 8	CFG_TSEG1	Time segment 1 Length of the first time segment: tseg1 = cfg_tseg1 + 1 Time segment 1 includes the propagation time. cfg_tseg1=0 and cfg_tseg1=1 are not allowed. Default Value: 0
7 : 5	CFG_TSEG2	Time segment 2 Length of the second time segment: tseg2 = cfg_tseg2 + 1 cfg_tseg2=0 is not allowed; cfg_tseg2=1 is only allowed in direct sampling mode. Default Value: 0
4	AUTO_RESTART	¡®0¡¯: After bus-off, the CAN core must be restarted by setting COMMAND.RUN register. This is the recommended setting. ¡®1¡¯: After bus-off, the CAN core is restarting automatically after 128 groups of 11 recessive bits Default Value: 0
3 : 2	CFG_SJW	Synchronization jump width - 1 sjw ¡Ü tseg1 and sjw ¡Ü tseg2 Default Value: 0
1	SAMPLING_MODE	CAN bus bit sampling ¡®0¡¯: One sampling point is used in the receiver path ¡®1¡¯: 3 sampling points with majority decision are used Default Value: 0
0	EDGE_MODE	CAN bus synchronization logic ¡®0¡¯: Edge from ¡®R¡¯ to ¡®D¡¯ is used for synchronization ¡®1¡¯: Both edges are used Note, only ¡®R¡¯ to ¡®D¡¯ edge shall be used for synchronization per ISO-11898-1 spec, so this bit should always be set 0 (by default) Default Value: 0

2.1.23 CAN1_ECR

Error Capture Register

Address: 0x402F0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R	R	R			RW
HW Access	RW		RW	RW	RW			RW
Name	BIT [7:6]		TX_MODE	RX_MODE	ERROR_TYPE [3:1]			ECR_STATUS

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	Field [15:12]				BIT [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							RW
Name	None [23:17]							Field

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

2.1.23 CAN1_ECR (continued)

16 : 12	Field	Field - 0x00 : Stopped 0x01 : Synchronize 0x05 : Interframe 0x06 : Bus Idle 0x07 : Start of Frame 0x08 : Arbitration 0x09 : Control 0x0A : Data 0x0B : CRC 0x0C : ACK 0x0D : End of frame 0x10 : Error flag 0x11 : Error echo 0x12 : Error delimiter 0x18 : Overload flag 0x19 : Overload echo 0x1A : Overload delimiter Others : N/A Default Value: 0
11 : 6	BIT	Bit number inside of Field Default Value: 0
5	TX_MODE	TX Mode - 0: No status 1: CAN Controller is transmitter Default Value: 0
4	RX_MODE	RX Mode - 0: No status 1: CAN Controller is receiver Default Value: 0
3 : 1	ERROR_TYPE	Error type - 000 : Arbitration loss 001 : Bit Error 010 : Bit Stuffing Error 011 : Acknowledge Error 100 : Form Error 101 : CRC Error Others : N/A Default Value: 0
0	ECR_STATUS	ECR STATUS - 0: ECR register captured an error, or it is in free running mode 1: ECR register is armed Default Value: 0

2.1.24 CAN1_CNTL

Control

Address: 0x402F0400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TT_ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	IP_ENABLE	None [30:24]						

Bits	Name	Description
31	IP_ENABLE	IP Enable/Disable 0=IP is disabled/reset 1=IP is enabled/running Default Value: 0
0	TT_ENABLE	TTCAN enable/disable 0=TTCAN is disabled; Interrupt_can is sourced from 3PIP. INT_EBL.GLOBAL_INT_ENBL & (INT_EBL[i] & INT_STATUS[i]) 1=TTCAN is enabled; Interrupt_can is sourced from INTR_CAN_MASKED. Default Value: 0

2.1.25 CAN1_TTCAN_COUNTER

TTCAN Level1 16-Bit local time counter

Address: 0x402F0404

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	LOCAL_TIME [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	LOCAL_TIME [31:24]							

Bits	Name	Description
31 : 16	LOCAL_TIME	Bit time counter in TTCAN level 1 Default Value: 0

2.1.26 CAN1_TTCAN_COMPARE

TTCAN Level1 compare configuration

Address: 0x402F0408

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TIME_MARK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TIME_MARK [31:24]							

Bits	Name	Description
31 : 16	TIME_MARK	compare target, when TTCAN_COUNTER.LOCAL_TIME counts to TT_COMPARE, INTR_CAN.TT_COMPARE will be set Default Value: 65535

2.1.27 CAN1_TTCAN_CAPTURE

TTCAN Level1 capture configuration

Address: 0x402F040C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SYNC_MARK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SYNC_MARK [31:24]							

Bits	Name	Description
31 : 16	SYNC_MARK	copy TTCAN_COUNTER.LOCAL_TIME to TTCAN_CAPTURE.SYNC_MARK, when SOF detected. when new event triggers, new LOCAL_TIME value will overwrite previous SYNC_MARK value Default Value: 0

2.1.28 CAN1_TTCAN_TIMING

TTCAN Level1 timing configuration, duplicate of CONFIG fields

Address: 0x402F0410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			None			RW	None
HW Access	R			None			R	None
Name	CFG_TSEG2 [7:5]			None [4:2]			SAMPLING_MODE	None

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				CFG_TSEG1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CFG_BITRATE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	CFG_BITRATE [30:24]						

Bits	Name	Description
30 : 16	CFG_BITRATE	Prescaler for generating the time quantum which defines the TQ: 0: One time quantum equals 1 clock cycle 1: One time quantum equals 2 clock cycles ... 32767: One time quantum equals 32768 clock cycles Default Value: 0
11 : 8	CFG_TSEG1	Time segment 1 Length of the first time segment: tseg1 = cfg_tseg1 + 1 Time segment 1 includes the propagation time. cfg_tseg1=0 and cfg_tseg1=1 are not allowed. Default Value: 0

2.1.28 CAN1_TTCAN_TIMING (continued)

7 : 5	CFG_TSEG2	Time segment 2 Length of the second time segment: tseg2 = cfg_tseg2 + 1 cfg_tseg2=0 is not allowed; cfg_tseg2=1 is only allowed in direct sampling mode. Default Value: 0
1	SAMPLING_MODE	CAN bus bit sampling ¡®0¡¯: One sampling point is used in the receiver path ¡®1¡¯: 3 sampling points with majority decision are used Default Value: 0

2.1.29 CAN1_INTR_CAN

CAN Interrupt Cause (TTCAN + INT_STATUS Or)

Address: 0x402F0414

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [7:3]					TT_CAPTURE	TT_COMPARE	INT_STATUS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	TT_CAPTURE	Triggers when LOCAL_TIME is saved to TT_CAPTURE, on SOF detection Default Value: 0
1	TT_COMPARE	Triggers when LOCAL_TIME is equal to TT_COMPARE Default Value: 0
0	INT_STATUS	Triggers when any enabled (INT_EBL) interrupt are set in INT_STATUS Default Value: 0

2.1.30 CAN1_INTR_CAN_SET

CAN Interrupt Set (TTCAN + INT_STATUS Or)

Address: 0x402F0418

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					TT_CAPTURE	TT_COMPARE	INT_STATUS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	TT_CAPTURE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	TT_COMPARE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	INT_STATUS	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

2.1.31 CAN1_INTR_CAN_MASK

CAN Interrupt Mask (TTCAN + INT_STATUS Or)

Address: 0x402F041C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					TT_CAPTURE	TT_COMPARE	INT_STATUS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	TT_CAPTURE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	TT_COMPARE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	INT_STATUS	Mask bit for corresponding bit in interrupt request register. Default Value: 0

2.1.32 CAN1_INTR_CAN_MASKED

Can Interrupt Masked (TTCAN + INT_STATUS Or)

Address: 0x402F0420

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					TT_CAPTURE	TT_COMPARE	INT_STATUS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	TT_CAPTURE	Logical and of corresponding request and mask bits. Default Value: 0
1	TT_COMPARE	Logical and of corresponding request and mask bits. Default Value: 0
0	INT_STATUS	Logical and of corresponding request and mask bits. Default Value: 0

3 CAN_RX Registers

This section discusses the CAN_RX registers. It lists all the registers in mapping tables, in address order.

3.1 Register Details

Register Name	Address
CAN0_CAN_RX0_CONTROL	0x402E00A0
CAN0_CAN_RX0_ID	0x402E00A4
CAN0_CAN_RX0_DATA_HIGH	0x402E00A8
CAN0_CAN_RX0_DATA_LOW	0x402E00AC
CAN0_CAN_RX0_AMR	0x402E00B0
CAN0_CAN_RX0_ACR	0x402E00B4
CAN0_CAN_RX0_AMR_DATA	0x402E00B8
CAN0_CAN_RX0_ACR_DATA	0x402E00BC
CAN0_CAN_RX1_CONTROL	0x402E00C0
CAN0_CAN_RX1_ID	0x402E00C4
CAN0_CAN_RX1_DATA_HIGH	0x402E00C8
CAN0_CAN_RX1_DATA_LOW	0x402E00CC
CAN0_CAN_RX1_AMR	0x402E00D0
CAN0_CAN_RX1_ACR	0x402E00D4
CAN0_CAN_RX1_AMR_DATA	0x402E00D8
CAN0_CAN_RX1_ACR_DATA	0x402E00DC
CAN0_CAN_RX2_CONTROL	0x402E00E0
CAN0_CAN_RX2_ID	0x402E00E4
CAN0_CAN_RX2_DATA_HIGH	0x402E00E8
CAN0_CAN_RX2_DATA_LOW	0x402E00EC
CAN0_CAN_RX2_AMR	0x402E00F0
CAN0_CAN_RX2_ACR	0x402E00F4
CAN0_CAN_RX2_AMR_DATA	0x402E00F8
CAN0_CAN_RX2_ACR_DATA	0x402E00FC
CAN0_CAN_RX3_CONTROL	0x402E0100
CAN0_CAN_RX3_ID	0x402E0104
CAN0_CAN_RX3_DATA_HIGH	0x402E0108

Register Name	Address
CAN0_CAN_RX3_DATA_LOW	0x402E010C
CAN0_CAN_RX3_AMR	0x402E0110
CAN0_CAN_RX3_ACR	0x402E0114
CAN0_CAN_RX3_AMR_DATA	0x402E0118
CAN0_CAN_RX3_ACR_DATA	0x402E011C
CAN0_CAN_RX4_CONTROL	0x402E0120
CAN0_CAN_RX4_ID	0x402E0124
CAN0_CAN_RX4_DATA_HIGH	0x402E0128
CAN0_CAN_RX4_DATA_LOW	0x402E012C
CAN0_CAN_RX4_AMR	0x402E0130
CAN0_CAN_RX4_ACR	0x402E0134
CAN0_CAN_RX4_AMR_DATA	0x402E0138
CAN0_CAN_RX4_ACR_DATA	0x402E013C
CAN0_CAN_RX5_CONTROL	0x402E0140
CAN0_CAN_RX5_ID	0x402E0144
CAN0_CAN_RX5_DATA_HIGH	0x402E0148
CAN0_CAN_RX5_DATA_LOW	0x402E014C
CAN0_CAN_RX5_AMR	0x402E0150
CAN0_CAN_RX5_ACR	0x402E0154
CAN0_CAN_RX5_AMR_DATA	0x402E0158
CAN0_CAN_RX5_ACR_DATA	0x402E015C
CAN0_CAN_RX6_CONTROL	0x402E0160
CAN0_CAN_RX6_ID	0x402E0164
CAN0_CAN_RX6_DATA_HIGH	0x402E0168
CAN0_CAN_RX6_DATA_LOW	0x402E016C
CAN0_CAN_RX6_AMR	0x402E0170
CAN0_CAN_RX6_ACR	0x402E0174
CAN0_CAN_RX6_AMR_DATA	0x402E0178
CAN0_CAN_RX6_ACR_DATA	0x402E017C
CAN0_CAN_RX7_CONTROL	0x402E0180
CAN0_CAN_RX7_ID	0x402E0184
CAN0_CAN_RX7_DATA_HIGH	0x402E0188
CAN0_CAN_RX7_DATA_LOW	0x402E018C
CAN0_CAN_RX7_AMR	0x402E0190
CAN0_CAN_RX7_ACR	0x402E0194
CAN0_CAN_RX7_AMR_DATA	0x402E0198
CAN0_CAN_RX7_ACR_DATA	0x402E019C
CAN0_CAN_RX8_CONTROL	0x402E01A0
CAN0_CAN_RX8_ID	0x402E01A4
CAN0_CAN_RX8_DATA_HIGH	0x402E01A8
CAN0_CAN_RX8_DATA_LOW	0x402E01AC
CAN0_CAN_RX8_AMR	0x402E01B0

Register Name	Address
CAN0_CAN_RX8_ACR	0x402E01B4
CAN0_CAN_RX8_AMR_DATA	0x402E01B8
CAN0_CAN_RX8_ACR_DATA	0x402E01BC
CAN0_CAN_RX9_CONTROL	0x402E01C0
CAN0_CAN_RX9_ID	0x402E01C4
CAN0_CAN_RX9_DATA_HIGH	0x402E01C8
CAN0_CAN_RX9_DATA_LOW	0x402E01CC
CAN0_CAN_RX9_AMR	0x402E01D0
CAN0_CAN_RX9_ACR	0x402E01D4
CAN0_CAN_RX9_AMR_DATA	0x402E01D8
CAN0_CAN_RX9_ACR_DATA	0x402E01DC
CAN0_CAN_RX10_CONTROL	0x402E01E0
CAN0_CAN_RX10_ID	0x402E01E4
CAN0_CAN_RX10_DATA_HIGH	0x402E01E8
CAN0_CAN_RX10_DATA_LOW	0x402E01EC
CAN0_CAN_RX10_AMR	0x402E01F0
CAN0_CAN_RX10_ACR	0x402E01F4
CAN0_CAN_RX10_AMR_DATA	0x402E01F8
CAN0_CAN_RX10_ACR_DATA	0x402E01FC
CAN0_CAN_RX11_CONTROL	0x402E0200
CAN0_CAN_RX11_ID	0x402E0204
CAN0_CAN_RX11_DATA_HIGH	0x402E0208
CAN0_CAN_RX11_DATA_LOW	0x402E020C
CAN0_CAN_RX11_AMR	0x402E0210
CAN0_CAN_RX11_ACR	0x402E0214
CAN0_CAN_RX11_AMR_DATA	0x402E0218
CAN0_CAN_RX11_ACR_DATA	0x402E021C
CAN0_CAN_RX12_CONTROL	0x402E0220
CAN0_CAN_RX12_ID	0x402E0224
CAN0_CAN_RX12_DATA_HIGH	0x402E0228
CAN0_CAN_RX12_DATA_LOW	0x402E022C
CAN0_CAN_RX12_AMR	0x402E0230
CAN0_CAN_RX12_ACR	0x402E0234
CAN0_CAN_RX12_AMR_DATA	0x402E0238
CAN0_CAN_RX12_ACR_DATA	0x402E023C
CAN0_CAN_RX13_CONTROL	0x402E0240
CAN0_CAN_RX13_ID	0x402E0244
CAN0_CAN_RX13_DATA_HIGH	0x402E0248
CAN0_CAN_RX13_DATA_LOW	0x402E024C
CAN0_CAN_RX13_AMR	0x402E0250
CAN0_CAN_RX13_ACR	0x402E0254
CAN0_CAN_RX13_AMR_DATA	0x402E0258

Register Name	Address
CAN0_CAN_RX13_ACR_DATA	0x402E025C
CAN0_CAN_RX14_CONTROL	0x402E0260
CAN0_CAN_RX14_ID	0x402E0264
CAN0_CAN_RX14_DATA_HIGH	0x402E0268
CAN0_CAN_RX14_DATA_LOW	0x402E026C
CAN0_CAN_RX14_AMR	0x402E0270
CAN0_CAN_RX14_ACR	0x402E0274
CAN0_CAN_RX14_AMR_DATA	0x402E0278
CAN0_CAN_RX14_ACR_DATA	0x402E027C
CAN0_CAN_RX15_CONTROL	0x402E0280
CAN0_CAN_RX15_ID	0x402E0284
CAN0_CAN_RX15_DATA_HIGH	0x402E0288
CAN0_CAN_RX15_DATA_LOW	0x402E028C
CAN0_CAN_RX15_AMR	0x402E0290
CAN0_CAN_RX15_ACR	0x402E0294
CAN0_CAN_RX15_AMR_DATA	0x402E0298
CAN0_CAN_RX15_ACR_DATA	0x402E029C
CAN1_CAN_RX0_CONTROL	0x402F00A0
CAN1_CAN_RX0_ID	0x402F00A4
CAN1_CAN_RX0_DATA_HIGH	0x402F00A8
CAN1_CAN_RX0_DATA_LOW	0x402F00AC
CAN1_CAN_RX0_AMR	0x402F00B0
CAN1_CAN_RX0_ACR	0x402F00B4
CAN1_CAN_RX0_AMR_DATA	0x402F00B8
CAN1_CAN_RX0_ACR_DATA	0x402F00BC
CAN1_CAN_RX1_CONTROL	0x402F00C0
CAN1_CAN_RX1_ID	0x402F00C4
CAN1_CAN_RX1_DATA_HIGH	0x402F00C8
CAN1_CAN_RX1_DATA_LOW	0x402F00CC
CAN1_CAN_RX1_AMR	0x402F00D0
CAN1_CAN_RX1_ACR	0x402F00D4
CAN1_CAN_RX1_AMR_DATA	0x402F00D8
CAN1_CAN_RX1_ACR_DATA	0x402F00DC
CAN1_CAN_RX2_CONTROL	0x402F00E0
CAN1_CAN_RX2_ID	0x402F00E4
CAN1_CAN_RX2_DATA_HIGH	0x402F00E8
CAN1_CAN_RX2_DATA_LOW	0x402F00EC
CAN1_CAN_RX2_AMR	0x402F00F0
CAN1_CAN_RX2_ACR	0x402F00F4
CAN1_CAN_RX2_AMR_DATA	0x402F00F8
CAN1_CAN_RX2_ACR_DATA	0x402F00FC
CAN1_CAN_RX3_CONTROL	0x402F0100

Register Name	Address
CAN1_CAN_RX3_ID	0x402F0104
CAN1_CAN_RX3_DATA_HIGH	0x402F0108
CAN1_CAN_RX3_DATA_LOW	0x402F010C
CAN1_CAN_RX3_AMR	0x402F0110
CAN1_CAN_RX3_ACR	0x402F0114
CAN1_CAN_RX3_AMR_DATA	0x402F0118
CAN1_CAN_RX3_ACR_DATA	0x402F011C
CAN1_CAN_RX4_CONTROL	0x402F0120
CAN1_CAN_RX4_ID	0x402F0124
CAN1_CAN_RX4_DATA_HIGH	0x402F0128
CAN1_CAN_RX4_DATA_LOW	0x402F012C
CAN1_CAN_RX4_AMR	0x402F0130
CAN1_CAN_RX4_ACR	0x402F0134
CAN1_CAN_RX4_AMR_DATA	0x402F0138
CAN1_CAN_RX4_ACR_DATA	0x402F013C
CAN1_CAN_RX5_CONTROL	0x402F0140
CAN1_CAN_RX5_ID	0x402F0144
CAN1_CAN_RX5_DATA_HIGH	0x402F0148
CAN1_CAN_RX5_DATA_LOW	0x402F014C
CAN1_CAN_RX5_AMR	0x402F0150
CAN1_CAN_RX5_ACR	0x402F0154
CAN1_CAN_RX5_AMR_DATA	0x402F0158
CAN1_CAN_RX5_ACR_DATA	0x402F015C
CAN1_CAN_RX6_CONTROL	0x402F0160
CAN1_CAN_RX6_ID	0x402F0164
CAN1_CAN_RX6_DATA_HIGH	0x402F0168
CAN1_CAN_RX6_DATA_LOW	0x402F016C
CAN1_CAN_RX6_AMR	0x402F0170
CAN1_CAN_RX6_ACR	0x402F0174
CAN1_CAN_RX6_AMR_DATA	0x402F0178
CAN1_CAN_RX6_ACR_DATA	0x402F017C
CAN1_CAN_RX7_CONTROL	0x402F0180
CAN1_CAN_RX7_ID	0x402F0184
CAN1_CAN_RX7_DATA_HIGH	0x402F0188
CAN1_CAN_RX7_DATA_LOW	0x402F018C
CAN1_CAN_RX7_AMR	0x402F0190
CAN1_CAN_RX7_ACR	0x402F0194
CAN1_CAN_RX7_AMR_DATA	0x402F0198
CAN1_CAN_RX7_ACR_DATA	0x402F019C
CAN1_CAN_RX8_CONTROL	0x402F01A0
CAN1_CAN_RX8_ID	0x402F01A4
CAN1_CAN_RX8_DATA_HIGH	0x402F01A8

Register Name	Address
CAN1_CAN_RX8_DATA_LOW	0x402F01AC
CAN1_CAN_RX8_AMR	0x402F01B0
CAN1_CAN_RX8_ACR	0x402F01B4
CAN1_CAN_RX8_AMR_DATA	0x402F01B8
CAN1_CAN_RX8_ACR_DATA	0x402F01BC
CAN1_CAN_RX9_CONTROL	0x402F01C0
CAN1_CAN_RX9_ID	0x402F01C4
CAN1_CAN_RX9_DATA_HIGH	0x402F01C8
CAN1_CAN_RX9_DATA_LOW	0x402F01CC
CAN1_CAN_RX9_AMR	0x402F01D0
CAN1_CAN_RX9_ACR	0x402F01D4
CAN1_CAN_RX9_AMR_DATA	0x402F01D8
CAN1_CAN_RX9_ACR_DATA	0x402F01DC
CAN1_CAN_RX10_CONTROL	0x402F01E0
CAN1_CAN_RX10_ID	0x402F01E4
CAN1_CAN_RX10_DATA_HIGH	0x402F01E8
CAN1_CAN_RX10_DATA_LOW	0x402F01EC
CAN1_CAN_RX10_AMR	0x402F01F0
CAN1_CAN_RX10_ACR	0x402F01F4
CAN1_CAN_RX10_AMR_DATA	0x402F01F8
CAN1_CAN_RX10_ACR_DATA	0x402F01FC
CAN1_CAN_RX11_CONTROL	0x402F0200
CAN1_CAN_RX11_ID	0x402F0204
CAN1_CAN_RX11_DATA_HIGH	0x402F0208
CAN1_CAN_RX11_DATA_LOW	0x402F020C
CAN1_CAN_RX11_AMR	0x402F0210
CAN1_CAN_RX11_ACR	0x402F0214
CAN1_CAN_RX11_AMR_DATA	0x402F0218
CAN1_CAN_RX11_ACR_DATA	0x402F021C
CAN1_CAN_RX12_CONTROL	0x402F0220
CAN1_CAN_RX12_ID	0x402F0224
CAN1_CAN_RX12_DATA_HIGH	0x402F0228
CAN1_CAN_RX12_DATA_LOW	0x402F022C
CAN1_CAN_RX12_AMR	0x402F0230
CAN1_CAN_RX12_ACR	0x402F0234
CAN1_CAN_RX12_AMR_DATA	0x402F0238
CAN1_CAN_RX12_ACR_DATA	0x402F023C
CAN1_CAN_RX13_CONTROL	0x402F0240
CAN1_CAN_RX13_ID	0x402F0244
CAN1_CAN_RX13_DATA_HIGH	0x402F0248
CAN1_CAN_RX13_DATA_LOW	0x402F024C
CAN1_CAN_RX13_AMR	0x402F0250

Register Name	Address
CAN1_CAN_RX13_ACR	0x402F0254
CAN1_CAN_RX13_AMR_DATA	0x402F0258
CAN1_CAN_RX13_ACR_DATA	0x402F025C
CAN1_CAN_RX14_CONTROL	0x402F0260
CAN1_CAN_RX14_ID	0x402F0264
CAN1_CAN_RX14_DATA_HIGH	0x402F0268
CAN1_CAN_RX14_DATA_LOW	0x402F026C
CAN1_CAN_RX14_AMR	0x402F0270
CAN1_CAN_RX14_ACR	0x402F0274
CAN1_CAN_RX14_AMR_DATA	0x402F0278
CAN1_CAN_RX14_ACR_DATA	0x402F027C
CAN1_CAN_RX15_CONTROL	0x402F0280
CAN1_CAN_RX15_ID	0x402F0284
CAN1_CAN_RX15_DATA_HIGH	0x402F0288
CAN1_CAN_RX15_DATA_LOW	0x402F028C
CAN1_CAN_RX15_AMR	0x402F0290
CAN1_CAN_RX15_ACR	0x402F0294
CAN1_CAN_RX15_AMR_DATA	0x402F0298
CAN1_CAN_RX15_ACR_DATA	0x402F029C

3.1.1 CAN0_CAN_RX0_CONTROL

RxMessage Buffer control/command

Address: 0x402E00A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.1 CAN0_CAN_RX0_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.1 CAN0_CAN_RX0_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.2 CAN0_CAN_RX0_ID

Identifier

Address: 0x402E00A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.3 CAN0_CAN_RX0_DATA_HIGH

RxMessage Data high

Address: 0x402E00A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.4 CAN0_CAN_RX0_DATA_LOW

RxMessage Data low

Address: 0x402E00AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.5 CAN0_CAN_RX0_AMR

Acceptance Mask Register

Address: 0x402E00B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.6 CAN0_CAN_RX0_ACR

Acceptance Code Register

Address: 0x402E00B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.7 CAN0_CAN_RX0_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402E00B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.8 CAN0_CAN_RX0_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402E00BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.9 CAN0_CAN_RX1_CONTROL

RxMessage Buffer control/command

Address: 0x402E00C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.9 CAN0_CAN_RX1_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.9 CAN0_CAN_RX1_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.10 CAN0_CAN_RX1_ID

Identifier

Address: 0x402E00C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.11 CAN0_CAN_RX1_DATA_HIGH

RxMessage Data high

Address: 0x402E00C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.12 CAN0_CAN_RX1_DATA_LOW

RxMessage Data low

Address: 0x402E00CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.13 CAN0_CAN_RX1_AMR

Acceptance Mask Register

Address: 0x402E00D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.14 CAN0_CAN_RX1_ACR

Acceptance Code Register

Address: 0x402E00D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.15 CAN0_CAN_RX1_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402E00D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.16 CAN0_CAN_RX1_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402E00DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.17 CAN0_CAN_RX2_CONTROL

RxMessage Buffer control/command

Address: 0x402E00E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.17 CAN0_CAN_RX2_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.17 CAN0_CAN_RX2_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.18 CAN0_CAN_RX2_ID

Identifier

Address: 0x402E00E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.19 CAN0_CAN_RX2_DATA_HIGH

RxMessage Data high

Address: 0x402E00E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.20 CAN0_CAN_RX2_DATA_LOW

RxMessage Data low

Address: 0x402E00EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.21 CAN0_CAN_RX2_AMR

Acceptance Mask Register

Address: 0x402E00F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.22 CAN0_CAN_RX2_ACR

Acceptance Code Register

Address: 0x402E00F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.23 CAN0_CAN_RX2_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402E00F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.24 CAN0_CAN_RX2_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402E00FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.25 CAN0_CAN_RX3_CONTROL

RxMessage Buffer control/command

Address: 0x402E0100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.25 CAN0_CAN_RX3_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.25 CAN0_CAN_RX3_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.26 CAN0_CAN_RX3_ID

Identifier

Address: 0x402E0104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.27 CAN0_CAN_RX3_DATA_HIGH

RxMessage Data high

Address: 0x402E0108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.28 CAN0_CAN_RX3_DATA_LOW

RxMessage Data low

Address: 0x402E010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.29 CAN0_CAN_RX3_AMR

Acceptance Mask Register

Address: 0x402E0110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.30 CAN0_CAN_RX3_ACR

Acceptance Code Register

Address: 0x402E0114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.31 CAN0_CAN_RX3_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402E0118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.32 CAN0_CAN_RX3_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402E011C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.33 CAN0_CAN_RX4_CONTROL

RxMessage Buffer control/command

Address: 0x402E0120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.33 CAN0_CAN_RX4_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.33 CAN0_CAN_RX4_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.34 CAN0_CAN_RX4_ID

Identifier

Address: 0x402E0124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.35 CAN0_CAN_RX4_DATA_HIGH

RxMessage Data high

Address: 0x402E0128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.36 CAN0_CAN_RX4_DATA_LOW

RxMessage Data low

Address: 0x402E012C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.37 CAN0_CAN_RX4_AMR

Acceptance Mask Register

Address: 0x402E0130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.38 CAN0_CAN_RX4_ACR

Acceptance Code Register

Address: 0x402E0134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.39 CAN0_CAN_RX4_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402E0138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.40 CAN0_CAN_RX4_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402E013C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.41 CAN0_CAN_RX5_CONTROL

RxMessage Buffer control/command

Address: 0x402E0140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.41 CAN0_CAN_RX5_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.41 CAN0_CAN_RX5_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.42 CAN0_CAN_RX5_ID

Identifier

Address: 0x402E0144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.43 CAN0_CAN_RX5_DATA_HIGH

RxMessage Data high

Address: 0x402E0148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.44 CAN0_CAN_RX5_DATA_LOW

RxMessage Data low

Address: 0x402E014C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.45 CAN0_CAN_RX5_AMR

Acceptance Mask Register

Address: 0x402E0150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.46 CAN0_CAN_RX5_ACR

Acceptance Code Register

Address: 0x402E0154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.47 CAN0_CAN_RX5_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402E0158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.48 CAN0_CAN_RX5_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402E015C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.49 CAN0_CAN_RX6_CONTROL

RxMessage Buffer control/command

Address: 0x402E0160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.49 CAN0_CAN_RX6_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.49 CAN0_CAN_RX6_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.50 CAN0_CAN_RX6_ID

Identifier

Address: 0x402E0164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.51 CAN0_CAN_RX6_DATA_HIGH

RxMessage Data high

Address: 0x402E0168

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.52 CAN0_CAN_RX6_DATA_LOW

RxMessage Data low

Address: 0x402E016C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.53 CAN0_CAN_RX6_AMR

Acceptance Mask Register

Address: 0x402E0170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.54 CAN0_CAN_RX6_ACR

Acceptance Code Register

Address: 0x402E0174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.55 CAN0_CAN_RX6_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402E0178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.56 CAN0_CAN_RX6_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402E017C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.57 CAN0_CAN_RX7_CONTROL

RxMessage Buffer control/command

Address: 0x402E0180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.57 CAN0_CAN_RX7_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.57 CAN0_CAN_RX7_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.58 CAN0_CAN_RX7_ID

Identifier

Address: 0x402E0184

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.59 CAN0_CAN_RX7_DATA_HIGH

RxMessage Data high

Address: 0x402E0188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.60 CAN0_CAN_RX7_DATA_LOW

RxMessage Data low

Address: 0x402E018C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.61 CAN0_CAN_RX7_AMR

Acceptance Mask Register

Address: 0x402E0190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.62 CAN0_CAN_RX7_ACR

Acceptance Code Register

Address: 0x402E0194

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.63 CAN0_CAN_RX7_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402E0198

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.64 CAN0_CAN_RX7_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402E019C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.65 CAN0_CAN_RX8_CONTROL

RxMessage Buffer control/command

Address: 0x402E01A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.65 CAN0_CAN_RX8_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.65 CAN0_CAN_RX8_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.66 CAN0_CAN_RX8_ID

Identifier

Address: 0x402E01A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.67 CAN0_CAN_RX8_DATA_HIGH

RxMessage Data high

Address: 0x402E01A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.68 CAN0_CAN_RX8_DATA_LOW

RxMessage Data low

Address: 0x402E01AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.69 CAN0_CAN_RX8_AMR

Acceptance Mask Register

Address: 0x402E01B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.70 CAN0_CAN_RX8_ACR

Acceptance Code Register

Address: 0x402E01B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.71 CAN0_CAN_RX8_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402E01B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.72 CAN0_CAN_RX8_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402E01BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.73 CAN0_CAN_RX9_CONTROL

RxMessage Buffer control/command

Address: 0x402E01C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.73 CAN0_CAN_RX9_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.73 CAN0_CAN_RX9_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.74 CAN0_CAN_RX9_ID

Identifier

Address: 0x402E01C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.75 CAN0_CAN_RX9_DATA_HIGH

RxMessage Data high

Address: 0x402E01C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.76 CAN0_CAN_RX9_DATA_LOW

RxMessage Data low

Address: 0x402E01CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.77 CAN0_CAN_RX9_AMR

Acceptance Mask Register

Address: 0x402E01D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.78 CAN0_CAN_RX9_ACR

Acceptance Code Register

Address: 0x402E01D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.79 CAN0_CAN_RX9_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402E01D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.80 CAN0_CAN_RX9_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402E01DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.81 CAN0_CAN_RX10_CONTROL

RxMessage Buffer control/command

Address: 0x402E01E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.81 CAN0_CAN_RX10_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.81 CAN0_CAN_RX10_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.82 CAN0_CAN_RX10_ID

Identifier

Address: 0x402E01E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.83 CAN0_CAN_RX10_DATA_HIGH

RxMessage Data high

Address: 0x402E01E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.84 CAN0_CAN_RX10_DATA_LOW

RxMessage Data low

Address: 0x402E01EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.85 CAN0_CAN_RX10_AMR

Acceptance Mask Register

Address: 0x402E01F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.86 CAN0_CAN_RX10_ACR

Acceptance Code Register

Address: 0x402E01F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.87 CAN0_CAN_RX10_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402E01F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.88 CAN0_CAN_RX10_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402E01FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.89 CAN0_CAN_RX11_CONTROL

RxMessage Buffer control/command

Address: 0x402E0200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.89 CAN0_CAN_RX11_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.89 CAN0_CAN_RX11_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.90 CAN0_CAN_RX11_ID

Identifier

Address: 0x402E0204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.91 CAN0_CAN_RX11_DATA_HIGH

RxMessage Data high

Address: 0x402E0208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.92 CAN0_CAN_RX11_DATA_LOW

RxMessage Data low

Address: 0x402E020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.93 CAN0_CAN_RX11_AMR

Acceptance Mask Register

Address: 0x402E0210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.94 CAN0_CAN_RX11_ACR

Acceptance Code Register

Address: 0x402E0214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.95 CAN0_CAN_RX11_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402E0218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.96 CAN0_CAN_RX11_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402E021C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.97 CAN0_CAN_RX12_CONTROL

RxMessage Buffer control/command

Address: 0x402E0220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.97 CAN0_CAN_RX12_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.97 CAN0_CAN_RX12_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.98 CAN0_CAN_RX12_ID

Identifier

Address: 0x402E0224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.99 CAN0_CAN_RX12_DATA_HIGH

RxMessage Data high

Address: 0x402E0228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.100 CAN0_CAN_RX12_DATA_LOW

RxMessage Data low

Address: 0x402E022C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.101 CAN0_CAN_RX12_AMR

Acceptance Mask Register

Address: 0x402E0230

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.102 CAN0_CAN_RX12_ACR

Acceptance Code Register

Address: 0x402E0234

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.103 CAN0_CAN_RX12_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402E0238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.104 CAN0_CAN_RX12_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402E023C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.105 CAN0_CAN_RX13_CONTROL

RxMessage Buffer control/command

Address: 0x402E0240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.105 CAN0_CAN_RX13_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.105 CAN0_CAN_RX13_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.106 CAN0_CAN_RX13_ID

Identifier

Address: 0x402E0244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.107 CAN0_CAN_RX13_DATA_HIGH

RxMessage Data high

Address: 0x402E0248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.108 CAN0_CAN_RX13_DATA_LOW

RxMessage Data low

Address: 0x402E024C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.109 CAN0_CAN_RX13_AMR

Acceptance Mask Register

Address: 0x402E0250

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.110 CAN0_CAN_RX13_ACR

Acceptance Code Register

Address: 0x402E0254

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.111 CAN0_CAN_RX13_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402E0258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.112 CAN0_CAN_RX13_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402E025C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.113 CAN0_CAN_RX14_CONTROL

RxMessage Buffer control/command

Address: 0x402E0260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.113 CAN0_CAN_RX14_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.113 CAN0_CAN_RX14_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.114 CAN0_CAN_RX14_ID

Identifier

Address: 0x402E0264

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.115 CAN0_CAN_RX14_DATA_HIGH

RxMessage Data high

Address: 0x402E0268

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.116 CAN0_CAN_RX14_DATA_LOW

RxMessage Data low

Address: 0x402E026C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.117 CAN0_CAN_RX14_AMR

Acceptance Mask Register

Address: 0x402E0270

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.118 CAN0_CAN_RX14_ACR

Acceptance Code Register

Address: 0x402E0274

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.119 CAN0_CAN_RX14_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402E0278

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.120 CAN0_CAN_RX14_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402E027C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.121 CAN0_CAN_RX15_CONTROL

RxMessage Buffer control/command

Address: 0x402E0280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.121 CAN0_CAN_RX15_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.121 CAN0_CAN_RX15_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.122 CAN0_CAN_RX15_ID

Identifier

Address: 0x402E0284

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.123 CAN0_CAN_RX15_DATA_HIGH

RxMessage Data high

Address: 0x402E0288

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.124 CAN0_CAN_RX15_DATA_LOW

RxMessage Data low

Address: 0x402E028C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.125 CAN0_CAN_RX15_AMR

Acceptance Mask Register

Address: 0x402E0290

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.126 CAN0_CAN_RX15_ACR

Acceptance Code Register

Address: 0x402E0294

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.127 CAN0_CAN_RX15_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402E0298

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.128 CAN0_CAN_RX15_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402E029C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.129 CAN1_CAN_RX0_CONTROL

RxMessage Buffer control/command

Address: 0x402F00A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.129 CAN1_CAN_RX0_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.129 CAN1_CAN_RX0_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.130 CAN1_CAN_RX0_ID

Identifier

Address: 0x402F00A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.131 CAN1_CAN_RX0_DATA_HIGH

RxMessage Data high

Address: 0x402F00A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.132 CAN1_CAN_RX0_DATA_LOW

RxMessage Data low

Address: 0x402F00AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.133 CAN1_CAN_RX0_AMR

Acceptance Mask Register

Address: 0x402F00B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.134 CAN1_CAN_RX0_ACR

Acceptance Code Register

Address: 0x402F00B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.135 CAN1_CAN_RX0_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402F00B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.136 CAN1_CAN_RX0_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402F00BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.137 CAN1_CAN_RX1_CONTROL

RxMessage Buffer control/command

Address: 0x402F00C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.137 CAN1_CAN_RX1_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.137 CAN1_CAN_RX1_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.138 CAN1_CAN_RX1_ID

Identifier

Address: 0x402F00C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.139 CAN1_CAN_RX1_DATA_HIGH

RxMessage Data high

Address: 0x402F00C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.140 CAN1_CAN_RX1_DATA_LOW

RxMessage Data low

Address: 0x402F00CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.141 CAN1_CAN_RX1_AMR

Acceptance Mask Register

Address: 0x402F00D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.142 CAN1_CAN_RX1_ACR

Acceptance Code Register

Address: 0x402F00D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.143 CAN1_CAN_RX1_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402F00D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.144 CAN1_CAN_RX1_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402F00DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.145 CAN1_CAN_RX2_CONTROL

RxMessage Buffer control/command

Address: 0x402F00E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.145 CAN1_CAN_RX2_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.145 CAN1_CAN_RX2_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.146 CAN1_CAN_RX2_ID

Identifier

Address: 0x402F00E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.147 CAN1_CAN_RX2_DATA_HIGH

RxMessage Data high

Address: 0x402F00E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.148 CAN1_CAN_RX2_DATA_LOW

RxMessage Data low

Address: 0x402F00EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.149 CAN1_CAN_RX2_AMR

Acceptance Mask Register

Address: 0x402F00F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.150 CAN1_CAN_RX2_ACR

Acceptance Code Register

Address: 0x402F00F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.151 CAN1_CAN_RX2_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402F00F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.152 CAN1_CAN_RX2_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402F00FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.153 CAN1_CAN_RX3_CONTROL

RxMessage Buffer control/command

Address: 0x402F0100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.153 CAN1_CAN_RX3_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.153 CAN1_CAN_RX3_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.154 CAN1_CAN_RX3_ID

Identifier

Address: 0x402F0104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.155 CAN1_CAN_RX3_DATA_HIGH

RxMessage Data high

Address: 0x402F0108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.156 CAN1_CAN_RX3_DATA_LOW

RxMessage Data low

Address: 0x402F010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.157 CAN1_CAN_RX3_AMR

Acceptance Mask Register

Address: 0x402F0110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.158 CAN1_CAN_RX3_ACR

Acceptance Code Register

Address: 0x402F0114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.159 CAN1_CAN_RX3_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402F0118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.160 CAN1_CAN_RX3_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402F011C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.161 CAN1_CAN_RX4_CONTROL

RxMessage Buffer control/command

Address: 0x402F0120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.161 CAN1_CAN_RX4_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.161 CAN1_CAN_RX4_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.162 CAN1_CAN_RX4_ID

Identifier

Address: 0x402F0124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.163 CAN1_CAN_RX4_DATA_HIGH

RxMessage Data high

Address: 0x402F0128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.164 CAN1_CAN_RX4_DATA_LOW

RxMessage Data low

Address: 0x402F012C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.165 CAN1_CAN_RX4_AMR

Acceptance Mask Register

Address: 0x402F0130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.166 CAN1_CAN_RX4_ACR

Acceptance Code Register

Address: 0x402F0134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.167 CAN1_CAN_RX4_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402F0138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.168 CAN1_CAN_RX4_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402F013C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.169 CAN1_CAN_RX5_CONTROL

RxMessage Buffer control/command

Address: 0x402F0140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.169 CAN1_CAN_RX5_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.169 CAN1_CAN_RX5_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.170 CAN1_CAN_RX5_ID

Identifier

Address: 0x402F0144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.171 CAN1_CAN_RX5_DATA_HIGH

RxMessage Data high

Address: 0x402F0148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.172 CAN1_CAN_RX5_DATA_LOW

RxMessage Data low

Address: 0x402F014C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.173 CAN1_CAN_RX5_AMR

Acceptance Mask Register

Address: 0x402F0150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.174 CAN1_CAN_RX5_ACR

Acceptance Code Register

Address: 0x402F0154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.175 CAN1_CAN_RX5_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402F0158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.176 CAN1_CAN_RX5_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402F015C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.177 CAN1_CAN_RX6_CONTROL

RxMessage Buffer control/command

Address: 0x402F0160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.177 CAN1_CAN_RX6_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.177 CAN1_CAN_RX6_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.178 CAN1_CAN_RX6_ID

Identifier

Address: 0x402F0164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.179 CAN1_CAN_RX6_DATA_HIGH

RxMessage Data high

Address: 0x402F0168

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.180 CAN1_CAN_RX6_DATA_LOW

RxMessage Data low

Address: 0x402F016C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.181 CAN1_CAN_RX6_AMR

Acceptance Mask Register

Address: 0x402F0170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.182 CAN1_CAN_RX6_ACR

Acceptance Code Register

Address: 0x402F0174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.183 CAN1_CAN_RX6_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402F0178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.184 CAN1_CAN_RX6_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402F017C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.185 CAN1_CAN_RX7_CONTROL

RxMessage Buffer control/command

Address: 0x402F0180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.185 CAN1_CAN_RX7_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.185 CAN1_CAN_RX7_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.186 CAN1_CAN_RX7_ID

Identifier

Address: 0x402F0184

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.187 CAN1_CAN_RX7_DATA_HIGH

RxMessage Data high

Address: 0x402F0188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.188 CAN1_CAN_RX7_DATA_LOW

RxMessage Data low

Address: 0x402F018C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.189 CAN1_CAN_RX7_AMR

Acceptance Mask Register

Address: 0x402F0190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.190 CAN1_CAN_RX7_ACR

Acceptance Code Register

Address: 0x402F0194

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.191 CAN1_CAN_RX7_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402F0198

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.192 CAN1_CAN_RX7_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402F019C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.193 CAN1_CAN_RX8_CONTROL

RxMessage Buffer control/command

Address: 0x402F01A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.193 CAN1_CAN_RX8_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.193 CAN1_CAN_RX8_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.194 CAN1_CAN_RX8_ID

Identifier

Address: 0x402F01A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.195 CAN1_CAN_RX8_DATA_HIGH

RxMessage Data high

Address: 0x402F01A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.196 CAN1_CAN_RX8_DATA_LOW

RxMessage Data low

Address: 0x402F01AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.197 CAN1_CAN_RX8_AMR

Acceptance Mask Register

Address: 0x402F01B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.198 CAN1_CAN_RX8_ACR

Acceptance Code Register

Address: 0x402F01B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.199 CAN1_CAN_RX8_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402F01B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.200 CAN1_CAN_RX8_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402F01BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.201 CAN1_CAN_RX9_CONTROL

RxMessage Buffer control/command

Address: 0x402F01C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.201 CAN1_CAN_RX9_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.201 CAN1_CAN_RX9_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.202 CAN1_CAN_RX9_ID

Identifier

Address: 0x402F01C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.203 CAN1_CAN_RX9_DATA_HIGH

RxMessage Data high

Address: 0x402F01C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.204 CAN1_CAN_RX9_DATA_LOW

RxMessage Data low

Address: 0x402F01CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.205 CAN1_CAN_RX9_AMR

Acceptance Mask Register

Address: 0x402F01D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.206 CAN1_CAN_RX9_ACR

Acceptance Code Register

Address: 0x402F01D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.207 CAN1_CAN_RX9_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402F01D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.208 CAN1_CAN_RX9_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402F01DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.209 CAN1_CAN_RX10_CONTROL

RxMessage Buffer control/command

Address: 0x402F01E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.209 CAN1_CAN_RX10_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.209 CAN1_CAN_RX10_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.210 CAN1_CAN_RX10_ID

Identifier

Address: 0x402F01E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.211 CAN1_CAN_RX10_DATA_HIGH

RxMessage Data high

Address: 0x402F01E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.212 CAN1_CAN_RX10_DATA_LOW

RxMessage Data low

Address: 0x402F01EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.213 CAN1_CAN_RX10_AMR

Acceptance Mask Register

Address: 0x402F01F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.214 CAN1_CAN_RX10_ACR

Acceptance Code Register

Address: 0x402F01F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.215 CAN1_CAN_RX10_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402F01F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.216 CAN1_CAN_RX10_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402F01FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.217 CAN1_CAN_RX11_CONTROL

RxMessage Buffer control/command

Address: 0x402F0200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.217 CAN1_CAN_RX11_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.217 CAN1_CAN_RX11_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.218 CAN1_CAN_RX11_ID

Identifier

Address: 0x402F0204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.219 CAN1_CAN_RX11_DATA_HIGH

RxMessage Data high

Address: 0x402F0208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.220 CAN1_CAN_RX11_DATA_LOW

RxMessage Data low

Address: 0x402F020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.221 CAN1_CAN_RX11_AMR

Acceptance Mask Register

Address: 0x402F0210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.222 CAN1_CAN_RX11_ACR

Acceptance Code Register

Address: 0x402F0214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.223 CAN1_CAN_RX11_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402F0218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.224 CAN1_CAN_RX11_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402F021C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.225 CAN1_CAN_RX12_CONTROL

RxMessage Buffer control/command

Address: 0x402F0220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.225 CAN1_CAN_RX12_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.225 CAN1_CAN_RX12_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.226 CAN1_CAN_RX12_ID

Identifier

Address: 0x402F0224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.227 CAN1_CAN_RX12_DATA_HIGH

RxMessage Data high

Address: 0x402F0228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.228 CAN1_CAN_RX12_DATA_LOW

RxMessage Data low

Address: 0x402F022C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.229 CAN1_CAN_RX12_AMR

Acceptance Mask Register

Address: 0x402F0230

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.230 CAN1_CAN_RX12_ACR

Acceptance Code Register

Address: 0x402F0234

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.231 CAN1_CAN_RX12_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402F0238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.232 CAN1_CAN_RX12_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402F023C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.233 CAN1_CAN_RX13_CONTROL

RxMessage Buffer control/command

Address: 0x402F0240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.233 CAN1_CAN_RX13_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.233 CAN1_CAN_RX13_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.234 CAN1_CAN_RX13_ID

Identifier

Address: 0x402F0244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.235 CAN1_CAN_RX13_DATA_HIGH

RxMessage Data high

Address: 0x402F0248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.236 CAN1_CAN_RX13_DATA_LOW

RxMessage Data low

Address: 0x402F024C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.237 CAN1_CAN_RX13_AMR

Acceptance Mask Register

Address: 0x402F0250

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.238 CAN1_CAN_RX13_ACR

Acceptance Code Register

Address: 0x402F0254

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.239 CAN1_CAN_RX13_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402F0258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.240 CAN1_CAN_RX13_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402F025C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.241 CAN1_CAN_RX14_CONTROL

RxMessage Buffer control/command

Address: 0x402F0260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.241 CAN1_CAN_RX14_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.241 CAN1_CAN_RX14_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.242 CAN1_CAN_RX14_ID

Identifier

Address: 0x402F0264

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.243 CAN1_CAN_RX14_DATA_HIGH

RxMessage Data high

Address: 0x402F0268

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.244 CAN1_CAN_RX14_DATA_LOW

RxMessage Data low

Address: 0x402F026C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.245 CAN1_CAN_RX14_AMR

Acceptance Mask Register

Address: 0x402F0270

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.246 CAN1_CAN_RX14_ACR

Acceptance Code Register

Address: 0x402F0274

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.247 CAN1_CAN_RX14_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402F0278

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.248 CAN1_CAN_RX14_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402F027C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3.1.249 CAN1_CAN_RX15_CONTROL

RxMessage Buffer control/command

Address: 0x402F0280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_EBL	RTR_REPLY	BUFFER_EN	RTR_ABORT	RTR_REPLY_PEND	MSG_AV_RTRSent

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

3.1.249 CAN1_CAN_RX15_CONTROL (continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback Default Value: 0
6	LINK_FLAG	Link Flag ¡®0¡¯: This buffer is not linked to the next ¡®1¡¯: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable ¡®0¡¯: Interrupt generation is disabled '1¡¯: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message ¡®0¡¯: Automatic RTR message handling disabled ¡®1¡¯: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable ¡®0¡¯: Buffer is disabled ¡®1¡¯: Buffer is enabled Default Value: 0
2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0

3.1.249 CAN1_CAN_RX15_CONTROL (continued)

1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSent	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

3.1.250 CAN1_CAN_RX15_ID

Identifier

Address: 0x402F0284

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

3.1.251 CAN1_CAN_RX15_DATA_HIGH

RxMessage Data high

Address: 0x402F0288

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

3.1.252 CAN1_CAN_RX15_DATA_LOW

RxMessage Data low

Address: 0x402F028C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.253 CAN1_CAN_RX15_AMR

Acceptance Mask Register

Address: 0x402F0290

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (don¡¯t care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.254 CAN1_CAN_RX15_ACR

Acceptance Code Register

Address: 0x402F0294

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

3.1.255 CAN1_CAN_RX15_AMR_DATA

Acceptance Mask Register ¨C Data

Address: 0x402F0298

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (don¡¯t care) Default Value: Undefined

3.1.256 CAN1_CAN_RX15_ACR_DATA

Acceptance Code Register ¨C Data

Address: 0x402F029C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

4 CAN_TX Registers

This section discusses the CAN_TX registers. It lists all the registers in mapping tables, in address order.

4.1 Register Details

Register Name	Address
CAN0_CAN_TX0_CONTROL	0x402E0020
CAN0_CAN_TX0_ID	0x402E0024
CAN0_CAN_TX0_DATA_HIGH	0x402E0028
CAN0_CAN_TX0_DATA_LOW	0x402E002C
CAN0_CAN_TX1_CONTROL	0x402E0030
CAN0_CAN_TX1_ID	0x402E0034
CAN0_CAN_TX1_DATA_HIGH	0x402E0038
CAN0_CAN_TX1_DATA_LOW	0x402E003C
CAN0_CAN_TX2_CONTROL	0x402E0040
CAN0_CAN_TX2_ID	0x402E0044
CAN0_CAN_TX2_DATA_HIGH	0x402E0048
CAN0_CAN_TX2_DATA_LOW	0x402E004C
CAN0_CAN_TX3_CONTROL	0x402E0050
CAN0_CAN_TX3_ID	0x402E0054
CAN0_CAN_TX3_DATA_HIGH	0x402E0058
CAN0_CAN_TX3_DATA_LOW	0x402E005C
CAN0_CAN_TX4_CONTROL	0x402E0060
CAN0_CAN_TX4_ID	0x402E0064
CAN0_CAN_TX4_DATA_HIGH	0x402E0068
CAN0_CAN_TX4_DATA_LOW	0x402E006C
CAN0_CAN_TX5_CONTROL	0x402E0070
CAN0_CAN_TX5_ID	0x402E0074
CAN0_CAN_TX5_DATA_HIGH	0x402E0078
CAN0_CAN_TX5_DATA_LOW	0x402E007C
CAN0_CAN_TX6_CONTROL	0x402E0080
CAN0_CAN_TX6_ID	0x402E0084
CAN0_CAN_TX6_DATA_HIGH	0x402E0088

Register Name	Address
CAN0_CAN_TX6_DATA_LOW	0x402E008C
CAN0_CAN_TX7_CONTROL	0x402E0090
CAN0_CAN_TX7_ID	0x402E0094
CAN0_CAN_TX7_DATA_HIGH	0x402E0098
CAN0_CAN_TX7_DATA_LOW	0x402E009C
CAN1_CAN_TX0_CONTROL	0x402F0020
CAN1_CAN_TX0_ID	0x402F0024
CAN1_CAN_TX0_DATA_HIGH	0x402F0028
CAN1_CAN_TX0_DATA_LOW	0x402F002C
CAN1_CAN_TX1_CONTROL	0x402F0030
CAN1_CAN_TX1_ID	0x402F0034
CAN1_CAN_TX1_DATA_HIGH	0x402F0038
CAN1_CAN_TX1_DATA_LOW	0x402F003C
CAN1_CAN_TX2_CONTROL	0x402F0040
CAN1_CAN_TX2_ID	0x402F0044
CAN1_CAN_TX2_DATA_HIGH	0x402F0048
CAN1_CAN_TX2_DATA_LOW	0x402F004C
CAN1_CAN_TX3_CONTROL	0x402F0050
CAN1_CAN_TX3_ID	0x402F0054
CAN1_CAN_TX3_DATA_HIGH	0x402F0058
CAN1_CAN_TX3_DATA_LOW	0x402F005C
CAN1_CAN_TX4_CONTROL	0x402F0060
CAN1_CAN_TX4_ID	0x402F0064
CAN1_CAN_TX4_DATA_HIGH	0x402F0068
CAN1_CAN_TX4_DATA_LOW	0x402F006C
CAN1_CAN_TX5_CONTROL	0x402F0070
CAN1_CAN_TX5_ID	0x402F0074
CAN1_CAN_TX5_DATA_HIGH	0x402F0078
CAN1_CAN_TX5_DATA_LOW	0x402F007C
CAN1_CAN_TX6_CONTROL	0x402F0080
CAN1_CAN_TX6_ID	0x402F0084
CAN1_CAN_TX6_DATA_HIGH	0x402F0088
CAN1_CAN_TX6_DATA_LOW	0x402F008C
CAN1_CAN_TX7_CONTROL	0x402F0090
CAN1_CAN_TX7_ID	0x402F0094
CAN1_CAN_TX7_DATA_HIGH	0x402F0098
CAN1_CAN_TX7_DATA_LOW	0x402F009C

4.1.1 CAN0_CAN_TX0_CONTROL

TxMessage Buffer control/command

Address: 0x402E0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_EBL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Control Flags [23]: WPN, Write Protect Not3 '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

4.1.1 CAN0_CAN_TX0_CONTROL (continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPN: Write protect not. '0': Bit [2] remains unchanged '1': Bit [2] is modified, default. This bit is always zero for readback Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable ¡®0¡¯: Interrupt disabled ¡®1¡¯: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle ¡®1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

4.1.2 CAN0_CAN_TX0_ID

TxMessage Buffer Identifier

Address: 0x402E0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

4.1.3 CAN0_CAN_TX0_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402E0028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

4.1.4 CAN0_CAN_TX0_DATA_LOW

TxMessageBuffer Data low

Address: 0x402E002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

4.1.5 CAN0_CAN_TX1_CONTROL

TxMessage Buffer control/command

Address: 0x402E0030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_EBL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Control Flags [23]: WPN, Write Protect Not3 '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

4.1.5 CAN0_CAN_TX1_CONTROL (continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPN: Write protect not. '0': Bit [2] remains unchanged '1': Bit [2] is modified, default. This bit is always zero for readback Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable ¡®0¡¯: Interrupt disabled ¡®1¡¯: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle ¡®1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

4.1.6 CAN0_CAN_TX1_ID

TxMessage Buffer Identifier

Address: 0x402E0034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

4.1.7 CAN0_CAN_TX1_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402E0038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

4.1.8 CAN0_CAN_TX1_DATA_LOW

TxMessageBuffer Data low

Address: 0x402E003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

4.1.9 CAN0_CAN_TX2_CONTROL

TxMessage Buffer control/command

Address: 0x402E0040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_EBL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Control Flags [23]: WPN, Write Protect Not3 '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

4.1.9 CAN0_CAN_TX2_CONTROL (continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPN: Write protect not. '0': Bit [2] remains unchanged '1': Bit [2] is modified, default. This bit is always zero for readback Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable ¡®0¡¯: Interrupt disabled ¡®1¡¯: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle ¡®1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

4.1.10 CAN0_CAN_TX2_ID

TxMessage Buffer Identifier

Address: 0x402E0044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

4.1.11 CAN0_CAN_TX2_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402E0048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

4.1.12 CAN0_CAN_TX2_DATA_LOW

TxMessageBuffer Data low

Address: 0x402E004C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

4.1.13 CAN0_CAN_TX3_CONTROL

TxMessage Buffer control/command

Address: 0x402E0050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_EBL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Control Flags [23]: WPN, Write Protect Not3 '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

4.1.13 CAN0_CAN_TX3_CONTROL (continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPN: Write protect not. '0': Bit [2] remains unchanged '1': Bit [2] is modified, default. This bit is always zero for readback Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable ¡®0¡¯: Interrupt disabled ¡®1¡¯: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle ¡®1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

4.1.14 CAN0_CAN_TX3_ID

TxMessage Buffer Identifier

Address: 0x402E0054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

4.1.15 CAN0_CAN_TX3_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402E0058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

4.1.16 CAN0_CAN_TX3_DATA_LOW

TxMessageBuffer Data low

Address: 0x402E005C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

4.1.17 CAN0_CAN_TX4_CONTROL

TxMessage Buffer control/command

Address: 0x402E0060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_EBL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Control Flags [23]: WPN, Write Protect Not3 '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

4.1.17 CAN0_CAN_TX4_CONTROL (continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPN: Write protect not. '0': Bit [2] remains unchanged '1': Bit [2] is modified, default. This bit is always zero for readback Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable ¡®0¡¯: Interrupt disabled ¡®1¡¯: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle ¡®1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

4.1.18 CAN0_CAN_TX4_ID

TxMessage Buffer Identifier

Address: 0x402E0064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

4.1.19 CAN0_CAN_TX4_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402E0068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

4.1.20 CAN0_CAN_TX4_DATA_LOW

TxMessageBuffer Data low

Address: 0x402E006C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

4.1.21 CAN0_CAN_TX5_CONTROL

TxMessage Buffer control/command

Address: 0x402E0070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_EBL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Control Flags [23]: WPN, Write Protect Not3 '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

4.1.21 CAN0_CAN_TX5_CONTROL (continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPN: Write protect not. '0': Bit [2] remains unchanged '1': Bit [2] is modified, default. This bit is always zero for readback Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable ¡®0¡¯: Interrupt disabled ¡®1¡¯: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle ¡®1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

4.1.22 CAN0_CAN_TX5_ID

TxMessage Buffer Identifier

Address: 0x402E0074

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

4.1.23 CAN0_CAN_TX5_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402E0078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

4.1.24 CAN0_CAN_TX5_DATA_LOW

TxMessageBuffer Data low

Address: 0x402E007C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

4.1.25 CAN0_CAN_TX6_CONTROL

TxMessage Buffer control/command

Address: 0x402E0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_EBL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Control Flags [23]: WPN, Write Protect Not3 '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

4.1.25 CAN0_CAN_TX6_CONTROL (continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPN: Write protect not. '0': Bit [2] remains unchanged '1': Bit [2] is modified, default. This bit is always zero for readback Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable ¡®0¡¯: Interrupt disabled ¡®1¡¯: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle ¡®1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

4.1.26 CAN0_CAN_TX6_ID

TxMessage Buffer Identifier

Address: 0x402E0084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

4.1.27 CAN0_CAN_TX6_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402E0088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

4.1.28 CAN0_CAN_TX6_DATA_LOW

TxMessageBuffer Data low

Address: 0x402E008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

4.1.29 CAN0_CAN_TX7_CONTROL

TxMessage Buffer control/command

Address: 0x402E0090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_EBL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Control Flags [23]: WPN, Write Protect Not3 '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

4.1.29 CAN0_CAN_TX7_CONTROL (continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPN: Write protect not. '0': Bit [2] remains unchanged '1': Bit [2] is modified, default. This bit is always zero for readback Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable ¡®0¡¯: Interrupt disabled ¡®1¡¯: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle ¡®1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

4.1.30 CAN0_CAN_TX7_ID

TxMessage Buffer Identifier

Address: 0x402E0094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

4.1.31 CAN0_CAN_TX7_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402E0098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

4.1.32 CAN0_CAN_TX7_DATA_LOW

TxMessageBuffer Data low

Address: 0x402E009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

4.1.33 CAN1_CAN_TX0_CONTROL

TxMessage Buffer control/command

Address: 0x402F0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_EBL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Control Flags [23]: WPN, Write Protect Not3 '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

4.1.33 CAN1_CAN_TX0_CONTROL (continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPN: Write protect not. '0': Bit [2] remains unchanged '1': Bit [2] is modified, default. This bit is always zero for readback Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable ¡®0¡¯: Interrupt disabled ¡®1¡¯: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle ¡®1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

4.1.34 CAN1_CAN_TX0_ID

TxMessage Buffer Identifier

Address: 0x402F0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

4.1.35 CAN1_CAN_TX0_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402F0028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

4.1.36 CAN1_CAN_TX0_DATA_LOW

TxMessageBuffer Data low

Address: 0x402F002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

4.1.37 CAN1_CAN_TX1_CONTROL

TxMessage Buffer control/command

Address: 0x402F0030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_EBL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Control Flags [23]: WPN, Write Protect Not3 '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

4.1.37 CAN1_CAN_TX1_CONTROL (continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPN: Write protect not. '0': Bit [2] remains unchanged '1': Bit [2] is modified, default. This bit is always zero for readback Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable ¡®0¡¯: Interrupt disabled ¡®1¡¯: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle ¡®1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

4.1.38 CAN1_CAN_TX1_ID

TxMessage Buffer Identifier

Address: 0x402F0034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

4.1.39 CAN1_CAN_TX1_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402F0038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

4.1.40 CAN1_CAN_TX1_DATA_LOW

TxMessageBuffer Data low

Address: 0x402F003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

4.1.41 CAN1_CAN_TX2_CONTROL

TxMessage Buffer control/command

Address: 0x402F0040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_EBL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Control Flags [23]: WPN, Write Protect Not3 '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

4.1.41 CAN1_CAN_TX2_CONTROL (continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPN: Write protect not. '0': Bit [2] remains unchanged '1': Bit [2] is modified, default. This bit is always zero for readback Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable ¡®0¡¯: Interrupt disabled ¡®1¡¯: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle ¡®1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

4.1.42 CAN1_CAN_TX2_ID

TxMessage Buffer Identifier

Address: 0x402F0044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

4.1.43 CAN1_CAN_TX2_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402F0048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

4.1.44 CAN1_CAN_TX2_DATA_LOW

TxMessageBuffer Data low

Address: 0x402F004C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

4.1.45 CAN1_CAN_TX3_CONTROL

TxMessage Buffer control/command

Address: 0x402F0050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_EBL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Control Flags [23]: WPN, Write Protect Not3 '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

4.1.45 CAN1_CAN_TX3_CONTROL (continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPN: Write protect not. '0': Bit [2] remains unchanged '1': Bit [2] is modified, default. This bit is always zero for readback Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable ¡®0¡¯: Interrupt disabled ¡®1¡¯: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle ¡®1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

4.1.46 CAN1_CAN_TX3_ID

TxMessage Buffer Identifier

Address: 0x402F0054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

4.1.47 CAN1_CAN_TX3_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402F0058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

4.1.48 CAN1_CAN_TX3_DATA_LOW

TxMessageBuffer Data low

Address: 0x402F005C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

4.1.49 CAN1_CAN_TX4_CONTROL

TxMessage Buffer control/command

Address: 0x402F0060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_EBL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Control Flags [23]: WPN, Write Protect Not3 '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

4.1.49 CAN1_CAN_TX4_CONTROL (continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPN: Write protect not. '0': Bit [2] remains unchanged '1': Bit [2] is modified, default. This bit is always zero for readback Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable ¡®0¡¯: Interrupt disabled ¡®1¡¯: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle ¡®1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

4.1.50 CAN1_CAN_TX4_ID

TxMessage Buffer Identifier

Address: 0x402F0064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

4.1.51 CAN1_CAN_TX4_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402F0068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

4.1.52 CAN1_CAN_TX4_DATA_LOW

TxMessageBuffer Data low

Address: 0x402F006C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

4.1.53 CAN1_CAN_TX5_CONTROL

TxMessage Buffer control/command

Address: 0x402F0070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_EBL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Control Flags [23]: WPN, Write Protect Not3 '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

4.1.53 CAN1_CAN_TX5_CONTROL (continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPN: Write protect not. '0': Bit [2] remains unchanged '1': Bit [2] is modified, default. This bit is always zero for readback Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable ¡®0¡¯: Interrupt disabled ¡®1¡¯: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle ¡®1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

4.1.54 CAN1_CAN_TX5_ID

TxMessage Buffer Identifier

Address: 0x402F0074

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

4.1.55 CAN1_CAN_TX5_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402F0078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

4.1.56 CAN1_CAN_TX5_DATA_LOW

TxMessageBuffer Data low

Address: 0x402F007C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

4.1.57 CAN1_CAN_TX6_CONTROL

TxMessage Buffer control/command

Address: 0x402F0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_EBL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Control Flags [23]: WPN, Write Protect Not3 '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

4.1.57 CAN1_CAN_TX6_CONTROL (continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPN: Write protect not. '0': Bit [2] remains unchanged '1': Bit [2] is modified, default. This bit is always zero for readback Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable ¡®0¡¯: Interrupt disabled ¡®1¡¯: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle ¡®1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

4.1.58 CAN1_CAN_TX6_ID

TxMessage Buffer Identifier

Address: 0x402F0084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

4.1.59 CAN1_CAN_TX6_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402F0088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

4.1.60 CAN1_CAN_TX6_DATA_LOW

TxMessageBuffer Data low

Address: 0x402F008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

4.1.61 CAN1_CAN_TX7_CONTROL

TxMessage Buffer control/command

Address: 0x402F0090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_EBL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	Control Flags [23]: WPN, Write Protect Not3 '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

4.1.61 CAN1_CAN_TX7_CONTROL (continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPN: Write protect not. '0': Bit [2] remains unchanged '1': Bit [2] is modified, default. This bit is always zero for readback Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable ¡®0¡¯: Interrupt disabled ¡®1¡¯: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle ¡®1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

4.1.62 CAN1_CAN_TX7_ID

TxMessage Buffer Identifier

Address: 0x402F0094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

4.1.63 CAN1_CAN_TX7_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402F0098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

4.1.64 CAN1_CAN_TX7_DATA_LOW

TxMessageBuffer Data low

Address: 0x402F009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

5 Cortex M0 (CM0) Registers

This section discusses the CM0 registers. It lists all the registers in mapping tables, in address order.

5.1 Register Details

Register Name	Address
CM0_DWT_PID4	0xE0001FD0
CM0_DWT_PID0	0xE0001FE0
CM0_DWT_PID1	0xE0001FE4
CM0_DWT_PID2	0xE0001FE8
CM0_DWT_PID3	0xE0001FEC
CM0_DWT_CID0	0xE0001FF0
CM0_DWT_CID1	0xE0001FF4
CM0_DWT_CID2	0xE0001FF8
CM0_DWT_CID3	0xE0001FFC
CM0_BP_PID4	0xE0002FD0
CM0_BP_PID0	0xE0002FE0
CM0_BP_PID1	0xE0002FE4
CM0_BP_PID2	0xE0002FE8
CM0_BP_PID3	0xE0002FEC
CM0_BP_CID0	0xE0002FF0
CM0_BP_CID1	0xE0002FF4
CM0_BP_CID2	0xE0002FF8
CM0_BP_CID3	0xE0002FFC
CM0_SYST_CSR	0xE000E010
CM0_SYST_RVR	0xE000E014
CM0_SYST_CVR	0xE000E018
CM0_SYST_CALIB	0xE000E01C
CM0_ISER	0xE000E100
CM0_ICER	0xE000E180
CM0_ISPR	0xE000E200
CM0_ICPR	0xE000E280
CM0_IPR0	0xE000E400

Register Name	Address
CM0_IPR1	0xE000E404
CM0_IPR2	0xE000E408
CM0_IPR3	0xE000E40C
CM0_IPR4	0xE000E410
CM0_IPR5	0xE000E414
CM0_IPR6	0xE000E418
CM0_IPR7	0xE000E41C
CM0_CPUID	0xE000ED00
CM0_ICSR	0xE000ED04
CM0_AIRCR	0xE000ED0C
CM0_SCR	0xE000ED10
CM0_CCR	0xE000ED14
CM0_SHPR2	0xE000ED1C
CM0_SHPR3	0xE000ED20
CM0_SHCSR	0xE000ED24
CM0_SCS_PID4	0xE000EFD0
CM0_SCS_PID0	0xE000EFE0
CM0_SCS_PID1	0xE000EFE4
CM0_SCS_PID2	0xE000EFE8
CM0_SCS_PID3	0xE000EFEC
CM0_SCS_CID0	0xE000EFF0
CM0_SCS_CID1	0xE000EFF4
CM0_SCS_CID2	0xE000EFF8
CM0_SCS_CID3	0xE000EFFC
CM0_ROM_SCS	0xE00FF000
CM0_ROM_DWT	0xE00FF004
CM0_ROM_BPU	0xE00FF008
CM0_ROM_END	0xE00FF00C
CM0_ROM_CSMT	0xE00FFFCC
CM0_ROM_PID4	0xE00FFFD0
CM0_ROM_PID0	0xE00FFFE0
CM0_ROM_PID1	0xE00FFFE4
CM0_ROM_PID2	0xE00FFFE8
CM0_ROM_PID3	0xE00FFFEC
CM0_ROM_CID0	0xE00FFFF0
CM0_ROM_CID1	0xE00FFFF4
CM0_ROM_CID2	0xE00FFFF8
CM0_ROM_CID3	0xE00FFFFC

5.1.1 CM0_DWT_PID4

Watchpoint Unit CoreSight ROM Table Peripheral ID #4

Address: 0xE0001FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

5.1.2 CM0_DWT_PID0

Watchpoint Unit CoreSight ROM Table Peripheral ID #0

Address: 0xE0001FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 10

5.1.3 CM0_DWT_PID1

Watchpoint Unit CoreSight ROM Table Peripheral ID #1

Address: 0xE0001FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

5.1.4 CM0_DWT_PID2

Watchpoint Unit CoreSight ROM Table Peripheral ID #2

Address: 0xE0001FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

5.1.5 CM0_DWT_PID3

Watchpoint Unit CoreSight ROM Table Peripheral ID #3

Address: 0xE0001FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

5.1.6 CM0_DWT_CID0

Watchpoint Unit CoreSight ROM Table Component ID #0

Address: 0xE0001FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

5.1.7 CM0_DWT_CID1

Watchpoint Unit CoreSight ROM Table Component ID #1

Address: 0xE0001FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

5.1.8 CM0_DWT_CID2

Watchpoint Unit CoreSight ROM Table Component ID #2

Address: 0xE0001FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

5.1.9 CM0_DWT_CID3

Watchpoint Unit CoreSight ROM Table Component ID #3

Address: 0xE0001FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

5.1.10 CM0_BP_PID4

Breakpoint Unit CoreSight ROM Table Peripheral ID #4

Address: 0xE0002FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

5.1.11 CM0_BP_PID0

Breakpoint Unit CoreSight ROM Table Peripheral ID #0

Address: 0xE0002FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 11

5.1.12 CM0_BP_PID1

Breakpoint Unit CoreSight ROM Table Peripheral ID #1

Address: 0xE0002FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

5.1.13 CM0_BP_PID2

Breakpoint Unit CoreSight ROM Table Peripheral ID #2

Address: 0xE0002FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

5.1.14 CM0_BP_PID3

Breakpoint Unit CoreSight ROM Table Peripheral ID #3

Address: 0xE0002FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

5.1.15 CM0_BP_CID0

Breakpoint Unit CoreSight ROM Table Component ID #0

Address: 0xE0002FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

5.1.16 CM0_BP_CID1

Breakpoint Unit CoreSight ROM Table Component ID #1

Address: 0xE0002FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

5.1.17 CM0_BP_CID2

Breakpoint Unit CoreSight ROM Table Component ID #2

Address: 0xE0002FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

5.1.18 CM0_BP_CID3

Breakpoint Unit CoreSight ROM Table Component ID #3

Address: 0xE0002FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

5.1.19 CM0_SYST_CSR

SysTick Control & Status

Address: 0xE000E010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CLK-SOURCE	TICKINT	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							RW
Name	None [23:17]							COUNT-FLAG

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	COUNTFLAG	Indicates whether the counter has counted to "0" since the last read of this register: '0': counter has not counted to "0". '1': counter has counted to "0". COUNTFLAG is set to '1' by a count transition from "1" to "0". COUNTFLAG is cleared to '0' by a read of this register, and by any write to the SYST_CVR register. Default Value: 0
2	CLKSOURCE	Indicates the SysTick counter clock source: '0': SysTick uses the low frequency clock "clk_lf". For this mode to function, "clk_lf" should be less than half the frequency of "clk_sys". Note that "clk_lf" is generated by a low accuracy ILO (Internal Low power Oscillator), with a target frequency of 32.768 kHz (frequency can be as low as 15 KHz and as high as 60 kHz). '1': SysTick uses the system/processor clock "clk_sys". Default Value: 0

5.1.19 CM0_SYST_CSR (continued)

1	TICKINT	Indicates whether counting to "0" causes the status of the SysTick exception to change to pending: '0': count to "0" does not affect the SysTick exception status. '1': count to "0" changes the SysTick exception status to pending. Changing the value of the counter to "0" by writing zero to the SYST_CVR register to "0" never changes the status of the SysTick exception. Default Value: 0
0	ENABLE	Indicates the enabled status of the SysTick counter: '0': counter is disabled. '1': counter is operating. Default Value: 0

5.1.20 CM0_SYST_RVR

SysTick Reload Value

Address: 0xE000E014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RELOAD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RELOAD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RELOAD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	RELOAD	The value to load into the SYST_CVR register when the counter reaches 0. Default Value: X

5.1.21 CM0_SYST_CVR

SysTick Current Value

Address: 0xE000E018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CURRENT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CURRENT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CURRENT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	CURRENT	Current counter value. This is the value of the counter at the time it is sampled. Default Value: X

5.1.22 CM0_SYST_CALIB

SysTick Calibration Value

Address: 0xE000E01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TENMS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TENMS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TENMS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	None	RW	None					
Name	NOREF	SKEW	None [29:24]					

Bits	Name	Description
31	NOREF	Indicates whether a implementation defined reference clock is provided: '0': the reference clock is provided. '1': the reference clock is not provided. When this bit is '1', the SYST_CSR.CLKSOURCEis forced to '1' and cannot be cleared to '0'. Default Value: 0
30	SKEW	Indicates whether the 10ms calibration value is exact: '0': 10ms calibration value is exact. '1': 10ms calibration value is inexact, because of the clock frequency. Default Value: X
23 : 0	TENMS	Optionally, holds a reload value to be used for 10ms (100Hz) timing, subject to system clock skew errors. If this field is "0", the calibration value is not known. Default Value: X

5.1.23 CM0_ISER

Interrupt Set-Enable Register

Address: 0xE000E100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	SETENA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	R							
Name	SETENA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	R							
Name	SETENA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	R							
Name	SETENA [31:24]							

Bits	Name	Description
31 : 0	SETENA	Enables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default Value: 0

5.1.24 CM0_ICER

Interrupt Clear Enable Register

Address: 0xE000E180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	R							
Name	CLRENA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	CLRENA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	R							
Name	CLRENA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	CLRENA [31:24]							

Bits	Name	Description
31 : 0	CLRENA	Disables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default Value: 0

5.1.25 CM0_ISPR

Interrupt Set-Pending Register

Address: 0xE000E200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	SETPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	R							
Name	SETPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	R							
Name	SETPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	R							
Name	SETPEND [31:24]							

Bits	Name	Description
31 : 0	SETPEND	Changes the state of one or more interrupts to pending. Each bit corresponds to the same numbered interrupt. Default Value: 0

5.1.26 CM0_ICPR

Interrupt Clear-Pending Register

Address: 0xE000E280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [31:24]							

Bits	Name	Description
31 : 0	CLRPEND	Changes the state of one or more interrupts to not pending. Each bit corresponds to the same numbered interrupt. Default Value: 0

5.1.27 CM0_IPR0

Interrupt Priority Registers

Address: 0xE000E400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

5.1.28 CM0_IPR1

Interrupt Priority Registers

Address: 0xE000E404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

5.1.29 CM0_IPR2

Interrupt Priority Registers

Address: 0xE000E408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

5.1.30 CM0_IPR3

Interrupt Priority Registers

Address: 0xE000E40C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

5.1.31 CM0_IPR4

Interrupt Priority Registers

Address: 0xE000E410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

5.1.32 CM0_IPR5

Interrupt Priority Registers

Address: 0xE000E414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

5.1.33 CM0_IPR6

Interrupt Priority Registers

Address: 0xE000E418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

5.1.34 CM0_IPR7

Interrupt Priority Registers

Address: 0xE000E41C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

5.1.35 CM0_CPUID

CPUID Register

Address: 0xE000ED00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	None				None			
Name	PARTNO [7:4]				REVISION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	PARTNO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	None				None			
Name	VARIANT [23:20]				CONSTANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	IMPLEMENTER [31:24]							

Bits	Name	Description
31 : 24	IMPLEMENTER	Implementer code for ARM. Default Value: 65
23 : 20	VARIANT	Implementation defined. In ARM implementations this is the major revision number n in the rn part of the rnpn revision status Default Value: 0
19 : 16	CONSTANT	Indicates the architecture, ARMv6-M Default Value: 12
15 : 4	PARTNO	Indicates part number, Cortex-M0 Default Value: 3104
3 : 0	REVISION	Indicates revision. In ARM implementations this is the minor revision number n in the pn part of the rnpn revision status Default Value: 0

5.1.36 CM0_ICSR

Interrupt Control State Register

Address: 0xE000ED04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VECTACTIVE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			R
HW Access	RW				None			RW
Name	VECTPENDING [15:12]				None [11:9]			VECTAC-TIVE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	None	R				
HW Access	RW	RW	None	RW				
Name	ISRPRE-EMPT	ISRPEND-ING	None	VECTPENDING [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None		RW1S	RW1C	RW1S	RW1C	None
HW Access	RW	None		RW	R	RW	R	None
Name	NMIPEND-SET	None [30:29]		PENDSV-SET	PENDSV-CLR	PENDST-SETb	PENDST-CLR	None

Bits	Name	Description
31	NMIPENDSET	Activates an NMI exception or reads back the current state. Because NMI is the highest priority exception, it activates as soon as it is registered. Default Value: 0
28	PENDSVSET	Sets a pending PendSV interrupt or reads back the current state. Use this normally to request a context switch. Writing PENDSVSET and PENDSVCLR to '1' concurrently is UNPREDICT-ABLE. Default Value: 0
27	PENDSVCLR	Clears a pending PendSV interrupt. Default Value: 0
26	PENDSTSETb	Sets a pending SysTick or reads back the current state. Writing PENDSTSET and PENDSTCLR to '1' concurrently is UNPREDICTABLE. Default Value: 0
25	PENDSTCLR	Clears a pending SysTick, whether set here or by the timer hardware. Default Value: 0

5.1.36 CM0_ICSR (continued)

23	ISRPREEMPT	Indicates whether a pending exception will be serviced on exit from debug halt state. Default Value: 0
22	ISRPENDING	Indicates if an external configurable, NVIC generated, interrupt is pending. Default Value: 0
20 : 12	VECTPENDING	The exception number for the highest priority pending exception. 0= No pending exceptions. The pending state includes the effect of memory-mapped enable and mask registers. It does not include the PRIMASK special-purpose register qualifier. Default Value: 0
8 : 0	VECTACTIVE	The exception number for the current executing exception. 0= Thread mode. This is the same value as IPSR[8:0] Default Value: 0

5.1.37 CM0_AIRCR

Application Interrupt and Reset Control Register

Address: 0xE000ED0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1C	None
HW Access	None					R	R	None
Name	None [7:3]					SYSRESE-TREQ	VECTCL-RACTIVE	None

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	None	None						
Name	ENDIAN-NESS	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VECTKEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VECTKEY [31:24]							

Bits	Name	Description
31 : 16	VECTKEY	Vector Key. The value 0x05FA must be written to this register, otherwise the register write is UN-PREDICTABLE. Readback value is UNKNOWN. Default Value: X
15	ENDIANNESS	Indicates the memory system data endianness: 0 little endian 1 big endian. Default Value: 0
2	SYSRESETREQ	System Reset Request. Writing 1 to this bit asserts a signal to request a reset by the external system. This will cause a full system reset of the CPU and all other components in the device. Default Value: 0
1	VECTCLRACTIVE	Clears all active state information for fixed and configurable exceptions. The effect of writing a 1 to this bit if the processor is not halted in Debug state is UNPREDICTABLE. Default Value: 0

5.1.38 CM0_SCR

System Control Register

Address: 0xE000ED10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	None
HW Access	None			R	None	R	R	None
Name	None [7:5]			SEVON-PEND	None	SLEEP-DEEP	SLEEPON-EXIT	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	SEVONPEND	Determines whether an interrupt transition from inactive state to pending state is a wakeup event: 0: transitions from inactive to pending are not wakeup events. 1: transitions from inactive to pending are wakeup events. Default Value: 0
2	SLEEPDEEP	An implementation can use this bit to select DeepSleep/Hibernate power modes upon execution of WFI/WFE: 0: Select Sleep mode 1: Select DeepSleep/Hibernate (depends on PWR_CONTROL.HIBERNATE) Default Value: 0
1	SLEEPONEXIT	Determines whether, on an exit from an ISR that returns to the base level of execution priority, the processor enters a sleep state: 0 do not enter sleep state. 1 enter sleep state. Default Value: 0

5.1.39 CM0_CCR

Configuration and Control Register

Address: 0xE000ED14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	None		
HW Access	None				None	None		
Name	None [7:4]				UNALIGN_ TRP	None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	None
HW Access	None						None	None
Name	None [15:10]						STKALIGN	None

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	STKALIGN	1: On exception entry, the SP used prior to the exception is adjusted to be 8-byte aligned and the context to restore it is saved. The SP is restored on the associated exception return. Default Value: 1
3	UNALIGN_TRP	1: unaligned word and halfword accesses generate a HardFault exception. Default Value: 1

5.1.40 CM0_SHPR2

System Handler Priority Register 2

Address: 0xE000ED1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_11 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_11	Priority of system handler 11, SVCall Default Value: 0

5.1.41 CM0_SHPR3

System Handler Priority Register 3

Address: 0xE000ED20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_14 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_15 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_15	Priority of system handler 15, SysTick Default Value: 0
23 : 22	PRI_14	Priority of system handler 14, PendSV Default Value: 0

5.1.42 CM0_SHCSR

System Handler Control and State Register

Address: 0xE000ED24

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None						
HW Access	RW	None						
Name	SVCALL-PENDED	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	SVCALLPENDED	0 SVCall is not pending. 1 SVCall is pending. This bit reflects the pending state on a read, and updates the pending state, to the value written, on a write. (Pending state bits are set to 1 when an exception occurs, and are cleared to 0 when an exception becomes active.) Default Value: 0

5.1.43 CM0_SCS_PID4

System Control Space ROM Table Peripheral ID #4

Address: 0xE000EFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

5.1.44 CM0_SCS_PID0

System Control Space ROM Table Peripheral ID #0

Address: 0xE000EFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 8

5.1.45 CM0_SCS_PID1

System Control Space ROM Table Peripheral ID #1

Address: 0xE000EFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

5.1.46 CM0_SCS_PID2

System Control Space ROM Table Peripheral ID #2

Address: 0xE000EFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

5.1.47 CM0_SCS_PID3

System Control Space ROM Table Peripheral ID #3

Address: 0xE000EFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

5.1.48 CM0_SCS_CID0

System Control Space ROM Table Component ID #0

Address: 0xE000EFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

5.1.49 CM0_SCS_CID1

System Control Space ROM Table Component ID #1

Address: 0xE000EFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

5.1.50 CM0_SCS_CID2

System Control Space ROM Table Component ID #2

Address: 0xE000EFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

5.1.51 CM0_SCS_CID3

System Control Space ROM Table Component ID #3

Address: 0xE000EFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

5.1.52 CM0_ROM_SCS

CM0 CoreSight ROM Table Peripheral #0

Address: 0xE00FF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to SCS ROM Table Default Value: 4293980163

5.1.53 CM0_ROM_DWT

CM0 CoreSight ROM Table Peripheral #1

Address: 0xE00FF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to DWT ROM Table Default Value: 4293926915

5.1.54 CM0_ROM_BPU

CM0 CoreSight ROM Table Peripheral #2

Address: 0xE00FF008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to BPU ROM Table Default Value: 4293931011

5.1.55 CM0_ROM_END

CM0 CoreSight ROM Table End Marker

Address: 0xE00FF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	End marker in peripheral list Default Value: 0

5.1.56 CM0_ROM_CSMT

CM0 CoreSight ROM Table Memory Type

Address: 0xE00FFFCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Memory Type Default Value: 1

5.1.57 CM0_ROM_PID4

CM0 CoreSight ROM Table Peripheral ID #4

Address: 0xE00FFFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

5.1.58 CM0_ROM_PID0

CM0 CoreSight ROM Table Peripheral ID #0

Address: 0xE00FFFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 113

5.1.59 CM0_ROM_PID1

CM0 CoreSight ROM Table Peripheral ID #1

Address: 0xE00FFFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 180

5.1.60 CM0_ROM_PID2

CM0 CoreSight ROM Table Peripheral ID #2

Address: 0xE00FFFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

5.1.61 CM0_ROM_PID3

CM0 CoreSight ROM Table Peripheral ID #3

Address: 0xE00FFFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

5.1.62 CM0_ROM_CID0

CM0 CoreSight ROM Table Component ID #0

Address: 0xE00FFFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

5.1.63 CM0_ROM_CID1

CM0 CoreSight ROM Table Component ID #1

Address: 0xE00FFFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 16

5.1.64 CM0_ROM_CID2

CM0 CoreSight ROM Table Component ID #2

Address: 0xE00FFFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

5.1.65 CM0_ROM_CID3

CM0 CoreSight ROM Table Component ID #3

Address: 0xE00FFFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

6 Timer, Counter, PWM Counter (CNT) Registers

This section discusses the CNT registers. It lists all the registers in mapping tables, in address order.

6.1 Register Details

Register Name	Address
TCPWM_CNT0_CTRL	0x40200100
TCPWM_CNT0_STATUS	0x40200104
TCPWM_CNT0_COUNTER	0x40200108
TCPWM_CNT0_CC	0x4020010C
TCPWM_CNT0_CC_BUFF	0x40200110
TCPWM_CNT0_PERIOD	0x40200114
TCPWM_CNT0_PERIOD_BUFF	0x40200118
TCPWM_CNT0_TR_CTRL0	0x40200120
TCPWM_CNT0_TR_CTRL1	0x40200124
TCPWM_CNT0_TR_CTRL2	0x40200128
TCPWM_CNT0_INTR	0x40200130
TCPWM_CNT0_INTR_SET	0x40200134
TCPWM_CNT0_INTR_MASK	0x40200138
TCPWM_CNT0_INTR_MASKED	0x4020013C
TCPWM_CNT1_CTRL	0x40200140
TCPWM_CNT1_STATUS	0x40200144
TCPWM_CNT1_COUNTER	0x40200148
TCPWM_CNT1_CC	0x4020014C
TCPWM_CNT1_CC_BUFF	0x40200150
TCPWM_CNT1_PERIOD	0x40200154
TCPWM_CNT1_PERIOD_BUFF	0x40200158
TCPWM_CNT1_TR_CTRL0	0x40200160
TCPWM_CNT1_TR_CTRL1	0x40200164
TCPWM_CNT1_TR_CTRL2	0x40200168
TCPWM_CNT1_INTR	0x40200170
TCPWM_CNT1_INTR_SET	0x40200174
TCPWM_CNT1_INTR_MASK	0x40200178

Register Name	Address
TCPWM_CNT1_INTR_MASKED	0x4020017C
TCPWM_CNT2_CTRL	0x40200180
TCPWM_CNT2_STATUS	0x40200184
TCPWM_CNT2_COUNTER	0x40200188
TCPWM_CNT2_CC	0x4020018C
TCPWM_CNT2_CC_BUFF	0x40200190
TCPWM_CNT2_PERIOD	0x40200194
TCPWM_CNT2_PERIOD_BUFF	0x40200198
TCPWM_CNT2_TR_CTRL0	0x402001A0
TCPWM_CNT2_TR_CTRL1	0x402001A4
TCPWM_CNT2_TR_CTRL2	0x402001A8
TCPWM_CNT2_INTR	0x402001B0
TCPWM_CNT2_INTR_SET	0x402001B4
TCPWM_CNT2_INTR_MASK	0x402001B8
TCPWM_CNT2_INTR_MASKED	0x402001BC
TCPWM_CNT3_CTRL	0x402001C0
TCPWM_CNT3_STATUS	0x402001C4
TCPWM_CNT3_COUNTER	0x402001C8
TCPWM_CNT3_CC	0x402001CC
TCPWM_CNT3_CC_BUFF	0x402001D0
TCPWM_CNT3_PERIOD	0x402001D4
TCPWM_CNT3_PERIOD_BUFF	0x402001D8
TCPWM_CNT3_TR_CTRL0	0x402001E0
TCPWM_CNT3_TR_CTRL1	0x402001E4
TCPWM_CNT3_TR_CTRL2	0x402001E8
TCPWM_CNT3_INTR	0x402001F0
TCPWM_CNT3_INTR_SET	0x402001F4
TCPWM_CNT3_INTR_MASK	0x402001F8
TCPWM_CNT3_INTR_MASKED	0x402001FC
TCPWM_CNT4_CTRL	0x40200200
TCPWM_CNT4_STATUS	0x40200204
TCPWM_CNT4_COUNTER	0x40200208
TCPWM_CNT4_CC	0x4020020C
TCPWM_CNT4_CC_BUFF	0x40200210
TCPWM_CNT4_PERIOD	0x40200214
TCPWM_CNT4_PERIOD_BUFF	0x40200218
TCPWM_CNT4_TR_CTRL0	0x40200220
TCPWM_CNT4_TR_CTRL1	0x40200224
TCPWM_CNT4_TR_CTRL2	0x40200228
TCPWM_CNT4_INTR	0x40200230
TCPWM_CNT4_INTR_SET	0x40200234
TCPWM_CNT4_INTR_MASK	0x40200238

Register Name	Address
TCPWM_CNT4_INTR_MASKED	0x4020023C
TCPWM_CNT5_CTRL	0x40200240
TCPWM_CNT5_STATUS	0x40200244
TCPWM_CNT5_COUNTER	0x40200248
TCPWM_CNT5_CC	0x4020024C
TCPWM_CNT5_CC_BUFF	0x40200250
TCPWM_CNT5_PERIOD	0x40200254
TCPWM_CNT5_PERIOD_BUFF	0x40200258
TCPWM_CNT5_TR_CTRL0	0x40200260
TCPWM_CNT5_TR_CTRL1	0x40200264
TCPWM_CNT5_TR_CTRL2	0x40200268
TCPWM_CNT5_INTR	0x40200270
TCPWM_CNT5_INTR_SET	0x40200274
TCPWM_CNT5_INTR_MASK	0x40200278
TCPWM_CNT5_INTR_MASKED	0x4020027C
TCPWM_CNT6_CTRL	0x40200280
TCPWM_CNT6_STATUS	0x40200284
TCPWM_CNT6_COUNTER	0x40200288
TCPWM_CNT6_CC	0x4020028C
TCPWM_CNT6_CC_BUFF	0x40200290
TCPWM_CNT6_PERIOD	0x40200294
TCPWM_CNT6_PERIOD_BUFF	0x40200298
TCPWM_CNT6_TR_CTRL0	0x402002A0
TCPWM_CNT6_TR_CTRL1	0x402002A4
TCPWM_CNT6_TR_CTRL2	0x402002A8
TCPWM_CNT6_INTR	0x402002B0
TCPWM_CNT6_INTR_SET	0x402002B4
TCPWM_CNT6_INTR_MASK	0x402002B8
TCPWM_CNT6_INTR_MASKED	0x402002BC
TCPWM_CNT7_CTRL	0x402002C0
TCPWM_CNT7_STATUS	0x402002C4
TCPWM_CNT7_COUNTER	0x402002C8
TCPWM_CNT7_CC	0x402002CC
TCPWM_CNT7_CC_BUFF	0x402002D0
TCPWM_CNT7_PERIOD	0x402002D4
TCPWM_CNT7_PERIOD_BUFF	0x402002D8
TCPWM_CNT7_TR_CTRL0	0x402002E0
TCPWM_CNT7_TR_CTRL1	0x402002E4
TCPWM_CNT7_TR_CTRL2	0x402002E8
TCPWM_CNT7_INTR	0x402002F0
TCPWM_CNT7_INTR_SET	0x402002F4
TCPWM_CNT7_INTR_MASK	0x402002F8

Register Name	Address
TCPWM_CNT7_INTR_MASKED	0x402002FC

6.1.1 TCPWM_CNT0_CTRL

Counter control register

Address: 0x40200100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

6.1.1 TCPWM_CNT0_CTRL (continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

6.1.1 TCPWM_CNT0_CTRL (continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

6.1.2 TCPWM_CNT0_STATUS

Counter status register

Address: 0x40200104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

6.1.3 TCPWM_CNT0_COUNTER

Counter count register

Address: 0x40200108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

6.1.4 TCPWM_CNT0_CC

Counter compare/capture register

Address: 0x4020010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

6.1.5 TCPWM_CNT0_CC_BUFF

Counter buffered compare/capture register

Address: 0x40200110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

6.1.6 TCPWM_CNT0_PERIOD

Counter period register

Address: 0x40200114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

6.1.7 TCPWM_CNT0_PERIOD_BUFF

Counter buffered period register

Address: 0x40200118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

6.1.8 TCPWM_CNT0_TR_CTRL0

Counter trigger control register 0

Address: 0x40200120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

6.1.8 TCPWM_CNT0_TR_CTRL0 (continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

6.1.9 TCPWM_CNT0_TR_CTRL1

Counter trigger control register 1

Address: 0x40200124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

6.1.9 TCPWM_CNT0_TR_CTRL1 (continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

6.1.10 TCPWM_CNT0_TR_CTRL2

Counter trigger control register 2

Address: 0x40200128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

6.1.10 TCPWM_CNT0_TR_CTRL2 (continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

6.1.11 TCPWM_CNT0_INTR

Interrupt request register.

Address: 0x40200130

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

6.1.12 TCPWM_CNT0_INTR_SET

Interrupt set request register.

Address: 0x40200134

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

6.1.13 TCPWM_CNT0_INTR_MASK

Interrupt mask register.

Address: 0x40200138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

6.1.14 TCPWM_CNT0_INTR_MASKED

Interrupt masked request register

Address: 0x4020013C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

6.1.15 TCPWM_CNT1_CTRL

Counter control register

Address: 0x40200140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

6.1.15 TCPWM_CNT1_CTRL (continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

6.1.15 TCPWM_CNT1_CTRL (continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

6.1.16 TCPWM_CNT1_STATUS

Counter status register

Address: 0x40200144

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

6.1.17 TCPWM_CNT1_COUNTER

Counter count register

Address: 0x40200148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

6.1.18 TCPWM_CNT1_CC

Counter compare/capture register

Address: 0x4020014C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

6.1.19 TCPWM_CNT1_CC_BUFF

Counter buffered compare/capture register

Address: 0x40200150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

6.1.20 TCPWM_CNT1_PERIOD

Counter period register

Address: 0x40200154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

6.1.21 TCPWM_CNT1_PERIOD_BUFF

Counter buffered period register

Address: 0x40200158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

6.1.22 TCPWM_CNT1_TR_CTRL0

Counter trigger control register 0

Address: 0x40200160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

6.1.22 TCPWM_CNT1_TR_CTRL0 (continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

6.1.23 TCPWM_CNT1_TR_CTRL1

Counter trigger control register 1

Address: 0x40200164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

6.1.23 TCPWM_CNT1_TR_CTRL1 (continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

6.1.24 TCPWM_CNT1_TR_CTRL2

Counter trigger control register 2

Address: 0x40200168

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

6.1.24 TCPWM_CNT1_TR_CTRL2 (continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

6.1.25 TCPWM_CNT1_INTR

Interrupt request register.

Address: 0x40200170

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

6.1.26 TCPWM_CNT1_INTR_SET

Interrupt set request register.

Address: 0x40200174

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

6.1.27 TCPWM_CNT1_INTR_MASK

Interrupt mask register.

Address: 0x40200178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

6.1.28 TCPWM_CNT1_INTR_MASKED

Interrupt masked request register

Address: 0x4020017C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

6.1.29 TCPWM_CNT2_CTRL

Counter control register

Address: 0x40200180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

6.1.29 TCPWM_CNT2_CTRL (continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

6.1.29 TCPWM_CNT2_CTRL (continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

6.1.30 TCPWM_CNT2_STATUS

Counter status register

Address: 0x40200184

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

6.1.31 TCPWM_CNT2_COUNTER

Counter count register

Address: 0x40200188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

6.1.32 TCPWM_CNT2_CC

Counter compare/capture register

Address: 0x4020018C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

6.1.33 TCPWM_CNT2_CC_BUFF

Counter buffered compare/capture register

Address: 0x40200190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

6.1.34 TCPWM_CNT2_PERIOD

Counter period register

Address: 0x40200194

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

6.1.35 TCPWM_CNT2_PERIOD_BUFF

Counter buffered period register

Address: 0x40200198

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

6.1.36 TCPWM_CNT2_TR_CTRL0

Counter trigger control register 0

Address: 0x402001A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

6.1.36 TCPWM_CNT2_TR_CTRL0 (continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

6.1.37 TCPWM_CNT2_TR_CTRL1

Counter trigger control register 1

Address: 0x402001A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

6.1.37 TCPWM_CNT2_TR_CTRL1 (continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

6.1.38 TCPWM_CNT2_TR_CTRL2

Counter trigger control register 2

Address: 0x402001A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

6.1.38 TCPWM_CNT2_TR_CTRL2 (continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

6.1.39 TCPWM_CNT2_INTR

Interrupt request register.

Address: 0x402001B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

6.1.40 TCPWM_CNT2_INTR_SET

Interrupt set request register.

Address: 0x402001B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

6.1.41 TCPWM_CNT2_INTR_MASK

Interrupt mask register.

Address: 0x402001B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

6.1.42 TCPWM_CNT2_INTR_MASKED

Interrupt masked request register

Address: 0x402001BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

6.1.43 TCPWM_CNT3_CTRL

Counter control register

Address: 0x402001C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

6.1.43 TCPWM_CNT3_CTRL (continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

6.1.43 TCPWM_CNT3_CTRL (continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

6.1.44 TCPWM_CNT3_STATUS

Counter status register

Address: 0x402001C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

6.1.45 TCPWM_CNT3_COUNTER

Counter count register

Address: 0x402001C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

6.1.46 TCPWM_CNT3_CC

Counter compare/capture register

Address: 0x402001CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

6.1.47 TCPWM_CNT3_CC_BUFF

Counter buffered compare/capture register

Address: 0x402001D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

6.1.48 TCPWM_CNT3_PERIOD

Counter period register

Address: 0x402001D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

6.1.49 TCPWM_CNT3_PERIOD_BUFF

Counter buffered period register

Address: 0x402001D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

6.1.50 TCPWM_CNT3_TR_CTRL0

Counter trigger control register 0

Address: 0x402001E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

6.1.50 TCPWM_CNT3_TR_CTRL0 (continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

6.1.51 TCPWM_CNT3_TR_CTRL1

Counter trigger control register 1

Address: 0x402001E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

6.1.51 TCPWM_CNT3_TR_CTRL1 (continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

6.1.52 TCPWM_CNT3_TR_CTRL2

Counter trigger control register 2

Address: 0x402001E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

6.1.52 TCPWM_CNT3_TR_CTRL2 (continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

6.1.53 TCPWM_CNT3_INTR

Interrupt request register.

Address: 0x402001F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

6.1.54 TCPWM_CNT3_INTR_SET

Interrupt set request register.

Address: 0x402001F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

6.1.55 TCPWM_CNT3_INTR_MASK

Interrupt mask register.

Address: 0x402001F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

6.1.56 TCPWM_CNT3_INTR_MASKED

Interrupt masked request register

Address: 0x402001FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

6.1.57 TCPWM_CNT4_CTRL

Counter control register

Address: 0x40200200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

6.1.57 TCPWM_CNT4_CTRL (continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

6.1.57 TCPWM_CNT4_CTRL (continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

6.1.58 TCPWM_CNT4_STATUS

Counter status register

Address: 0x40200204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

6.1.59 TCPWM_CNT4_COUNTER

Counter count register

Address: 0x40200208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

6.1.60 TCPWM_CNT4_CC

Counter compare/capture register

Address: 0x4020020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

6.1.61 TCPWM_CNT4_CC_BUFF

Counter buffered compare/capture register

Address: 0x40200210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

6.1.62 TCPWM_CNT4_PERIOD

Counter period register

Address: 0x40200214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

6.1.63 TCPWM_CNT4_PERIOD_BUFF

Counter buffered period register

Address: 0x40200218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

6.1.64 TCPWM_CNT4_TR_CTRL0

Counter trigger control register 0

Address: 0x40200220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

6.1.64 TCPWM_CNT4_TR_CTRL0 (continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

6.1.65 TCPWM_CNT4_TR_CTRL1

Counter trigger control register 1

Address: 0x40200224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

6.1.65 TCPWM_CNT4_TR_CTRL1 (continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

6.1.66 TCPWM_CNT4_TR_CTRL2

Counter trigger control register 2

Address: 0x40200228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

6.1.66 TCPWM_CNT4_TR_CTRL2 (continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

6.1.67 TCPWM_CNT4_INTR

Interrupt request register.

Address: 0x40200230

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

6.1.68 TCPWM_CNT4_INTR_SET

Interrupt set request register.

Address: 0x40200234

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

6.1.69 TCPWM_CNT4_INTR_MASK

Interrupt mask register.

Address: 0x40200238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

6.1.70 TCPWM_CNT4_INTR_MASKED

Interrupt masked request register

Address: 0x4020023C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

6.1.71 TCPWM_CNT5_CTRL

Counter control register

Address: 0x40200240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

6.1.71 TCPWM_CNT5_CTRL (continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

6.1.71 TCPWM_CNT5_CTRL (continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

6.1.72 TCPWM_CNT5_STATUS

Counter status register

Address: 0x40200244

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

6.1.73 TCPWM_CNT5_COUNTER

Counter count register

Address: 0x40200248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

6.1.74 TCPWM_CNT5_CC

Counter compare/capture register

Address: 0x4020024C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

6.1.75 TCPWM_CNT5_CC_BUFF

Counter buffered compare/capture register

Address: 0x40200250

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

6.1.76 TCPWM_CNT5_PERIOD

Counter period register

Address: 0x40200254

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

6.1.77 TCPWM_CNT5_PERIOD_BUFF

Counter buffered period register

Address: 0x40200258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

6.1.78 TCPWM_CNT5_TR_CTRL0

Counter trigger control register 0

Address: 0x40200260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

6.1.78 TCPWM_CNT5_TR_CTRL0 (continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

6.1.79 TCPWM_CNT5_TR_CTRL1

Counter trigger control register 1

Address: 0x40200264

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

6.1.79 TCPWM_CNT5_TR_CTRL1 (continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

6.1.80 TCPWM_CNT5_TR_CTRL2

Counter trigger control register 2

Address: 0x40200268

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

6.1.80 TCPWM_CNT5_TR_CTRL2 (continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

6.1.81 TCPWM_CNT5_INTR

Interrupt request register.

Address: 0x40200270

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

6.1.82 TCPWM_CNT5_INTR_SET

Interrupt set request register.

Address: 0x40200274

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

6.1.83 TCPWM_CNT5_INTR_MASK

Interrupt mask register.

Address: 0x40200278

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

6.1.84 TCPWM_CNT5_INTR_MASKED

Interrupt masked request register

Address: 0x4020027C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

6.1.85 TCPWM_CNT6_CTRL

Counter control register

Address: 0x40200280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

6.1.85 TCPWM_CNT6_CTRL (continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

6.1.85 TCPWM_CNT6_CTRL (continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

6.1.86 TCPWM_CNT6_STATUS

Counter status register

Address: 0x40200284

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

6.1.87 TCPWM_CNT6_COUNTER

Counter count register

Address: 0x40200288

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

6.1.88 TCPWM_CNT6_CC

Counter compare/capture register

Address: 0x4020028C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

6.1.89 TCPWM_CNT6_CC_BUFF

Counter buffered compare/capture register

Address: 0x40200290

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

6.1.90 TCPWM_CNT6_PERIOD

Counter period register

Address: 0x40200294

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

6.1.91 TCPWM_CNT6_PERIOD_BUFF

Counter buffered period register

Address: 0x40200298

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

6.1.92 TCPWM_CNT6_TR_CTRL0

Counter trigger control register 0

Address: 0x402002A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

6.1.92 TCPWM_CNT6_TR_CTRL0 (continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

6.1.93 TCPWM_CNT6_TR_CTRL1

Counter trigger control register 1

Address: 0x402002A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

6.1.93 TCPWM_CNT6_TR_CTRL1 (continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

6.1.94 TCPWM_CNT6_TR_CTRL2

Counter trigger control register 2

Address: 0x402002A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

6.1.94 TCPWM_CNT6_TR_CTRL2 (continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

6.1.95 TCPWM_CNT6_INTR

Interrupt request register.

Address: 0x402002B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

6.1.96 TCPWM_CNT6_INTR_SET

Interrupt set request register.

Address: 0x402002B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

6.1.97 TCPWM_CNT6_INTR_MASK

Interrupt mask register.

Address: 0x402002B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

6.1.98 TCPWM_CNT6_INTR_MASKED

Interrupt masked request register

Address: 0x402002BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

6.1.99 TCPWM_CNT7_CTRL

Counter control register

Address: 0x402002C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

6.1.99 TCPWM_CNT7_CTRL (continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

6.1.99 TCPWM_CNT7_CTRL (continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

6.1.100 TCPWM_CNT7_STATUS

Counter status register

Address: 0x402002C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

6.1.101 TCPWM_CNT7_COUNTER

Counter count register

Address: 0x402002C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

6.1.102 TCPWM_CNT7_CC

Counter compare/capture register

Address: 0x402002CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

6.1.103 TCPWM_CNT7_CC_BUFF

Counter buffered compare/capture register

Address: 0x402002D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

6.1.104 TCPWM_CNT7_PERIOD

Counter period register

Address: 0x402002D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

6.1.105 TCPWM_CNT7_PERIOD_BUFF

Counter buffered period register

Address: 0x402002D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

6.1.106 TCPWM_CNT7_TR_CTRL0

Counter trigger control register 0

Address: 0x402002E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

6.1.106 TCPWM_CNT7_TR_CTRL0 (continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

6.1.107 TCPWM_CNT7_TR_CTRL1

Counter trigger control register 1

Address: 0x402002E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

6.1.107 TCPWM_CNT7_TR_CTRL1 (continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

6.1.108 TCPWM_CNT7_TR_CTRL2

Counter trigger control register 2

Address: 0x402002E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

6.1.108 TCPWM_CNT7_TR_CTRL2 (continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

6.1.109 TCPWM_CNT7_INTR

Interrupt request register.

Address: 0x402002F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

6.1.110 TCPWM_CNT7_INTR_SET

Interrupt set request register.

Address: 0x402002F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

6.1.111 TCPWM_CNT7_INTR_MASK

Interrupt mask register.

Address: 0x402002F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

6.1.112 TCPWM_CNT7_INTR_MASKED

Interrupt masked request register

Address: 0x402002FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

7 System Resource Sub System Registers

This section discusses the CORE registers. It lists all the registers in mapping tables, in address order.

7.1 Register Details

Register Name	Address
PWR_CONTROL	0x400B0000
PWR_INTR	0x400B0004
PWR_INTR_MASK	0x400B0008
PWR_KEY_DELAY	0x400B000C
PWR_VMON_CONFIG	0x400B0018
PWR_BOD_KEY	0x400B0028
PWR_STOP	0x400B002C
CLK_SELECT	0x400B0100
CLK_ILO_CONFIG	0x400B0104
CLK_IMO_CONFIG	0x400B0108
CLK_IMO_SPREAD	0x400B010C
WDT_CTRLOW	0x400B0200
WDT_CTRHIGH	0x400B0204
WDT_MATCH	0x400B0208
WDT_CONFIG	0x400B020C
WDT_CONTROL	0x400B0210
RES_CAUSE	0x400B0300
PWR_BG_TRIM3	0x400BFF18
PWR_BG_TRIM4	0x400BFF1C
PWR_BG_TRIM5	0x400BFF20
CLK_IMO_TRIM1	0x400BFF28
CLK_IMO_TRIM2	0x400BFF2C
PWR_RSVD_TRIM	0x400BFF38

7.1.1 PWR_CONTROL

Power Mode Control

Address: 0x400B0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R			
HW Access	None		RW	RW	RW			
Name	None [7:6]		LPM_READY	DEBUG_SESSION	POWER_MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None						
HW Access	R	None						
Name	EXT_VCCD	None [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW	RW1S	RW	None	RW1S	RW
HW Access	R	None	R	R	A	None	RW0C	R
Name	HIBER-NATE	None	LFCLK_SHORT	HIBERNATE_DISABLE	FIMO_DISABLE	None	HVMON_RELOAD	HVMON_ENABLE

Bits	Name	Description
31	HIBERNATE	Selects between HIBERNATE/DEEPSLEEP modes when Cortex-M0 enters low power mode (SleepDeep). Note: this bit is ignored when HIBERNATE_DISABLE=1. Default Value: 1 **0x0: DEEP_SLEEP:** Enter DeepSleep mode when CPU asserts SLEEPDEEP signal **0x1: HIBERNATE:** Enter Hibernate mode when CPU asserts SLEEPDEEP signal
29	LFCLK_SHORT	Short Vcclfclk and Vccdpslp power rails in DeepSleep power mode. This mode selection affects the accuracy specifications of the ILO oscillator due to supply noise. See Data Sheet for more details. 0: Do not short power domains 1: Short power domains Default Value: 0

7.1.1 PWR_CONTROL (continued)

28	HIBERNATE_DISABLE	0: Normal operation, HIBERNATE works as described 1: HIBERNATE bit is ignored, Hibernate mode is permanently disabled (part will go to DeepSleep instead. Note: This bit is a write-once bit until the next reset. Default Value: 0
27	FIMO_DISABLE	This bit is asserted during the boot process 0: Forces IMO to operate at 12MHz, ignore its frequency and trim settings and operate independent on its external references. 1: Turns IMO into normal operational mode Default Value: 0
25	HVMON_RELOAD	Firmware writes 1 to reload HV State in hibernate shadow copy. Hardware clears this bit after reload was successful. Wait at least 9 cycles after writing/recalling NVL before reloading the HVMON. Default Value: 0
24	HVMON_ENABLE	0: HV State Monitoring is disabled 1: HV State Monitoring is automatically enable by sleep controller Default Value: 1
23	EXT_VCCD	Should be set by firmware if Vccd is provided externally (on Vccd pin). Setting this bit turns off the active regulator and will lead to system reset (PBOD) unless both Vddd and Vccd pins are supplied externally. Default Value: 0
5	LPM_READY	Indicates whether the low power mode regulators are ready to enter DEEPSLEEP or HIBERNATE mode. 0: If DEEPSLEEP or HIBERNATE mode is requested, device will enter SLEEP mode. When low power regulators are ready, device will automatically enter the originally requested mode. 1: Normal operation. DEEPSLEEP and HIBERNATE work as described. Default Value: 0
4	DEBUG_SESSION	Indicates whether a debug session is active (CDBGPWRUPREQ signal is 1) Default Value: 0 **0x0: NO_SESSION:** No debug session active **0x1: SESSION_ACTIVE:** Debug session is active
3 : 0	POWER_MODE	Current power mode of the device. Note that this field cannot be read in all power modes on actual silicon. Default Value: 0 **0x0: RESET:** RESET state **0x1: ACTIVE:** ACTIVE state **0x2: SLEEP:** SLEEP state **0x3: DEEP_SLEEP:** DEEP_SLEEP state **0x4: HIBERNATE:** HIBERNATE state

7.1.2 PWR_INTR

Power System Interrupt Register

Address: 0x400B0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	None
HW Access	None						A	None
Name	None [7:2]						LVD	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	LVD	Indicates an Low Voltage Detect interrupt Default Value: 0

7.1.3 PWR_INTR_MASK

Power System Interrupt Mask Register

Address: 0x400B0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	None
HW Access	None						R	None
Name	None [7:2]						LVD	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	LVD	1: Propagate interrupt to CPU Default Value: 0

7.1.4 PWR_KEY_DELAY

Power System Key Register

Address: 0x400B000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: 780

7.1.5 PWR_VMON_CONFIG

Voltage Monitoring Trim and Configuration

Address: 0x400B0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				RW
HW Access	R			R				R
Name	RESERVED			LVD_SEL [4:1]				LVD_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						RESERVED	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	RESERVED	Reserved Default Value: 0
7 : 5	RESERVED	Reserved Default Value: 0

7.1.5 PWR_VMON_CONFIG (continued)

4 : 1	LVD_SEL	Threshold selection for Low Voltage Detect circuit. Disable the LVD (LVD_EN=0) before changing the threshold. Threshold variation is +/- 2.5% from these typical voltage choices: 0: 1.7500 V 1: 1.8000 V 2: 1.9000 V 3: 2.0000 V 4: 2.1000 V 5: 2.2000 V 6: 2.3000 V 7: 2.4000 V 8: 2.5000 V 9: 2.6000 V 10: 2.7000 V 11: 2.8000 V 12: 2.9000 V 13: 3.0000 V 14: 3.2000 V 15: 4.5000 V Default Value: 0
0	LVD_EN	Enable Low Voltage Detect circuit. Default Value: 0

7.1.6 PWR_BOD_KEY

BOD Detection Key

Address: 0x400B0028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	KEY16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	KEY16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	KEY16	To detect brown-outs firmware should do this on boot: 1. Set key= KEY16 2. Set KEY16= 0x3A71 3. If key==0x3A71 this was a brown-out event. Default Value: X

7.1.7 PWR_STOP

STOP Mode Register

Address: 0x400B002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	TOKEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	UNLOCK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						A	A
Name	None [23:18]						FREEZE	POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	STOP	None [30:24]						

Bits	Name	Description
31	STOP	Firmware sets this bit to enter STOP mode. Both UNLOCK and FREEZE must have been set correctly in a previous write operation. Otherwise, writes to this bit will affect the freeze override but will not actually set the STOP bit. The system will enter STOP mode immediately after writing to this bit and will wakeup only in response to XRES or WAKEUP event. Default Value: 0
17	FREEZE	Firmware sets this bit to freeze the configuration, mode and state of all GPIOs and SIOs in the system. Two identical write cycles are required to freeze the IO explicitly. The first cycle instructs DEEPSLEEP and HIBERNATE peripherals whether they can override upcoming freeze command(s). UNLOCK setting does not affect this. If firmware writes FREEZE=1 and STOP=0, peripherals can override the freeze and remain functional according to their configuration. If firmware writes FREEZE=1 and STOP=1, peripherals cannot override the next freeze command. The second write cycle freezes the IO if UNLOCK is set and the peripheral does not override the freeze. While FREEZE=1, peripherals will automatically freeze according to the override directive when entering DEEPSLEEP or HIBERNATE, regardless of the UNLOCK setting. Default Value: 0
16	POLARITY	0: WAKEUP=0 will wakeup the part from STOP 1: WAKEUP=1 will wakeup the part from STOP Default Value: 0

7.1.7 PWR_STOP (continued)

15 : 8	UNLOCK	This byte must be set to 0x3A for FREEZE or STOP fields to operate. Any other value in this register will cause FREEZE/STOP to have no effect, except as noted in the FREEZE description. Default Value: 0
7 : 0	TOKEN	Contains a 8-bit token that is retained through a STOP/WAKEUP sequence that can be used by firmware to differentiate WAKEUP from a general RESET event. Note that waking up from STOP using XRES will reset this register. Default Value: 0

7.1.8 CLK_SELECT

Clock Select Register

Address: 0x400B0100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	PLL_SEL [7:6]		DBL_SEL [5:3]			DIRECT_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW			RW
HW Access	A		R		R			R
Name	WDT_LOCK [15:14]		DPLLREF_SEL [13:12]		DPLLIN_SEL [11:9]			PLL_SEL

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW			RW	RW	
HW Access	None		R			R	R	
Name	None [23:22]		SYSCLK_DIV [21:19]			HALF_EN	HFCLK_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 19	SYSCLK_DIV	SYSCLK Pre-Scaler Value. Default Value: 0 **0x0: NO_DIV:** SYSCLK= HFCLK/1 **0x1: DIV_BY_2:** SYSCLK= HFCLK/2 **0x2: DIV_BY_4:** SYSCLK= HFCLK/4 **0x3: DIV_BY_8:** SYSCLK= HFCLK/8 **0x4: DIV_BY_16:** SYSCLK= HFCLK/16 **0x5: DIV_BY_32:** SYSCLK= HFCLK/32 **0x6: DIV_BY_64:** SYSCLK= HFCLK/64

7.1.8 CLK_SELECT (continued)

		0x7: DIV_BY_128: SYSCLK= HFCLK/128
18	HALF_EN	FLASH Wait-state selection. This must be set to 1 when clk_sys is set to a frequency greater than 24MHz. 0: Access FLASH using 0 wait-states. Only use this setting when HFCLK is <=24MHz. 1: Access FLASH using 1 wait-state. Safe to use this setting for any clock frequency. Default Value: 0
17 : 16	HFCLK_SEL	Selects the source for HFCLK. Default Value: 0 **0x0: DIRECT_SEL:** Source selected by DIRECT_SEL **0x1: DBL:** Output of DBL (Doubler)
15 : 14	WDT_LOCK	Prohibits writing to WDT_* registers and CLK_ILO/WCO_CONFIG registers when not equal 0. Requires at least two different writes to unlock. Note that this field is 2 bits to force multiple writes only. It represents only a single write protect signal protecting all WATCHDOG registers at the same time. Default Value: 0 **0x0: NO_CHG:** No effect **0x1: CLR0:** Clears bit 0 **0x2: CLR1:** Clears bit 1 **0x3: SET01:** Sets both bits 0 and 1
13 : 12	DPLLREF_SEL	Reserved **0x0: DSI0:** DSI_OUT[0] **0x1: DSI1:** DSI_OUT[1] **0x2: DSI2:** DSI_OUT[2] **0x3: DSI3:** DSI_OUT[3]
11 : 9	DPLLIN_SEL	Selects a source for the input of DPLL. Selecting a clock source that is not supported will result in undefined behavior. Default Value: 0 **0x0: IMO:** IMO - Internal R/C Oscillator **0x1: EXTCLK:** EXTCLK - External Clock Pin **0x2: ECO:** ECO - External Crystal Oscillator

7.1.8 CLK_SELECT (continued)

		0x4: DSI0: DSI_OUT[0] **0x5: DSI1:** DSI_OUT[1] **0x6: DSI2:** DSI_OUT[2] **0x7: DSI3:** DSI_OUT[3]
8 : 6	PLL_SEL	Reserved **0x0: IMO:** IMO - Internal R/C Oscillator **0x1: EXTCLK:** EXTCLK - External Clock Pin **0x2: ECO:** ECO - Internal Crystal Oscillator **0x3: DPLL:** DPLL - DPLL Output **0x4: DSI0:** DSI_OUT[0] **0x5: DSI1:** DSI_OUT[1] **0x6: DSI2:** DSI_OUT[2] **0x7: DSI3:** DSI_OUT[3]
5 : 3	DBL_SEL	Selects a source the input of EXCO PLL1, if supported. Default Value: 0 **0x0: IMO:** IMO - Internal R/C Oscillator **0x1: EXTCLK:** EXTCLK - External Clock Pin **0x2: ECO:** ECO - External Crystal Oscillator **0x4: DSI0:** DSI_OUT[0] **0x5: DSI1:** DSI_OUT[1] **0x6: DSI2:** DSI_OUT[2] **0x7: DSI3:** DSI_OUT[3]
2 : 0	DIRECT_SEL	Selects a source for HFCLK (when HFCLK_SEL=0) and DSI_IN[0]. Note that using DSI_OUT[3:0] as HFCLK source will result in undefined behaviour. These values are available strictly to provide a clock in DSI_IN[0]. Default Value: 0

7.1.8 CLK_SELECT (continued)

0x0: IMO:
IMO - Internal R/C Oscillator

0x1: EXTCLK:
EXTCLK - External Clock Pin

0x2: ECO:
ECO - External Crystal Oscillator

0x4: DSI0:
DSI_OUT[0]

0x5: DSI1:
DSI_OUT[1]

0x6: DSI2:
DSI_OUT[2]

0x7: DSI3:
DSI_OUT[3]

7.1.9 CLK_ILO_CONFIG

ILO Configuration

Address: 0x400B0104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					SATBIAS	TURBO	PD_MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Master enable for ILO oscillator Default Value: 0
2	SATBIAS	Reserved
1	TURBO	Turbo mode for faster startup from coma power down 0: turbo disabled 1: turbo enabled Default Value: 1
0	PD_MODE	Power down mode. Note: this bit must always be set to 0 and never changed. Behavior is un-defined when set to 1. Default Value: 0 **0x0: SLEEP:**

7.1.9 CLK_ILO_CONFIG (continued)

0x1: COMA:
Coma (slower startup)

7.1.10 CLK_IMO_CONFIG

IMO Configuration

Address: 0x400B0108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	EN_FASTBIAS	FLASHPUMP_SEL	None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW			RW
HW Access	R	R	R	R	R			R
Name	ENABLE	EN_CLK2X	EN_CLK36	TEST_USB_MODE	PUMP_SEL [27:25]			TEST_FASTBIAS

Bits	Name	Description
31	ENABLE	Master enable for IMO oscillator. Clearing this bit will disable the IMO but not disconnect it from the power rail. Default Value: 1
30	EN_CLK2X	Reserved
29	EN_CLK36	Enables 36MHz secondary oscillator that can be used for Pump or Flash Pump. Note: Since there are two consumers of the 36MHz clock, care should be taken when clearing this bit. The correct procedure for clearing this bit is: 1. Disable interrupts 2. Check if both FLASHPUMP_SEL bit is 1 and PUMP_SEL bit field is 3 3. If so, set EN_CLK36=0 4. Enable interrupts Default Value: 0
28	TEST_USB_MODE	Reserved

7.1.10 CLK_IMO_CONFIG (continued)

27 : 25	PUMP_SEL	Selects operating source for Pump clock. This clock is not guaranteed to be glitch free when changing IMO parameters or clock divider settings. 5-7: reserved, do not use Default Value: 0 **0x0: GND:** No clock, connect to gnd **0x1: IMO:** Use main IMO output **0x2: DBL:** Use doubler output **0x3: CLK36:** Use 36MHz oscillator. Note: always set EN_CLK36 when selecting this value for PUMP_SEL. Flash program/erase operations will set EN_CLK36=0 when PUMP_SEL!=CLK36. **0x4: FF1:** Use divided clock FF1
24	TEST_FASTBIAS	Reserved
23	EN_FASTBIAS	Reserved
22	FLASHPUMP_SEL	Selects operating source for SPCIF Timer/Flash Pump clock. Default Value: 0 **0x0: GND:** No clock, connect to gnd **0x1: CLK36:** Use 36MHz oscillator

7.1.11 CLK_IMO_SPREAD

IMO Spread Spectrum Configuration

Address: 0x400B010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				A			
Name	None [7:5]				SS_VALUE [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:13]				SS_MAX [12:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		None			
HW Access	R		R		None			
Name	SS_MODE [31:30]		SS_RANGE [29:28]		None [27:24]			

Bits	Name	Description
31 : 30	SS_MODE	Spread Spectrum Mode. Default Value: 0 **0x0: OFF:** Off, do not change SS_VALUE **0x1: TRIANGLE:** Modulate using triangle wave (see SS_MAX) **0x2: LFSR:** Modulate using pseudo random sequence (using LFSR) **0x3: DSI:** Take value directly from DSI (synchronized by divided clock FF1)
29 : 28	SS_RANGE	Spread spectrum range (downspread when SS_VALUE=16). 3: reserved, do not use Default Value: 0 **0x0: M1:** 0 .. -1%

7.1.11 CLK_IMO_SPREAD (continued)

		0x1: M2: 0 .. -2% **0x2: M4:** 0 .. -4%
12 : 8	SS_MAX	Maximum counter value for spread spectrum. Counter will count from 0..SS_MAX..0 and keep repeating this indefinitely. Only works when SS_MODE=1. Default Value: 0
4 : 0	SS_VALUE	Current offset value for spread spectrum modulation. IMO supports values 0..16. Step size is determined by SS_RANGE. Value is encoded in proper thermometric format for IMO in hardware. Value can be modified in firmware only when SS_MODE=0. Default Value: 0

7.1.12 WDT_CTRLOW

Watchdog Counters 0/1

Address: 0x400B0200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WDT_CTR0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WDT_CTR0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WDT_CTR1 [7:0]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WDT_CTR1 [15:8]							

Bits	Name	Description
31 : 16	WDT_CTR1	Current value of WDT Counter 1 Default Value: 0
15 : 0	WDT_CTR0	Current value of WDT Counter 0 Default Value: 0

7.1.13 WDT_CTRHIGH

Watchdog Counter 2

Address: 0x400B0204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [31:24]							

Bits	Name	Description
31 : 0	WDT_CTR2	Current value of WDT Counter 2 Default Value: 0

7.1.14 WDT_MATCH

Watchdog counter match values

Address: 0x400B0208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [7:0]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [15:8]							

Bits	Name	Description
31 : 16	WDT_MATCH1	Match value for Watchdog Counter 1 Default Value: 0
15 : 0	WDT_MATCH0	Match value for Watchdog Counter 0 Default Value: 0

7.1.15 WDT_CONFIG

Watchdog Counters Configuration

Address: 0x400B020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [7:4]				WDT_CASCADE0_1	WDT_CLEAR0	WDT_MODE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [15:12]				WDT_CASCADE1_2	WDT_CLEAR1	WDT_MODE1 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							WDT_MODE2

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None	RW				
HW Access	R		None	R				
Name	LFCLK_SEL [31:30]		None	WDT_BITS2 [28:24]				

Bits	Name	Description
31 : 30	LFCLK_SEL	Select source for LFCLK: 0: ILO - Internal R/C Oscillator 1: WCO - Internal Crystal Oscillator 2-3: Reserved - do not use To safely change LFCLK_SEL wait for WDT_CTRLOW/WDT_CTRHIGH to change then change the setting immediately. Default Value: 0
28 : 24	WDT_BITS2	Bit to observe for WDT_INT2: 0: Assert when bit0 of WDT_CTR2 toggles (one int every tick) .. 31: Assert when bit31 of WDT_CTR2 toggles (one int every 2^31 ticks) Default Value: 0
16	WDT_MODE2	Watchdog Counter 2 Mode. Default Value: 0 **0x0: NOTHING:** Free running counter with no interrupt requests

7.1.15 WDT_CONFIG (continued)

		0x1: INT: Free running counter with interrupt request when a specified bit in CTR2 toggles (see WDT_BITS2)
11	WDT_CASCADE1_2	Cascade Watchdog Counters 1,2. Counter 2 increments the cycle after WDT_CTR1=WDT_MATCH1. It is allowed to cascade all three WDT counters. 0: Independent counters 1: Cascaded counters Default Value: 0
10	WDT_CLEAR1	Clear Watchdog Counter when WDT_CTR1=WDT_MATCH1. In other words WDT_CTR1 divides LFCLK by (WDT_MATCH1+1). 0: Free running counter 1: Clear on match Default Value: 0
9 : 8	WDT_MODE1	Watchdog Counter Action on Match (WDT_CTR1=WDT_MATCH1). Default Value: 0 **0x0: NOTHING:** Do nothing **0x1: INT:** Assert WDT_INTx **0x2: RESET:** Assert WDT Reset **0x3: INT_THEN_RESET:** Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt
3	WDT_CASCADE0_1	Cascade Watchdog Counters 0,1. Counter 1 increments the cycle after WDT_CTR0=WDT_MATCH0. 0: Independent counters 1: Cascaded counters Default Value: 0
2	WDT_CLEAR0	Clear Watchdog Counter when WDT_CTR0=WDT_MATCH0. In other words WDT_CTR0 divides LFCLK by (WDT_MATCH0+1). 0: Free running counter 1: Clear on match Default Value: 0
1 : 0	WDT_MODE0	Watchdog Counter Action on Match (WDT_CTR0=WDT_MATCH0). Default Value: 0 **0x0: NOTHING:** Do nothing **0x1: INT:** Assert WDT_INTx **0x2: RESET:** Assert WDT Reset **0x3: INT_THEN_RESET:** Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt

7.1.16 WDT_CONTROL

Watchdog Counters Control

Address: 0x400B0210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [7:4]				WDT_RESET0	WDT_INT0	WDT_ENABLED0	WDT_ENABLE0

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [15:12]				WDT_RESET1	WDT_INT1	WDT_ENABLED1	WDT_ENABLE1

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [23:20]				WDT_RESET2	WDT_INT2	WDT_ENABLED2	WDT_ENABLE2

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	WDT_RESET2	Resets counter 2 back to 0000_0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Wait until the reset completes before enabling the WDT. Default Value: 0
18	WDT_INT2	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Default Value: 0
17	WDT_ENABLED2	Indicates actual state of counter. May lag WDT_ENABLE2 by up to 3 LFCLK cycles. After changing WDT_ENABLE2, do not enter DEEPSLEEP mode until this field acknowledges the change. Default Value: 0

7.1.16 WDT_CONTROL (continued)

16	WDT_ENABLE2	Enable Counter 2 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default Value: 0
11	WDT_RESET1	Resets counter 1 back to 0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Wait until the reset completes before enabling the WDT. Default Value: 0
10	WDT_INT1	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODEx=3. Default Value: 0
9	WDT_ENABLED1	Indicates actual state of counter. May lag WDT_ENABLE1 by up to 3 LFCLK cycles. After changing WDT_ENABLE1, do not enter DEEPSLEEP mode until this field acknowledges the change. Default Value: 0
8	WDT_ENABLE1	Enable Counter 1 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default Value: 0
3	WDT_RESET0	Resets counter 0 back to 0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Wait until the reset completes before enabling the WDT. Default Value: 0
2	WDT_INT0	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODEx=3. Default Value: 0
1	WDT_ENABLED0	Indicates actual state of counter. May lag WDT_ENABLE0 by up to 3 LFCLK cycles. After changing WDT_ENABLE0, do not enter DEEPSLEEP mode until this field acknowledges the change. Default Value: 0
0	WDT_ENABLE0	Enable Counter 0 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default Value: 0

7.1.17 RES_CAUSE

Reset Cause Observation Register

Address: 0x400B0300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	RESET_XRES	RESET_PBOD	RESET_HVBOD	RESET_SOFT	RESET_PROT_FAULT	RESET_LOCKUP	RESET_DSBOD	RESET_WDT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	RESET_XRES	This field is deprecated and will always read 0. Default Value: 0
6	RESET_PBOD	This field is deprecated and will always read 0. Default Value: 0
5	RESET_HVBOD	This field is deprecated and will always read 0. Default Value: 0
4	RESET_SOFT	Cortex-M0 requested a system reset through it's SYSRESETREQ. This can be done via a debugger probe or in firmware. Default Value: 0
3	RESET_PROT_FAULT	A protection violation occurred that requires a RESET. This includes, but is not limited to, hitting a debug breakpoint while in Privileged Mode. Default Value: 0
2	RESET_LOCKUP	This field is deprecated and will always read 0. Cortex-M0 LOCKUP is no longer a reset source. Default Value: 0
1	RESET_DSBOD	This field is deprecated and will always read 0. Default Value: 0

7.1.17 RES_CAUSE (continued)

0	RESET_WDT	A WatchDog Timer reset has occurred since last power cycle. Default Value: 0

7.1.18 PWR_BG_TRIM3

Bandgap Trim Register

Address: 0x400BFF18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW				RW		
HW Access	None	R				R		
Name	None	INL_CROSS_IMO [6:3]				INL_TRIM_IMO [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 3	INL_CROSS_IMO	IMO Irefgen INL cross-over point control for centering curve at 30C. Default Value: 11
2 : 0	INL_TRIM_IMO	IMO Irefgen nonlinear current trim for curvature correction. Default Value: 7

7.1.19 PWR_BG_TRIM4

Bandgap Trim Register

Address: 0x400BFF1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: 32

7.1.20 PWR_BG_TRIM5

Bandgap Trim Register

Address: 0x400BFF20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: 32

7.1.21 CLK_IMO_TRIM1

IMO Trim Register

Address: 0x400BFF28

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: 128

7.1.22 CLK_IMO_TRIM2

IMO Trim Register

Address: 0x400BFF2C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		FREQ [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	FREQ	Frequency to be selected (default 24MHz). Frequencies can be selected from 3..48MHz. When changing this field approriate values for IMO_CLK_TRIM1, PWR_BG_TRIM4 and PWR_BG_TRIM5 must be selected from trim tables determined at manufacturing time and stored in SFLASH. For encoding of this field a lookup table is required, where the frequency increases in 1MHz steps in the regions listed below. Unspecified values have undefined behavior. [3-12] => [3MHz-12MHz] [14-25] => [13MHz-24MHz] [27-35] => [25MHz-33MHz] [37-43] => [34MHz-40MHz] [46-53] => [41MHz-48MHz] Default Value: 25

7.1.23 PWR_RSVD_TRIM

Reserved, unused registers

Address: 0x400BFF38

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				RSVD_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	RSVD_TRIM	Reserved, unused registers. Default Value: 0

8 CPU Sub System (CPUSS) Registers

This section discusses the CPUSS registers. It lists all the registers in mapping tables, in address order.

8.1 Register Details

Register Name	Address
CPUSS_CONFIG	0x40100000
CPUSS_SYSREQ	0x40100004
CPUSS_SYSARG	0x40100008
CPUSS_INT_SEL	0x40100020
CPUSS_INT_MODE	0x40100024
CPUSS_NMI_MODE	0x40100028
CPUSS_FLASH_CTL	0x40100030
CPUSS_ROM_CTL	0x40100034
CPUSS_RAM_CTL	0x40100038
CPUSS_DMAC_CTL	0x4010003C
CPUSS_SL_CTL0	0x40100100
CPUSS_SL_CTL1	0x40100104
CPUSS_SL_CTL2	0x40100108

8.1.1 CPUSS_CONFIG

Configuration register

Address: 0x40100000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							VECT_IN_RAM

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	VECT_IN_RAM	0': Vector Table is located at 0x0000:0000 in flash '1': Vector Table is located at 0x2000:0000 in SRAM Note that vectors for RESET and FAULT are always fetched from ROM. Value in flash/RAM is ignored for these vectors. Default Value: 0

8.1.2 CPUSS_SYSREQ

SYSCALL control register

Address: 0x40100004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SYSCALL_COMMAND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	SYSCALL_COMMAND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	R	R	RW	RW	None		
HW Access	R	A	RW	A	R	None		
Name	SYSCALL_REQ	HMASTER_0	ROM_ACCESS_EN	PRIVI-LEGED	DIS_RESET_VECT_REL	None [26:24]		

Bits	Name	Description
31	SYSCALL_REQ	CPU/DAP writes a '1' to this field to request a SystemCall. The HMASTER_0 field indicates the source of the write access. Setting this field to '1' immediate results in a NMI. The SystemCall NMI interrupt handler sets this field to '0' after servicing the request. Default Value: 0
30	HMASTER_0	Indicates the source of the write access to the SYSREQ register. '0': CPU write access. '1': DAP write access. HW sets this field when the SYSREQ register is written to and SYSCALL_REQ is '0' (the last time it is set is when SW sets SYSCALL_REQ from '0' to '1'). Default Value: 0
29	ROM_ACCESS_EN	Indicates that executing from Boot ROM is enabled. HW sets this field to '1', on reset or when the SystemCall NMI vector is fetched from Boot ROM. HW sets this field to '0', when the CPU is NOT executing from either Boot or System ROM. This bit is used for debug purposes only. Default Value: 1

8.1.2 CPUSS_SYSREQ (continued)

28	PRIVILEGED	Indicates whether the system is in privileged ('1') or user mode ('0'). Only CPU SW executing from ROM can set this field to '1' when ROM_ACCESS_EN is '1' (the CPU is executing a SystemCall NMI interrupt handler). Any other write to this field sets is to '0'. This field is used as the AHB-Lite hprot[1] signal to implement Cypress proprietary user/privileged modes. These modes are used to enable/disable access to specific MMIO registers and memory regions. Default Value: 1
27	DIS_RESET_VECT_REL	Disable Reset Vector fetch relocation: '0': CPU accesses to locations 0x0000:0000 - 0x0000:0007 are redirected to ROM. '1': CPU accesses to locations 0x0000:0000 - 0x0000:0007 are made to flash. Note that this field defaults to '0' on reset, ensuring actual reset vector fetches are always made to ROM. Note that this field does not affect DAP accesses. Default Value: 0
15 : 0	SYSCALL_COMMAND	Opcode of the system call being requested. Default Value: 0

8.1.3 CPUSS_SYSARG

SYSARG control register

Address: 0x40100008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SYSCALL_ARG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	SYSCALL_ARG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	SYSCALL_ARG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	SYSCALL_ARG [31:24]							

Bits	Name	Description
31 : 0	SYSCALL_ARG	Argument to System Call specified in SYSREQ. Semantics of argument depends on system call made. Typically a pointer to a parameter block. Default Value: 0

8.1.4 CPUSS_INT_SEL

Interrupt multiplexer select register

Address: 0x40100020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DSI [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DSI [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DSI [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DSI [31:24]							

Bits	Name	Description
31 : 0	DSI	Specifies interrupt source: '0': Fixed Function. '1': DSI. When changing the source of a specific interrupt, it is advised to temporarily disable the interrupt using the CM0 NVIC's CLRENA and SETENA interrupt enable clear and set registers to prevent a spurious interrupt activation. In addition, the CM0 NVIC's CLRPEND interrupt pending clear register should be used clear a pending interrupt before re-enabling the interrupt. Default Value: 0

8.1.5 CPUSS_INT_MODE

DSI interrupt pulse mode register

Address: 0x40100024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DSI_INT_PULSE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DSI_INT_PULSE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DSI_INT_PULSE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DSI_INT_PULSE [31:24]							

Bits	Name	Description
31 : 0	DSI_INT_PULSE	Specifies DSI interrupt format: '0': level sensitive; i.e. no pulse generator. '1': pulse generator on rising edge. Default Value: 0

8.1.6 CPUSS_NMI_MODE

DSI NMI pulse mode register

Address: 0x40100028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							DSI_NMI_PULSE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	DSI_NMI_PULSE	Specifies DSI NMI format: '0': level sensitive; i.e. no pulse generator. '1': pulse generator on rising edge. Default Value: 0

8.1.7 CPUSS_FLASH_CTL

FLASH control register

Address: 0x40100030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			PREF_EN	None [3:2]		FLASH_WS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							RW1C
Name	None [15:9]							FLASH_INVALIDATE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	ARB	Arbitration policy: "0": CPU has priority "1": DW/DMA has priority "2": Roundrobin "3": Roundrobin - sticky Default Value: 0
8	FLASH_INVALIDATE	1': Invalidates the content of the flash controller's buffers. Default Value: 0
4	PREF_EN	Prefetch enable: '0': disabled. This is a desirable seeting when FLASH_WS is "0" or when predictable execution behavior is required. '1': enabled. Default Value: 0

8.1.7 CPUSS_FLASH_CTL (continued)

1 : 0	FLASH_WS	Amount of ROM wait states: "0": 0 wait states (fast flash: [0, 24] MHz system frequency, slow flash: [0, 16] MHz system frequency) "1": 1 wait state (fast flash: [24, 48] MHz system frequency, slow flash: [16, 32] MHz system frequency) "2": 2 wait states (slow flash: [32, 48] MHz system frequency) "3": undefined Default Value: 0

8.1.8 CPUSS_ROM_CTL

ROM control register

Address: 0x40100034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ROM_WS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ROM_WS	Reserved

8.1.9 CPUSS_RAM_CTL

RAM control register

Address: 0x40100038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	ARB	Arbitration policy: "0": CPU has priority "1": DW/DMA has priority "2": Roundrobin "3": Roundrobin - sticky Default Value: 0

8.1.10 CPUSS_DMAC_CTL

DMA controller register

Address: 0x4010003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	ARB	Arbitration policy: "0": CPU has priority "1": DW/DMA has priority "2": Roundrobin "3": Roundrobin - sticky Default Value: 0

8.1.11 CPUSS_SL_CTL0

Slave control register

Address: 0x40100100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	ARB	Arbitration policy: "0": CPU priority "1": DMA priority "2": Roundrobin "3": Roundrobin - sticky Default Value: 0

8.1.12 CPUSS_SL_CTL1

Slave control register

Address: 0x40100104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	ARB	Arbitration policy: "0": CPU priority "1": DMA priority "2": Roundrobin "3": Roundrobin - sticky Default Value: 0

8.1.13 CPUSS_SL_CTL2

Slave control register

Address: 0x40100108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	ARB	Arbitration policy: "0": CPU priority "1": DMA priority "2": Roundrobin "3": Roundrobin - sticky Default Value: 0

9 CapSense Sigma Delta (CSD) Registers

This section discusses the CSD registers. It lists all the registers in mapping tables, in address order.

9.1 Register Details

Register Name	Address
CSD0_ID	0x40280000
CSD0_CONFIG	0x40280004
CSD0_IDAC	0x40280008
CSD0_COUNTER	0x4028000C
CSD0_STATUS	0x40280010
CSD0_INTR	0x40280014
CSD0_INTR_SET	0x40280018
CSD0_PWM	0x4028001C
CSD0_TRIM1	0x4028FF00
CSD0_TRIM2	0x4028FF04
CSD1_ID	0x40290000
CSD1_CONFIG	0x40290004
CSD1_IDAC	0x40290008
CSD1_COUNTER	0x4029000C
CSD1_STATUS	0x40290010
CSD1_INTR	0x40290014
CSD1_INTR_SET	0x40290018
CSD1_PWM	0x4029001C
CSD1_TRIM1	0x4029FF00
CSD1_TRIM2	0x4029FF04

9.1.1 CSD0_ID

ID & Revision Number

Address: 0x40280000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	REVISION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	REVISION [31:24]							

Bits	Name	Description
31 : 16	REVISION	the version number is 0x0001 Default Value: 1
15 : 0	ID	the ID of CSD peripheral is 0xE0E1 Default Value: 57569

9.1.2 CSD0_CONFIG

Configuration and Control

Address: 0x40280004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW1S	RW	RW	RW	RW	RW
HW Access	R	R	RW1C	R	R	R	R	R
Name	PRS_12_8	PRS_SELECT	PRS_CLEAR	Reserved_1	FILTER_ENABLE	BYPASS_SEL	SAMPLE_SYNC	DSI_SAMPLE_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW		RW
HW Access	R	R	R	R	R	R		R
Name	COMP_PIN	COMP_MODE	REFBUF_EN	SENSE_EN	SENSE_COMP_BW	SHIELD_DELAY [10:9]		DSI_SENSE_EN

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	None	RW	RW	RW	RW
HW Access	R	R	R	None	R	R	RW	RW
Name	REFBUF_DRV	SENSE_INSEL	REBUF_OUTSEL	None	SENSE_COMP_EN	Reserved_2	POLARITY2	POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW			None	RW
HW Access	R	R	R	R			None	R
Name	ENABLE	Reserved_5	Reserved_4	Reserved_3 [28:26]			None	REFBUF_DRV

Bits	Name	Description
31	ENABLE	Master enable of the CSD IP. Must be set to 1 for any CSD operation to function. Default Value: 0
30	Reserved_5	Keep this bit at the default value Default Value: 0
29	Reserved_4	Keep this bit at the default value Default Value: 0
28 : 26	Reserved_3	Keep this field at the default value Default Value: 0
24 : 23	REFBUF_DRV	Current drive strength for reference buffer. Default Value: 0 **0x0: OFF:** Current drive mode OFF

9.1.2 CSD0_CONFIG (continued)

		0x1: DRV_1: Lowest current drive mode **0x2: DRV_2:** Mid current drive mode **0x3: DRV_3:** Highest current drive mode
22	SENSE_INSEL	Selects how the Cmodcapacitor is connected to CSD modulator Default Value: 0 **0x0: SENSE_CHANNEL1:** Direct connection from Cmod to CSD modulator; direct connection is called channel1 **0x1: SENSE_AMUXA:** Cmod capacitor is connected CSD modulator through AMUXBUS-A.
21	REBUF_OUTSEL	Selects which AMUXBUS the reference buffer connects to. Default Value: 1 **0x0: AMUXA:** Connect to AMUXBUS-A (not normally used). **0x1: AMUXB:** Connect to AMUXBUS-B (normally used for all CSD operations).
19	SENSE_COMP_EN	Turns on the sense comparator circuit. Must be done some time before enable SENSE_EN. 0: Sense comparator is powered off. 1: Sense comparator is powered on. Default Value: 0
18	Reserved_2	Keep this bit at the default value Default Value: 0
17	POLARITY2	For normal CSD operations this field is not used. When using the IDAC's for other-than-CSD purposes, this bit controls the IDAC2 polarity only. The IDAC register below provides the same functionality through POLARITY2_MIR bit. Default Value: 0 **0x0: VSSIO:** For non-CSD application, IDAC2 will source current. **0x1: VDDIO:** For non-CSD application, IDAC2 will sink current.
16	POLARITY	Selects the polarity of the sensing operation. When using the IDAC's for other-than-CSD purposes, this bit controls the IDAC1 polarity only. The IDAC register below provides the same functionality through POLARITY1_MIR bit. Default Value: 0 **0x0: VSSIO:** Normal: sensor switching between Vssio and Cmod. For non-CSD application, IDAC1 will source current. **0x1: VDDIO:** Inverted: sensor switch between Vddio and Cmod. For non-CSD application, IDAC1 will sink current.
15	COMP_PIN	Connects either the Cmod or Csh_tank sense return line to the reference buffer comparator. This switch must be set to the same pin that is being charged up by the reference buffer (through the AMUXBUS settings in GPIO). Default Value: 0

9.1.2 CSD0_CONFIG (continued)

		0x0: CHANNEL1: Use the sense line designated as "Channel 1"; this is normally used to conenct Cmod.
		0x1: CHANNEL2: Use the sense line designated as "Channel 2"; this is normally used to connect Csh_tank.
14	COMP_MODE	Selects between charging of the Cmod/Csh_tank capacitor using the GPIO digital output buffer or the CSD reference buffer. Note that using the GPIO requires proper configuraiton of the GPIO pin. Default Value: 0
		0x0: CHARGE_BUF: Use CSD Reference Buffer to charge capacitor. Capacitor must be connected to AMUXBUS-A/B (see REBUF_OUTSEL) and selected using COMP_PIN.
		0x1: CHARGE_IO: Use GPIO Driver to charge capacitor. Capacitor must be selected using COMP_PIN, and GPIO must be in AMUXBUS-B mode.
13	REFBUF_EN	Enables the reference buffer/comparator circuits for charging Cmod/Csh_tank using the mode selected in COMP_MODE. Default Value: 0
12	SENSE_EN	Enables the sensor and shield clocks, CSD modulator output and turns on the IDAC compensation current as selected by CSD_IDAC. Default Value: 0
11	SENSE_COMP_BW	Selects bandwidth for sensing comparator Default Value: 1
		0x0: LOW: Lower bandwidth
		0x1: HIGH: High bandwidth (default)
10 : 9	SHIELD_DELAY	Configures the delay between shield clock and sensor clock Default Value: 0
		0x0: OFF: Delay line is off; sensor clock = shield clock
		0x2: 50NS: shield clock is delayed by 50-100ns delay w.r.t sensor clock
		0x3: 10NS: shield clock is delayed by 10-20ns delay w.r.t sensor clock
8	DSI_SENSE_EN	DSI_SENSE_EN = 1-> sensor clock is driven directly by DSI DSI_SENSE_EN = 0-> sensor clock is driven by PRS/divide-by-2/DIRECT_CLOCK Set this bit at 0 (default) if DSI is not used in your design modify the CSD block Default Value: 0
7	PRS_12_8	Selects between 8-bit or 12-bit PRS sequence Default Value: 0
		0x0: 8B: 8-bit PRS sequence (G(x)=X^8+X^4+X^3+X^2+1, period= 255)
		0x1: 12B: 12-bit PRS sequence (G(x)=X^12+X^9+X^3+X^2+1, period=4095)
6	PRS_SELECT	Selects between PRS and divide-by-2 for sensor clock Default Value: 0

9.1.2 CSD0_CONFIG (continued)

		0x0: DIV2: divide-by-2 is source of sensor clock **0x1: PRS:** PRS is source of sensor clock
5	PRS_CLEAR	When set, forces the pseudo-random generator to it's initial state. Note that it may take some time for this setting to take effect depending on the clock frequency used for clk_csd1. Hardware clears this bit at the same time PRS is cleared. Default Value: 0
4	Reserved_1	Keep this bit at the default value Default Value: 0
3	FILTER_ENABLE	Enables the digital filtering on the CSD comparator Default Value: 0 **0x0: FILTER_OFF:** Digital Filter is OFF and has no effect. **0x1: FILTER_ON:** Digital Filter is ON. The digital filter disables the IDAC and sample COUNTER, regardless of CSD comparator state, for 1 clk_csd2 clock cycle after the start of each measurement and from the first comparator trip to the end of each measurement.
2	BYPASS_SEL	Selects the source of sensor clock. Default Value: 0 **0x0: PRS_OR_DIV2:** Select divide-by-2 or pseudo-random sequence as source of sensor clock(see PRS_SELECT) **0x1: DIRECT_CLOCK:** Selects clk_csd1 directly as source of sensor clock
1	SAMPLE_SYNC	Enables double synchronizing of sample input from DSI (only relevant when DSI_SAMPLE_EN=1). Default Value: 1
0	DSI_SAMPLE_EN	DSI_SAMPLE_EN = 1 -> COUNTER will count the samples generated by DSI DSI_SAMPLE_EN = 0 -> COUNTER will count the samples generated by CSD modulator Set this bit at 0 (default) if DSI is not used in your design modify the CSD block Default Value: 0

9.1.3 CSD0_IDAC

IDAC Configuration

Address: 0x40280008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IDAC1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None	RW	RW	
HW Access	None			A	None	R	R	
Name	None [15:13]			POLARITY1_MIR	None	IDAC1_RANGE	IDAC1_MODE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	IDAC2 [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	None	RW	None	RW	RW	
HW Access	None	R	None	A	None	R	R	
Name	None	FEEDBACK_MODE	None	POLARITY2_MIR	None	IDAC2_RANGE	IDAC2_MODE [25:24]	

Bits	Name	Description
30	FEEDBACK_MODE	This bit controls whether, during CSD operation, the IDAC is controlled from the sampling flip-flop or directly from the comparator. Default Value: 0 **0x0: FLOP:** Use feedback from sampling flip-flop (used in most modes). **0x1: COMP:** Use feedback from comparator directly (reserved for future use)
28	POLARITY2_MIR	Mirror bit for POLARITY2 bit in CONFIG register Default Value: 0
26	IDAC2_RANGE	Current multiplier setting for IDAC2. Default Value: 0 **0x0: 4X:** Use 4X gain setting. **0x1: 8X:** Use 8X gain setting.

9.1.3 CSD0_IDAC (continued)

25 : 24	IDAC2_MODE	Controls the usage mode of IDAC2 Default Value: 0 **0x0: OFF:** IDAC2 is not used. **0x1: FIXED:** IDAC2 is active whenever CSD_CONFIG.SENSE_EN is asserted. **0x2: VARIABLE:** IDAC2 is switched on and off depending on the result of the comparator. **0x3: DSI:** IDAC2 is controlled from dsi input. IDAC_SWAP in CSD_Regs is ignored,and IDAC2 is on AMUXBUSB. When IDAC2_MODE=3, HVIDAC is selected, and when IDAC2_MODE= 1/2, LV-IDAC is selected
22 : 16	IDAC2	Current setting for IDAC2 (7 bits). Default Value: 0
12	POLARITY1_MIR	Mirror bit for POLARITY bit in CONFIG register Default Value: 0
10	IDAC1_RANGE	Current multiplier setting for IDAC1. Default Value: 0 **0x0: 4X:** Use 4X gain setting. **0x1: 8X:** Use 8X gain setting.
9 : 8	IDAC1_MODE	Controls the usage mode of IDAC1 Default Value: 0 **0x0: OFF:** IDAC1 is not used. **0x1: FIXED:** IDAC1 is active whenever CSD_CONFIG.SENSE_EN is asserted. **0x2: VARIABLE:** IDAC1 is switched on and off depending on the result of the comparator. **0x3: DSI:** IDAC1 is controlled from dsi input. IDAC_SWAP in CSD_Regs is ignored, and now IDAC1 is on AMUXBUSA. When IDAC1_MODE=3, HVIDAC is selected, and when IDAC1_MODE= 1/2, LVIDAC is selected
7 : 0	IDAC1	Current setting for IDAC1 (8 bits). Default Value: 0

9.1.4 CSD0_COUNTER

CSD Counter Register

Address: 0x4028000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	PERIOD [31:24]							

Bits	Name	Description
31 : 16	PERIOD	The remaining period (in cycles) during which COUNTER will count the samples generated by CSD modulator or DSI. Firmware will write this field to the desired period, after which it will start counting down to 0. Upon completion of the sense operation, this field will be 0. Writing a non-0 value to this register initiates a sensing operation. It is assumed that the modulation is properly configured, all pins are properly selected and configured and that sense currents are flowing before this field is written. Default Value: 0
15 : 0	COUNTER	This is 16-bit sample counter. Firmware typically writes 0 to this field whenever a new sense operation is initiated by writing a non-0 value to PERIOD. Default Value: 0

9.1.5 CSD0_STATUS

Status Register

Address: 0x40280010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				SAMPLE	COMP_OUT	CSD_SENSE	CSD_CHARGE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	SAMPLE	Only for Debug/test purpose: the output status of CSD modulator can be read by CPU Default Value: 0
2	COMP_OUT	Only for Debug/test purpose: the output status of CSD comparator can be read by CPU Default Value: 0 **0x0: C_LT_VREF:** 0: Ctank < Vref **0x1: C_GT_VREF:** 1: Ctank > Vref
1	CSD_SENSE	Only for Debug/test purpose: this internal signal (sensor clock) status can be read by CPU Default Value: 0
0	CSD_CHARGE	Only for Debug/test purpose: this internal signal status can be read by CPU. During shield operation if GPIO is used to charge/discharge the Cmod/Ctank capacitors, the charging/discharging status is available Default Value: 0

9.1.6 CSD0_INTR

CSD Interrupt Request Register

Address: 0x40280014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							CSD

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CSD	The CSD Interrupt request (IRQ) bit is set. Firmware must clear this bit as part of the interrupt handler. Default Value: 0

9.1.7 CSD0_INTR_SET

CSD Interrupt set register

Address: 0x40280018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							CSD

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CSD	Only for debug/test purpose this field can be set to '1' to set corresponding bit in interrupt request register INTR. Default Value: 0

9.1.8 CSD0_PWM

CSD PWM Register

Address: 0x4028001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW			
HW Access	None		R		R			
Name	None [7:6]		PWM_SEL [5:4]		PWM_COUNT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	PWM_SEL	The mode of the PWM modulator Default Value: 0 **0x0: OFF:** The PWM modulator is OFF and it has no effect on sensor clock generated by PRS/divide-by-2 **0x2: FIXED_HIGH:** The PWM modulator changes the low phase of sensor clock to a fixed length (used during negative charge transfer mode). **0x3: FIXED_LOW:** The PWM modulator changes the high phase of sensor clock to a fixed length (used during positive charge transfer mode).
3 : 0	PWM_COUNT	Pulse widht modulation can be used to change the length of sensor clock pulse (low time/high time) when using PRS/Divide-by-2 as source of sensor clock. The length of the sensor clock pulse low/high time is multiples of clk_csd2 cycles. Default Value: 0

9.1.9 CSD0_TRIM1

CSD Trim Register

Address: 0x4028FF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	IDAC2_SRC_TRIM [7:4]				IDAC1_SRC_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	IDAC2_SRC_TRIM	IDAC2 trim bits for gain control in current source mode Default Value: 0
3 : 0	IDAC1_SRC_TRIM	IDAC1 trim bits for gain control in current source mode Default Value: 0

9.1.10 CSD0_TRIM2

CSD Trim Register

Address: 0x4028FF04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	IDAC2_SNK_TRIM [7:4]				IDAC1_SNK_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	IDAC2_SNK_TRIM	IDAC2 trim bits for gain control in current sink mode Default Value: 0
3 : 0	IDAC1_SNK_TRIM	IDAC1 trim bits for gain control in current sink mode Default Value: 0

9.1.11 CSD1_ID

ID & Revision Number

Address: 0x40290000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	REVISION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	REVISION [31:24]							

Bits	Name	Description
31 : 16	REVISION	the version number is 0x0001 Default Value: 1
15 : 0	ID	the ID of CSD peripheral is 0xE0E1 Default Value: 57569

9.1.12 CSD1_CONFIG

Configuration and Control

Address: 0x40290004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW1S	RW	RW	RW	RW	RW
HW Access	R	R	RW1C	R	R	R	R	R
Name	PRS_12_8	PRS_SELECT	PRS_CLEAR	Reserved_1	FILTER_ENABLE	BYPASS_SEL	SAMPLE_SYNC	DSI_SAMPLE_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW		RW
HW Access	R	R	R	R	R	R		R
Name	COMP_PIN	COMP_MODE	REFBUF_EN	SENSE_EN	SENSE_COMP_BW	SHIELD_DELAY [10:9]		DSI_SENSE_EN

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	None	RW	RW	RW	RW
HW Access	R	R	R	None	R	R	RW	RW
Name	REFBUF_DRV	SENSE_INSEL	REBUF_OUTSEL	None	SENSE_COMP_EN	Reserved_2	POLARITY2	POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW			None	RW
HW Access	R	R	R	R			None	R
Name	ENABLE	Reserved_5	Reserved_4	Reserved_3 [28:26]			None	REFBUF_DRV

Bits	Name	Description
31	ENABLE	Master enable of the CSD IP. Must be set to 1 for any CSD operation to function. Default Value: 0
30	Reserved_5	Keep this bit at the default value Default Value: 0
29	Reserved_4	Keep this bit at the default value Default Value: 0
28 : 26	Reserved_3	Keep this field at the default value Default Value: 0
24 : 23	REFBUF_DRV	Current drive strength for reference buffer. Default Value: 0 **0x0: OFF:** Current drive mode OFF

9.1.12 CSD1_CONFIG (continued)

		0x1: DRV_1: Lowest current drive mode **0x2: DRV_2:** Mid current drive mode **0x3: DRV_3:** Highest current drive mode
22	SENSE_INSEL	Selects how the Cmodcapacitor is connected to CSD modulator Default Value: 0 **0x0: SENSE_CHANNEL1:** Direct connection from Cmod to CSD modulator; direct connection is called channel1 **0x1: SENSE_AMUXA:** Cmod capacitor is connected CSD modulator through AMUXBUS-A.
21	REBUF_OUTSEL	Selects which AMUXBUS the reference buffer connects to. Default Value: 1 **0x0: AMUXA:** Connect to AMUXBUS-A (not normally used). **0x1: AMUXB:** Connect to AMUXBUS-B (normally used for all CSD operations).
19	SENSE_COMP_EN	Turns on the sense comparator circuit. Must be done some time before enable SENSE_EN. 0: Sense comparator is powered off. 1: Sense comparator is powered on. Default Value: 0
18	Reserved_2	Keep this bit at the default value Default Value: 0
17	POLARITY2	For normal CSD operations this field is not used. When using the IDAC's for other-than-CSD purposes, this bit controls the IDAC2 polarity only. The IDAC register below provides the same functionality through POLARITY2_MIR bit. Default Value: 0 **0x0: VSSIO:** For non-CSD application, IDAC2 will source current. **0x1: VDDIO:** For non-CSD application, IDAC2 will sink current.
16	POLARITY	Selects the polarity of the sensing operation. When using the IDAC's for other-than-CSD purposes, this bit controls the IDAC1 polarity only. The IDAC register below provides the same functionality through POLARITY1_MIR bit. Default Value: 0 **0x0: VSSIO:** Normal: sensor switching between Vssio and Cmod. For non-CSD application, IDAC1 will source current. **0x1: VDDIO:** Inverted: sensor switch between Vddio and Cmod. For non-CSD application, IDAC1 will sink current.
15	COMP_PIN	Connects either the Cmod or Csh_tank sense return line to the reference buffer comparator. This switch must be set to the same pin that is being charged up by the reference buffer (through the AMUXBUS settings in GPIO). Default Value: 0

9.1.12 CSD1_CONFIG (continued)

		0x0: CHANNEL1: Use the sense line designated as "Channel 1"; this is normally used to conenct Cmod.
		0x1: CHANNEL2: Use the sense line designated as "Channel 2"; this is normally used to connect Csh_tank.
14	COMP_MODE	Selects between charging of the Cmod/Csh_tank capacitor using the GPIO digital output buffer or the CSD reference buffer. Note that using the GPIO requires proper configuraiton of the GPIO pin. Default Value: 0
		0x0: CHARGE_BUF: Use CSD Reference Buffer to charge capacitor. Capacitor must be connected to AMUXBUS-A/B (see REBUF_OUTSEL) and selected using COMP_PIN.
		0x1: CHARGE_IO: Use GPIO Driver to charge capacitor. Capacitor must be selected using COMP_PIN, and GPIO must be in AMUXBUS-B mode.
13	REFBUF_EN	Enables the reference buffer/comparator circuits for charging Cmod/Csh_tank using the mode selected in COMP_MODE. Default Value: 0
12	SENSE_EN	Enables the sensor and shield clocks, CSD modulator output and turns on the IDAC compensation current as selected by CSD_IDAC. Default Value: 0
11	SENSE_COMP_BW	Selects bandwidth for sensing comparator Default Value: 1
		0x0: LOW: Lower bandwidth
		0x1: HIGH: High bandwidth (default)
10 : 9	SHIELD_DELAY	Configures the delay between shield clock and sensor clock Default Value: 0
		0x0: OFF: Delay line is off; sensor clock = shield clock
		0x2: 50NS: shield clock is delayed by 50-100ns delay w.r.t sensor clock
		0x3: 10NS: shield clock is delayed by 10-20ns delay w.r.t sensor clock
8	DSI_SENSE_EN	DSI_SENSE_EN = 1-> sensor clock is driven directly by DSI DSI_SENSE_EN = 0-> sensor clock is driven by PRS/divide-by-2/DIRECT_CLOCK Set this bit at 0 (default) if DSI is not used in your design modify the CSD block Default Value: 0
7	PRS_12_8	Selects between 8-bit or 12-bit PRS sequence Default Value: 0
		0x0: 8B: 8-bit PRS sequence (G(x)=X^8+X^4+X^3+X^2+1, period= 255)
		0x1: 12B: 12-bit PRS sequence (G(x)=X^12+X^9+X^3+X^2+1, period=4095)
6	PRS_SELECT	Selects between PRS and divide-by-2 for sensor clock Default Value: 0

9.1.12 CSD1_CONFIG (continued)

		0x0: DIV2: divide-by-2 is source of sensor clock **0x1: PRS:** PRS is source of sensor clock
5	PRS_CLEAR	When set, forces the pseudo-random generator to it's initial state. Note that it may take some time for this setting to take effect depending on the clock frequency used for clk_csd1. Hardware clears this bit at the same time PRS is cleared. Default Value: 0
4	Reserved_1	Keep this bit at the default value Default Value: 0
3	FILTER_ENABLE	Enables the digital filtering on the CSD comparator Default Value: 0 **0x0: FILTER_OFF:** Digital Filter is OFF and has no effect. **0x1: FILTER_ON:** Digital Filter is ON. The digital filter disables the IDAC and sample COUNTER, regardless of CSD comparator state, for 1 clk_csd2 clock cycle after the start of each measurement and from the first comparator trip to the end of each measurement.
2	BYPASS_SEL	Selects the source of sensor clock. Default Value: 0 **0x0: PRS_OR_DIV2:** Select divide-by-2 or pseudo-random sequence as source of sensor clock(see PRS_SELECT) **0x1: DIRECT_CLOCK:** Selects clk_csd1 directly as source of sensor clock
1	SAMPLE_SYNC	Enables double synchronizing of sample input from DSI (only relevant when DSI_SAMPLE_EN=1). Default Value: 1
0	DSI_SAMPLE_EN	DSI_SAMPLE_EN = 1 -> COUNTER will count the samples generated by DSI DSI_SAMPLE_EN = 0 -> COUNTER will count the samples generated by CSD modulator Set this bit at 0 (default) if DSI is not used in your design modify the CSD block Default Value: 0

9.1.13 CSD1_IDAC

IDAC Configuration

Address: 0x40290008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IDAC1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None	RW	RW	
HW Access	None			A	None	R	R	
Name	None [15:13]			POLARITY1_MIR	None	IDAC1_RANGE	IDAC1_MODE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	IDAC2 [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	None	RW	None	RW	RW	
HW Access	None	R	None	A	None	R	R	
Name	None	FEEDBACK_MODE	None	POLARITY2_MIR	None	IDAC2_RANGE	IDAC2_MODE [25:24]	

Bits	Name	Description
30	FEEDBACK_MODE	This bit controls whether, during CSD operation, the IDAC is controlled from the sampling flip-flop or directly from the comparator. Default Value: 0 **0x0: FLOP:** Use feedback from sampling flip-flop (used in most modes). **0x1: COMP:** Use feedback from comparator directly (reserved for future use)
28	POLARITY2_MIR	Mirror bit for POLARITY2 bit in CONFIG register Default Value: 0
26	IDAC2_RANGE	Current multiplier setting for IDAC2. Default Value: 0 **0x0: 4X:** Use 4X gain setting. **0x1: 8X:** Use 8X gain setting.

9.1.13 CSD1_IDAC (continued)

25 : 24	IDAC2_MODE	Controls the usage mode of IDAC2 Default Value: 0 **0x0: OFF:** IDAC2 is not used. **0x1: FIXED:** IDAC2 is active whenever CSD_CONFIG.SENSE_EN is asserted. **0x2: VARIABLE:** IDAC2 is switched on and off depending on the result of the comparator. **0x3: DSI:** IDAC2 is controlled from dsi input. IDAC_SWAP in CSD_Regs is ignored,and IDAC2 is on AMUXBUSB. When IDAC2_MODE=3, HVIDAC is selected, and when IDAC2_MODE= 1/2, LV-IDAC is selected
22 : 16	IDAC2	Current setting for IDAC2 (7 bits). Default Value: 0
12	POLARITY1_MIR	Mirror bit for POLARITY bit in CONFIG register Default Value: 0
10	IDAC1_RANGE	Current multiplier setting for IDAC1. Default Value: 0 **0x0: 4X:** Use 4X gain setting. **0x1: 8X:** Use 8X gain setting.
9 : 8	IDAC1_MODE	Controls the usage mode of IDAC1 Default Value: 0 **0x0: OFF:** IDAC1 is not used. **0x1: FIXED:** IDAC1 is active whenever CSD_CONFIG.SENSE_EN is asserted. **0x2: VARIABLE:** IDAC1 is switched on and off depending on the result of the comparator. **0x3: DSI:** IDAC1 is controlled from dsi input. IDAC_SWAP in CSD_Regs is ignored, and now IDAC1 is on AMUXBUSA. When IDAC1_MODE=3, HVIDAC is selected, and when IDAC1_MODE= 1/2, LVIDAC is selected
7 : 0	IDAC1	Current setting for IDAC1 (8 bits). Default Value: 0

9.1.14 CSD1_COUNTER

CSD Counter Register

Address: 0x4029000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	PERIOD [31:24]							

Bits	Name	Description
31 : 16	PERIOD	The remaining period (in cycles) during which COUNTER will count the samples generated by CSD modulator or DSI. Firmware will write this field to the desired period, after which it will start counting down to 0. Upon completion of the sense operation, this field will be 0. Writing a non-0 value to this register initiates a sensing operation. It is assumed that the modulation is properly configured, all pins are properly selected and configured and that sense currents are flowing before this field is written. Default Value: 0
15 : 0	COUNTER	This is 16-bit sample counter. Firmware typically writes 0 to this field whenever a new sense operation is initiated by writing a non-0 value to PERIOD. Default Value: 0

9.1.15 CSD1_STATUS

Status Register

Address: 0x40290010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				SAMPLE	COMP_OUT	CSD_SENSE	CSD_CHARGE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	SAMPLE	Only for Debug/test purpose: the output status of CSD modulator can be read by CPU Default Value: 0
2	COMP_OUT	Only for Debug/test purpose: the output status of CSD comparator can be read by CPU Default Value: 0 **0x0: C_LT_VREF:** 0: Ctank < Vref **0x1: C_GT_VREF:** 1: Ctank > Vref
1	CSD_SENSE	Only for Debug/test purpose: this internal signal (sensor clock) status can be read by CPU Default Value: 0
0	CSD_CHARGE	Only for Debug/test purpose: this internal signal status can be read by CPU. During shield operation if GPIO is used to charge/discharge the Cmod/Ctank capacitors, the charging/discharging status is available Default Value: 0

9.1.16 CSD1_INTR

CSD Interrupt Request Register

Address: 0x40290014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							CSD

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CSD	The CSD Interrupt request (IRQ) bit is set. Firmware must clear this bit as part of the interrupt handler. Default Value: 0

9.1.17 CSD1_INTR_SET

CSD Interrupt set register

Address: 0x40290018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							CSD

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CSD	Only for debug/test purpose this field can be set to '1' to set corresponding bit in interrupt request register INTR. Default Value: 0

9.1.18 CSD1_PWM

CSD PWM Register

Address: 0x4029001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW			
HW Access	None		R		R			
Name	None [7:6]		PWM_SEL [5:4]		PWM_COUNT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	PWM_SEL	The mode of the PWM modulator Default Value: 0 **0x0: OFF:** The PWM modulator is OFF and it has no effect on sensor clock generated by PRS/divide-by-2 **0x2: FIXED_HIGH:** The PWM modulator changes the low phase of sensor clock to a fixed length (used during negative charge transfer mode). **0x3: FIXED_LOW:** The PWM modulator changes the high phase of sensor clock to a fixed length (used during positive charge transfer mode).
3 : 0	PWM_COUNT	Pulse widht modulation can be used to change the length of sensor clock pulse (low time/high time) when using PRS/Divide-by-2 as source of sensor clock. The length of the sensor clock pulse low/high time is multiples of clk_csd2 cycles. Default Value: 0

9.1.19 CSD1_TRIM1

CSD Trim Register

Address: 0x4029FF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	IDAC2_SRC_TRIM [7:4]				IDAC1_SRC_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	IDAC2_SRC_TRIM	IDAC2 trim bits for gain control in current source mode Default Value: 0
3 : 0	IDAC1_SRC_TRIM	IDAC1 trim bits for gain control in current source mode Default Value: 0

9.1.20 CSD1_TRIM2

CSD Trim Register

Address: 0x4029FF04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	IDAC2_SNK_TRIM [7:4]				IDAC1_SNK_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	IDAC2_SNK_TRIM	IDAC2 trim bits for gain control in current sink mode Default Value: 0
3 : 0	IDAC1_SNK_TRIM	IDAC1 trim bits for gain control in current sink mode Default Value: 0

10 Continuous Time Block Mini (CTBM)

This section discusses the CTBM registers. It lists all the registers in mapping tables, in address order.

10.1 Register Details

Register Name	Address
CTBM0_CTB_CTRL	0x40300000
CTBM0_OA_RES0_CTRL	0x40300004
CTBM0_OA_RES1_CTRL	0x40300008
CTBM0_COMP_STAT	0x4030000C
CTBM0_INTR	0x40300020
CTBM0_INTR_SET	0x40300024
CTBM0_INTR_MASK	0x40300028
CTBM0_INTR_MASKED	0x4030002C
CTBM0_OA0_SW	0x40300080
CTBM0_OA0_SW_CLEAR	0x40300084
CTBM0_OA1_SW	0x40300088
CTBM0_OA1_SW_CLEAR	0x4030008C
CTBM0_CTB_SW_HW_CTRL	0x403000C0
CTBM0_CTB_SW_STATUS	0x403000C4
CTBM0_OA0_OFFSET_TRIM	0x40300F00
CTBM0_OA0_SLOPE_OFFSET_TRIM	0x40300F04
CTBM0_OA0_COMP_TRIM	0x40300F08
CTBM0_OA1_OFFSET_TRIM	0x40300F0C
CTBM0_OA1_SLOPE_OFFSET_TRIM	0x40300F10
CTBM0_OA1_COMP_TRIM	0x40300F14
CTBM1_CTB_CTRL	0x40310000
CTBM1_OA_RES0_CTRL	0x40310004
CTBM1_OA_RES1_CTRL	0x40310008
CTBM1_COMP_STAT	0x4031000C
CTBM1_INTR	0x40310020
CTBM1_INTR_SET	0x40310024
CTBM1_INTR_MASK	0x40310028

Register Name	Address
CTBM1_INTR_MASKED	0x4031002C
CTBM1_OA0_SW	0x40310080
CTBM1_OA0_SW_CLEAR	0x40310084
CTBM1_OA1_SW	0x40310088
CTBM1_OA1_SW_CLEAR	0x4031008C
CTBM1_CTB_SW_HW_CTRL	0x403100C0
CTBM1_CTB_SW_STATUS	0x403100C4
CTBM1_OA0_OFFSET_TRIM	0x40310F00
CTBM1_OA0_SLOPE_OFFSET_TRIM	0x40310F04
CTBM1_OA0_COMP_TRIM	0x40310F08
CTBM1_OA1_OFFSET_TRIM	0x40310F0C
CTBM1_OA1_SLOPE_OFFSET_TRIM	0x40310F10
CTBM1_OA1_COMP_TRIM	0x40310F14

10.1.1 CTBM0_CTB_CTRL

global CTB and power control

Address: 0x40300000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLED	DEEPSLEEP_ON	None [29:24]					

Bits	Name	Description
31	ENABLED	- 0: CTB IP disabled (put analog in power down, open all switches) - 1: CTB IP enabled Default Value: 0
30	DEEPSLEEP_ON	- 0: CTB IP disabled off during DeepSleep power mode - 1: CTB IP remains enabled during DeepSleep power mode (if ENABLED=1) Default Value: 0

10.1.2 CTBM0_OA_RES0_CTRL

Opamp0 and resistor0 control

Address: 0x40300004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	
HW Access	R	R	R	R	None	R	R	
Name	OA0_DSI_LEVEL	OA0_BYPASS_DSI_SYNC	OA0_HYST_EN	OA0_COMP_EN	None	OA0_DRIVE_STR_SEL	OA0_PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				OA0_PUMP_EN	None	OA0_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	OA0_PUMP_EN	Opamp0 pump enable Default Value: 0
9 : 8	OA0_COMPINT	Opamp0 comparator edge detect Default Value: 0 **0x0: DISABLE:** Disabled, no interrupts will be detected **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
7	OA0_DSI_LEVEL	Opamp0 comparator DSI (trigger) out level : 0=pulse, 1=level Default Value: 0

10.1.2 CTBM0_OA_RES0_CTRL (continued)

6	OA0_BYPASS_DSI_SYNC	Opamp0 bypass comparator output synchronization for DSI (trigger) output: 0=synchronize (level or pulse), 1=bypass (output async) Default Value: 0
5	OA0_HYST_EN	Opamp0 hysteresis enable (10mV) Default Value: 0
4	OA0_COMP_EN	Opamp0 comparator enable Default Value: 0
2	OA0_DRIVE_STR_SEL	Opamp0 output strenght select 0=1x, 1=10x Default Value: 0
1 : 0	OA0_PWR_MODE	Opamp0 power level: 0=off Default Value: 0

10.1.3 CTBM0_OA_RES1_CTRL

Opamp1 and resistor1 control

Address: 0x40300008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	
HW Access	R	R	R	R	None	R	R	
Name	OA1_DSI_LEVEL	OA1_BYPASS_DSI_SYNC	OA1_HYST_EN	OA1_COMP_EN	None	OA1_DRIVE_STR_SEL	OA1_PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				OA1_PUMP_EN	None	OA1_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	OA1_PUMP_EN	Opamp1 pump enable Default Value: 0
9 : 8	OA1_COMPINT	Opamp0 comparator edge detect Default Value: 0 **0x0: DISABLE:** Disabled, no interrupts will be detected **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
7	OA1_DSI_LEVEL	Opamp0 comparator DSI (trigger) out level : 0=pulse, 1=level Default Value: 0

10.1.3 CTBM0_OA_RES1_CTRL (continued)

6	OA1_BYPASS_DSI_SYNC	Opamp1 bypass comparator output synchronization for DSI output: 0=synchronize, 1=bypass Default Value: 0
5	OA1_HYST_EN	Opamp1 hysteresis enable (10mV) Default Value: 0
4	OA1_COMP_EN	Opamp1 comparator enable Default Value: 0
2	OA1_DRIVE_STR_SEL	Opamp1 output strenght select 0=1x, 1=10x Default Value: 0
1 : 0	OA1_PWR_MODE	Opamp1 power level: 0=off Default Value: 0

10.1.4 CTBM0_COMP_STAT

Comparator status

Address: 0x4030000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							OA0_COMP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							W
Name	None [23:17]							OA1_COMP

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	OA1_COMP	Opamp1 current comparator status Default Value: 0
0	OA0_COMP	Opamp0 current comparator status Default Value: 0

10.1.5 CTBM0_INTR

Interrupt request register

Address: 0x40300020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						COMP1	COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1	Comparator 1 Interrupt: hardware sets this interrupt when comparator 1 triggers. Write with '1' to clear bit. Default Value: 0
0	COMP0	Comparator 0 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0

10.1.6 CTBM0_INTR_SET

Interrupt request set register

Address: 0x40300024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						COMP1_SET	COMP0_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	COMP0_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

10.1.7 CTBM0_INTR_MASK

Interrupt request mask

Address: 0x40300028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						COMP1_MASK	COMP0_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	COMP0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.8 CTBM0_INTR_MASKED

Interrupt request masked

Address: 0x4030002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						COMP1_MASKED	COMP0_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	COMP0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

10.1.9 CTBM0_OA0_SW

Opamp0 switch control

Address: 0x40300080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	None	RW1S
HW Access	None				RW1C	RW1C	None	RW1C
Name	None [7:4]				OA0P_A30	OA0P_A20	None	OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	OA0M_A81	None [13:9]					OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None		RW1S	None	
HW Access	None		RW1C	None		RW1C	None	
Name	None [23:22]		OA0O_D81	None [20:19]		OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA0O_D81	Opamp0 output switch to short 1x with 10x drive Default Value: 0
18	OA0O_D51	Opamp0 output sarbus0 (ctbbus2 in CTB) Default Value: 0
14	OA0M_A81	Opamp0 negative terminal Opamp0 bottom Default Value: 0
8	OA0M_A11	Opamp0 negative terminal P1 Default Value: 0
3	OA0P_A30	Opamp0 positive terminal ctbbus0 Default Value: 0
2	OA0P_A20	Opamp0 positive terminal P0 Default Value: 0
0	OA0P_A00	Opamp0 positive terminal amuxbusa Default Value: 0

10.1.10 CTBM0_OA0_SW_CLEAR

Opamp0 switch control clear

Address: 0x40300084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	None	RW1C
HW Access	None				A	A	None	A
Name	None [7:4]				OA0P_A30	OA0P_A20	None	OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	OA0M_A81	None [13:9]					OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None		RW1C	None	
HW Access	None		A	None		A	None	
Name	None [23:22]		OA0O_D81	None [20:19]		OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA0O_D81	see corresponding bit in OA0_SW Default Value: 0
18	OA0O_D51	see corresponding bit in OA0_SW Default Value: 0
14	OA0M_A81	see corresponding bit in OA0_SW Default Value: 0
8	OA0M_A11	see corresponding bit in OA0_SW Default Value: 0
3	OA0P_A30	see corresponding bit in OA0_SW Default Value: 0
2	OA0P_A20	see corresponding bit in OA0_SW Default Value: 0
0	OA0P_A00	see corresponding bit in OA0_SW Default Value: 0

10.1.11 CTBM0_OA1_SW

Opamp1 switch control

Address: 0x40300088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None		RW1S	RW1S
HW Access	None			RW1C	None		RW1C	RW1C
Name	None [7:5]			OA1P_A43	None [3:2]		OA1P_A13	OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	OA1M_A82	None [13:9]					OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None	RW1S	RW1S	None	
HW Access	None		RW1C	None	RW1C	RW1C	None	
Name	None [23:22]		OA1O_D82	None	OA1O_D62	OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA1O_D82	Opamp1 output switch to short 1x with 10x drive Default Value: 0
19	OA1O_D62	Opamp1 output sarbus1 (ctbbus3 in CTB) Default Value: 0
18	OA1O_D52	Opamp1 output sarbus0 (ctbbus2 in CTB) Default Value: 0
14	OA1M_A82	Opamp1 negative terminal Opamp1 bottom Default Value: 0
8	OA1M_A22	Opamp1 negative terminal P4 Default Value: 0
4	OA1P_A43	Opamp1 positive terminal ctbbus1 Default Value: 0
1	OA1P_A13	Opamp1 positive terminal P5 Default Value: 0
0	OA1P_A03	Opamp1 positive terminal amuxbusb Default Value: 0

10.1.12 CTBM0_OA1_SW_CLEAR

Opamp1 switch control clear

Address: 0x4030008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None		RW1C	RW1C
HW Access	None			A	None		A	A
Name	None [7:5]			OA1P_A43	None [3:2]		OA1P_A13	OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	OA1M_A82	None [13:9]					OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None	RW1C	RW1C	None	
HW Access	None		A	None	A	A	None	
Name	None [23:22]		OA1O_D82	None	OA1O_D62	OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA1O_D82	see corresponding bit in OA1_SW Default Value: 0
19	OA1O_D62	see corresponding bit in OA1_SW Default Value: 0
18	OA1O_D52	see corresponding bit in OA1_SW Default Value: 0
14	OA1M_A82	see corresponding bit in OA1_SW Default Value: 0
8	OA1M_A22	see corresponding bit in OA1_SW Default Value: 0
4	OA1P_A43	see corresponding bit in OA1_SW Default Value: 0
1	OA1P_A13	see corresponding bit in OA1_SW Default Value: 0
0	OA1P_A03	see corresponding bit in OA1_SW Default Value: 0

10.1.13 CTBM0_CTB_SW_HW_CTRL

CTB bus switch control status

Address: 0x403000C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [7:4]				P3_HW_CTRL	P2_HW_CTRL	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	P3_HW_CTRL	Pin P3 switches Default Value: 0
2	P2_HW_CTRL	Pin P2 switches Default Value: 0

10.1.14 CTBM0_CTB_SW_STATUS

CTB bus switch control status

Address: 0x403000C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	R	R	R	None			
HW Access	None	W	W	W	None			
Name	None	OA1O_D62_STAT	OA1O_D52_STAT	OA0O_D51_STAT	None [27:24]			

Bits	Name	Description
30	OA1O_D62_STAT	see OA1O_D62 bit in OA1_SW Default Value: 0
29	OA1O_D52_STAT	see OA1O_D52 bit in OA1_SW Default Value: 0
28	OA0O_D51_STAT	see OA0O_D51 bit in OA0_SW Default Value: 0

10.1.15 CTBM0_OA0_OFFSET_TRIM

Opamp0 trim control

Address: 0x40300F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA0_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA0_OFFSET_TRIM	Opamp0 offset trim Default Value: 0

10.1.16 CTBM0_OA0_SLOPE_OFFSET_TRIM

Opamp0 trim control

Address: 0x40300F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA0_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA0_SLOPE_OFFSET_TRIM	Opamp0 slope offset drift trim Default Value: 0

10.1.17 CTBM0_OA0_COMP_TRIM

Opamp0 trim control

Address: 0x40300F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						OA0_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	OA0_COMP_TRIM	Opamp0 Compenation Capacitor Trim Default Value: 0

10.1.18 CTBM0_OA1_OFFSET_TRIM

Opamp1 trim control

Address: 0x40300F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA1_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA1_OFFSET_TRIM	Opamp1 offset trim Default Value: 0

10.1.19 CTBM0_OA1_SLOPE_OFFSET_TRIM

Opamp1 trim control

Address: 0x40300F10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA1_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA1_SLOPE_OFFSET_TRIM	Opamp1 slope offset drift trim Default Value: 0

10.1.20 CTBM0_OA1_COMP_TRIM

Opamp1 trim control

Address: 0x40300F14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						OA1_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	OA1_COMP_TRIM	Opamp1 Compenation Capacitor Trim Default Value: 0

10.1.21 CTBM1_CTB_CTRL

global CTB and power control

Address: 0x40310000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLED	DEEPSLEEP_ON	None [29:24]					

Bits	Name	Description
31	ENABLED	- 0: CTB IP disabled (put analog in power down, open all switches) - 1: CTB IP enabled Default Value: 0
30	DEEPSLEEP_ON	- 0: CTB IP disabled off during DeepSleep power mode - 1: CTB IP remains enabled during DeepSleep power mode (if ENABLED=1) Default Value: 0

10.1.22 CTBM1_OA_RES0_CTRL

Opamp0 and resistor0 control

Address: 0x40310004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	
HW Access	R	R	R	R	None	R	R	
Name	OA0_DSI_LEVEL	OA0_BYPASS_DSI_SYNC	OA0_HYST_EN	OA0_COMP_EN	None	OA0_DRIVE_STR_SEL	OA0_PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				OA0_PUMP_EN	None	OA0_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	OA0_PUMP_EN	Opamp0 pump enable Default Value: 0
9 : 8	OA0_COMPINT	Opamp0 comparator edge detect Default Value: 0 **0x0: DISABLE:** Disabled, no interrupts will be detected **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
7	OA0_DSI_LEVEL	Opamp0 comparator DSI (trigger) out level : 0=pulse, 1=level Default Value: 0

10.1.22 CTBM1_OA_RES0_CTRL (continued)

6	OA0_BYPASS_DSI_SYNC	Opamp0 bypass comparator output synchronization for DSI (trigger) output: 0=synchronize (level or pulse), 1=bypass (output async) Default Value: 0
5	OA0_HYST_EN	Opamp0 hysteresis enable (10mV) Default Value: 0
4	OA0_COMP_EN	Opamp0 comparator enable Default Value: 0
2	OA0_DRIVE_STR_SEL	Opamp0 output strenght select 0=1x, 1=10x Default Value: 0
1 : 0	OA0_PWR_MODE	Opamp0 power level: 0=off Default Value: 0

10.1.23 CTBM1_OA_RES1_CTRL

Opamp1 and resistor1 control

Address: 0x40310008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	
HW Access	R	R	R	R	None	R	R	
Name	OA1_DSI_LEVEL	OA1_BYPASS_DSI_SYNC	OA1_HYST_EN	OA1_COMP_EN	None	OA1_DRIVE_STR_SEL	OA1_PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				OA1_PUMP_EN	None	OA1_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	OA1_PUMP_EN	Opamp1 pump enable Default Value: 0
9 : 8	OA1_COMPINT	Opamp0 comparator edge detect Default Value: 0 **0x0: DISABLE:** Disabled, no interrupts will be detected **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
7	OA1_DSI_LEVEL	Opamp0 comparator DSI (trigger) out level : 0=pulse, 1=level Default Value: 0

10.1.23 CTBM1_OA_RES1_CTRL (continued)

6	OA1_BYPASS_DSI_SYNC	Opamp1 bypass comparator output synchronization for DSI output: 0=synchronize, 1=bypass Default Value: 0
5	OA1_HYST_EN	Opamp1 hysteresis enable (10mV) Default Value: 0
4	OA1_COMP_EN	Opamp1 comparator enable Default Value: 0
2	OA1_DRIVE_STR_SEL	Opamp1 output strenght select 0=1x, 1=10x Default Value: 0
1 : 0	OA1_PWR_MODE	Opamp1 power level: 0=off Default Value: 0

10.1.24 CTBM1_COMP_STAT

Comparator status

Address: 0x4031000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							OA0_COMP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							W
Name	None [23:17]							OA1_COMP

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	OA1_COMP	Opamp1 current comparator status Default Value: 0
0	OA0_COMP	Opamp0 current comparator status Default Value: 0

10.1.25 CTBM1_INTR

Interrupt request register

Address: 0x40310020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						COMP1	COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1	Comparator 1 Interrupt: hardware sets this interrupt when comparator 1 triggers. Write with '1' to clear bit. Default Value: 0
0	COMP0	Comparator 0 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0

10.1.26 CTBM1_INTR_SET

Interrupt request set register

Address: 0x40310024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						COMP1_SET	COMP0_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	COMP0_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

10.1.27 CTBM1_INTR_MASK

Interrupt request mask

Address: 0x40310028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						COMP1_MASK	COMP0_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	COMP0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.28 CTBM1_INTR_MASKED

Interrupt request masked

Address: 0x4031002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						COMP1_MASKED	COMP0_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	COMP0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

10.1.29 CTBM1_OA0_SW

Opamp0 switch control

Address: 0x40310080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	None	RW1S
HW Access	None				RW1C	RW1C	None	RW1C
Name	None [7:4]				OA0P_A30	OA0P_A20	None	OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	OA0M_A81	None [13:9]					OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None		RW1S	None	
HW Access	None		RW1C	None		RW1C	None	
Name	None [23:22]		OA0O_D81	None [20:19]		OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA0O_D81	Opamp0 output switch to short 1x with 10x drive Default Value: 0
18	OA0O_D51	Opamp0 output sarbus0 (ctbbus2 in CTB) Default Value: 0
14	OA0M_A81	Opamp0 negative terminal Opamp0 bottom Default Value: 0
8	OA0M_A11	Opamp0 negative terminal P1 Default Value: 0
3	OA0P_A30	Opamp0 positive terminal ctbbus0 Default Value: 0
2	OA0P_A20	Opamp0 positive terminal P0 Default Value: 0
0	OA0P_A00	Opamp0 positive terminal amuxbusa Default Value: 0

10.1.30 CTBM1_OA0_SW_CLEAR

Opamp0 switch control clear

Address: 0x40310084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	None	RW1C
HW Access	None				A	A	None	A
Name	None [7:4]				OA0P_A30	OA0P_A20	None	OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	OA0M_A81	None [13:9]					OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None		RW1C	None	
HW Access	None		A	None		A	None	
Name	None [23:22]		OA0O_D81	None [20:19]		OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA0O_D81	see corresponding bit in OA0_SW Default Value: 0
18	OA0O_D51	see corresponding bit in OA0_SW Default Value: 0
14	OA0M_A81	see corresponding bit in OA0_SW Default Value: 0
8	OA0M_A11	see corresponding bit in OA0_SW Default Value: 0
3	OA0P_A30	see corresponding bit in OA0_SW Default Value: 0
2	OA0P_A20	see corresponding bit in OA0_SW Default Value: 0
0	OA0P_A00	see corresponding bit in OA0_SW Default Value: 0

10.1.31 CTBM1_OA1_SW

Opamp1 switch control

Address: 0x40310088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None		RW1S	RW1S
HW Access	None			RW1C	None		RW1C	RW1C
Name	None [7:5]			OA1P_A43	None [3:2]		OA1P_A13	OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	OA1M_A82	None [13:9]					OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None	RW1S	RW1S	None	
HW Access	None		RW1C	None	RW1C	RW1C	None	
Name	None [23:22]		OA1O_D82	None	OA1O_D62	OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA1O_D82	Opamp1 output switch to short 1x with 10x drive Default Value: 0
19	OA1O_D62	Opamp1 output sarbus1 (ctbbus3 in CTB) Default Value: 0
18	OA1O_D52	Opamp1 output sarbus0 (ctbbus2 in CTB) Default Value: 0
14	OA1M_A82	Opamp1 negative terminal Opamp1 bottom Default Value: 0
8	OA1M_A22	Opamp1 negative terminal P4 Default Value: 0
4	OA1P_A43	Opamp1 positive terminal ctbbus1 Default Value: 0
1	OA1P_A13	Opamp1 positive terminal P5 Default Value: 0
0	OA1P_A03	Opamp1 positive terminal amuxbusb Default Value: 0

10.1.32 CTBM1_OA1_SW_CLEAR

Opamp1 switch control clear

Address: 0x4031008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None		RW1C	RW1C
HW Access	None			A	None		A	A
Name	None [7:5]			OA1P_A43	None [3:2]		OA1P_A13	OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	OA1M_A82	None [13:9]					OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None	RW1C	RW1C	None	
HW Access	None		A	None	A	A	None	
Name	None [23:22]		OA1O_D82	None	OA1O_D62	OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA1O_D82	see corresponding bit in OA1_SW Default Value: 0
19	OA1O_D62	see corresponding bit in OA1_SW Default Value: 0
18	OA1O_D52	see corresponding bit in OA1_SW Default Value: 0
14	OA1M_A82	see corresponding bit in OA1_SW Default Value: 0
8	OA1M_A22	see corresponding bit in OA1_SW Default Value: 0
4	OA1P_A43	see corresponding bit in OA1_SW Default Value: 0
1	OA1P_A13	see corresponding bit in OA1_SW Default Value: 0
0	OA1P_A03	see corresponding bit in OA1_SW Default Value: 0

10.1.33 CTBM1_CTB_SW_HW_CTRL

CTB bus switch control status

Address: 0x403100C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [7:4]				P3_HW_CTRL	P2_HW_CTRL	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	P3_HW_CTRL	Pin P3 switches Default Value: 0
2	P2_HW_CTRL	Pin P2 switches Default Value: 0

10.1.34 CTBM1_CTB_SW_STATUS

CTB bus switch control status

Address: 0x403100C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	R	R	R	None			
HW Access	None	W	W	W	None			
Name	None	OA1O_D62_STAT	OA1O_D52_STAT	OA0O_D51_STAT	None [27:24]			

Bits	Name	Description
30	OA1O_D62_STAT	see OA1O_D62 bit in OA1_SW Default Value: 0
29	OA1O_D52_STAT	see OA1O_D52 bit in OA1_SW Default Value: 0
28	OA0O_D51_STAT	see OA0O_D51 bit in OA0_SW Default Value: 0

10.1.35 CTBM1_OA0_OFFSET_TRIM

Opamp0 trim control

Address: 0x40310F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA0_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA0_OFFSET_TRIM	Opamp0 offset trim Default Value: 0

10.1.36 CTBM1_OA0_SLOPE_OFFSET_TRIM

Opamp0 trim control

Address: 0x40310F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA0_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA0_SLOPE_OFFSET_TRIM	Opamp0 slope offset drift trim Default Value: 0

10.1.37 CTBM1_OA0_COMP_TRIM

Opamp0 trim control

Address: 0x40310F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						OA0_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	OA0_COMP_TRIM	Opamp0 Compenation Capacitor Trim Default Value: 0

10.1.38 CTBM1_OA1_OFFSET_TRIM

Opamp1 trim control

Address: 0x40310F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA1_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA1_OFFSET_TRIM	Opamp1 offset trim Default Value: 0

10.1.39 CTBM1_OA1_SLOPE_OFFSET_TRIM

Opamp1 trim control

Address: 0x40310F10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA1_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA1_SLOPE_OFFSET_TRIM	Opamp1 slope offset drift trim Default Value: 0

10.1.40 CTBM1_OA1_COMP_TRIM

Opamp1 trim control

Address: 0x40310F14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						OA1_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	OA1_COMP_TRIM	Opamp1 Compenation Capacitor Trim Default Value: 0

11 DMAC Registers

This section discusses the DMAC registers. It lists all the registers in mapping tables, in address order.

11.1 Register Details

Register Name	Address
DMAC_CTL	0x40101000
DMAC_STATUS	0x40101010
DMAC_STATUS_SRC_ADDR	0x40101014
DMAC_STATUS_DST_ADDR	0x40101018
DMAC_STATUS_CH_ACT	0x4010101C
DMAC_CH_CTL0	0x40101080
DMAC_CH_CTL1	0x40101084
DMAC_CH_CTL2	0x40101088
DMAC_CH_CTL3	0x4010108C
DMAC_CH_CTL4	0x40101090
DMAC_CH_CTL5	0x40101094
DMAC_CH_CTL6	0x40101098
DMAC_CH_CTL7	0x4010109C
DMAC_INTR	0x401017F0
DMAC_INTR_SET	0x401017F4
DMAC_INTR_MASK	0x401017F8
DMAC_INTR_MASKED	0x401017FC

11.1.1 DMAC_CTL

Control register

Address: 0x40101000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	0': IP is disabled. Non-retainable MMIO registers and logic functionality are reset (retainable MMIO registers are NOT reset): - INTR register is set to "0". - DW/DMA functionality is aborted. - DW/DMA controller input/pending triggers are de-activated. - DW/DMA controller output triggers are de-activated. Disabling the IP has the same effect as an active "rst_sys_act_n" reset in DeepSleep power mode. To prevent a loss of active (pending) DW/DMA triggers when disabling the IP or when transitioning from Active to DeepSleep power mode, the STATUS.ACTIVE and STATUS_CH_ACTIVE.CH fields can be used. Note that most MMIO registers are retainable, and a transition from DeepSleep to Active/Sleep power modes makes the DW/DMA controller operational, and ready to react to DW/DMA input triggers that are activated after the transition. Triggers are Active/Sleep functionality. '1': IP is enabled. Default Value: 0

11.1.2 DMAC_STATUS

Status register

Address: 0x40101010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					R		
HW Access	None					W		
Name	None [23:19]					CH_ADDR [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R		None	R		
HW Access	W	W	W		None	W		
Name	ACTIVE	PING_PONG	PRIO [29:28]		None	STATE [26:24]		

Bits	Name	Description
31	ACTIVE	Specifies if there is a currently active (pending) channel in the data transfer engine: ¡®0¡¯: no currently active channel. ¡®1¡¯: currently active channel. Default Value: 0
30	PING_PONG	Specifies whether the PING descriptor (¡®0¡¯) or PONG descriptor (¡®1¡¯) of the channel is currently in use. Default Value: Undefined
29 : 28	PRIO	Specifies the priority of the currently active channel. Default Value: Undefined
26 : 24	STATE	State of the data transfer engine. ¡°0¡: DEFAULT state. ¡°1¡: Loading descriptor (SRC, DST, CONTROL and STATUS words). ¡°2¡: Loading data element from source location. ¡°3¡: Storing data element to destination location. ¡°4¡: Storing descriptor (STATUS word). ¡°5¡: Wait for trigger de-activation. ¡°6¡: Storing descriptor with error response (STATUS word). Default Value: 0

11.1.2 DMAC_STATUS (continued)

18 : 16	CH_ADDR	Specifies the channel number of the currently active channel. E.g. if we have 32 channels, the channel number address with CH_ADDR_WIDTH is LOG2 (32) = 5, and this field is a 5-bit field. If channel 7 is active, STATUS.ACTIVE is '1' and STATUS.CH_ADDR is "7". Default Value: Undefined
15 : 0	DATA_NR	Specifies the index of the currently active data transfer. This value increases from "0" to CONTROL.DATA_NR. Default Value: Undefined

11.1.3 DMAC_STATUS_SRC_ADDR

Source address status register

Address: 0x40101014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address or current address of source location of currently active channel. The specific address information is cycle dependent. This is field is provided for debug purposes. Functionally, no assumption should be made on whether the base or current address is provided. The specifics of the currently active channel are available through STATUS. Note while reading the STATUS, STATUS_SRC and STATUS_DST registers, the transfer engine may have moved from one active channel to another. Default Value: Undefined

11.1.4 DMAC_STATUS_DST_ADDR

Destination address register

Address: 0x40101018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address or current address of destination location of currently active channel. The specific address information is cycle dependent. This is field is provided for debug purposes. Functionally, no assumption should be made on whether the base or current address is provided. The specifics of the currently active channel are available through STATUS. Note while reading the STATUS, STATUS_SRC and STATUS_DST registers, the transfer engine may have moved from one active channel to another. Default Value: Undefined

11.1.5 DMAC_STATUS_CH_ACT

Channel activation status register

Address: 0x4010101C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Channel activation status. Bit i is associated to channel i, with i = 0, ¡-, CH_NR-1. Software reads this field to get information on all actively pending channels (either in pending or in the data transfer engine). Default Value: 0

11.1.6 DMAC_CH_CTL0

Channel control register

Address: 0x40101080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	¡®0¡¯: channel disabled. The channel¡¯s trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. ¡®1¡¯: channel enabled. Software sets this field to ¡®1¡¯ to enable a specific channel. Hardware sets this field to ¡®0¡¯ on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channel¡¯s descriptor structure). Default Value: 0

11.1.6 DMAC_CH_CTL0 (continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (¡®0¡¯) and PONG (¡®1¡¯). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to ¡®1¡¯. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (¡®0¡¯) and PONG (¡®1¡¯). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with ¡°0¡ representing the highest priority and ¡°3¡ representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

11.1.7 DMAC_CH_CTL1

Channel control register

Address: 0x40101084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	¡®0¡¯: channel disabled. The channel¡¯s trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. ¡®1¡¯: channel enabled. Software sets this field to ¡®1¡¯ to enable a specific channel. Hardware sets this field to ¡®0¡¯ on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channel¡¯s descriptor structure). Default Value: 0

11.1.7 DMAC_CH_CTL1 (continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (¡®0¡¯) and PONG (¡®1¡¯). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to ¡®1¡¯. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (¡®0¡¯) and PONG (¡®1¡¯). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with ¡°0¡ representing the highest priority and ¡°3¡ representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

11.1.8 DMAC_CH_CTL2

Channel control register

Address: 0x40101088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	¡®0¡¯: channel disabled. The channel¡¯s trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. ¡®1¡¯: channel enabled. Software sets this field to ¡®1¡¯ to enable a specific channel. Hardware sets this field to ¡®0¡¯ on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channel¡¯s descriptor structure). Default Value: 0

11.1.8 DMAC_CH_CTL2 (continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (¡®0¡¯) and PONG (¡®1¡¯). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to ¡®1¡¯. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (¡®0¡¯) and PONG (¡®1¡¯). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with ¡°0¡ representing the highest priority and ¡°3¡ representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

11.1.9 DMAC_CH_CTL3

Channel control register

Address: 0x4010108C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	¡®0¡¯: channel disabled. The channel¡¯s trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. ¡®1¡¯: channel enabled. Software sets this field to ¡®1¡¯ to enable a specific channel. Hardware sets this field to ¡®0¡¯ on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channel¡¯s descriptor structure). Default Value: 0

11.1.9 DMAC_CH_CTL3 (continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (¡®0¡¯) and PONG (¡®1¡¯). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to ¡®1¡¯. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (¡®0¡¯) and PONG (¡®1¡¯). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with ¡°0¡ representing the highest priority and ¡°3¡ representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

11.1.10 DMAC_CH_CTL4

Channel control register

Address: 0x40101090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	¡®0¡¯: channel disabled. The channel¡¯s trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. ¡®1¡¯: channel enabled. Software sets this field to ¡®1¡¯ to enable a specific channel. Hardware sets this field to ¡®0¡¯ on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channel¡¯s descriptor structure). Default Value: 0

11.1.10 DMAC_CH_CTL4 (continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (¡®0¡¯) and PONG (¡®1¡¯). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to ¡®1¡¯. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (¡®0¡¯) and PONG (¡®1¡¯). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with ¡°0¡ representing the highest priority and ¡°3¡ representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

11.1.11 DMAC_CH_CTL5

Channel control register

Address: 0x40101094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	¡®0¡¯: channel disabled. The channel¡¯s trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. ¡®1¡¯: channel enabled. Software sets this field to ¡®1¡¯ to enable a specific channel. Hardware sets this field to ¡®0¡¯ on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channel¡¯s descriptor structure). Default Value: 0

11.1.11 DMAC_CH_CTL5 (continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (¡®0¡¯) and PONG (¡®1¡¯). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to ¡®1¡¯. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (¡®0¡¯) and PONG (¡®1¡¯). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with ¡°0¡ representing the highest priority and ¡°3¡ representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

11.1.12 DMAC_CH_CTL6

Channel control register

Address: 0x40101098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	¡®0¡¯: channel disabled. The channel¡¯s trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. ¡®1¡¯: channel enabled. Software sets this field to ¡®1¡¯ to enable a specific channel. Hardware sets this field to ¡®0¡¯ on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channel¡¯s descriptor structure). Default Value: 0

11.1.12 DMAC_CH_CTL6 (continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (¡®0¡¯) and PONG (¡®1¡¯). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to ¡®1¡¯. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (¡®0¡¯) and PONG (¡®1¡¯). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with ¡°0¡ representing the highest priority and ¡°3¡ representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

11.1.13 DMAC_CH_CTL7

Channel control register

Address: 0x4010109C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	¡®0¡¯: channel disabled. The channel¡¯s trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. ¡®1¡¯: channel enabled. Software sets this field to ¡®1¡¯ to enable a specific channel. Hardware sets this field to ¡®0¡¯ on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channel¡¯s descriptor structure). Default Value: 0

11.1.13 DMAC_CH_CTL7 (continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (¡®0¡¯) and PONG (¡®1¡¯). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to ¡®1¡¯. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (¡®0¡¯) and PONG (¡®1¡¯). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with ¡°0¡ representing the highest priority and ¡°3¡ representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

11.1.14 DMAC_INTR

Interrupt register

Address: 0x401017F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit. Default Value: 0

11.1.15 DMAC_INTR_SET

Interrupt set register

Address: 0x401017F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0

11.1.16 DMAC_INTR_MASK

Interrupt mask register

Address: 0x401017F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Mask for corresponding field in INTR register. Default Value: 0

11.1.17 DMAC_INTR_MASKED

Interrupt masked register

Address: 0x401017FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Logical and of corresponding request and mask fields. Default Value: 0

12 DMAC_DESCR Registers

This section discusses the DMAC_DESCR registers. It lists all the registers in mapping tables, in address order.

12.1 Register Details

Register Name	Address
DMAC_DESCR0_PING_SRC	0x40101800
DMAC_DESCR0_PING_DST	0x40101804
DMAC_DESCR0_PING_CTL	0x40101808
DMAC_DESCR0_PING_STATUS	0x4010180C
DMAC_DESCR0_PONG_SRC	0x40101810
DMAC_DESCR0_PONG_DST	0x40101814
DMAC_DESCR0_PONG_CTL	0x40101818
DMAC_DESCR0_PONG_STATUS	0x4010181C
DMAC_DESCR1_PING_SRC	0x40101820
DMAC_DESCR1_PING_DST	0x40101824
DMAC_DESCR1_PING_CTL	0x40101828
DMAC_DESCR1_PING_STATUS	0x4010182C
DMAC_DESCR1_PONG_SRC	0x40101830
DMAC_DESCR1_PONG_DST	0x40101834
DMAC_DESCR1_PONG_CTL	0x40101838
DMAC_DESCR1_PONG_STATUS	0x4010183C
DMAC_DESCR2_PING_SRC	0x40101840
DMAC_DESCR2_PING_DST	0x40101844
DMAC_DESCR2_PING_CTL	0x40101848
DMAC_DESCR2_PING_STATUS	0x4010184C
DMAC_DESCR2_PONG_SRC	0x40101850
DMAC_DESCR2_PONG_DST	0x40101854
DMAC_DESCR2_PONG_CTL	0x40101858
DMAC_DESCR2_PONG_STATUS	0x4010185C
DMAC_DESCR3_PING_SRC	0x40101860
DMAC_DESCR3_PING_DST	0x40101864
DMAC_DESCR3_PING_CTL	0x40101868

Register Name	Address
DMAC_DESCR3_PING_STATUS	0x4010186C
DMAC_DESCR3_PONG_SRC	0x40101870
DMAC_DESCR3_PONG_DST	0x40101874
DMAC_DESCR3_PONG_CTL	0x40101878
DMAC_DESCR3_PONG_STATUS	0x4010187C
DMAC_DESCR4_PING_SRC	0x40101880
DMAC_DESCR4_PING_DST	0x40101884
DMAC_DESCR4_PING_CTL	0x40101888
DMAC_DESCR4_PING_STATUS	0x4010188C
DMAC_DESCR4_PONG_SRC	0x40101890
DMAC_DESCR4_PONG_DST	0x40101894
DMAC_DESCR4_PONG_CTL	0x40101898
DMAC_DESCR4_PONG_STATUS	0x4010189C
DMAC_DESCR5_PING_SRC	0x401018A0
DMAC_DESCR5_PING_DST	0x401018A4
DMAC_DESCR5_PING_CTL	0x401018A8
DMAC_DESCR5_PING_STATUS	0x401018AC
DMAC_DESCR5_PONG_SRC	0x401018B0
DMAC_DESCR5_PONG_DST	0x401018B4
DMAC_DESCR5_PONG_CTL	0x401018B8
DMAC_DESCR5_PONG_STATUS	0x401018BC
DMAC_DESCR6_PING_SRC	0x401018C0
DMAC_DESCR6_PING_DST	0x401018C4
DMAC_DESCR6_PING_CTL	0x401018C8
DMAC_DESCR6_PING_STATUS	0x401018CC
DMAC_DESCR6_PONG_SRC	0x401018D0
DMAC_DESCR6_PONG_DST	0x401018D4
DMAC_DESCR6_PONG_CTL	0x401018D8
DMAC_DESCR6_PONG_STATUS	0x401018DC
DMAC_DESCR7_PING_SRC	0x401018E0
DMAC_DESCR7_PING_DST	0x401018E4
DMAC_DESCR7_PING_CTL	0x401018E8
DMAC_DESCR7_PING_STATUS	0x401018EC
DMAC_DESCR7_PONG_SRC	0x401018F0
DMAC_DESCR7_PONG_DST	0x401018F4
DMAC_DESCR7_PONG_CTL	0x401018F8
DMAC_DESCR7_PONG_STATUS	0x401018FC

12.1.1 DMAC_DESCR0_PING_SRC

Ping source address

Address: 0x40101800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

12.1.2 DMAC_DESCR0_PING_DST

Ping destination address

Address: 0x40101804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

12.1.3 DMAC_DESCR0_PING_CTL

Ping control word

Address: 0x40101808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

12.1.3 DMAC_DESCR0_PING_CTL (continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptor¡¯s STATUS word is ¡®1¡¯): ¡°0¡±: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). ¡°1¡±: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. ¡°2¡±: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	¡®1¡¯: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	¡®1¡¯: Transfer is preemptable. In DMA mode (OPCODE is ¡°1¡± or ¡°2¡±), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	¡®1¡¯: On completion of the current descriptor structure, the interrupt cause field of the channel is set to ¡®1¡¯ (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	¡®1¡¯: On completion of the current descriptor structure, the VALID bit of the descriptor¡¯s STATUS word is set to ¡®0¡¯. Default Value: Undefined

12.1.3 DMAC_DESCR0_PING_CTL (continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller¡¯s data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agent¡¯s trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. ¡°0¡: Do not wait for de-activation (for pulse sensitive triggers). ¡°1¡: Wait for up to 4 cycles. ¡°2¡: Wait for up to 8 cycles. ¡°3¡: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. ¡®0¡¯: No increment, typically used for receive (RX) FIFO structures. ¡®1¡¯: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: ¡®0¡¯: As specified by DATA_SIZE. ¡®1¡¯: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. ¡®0¡¯: No increment, typically used for transmit (TX) FIFO structures. ¡®1¡¯: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: ¡®0¡¯: As specified by DATA_SIZE. ¡®1¡¯: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

12.1.3 DMAC_DESCR0_PING_CTL (continued)

17 : 16	DATA_SIZE	Specifies the data element size: ¡°0¡: Byte (8 bits). ¡°1¡: Halfword (16 bits). ¡°2¡: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made ¡°0¡) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made ¡°0¡) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made ¡°0¡) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made ¡°0¡) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is ¡°0¡) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is ¡°1¡ or ¡°2¡) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

12.1.4 DMAC_DESCR0_PING_STATUS

Ping status word

Address: 0x4010180C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	¡®0¡¯: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to ¡®1¡¯). ¡®1¡¯: Valid. Hardware set this field to ¡®0¡¯ when a descriptor is done, but only if CONTROL.INV_DESCR is ¡®1¡¯. Software sets this field to ¡®1¡¯ when a descriptor is initialized. Default Value: Undefined

12.1.4 DMAC_DESCR0_PING_STATUS (continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). ¡°0¡/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to ¡®1¡¯. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to ¡°0¡/NO_ERROR during descriptor initialization. ¡°1¡/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to ¡®1¡¯ if CONTROL.SET_CAUSE is ¡®1¡¯. STATUS.VALID is set to ¡®0¡¯ if CONTROL.INV_DESCR is ¡®1¡¯. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is ¡®1¡¯. ¡°2¡/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°3¡/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°4¡/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°5¡/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°6¡/INVALID_DESCR: Invalid descriptor (STATUS.VALID is ¡®0¡¯). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be ¡®1¡¯). At descriptor initialization, SW should set this field to ¡°0¡. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

12.1.5 DMAC_DESCR0_PONG_SRC

Pong source address

Address: 0x40101810

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

12.1.6 DMAC_DESCR0_PONG_DST

Pong destination address

Address: 0x40101814

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

12.1.7 DMAC_DESCR0_PONG_CTL

Pong control word

Address: 0x40101818

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

12.1.7 DMAC_DESCR0_PONG_CTL (continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

12.1.8 DMAC_DESCR0_PONG_STATUS

Pong status word

Address: 0x4010181C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

12.1.9 DMAC_DESCR1_PING_SRC

Ping source address

Address: 0x40101820

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

12.1.10 DMAC_DESCR1_PING_DST

Ping destination address

Address: 0x40101824

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

12.1.11 DMAC_DESCR1_PING_CTL

Ping control word

Address: 0x40101828

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

12.1.11 DMAC_DESCR1_PING_CTL (continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptor¡¯s STATUS word is ¡®1¡¯): ¡°0¡±: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). ¡°1¡±: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. ¡°2¡±: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	¡®1¡¯: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	¡®1¡¯: Transfer is preemptable. In DMA mode (OPCODE is ¡°1¡± or ¡°2¡±), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	¡®1¡¯: On completion of the current descriptor structure, the interrupt cause field of the channel is set to ¡®1¡¯ (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	¡®1¡¯: On completion of the current descriptor structure, the VALID bit of the descriptor¡¯s STATUS word is set to ¡®0¡¯. Default Value: Undefined

12.1.11 DMAC_DESCR1_PING_CTL (continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller¡¯s data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agent¡¯s trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. ¡°0¡: Do not wait for de-activation (for pulse sensitive triggers). ¡°1¡: Wait for up to 4 cycles. ¡°2¡: Wait for up to 8 cycles. ¡°3¡: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. ¡®0¡¯: No increment, typically used for receive (RX) FIFO structures. ¡®1¡¯: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: ¡®0¡¯: As specified by DATA_SIZE. ¡®1¡¯: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. ¡®0¡¯: No increment, typically used for transmit (TX) FIFO structures. ¡®1¡¯: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: ¡®0¡¯: As specified by DATA_SIZE. ¡®1¡¯: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

12.1.11 DMAC_DESCR1_PING_CTL (continued)

17 : 16	DATA_SIZE	Specifies the data element size: ¡°0¡: Byte (8 bits). ¡°1¡: Halfword (16 bits). ¡°2¡: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made ¡°0¡) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made ¡°0¡) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made ¡°0¡) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made ¡°0¡) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is ¡°0¡) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is ¡°1¡ or ¡°2¡) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

12.1.12 DMAC_DESCR1_PING_STATUS

Ping status word

Address: 0x4010182C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	¡®0¡¯: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to ¡®1¡¯). ¡®1¡¯: Valid. Hardware set this field to ¡®0¡¯ when a descriptor is done, but only if CONTROL.INV_DESCR is ¡®1¡¯. Software sets this field to ¡®1¡¯ when a descriptor is initialized. Default Value: Undefined

12.1.12 DMAC_DESCR1_PING_STATUS (continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). ¡°0¡/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to ¡®1¡¯. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to ¡°0¡/NO_ERROR during descriptor initialization. ¡°1¡/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to ¡®1¡¯ if CONTROL.SET_CAUSE is ¡®1¡¯. STATUS.VALID is set to ¡®0¡¯ if CONTROL.INV_DESCR is ¡®1¡¯. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is ¡®1¡¯. ¡°2¡/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°3¡/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°4¡/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°5¡/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°6¡/INVALID_DESCR: Invalid descriptor (STATUS.VALID is ¡®0¡¯). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be ¡®1¡¯). At descriptor initialization, SW should set this field to ¡°0¡. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

12.1.13 DMAC_DESCR1_PONG_SRC

Pong source address

Address: 0x40101830

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

12.1.14 DMAC_DESCR1_PONG_DST

Pong destination address

Address: 0x40101834

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

12.1.15 DMAC_DESCR1_PONG_CTL

Pong control word

Address: 0x40101838

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

12.1.15 DMAC_DESCR1_PONG_CTL (continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

12.1.16 DMAC_DESCR1_PONG_STATUS

Pong status word

Address: 0x4010183C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

12.1.17 DMAC_DESCR2_PING_SRC

Ping source address

Address: 0x40101840

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

12.1.18 DMAC_DESCR2_PING_DST

Ping destination address

Address: 0x40101844

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

12.1.19 DMAC_DESCR2_PING_CTL

Ping control word

Address: 0x40101848

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

12.1.19 DMAC_DESCR2_PING_CTL (continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptor¡¯s STATUS word is ¡®1¡¯): ¡°0¡±: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). ¡°1¡±: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. ¡°2¡±: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	¡®1¡¯: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	¡®1¡¯: Transfer is preemptable. In DMA mode (OPCODE is ¡°1¡± or ¡°2¡±), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	¡®1¡¯: On completion of the current descriptor structure, the interrupt cause field of the channel is set to ¡®1¡¯ (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	¡®1¡¯: On completion of the current descriptor structure, the VALID bit of the descriptor¡¯s STATUS word is set to ¡®0¡¯. Default Value: Undefined

12.1.19 DMAC_DESCR2_PING_CTL (continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller¡¯s data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agent¡¯s trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. ¡°0¡: Do not wait for de-activation (for pulse sensitive triggers). ¡°1¡: Wait for up to 4 cycles. ¡°2¡: Wait for up to 8 cycles. ¡°3¡: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. ¡®0¡¯: No increment, typically used for receive (RX) FIFO structures. ¡®1¡¯: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: ¡®0¡¯: As specified by DATA_SIZE. ¡®1¡¯: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. ¡®0¡¯: No increment, typically used for transmit (TX) FIFO structures. ¡®1¡¯: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: ¡®0¡¯: As specified by DATA_SIZE. ¡®1¡¯: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

12.1.19 DMAC_DESCR2_PING_CTL (continued)

17 : 16	DATA_SIZE	Specifies the data element size: ¡°0¡: Byte (8 bits). ¡°1¡: Halfword (16 bits). ¡°2¡: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made ¡°0¡) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made ¡°0¡) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made ¡°0¡) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made ¡°0¡) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is ¡°0¡) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is ¡°1¡ or ¡°2¡) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

12.1.20 DMAC_DESCR2_PING_STATUS

Ping status word

Address: 0x4010184C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	¡®0¡¯: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to ¡®1¡¯). ¡®1¡¯: Valid. Hardware set this field to ¡®0¡¯ when a descriptor is done, but only if CONTROL.INV_DESCR is ¡®1¡¯. Software sets this field to ¡®1¡¯ when a descriptor is initialized. Default Value: Undefined

12.1.20 DMAC_DESCR2_PING_STATUS (continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). ¡°0¡/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to ¡®1¡¯. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to ¡°0¡/NO_ERROR during descriptor initialization. ¡°1¡/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to ¡®1¡¯ if CONTROL.SET_CAUSE is ¡®1¡¯. STATUS.VALID is set to ¡®0¡¯ if CONTROL.INV_DESCR is ¡®1¡¯. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is ¡®1¡¯. ¡°2¡/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°3¡/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°4¡/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°5¡/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°6¡/INVALID_DESCR: Invalid descriptor (STATUS.VALID is ¡®0¡¯). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be ¡®1¡¯). At descriptor initialization, SW should set this field to ¡°0¡. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

12.1.21 DMAC_DESCR2_PONG_SRC

Pong source address

Address: 0x40101850

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

12.1.22 DMAC_DESCR2_PONG_DST

Pong destination address

Address: 0x40101854

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

12.1.23 DMAC_DESCR2_PONG_CTL

Pong control word

Address: 0x40101858

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

12.1.23 DMAC_DESCR2_PONG_CTL (continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

12.1.24 DMAC_DESCR2_PONG_STATUS

Pong status word

Address: 0x4010185C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

12.1.25 DMAC_DESCR3_PING_SRC

Ping source address

Address: 0x40101860

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

12.1.26 DMAC_DESCR3_PING_DST

Ping destination address

Address: 0x40101864

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

12.1.27 DMAC_DESCR3_PING_CTL

Ping control word

Address: 0x40101868

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

12.1.27 DMAC_DESCR3_PING_CTL (continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptor¡¯s STATUS word is ¡®1¡¯): ¡°0¡±: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). ¡°1¡±: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. ¡°2¡±: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	¡®1¡¯: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	¡®1¡¯: Transfer is preemptable. In DMA mode (OPCODE is ¡°1¡± or ¡°2¡±), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	¡®1¡¯: On completion of the current descriptor structure, the interrupt cause field of the channel is set to ¡®1¡¯ (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	¡®1¡¯: On completion of the current descriptor structure, the VALID bit of the descriptor¡¯s STATUS word is set to ¡®0¡¯. Default Value: Undefined

12.1.27 DMAC_DESCR3_PING_CTL (continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller¡¯s data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agent¡¯s trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. ¡°0¡: Do not wait for de-activation (for pulse sensitive triggers). ¡°1¡: Wait for up to 4 cycles. ¡°2¡: Wait for up to 8 cycles. ¡°3¡: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. ¡®0¡¯: No increment, typically used for receive (RX) FIFO structures. ¡®1¡¯: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: ¡®0¡¯: As specified by DATA_SIZE. ¡®1¡¯: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. ¡®0¡¯: No increment, typically used for transmit (TX) FIFO structures. ¡®1¡¯: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: ¡®0¡¯: As specified by DATA_SIZE. ¡®1¡¯: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

12.1.27 DMAC_DESCR3_PING_CTL (continued)

17 : 16	DATA_SIZE	Specifies the data element size: ¡°0¡: Byte (8 bits). ¡°1¡: Halfword (16 bits). ¡°2¡: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made ¡°0¡) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made ¡°0¡) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made ¡°0¡) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made ¡°0¡) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is ¡°0¡) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is ¡°1¡ or ¡°2¡) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

12.1.28 DMAC_DESCR3_PING_STATUS

Ping status word

Address: 0x4010186C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	¡®0¡¯: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to ¡®1¡¯). ¡®1¡¯: Valid. Hardware set this field to ¡®0¡¯ when a descriptor is done, but only if CONTROL.INV_DESCR is ¡®1¡¯. Software sets this field to ¡®1¡¯ when a descriptor is initialized. Default Value: Undefined

12.1.28 DMAC_DESCR3_PING_STATUS (continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). ¡°0¡/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to ¡®1¡¯. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to ¡°0¡/NO_ERROR during descriptor initialization. ¡°1¡/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to ¡®1¡¯ if CONTROL.SET_CAUSE is ¡®1¡¯. STATUS.VALID is set to ¡®0¡¯ if CONTROL.INV_DESCR is ¡®1¡¯. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is ¡®1¡¯. ¡°2¡/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°3¡/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°4¡/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°5¡/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°6¡/INVALID_DESCR: Invalid descriptor (STATUS.VALID is ¡®0¡¯). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be ¡®1¡¯). At descriptor initialization, SW should set this field to ¡°0¡. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

12.1.29 DMAC_DESCR3_PONG_SRC

Pong source address

Address: 0x40101870

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

12.1.30 DMAC_DESCR3_PONG_DST

Pong destination address

Address: 0x40101874

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

12.1.31 DMAC_DESCR3_PONG_CTL

Pong control word

Address: 0x40101878

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

12.1.31 DMAC_DESCR3_PONG_CTL (continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

12.1.32 DMAC_DESCR3_PONG_STATUS

Pong status word

Address: 0x4010187C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

12.1.33 DMAC_DESCR4_PING_SRC

Ping source address

Address: 0x40101880

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

12.1.34 DMAC_DESCR4_PING_DST

Ping destination address

Address: 0x40101884

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

12.1.35 DMAC_DESCR4_PING_CTL

Ping control word

Address: 0x40101888

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

12.1.35 DMAC_DESCR4_PING_CTL (continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptor¡¯s STATUS word is ¡®1¡¯): ¡°0¡±: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). ¡°1¡±: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. ¡°2¡±: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	¡®1¡¯: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	¡®1¡¯: Transfer is preemptable. In DMA mode (OPCODE is ¡°1¡± or ¡°2¡±), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	¡®1¡¯: On completion of the current descriptor structure, the interrupt cause field of the channel is set to ¡®1¡¯ (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	¡®1¡¯: On completion of the current descriptor structure, the VALID bit of the descriptor¡¯s STATUS word is set to ¡®0¡¯. Default Value: Undefined

12.1.35 DMAC_DESCR4_PING_CTL (continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller¡¯s data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agent¡¯s trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. ¡°0¡: Do not wait for de-activation (for pulse sensitive triggers). ¡°1¡: Wait for up to 4 cycles. ¡°2¡: Wait for up to 8 cycles. ¡°3¡: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. ¡®0¡¯: No increment, typically used for receive (RX) FIFO structures. ¡®1¡¯: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: ¡®0¡¯: As specified by DATA_SIZE. ¡®1¡¯: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. ¡®0¡¯: No increment, typically used for transmit (TX) FIFO structures. ¡®1¡¯: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: ¡®0¡¯: As specified by DATA_SIZE. ¡®1¡¯: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

12.1.35 DMAC_DESCR4_PING_CTL (continued)

17 : 16	DATA_SIZE	Specifies the data element size: ¡°0¡: Byte (8 bits). ¡°1¡: Halfword (16 bits). ¡°2¡: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made ¡°0¡) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made ¡°0¡) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made ¡°0¡) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made ¡°0¡) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is ¡°0¡) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is ¡°1¡ or ¡°2¡) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

12.1.36 DMAC_DESCR4_PING_STATUS

Ping status word

Address: 0x4010188C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	¡®0¡¯: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to ¡®1¡¯). ¡®1¡¯: Valid. Hardware set this field to ¡®0¡¯ when a descriptor is done, but only if CONTROL.INV_DESCR is ¡®1¡¯. Software sets this field to ¡®1¡¯ when a descriptor is initialized. Default Value: Undefined

12.1.36 DMAC_DESCR4_PING_STATUS (continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). ¡°0¡/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to ¡®1¡¯. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to ¡°0¡/NO_ERROR during descriptor initialization. ¡°1¡/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to ¡®1¡¯ if CONTROL.SET_CAUSE is ¡®1¡¯. STATUS.VALID is set to ¡®0¡¯ if CONTROL.INV_DESCR is ¡®1¡¯. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is ¡®1¡¯. ¡°2¡/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°3¡/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°4¡/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°5¡/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°6¡/INVALID_DESCR: Invalid descriptor (STATUS.VALID is ¡®0¡¯). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be ¡®1¡¯). At descriptor initialization, SW should set this field to ¡°0¡. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

12.1.37 DMAC_DESCR4_PONG_SRC

Pong source address

Address: 0x40101890

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

12.1.38 DMAC_DESCR4_PONG_DST

Pong destination address

Address: 0x40101894

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

12.1.39 DMAC_DESCR4_PONG_CTL

Pong control word

Address: 0x40101898

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

12.1.39 DMAC_DESCR4_PONG_CTL (continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

12.1.40 DMAC_DESCR4_PONG_STATUS

Pong status word

Address: 0x4010189C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

12.1.41 DMAC_DESCR5_PING_SRC

Ping source address

Address: 0x401018A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

12.1.42 DMAC_DESCR5_PING_DST

Ping destination address

Address: 0x401018A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

12.1.43 DMAC_DESCR5_PING_CTL

Ping control word

Address: 0x401018A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

12.1.43 DMAC_DESCR5_PING_CTL (continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptor¡¯s STATUS word is ¡®1¡¯): ¡°0¡±: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). ¡°1¡±: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. ¡°2¡±: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	¡®1¡¯: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	¡®1¡¯: Transfer is preemptable. In DMA mode (OPCODE is ¡°1¡± or ¡°2¡±), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	¡®1¡¯: On completion of the current descriptor structure, the interrupt cause field of the channel is set to ¡®1¡¯ (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	¡®1¡¯: On completion of the current descriptor structure, the VALID bit of the descriptor¡¯s STATUS word is set to ¡®0¡¯. Default Value: Undefined

12.1.43 DMAC_DESCR5_PING_CTL (continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller¡¯s data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agent¡¯s trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. ¡°0¡: Do not wait for de-activation (for pulse sensitive triggers). ¡°1¡: Wait for up to 4 cycles. ¡°2¡: Wait for up to 8 cycles. ¡°3¡: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. ¡®0¡¯: No increment, typically used for receive (RX) FIFO structures. ¡®1¡¯: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: ¡®0¡¯: As specified by DATA_SIZE. ¡®1¡¯: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. ¡®0¡¯: No increment, typically used for transmit (TX) FIFO structures. ¡®1¡¯: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: ¡®0¡¯: As specified by DATA_SIZE. ¡®1¡¯: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

12.1.43 DMAC_DESCR5_PING_CTL (continued)

17 : 16	DATA_SIZE	Specifies the data element size: ¡°0¡: Byte (8 bits). ¡°1¡: Halfword (16 bits). ¡°2¡: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made ¡°0¡) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made ¡°0¡) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made ¡°0¡) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made ¡°0¡) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is ¡°0¡) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is ¡°1¡ or ¡°2¡) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

12.1.44 DMAC_DESCR5_PING_STATUS

Ping status word

Address: 0x401018AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	¡®0¡¯: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to ¡®1¡¯). ¡®1¡¯: Valid. Hardware set this field to ¡®0¡¯ when a descriptor is done, but only if CONTROL.INV_DESCR is ¡®1¡¯. Software sets this field to ¡®1¡¯ when a descriptor is initialized. Default Value: Undefined

12.1.44 DMAC_DESCR5_PING_STATUS (continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). ¡°0¡/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to ¡®1¡¯. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to ¡°0¡/NO_ERROR during descriptor initialization. ¡°1¡/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to ¡®1¡¯ if CONTROL.SET_CAUSE is ¡®1¡¯. STATUS.VALID is set to ¡®0¡¯ if CONTROL.INV_DESCR is ¡®1¡¯. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is ¡®1¡¯. ¡°2¡/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°3¡/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°4¡/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°5¡/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°6¡/INVALID_DESCR: Invalid descriptor (STATUS.VALID is ¡®0¡¯). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be ¡®1¡¯). At descriptor initialization, SW should set this field to ¡°0¡. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

12.1.45 DMAC_DESCR5_PONG_SRC

Pong source address

Address: 0x401018B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

12.1.46 DMAC_DESCR5_PONG_DST

Pong destination address

Address: 0x401018B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

12.1.47 DMAC_DESCR5_PONG_CTL

Pong control word

Address: 0x401018B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

12.1.47 DMAC_DESCR5_PONG_CTL (continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

12.1.48 DMAC_DESCR5_PONG_STATUS

Pong status word

Address: 0x401018BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

12.1.49 DMAC_DESCR6_PING_SRC

Ping source address

Address: 0x401018C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

12.1.50 DMAC_DESCR6_PING_DST

Ping destination address

Address: 0x401018C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

12.1.51 DMAC_DESCR6_PING_CTL

Ping control word

Address: 0x401018C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

12.1.51 DMAC_DESCR6_PING_CTL (continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptor¡¯s STATUS word is ¡®1¡¯): ¡°0¡±: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). ¡°1¡±: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. ¡°2¡±: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	¡®1¡¯: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	¡®1¡¯: Transfer is preemptable. In DMA mode (OPCODE is ¡°1¡± or ¡°2¡±), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	¡®1¡¯: On completion of the current descriptor structure, the interrupt cause field of the channel is set to ¡®1¡¯ (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	¡®1¡¯: On completion of the current descriptor structure, the VALID bit of the descriptor¡¯s STATUS word is set to ¡®0¡¯. Default Value: Undefined

12.1.51 DMAC_DESCR6_PING_CTL (continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller¡¯s data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agent¡¯s trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. ¡°0¡: Do not wait for de-activation (for pulse sensitive triggers). ¡°1¡: Wait for up to 4 cycles. ¡°2¡: Wait for up to 8 cycles. ¡°3¡: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. ¡®0¡¯: No increment, typically used for receive (RX) FIFO structures. ¡®1¡¯: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: ¡®0¡¯: As specified by DATA_SIZE. ¡®1¡¯: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. ¡®0¡¯: No increment, typically used for transmit (TX) FIFO structures. ¡®1¡¯: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: ¡®0¡¯: As specified by DATA_SIZE. ¡®1¡¯: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

12.1.51 DMAC_DESCR6_PING_CTL (continued)

17 : 16	DATA_SIZE	Specifies the data element size: ¡°0¡: Byte (8 bits). ¡°1¡: Halfword (16 bits). ¡°2¡: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made ¡°0¡) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made ¡°0¡) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made ¡°0¡) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made ¡°0¡) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is ¡°0¡) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is ¡°1¡ or ¡°2¡) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

12.1.52 DMAC_DESCR6_PING_STATUS

Ping status word

Address: 0x401018CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	¡®0¡¯: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to ¡®1¡¯). ¡®1¡¯: Valid. Hardware set this field to ¡®0¡¯ when a descriptor is done, but only if CONTROL.INV_DESCR is ¡®1¡¯. Software sets this field to ¡®1¡¯ when a descriptor is initialized. Default Value: Undefined

12.1.52 DMAC_DESCR6_PING_STATUS (continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). ¡°0¡/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to ¡®1¡¯. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to ¡°0¡/NO_ERROR during descriptor initialization. ¡°1¡/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to ¡®1¡¯ if CONTROL.SET_CAUSE is ¡®1¡¯. STATUS.VALID is set to ¡®0¡¯ if CONTROL.INV_DESCR is ¡®1¡¯. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is ¡®1¡¯. ¡°2¡/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°3¡/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°4¡/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°5¡/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°6¡/INVALID_DESCR: Invalid descriptor (STATUS.VALID is ¡®0¡¯). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be ¡®1¡¯). At descriptor initialization, SW should set this field to ¡°0¡. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

12.1.53 DMAC_DESCR6_PONG_SRC

Pong source address

Address: 0x401018D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

12.1.54 DMAC_DESCR6_PONG_DST

Pong destination address

Address: 0x401018D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

12.1.55 DMAC_DESCR6_PONG_CTL

Pong control word

Address: 0x401018D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

12.1.55 DMAC_DESCR6_PONG_CTL (continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

12.1.56 DMAC_DESCR6_PONG_STATUS

Pong status word

Address: 0x401018DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

12.1.57 DMAC_DESCR7_PING_SRC

Ping source address

Address: 0x401018E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

12.1.58 DMAC_DESCR7_PING_DST

Ping destination address

Address: 0x401018E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

12.1.59 DMAC_DESCR7_PING_CTL

Ping control word

Address: 0x401018E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

12.1.59 DMAC_DESCR7_PING_CTL (continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptor¡¯s STATUS word is ¡®1¡¯): ¡°0¡±: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). ¡°1¡±: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. ¡°2¡±: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	¡®1¡¯: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	¡®1¡¯: Transfer is preemptable. In DMA mode (OPCODE is ¡°1¡± or ¡°2¡±), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	¡®1¡¯: On completion of the current descriptor structure, the interrupt cause field of the channel is set to ¡®1¡¯ (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	¡®1¡¯: On completion of the current descriptor structure, the VALID bit of the descriptor¡¯s STATUS word is set to ¡®0¡¯. Default Value: Undefined

12.1.59 DMAC_DESCR7_PING_CTL (continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller¡¯s data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agent¡¯s trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. ¡°0¡: Do not wait for de-activation (for pulse sensitive triggers). ¡°1¡: Wait for up to 4 cycles. ¡°2¡: Wait for up to 8 cycles. ¡°3¡: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. ¡®0¡¯: No increment, typically used for receive (RX) FIFO structures. ¡®1¡¯: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: ¡®0¡¯: As specified by DATA_SIZE. ¡®1¡¯: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. ¡®0¡¯: No increment, typically used for transmit (TX) FIFO structures. ¡®1¡¯: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: ¡®0¡¯: As specified by DATA_SIZE. ¡®1¡¯: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

12.1.59 DMAC_DESCR7_PING_CTL (continued)

17 : 16	DATA_SIZE	Specifies the data element size: ¡°0¡: Byte (8 bits). ¡°1¡: Halfword (16 bits). ¡°2¡: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made ¡°0¡) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made ¡°0¡) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made ¡°0¡) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made ¡°0¡) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is ¡°0¡) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is ¡°1¡ or ¡°2¡) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

12.1.60 DMAC_DESCR7_PING_STATUS

Ping status word

Address: 0x401018EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	¡®0¡¯: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to ¡®1¡¯). ¡®1¡¯: Valid. Hardware set this field to ¡®0¡¯ when a descriptor is done, but only if CONTROL.INV_DESCR is ¡®1¡¯. Software sets this field to ¡®1¡¯ when a descriptor is initialized. Default Value: Undefined

12.1.60 DMAC_DESCR7_PING_STATUS (continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). ¡°0¡/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to ¡®1¡¯. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to ¡°0¡/NO_ERROR during descriptor initialization. ¡°1¡/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to ¡®1¡¯ if CONTROL.SET_CAUSE is ¡®1¡¯. STATUS.VALID is set to ¡®0¡¯ if CONTROL.INV_DESCR is ¡®1¡¯. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is ¡®1¡¯. ¡°2¡/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°3¡/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°4¡/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°5¡/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to ¡®1¡¯. STATUS.VALID is set ¡®0¡¯. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). ¡°6¡/INVALID_DESCR: Invalid descriptor (STATUS.VALID is ¡®0¡¯). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to ¡®0¡¯. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be ¡®1¡¯). At descriptor initialization, SW should set this field to ¡°0¡. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

12.1.61 DMAC_DESCR7_PONG_SRC

Pong source address

Address: 0x401018F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

12.1.62 DMAC_DESCR7_PONG_DST

Pong destination address

Address: 0x401018F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

12.1.63 DMAC_DESCR7_PONG_CTL

Pong control word

Address: 0x401018F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

12.1.63 DMAC_DESCR7_PONG_CTL (continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

12.1.64 DMAC_DESCR7_PONG_STATUS

Pong status word

Address: 0x401018FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

13 Deep Sleep Amplifier Bias (DSAB) Registers

This section discusses the DSAB registers. It lists all the registers in mapping tables, in address order.

13.1 Register Details

Register Name	Address
PASS_DSAB_DSAB_CTRL	0x403F0E00

13.1.1 PASS_DSAB_DSAB_CTRL

global DSAB control

Address: 0x403F0E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		CURRENT_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				SEL_OUT [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	- 0: DSAB IP disabled (put analog in power down, put all iref in bypass) - 1: DSAB IP enabled Default Value: 0
11 : 8	SEL_OUT	selection for ibias_out and irefout_ptat_2pt4 0: bypass respectively irefin_0tc_2pt4 and bypass irefin_ptat_2pt4 1: drive respectively replicated dsab_ibias and 0. Default Value: 0
5 : 0	CURRENT_SEL	current selection for dsab_ibias, dsab_ibias = CURRENT_SEL * 0.075 uA (+/-5%) Default Value: 0

14 Digital System Interconnect (DSI) Registers

This section discusses the DSI registers. It lists all the registers in mapping tables, in address order.

14.1 Register Details

Register Name	Address
UDB_DSI0_HC0	0x400F4000
UDB_DSI0_HC1	0x400F4001
UDB_DSI0_HC2	0x400F4002
UDB_DSI0_HC3	0x400F4003
UDB_DSI0_HC4	0x400F4004
UDB_DSI0_HC5	0x400F4005
UDB_DSI0_HC6	0x400F4006
UDB_DSI0_HC7	0x400F4007
UDB_DSI0_HC8	0x400F4008
UDB_DSI0_HC9	0x400F4009
UDB_DSI0_HC10	0x400F400A
UDB_DSI0_HC11	0x400F400B
UDB_DSI0_HC12	0x400F400C
UDB_DSI0_HC13	0x400F400D
UDB_DSI0_HC14	0x400F400E
UDB_DSI0_HC15	0x400F400F
UDB_DSI0_HC16	0x400F4010
UDB_DSI0_HC17	0x400F4011
UDB_DSI0_HC18	0x400F4012
UDB_DSI0_HC19	0x400F4013
UDB_DSI0_HC20	0x400F4014
UDB_DSI0_HC21	0x400F4015
UDB_DSI0_HC22	0x400F4016
UDB_DSI0_HC23	0x400F4017
UDB_DSI0_HC24	0x400F4018
UDB_DSI0_HC25	0x400F4019
UDB_DSI0_HC26	0x400F401A

Register Name	Address
UDB_DSI0_HC27	0x400F401B
UDB_DSI0_HC28	0x400F401C
UDB_DSI0_HC29	0x400F401D
UDB_DSI0_HC30	0x400F401E
UDB_DSI0_HC31	0x400F401F
UDB_DSI0_HC32	0x400F4020
UDB_DSI0_HC33	0x400F4021
UDB_DSI0_HC34	0x400F4022
UDB_DSI0_HC35	0x400F4023
UDB_DSI0_HC36	0x400F4024
UDB_DSI0_HC37	0x400F4025
UDB_DSI0_HC38	0x400F4026
UDB_DSI0_HC39	0x400F4027
UDB_DSI0_HC40	0x400F4028
UDB_DSI0_HC41	0x400F4029
UDB_DSI0_HC42	0x400F402A
UDB_DSI0_HC43	0x400F402B
UDB_DSI0_HC44	0x400F402C
UDB_DSI0_HC45	0x400F402D
UDB_DSI0_HC46	0x400F402E
UDB_DSI0_HC47	0x400F402F
UDB_DSI0_HC48	0x400F4030
UDB_DSI0_HC49	0x400F4031
UDB_DSI0_HC50	0x400F4032
UDB_DSI0_HC51	0x400F4033
UDB_DSI0_HC52	0x400F4034
UDB_DSI0_HC53	0x400F4035
UDB_DSI0_HC54	0x400F4036
UDB_DSI0_HC55	0x400F4037
UDB_DSI0_HC56	0x400F4038
UDB_DSI0_HC57	0x400F4039
UDB_DSI0_HC58	0x400F403A
UDB_DSI0_HC59	0x400F403B
UDB_DSI0_HC60	0x400F403C
UDB_DSI0_HC61	0x400F403D
UDB_DSI0_HC62	0x400F403E
UDB_DSI0_HC63	0x400F403F
UDB_DSI0_HC64	0x400F4040
UDB_DSI0_HC65	0x400F4041
UDB_DSI0_HC66	0x400F4042
UDB_DSI0_HC67	0x400F4043
UDB_DSI0_HC68	0x400F4044

Register Name	Address
UDB_DSI0_HC69	0x400F4045
UDB_DSI0_HC70	0x400F4046
UDB_DSI0_HC71	0x400F4047
UDB_DSI0_HC72	0x400F4048
UDB_DSI0_HC73	0x400F4049
UDB_DSI0_HC74	0x400F404A
UDB_DSI0_HC75	0x400F404B
UDB_DSI0_HC76	0x400F404C
UDB_DSI0_HC77	0x400F404D
UDB_DSI0_HC78	0x400F404E
UDB_DSI0_HC79	0x400F404F
UDB_DSI0_HC80	0x400F4050
UDB_DSI0_HC81	0x400F4051
UDB_DSI0_HC82	0x400F4052
UDB_DSI0_HC83	0x400F4053
UDB_DSI0_HC84	0x400F4054
UDB_DSI0_HC85	0x400F4055
UDB_DSI0_HC86	0x400F4056
UDB_DSI0_HC87	0x400F4057
UDB_DSI0_HC88	0x400F4058
UDB_DSI0_HC89	0x400F4059
UDB_DSI0_HC90	0x400F405A
UDB_DSI0_HC91	0x400F405B
UDB_DSI0_HC92	0x400F405C
UDB_DSI0_HC93	0x400F405D
UDB_DSI0_HC94	0x400F405E
UDB_DSI0_HC95	0x400F405F
UDB_DSI0_HC96	0x400F4060
UDB_DSI0_HC97	0x400F4061
UDB_DSI0_HC98	0x400F4062
UDB_DSI0_HC99	0x400F4063
UDB_DSI0_HC100	0x400F4064
UDB_DSI0_HC101	0x400F4065
UDB_DSI0_HC102	0x400F4066
UDB_DSI0_HC103	0x400F4067
UDB_DSI0_HC104	0x400F4068
UDB_DSI0_HC105	0x400F4069
UDB_DSI0_HC106	0x400F406A
UDB_DSI0_HC107	0x400F406B
UDB_DSI0_HC108	0x400F406C
UDB_DSI0_HC109	0x400F406D
UDB_DSI0_HC110	0x400F406E

Register Name	Address
UDB_DSI0_HC111	0x400F406F
UDB_DSI0_HC112	0x400F4070
UDB_DSI0_HC113	0x400F4071
UDB_DSI0_HC114	0x400F4072
UDB_DSI0_HC115	0x400F4073
UDB_DSI0_HC116	0x400F4074
UDB_DSI0_HC117	0x400F4075
UDB_DSI0_HC118	0x400F4076
UDB_DSI0_HC119	0x400F4077
UDB_DSI0_HC120	0x400F4078
UDB_DSI0_HC121	0x400F4079
UDB_DSI0_HC122	0x400F407A
UDB_DSI0_HC123	0x400F407B
UDB_DSI0_HC124	0x400F407C
UDB_DSI0_HC125	0x400F407D
UDB_DSI0_HC126	0x400F407E
UDB_DSI0_HC127	0x400F407F
UDB_DSI0_HV_L0	0x400F4080
UDB_DSI0_HV_L1	0x400F4081
UDB_DSI0_HV_L2	0x400F4082
UDB_DSI0_HV_L3	0x400F4083
UDB_DSI0_HV_L4	0x400F4084
UDB_DSI0_HV_L5	0x400F4085
UDB_DSI0_HV_L6	0x400F4086
UDB_DSI0_HV_L7	0x400F4087
UDB_DSI0_HV_L8	0x400F4088
UDB_DSI0_HV_L9	0x400F4089
UDB_DSI0_HV_L10	0x400F408A
UDB_DSI0_HV_L11	0x400F408B
UDB_DSI0_HV_L12	0x400F408C
UDB_DSI0_HV_L13	0x400F408D
UDB_DSI0_HV_L14	0x400F408E
UDB_DSI0_HV_L15	0x400F408F
UDB_DSI0_HS0	0x400F4090
UDB_DSI0_HS1	0x400F4091
UDB_DSI0_HS2	0x400F4092
UDB_DSI0_HS3	0x400F4093
UDB_DSI0_HS4	0x400F4094
UDB_DSI0_HS5	0x400F4095
UDB_DSI0_HS6	0x400F4096
UDB_DSI0_HS7	0x400F4097
UDB_DSI0_HS8	0x400F4098

Register Name	Address
UDB_DSI0_HS9	0x400F4099
UDB_DSI0_HS10	0x400F409A
UDB_DSI0_HS11	0x400F409B
UDB_DSI0_HS12	0x400F409C
UDB_DSI0_HS13	0x400F409D
UDB_DSI0_HS14	0x400F409E
UDB_DSI0_HS15	0x400F409F
UDB_DSI0_HS16	0x400F40A0
UDB_DSI0_HS17	0x400F40A1
UDB_DSI0_HS18	0x400F40A2
UDB_DSI0_HS19	0x400F40A3
UDB_DSI0_HS20	0x400F40A4
UDB_DSI0_HS21	0x400F40A5
UDB_DSI0_HS22	0x400F40A6
UDB_DSI0_HS23	0x400F40A7
UDB_DSI0_HV_R0	0x400F40A8
UDB_DSI0_HV_R1	0x400F40A9
UDB_DSI0_HV_R2	0x400F40AA
UDB_DSI0_HV_R3	0x400F40AB
UDB_DSI0_HV_R4	0x400F40AC
UDB_DSI0_HV_R5	0x400F40AD
UDB_DSI0_HV_R6	0x400F40AE
UDB_DSI0_HV_R7	0x400F40AF
UDB_DSI0_HV_R8	0x400F40B0
UDB_DSI0_HV_R9	0x400F40B1
UDB_DSI0_HV_R10	0x400F40B2
UDB_DSI0_HV_R11	0x400F40B3
UDB_DSI0_HV_R12	0x400F40B4
UDB_DSI0_HV_R13	0x400F40B5
UDB_DSI0_HV_R14	0x400F40B6
UDB_DSI0_HV_R15	0x400F40B7
UDB_DSI0_DSIINP0	0x400F40C0
UDB_DSI0_DSIINP1	0x400F40C2
UDB_DSI0_DSIINP2	0x400F40C4
UDB_DSI0_DSIINP3	0x400F40C6
UDB_DSI0_DSIINP4	0x400F40C8
UDB_DSI0_DSIINP5	0x400F40CA
UDB_DSI0_DSIOUTP0	0x400F40CC
UDB_DSI0_DSIOUTP1	0x400F40CE
UDB_DSI0_DSIOUTP2	0x400F40D0
UDB_DSI0_DSIOUTP3	0x400F40D2
UDB_DSI0_DSIOUTT0	0x400F40D4

Register Name	Address
UDB_DSI0_DSIOUTT1	0x400F40D6
UDB_DSI0_DSIOUTT2	0x400F40D8
UDB_DSI0_DSIOUTT3	0x400F40DA
UDB_DSI0_DSIOUTT4	0x400F40DC
UDB_DSI0_DSIOUTT5	0x400F40DE
UDB_DSI0_VS0	0x400F40E0
UDB_DSI0_VS1	0x400F40E2
UDB_DSI0_VS2	0x400F40E4
UDB_DSI0_VS3	0x400F40E6
UDB_DSI0_VS4	0x400F40E8
UDB_DSI0_VS5	0x400F40EA
UDB_DSI0_VS6	0x400F40EC
UDB_DSI0_VS7	0x400F40EE
UDB_DSI1_HC0	0x400F4100
UDB_DSI1_HC1	0x400F4101
UDB_DSI1_HC2	0x400F4102
UDB_DSI1_HC3	0x400F4103
UDB_DSI1_HC4	0x400F4104
UDB_DSI1_HC5	0x400F4105
UDB_DSI1_HC6	0x400F4106
UDB_DSI1_HC7	0x400F4107
UDB_DSI1_HC8	0x400F4108
UDB_DSI1_HC9	0x400F4109
UDB_DSI1_HC10	0x400F410A
UDB_DSI1_HC11	0x400F410B
UDB_DSI1_HC12	0x400F410C
UDB_DSI1_HC13	0x400F410D
UDB_DSI1_HC14	0x400F410E
UDB_DSI1_HC15	0x400F410F
UDB_DSI1_HC16	0x400F4110
UDB_DSI1_HC17	0x400F4111
UDB_DSI1_HC18	0x400F4112
UDB_DSI1_HC19	0x400F4113
UDB_DSI1_HC20	0x400F4114
UDB_DSI1_HC21	0x400F4115
UDB_DSI1_HC22	0x400F4116
UDB_DSI1_HC23	0x400F4117
UDB_DSI1_HC24	0x400F4118
UDB_DSI1_HC25	0x400F4119
UDB_DSI1_HC26	0x400F411A
UDB_DSI1_HC27	0x400F411B
UDB_DSI1_HC28	0x400F411C

Register Name	Address
UDB_DSI1_HC29	0x400F411D
UDB_DSI1_HC30	0x400F411E
UDB_DSI1_HC31	0x400F411F
UDB_DSI1_HC32	0x400F4120
UDB_DSI1_HC33	0x400F4121
UDB_DSI1_HC34	0x400F4122
UDB_DSI1_HC35	0x400F4123
UDB_DSI1_HC36	0x400F4124
UDB_DSI1_HC37	0x400F4125
UDB_DSI1_HC38	0x400F4126
UDB_DSI1_HC39	0x400F4127
UDB_DSI1_HC40	0x400F4128
UDB_DSI1_HC41	0x400F4129
UDB_DSI1_HC42	0x400F412A
UDB_DSI1_HC43	0x400F412B
UDB_DSI1_HC44	0x400F412C
UDB_DSI1_HC45	0x400F412D
UDB_DSI1_HC46	0x400F412E
UDB_DSI1_HC47	0x400F412F
UDB_DSI1_HC48	0x400F4130
UDB_DSI1_HC49	0x400F4131
UDB_DSI1_HC50	0x400F4132
UDB_DSI1_HC51	0x400F4133
UDB_DSI1_HC52	0x400F4134
UDB_DSI1_HC53	0x400F4135
UDB_DSI1_HC54	0x400F4136
UDB_DSI1_HC55	0x400F4137
UDB_DSI1_HC56	0x400F4138
UDB_DSI1_HC57	0x400F4139
UDB_DSI1_HC58	0x400F413A
UDB_DSI1_HC59	0x400F413B
UDB_DSI1_HC60	0x400F413C
UDB_DSI1_HC61	0x400F413D
UDB_DSI1_HC62	0x400F413E
UDB_DSI1_HC63	0x400F413F
UDB_DSI1_HC64	0x400F4140
UDB_DSI1_HC65	0x400F4141
UDB_DSI1_HC66	0x400F4142
UDB_DSI1_HC67	0x400F4143
UDB_DSI1_HC68	0x400F4144
UDB_DSI1_HC69	0x400F4145
UDB_DSI1_HC70	0x400F4146

Register Name	Address
UDB_DSI1_HC71	0x400F4147
UDB_DSI1_HC72	0x400F4148
UDB_DSI1_HC73	0x400F4149
UDB_DSI1_HC74	0x400F414A
UDB_DSI1_HC75	0x400F414B
UDB_DSI1_HC76	0x400F414C
UDB_DSI1_HC77	0x400F414D
UDB_DSI1_HC78	0x400F414E
UDB_DSI1_HC79	0x400F414F
UDB_DSI1_HC80	0x400F4150
UDB_DSI1_HC81	0x400F4151
UDB_DSI1_HC82	0x400F4152
UDB_DSI1_HC83	0x400F4153
UDB_DSI1_HC84	0x400F4154
UDB_DSI1_HC85	0x400F4155
UDB_DSI1_HC86	0x400F4156
UDB_DSI1_HC87	0x400F4157
UDB_DSI1_HC88	0x400F4158
UDB_DSI1_HC89	0x400F4159
UDB_DSI1_HC90	0x400F415A
UDB_DSI1_HC91	0x400F415B
UDB_DSI1_HC92	0x400F415C
UDB_DSI1_HC93	0x400F415D
UDB_DSI1_HC94	0x400F415E
UDB_DSI1_HC95	0x400F415F
UDB_DSI1_HC96	0x400F4160
UDB_DSI1_HC97	0x400F4161
UDB_DSI1_HC98	0x400F4162
UDB_DSI1_HC99	0x400F4163
UDB_DSI1_HC100	0x400F4164
UDB_DSI1_HC101	0x400F4165
UDB_DSI1_HC102	0x400F4166
UDB_DSI1_HC103	0x400F4167
UDB_DSI1_HC104	0x400F4168
UDB_DSI1_HC105	0x400F4169
UDB_DSI1_HC106	0x400F416A
UDB_DSI1_HC107	0x400F416B
UDB_DSI1_HC108	0x400F416C
UDB_DSI1_HC109	0x400F416D
UDB_DSI1_HC110	0x400F416E
UDB_DSI1_HC111	0x400F416F
UDB_DSI1_HC112	0x400F4170

Register Name	Address
UDB_DSI1_HC113	0x400F4171
UDB_DSI1_HC114	0x400F4172
UDB_DSI1_HC115	0x400F4173
UDB_DSI1_HC116	0x400F4174
UDB_DSI1_HC117	0x400F4175
UDB_DSI1_HC118	0x400F4176
UDB_DSI1_HC119	0x400F4177
UDB_DSI1_HC120	0x400F4178
UDB_DSI1_HC121	0x400F4179
UDB_DSI1_HC122	0x400F417A
UDB_DSI1_HC123	0x400F417B
UDB_DSI1_HC124	0x400F417C
UDB_DSI1_HC125	0x400F417D
UDB_DSI1_HC126	0x400F417E
UDB_DSI1_HC127	0x400F417F
UDB_DSI1_HV_L0	0x400F4180
UDB_DSI1_HV_L1	0x400F4181
UDB_DSI1_HV_L2	0x400F4182
UDB_DSI1_HV_L3	0x400F4183
UDB_DSI1_HV_L4	0x400F4184
UDB_DSI1_HV_L5	0x400F4185
UDB_DSI1_HV_L6	0x400F4186
UDB_DSI1_HV_L7	0x400F4187
UDB_DSI1_HV_L8	0x400F4188
UDB_DSI1_HV_L9	0x400F4189
UDB_DSI1_HV_L10	0x400F418A
UDB_DSI1_HV_L11	0x400F418B
UDB_DSI1_HV_L12	0x400F418C
UDB_DSI1_HV_L13	0x400F418D
UDB_DSI1_HV_L14	0x400F418E
UDB_DSI1_HV_L15	0x400F418F
UDB_DSI1_HS0	0x400F4190
UDB_DSI1_HS1	0x400F4191
UDB_DSI1_HS2	0x400F4192
UDB_DSI1_HS3	0x400F4193
UDB_DSI1_HS4	0x400F4194
UDB_DSI1_HS5	0x400F4195
UDB_DSI1_HS6	0x400F4196
UDB_DSI1_HS7	0x400F4197
UDB_DSI1_HS8	0x400F4198
UDB_DSI1_HS9	0x400F4199
UDB_DSI1_HS10	0x400F419A

Register Name	Address
UDB_DSI1_HS11	0x400F419B
UDB_DSI1_HS12	0x400F419C
UDB_DSI1_HS13	0x400F419D
UDB_DSI1_HS14	0x400F419E
UDB_DSI1_HS15	0x400F419F
UDB_DSI1_HS16	0x400F41A0
UDB_DSI1_HS17	0x400F41A1
UDB_DSI1_HS18	0x400F41A2
UDB_DSI1_HS19	0x400F41A3
UDB_DSI1_HS20	0x400F41A4
UDB_DSI1_HS21	0x400F41A5
UDB_DSI1_HS22	0x400F41A6
UDB_DSI1_HS23	0x400F41A7
UDB_DSI1_HV_R0	0x400F41A8
UDB_DSI1_HV_R1	0x400F41A9
UDB_DSI1_HV_R2	0x400F41AA
UDB_DSI1_HV_R3	0x400F41AB
UDB_DSI1_HV_R4	0x400F41AC
UDB_DSI1_HV_R5	0x400F41AD
UDB_DSI1_HV_R6	0x400F41AE
UDB_DSI1_HV_R7	0x400F41AF
UDB_DSI1_HV_R8	0x400F41B0
UDB_DSI1_HV_R9	0x400F41B1
UDB_DSI1_HV_R10	0x400F41B2
UDB_DSI1_HV_R11	0x400F41B3
UDB_DSI1_HV_R12	0x400F41B4
UDB_DSI1_HV_R13	0x400F41B5
UDB_DSI1_HV_R14	0x400F41B6
UDB_DSI1_HV_R15	0x400F41B7
UDB_DSI1_DSIINP0	0x400F41C0
UDB_DSI1_DSIINP1	0x400F41C2
UDB_DSI1_DSIINP2	0x400F41C4
UDB_DSI1_DSIINP3	0x400F41C6
UDB_DSI1_DSIINP4	0x400F41C8
UDB_DSI1_DSIINP5	0x400F41CA
UDB_DSI1_DSIOUTP0	0x400F41CC
UDB_DSI1_DSIOUTP1	0x400F41CE
UDB_DSI1_DSIOUTP2	0x400F41D0
UDB_DSI1_DSIOUTP3	0x400F41D2
UDB_DSI1_DSIOUTT0	0x400F41D4
UDB_DSI1_DSIOUTT1	0x400F41D6
UDB_DSI1_DSIOUTT2	0x400F41D8

Register Name	Address
UDB_DSI1_DSIOUTT3	0x400F41DA
UDB_DSI1_DSIOUTT4	0x400F41DC
UDB_DSI1_DSIOUTT5	0x400F41DE
UDB_DSI1_VS0	0x400F41E0
UDB_DSI1_VS1	0x400F41E2
UDB_DSI1_VS2	0x400F41E4
UDB_DSI1_VS3	0x400F41E6
UDB_DSI1_VS4	0x400F41E8
UDB_DSI1_VS5	0x400F41EA
UDB_DSI1_VS6	0x400F41EC
UDB_DSI1_VS7	0x400F41EE
UDB_DSI2_HC0	0x400F4200
UDB_DSI2_HC1	0x400F4201
UDB_DSI2_HC2	0x400F4202
UDB_DSI2_HC3	0x400F4203
UDB_DSI2_HC4	0x400F4204
UDB_DSI2_HC5	0x400F4205
UDB_DSI2_HC6	0x400F4206
UDB_DSI2_HC7	0x400F4207
UDB_DSI2_HC8	0x400F4208
UDB_DSI2_HC9	0x400F4209
UDB_DSI2_HC10	0x400F420A
UDB_DSI2_HC11	0x400F420B
UDB_DSI2_HC12	0x400F420C
UDB_DSI2_HC13	0x400F420D
UDB_DSI2_HC14	0x400F420E
UDB_DSI2_HC15	0x400F420F
UDB_DSI2_HC16	0x400F4210
UDB_DSI2_HC17	0x400F4211
UDB_DSI2_HC18	0x400F4212
UDB_DSI2_HC19	0x400F4213
UDB_DSI2_HC20	0x400F4214
UDB_DSI2_HC21	0x400F4215
UDB_DSI2_HC22	0x400F4216
UDB_DSI2_HC23	0x400F4217
UDB_DSI2_HC24	0x400F4218
UDB_DSI2_HC25	0x400F4219
UDB_DSI2_HC26	0x400F421A
UDB_DSI2_HC27	0x400F421B
UDB_DSI2_HC28	0x400F421C
UDB_DSI2_HC29	0x400F421D
UDB_DSI2_HC30	0x400F421E

Register Name	Address
UDB_DSI2_HC31	0x400F421F
UDB_DSI2_HC32	0x400F4220
UDB_DSI2_HC33	0x400F4221
UDB_DSI2_HC34	0x400F4222
UDB_DSI2_HC35	0x400F4223
UDB_DSI2_HC36	0x400F4224
UDB_DSI2_HC37	0x400F4225
UDB_DSI2_HC38	0x400F4226
UDB_DSI2_HC39	0x400F4227
UDB_DSI2_HC40	0x400F4228
UDB_DSI2_HC41	0x400F4229
UDB_DSI2_HC42	0x400F422A
UDB_DSI2_HC43	0x400F422B
UDB_DSI2_HC44	0x400F422C
UDB_DSI2_HC45	0x400F422D
UDB_DSI2_HC46	0x400F422E
UDB_DSI2_HC47	0x400F422F
UDB_DSI2_HC48	0x400F4230
UDB_DSI2_HC49	0x400F4231
UDB_DSI2_HC50	0x400F4232
UDB_DSI2_HC51	0x400F4233
UDB_DSI2_HC52	0x400F4234
UDB_DSI2_HC53	0x400F4235
UDB_DSI2_HC54	0x400F4236
UDB_DSI2_HC55	0x400F4237
UDB_DSI2_HC56	0x400F4238
UDB_DSI2_HC57	0x400F4239
UDB_DSI2_HC58	0x400F423A
UDB_DSI2_HC59	0x400F423B
UDB_DSI2_HC60	0x400F423C
UDB_DSI2_HC61	0x400F423D
UDB_DSI2_HC62	0x400F423E
UDB_DSI2_HC63	0x400F423F
UDB_DSI2_HC64	0x400F4240
UDB_DSI2_HC65	0x400F4241
UDB_DSI2_HC66	0x400F4242
UDB_DSI2_HC67	0x400F4243
UDB_DSI2_HC68	0x400F4244
UDB_DSI2_HC69	0x400F4245
UDB_DSI2_HC70	0x400F4246
UDB_DSI2_HC71	0x400F4247
UDB_DSI2_HC72	0x400F4248

Register Name	Address
UDB_DSI2_HC73	0x400F4249
UDB_DSI2_HC74	0x400F424A
UDB_DSI2_HC75	0x400F424B
UDB_DSI2_HC76	0x400F424C
UDB_DSI2_HC77	0x400F424D
UDB_DSI2_HC78	0x400F424E
UDB_DSI2_HC79	0x400F424F
UDB_DSI2_HC80	0x400F4250
UDB_DSI2_HC81	0x400F4251
UDB_DSI2_HC82	0x400F4252
UDB_DSI2_HC83	0x400F4253
UDB_DSI2_HC84	0x400F4254
UDB_DSI2_HC85	0x400F4255
UDB_DSI2_HC86	0x400F4256
UDB_DSI2_HC87	0x400F4257
UDB_DSI2_HC88	0x400F4258
UDB_DSI2_HC89	0x400F4259
UDB_DSI2_HC90	0x400F425A
UDB_DSI2_HC91	0x400F425B
UDB_DSI2_HC92	0x400F425C
UDB_DSI2_HC93	0x400F425D
UDB_DSI2_HC94	0x400F425E
UDB_DSI2_HC95	0x400F425F
UDB_DSI2_HC96	0x400F4260
UDB_DSI2_HC97	0x400F4261
UDB_DSI2_HC98	0x400F4262
UDB_DSI2_HC99	0x400F4263
UDB_DSI2_HC100	0x400F4264
UDB_DSI2_HC101	0x400F4265
UDB_DSI2_HC102	0x400F4266
UDB_DSI2_HC103	0x400F4267
UDB_DSI2_HC104	0x400F4268
UDB_DSI2_HC105	0x400F4269
UDB_DSI2_HC106	0x400F426A
UDB_DSI2_HC107	0x400F426B
UDB_DSI2_HC108	0x400F426C
UDB_DSI2_HC109	0x400F426D
UDB_DSI2_HC110	0x400F426E
UDB_DSI2_HC111	0x400F426F
UDB_DSI2_HC112	0x400F4270
UDB_DSI2_HC113	0x400F4271
UDB_DSI2_HC114	0x400F4272

Register Name	Address
UDB_DSI2_HC115	0x400F4273
UDB_DSI2_HC116	0x400F4274
UDB_DSI2_HC117	0x400F4275
UDB_DSI2_HC118	0x400F4276
UDB_DSI2_HC119	0x400F4277
UDB_DSI2_HC120	0x400F4278
UDB_DSI2_HC121	0x400F4279
UDB_DSI2_HC122	0x400F427A
UDB_DSI2_HC123	0x400F427B
UDB_DSI2_HC124	0x400F427C
UDB_DSI2_HC125	0x400F427D
UDB_DSI2_HC126	0x400F427E
UDB_DSI2_HC127	0x400F427F
UDB_DSI2_HV_L0	0x400F4280
UDB_DSI2_HV_L1	0x400F4281
UDB_DSI2_HV_L2	0x400F4282
UDB_DSI2_HV_L3	0x400F4283
UDB_DSI2_HV_L4	0x400F4284
UDB_DSI2_HV_L5	0x400F4285
UDB_DSI2_HV_L6	0x400F4286
UDB_DSI2_HV_L7	0x400F4287
UDB_DSI2_HV_L8	0x400F4288
UDB_DSI2_HV_L9	0x400F4289
UDB_DSI2_HV_L10	0x400F428A
UDB_DSI2_HV_L11	0x400F428B
UDB_DSI2_HV_L12	0x400F428C
UDB_DSI2_HV_L13	0x400F428D
UDB_DSI2_HV_L14	0x400F428E
UDB_DSI2_HV_L15	0x400F428F
UDB_DSI2_HS0	0x400F4290
UDB_DSI2_HS1	0x400F4291
UDB_DSI2_HS2	0x400F4292
UDB_DSI2_HS3	0x400F4293
UDB_DSI2_HS4	0x400F4294
UDB_DSI2_HS5	0x400F4295
UDB_DSI2_HS6	0x400F4296
UDB_DSI2_HS7	0x400F4297
UDB_DSI2_HS8	0x400F4298
UDB_DSI2_HS9	0x400F4299
UDB_DSI2_HS10	0x400F429A
UDB_DSI2_HS11	0x400F429B
UDB_DSI2_HS12	0x400F429C

Register Name	Address
UDB_DSI2_HS13	0x400F429D
UDB_DSI2_HS14	0x400F429E
UDB_DSI2_HS15	0x400F429F
UDB_DSI2_HS16	0x400F42A0
UDB_DSI2_HS17	0x400F42A1
UDB_DSI2_HS18	0x400F42A2
UDB_DSI2_HS19	0x400F42A3
UDB_DSI2_HS20	0x400F42A4
UDB_DSI2_HS21	0x400F42A5
UDB_DSI2_HS22	0x400F42A6
UDB_DSI2_HS23	0x400F42A7
UDB_DSI2_HV_R0	0x400F42A8
UDB_DSI2_HV_R1	0x400F42A9
UDB_DSI2_HV_R2	0x400F42AA
UDB_DSI2_HV_R3	0x400F42AB
UDB_DSI2_HV_R4	0x400F42AC
UDB_DSI2_HV_R5	0x400F42AD
UDB_DSI2_HV_R6	0x400F42AE
UDB_DSI2_HV_R7	0x400F42AF
UDB_DSI2_HV_R8	0x400F42B0
UDB_DSI2_HV_R9	0x400F42B1
UDB_DSI2_HV_R10	0x400F42B2
UDB_DSI2_HV_R11	0x400F42B3
UDB_DSI2_HV_R12	0x400F42B4
UDB_DSI2_HV_R13	0x400F42B5
UDB_DSI2_HV_R14	0x400F42B6
UDB_DSI2_HV_R15	0x400F42B7
UDB_DSI2_DSIINP0	0x400F42C0
UDB_DSI2_DSIINP1	0x400F42C2
UDB_DSI2_DSIINP2	0x400F42C4
UDB_DSI2_DSIINP3	0x400F42C6
UDB_DSI2_DSIINP4	0x400F42C8
UDB_DSI2_DSIINP5	0x400F42CA
UDB_DSI2_DSIOUTP0	0x400F42CC
UDB_DSI2_DSIOUTP1	0x400F42CE
UDB_DSI2_DSIOUTP2	0x400F42D0
UDB_DSI2_DSIOUTP3	0x400F42D2
UDB_DSI2_DSIOUTT0	0x400F42D4
UDB_DSI2_DSIOUTT1	0x400F42D6
UDB_DSI2_DSIOUTT2	0x400F42D8
UDB_DSI2_DSIOUTT3	0x400F42DA
UDB_DSI2_DSIOUTT4	0x400F42DC

Register Name	Address
UDB_DSI2_DSIOUTT5	0x400F42DE
UDB_DSI2_VS0	0x400F42E0
UDB_DSI2_VS1	0x400F42E2
UDB_DSI2_VS2	0x400F42E4
UDB_DSI2_VS3	0x400F42E6
UDB_DSI2_VS4	0x400F42E8
UDB_DSI2_VS5	0x400F42EA
UDB_DSI2_VS6	0x400F42EC
UDB_DSI2_VS7	0x400F42EE
UDB_DSI3_HC0	0x400F4300
UDB_DSI3_HC1	0x400F4301
UDB_DSI3_HC2	0x400F4302
UDB_DSI3_HC3	0x400F4303
UDB_DSI3_HC4	0x400F4304
UDB_DSI3_HC5	0x400F4305
UDB_DSI3_HC6	0x400F4306
UDB_DSI3_HC7	0x400F4307
UDB_DSI3_HC8	0x400F4308
UDB_DSI3_HC9	0x400F4309
UDB_DSI3_HC10	0x400F430A
UDB_DSI3_HC11	0x400F430B
UDB_DSI3_HC12	0x400F430C
UDB_DSI3_HC13	0x400F430D
UDB_DSI3_HC14	0x400F430E
UDB_DSI3_HC15	0x400F430F
UDB_DSI3_HC16	0x400F4310
UDB_DSI3_HC17	0x400F4311
UDB_DSI3_HC18	0x400F4312
UDB_DSI3_HC19	0x400F4313
UDB_DSI3_HC20	0x400F4314
UDB_DSI3_HC21	0x400F4315
UDB_DSI3_HC22	0x400F4316
UDB_DSI3_HC23	0x400F4317
UDB_DSI3_HC24	0x400F4318
UDB_DSI3_HC25	0x400F4319
UDB_DSI3_HC26	0x400F431A
UDB_DSI3_HC27	0x400F431B
UDB_DSI3_HC28	0x400F431C
UDB_DSI3_HC29	0x400F431D
UDB_DSI3_HC30	0x400F431E
UDB_DSI3_HC31	0x400F431F
UDB_DSI3_HC32	0x400F4320

Register Name	Address
UDB_DSI3_HC33	0x400F4321
UDB_DSI3_HC34	0x400F4322
UDB_DSI3_HC35	0x400F4323
UDB_DSI3_HC36	0x400F4324
UDB_DSI3_HC37	0x400F4325
UDB_DSI3_HC38	0x400F4326
UDB_DSI3_HC39	0x400F4327
UDB_DSI3_HC40	0x400F4328
UDB_DSI3_HC41	0x400F4329
UDB_DSI3_HC42	0x400F432A
UDB_DSI3_HC43	0x400F432B
UDB_DSI3_HC44	0x400F432C
UDB_DSI3_HC45	0x400F432D
UDB_DSI3_HC46	0x400F432E
UDB_DSI3_HC47	0x400F432F
UDB_DSI3_HC48	0x400F4330
UDB_DSI3_HC49	0x400F4331
UDB_DSI3_HC50	0x400F4332
UDB_DSI3_HC51	0x400F4333
UDB_DSI3_HC52	0x400F4334
UDB_DSI3_HC53	0x400F4335
UDB_DSI3_HC54	0x400F4336
UDB_DSI3_HC55	0x400F4337
UDB_DSI3_HC56	0x400F4338
UDB_DSI3_HC57	0x400F4339
UDB_DSI3_HC58	0x400F433A
UDB_DSI3_HC59	0x400F433B
UDB_DSI3_HC60	0x400F433C
UDB_DSI3_HC61	0x400F433D
UDB_DSI3_HC62	0x400F433E
UDB_DSI3_HC63	0x400F433F
UDB_DSI3_HC64	0x400F4340
UDB_DSI3_HC65	0x400F4341
UDB_DSI3_HC66	0x400F4342
UDB_DSI3_HC67	0x400F4343
UDB_DSI3_HC68	0x400F4344
UDB_DSI3_HC69	0x400F4345
UDB_DSI3_HC70	0x400F4346
UDB_DSI3_HC71	0x400F4347
UDB_DSI3_HC72	0x400F4348
UDB_DSI3_HC73	0x400F4349
UDB_DSI3_HC74	0x400F434A

Register Name	Address
UDB_DSI3_HC75	0x400F434B
UDB_DSI3_HC76	0x400F434C
UDB_DSI3_HC77	0x400F434D
UDB_DSI3_HC78	0x400F434E
UDB_DSI3_HC79	0x400F434F
UDB_DSI3_HC80	0x400F4350
UDB_DSI3_HC81	0x400F4351
UDB_DSI3_HC82	0x400F4352
UDB_DSI3_HC83	0x400F4353
UDB_DSI3_HC84	0x400F4354
UDB_DSI3_HC85	0x400F4355
UDB_DSI3_HC86	0x400F4356
UDB_DSI3_HC87	0x400F4357
UDB_DSI3_HC88	0x400F4358
UDB_DSI3_HC89	0x400F4359
UDB_DSI3_HC90	0x400F435A
UDB_DSI3_HC91	0x400F435B
UDB_DSI3_HC92	0x400F435C
UDB_DSI3_HC93	0x400F435D
UDB_DSI3_HC94	0x400F435E
UDB_DSI3_HC95	0x400F435F
UDB_DSI3_HC96	0x400F4360
UDB_DSI3_HC97	0x400F4361
UDB_DSI3_HC98	0x400F4362
UDB_DSI3_HC99	0x400F4363
UDB_DSI3_HC100	0x400F4364
UDB_DSI3_HC101	0x400F4365
UDB_DSI3_HC102	0x400F4366
UDB_DSI3_HC103	0x400F4367
UDB_DSI3_HC104	0x400F4368
UDB_DSI3_HC105	0x400F4369
UDB_DSI3_HC106	0x400F436A
UDB_DSI3_HC107	0x400F436B
UDB_DSI3_HC108	0x400F436C
UDB_DSI3_HC109	0x400F436D
UDB_DSI3_HC110	0x400F436E
UDB_DSI3_HC111	0x400F436F
UDB_DSI3_HC112	0x400F4370
UDB_DSI3_HC113	0x400F4371
UDB_DSI3_HC114	0x400F4372
UDB_DSI3_HC115	0x400F4373
UDB_DSI3_HC116	0x400F4374

Register Name	Address
UDB_DSI3_HC117	0x400F4375
UDB_DSI3_HC118	0x400F4376
UDB_DSI3_HC119	0x400F4377
UDB_DSI3_HC120	0x400F4378
UDB_DSI3_HC121	0x400F4379
UDB_DSI3_HC122	0x400F437A
UDB_DSI3_HC123	0x400F437B
UDB_DSI3_HC124	0x400F437C
UDB_DSI3_HC125	0x400F437D
UDB_DSI3_HC126	0x400F437E
UDB_DSI3_HC127	0x400F437F
UDB_DSI3_HV_L0	0x400F4380
UDB_DSI3_HV_L1	0x400F4381
UDB_DSI3_HV_L2	0x400F4382
UDB_DSI3_HV_L3	0x400F4383
UDB_DSI3_HV_L4	0x400F4384
UDB_DSI3_HV_L5	0x400F4385
UDB_DSI3_HV_L6	0x400F4386
UDB_DSI3_HV_L7	0x400F4387
UDB_DSI3_HV_L8	0x400F4388
UDB_DSI3_HV_L9	0x400F4389
UDB_DSI3_HV_L10	0x400F438A
UDB_DSI3_HV_L11	0x400F438B
UDB_DSI3_HV_L12	0x400F438C
UDB_DSI3_HV_L13	0x400F438D
UDB_DSI3_HV_L14	0x400F438E
UDB_DSI3_HV_L15	0x400F438F
UDB_DSI3_HS0	0x400F4390
UDB_DSI3_HS1	0x400F4391
UDB_DSI3_HS2	0x400F4392
UDB_DSI3_HS3	0x400F4393
UDB_DSI3_HS4	0x400F4394
UDB_DSI3_HS5	0x400F4395
UDB_DSI3_HS6	0x400F4396
UDB_DSI3_HS7	0x400F4397
UDB_DSI3_HS8	0x400F4398
UDB_DSI3_HS9	0x400F4399
UDB_DSI3_HS10	0x400F439A
UDB_DSI3_HS11	0x400F439B
UDB_DSI3_HS12	0x400F439C
UDB_DSI3_HS13	0x400F439D
UDB_DSI3_HS14	0x400F439E

Register Name	Address
UDB_DSI3_HS15	0x400F439F
UDB_DSI3_HS16	0x400F43A0
UDB_DSI3_HS17	0x400F43A1
UDB_DSI3_HS18	0x400F43A2
UDB_DSI3_HS19	0x400F43A3
UDB_DSI3_HS20	0x400F43A4
UDB_DSI3_HS21	0x400F43A5
UDB_DSI3_HS22	0x400F43A6
UDB_DSI3_HS23	0x400F43A7
UDB_DSI3_HV_R0	0x400F43A8
UDB_DSI3_HV_R1	0x400F43A9
UDB_DSI3_HV_R2	0x400F43AA
UDB_DSI3_HV_R3	0x400F43AB
UDB_DSI3_HV_R4	0x400F43AC
UDB_DSI3_HV_R5	0x400F43AD
UDB_DSI3_HV_R6	0x400F43AE
UDB_DSI3_HV_R7	0x400F43AF
UDB_DSI3_HV_R8	0x400F43B0
UDB_DSI3_HV_R9	0x400F43B1
UDB_DSI3_HV_R10	0x400F43B2
UDB_DSI3_HV_R11	0x400F43B3
UDB_DSI3_HV_R12	0x400F43B4
UDB_DSI3_HV_R13	0x400F43B5
UDB_DSI3_HV_R14	0x400F43B6
UDB_DSI3_HV_R15	0x400F43B7
UDB_DSI3_DSIINP0	0x400F43C0
UDB_DSI3_DSIINP1	0x400F43C2
UDB_DSI3_DSIINP2	0x400F43C4
UDB_DSI3_DSIINP3	0x400F43C6
UDB_DSI3_DSIINP4	0x400F43C8
UDB_DSI3_DSIINP5	0x400F43CA
UDB_DSI3_DSIOUTP0	0x400F43CC
UDB_DSI3_DSIOUTP1	0x400F43CE
UDB_DSI3_DSIOUTP2	0x400F43D0
UDB_DSI3_DSIOUTP3	0x400F43D2
UDB_DSI3_DSIOUTT0	0x400F43D4
UDB_DSI3_DSIOUTT1	0x400F43D6
UDB_DSI3_DSIOUTT2	0x400F43D8
UDB_DSI3_DSIOUTT3	0x400F43DA
UDB_DSI3_DSIOUTT4	0x400F43DC
UDB_DSI3_DSIOUTT5	0x400F43DE
UDB_DSI3_VS0	0x400F43E0

Register Name	Address
UDB_DSI3_VS1	0x400F43E2
UDB_DSI3_VS2	0x400F43E4
UDB_DSI3_VS3	0x400F43E6
UDB_DSI3_VS4	0x400F43E8
UDB_DSI3_VS5	0x400F43EA
UDB_DSI3_VS6	0x400F43EC
UDB_DSI3_VS7	0x400F43EE

14.1.1 UDB_DSI0_HC0

DSI HC Tile Configuration

Address: 0x400F4000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.2 UDB_DSI0_HC1

DSI HC Tile Configuration

Address: 0x400F4001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.3 UDB_DSI0_HC2

DSI HC Tile Configuration

Address: 0x400F4002

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.4 UDB_DSI0_HC3

DSI HC Tile Configuration

Address: 0x400F4003

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.5 UDB_DSI0_HC4

DSI HC Tile Configuration

Address: 0x400F4004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.6 UDB_DSI0_HC5

DSI HC Tile Configuration

Address: 0x400F4005

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.7 UDB_DSI0_HC6

DSI HC Tile Configuration

Address: 0x400F4006

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.8 UDB_DSI0_HC7

DSI HC Tile Configuration

Address: 0x400F4007

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.9 UDB_DSI0_HC8

DSI HC Tile Configuration

Address: 0x400F4008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.10 UDB_DSI0_HC9

DSI HC Tile Configuration

Address: 0x400F4009

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.11 UDB_DSI0_HC10

DSI HC Tile Configuration

Address: 0x400F400A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.12 UDB_DSI0_HC11

DSI HC Tile Configuration

Address: 0x400F400B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.13 UDB_DSI0_HC12

DSI HC Tile Configuration

Address: 0x400F400C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.14 UDB_DSI0_HC13

DSI HC Tile Configuration

Address: 0x400F400D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.15 UDB_DSI0_HC14

DSI HC Tile Configuration

Address: 0x400F400E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.16 UDB_DSI0_HC15

DSI HC Tile Configuration

Address: 0x400F400F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.17 UDB_DSI0_HC16

DSI HC Tile Configuration

Address: 0x400F4010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.18 UDB_DSI0_HC17

DSI HC Tile Configuration

Address: 0x400F4011

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.19 UDB_DSI0_HC18

DSI HC Tile Configuration

Address: 0x400F4012

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.20 UDB_DSI0_HC19

DSI HC Tile Configuration

Address: 0x400F4013

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.21 UDB_DSI0_HC20

DSI HC Tile Configuration

Address: 0x400F4014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.22 UDB_DSI0_HC21

DSI HC Tile Configuration

Address: 0x400F4015

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.23 UDB_DSI0_HC22

DSI HC Tile Configuration

Address: 0x400F4016

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.24 UDB_DSI0_HC23

DSI HC Tile Configuration

Address: 0x400F4017

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.25 UDB_DSI0_HC24

DSI HC Tile Configuration

Address: 0x400F4018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.26 UDB_DSI0_HC25

DSI HC Tile Configuration

Address: 0x400F4019

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.27 UDB_DSI0_HC26

DSI HC Tile Configuration

Address: 0x400F401A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.28 UDB_DSI0_HC27

DSI HC Tile Configuration

Address: 0x400F401B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.29 UDB_DSI0_HC28

DSI HC Tile Configuration

Address: 0x400F401C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.30 UDB_DSI0_HC29

DSI HC Tile Configuration

Address: 0x400F401D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.31 UDB_DSI0_HC30

DSI HC Tile Configuration

Address: 0x400F401E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.32 UDB_DSI0_HC31

DSI HC Tile Configuration

Address: 0x400F401F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.33 UDB_DSI0_HC32

DSI HC Tile Configuration

Address: 0x400F4020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.34 UDB_DSI0_HC33

DSI HC Tile Configuration

Address: 0x400F4021

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.35 UDB_DSI0_HC34

DSI HC Tile Configuration

Address: 0x400F4022

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.36 UDB_DSI0_HC35

DSI HC Tile Configuration

Address: 0x400F4023

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.37 UDB_DSI0_HC36

DSI HC Tile Configuration

Address: 0x400F4024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.38 UDB_DSI0_HC37

DSI HC Tile Configuration

Address: 0x400F4025

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.39 UDB_DSI0_HC38

DSI HC Tile Configuration

Address: 0x400F4026

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.40 UDB_DSI0_HC39

DSI HC Tile Configuration

Address: 0x400F4027

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.41 UDB_DSI0_HC40

DSI HC Tile Configuration

Address: 0x400F4028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.42 UDB_DSI0_HC41

DSI HC Tile Configuration

Address: 0x400F4029

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.43 UDB_DSI0_HC42

DSI HC Tile Configuration

Address: 0x400F402A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.44 UDB_DSI0_HC43

DSI HC Tile Configuration

Address: 0x400F402B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.45 UDB_DSI0_HC44

DSI HC Tile Configuration

Address: 0x400F402C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.46 UDB_DSI0_HC45

DSI HC Tile Configuration

Address: 0x400F402D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.47 UDB_DSI0_HC46

DSI HC Tile Configuration

Address: 0x400F402E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.48 UDB_DSI0_HC47

DSI HC Tile Configuration

Address: 0x400F402F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.49 UDB_DSI0_HC48

DSI HC Tile Configuration

Address: 0x400F4030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.50 UDB_DSI0_HC49

DSI HC Tile Configuration

Address: 0x400F4031

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.51 UDB_DSI0_HC50

DSI HC Tile Configuration

Address: 0x400F4032

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.52 UDB_DSI0_HC51

DSI HC Tile Configuration

Address: 0x400F4033

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.53 UDB_DSI0_HC52

DSI HC Tile Configuration

Address: 0x400F4034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.54 UDB_DSI0_HC53

DSI HC Tile Configuration

Address: 0x400F4035

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.55 UDB_DSI0_HC54

DSI HC Tile Configuration

Address: 0x400F4036

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.56 UDB_DSI0_HC55

DSI HC Tile Configuration

Address: 0x400F4037

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.57 UDB_DSI0_HC56

DSI HC Tile Configuration

Address: 0x400F4038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.58 UDB_DSI0_HC57

DSI HC Tile Configuration

Address: 0x400F4039

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.59 UDB_DSI0_HC58

DSI HC Tile Configuration

Address: 0x400F403A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.60 UDB_DSI0_HC59

DSI HC Tile Configuration

Address: 0x400F403B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.61 UDB_DSI0_HC60

DSI HC Tile Configuration

Address: 0x400F403C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.62 UDB_DSI0_HC61

DSI HC Tile Configuration

Address: 0x400F403D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.63 UDB_DSI0_HC62

DSI HC Tile Configuration

Address: 0x400F403E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.64 UDB_DSI0_HC63

DSI HC Tile Configuration

Address: 0x400F403F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.65 UDB_DSI0_HC64

DSI HC Tile Configuration

Address: 0x400F4040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.66 UDB_DSI0_HC65

DSI HC Tile Configuration

Address: 0x400F4041

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.67 UDB_DSI0_HC66

DSI HC Tile Configuration

Address: 0x400F4042

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.68 UDB_DSI0_HC67

DSI HC Tile Configuration

Address: 0x400F4043

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.69 UDB_DSI0_HC68

DSI HC Tile Configuration

Address: 0x400F4044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.70 UDB_DSI0_HC69

DSI HC Tile Configuration

Address: 0x400F4045

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.71 UDB_DSI0_HC70

DSI HC Tile Configuration

Address: 0x400F4046

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.72 UDB_DSI0_HC71

DSI HC Tile Configuration

Address: 0x400F4047

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.73 UDB_DSI0_HC72

DSI HC Tile Configuration

Address: 0x400F4048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.74 UDB_DSI0_HC73

DSI HC Tile Configuration

Address: 0x400F4049

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.75 UDB_DSI0_HC74

DSI HC Tile Configuration

Address: 0x400F404A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.76 UDB_DSI0_HC75

DSI HC Tile Configuration

Address: 0x400F404B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.77 UDB_DSI0_HC76

DSI HC Tile Configuration

Address: 0x400F404C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.78 UDB_DSI0_HC77

DSI HC Tile Configuration

Address: 0x400F404D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.79 UDB_DSI0_HC78

DSI HC Tile Configuration

Address: 0x400F404E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.80 UDB_DSI0_HC79

DSI HC Tile Configuration

Address: 0x400F404F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.81 UDB_DSI0_HC80

DSI HC Tile Configuration

Address: 0x400F4050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.82 UDB_DSI0_HC81

DSI HC Tile Configuration

Address: 0x400F4051

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.83 UDB_DSI0_HC82

DSI HC Tile Configuration

Address: 0x400F4052

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.84 UDB_DSI0_HC83

DSI HC Tile Configuration

Address: 0x400F4053

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.85 UDB_DSI0_HC84

DSI HC Tile Configuration

Address: 0x400F4054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.86 UDB_DSI0_HC85

DSI HC Tile Configuration

Address: 0x400F4055

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.87 UDB_DSI0_HC86

DSI HC Tile Configuration

Address: 0x400F4056

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.88 UDB_DSI0_HC87

DSI HC Tile Configuration

Address: 0x400F4057

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.89 UDB_DSI0_HC88

DSI HC Tile Configuration

Address: 0x400F4058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.90 UDB_DSI0_HC89

DSI HC Tile Configuration

Address: 0x400F4059

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.91 UDB_DSI0_HC90

DSI HC Tile Configuration

Address: 0x400F405A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.92 UDB_DSI0_HC91

DSI HC Tile Configuration

Address: 0x400F405B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.93 UDB_DSI0_HC92

DSI HC Tile Configuration

Address: 0x400F405C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.94 UDB_DSI0_HC93

DSI HC Tile Configuration

Address: 0x400F405D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.95 UDB_DSI0_HC94

DSI HC Tile Configuration

Address: 0x400F405E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.96 UDB_DSI0_HC95

DSI HC Tile Configuration

Address: 0x400F405F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.97 UDB_DSI0_HC96

DSI HC Tile Configuration

Address: 0x400F4060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.98 UDB_DSI0_HC97

DSI HC Tile Configuration

Address: 0x400F4061

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.99 UDB_DSI0_HC98

DSI HC Tile Configuration

Address: 0x400F4062

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.100 UDB_DSI0_HC99

DSI HC Tile Configuration

Address: 0x400F4063

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.101 UDB_DSI0_HC100

DSI HC Tile Configuration

Address: 0x400F4064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.102 UDB_DSI0_HC101

DSI HC Tile Configuration

Address: 0x400F4065

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.103 UDB_DSI0_HC102

DSI HC Tile Configuration

Address: 0x400F4066

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.104 UDB_DSI0_HC103

DSI HC Tile Configuration

Address: 0x400F4067

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.105 UDB_DSI0_HC104

DSI HC Tile Configuration

Address: 0x400F4068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.106 UDB_DSI0_HC105

DSI HC Tile Configuration

Address: 0x400F4069

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.107 UDB_DSI0_HC106

DSI HC Tile Configuration

Address: 0x400F406A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.108 UDB_DSI0_HC107

DSI HC Tile Configuration

Address: 0x400F406B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.109 UDB_DSI0_HC108

DSI HC Tile Configuration

Address: 0x400F406C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.110 UDB_DSI0_HC109

DSI HC Tile Configuration

Address: 0x400F406D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.111 UDB_DSI0_HC110

DSI HC Tile Configuration

Address: 0x400F406E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.112 UDB_DSI0_HC111

DSI HC Tile Configuration

Address: 0x400F406F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.113 UDB_DSI0_HC112

DSI HC Tile Configuration

Address: 0x400F4070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.114 UDB_DSI0_HC113

DSI HC Tile Configuration

Address: 0x400F4071

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.115 UDB_DSI0_HC114

DSI HC Tile Configuration

Address: 0x400F4072

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.116 UDB_DSI0_HC115

DSI HC Tile Configuration

Address: 0x400F4073

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.117 UDB_DSI0_HC116

DSI HC Tile Configuration

Address: 0x400F4074

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.118 UDB_DSI0_HC117

DSI HC Tile Configuration

Address: 0x400F4075

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.119 UDB_DSI0_HC118

DSI HC Tile Configuration

Address: 0x400F4076

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.120 UDB_DSI0_HC119

DSI HC Tile Configuration

Address: 0x400F4077

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.121 UDB_DSI0_HC120

DSI HC Tile Configuration

Address: 0x400F4078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.122 UDB_DSI0_HC121

DSI HC Tile Configuration

Address: 0x400F4079

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.123 UDB_DSI0_HC122

DSI HC Tile Configuration

Address: 0x400F407A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.124 UDB_DSI0_HC123

DSI HC Tile Configuration

Address: 0x400F407B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.125 UDB_DSI0_HC124

DSI HC Tile Configuration

Address: 0x400F407C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.126 UDB_DSI0_HC125

DSI HC Tile Configuration

Address: 0x400F407D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.127 UDB_DSI0_HC126

DSI HC Tile Configuration

Address: 0x400F407E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.128 UDB_DSI0_HC127

DSI HC Tile Configuration

Address: 0x400F407F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.129 UDB_DSI0_HV_L0

DSI HV Tile Configuration; Left

Address: 0x400F4080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.130 UDB_DSI0_HV_L1

DSI HV Tile Configuration; Left

Address: 0x400F4081

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.131 UDB_DSI0_HV_L2

DSI HV Tile Configuration; Left

Address: 0x400F4082

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.132 UDB_DSI0_HV_L3

DSI HV Tile Configuration; Left

Address: 0x400F4083

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.133 UDB_DSI0_HV_L4

DSI HV Tile Configuration; Left

Address: 0x400F4084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.134 UDB_DSI0_HV_L5

DSI HV Tile Configuration; Left

Address: 0x400F4085

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.135 UDB_DSI0_HV_L6

DSI HV Tile Configuration; Left

Address: 0x400F4086

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.136 UDB_DSI0_HV_L7

DSI HV Tile Configuration; Left

Address: 0x400F4087

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.137 UDB_DSI0_HV_L8

DSI HV Tile Configuration; Left

Address: 0x400F4088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.138 UDB_DSI0_HV_L9

DSI HV Tile Configuration; Left

Address: 0x400F4089

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.139 UDB_DSI0_HV_L10

DSI HV Tile Configuration; Left

Address: 0x400F408A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.140 UDB_DSI0_HV_L11

DSI HV Tile Configuration; Left

Address: 0x400F408B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.141 UDB_DSI0_HV_L12

DSI HV Tile Configuration; Left

Address: 0x400F408C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.142 UDB_DSI0_HV_L13

DSI HV Tile Configuration; Left

Address: 0x400F408D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.143 UDB_DSI0_HV_L14

DSI HV Tile Configuration; Left

Address: 0x400F408E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.144 UDB_DSI0_HV_L15

DSI HV Tile Configuration; Left

Address: 0x400F408F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.145 UDB_DSI0_HS0

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.146 UDB_DSI0_HS1

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4091

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.147 UDB_DSI0_HS2

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4092

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.148 UDB_DSI0_HS3

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4093

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.149 UDB_DSI0_HS4

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.150 UDB_DSI0_HS5

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4095

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.151 UDB_DSI0_HS6

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4096

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.152 UDB_DSI0_HS7

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4097

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.153 UDB_DSI0_HS8

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.154 UDB_DSI0_HS9

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4099

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.155 UDB_DSI0_HS10

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F409A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.156 UDB_DSI0_HS11

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F409B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.157 UDB_DSI0_HS12

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F409C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.158 UDB_DSI0_HS13

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F409D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.159 UDB_DSI0_HS14

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F409E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.160 UDB_DSI0_HS15

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F409F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.161 UDB_DSI0_HS16

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F40A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.162 UDB_DSI0_HS17

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F40A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.163 UDB_DSI0_HS18

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F40A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.164 UDB_DSI0_HS19

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F40A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.165 UDB_DSI0_HS20

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F40A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.166 UDB_DSI0_HS21

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F40A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.167 UDB_DSI0_HS22

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F40A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.168 UDB_DSI0_HS23

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F40A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.169 UDB_DSI0_HV_R0

DSI HV Tile Configuration; Right

Address: 0x400F40A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.170 UDB_DSI0_HV_R1

DSI HV Tile Configuration; Right

Address: 0x400F40A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.171 UDB_DSI0_HV_R2

DSI HV Tile Configuration; Right

Address: 0x400F40AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.172 UDB_DSI0_HV_R3

DSI HV Tile Configuration; Right

Address: 0x400F40AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.173 UDB_DSI0_HV_R4

DSI HV Tile Configuration; Right

Address: 0x400F40AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.174 UDB_DSI0_HV_R5

DSI HV Tile Configuration; Right

Address: 0x400F40AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.175 UDB_DSI0_HV_R6

DSI HV Tile Configuration; Right

Address: 0x400F40AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.176 UDB_DSI0_HV_R7

DSI HV Tile Configuration; Right

Address: 0x400F40AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.177 UDB_DSI0_HV_R8

DSI HV Tile Configuration; Right

Address: 0x400F40B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.178 UDB_DSI0_HV_R9

DSI HV Tile Configuration; Right

Address: 0x400F40B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.179 UDB_DSI0_HV_R10

DSI HV Tile Configuration; Right

Address: 0x400F40B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.180 UDB_DSI0_HV_R11

DSI HV Tile Configuration; Right

Address: 0x400F40B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.181 UDB_DSI0_HV_R12

DSI HV Tile Configuration; Right

Address: 0x400F40B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.182 UDB_DSI0_HV_R13

DSI HV Tile Configuration; Right

Address: 0x400F40B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.183 UDB_DSI0_HV_R14

DSI HV Tile Configuration; Right

Address: 0x400F40B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.184 UDB_DSI0_HV_R15

DSI HV Tile Configuration; Right

Address: 0x400F40B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.185 UDB_DSI0_DSIINP0

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F40C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.186 UDB_DSI0_DSIINP1

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F40C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.187 UDB_DSI0_DSIINP2

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F40C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.188 UDB_DSI0_DSIINP3

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F40C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.189 UDB_DSI0_DSIINP4

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F40C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.190 UDB_DSI0_DSIINP5

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F40CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.191 UDB_DSI0_DSIOUTP0

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F40CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.192 UDB_DSI0_DSIOUTP1

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F40CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.193 UDB_DSI0_DSIOUTP2

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F40D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.194 UDB_DSI0_DSIOUTP3

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F40D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.195 UDB_DSI0_DSIOUTT0

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F40D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.196 UDB_DSI0_DSIOUTT1

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F40D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.197 UDB_DSI0_DSIOUTT2

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F40D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.198 UDB_DSI0_DSIOUTT3

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F40DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.199 UDB_DSI0_DSIOUTT4

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F40DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.200 UDB_DSI0_DSIOUTT5

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F40DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.201 UDB_DSI0_VS0

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F40E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.202 UDB_DSI0_VS1

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F40E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.203 UDB_DSI0_VS2

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F40E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.204 UDB_DSI0_VS3

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F40E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.205 UDB_DSI0_VS4

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F40E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.206 UDB_DSI0_VS5

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F40EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.207 UDB_DSI0_VS6

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F40EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.208 UDB_DSI0_VS7

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F40EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.209 UDB_DSI1_HC0

DSI HC Tile Configuration

Address: 0x400F4100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.210 UDB_DSI1_HC1

DSI HC Tile Configuration

Address: 0x400F4101

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.211 UDB_DSI1_HC2

DSI HC Tile Configuration

Address: 0x400F4102

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.212 UDB_DSI1_HC3

DSI HC Tile Configuration

Address: 0x400F4103

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.213 UDB_DSI1_HC4

DSI HC Tile Configuration

Address: 0x400F4104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.214 UDB_DSI1_HC5

DSI HC Tile Configuration

Address: 0x400F4105

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.215 UDB_DSI1_HC6

DSI HC Tile Configuration

Address: 0x400F4106

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.216 UDB_DSI1_HC7

DSI HC Tile Configuration

Address: 0x400F4107

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.217 UDB_DSI1_HC8

DSI HC Tile Configuration

Address: 0x400F4108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.218 UDB_DSI1_HC9

DSI HC Tile Configuration

Address: 0x400F4109

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.219 UDB_DSI1_HC10

DSI HC Tile Configuration

Address: 0x400F410A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.220 UDB_DSI1_HC11

DSI HC Tile Configuration

Address: 0x400F410B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.221 UDB_DSI1_HC12

DSI HC Tile Configuration

Address: 0x400F410C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.222 UDB_DSI1_HC13

DSI HC Tile Configuration

Address: 0x400F410D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.223 UDB_DSI1_HC14

DSI HC Tile Configuration

Address: 0x400F410E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.224 UDB_DSI1_HC15

DSI HC Tile Configuration

Address: 0x400F410F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.225 UDB_DSI1_HC16

DSI HC Tile Configuration

Address: 0x400F4110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.226 UDB_DSI1_HC17

DSI HC Tile Configuration

Address: 0x400F4111

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.227 UDB_DSI1_HC18

DSI HC Tile Configuration

Address: 0x400F4112

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.228 UDB_DSI1_HC19

DSI HC Tile Configuration

Address: 0x400F4113

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.229 UDB_DSI1_HC20

DSI HC Tile Configuration

Address: 0x400F4114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.230 UDB_DSI1_HC21

DSI HC Tile Configuration

Address: 0x400F4115

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.231 UDB_DSI1_HC22

DSI HC Tile Configuration

Address: 0x400F4116

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.232 UDB_DSI1_HC23

DSI HC Tile Configuration

Address: 0x400F4117

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.233 UDB_DSI1_HC24

DSI HC Tile Configuration

Address: 0x400F4118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.234 UDB_DSI1_HC25

DSI HC Tile Configuration

Address: 0x400F4119

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.235 UDB_DSI1_HC26

DSI HC Tile Configuration

Address: 0x400F411A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.236 UDB_DSI1_HC27

DSI HC Tile Configuration

Address: 0x400F411B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.237 UDB_DSI1_HC28

DSI HC Tile Configuration

Address: 0x400F411C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.238 UDB_DSI1_HC29

DSI HC Tile Configuration

Address: 0x400F411D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.239 UDB_DSI1_HC30

DSI HC Tile Configuration

Address: 0x400F411E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.240 UDB_DSI1_HC31

DSI HC Tile Configuration

Address: 0x400F411F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.241 UDB_DSI1_HC32

DSI HC Tile Configuration

Address: 0x400F4120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.242 UDB_DSI1_HC33

DSI HC Tile Configuration

Address: 0x400F4121

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.243 UDB_DSI1_HC34

DSI HC Tile Configuration

Address: 0x400F4122

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.244 UDB_DSI1_HC35

DSI HC Tile Configuration

Address: 0x400F4123

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.245 UDB_DSI1_HC36

DSI HC Tile Configuration

Address: 0x400F4124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.246 UDB_DSI1_HC37

DSI HC Tile Configuration

Address: 0x400F4125

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.247 UDB_DSI1_HC38

DSI HC Tile Configuration

Address: 0x400F4126

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.248 UDB_DSI1_HC39

DSI HC Tile Configuration

Address: 0x400F4127

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.249 UDB_DSI1_HC40

DSI HC Tile Configuration

Address: 0x400F4128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.250 UDB_DSI1_HC41

DSI HC Tile Configuration

Address: 0x400F4129

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.251 UDB_DSI1_HC42

DSI HC Tile Configuration

Address: 0x400F412A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.252 UDB_DSI1_HC43

DSI HC Tile Configuration

Address: 0x400F412B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.253 UDB_DSI1_HC44

DSI HC Tile Configuration

Address: 0x400F412C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.254 UDB_DSI1_HC45

DSI HC Tile Configuration

Address: 0x400F412D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.255 UDB_DSI1_HC46

DSI HC Tile Configuration

Address: 0x400F412E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.256 UDB_DSI1_HC47

DSI HC Tile Configuration

Address: 0x400F412F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.257 UDB_DSI1_HC48

DSI HC Tile Configuration

Address: 0x400F4130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.258 UDB_DSI1_HC49

DSI HC Tile Configuration

Address: 0x400F4131

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.259 UDB_DSI1_HC50

DSI HC Tile Configuration

Address: 0x400F4132

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.260 UDB_DSI1_HC51

DSI HC Tile Configuration

Address: 0x400F4133

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.261 UDB_DSI1_HC52

DSI HC Tile Configuration

Address: 0x400F4134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.262 UDB_DSI1_HC53

DSI HC Tile Configuration

Address: 0x400F4135

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.263 UDB_DSI1_HC54

DSI HC Tile Configuration

Address: 0x400F4136

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.264 UDB_DSI1_HC55

DSI HC Tile Configuration

Address: 0x400F4137

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.265 UDB_DSI1_HC56

DSI HC Tile Configuration

Address: 0x400F4138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.266 UDB_DSI1_HC57

DSI HC Tile Configuration

Address: 0x400F4139

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.267 UDB_DSI1_HC58

DSI HC Tile Configuration

Address: 0x400F413A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.268 UDB_DSI1_HC59

DSI HC Tile Configuration

Address: 0x400F413B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.269 UDB_DSI1_HC60

DSI HC Tile Configuration

Address: 0x400F413C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.270 UDB_DSI1_HC61

DSI HC Tile Configuration

Address: 0x400F413D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.271 UDB_DSI1_HC62

DSI HC Tile Configuration

Address: 0x400F413E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.272 UDB_DSI1_HC63

DSI HC Tile Configuration

Address: 0x400F413F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.273 UDB_DSI1_HC64

DSI HC Tile Configuration

Address: 0x400F4140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.274 UDB_DSI1_HC65

DSI HC Tile Configuration

Address: 0x400F4141

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.275 UDB_DSI1_HC66

DSI HC Tile Configuration

Address: 0x400F4142

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.276 UDB_DSI1_HC67

DSI HC Tile Configuration

Address: 0x400F4143

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.277 UDB_DSI1_HC68

DSI HC Tile Configuration

Address: 0x400F4144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.278 UDB_DSI1_HC69

DSI HC Tile Configuration

Address: 0x400F4145

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.279 UDB_DSI1_HC70

DSI HC Tile Configuration

Address: 0x400F4146

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.280 UDB_DSI1_HC71

DSI HC Tile Configuration

Address: 0x400F4147

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.281 UDB_DSI1_HC72

DSI HC Tile Configuration

Address: 0x400F4148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.282 UDB_DSI1_HC73

DSI HC Tile Configuration

Address: 0x400F4149

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.283 UDB_DSI1_HC74

DSI HC Tile Configuration

Address: 0x400F414A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.284 UDB_DSI1_HC75

DSI HC Tile Configuration

Address: 0x400F414B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.285 UDB_DSI1_HC76

DSI HC Tile Configuration

Address: 0x400F414C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.286 UDB_DSI1_HC77

DSI HC Tile Configuration

Address: 0x400F414D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.287 UDB_DSI1_HC78

DSI HC Tile Configuration

Address: 0x400F414E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.288 UDB_DSI1_HC79

DSI HC Tile Configuration

Address: 0x400F414F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.289 UDB_DSI1_HC80

DSI HC Tile Configuration

Address: 0x400F4150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.290 UDB_DSI1_HC81

DSI HC Tile Configuration

Address: 0x400F4151

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.291 UDB_DSI1_HC82

DSI HC Tile Configuration

Address: 0x400F4152

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.292 UDB_DSI1_HC83

DSI HC Tile Configuration

Address: 0x400F4153

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.293 UDB_DSI1_HC84

DSI HC Tile Configuration

Address: 0x400F4154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.294 UDB_DSI1_HC85

DSI HC Tile Configuration

Address: 0x400F4155

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.295 UDB_DSI1_HC86

DSI HC Tile Configuration

Address: 0x400F4156

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.296 UDB_DSI1_HC87

DSI HC Tile Configuration

Address: 0x400F4157

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.297 UDB_DSI1_HC88

DSI HC Tile Configuration

Address: 0x400F4158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.298 UDB_DSI1_HC89

DSI HC Tile Configuration

Address: 0x400F4159

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.299 UDB_DSI1_HC90

DSI HC Tile Configuration

Address: 0x400F415A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.300 UDB_DSI1_HC91

DSI HC Tile Configuration

Address: 0x400F415B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.301 UDB_DSI1_HC92

DSI HC Tile Configuration

Address: 0x400F415C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.302 UDB_DSI1_HC93

DSI HC Tile Configuration

Address: 0x400F415D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.303 UDB_DSI1_HC94

DSI HC Tile Configuration

Address: 0x400F415E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.304 UDB_DSI1_HC95

DSI HC Tile Configuration

Address: 0x400F415F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.305 UDB_DSI1_HC96

DSI HC Tile Configuration

Address: 0x400F4160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.306 UDB_DSI1_HC97

DSI HC Tile Configuration

Address: 0x400F4161

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.307 UDB_DSI1_HC98

DSI HC Tile Configuration

Address: 0x400F4162

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.308 UDB_DSI1_HC99

DSI HC Tile Configuration

Address: 0x400F4163

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.309 UDB_DSI1_HC100

DSI HC Tile Configuration

Address: 0x400F4164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.310 UDB_DSI1_HC101

DSI HC Tile Configuration

Address: 0x400F4165

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.311 UDB_DSI1_HC102

DSI HC Tile Configuration

Address: 0x400F4166

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.312 UDB_DSI1_HC103

DSI HC Tile Configuration

Address: 0x400F4167

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.313 UDB_DSI1_HC104

DSI HC Tile Configuration

Address: 0x400F4168

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.314 UDB_DSI1_HC105

DSI HC Tile Configuration

Address: 0x400F4169

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.315 UDB_DSI1_HC106

DSI HC Tile Configuration

Address: 0x400F416A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.316 UDB_DSI1_HC107

DSI HC Tile Configuration

Address: 0x400F416B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.317 UDB_DSI1_HC108

DSI HC Tile Configuration

Address: 0x400F416C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.318 UDB_DSI1_HC109

DSI HC Tile Configuration

Address: 0x400F416D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.319 UDB_DSI1_HC110

DSI HC Tile Configuration

Address: 0x400F416E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.320 UDB_DSI1_HC111

DSI HC Tile Configuration

Address: 0x400F416F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.321 UDB_DSI1_HC112

DSI HC Tile Configuration

Address: 0x400F4170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.322 UDB_DSI1_HC113

DSI HC Tile Configuration

Address: 0x400F4171

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.323 UDB_DSI1_HC114

DSI HC Tile Configuration

Address: 0x400F4172

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.324 UDB_DSI1_HC115

DSI HC Tile Configuration

Address: 0x400F4173

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.325 UDB_DSI1_HC116

DSI HC Tile Configuration

Address: 0x400F4174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.326 UDB_DSI1_HC117

DSI HC Tile Configuration

Address: 0x400F4175

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.327 UDB_DSI1_HC118

DSI HC Tile Configuration

Address: 0x400F4176

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.328 UDB_DSI1_HC119

DSI HC Tile Configuration

Address: 0x400F4177

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.329 UDB_DSI1_HC120

DSI HC Tile Configuration

Address: 0x400F4178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.330 UDB_DSI1_HC121

DSI HC Tile Configuration

Address: 0x400F4179

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.331 UDB_DSI1_HC122

DSI HC Tile Configuration

Address: 0x400F417A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.332 UDB_DSI1_HC123

DSI HC Tile Configuration

Address: 0x400F417B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.333 UDB_DSI1_HC124

DSI HC Tile Configuration

Address: 0x400F417C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.334 UDB_DSI1_HC125

DSI HC Tile Configuration

Address: 0x400F417D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.335 UDB_DSI1_HC126

DSI HC Tile Configuration

Address: 0x400F417E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.336 UDB_DSI1_HC127

DSI HC Tile Configuration

Address: 0x400F417F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.337 UDB_DSI1_HV_L0

DSI HV Tile Configuration; Left

Address: 0x400F4180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.338 UDB_DSI1_HV_L1

DSI HV Tile Configuration; Left

Address: 0x400F4181

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.339 UDB_DSI1_HV_L2

DSI HV Tile Configuration; Left

Address: 0x400F4182

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.340 UDB_DSI1_HV_L3

DSI HV Tile Configuration; Left

Address: 0x400F4183

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.341 UDB_DSI1_HV_L4

DSI HV Tile Configuration; Left

Address: 0x400F4184

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.342 UDB_DSI1_HV_L5

DSI HV Tile Configuration; Left

Address: 0x400F4185

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.343 UDB_DSI1_HV_L6

DSI HV Tile Configuration; Left

Address: 0x400F4186

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.344 UDB_DSI1_HV_L7

DSI HV Tile Configuration; Left

Address: 0x400F4187

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.345 UDB_DSI1_HV_L8

DSI HV Tile Configuration; Left

Address: 0x400F4188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.346 UDB_DSI1_HV_L9

DSI HV Tile Configuration; Left

Address: 0x400F4189

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.347 UDB_DSI1_HV_L10

DSI HV Tile Configuration; Left

Address: 0x400F418A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.348 UDB_DSI1_HV_L11

DSI HV Tile Configuration; Left

Address: 0x400F418B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.349 UDB_DSI1_HV_L12

DSI HV Tile Configuration; Left

Address: 0x400F418C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.350 UDB_DSI1_HV_L13

DSI HV Tile Configuration; Left

Address: 0x400F418D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.351 UDB_DSI1_HV_L14

DSI HV Tile Configuration; Left

Address: 0x400F418E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.352 UDB_DSI1_HV_L15

DSI HV Tile Configuration; Left

Address: 0x400F418F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.353 UDB_DSI1_HS0

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.354 UDB_DSI1_HS1

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4191

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.355 UDB_DSI1_HS2

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4192

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.356 UDB_DSI1_HS3

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4193

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.357 UDB_DSI1_HS4

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4194

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.358 UDB_DSI1_HS5

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4195

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.359 UDB_DSI1_HS6

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4196

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.360 UDB_DSI1_HS7

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4197

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.361 UDB_DSI1_HS8

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4198

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.362 UDB_DSI1_HS9

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4199

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.363 UDB_DSI1_HS10

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F419A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.364 UDB_DSI1_HS11

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F419B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.365 UDB_DSI1_HS12

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F419C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.366 UDB_DSI1_HS13

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F419D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.367 UDB_DSI1_HS14

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F419E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.368 UDB_DSI1_HS15

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F419F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.369 UDB_DSI1_HS16

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F41A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.370 UDB_DSI1_HS17

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F41A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.371 UDB_DSI1_HS18

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F41A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.372 UDB_DSI1_HS19

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F41A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.373 UDB_DSI1_HS20

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F41A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.374 UDB_DSI1_HS21

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F41A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.375 UDB_DSI1_HS22

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F41A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.376 UDB_DSI1_HS23

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F41A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.377 UDB_DSI1_HV_R0

DSI HV Tile Configuration; Right

Address: 0x400F41A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.378 UDB_DSI1_HV_R1

DSI HV Tile Configuration; Right

Address: 0x400F41A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.379 UDB_DSI1_HV_R2

DSI HV Tile Configuration; Right

Address: 0x400F41AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.380 UDB_DSI1_HV_R3

DSI HV Tile Configuration; Right

Address: 0x400F41AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.381 UDB_DSI1_HV_R4

DSI HV Tile Configuration; Right

Address: 0x400F41AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.382 UDB_DSI1_HV_R5

DSI HV Tile Configuration; Right

Address: 0x400F41AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.383 UDB_DSI1_HV_R6

DSI HV Tile Configuration; Right

Address: 0x400F41AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.384 UDB_DSI1_HV_R7

DSI HV Tile Configuration; Right

Address: 0x400F41AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.385 UDB_DSI1_HV_R8

DSI HV Tile Configuration; Right

Address: 0x400F41B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.386 UDB_DSI1_HV_R9

DSI HV Tile Configuration; Right

Address: 0x400F41B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.387 UDB_DSI1_HV_R10

DSI HV Tile Configuration; Right

Address: 0x400F41B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.388 UDB_DSI1_HV_R11

DSI HV Tile Configuration; Right

Address: 0x400F41B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.389 UDB_DSI1_HV_R12

DSI HV Tile Configuration; Right

Address: 0x400F41B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.390 UDB_DSI1_HV_R13

DSI HV Tile Configuration; Right

Address: 0x400F41B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.391 UDB_DSI1_HV_R14

DSI HV Tile Configuration; Right

Address: 0x400F41B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.392 UDB_DSI1_HV_R15

DSI HV Tile Configuration; Right

Address: 0x400F41B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.393 UDB_DSI1_DSIINP0

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F41C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.394 UDB_DSI1_DSIINP1

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F41C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.395 UDB_DSI1_DSIINP2

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F41C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.396 UDB_DSI1_DSIINP3

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F41C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.397 UDB_DSI1_DSIINP4

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F41C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.398 UDB_DSI1_DSIINP5

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F41CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.399 UDB_DSI1_DSIOUTP0

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F41CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.400 UDB_DSI1_DSIOUTP1

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F41CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.401 UDB_DSI1_DSIOUTP2

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F41D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.402 UDB_DSI1_DSIOUTP3

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F41D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.403 UDB_DSI1_DSIOUTT0

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F41D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.404 UDB_DSI1_DSIOUTT1

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F41D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.405 UDB_DSI1_DSIOUTT2

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F41D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.406 UDB_DSI1_DSIOUTT3

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F41DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.407 UDB_DSI1_DSIOUTT4

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F41DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.408 UDB_DSI1_DSIOUTT5

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F41DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.409 UDB_DSI1_VS0

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F41E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.410 UDB_DSI1_VS1

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F41E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.411 UDB_DSI1_VS2

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F41E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.412 UDB_DSI1_VS3

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F41E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.413 UDB_DSI1_VS4

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F41E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.414 UDB_DSI1_VS5

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F41EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.415 UDB_DSI1_VS6

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F41EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.416 UDB_DSI1_VS7

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F41EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.417 UDB_DSI2_HC0

DSI HC Tile Configuration

Address: 0x400F4200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.418 UDB_DSI2_HC1

DSI HC Tile Configuration

Address: 0x400F4201

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.419 UDB_DSI2_HC2

DSI HC Tile Configuration

Address: 0x400F4202

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.420 UDB_DSI2_HC3

DSI HC Tile Configuration

Address: 0x400F4203

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.421 UDB_DSI2_HC4

DSI HC Tile Configuration

Address: 0x400F4204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.422 UDB_DSI2_HC5

DSI HC Tile Configuration

Address: 0x400F4205

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.423 UDB_DSI2_HC6

DSI HC Tile Configuration

Address: 0x400F4206

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.424 UDB_DSI2_HC7

DSI HC Tile Configuration

Address: 0x400F4207

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.425 UDB_DSI2_HC8

DSI HC Tile Configuration

Address: 0x400F4208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.426 UDB_DSI2_HC9

DSI HC Tile Configuration

Address: 0x400F4209

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.427 UDB_DSI2_HC10

DSI HC Tile Configuration

Address: 0x400F420A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.428 UDB_DSI2_HC11

DSI HC Tile Configuration

Address: 0x400F420B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.429 UDB_DSI2_HC12

DSI HC Tile Configuration

Address: 0x400F420C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.430 UDB_DSI2_HC13

DSI HC Tile Configuration

Address: 0x400F420D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.431 UDB_DSI2_HC14

DSI HC Tile Configuration

Address: 0x400F420E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.432 UDB_DSI2_HC15

DSI HC Tile Configuration

Address: 0x400F420F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.433 UDB_DSI2_HC16

DSI HC Tile Configuration

Address: 0x400F4210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.434 UDB_DSI2_HC17

DSI HC Tile Configuration

Address: 0x400F4211

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.435 UDB_DSI2_HC18

DSI HC Tile Configuration

Address: 0x400F4212

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.436 UDB_DSI2_HC19

DSI HC Tile Configuration

Address: 0x400F4213

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.437 UDB_DSI2_HC20

DSI HC Tile Configuration

Address: 0x400F4214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.438 UDB_DSI2_HC21

DSI HC Tile Configuration

Address: 0x400F4215

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.439 UDB_DSI2_HC22

DSI HC Tile Configuration

Address: 0x400F4216

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.440 UDB_DSI2_HC23

DSI HC Tile Configuration

Address: 0x400F4217

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.441 UDB_DSI2_HC24

DSI HC Tile Configuration

Address: 0x400F4218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.442 UDB_DSI2_HC25

DSI HC Tile Configuration

Address: 0x400F4219

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.443 UDB_DSI2_HC26

DSI HC Tile Configuration

Address: 0x400F421A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.444 UDB_DSI2_HC27

DSI HC Tile Configuration

Address: 0x400F421B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.445 UDB_DSI2_HC28

DSI HC Tile Configuration

Address: 0x400F421C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.446 UDB_DSI2_HC29

DSI HC Tile Configuration

Address: 0x400F421D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.447 UDB_DSI2_HC30

DSI HC Tile Configuration

Address: 0x400F421E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.448 UDB_DSI2_HC31

DSI HC Tile Configuration

Address: 0x400F421F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.449 UDB_DSI2_HC32

DSI HC Tile Configuration

Address: 0x400F4220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.450 UDB_DSI2_HC33

DSI HC Tile Configuration

Address: 0x400F4221

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.451 UDB_DSI2_HC34

DSI HC Tile Configuration

Address: 0x400F4222

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.452 UDB_DSI2_HC35

DSI HC Tile Configuration

Address: 0x400F4223

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.453 UDB_DSI2_HC36

DSI HC Tile Configuration

Address: 0x400F4224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.454 UDB_DSI2_HC37

DSI HC Tile Configuration

Address: 0x400F4225

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.455 UDB_DSI2_HC38

DSI HC Tile Configuration

Address: 0x400F4226

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.456 UDB_DSI2_HC39

DSI HC Tile Configuration

Address: 0x400F4227

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.457 UDB_DSI2_HC40

DSI HC Tile Configuration

Address: 0x400F4228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.458 UDB_DSI2_HC41

DSI HC Tile Configuration

Address: 0x400F4229

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.459 UDB_DSI2_HC42

DSI HC Tile Configuration

Address: 0x400F422A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.460 UDB_DSI2_HC43

DSI HC Tile Configuration

Address: 0x400F422B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.461 UDB_DSI2_HC44

DSI HC Tile Configuration

Address: 0x400F422C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.462 UDB_DSI2_HC45

DSI HC Tile Configuration

Address: 0x400F422D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.463 UDB_DSI2_HC46

DSI HC Tile Configuration

Address: 0x400F422E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.464 UDB_DSI2_HC47

DSI HC Tile Configuration

Address: 0x400F422F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.465 UDB_DSI2_HC48

DSI HC Tile Configuration

Address: 0x400F4230

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.466 UDB_DSI2_HC49

DSI HC Tile Configuration

Address: 0x400F4231

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.467 UDB_DSI2_HC50

DSI HC Tile Configuration

Address: 0x400F4232

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.468 UDB_DSI2_HC51

DSI HC Tile Configuration

Address: 0x400F4233

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.469 UDB_DSI2_HC52

DSI HC Tile Configuration

Address: 0x400F4234

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.470 UDB_DSI2_HC53

DSI HC Tile Configuration

Address: 0x400F4235

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.471 UDB_DSI2_HC54

DSI HC Tile Configuration

Address: 0x400F4236

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.472 UDB_DSI2_HC55

DSI HC Tile Configuration

Address: 0x400F4237

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.473 UDB_DSI2_HC56

DSI HC Tile Configuration

Address: 0x400F4238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.474 UDB_DSI2_HC57

DSI HC Tile Configuration

Address: 0x400F4239

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.475 UDB_DSI2_HC58

DSI HC Tile Configuration

Address: 0x400F423A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.476 UDB_DSI2_HC59

DSI HC Tile Configuration

Address: 0x400F423B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.477 UDB_DSI2_HC60

DSI HC Tile Configuration

Address: 0x400F423C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.478 UDB_DSI2_HC61

DSI HC Tile Configuration

Address: 0x400F423D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.479 UDB_DSI2_HC62

DSI HC Tile Configuration

Address: 0x400F423E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.480 UDB_DSI2_HC63

DSI HC Tile Configuration

Address: 0x400F423F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.481 UDB_DSI2_HC64

DSI HC Tile Configuration

Address: 0x400F4240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.482 UDB_DSI2_HC65

DSI HC Tile Configuration

Address: 0x400F4241

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.483 UDB_DSI2_HC66

DSI HC Tile Configuration

Address: 0x400F4242

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.484 UDB_DSI2_HC67

DSI HC Tile Configuration

Address: 0x400F4243

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.485 UDB_DSI2_HC68

DSI HC Tile Configuration

Address: 0x400F4244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.486 UDB_DSI2_HC69

DSI HC Tile Configuration

Address: 0x400F4245

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.487 UDB_DSI2_HC70

DSI HC Tile Configuration

Address: 0x400F4246

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.488 UDB_DSI2_HC71

DSI HC Tile Configuration

Address: 0x400F4247

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.489 UDB_DSI2_HC72

DSI HC Tile Configuration

Address: 0x400F4248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.490 UDB_DSI2_HC73

DSI HC Tile Configuration

Address: 0x400F4249

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.491 UDB_DSI2_HC74

DSI HC Tile Configuration

Address: 0x400F424A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.492 UDB_DSI2_HC75

DSI HC Tile Configuration

Address: 0x400F424B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.493 UDB_DSI2_HC76

DSI HC Tile Configuration

Address: 0x400F424C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.494 UDB_DSI2_HC77

DSI HC Tile Configuration

Address: 0x400F424D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.495 UDB_DSI2_HC78

DSI HC Tile Configuration

Address: 0x400F424E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.496 UDB_DSI2_HC79

DSI HC Tile Configuration

Address: 0x400F424F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.497 UDB_DSI2_HC80

DSI HC Tile Configuration

Address: 0x400F4250

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.498 UDB_DSI2_HC81

DSI HC Tile Configuration

Address: 0x400F4251

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.499 UDB_DSI2_HC82

DSI HC Tile Configuration

Address: 0x400F4252

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.500 UDB_DSI2_HC83

DSI HC Tile Configuration

Address: 0x400F4253

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.501 UDB_DSI2_HC84

DSI HC Tile Configuration

Address: 0x400F4254

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.502 UDB_DSI2_HC85

DSI HC Tile Configuration

Address: 0x400F4255

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.503 UDB_DSI2_HC86

DSI HC Tile Configuration

Address: 0x400F4256

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.504 UDB_DSI2_HC87

DSI HC Tile Configuration

Address: 0x400F4257

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.505 UDB_DSI2_HC88

DSI HC Tile Configuration

Address: 0x400F4258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.506 UDB_DSI2_HC89

DSI HC Tile Configuration

Address: 0x400F4259

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.507 UDB_DSI2_HC90

DSI HC Tile Configuration

Address: 0x400F425A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.508 UDB_DSI2_HC91

DSI HC Tile Configuration

Address: 0x400F425B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.509 UDB_DSI2_HC92

DSI HC Tile Configuration

Address: 0x400F425C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.510 UDB_DSI2_HC93

DSI HC Tile Configuration

Address: 0x400F425D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.511 UDB_DSI2_HC94

DSI HC Tile Configuration

Address: 0x400F425E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.512 UDB_DSI2_HC95

DSI HC Tile Configuration

Address: 0x400F425F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.513 UDB_DSI2_HC96

DSI HC Tile Configuration

Address: 0x400F4260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.514 UDB_DSI2_HC97

DSI HC Tile Configuration

Address: 0x400F4261

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.515 UDB_DSI2_HC98

DSI HC Tile Configuration

Address: 0x400F4262

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.516 UDB_DSI2_HC99

DSI HC Tile Configuration

Address: 0x400F4263

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.517 UDB_DSI2_HC100

DSI HC Tile Configuration

Address: 0x400F4264

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.518 UDB_DSI2_HC101

DSI HC Tile Configuration

Address: 0x400F4265

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.519 UDB_DSI2_HC102

DSI HC Tile Configuration

Address: 0x400F4266

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.520 UDB_DSI2_HC103

DSI HC Tile Configuration

Address: 0x400F4267

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.521 UDB_DSI2_HC104

DSI HC Tile Configuration

Address: 0x400F4268

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.522 UDB_DSI2_HC105

DSI HC Tile Configuration

Address: 0x400F4269

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.523 UDB_DSI2_HC106

DSI HC Tile Configuration

Address: 0x400F426A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.524 UDB_DSI2_HC107

DSI HC Tile Configuration

Address: 0x400F426B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.525 UDB_DSI2_HC108

DSI HC Tile Configuration

Address: 0x400F426C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.526 UDB_DSI2_HC109

DSI HC Tile Configuration

Address: 0x400F426D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.527 UDB_DSI2_HC110

DSI HC Tile Configuration

Address: 0x400F426E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.528 UDB_DSI2_HC111

DSI HC Tile Configuration

Address: 0x400F426F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.529 UDB_DSI2_HC112

DSI HC Tile Configuration

Address: 0x400F4270

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.530 UDB_DSI2_HC113

DSI HC Tile Configuration

Address: 0x400F4271

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.531 UDB_DSI2_HC114

DSI HC Tile Configuration

Address: 0x400F4272

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.532 UDB_DSI2_HC115

DSI HC Tile Configuration

Address: 0x400F4273

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.533 UDB_DSI2_HC116

DSI HC Tile Configuration

Address: 0x400F4274

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.534 UDB_DSI2_HC117

DSI HC Tile Configuration

Address: 0x400F4275

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.535 UDB_DSI2_HC118

DSI HC Tile Configuration

Address: 0x400F4276

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.536 UDB_DSI2_HC119

DSI HC Tile Configuration

Address: 0x400F4277

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.537 UDB_DSI2_HC120

DSI HC Tile Configuration

Address: 0x400F4278

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.538 UDB_DSI2_HC121

DSI HC Tile Configuration

Address: 0x400F4279

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.539 UDB_DSI2_HC122

DSI HC Tile Configuration

Address: 0x400F427A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.540 UDB_DSI2_HC123

DSI HC Tile Configuration

Address: 0x400F427B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.541 UDB_DSI2_HC124

DSI HC Tile Configuration

Address: 0x400F427C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.542 UDB_DSI2_HC125

DSI HC Tile Configuration

Address: 0x400F427D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.543 UDB_DSI2_HC126

DSI HC Tile Configuration

Address: 0x400F427E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.544 UDB_DSI2_HC127

DSI HC Tile Configuration

Address: 0x400F427F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.545 UDB_DSI2_HV_L0

DSI HV Tile Configuration; Left

Address: 0x400F4280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.546 UDB_DSI2_HV_L1

DSI HV Tile Configuration; Left

Address: 0x400F4281

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.547 UDB_DSI2_HV_L2

DSI HV Tile Configuration; Left

Address: 0x400F4282

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.548 UDB_DSI2_HV_L3

DSI HV Tile Configuration; Left

Address: 0x400F4283

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.549 UDB_DSI2_HV_L4

DSI HV Tile Configuration; Left

Address: 0x400F4284

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.550 UDB_DSI2_HV_L5

DSI HV Tile Configuration; Left

Address: 0x400F4285

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.551 UDB_DSI2_HV_L6

DSI HV Tile Configuration; Left

Address: 0x400F4286

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.552 UDB_DSI2_HV_L7

DSI HV Tile Configuration; Left

Address: 0x400F4287

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.553 UDB_DSI2_HV_L8

DSI HV Tile Configuration; Left

Address: 0x400F4288

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.554 UDB_DSI2_HV_L9

DSI HV Tile Configuration; Left

Address: 0x400F4289

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.555 UDB_DSI2_HV_L10

DSI HV Tile Configuration; Left

Address: 0x400F428A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.556 UDB_DSI2_HV_L11

DSI HV Tile Configuration; Left

Address: 0x400F428B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.557 UDB_DSI2_HV_L12

DSI HV Tile Configuration; Left

Address: 0x400F428C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.558 UDB_DSI2_HV_L13

DSI HV Tile Configuration; Left

Address: 0x400F428D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.559 UDB_DSI2_HV_L14

DSI HV Tile Configuration; Left

Address: 0x400F428E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.560 UDB_DSI2_HV_L15

DSI HV Tile Configuration; Left

Address: 0x400F428F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.561 UDB_DSI2_HS0

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4290

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.562 UDB_DSI2_HS1

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4291

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.563 UDB_DSI2_HS2

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4292

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.564 UDB_DSI2_HS3

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4293

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.565 UDB_DSI2_HS4

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4294

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.566 UDB_DSI2_HS5

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4295

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.567 UDB_DSI2_HS6

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4296

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.568 UDB_DSI2_HS7

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4297

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.569 UDB_DSI2_HS8

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4298

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.570 UDB_DSI2_HS9

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4299

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.571 UDB_DSI2_HS10

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F429A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.572 UDB_DSI2_HS11

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F429B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.573 UDB_DSI2_HS12

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F429C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.574 UDB_DSI2_HS13

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F429D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.575 UDB_DSI2_HS14

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F429E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.576 UDB_DSI2_HS15

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F429F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.577 UDB_DSI2_HS16

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F42A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.578 UDB_DSI2_HS17

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F42A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.579 UDB_DSI2_HS18

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F42A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.580 UDB_DSI2_HS19

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F42A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.581 UDB_DSI2_HS20

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F42A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.582 UDB_DSI2_HS21

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F42A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.583 UDB_DSI2_HS22

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F42A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.584 UDB_DSI2_HS23

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F42A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.585 UDB_DSI2_HV_R0

DSI HV Tile Configuration; Right

Address: 0x400F42A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.586 UDB_DSI2_HV_R1

DSI HV Tile Configuration; Right

Address: 0x400F42A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.587 UDB_DSI2_HV_R2

DSI HV Tile Configuration; Right

Address: 0x400F42AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.588 UDB_DSI2_HV_R3

DSI HV Tile Configuration; Right

Address: 0x400F42AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.589 UDB_DSI2_HV_R4

DSI HV Tile Configuration; Right

Address: 0x400F42AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.590 UDB_DSI2_HV_R5

DSI HV Tile Configuration; Right

Address: 0x400F42AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.591 UDB_DSI2_HV_R6

DSI HV Tile Configuration; Right

Address: 0x400F42AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.592 UDB_DSI2_HV_R7

DSI HV Tile Configuration; Right

Address: 0x400F42AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.593 UDB_DSI2_HV_R8

DSI HV Tile Configuration; Right

Address: 0x400F42B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.594 UDB_DSI2_HV_R9

DSI HV Tile Configuration; Right

Address: 0x400F42B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.595 UDB_DSI2_HV_R10

DSI HV Tile Configuration; Right

Address: 0x400F42B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.596 UDB_DSI2_HV_R11

DSI HV Tile Configuration; Right

Address: 0x400F42B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.597 UDB_DSI2_HV_R12

DSI HV Tile Configuration; Right

Address: 0x400F42B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.598 UDB_DSI2_HV_R13

DSI HV Tile Configuration; Right

Address: 0x400F42B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.599 UDB_DSI2_HV_R14

DSI HV Tile Configuration; Right

Address: 0x400F42B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.600 UDB_DSI2_HV_R15

DSI HV Tile Configuration; Right

Address: 0x400F42B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.601 UDB_DSI2_DSIINP0

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F42C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.602 UDB_DSI2_DSIINP1

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F42C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.603 UDB_DSI2_DSIINP2

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F42C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.604 UDB_DSI2_DSIINP3

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F42C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.605 UDB_DSI2_DSIINP4

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F42C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.606 UDB_DSI2_DSIINP5

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F42CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.607 UDB_DSI2_DSIOUTP0

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F42CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.608 UDB_DSI2_DSIOUTP1

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F42CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.609 UDB_DSI2_DSIOUTP2

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F42D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.610 UDB_DSI2_DSIOUTP3

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F42D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.611 UDB_DSI2_DSIOUTT0

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F42D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.612 UDB_DSI2_DSIOUTT1

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F42D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.613 UDB_DSI2_DSIOUTT2

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F42D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.614 UDB_DSI2_DSIOUTT3

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F42DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.615 UDB_DSI2_DSIOUTT4

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F42DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.616 UDB_DSI2_DSIOUTT5

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F42DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.617 UDB_DSI2_VS0

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F42E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.618 UDB_DSI2_VS1

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F42E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.619 UDB_DSI2_VS2

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F42E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.620 UDB_DSI2_VS3

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F42E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.621 UDB_DSI2_VS4

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F42E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.622 UDB_DSI2_VS5

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F42EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.623 UDB_DSI2_VS6

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F42EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.624 UDB_DSI2_VS7

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F42EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.625 UDB_DSI3_HC0

DSI HC Tile Configuration

Address: 0x400F4300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.626 UDB_DSI3_HC1

DSI HC Tile Configuration

Address: 0x400F4301

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.627 UDB_DSI3_HC2

DSI HC Tile Configuration

Address: 0x400F4302

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.628 UDB_DSI3_HC3

DSI HC Tile Configuration

Address: 0x400F4303

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.629 UDB_DSI3_HC4

DSI HC Tile Configuration

Address: 0x400F4304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.630 UDB_DSI3_HC5

DSI HC Tile Configuration

Address: 0x400F4305

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.631 UDB_DSI3_HC6

DSI HC Tile Configuration

Address: 0x400F4306

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.632 UDB_DSI3_HC7

DSI HC Tile Configuration

Address: 0x400F4307

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.633 UDB_DSI3_HC8

DSI HC Tile Configuration

Address: 0x400F4308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.634 UDB_DSI3_HC9

DSI HC Tile Configuration

Address: 0x400F4309

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.635 UDB_DSI3_HC10

DSI HC Tile Configuration

Address: 0x400F430A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.636 UDB_DSI3_HC11

DSI HC Tile Configuration

Address: 0x400F430B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.637 UDB_DSI3_HC12

DSI HC Tile Configuration

Address: 0x400F430C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.638 UDB_DSI3_HC13

DSI HC Tile Configuration

Address: 0x400F430D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.639 UDB_DSI3_HC14

DSI HC Tile Configuration

Address: 0x400F430E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.640 UDB_DSI3_HC15

DSI HC Tile Configuration

Address: 0x400F430F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.641 UDB_DSI3_HC16

DSI HC Tile Configuration

Address: 0x400F4310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.642 UDB_DSI3_HC17

DSI HC Tile Configuration

Address: 0x400F4311

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.643 UDB_DSI3_HC18

DSI HC Tile Configuration

Address: 0x400F4312

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.644 UDB_DSI3_HC19

DSI HC Tile Configuration

Address: 0x400F4313

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.645 UDB_DSI3_HC20

DSI HC Tile Configuration

Address: 0x400F4314

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.646 UDB_DSI3_HC21

DSI HC Tile Configuration

Address: 0x400F4315

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.647 UDB_DSI3_HC22

DSI HC Tile Configuration

Address: 0x400F4316

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.648 UDB_DSI3_HC23

DSI HC Tile Configuration

Address: 0x400F4317

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.649 UDB_DSI3_HC24

DSI HC Tile Configuration

Address: 0x400F4318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.650 UDB_DSI3_HC25

DSI HC Tile Configuration

Address: 0x400F4319

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.651 UDB_DSI3_HC26

DSI HC Tile Configuration

Address: 0x400F431A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.652 UDB_DSI3_HC27

DSI HC Tile Configuration

Address: 0x400F431B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.653 UDB_DSI3_HC28

DSI HC Tile Configuration

Address: 0x400F431C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.654 UDB_DSI3_HC29

DSI HC Tile Configuration

Address: 0x400F431D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.655 UDB_DSI3_HC30

DSI HC Tile Configuration

Address: 0x400F431E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.656 UDB_DSI3_HC31

DSI HC Tile Configuration

Address: 0x400F431F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.657 UDB_DSI3_HC32

DSI HC Tile Configuration

Address: 0x400F4320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.658 UDB_DSI3_HC33

DSI HC Tile Configuration

Address: 0x400F4321

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.659 UDB_DSI3_HC34

DSI HC Tile Configuration

Address: 0x400F4322

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.660 UDB_DSI3_HC35

DSI HC Tile Configuration

Address: 0x400F4323

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.661 UDB_DSI3_HC36

DSI HC Tile Configuration

Address: 0x400F4324

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.662 UDB_DSI3_HC37

DSI HC Tile Configuration

Address: 0x400F4325

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.663 UDB_DSI3_HC38

DSI HC Tile Configuration

Address: 0x400F4326

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.664 UDB_DSI3_HC39

DSI HC Tile Configuration

Address: 0x400F4327

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.665 UDB_DSI3_HC40

DSI HC Tile Configuration

Address: 0x400F4328

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.666 UDB_DSI3_HC41

DSI HC Tile Configuration

Address: 0x400F4329

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.667 UDB_DSI3_HC42

DSI HC Tile Configuration

Address: 0x400F432A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.668 UDB_DSI3_HC43

DSI HC Tile Configuration

Address: 0x400F432B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.669 UDB_DSI3_HC44

DSI HC Tile Configuration

Address: 0x400F432C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.670 UDB_DSI3_HC45

DSI HC Tile Configuration

Address: 0x400F432D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.671 UDB_DSI3_HC46

DSI HC Tile Configuration

Address: 0x400F432E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.672 UDB_DSI3_HC47

DSI HC Tile Configuration

Address: 0x400F432F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.673 UDB_DSI3_HC48

DSI HC Tile Configuration

Address: 0x400F4330

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.674 UDB_DSI3_HC49

DSI HC Tile Configuration

Address: 0x400F4331

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.675 UDB_DSI3_HC50

DSI HC Tile Configuration

Address: 0x400F4332

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.676 UDB_DSI3_HC51

DSI HC Tile Configuration

Address: 0x400F4333

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.677 UDB_DSI3_HC52

DSI HC Tile Configuration

Address: 0x400F4334

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.678 UDB_DSI3_HC53

DSI HC Tile Configuration

Address: 0x400F4335

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.679 UDB_DSI3_HC54

DSI HC Tile Configuration

Address: 0x400F4336

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.680 UDB_DSI3_HC55

DSI HC Tile Configuration

Address: 0x400F4337

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.681 UDB_DSI3_HC56

DSI HC Tile Configuration

Address: 0x400F4338

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.682 UDB_DSI3_HC57

DSI HC Tile Configuration

Address: 0x400F4339

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.683 UDB_DSI3_HC58

DSI HC Tile Configuration

Address: 0x400F433A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.684 UDB_DSI3_HC59

DSI HC Tile Configuration

Address: 0x400F433B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.685 UDB_DSI3_HC60

DSI HC Tile Configuration

Address: 0x400F433C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.686 UDB_DSI3_HC61

DSI HC Tile Configuration

Address: 0x400F433D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.687 UDB_DSI3_HC62

DSI HC Tile Configuration

Address: 0x400F433E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.688 UDB_DSI3_HC63

DSI HC Tile Configuration

Address: 0x400F433F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.689 UDB_DSI3_HC64

DSI HC Tile Configuration

Address: 0x400F4340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.690 UDB_DSI3_HC65

DSI HC Tile Configuration

Address: 0x400F4341

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.691 UDB_DSI3_HC66

DSI HC Tile Configuration

Address: 0x400F4342

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.692 UDB_DSI3_HC67

DSI HC Tile Configuration

Address: 0x400F4343

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.693 UDB_DSI3_HC68

DSI HC Tile Configuration

Address: 0x400F4344

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.694 UDB_DSI3_HC69

DSI HC Tile Configuration

Address: 0x400F4345

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.695 UDB_DSI3_HC70

DSI HC Tile Configuration

Address: 0x400F4346

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.696 UDB_DSI3_HC71

DSI HC Tile Configuration

Address: 0x400F4347

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.697 UDB_DSI3_HC72

DSI HC Tile Configuration

Address: 0x400F4348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.698 UDB_DSI3_HC73

DSI HC Tile Configuration

Address: 0x400F4349

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.699 UDB_DSI3_HC74

DSI HC Tile Configuration

Address: 0x400F434A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.700 UDB_DSI3_HC75

DSI HC Tile Configuration

Address: 0x400F434B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.701 UDB_DSI3_HC76

DSI HC Tile Configuration

Address: 0x400F434C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.702 UDB_DSI3_HC77

DSI HC Tile Configuration

Address: 0x400F434D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.703 UDB_DSI3_HC78

DSI HC Tile Configuration

Address: 0x400F434E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.704 UDB_DSI3_HC79

DSI HC Tile Configuration

Address: 0x400F434F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.705 UDB_DSI3_HC80

DSI HC Tile Configuration

Address: 0x400F4350

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.706 UDB_DSI3_HC81

DSI HC Tile Configuration

Address: 0x400F4351

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.707 UDB_DSI3_HC82

DSI HC Tile Configuration

Address: 0x400F4352

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.708 UDB_DSI3_HC83

DSI HC Tile Configuration

Address: 0x400F4353

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.709 UDB_DSI3_HC84

DSI HC Tile Configuration

Address: 0x400F4354

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.710 UDB_DSI3_HC85

DSI HC Tile Configuration

Address: 0x400F4355

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.711 UDB_DSI3_HC86

DSI HC Tile Configuration

Address: 0x400F4356

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.712 UDB_DSI3_HC87

DSI HC Tile Configuration

Address: 0x400F4357

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.713 UDB_DSI3_HC88

DSI HC Tile Configuration

Address: 0x400F4358

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.714 UDB_DSI3_HC89

DSI HC Tile Configuration

Address: 0x400F4359

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.715 UDB_DSI3_HC90

DSI HC Tile Configuration

Address: 0x400F435A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.716 UDB_DSI3_HC91

DSI HC Tile Configuration

Address: 0x400F435B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.717 UDB_DSI3_HC92

DSI HC Tile Configuration

Address: 0x400F435C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.718 UDB_DSI3_HC93

DSI HC Tile Configuration

Address: 0x400F435D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.719 UDB_DSI3_HC94

DSI HC Tile Configuration

Address: 0x400F435E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.720 UDB_DSI3_HC95

DSI HC Tile Configuration

Address: 0x400F435F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.721 UDB_DSI3_HC96

DSI HC Tile Configuration

Address: 0x400F4360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.722 UDB_DSI3_HC97

DSI HC Tile Configuration

Address: 0x400F4361

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.723 UDB_DSI3_HC98

DSI HC Tile Configuration

Address: 0x400F4362

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.724 UDB_DSI3_HC99

DSI HC Tile Configuration

Address: 0x400F4363

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.725 UDB_DSI3_HC100

DSI HC Tile Configuration

Address: 0x400F4364

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.726 UDB_DSI3_HC101

DSI HC Tile Configuration

Address: 0x400F4365

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.727 UDB_DSI3_HC102

DSI HC Tile Configuration

Address: 0x400F4366

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.728 UDB_DSI3_HC103

DSI HC Tile Configuration

Address: 0x400F4367

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.729 UDB_DSI3_HC104

DSI HC Tile Configuration

Address: 0x400F4368

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.730 UDB_DSI3_HC105

DSI HC Tile Configuration

Address: 0x400F4369

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.731 UDB_DSI3_HC106

DSI HC Tile Configuration

Address: 0x400F436A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.732 UDB_DSI3_HC107

DSI HC Tile Configuration

Address: 0x400F436B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.733 UDB_DSI3_HC108

DSI HC Tile Configuration

Address: 0x400F436C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.734 UDB_DSI3_HC109

DSI HC Tile Configuration

Address: 0x400F436D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.735 UDB_DSI3_HC110

DSI HC Tile Configuration

Address: 0x400F436E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.736 UDB_DSI3_HC111

DSI HC Tile Configuration

Address: 0x400F436F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.737 UDB_DSI3_HC112

DSI HC Tile Configuration

Address: 0x400F4370

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.738 UDB_DSI3_HC113

DSI HC Tile Configuration

Address: 0x400F4371

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.739 UDB_DSI3_HC114

DSI HC Tile Configuration

Address: 0x400F4372

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.740 UDB_DSI3_HC115

DSI HC Tile Configuration

Address: 0x400F4373

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.741 UDB_DSI3_HC116

DSI HC Tile Configuration

Address: 0x400F4374

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.742 UDB_DSI3_HC117

DSI HC Tile Configuration

Address: 0x400F4375

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.743 UDB_DSI3_HC118

DSI HC Tile Configuration

Address: 0x400F4376

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.744 UDB_DSI3_HC119

DSI HC Tile Configuration

Address: 0x400F4377

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.745 UDB_DSI3_HC120

DSI HC Tile Configuration

Address: 0x400F4378

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.746 UDB_DSI3_HC121

DSI HC Tile Configuration

Address: 0x400F4379

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.747 UDB_DSI3_HC122

DSI HC Tile Configuration

Address: 0x400F437A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.748 UDB_DSI3_HC123

DSI HC Tile Configuration

Address: 0x400F437B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.749 UDB_DSI3_HC124

DSI HC Tile Configuration

Address: 0x400F437C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.750 UDB_DSI3_HC125

DSI HC Tile Configuration

Address: 0x400F437D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.751 UDB_DSI3_HC126

DSI HC Tile Configuration

Address: 0x400F437E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.752 UDB_DSI3_HC127

DSI HC Tile Configuration

Address: 0x400F437F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.753 UDB_DSI3_HV_L0

DSI HV Tile Configuration; Left

Address: 0x400F4380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.754 UDB_DSI3_HV_L1

DSI HV Tile Configuration; Left

Address: 0x400F4381

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.755 UDB_DSI3_HV_L2

DSI HV Tile Configuration; Left

Address: 0x400F4382

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.756 UDB_DSI3_HV_L3

DSI HV Tile Configuration; Left

Address: 0x400F4383

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.757 UDB_DSI3_HV_L4

DSI HV Tile Configuration; Left

Address: 0x400F4384

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.758 UDB_DSI3_HV_L5

DSI HV Tile Configuration; Left

Address: 0x400F4385

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.759 UDB_DSI3_HV_L6

DSI HV Tile Configuration; Left

Address: 0x400F4386

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.760 UDB_DSI3_HV_L7

DSI HV Tile Configuration; Left

Address: 0x400F4387

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.761 UDB_DSI3_HV_L8

DSI HV Tile Configuration; Left

Address: 0x400F4388

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.762 UDB_DSI3_HV_L9

DSI HV Tile Configuration; Left

Address: 0x400F4389

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.763 UDB_DSI3_HV_L10

DSI HV Tile Configuration; Left

Address: 0x400F438A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.764 UDB_DSI3_HV_L11

DSI HV Tile Configuration; Left

Address: 0x400F438B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.765 UDB_DSI3_HV_L12

DSI HV Tile Configuration; Left

Address: 0x400F438C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.766 UDB_DSI3_HV_L13

DSI HV Tile Configuration; Left

Address: 0x400F438D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.767 UDB_DSI3_HV_L14

DSI HV Tile Configuration; Left

Address: 0x400F438E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.768 UDB_DSI3_HV_L15

DSI HV Tile Configuration; Left

Address: 0x400F438F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.769 UDB_DSI3_HS0

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4390

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.770 UDB_DSI3_HS1

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4391

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.771 UDB_DSI3_HS2

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4392

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.772 UDB_DSI3_HS3

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4393

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.773 UDB_DSI3_HS4

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4394

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.774 UDB_DSI3_HS5

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4395

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.775 UDB_DSI3_HS6

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4396

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.776 UDB_DSI3_HS7

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4397

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.777 UDB_DSI3_HS8

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4398

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.778 UDB_DSI3_HS9

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4399

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.779 UDB_DSI3_HS10

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F439A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.780 UDB_DSI3_HS11

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F439B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.781 UDB_DSI3_HS12

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F439C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.782 UDB_DSI3_HS13

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F439D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.783 UDB_DSI3_HS14

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F439E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.784 UDB_DSI3_HS15

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F439F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.785 UDB_DSI3_HS16

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F43A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.786 UDB_DSI3_HS17

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F43A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.787 UDB_DSI3_HS18

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F43A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.788 UDB_DSI3_HS19

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F43A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.789 UDB_DSI3_HS20

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F43A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.790 UDB_DSI3_HS21

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F43A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.791 UDB_DSI3_HS22

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F43A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.792 UDB_DSI3_HS23

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F43A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.793 UDB_DSI3_HV_R0

DSI HV Tile Configuration; Right

Address: 0x400F43A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.794 UDB_DSI3_HV_R1

DSI HV Tile Configuration; Right

Address: 0x400F43A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.795 UDB_DSI3_HV_R2

DSI HV Tile Configuration; Right

Address: 0x400F43AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.796 UDB_DSI3_HV_R3

DSI HV Tile Configuration; Right

Address: 0x400F43AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.797 UDB_DSI3_HV_R4

DSI HV Tile Configuration; Right

Address: 0x400F43AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.798 UDB_DSI3_HV_R5

DSI HV Tile Configuration; Right

Address: 0x400F43AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.799 UDB_DSI3_HV_R6

DSI HV Tile Configuration; Right

Address: 0x400F43AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.800 UDB_DSI3_HV_R7

DSI HV Tile Configuration; Right

Address: 0x400F43AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.801 UDB_DSI3_HV_R8

DSI HV Tile Configuration; Right

Address: 0x400F43B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.802 UDB_DSI3_HV_R9

DSI HV Tile Configuration; Right

Address: 0x400F43B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.803 UDB_DSI3_HV_R10

DSI HV Tile Configuration; Right

Address: 0x400F43B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.804 UDB_DSI3_HV_R11

DSI HV Tile Configuration; Right

Address: 0x400F43B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.805 UDB_DSI3_HV_R12

DSI HV Tile Configuration; Right

Address: 0x400F43B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.806 UDB_DSI3_HV_R13

DSI HV Tile Configuration; Right

Address: 0x400F43B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.807 UDB_DSI3_HV_R14

DSI HV Tile Configuration; Right

Address: 0x400F43B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.808 UDB_DSI3_HV_R15

DSI HV Tile Configuration; Right

Address: 0x400F43B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

14.1.809 UDB_DSI3_DSIINP0

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F43C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.810 UDB_DSI3_DSIINP1

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F43C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.811 UDB_DSI3_DSIINP2

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F43C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.812 UDB_DSI3_DSIINP3

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F43C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.813 UDB_DSI3_DSIINP4

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F43C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.814 UDB_DSI3_DSIINP5

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F43CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.815 UDB_DSI3_DSIOUTP0

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F43CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.816 UDB_DSI3_DSIOUTP1

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F43CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.817 UDB_DSI3_DSIOUTP2

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F43D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.818 UDB_DSI3_DSIOUTP3

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F43D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.819 UDB_DSI3_DSIOUTT0

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F43D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.820 UDB_DSI3_DSIOUTT1

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F43D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.821 UDB_DSI3_DSIOUTT2

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F43D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.822 UDB_DSI3_DSIOUTT3

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F43DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.823 UDB_DSI3_DSIOUTT4

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F43DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.824 UDB_DSI3_DSIOUTT5

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F43DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

14.1.825 UDB_DSI3_VS0

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F43E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.826 UDB_DSI3_VS1

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F43E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.827 UDB_DSI3_VS2

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F43E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.828 UDB_DSI3_VS3

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F43E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.829 UDB_DSI3_VS4

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F43E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.830 UDB_DSI3_VS5

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F43EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.831 UDB_DSI3_VS6

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F43EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

14.1.832 UDB_DSI3_VS7

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F43EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

15 GPIO Registers

This section discusses the GPIO registers. It lists all the registers in mapping tables, in address order.

15.1 Register Details

Register Name	Address
GPIO_INTR_CAUSE	0x40041000

15.1.1 GPIO_INTR_CAUSE

Interrupt port cause register

Address: 0x40041000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PORT_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PORT_INT	Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects "gpio_interrupts[i]" for IO port i). The register is used when the system uses a shared/combined interrupt line "gpio_interrupt". The SW ISR reads the register to determine which IO port(s) is responsible for the shared/combined interrupt line "gpio_interrupt". Once, the IO port(s) is determined, the IO port's INTR register is read to determine the IO pad(s) in the IO port that caused the interrupt. Default Value: 0

16 GPIO Port Registers

This section discusses the GPIO Port registers. It lists all the registers in mapping tables, in address order.

16.1 Register Details

Register Name	Address
GPIO_PRT0_PS	0x40040000
GPIO_PRT0_PS	0x40040004
GPIO_PRT0_PC	0x40040008
GPIO_PRT0_INTR_CFG	0x4004000C
GPIO_PRT0_INTR	0x40040010
GPIO_PRT0_PC2	0x40040018
GPIO_PRT0_DR_SET	0x40040040
GPIO_PRT0_DR_CLR	0x40040044
GPIO_PRT0_DR_INV	0x40040048
GPIO_PRT1_DR	0x40040100
GPIO_PRT1_PS	0x40040104
GPIO_PRT1_PC	0x40040108
GPIO_PRT1_INTR_CFG	0x4004010C
GPIO_PRT1_INTR	0x40040110
GPIO_PRT1_PC2	0x40040118
GPIO_PRT1_DR_SET	0x40040140
GPIO_PRT1_DR_CLR	0x40040144
GPIO_PRT1_DR_INV	0x40040148
GPIO_PRT2_DR	0x40040200
GPIO_PRT2_PS	0x40040204
GPIO_PRT2_PC	0x40040208
GPIO_PRT2_INTR_CFG	0x4004020C
GPIO_PRT2_INTR	0x40040210
GPIO_PRT2_PC2	0x40040218
GPIO_PRT2_DR_SET	0x40040240
GPIO_PRT2_DR_CLR	0x40040244
GPIO_PRT2_DR_INV	0x40040248

Register Name	Address
GPIO_PRT3_DR	0x40040300
GPIO_PRT3_PS	0x40040304
GPIO_PRT3_PC	0x40040308
GPIO_PRT3_INTR_CFG	0x4004030C
GPIO_PRT3_INTR	0x40040310
GPIO_PRT3_PC2	0x40040318
GPIO_PRT3_DR_SET	0x40040340
GPIO_PRT3_DR_CLR	0x40040344
GPIO_PRT3_DR_INV	0x40040348
GPIO_PRT4_DR	0x40040400
GPIO_PRT4_PS	0x40040404
GPIO_PRT4_PC	0x40040408
GPIO_PRT4_INTR_CFG	0x4004040C
GPIO_PRT4_INTR	0x40040410
GPIO_PRT4_PC2	0x40040418
GPIO_PRT4_DR_SET	0x40040440
GPIO_PRT4_DR_CLR	0x40040444
GPIO_PRT4_DR_INV	0x40040448
GPIO_PRT5_DR	0x40040500
GPIO_PRT5_PS	0x40040504
GPIO_PRT5_PC	0x40040508
GPIO_PRT5_INTR_CFG	0x4004050C
GPIO_PRT5_INTR	0x40040510
GPIO_PRT5_PC2	0x40040518
GPIO_PRT5_DR_SET	0x40040540
GPIO_PRT5_DR_CLR	0x40040544
GPIO_PRT5_DR_INV	0x40040548
GPIO_PRT6_DR	0x40040600
GPIO_PRT6_PS	0x40040604
GPIO_PRT6_PC	0x40040608
GPIO_PRT6_INTR_CFG	0x4004060C
GPIO_PRT6_INTR	0x40040610
GPIO_PRT6_PC2	0x40040618
GPIO_PRT6_DR_SET	0x40040640
GPIO_PRT6_DR_CLR	0x40040644
GPIO_PRT6_DR_INV	0x40040648
GPIO_PRT7_DR	0x40040700
GPIO_PRT7_PS	0x40040704
GPIO_PRT7_PC	0x40040708
GPIO_PRT7_INTR_CFG	0x4004070C
GPIO_PRT7_INTR	0x40040710
GPIO_PRT7_PC2	0x40040718

Register Name	Address
GPIO_PRT7_DR_SET	0x40040740
GPIO_PRT7_DR_CLR	0x40040744
GPIO_PRT7_DR_INV	0x40040748

16.1.1 GPIO_PRT0_DR

Port output data register

Address: 0x40040000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	Pin 7 output data. Default Value: 0
6	DATA6	Pin 6 output data. Default Value: 0
5	DATA5	Pin 5 output data. Default Value: 0
4	DATA4	Pin 4 output data. Default Value: 0
3	DATA3	Pin 3 output data. Default Value: 0
2	DATA2	Pin 2 output data. Default Value: 0
1	DATA1	Pin 1 output data. Default Value: 0
0	DATA0	Pin 0 output data. Default Value: 0

16.1.2 GPIO_PRT0_PS

Port GPIO state register

Address: 0x40040004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	Pin 7 state. Default Value: 0
6	DATA6	Pin 6 state. Default Value: 0
5	DATA5	Pin 5 state. Default Value: 0
4	DATA4	Pin 4 state. Default Value: 0
3	DATA3	Pin 3 state. Default Value: 0
2	DATA2	Pin 2 state. Default Value: 0
1	DATA1	Pin 1 state. Default Value: 0

16.1.2 GPIO_PRT0_PS (continued)

0	DATA0	Pin 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

16.1.3 GPIO_PRT0_PC

Port configuration register

Address: 0x40040008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for Pin 7. Default Value: 0

16.1.3 GPIO_PRT0_PC (continued)

20 : 18	DM6	The GPIO drive mode for Pin 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for Pin 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for Pin 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for Pin 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for Pin 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for Pin 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for Pin 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

16.1.4 GPIO_PRT0_INTR_CFG

Port interrupt configuration register

Address: 0x4004000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Edge selection for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for Pin 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for Pin 6. Default Value: 0

16.1.4 GPIO_PRT0_INTR_CFG (continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for Pin 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for Pin 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for Pin 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for Pin 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for Pin 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for Pin 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

16.1.5 GPIO_PRT0_INTR

Port interrupt status register

Address: 0x40040010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

16.1.5 GPIO_PRT0_INTR (continued)

7	DATA7	Interrupt pending on Pin 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on Pin 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on Pin 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on Pin 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on Pin 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on Pin 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on Pin 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on Pin 0. Firmware writes 1 to clear the interrupt. Default Value: 0

16.1.6 GPIO_PRT0_PC2

Port configuration register 2

Address: 0x40040018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for Pin 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for Pin 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for Pin 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for Pin 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for Pin 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for Pin 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for Pin 1. Default Value: 0

16.1.6 GPIO_PRT0_PC2 (continued)

0	INP_DIS0	Disables the input buffer for Pin 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

16.1.7 GPIO_PRT0_DR_SET

Port output data set register

Address: 0x40040040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

16.1.8 GPIO_PRT0_DR_CLR

Port output data clear register

Address: 0x40040044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

16.1.9 GPIO_PRT0_DR_INV

Port output data invert register

Address: 0x40040048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

16.1.10 GPIO_PRT1_DR

Port output data register

Address: 0x40040100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	Pin 7 output data. Default Value: 0
6	DATA6	Pin 6 output data. Default Value: 0
5	DATA5	Pin 5 output data. Default Value: 0
4	DATA4	Pin 4 output data. Default Value: 0
3	DATA3	Pin 3 output data. Default Value: 0
2	DATA2	Pin 2 output data. Default Value: 0
1	DATA1	Pin 1 output data. Default Value: 0
0	DATA0	Pin 0 output data. Default Value: 0

16.1.11 GPIO_PRT1_PS

Port GPIO state register

Address: 0x40040104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	Pin 7 state. Default Value: 0
6	DATA6	Pin 6 state. Default Value: 0
5	DATA5	Pin 5 state. Default Value: 0
4	DATA4	Pin 4 state. Default Value: 0
3	DATA3	Pin 3 state. Default Value: 0
2	DATA2	Pin 2 state. Default Value: 0
1	DATA1	Pin 1 state. Default Value: 0

16.1.11 GPIO_PRT1_PS (continued)

0	DATA0	Pin 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

16.1.12 GPIO_PRT1_PC

Port configuration register

Address: 0x40040108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for Pin 7. Default Value: 0

16.1.12 GPIO_PRT1_PC (continued)

20 : 18	DM6	The GPIO drive mode for Pin 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for Pin 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for Pin 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for Pin 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for Pin 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for Pin 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for Pin 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

16.1.13 GPIO_PRT1_INTR_CFG

Port interrupt configuration register

Address: 0x4004010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Edge selection for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for Pin 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for Pin 6. Default Value: 0

16.1.13 GPIO_PRT1_INTR_CFG (continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for Pin 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for Pin 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for Pin 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for Pin 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for Pin 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for Pin 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

16.1.14 GPIO_PRT1_INTR

Port interrupt status register

Address: 0x40040110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

16.1.14 GPIO_PRT1_INTR (continued)

7	DATA7	Interrupt pending on Pin 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on Pin 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on Pin 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on Pin 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on Pin 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on Pin 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on Pin 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on Pin 0. Firmware writes 1 to clear the interrupt. Default Value: 0

16.1.15 GPIO_PRT1_PC2

Port configuration register 2

Address: 0x40040118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for Pin 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for Pin 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for Pin 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for Pin 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for Pin 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for Pin 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for Pin 1. Default Value: 0

16.1.15 GPIO_PRT1_PC2 (continued)

0	INP_DIS0	Disables the input buffer for Pin 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

16.1.16 GPIO_PRT1_DR_SET

Port output data set register

Address: 0x40040140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

16.1.17 GPIO_PRT1_DR_CLR

Port output data clear register

Address: 0x40040144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

16.1.18 GPIO_PRT1_DR_INV

Port output data invert register

Address: 0x40040148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

16.1.19 GPIO_PRT2_DR

Port output data register

Address: 0x40040200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	Pin 7 output data. Default Value: 0
6	DATA6	Pin 6 output data. Default Value: 0
5	DATA5	Pin 5 output data. Default Value: 0
4	DATA4	Pin 4 output data. Default Value: 0
3	DATA3	Pin 3 output data. Default Value: 0
2	DATA2	Pin 2 output data. Default Value: 0
1	DATA1	Pin 1 output data. Default Value: 0
0	DATA0	Pin 0 output data. Default Value: 0

16.1.20 GPIO_PRT2_PS

Port GPIO state register

Address: 0x40040204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	Pin 7 state. Default Value: 0
6	DATA6	Pin 6 state. Default Value: 0
5	DATA5	Pin 5 state. Default Value: 0
4	DATA4	Pin 4 state. Default Value: 0
3	DATA3	Pin 3 state. Default Value: 0
2	DATA2	Pin 2 state. Default Value: 0
1	DATA1	Pin 1 state. Default Value: 0

16.1.20 GPIO_PRT2_PS (continued)

0	DATA0	Pin 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

16.1.21 GPIO_PRT2_PC

Port configuration register

Address: 0x40040208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for Pin 7. Default Value: 0

16.1.21 GPIO_PRT2_PC (continued)

20 : 18	DM6	The GPIO drive mode for Pin 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for Pin 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for Pin 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for Pin 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for Pin 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for Pin 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for Pin 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

16.1.22 GPIO_PRT2_INTR_CFG

Port interrupt configuration register

Address: 0x4004020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Edge selection for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for Pin 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for Pin 6. Default Value: 0

16.1.22 GPIO_PRT2_INTR_CFG (continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for Pin 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for Pin 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for Pin 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for Pin 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for Pin 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for Pin 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

16.1.23 GPIO_PRT2_INTR

Port interrupt status register

Address: 0x40040210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

16.1.23 GPIO_PRT2_INTR (continued)

7	DATA7	Interrupt pending on Pin 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on Pin 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on Pin 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on Pin 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on Pin 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on Pin 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on Pin 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on Pin 0. Firmware writes 1 to clear the interrupt. Default Value: 0

16.1.24 GPIO_PRT2_PC2

Port configuration register 2

Address: 0x40040218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for Pin 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for Pin 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for Pin 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for Pin 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for Pin 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for Pin 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for Pin 1. Default Value: 0

16.1.24 GPIO_PRT2_PC2 (continued)

0	INP_DIS0	Disables the input buffer for Pin 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

16.1.25 GPIO_PRT2_DR_SET

Port output data set register

Address: 0x40040240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

16.1.26 GPIO_PRT2_DR_CLR

Port output data clear register

Address: 0x40040244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

16.1.27 GPIO_PRT2_DR_INV

Port output data invert register

Address: 0x40040248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

16.1.28 GPIO_PRT3_DR

Port output data register

Address: 0x40040300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	Pin 7 output data. Default Value: 0
6	DATA6	Pin 6 output data. Default Value: 0
5	DATA5	Pin 5 output data. Default Value: 0
4	DATA4	Pin 4 output data. Default Value: 0
3	DATA3	Pin 3 output data. Default Value: 0
2	DATA2	Pin 2 output data. Default Value: 0
1	DATA1	Pin 1 output data. Default Value: 0
0	DATA0	Pin 0 output data. Default Value: 0

16.1.29 GPIO_PRT3_PS

Port GPIO state register

Address: 0x40040304

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	Pin 7 state. Default Value: 0
6	DATA6	Pin 6 state. Default Value: 0
5	DATA5	Pin 5 state. Default Value: 0
4	DATA4	Pin 4 state. Default Value: 0
3	DATA3	Pin 3 state. Default Value: 0
2	DATA2	Pin 2 state. Default Value: 0
1	DATA1	Pin 1 state. Default Value: 0

16.1.29 GPIO_PRT3_PS (continued)

0	DATA0	Pin 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

16.1.30 GPIO_PRT3_PC

Port configuration register

Address: 0x40040308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for Pin 7. Default Value: 0

16.1.30 GPIO_PRT3_PC (continued)

20 : 18	DM6	The GPIO drive mode for Pin 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for Pin 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for Pin 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for Pin 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for Pin 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for Pin 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for Pin 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

16.1.31 GPIO_PRT3_INTR_CFG

Port interrupt configuration register

Address: 0x4004030C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Edge selection for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for Pin 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for Pin 6. Default Value: 0

16.1.31 GPIO_PRT3_INTR_CFG (continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for Pin 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for Pin 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for Pin 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for Pin 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for Pin 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for Pin 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

16.1.32 GPIO_PRT3_INTR

Port interrupt status register

Address: 0x40040310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

16.1.32 GPIO_PRT3_INTR (continued)

7	DATA7	Interrupt pending on Pin 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on Pin 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on Pin 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on Pin 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on Pin 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on Pin 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on Pin 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on Pin 0. Firmware writes 1 to clear the interrupt. Default Value: 0

16.1.33 GPIO_PRT3_PC2

Port configuration register 2

Address: 0x40040318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for Pin 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for Pin 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for Pin 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for Pin 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for Pin 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for Pin 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for Pin 1. Default Value: 0

16.1.33 GPIO_PRT3_PC2 (continued)

0	INP_DIS0	Disables the input buffer for Pin 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

16.1.34 GPIO_PRT3_DR_SET

Port output data set register

Address: 0x40040340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

16.1.35 GPIO_PRT3_DR_CLR

Port output data clear register

Address: 0x40040344

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

16.1.36 GPIO_PRT3_DR_INV

Port output data invert register

Address: 0x40040348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

16.1.37 GPIO_PRT4_DR

Port output data register

Address: 0x40040400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	Pin 7 output data. Default Value: 0
6	DATA6	Pin 6 output data. Default Value: 0
5	DATA5	Pin 5 output data. Default Value: 0
4	DATA4	Pin 4 output data. Default Value: 0
3	DATA3	Pin 3 output data. Default Value: 0
2	DATA2	Pin 2 output data. Default Value: 0
1	DATA1	Pin 1 output data. Default Value: 0
0	DATA0	Pin 0 output data. Default Value: 0

16.1.38 GPIO_PRT4_PS

Port GPIO state register

Address: 0x40040404

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	Pin 7 state. Default Value: 0
6	DATA6	Pin 6 state. Default Value: 0
5	DATA5	Pin 5 state. Default Value: 0
4	DATA4	Pin 4 state. Default Value: 0
3	DATA3	Pin 3 state. Default Value: 0
2	DATA2	Pin 2 state. Default Value: 0
1	DATA1	Pin 1 state. Default Value: 0

16.1.38 GPIO_PRT4_PS (continued)

0	DATA0	Pin 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

16.1.39 GPIO_PRT4_PC

Port configuration register

Address: 0x40040408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for Pin 7. Default Value: 0

16.1.39 GPIO_PRT4_PC (continued)

20 : 18	DM6	The GPIO drive mode for Pin 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for Pin 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for Pin 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for Pin 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for Pin 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for Pin 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for Pin 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

16.1.40 GPIO_PRT4_INTR_CFG

Port interrupt configuration register

Address: 0x4004040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Edge selection for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for Pin 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for Pin 6. Default Value: 0

16.1.40 GPIO_PRT4_INTR_CFG (continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for Pin 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for Pin 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for Pin 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for Pin 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for Pin 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for Pin 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

16.1.41 GPIO_PRT4_INTR

Port interrupt status register

Address: 0x40040410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

16.1.41 GPIO_PRT4_INTR (continued)

7	DATA7	Interrupt pending on Pin 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on Pin 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on Pin 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on Pin 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on Pin 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on Pin 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on Pin 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on Pin 0. Firmware writes 1 to clear the interrupt. Default Value: 0

16.1.42 GPIO_PRT4_PC2

Port configuration register 2

Address: 0x40040418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for Pin 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for Pin 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for Pin 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for Pin 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for Pin 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for Pin 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for Pin 1. Default Value: 0

16.1.42 GPIO_PRT4_PC2 (continued)

0	INP_DIS0	Disables the input buffer for Pin 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

16.1.43 GPIO_PRT4_DR_SET

Port output data set register

Address: 0x40040440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

16.1.44 GPIO_PRT4_DR_CLR

Port output data clear register

Address: 0x40040444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

16.1.45 GPIO_PRT4_DR_INV

Port output data invert register

Address: 0x40040448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

16.1.46 GPIO_PRT5_DR

Port output data register

Address: 0x40040500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	Pin 7 output data. Default Value: 0
6	DATA6	Pin 6 output data. Default Value: 0
5	DATA5	Pin 5 output data. Default Value: 0
4	DATA4	Pin 4 output data. Default Value: 0
3	DATA3	Pin 3 output data. Default Value: 0
2	DATA2	Pin 2 output data. Default Value: 0
1	DATA1	Pin 1 output data. Default Value: 0
0	DATA0	Pin 0 output data. Default Value: 0

16.1.47 GPIO_PRT5_PS

Port GPIO state register

Address: 0x40040504

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	Pin 7 state. Default Value: 0
6	DATA6	Pin 6 state. Default Value: 0
5	DATA5	Pin 5 state. Default Value: 0
4	DATA4	Pin 4 state. Default Value: 0
3	DATA3	Pin 3 state. Default Value: 0
2	DATA2	Pin 2 state. Default Value: 0
1	DATA1	Pin 1 state. Default Value: 0

16.1.47 GPIO_PRT5_PS (continued)

0	DATA0	Pin 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

16.1.48 GPIO_PRT5_PC

Port configuration register

Address: 0x40040508

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for Pin 7. Default Value: 0

16.1.48 GPIO_PRT5_PC (continued)

20 : 18	DM6	The GPIO drive mode for Pin 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for Pin 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for Pin 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for Pin 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for Pin 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for Pin 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for Pin 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

16.1.49 GPIO_PRT5_INTR_CFG

Port interrupt configuration register

Address: 0x4004050C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Edge selection for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for Pin 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for Pin 6. Default Value: 0

16.1.49 GPIO_PRT5_INTR_CFG (continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for Pin 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for Pin 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for Pin 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for Pin 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for Pin 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for Pin 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

16.1.50 GPIO_PRT5_INTR

Port interrupt status register

Address: 0x40040510

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

16.1.50 GPIO_PRT5_INTR (continued)

7	DATA7	Interrupt pending on Pin 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on Pin 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on Pin 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on Pin 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on Pin 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on Pin 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on Pin 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on Pin 0. Firmware writes 1 to clear the interrupt. Default Value: 0

16.1.51 GPIO_PRT5_PC2

Port configuration register 2

Address: 0x40040518

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for Pin 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for Pin 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for Pin 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for Pin 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for Pin 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for Pin 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for Pin 1. Default Value: 0

16.1.51 GPIO_PRT5_PC2 (continued)

0	INP_DIS0	Disables the input buffer for Pin 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

16.1.52 GPIO_PRT5_DR_SET

Port output data set register

Address: 0x40040540

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

16.1.53 GPIO_PRT5_DR_CLR

Port output data clear register

Address: 0x40040544

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

16.1.54 GPIO_PRT5_DR_INV

Port output data invert register

Address: 0x40040548

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

16.1.55 GPIO_PRT6_DR

Port output data register

Address: 0x40040600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	DATA5	Pin 5 output data. Default Value: 0
4	DATA4	Pin 4 output data. Default Value: 0
3	DATA3	Pin 3 output data. Default Value: 0
2	DATA2	Pin 2 output data. Default Value: 0
1	DATA1	Pin 1 output data. Default Value: 0
0	DATA0	Pin 0 output data. Default Value: 0

16.1.56 GPIO_PRT6_PS

Port GPIO state register

Address: 0x40040604

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
5	DATA5	Pin 5 state. Default Value: 0
4	DATA4	Pin 4 state. Default Value: 0
3	DATA3	Pin 3 state. Default Value: 0
2	DATA2	Pin 2 state. Default Value: 0
1	DATA1	Pin 1 state. Default Value: 0

16.1.56 GPIO_PRT6_PS (continued)

0	DATA0	Pin 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

16.1.57 GPIO_PRT6_PC

Port configuration register

Address: 0x40040608

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW			
HW Access	R		R		R			
Name	DM2 [7:6]		DM1 [5:3]		DM0 [2:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW	None	RW	RW
HW Access	R		R		R	None	R	R
Name	PORT_IB_MODE_SEL [31:30]		PORT_SLEW_CTL [29:28]		PORT_HYST_TRIM	None	PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. Default Value: 0
29 : 28	PORT_SLEW_CTL	Slew control. Only used in the O_Z drive mode (mode 4: strong pull down, open drain): This field is intended for I2C functionality. Default Value: 0
27	PORT_HYST_TRIM	This field is used to improve the hysteresis (to 10% of vddio) of the selectable trip point input buffer. The voltage reference comes from the VREFGEN block and is only available when using the VREFGEN block: '0': <= 2.2 V input signaling Voltage. '1': > 2.2 V input signaling Voltage. Default Value: 0

16.1.57 GPIO_PRT6_PC (continued)

25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
17 : 15	DM5	The GPIO drive mode for Pin 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for Pin 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for Pin 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for Pin 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for Pin 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for Pin 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

16.1.58 GPIO_PRT6_INTR_CFG

Port interrupt configuration register

Address: 0x4004060C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [15:12]				EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Edge selection for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for Pin 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for Pin 4. Default Value: 0

16.1.58 GPIO_PRT6_INTR_CFG (continued)

7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for Pin 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for Pin 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for Pin 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for Pin 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

16.1.59 GPIO_PRT6_INTR

Port interrupt status register

Address: 0x40040610

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		A	A	A	A	A	A
Name	None [7:6]		DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [23:22]		PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
5	DATA5	Interrupt pending on Pin 5. Firmware writes 1 to clear the interrupt. Default Value: 0

16.1.59 GPIO_PRT6_INTR (continued)

4	DATA4	Interrupt pending on Pin 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on Pin 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on Pin 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on Pin 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on Pin 0. Firmware writes 1 to clear the interrupt. Default Value: 0

16.1.60 GPIO_PRT6_PC2

Port configuration register 2

Address: 0x40040618

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	INP_DIS5	Disables the input buffer for Pin 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for Pin 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for Pin 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for Pin 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for Pin 1. Default Value: 0
0	INP_DIS0	Disables the input buffer for Pin 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

16.1.61 GPIO_PRT6_DR_SET

Port output data set register

Address: 0x40040640

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

16.1.62 GPIO_PRT6_DR_CLR

Port output data clear register

Address: 0x40040644

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

16.1.63 GPIO_PRT6_DR_INV

Port output data invert register

Address: 0x40040648

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

16.1.64 GPIO_PRT7_DR

Port output data register

Address: 0x40040700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					RW	RW	RW
Name	None [7:3]					DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	DATA2	Pin 2 output data. Default Value: 0
1	DATA1	Pin 1 output data. Default Value: 0
0	DATA0	Pin 0 output data. Default Value: 0

16.1.65 GPIO_PRT7_PS

Port GPIO state register

Address: 0x40040704

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
2	DATA2	Pin 2 state. Default Value: 0
1	DATA1	Pin 1 state. Default Value: 0
0	DATA0	Pin 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

16.1.66 GPIO_PRT7_PC

Port configuration register

Address: 0x40040708

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							DM2

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
8 : 6	DM2	The GPIO drive mode for Pin 2. Default Value: 0

16.1.66 GPIO_PRT7_PC (continued)

5 : 3	DM1	The GPIO drive mode for Pin 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for Pin 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

16.1.67 GPIO_PRT7_INTR_CFG

Port interrupt configuration register

Address: 0x4004070C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Edge selection for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for Pin 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for Pin 1. Default Value: 0

16.1.67 GPIO_PRT7_INTR_CFG (continued)

1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for Pin 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

16.1.68 GPIO_PRT7_INTR

Port interrupt status register

Address: 0x40040710

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					A	A	A
Name	None [7:3]					DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [23:19]					PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
2	DATA2	Interrupt pending on Pin 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on Pin 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on Pin 0. Firmware writes 1 to clear the interrupt. Default Value: 0

16.1.69 GPIO_PRT7_PC2

Port configuration register 2

Address: 0x40040718

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	INP_DIS2	Disables the input buffer for Pin 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for Pin 1. Default Value: 0
0	INP_DIS0	Disables the input buffer for Pin 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

16.1.70 GPIO_PRT7_DR_SET

Port output data set register

Address: 0x40040740

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

16.1.71 GPIO_PRT7_DR_CLR

Port output data clear register

Address: 0x40040744

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

16.1.72 GPIO_PRT7_DR_INV

Port output data invert register

Address: 0x40040748

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Pin i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

17 High Speed IO Matrix (HSIOM) Registers

This section discusses the HSIOM registers. It lists all the registers in mapping tables, in address order.

17.1 Register Details

Register Name	Address
HSIOM_AMUX_SPLIT_CTL0	0x40022100
HSIOM_AMUX_SPLIT_CTL1	0x40022104

17.1.1 HSIOM_AMUX_SPLIT_CTL0

AMUX splitter cell control

Address: 0x40022100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	SWITCH_BB_S0	SWITCH_BB_SR	SWITCH_BB_SL	None	SWITCH_AA_S0	SWITCH_AA_SR	SWITCH_AA_SL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	SWITCH_BB_S0	T-switch control for AMUXBUSB vssa/ground switch. Default Value: 0
5	SWITCH_BB_SR	T-switch control for Right AMUXBUSB switch. Default Value: 0
4	SWITCH_BB_SL	T-switch control for Left AMUXBUSB switch. Default Value: 0
2	SWITCH_AA_S0	T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed. Default Value: 0
1	SWITCH_AA_SR	T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

17.1.1 HSIOM_AMUX_SPLIT_CTL0 (continued)

0	SWITCH_AA_SL	T-switch control for Left AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

17.1.2 HSIOM_AMUX_SPLIT_CTL1

AMUX splitter cell control

Address: 0x40022104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	SWITCH_BB_S0	SWITCH_BB_SR	SWITCH_BB_SL	None	SWITCH_AA_S0	SWITCH_AA_SR	SWITCH_AA_SL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	SWITCH_BB_S0	T-switch control for AMUXBUSB vssa/ground switch. Default Value: 0
5	SWITCH_BB_SR	T-switch control for Right AMUXBUSB switch. Default Value: 0
4	SWITCH_BB_SL	T-switch control for Left AMUXBUSB switch. Default Value: 0
2	SWITCH_AA_S0	T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed. Default Value: 0
1	SWITCH_AA_SR	T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

17.1.2 HSIOM_AMUX_SPLIT_CTL1 (continued)

0	SWITCH_AA_SL	T-switch control for Left AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

18 HSIOM Port Registers

This section discusses the HSIOM Port registers. It lists all the registers in mapping tables, in address order.

18.1 Register Details

Register Name	Address
HSIOM_PORT_SEL1	0x40020000
HSIOM_PORT_SEL1	0x40020100
HSIOM_PORT_SEL2	0x40020200
HSIOM_PORT_SEL3	0x40020300
HSIOM_PORT_SEL4	0x40020400
HSIOM_PORT_SEL5	0x40020500
HSIOM_PORT_SEL6	0x40020600
HSIOM_PORT_SEL7	0x40020700

18.1.1 HSIOM_PORT_SEL0

Port selection register

Address: 0x40020000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for Pin 7. Default Value: 0
27 : 24	IO6_SEL	Selects connection for Pin 6. Default Value: 0
23 : 20	IO5_SEL	Selects connection for Pin 5. Default Value: 0
19 : 16	IO4_SEL	Selects connection for Pin 4. Default Value: 0
15 : 12	IO3_SEL	Selects connection for Pin 3. Default Value: 0
11 : 8	IO2_SEL	Selects connection for Pin 2. Default Value: 0
7 : 4	IO1_SEL	Selects connection for Pin 1. Default Value: 0
3 : 0	IO0_SEL	Selects connection for Pin 0. Default Value: 0

18.1.1 HSIOM_PORT_SEL0 (continued)

Note that the availability of Active and Deep Sleep source depends on the pin. See the Pin Outs section of the device datasheet to know the functions available for each pin.

0x0: GPIO:
Pin is regular firmware-controlled I/O or connected to dedicated hardware block

0x1: GPIO_DSI:
Output is firmware controlled, but OE is controlled from DSI.

0x2: DSI_DSI:
Both output and OE are controlled from DSI.

0x3: DSI_GPIO:
Output is controlled from DSI, but OE is firmware controlled

0x4: CSD_SENSE:
Pin is a CSD sense pin (analog mode)

0x5: CSD_SHIELD:
Pin is a CSD shield pin (analog mode).

0x6: AMUXA:
Pin is connected to AMUXBUS-A.

0x7: AMUXB:
Pin is connected to AMUXBUS-B. This mode is also used for CSD I/O charging. When CSD I/O charging is enabled in CSD_CONTROL, digital I/O driver is connected to csd_charge signal (pin is still connected to AMUXBUS-B).

0x8: ACT_0:
Pin-specific Active source #0 (TCPWM, EXT CLOCK). See the device datasheet for details.

0x9: ACT_1:
Pin-specific Active source #1 (SCB-UART). See the device datasheet for details.

0xa: ACT_2:
Pin-specific Active source #2 (CAN)
See the device datasheet for details.

0xb: ACT_3:
Reserved

0xc: DS_0:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xe: DS_2:
Chip specific DeepSleep source 2 connection(SCB-I2C, TCPWM, SWD, LPComp, Wakeup). See the device datasheet for details.

0xf: DS_3:
Chip specific DeepSleep source 3 connection(SCB-SPI). See the device datasheet for details.

18.1.2 HSIOM_PORT_SEL1

Port selection register

Address: 0x40020100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for Pin 7. Default Value: 0
27 : 24	IO6_SEL	Selects connection for Pin 6. Default Value: 0
23 : 20	IO5_SEL	Selects connection for Pin 5. Default Value: 0
19 : 16	IO4_SEL	Selects connection for Pin 4. Default Value: 0
15 : 12	IO3_SEL	Selects connection for Pin 3. Default Value: 0
11 : 8	IO2_SEL	Selects connection for Pin 2. Default Value: 0
7 : 4	IO1_SEL	Selects connection for Pin 1. Default Value: 0
3 : 0	IO0_SEL	Selects connection for Pin 0. Default Value: 0

18.1.2 HSIOM_PORT_SEL1 (continued)

Note that the availability of Active and Deep Sleep source depends on the pin. See the Pin Outs section of the device datasheet to know the functions available for each pin.

0x0: GPIO:
Pin is regular firmware-controlled I/O or connected to dedicated hardware block

0x1: GPIO_DSI:
Output is firmware controlled, but OE is controlled from DSI.

0x2: DSI_DSI:
Both output and OE are controlled from DSI.

0x3: DSI_GPIO:
Output is controlled from DSI, but OE is firmware controlled

0x4: CSD_SENSE:
Pin is a CSD sense pin (analog mode)

0x5: CSD_SHIELD:
Pin is a CSD shield pin (analog mode).

0x6: AMUXA:
Pin is connected to AMUXBUS-A.

0x7: AMUXB:
Pin is connected to AMUXBUS-B. This mode is also used for CSD I/O charging. When CSD I/O charging is enabled in CSD_CONTROL, digital I/O driver is connected to csd_charge signal (pin is still connected to AMUXBUS-B).

0x8: ACT_0:
Pin-specific Active source #0 (TCPWM, EXT CLOCK). See the device datasheet for details.

0x9: ACT_1:
Pin-specific Active source #1 (SCB-UART). See the device datasheet for details.

0xa: ACT_2:
Pin-specific Active source #2 (CAN)
See the device datasheet for details.

0xb: ACT_3:
Reserved

0xc: DS_0:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xe: DS_2:
Chip specific DeepSleep source 2 connection(SCB-I2C, TCPWM, SWD, LPComp, Wakeup). See the device datasheet for details.

0xf: DS_3:
Chip specific DeepSleep source 3 connection(SCB-SPI). See the device datasheet for details.

18.1.3 HSIOM_PORT_SEL2

Port selection register

Address: 0x40020200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for Pin 7. Default Value: 0
27 : 24	IO6_SEL	Selects connection for Pin 6. Default Value: 0
23 : 20	IO5_SEL	Selects connection for Pin 5. Default Value: 0
19 : 16	IO4_SEL	Selects connection for Pin 4. Default Value: 0
15 : 12	IO3_SEL	Selects connection for Pin 3. Default Value: 0
11 : 8	IO2_SEL	Selects connection for Pin 2. Default Value: 0
7 : 4	IO1_SEL	Selects connection for Pin 1. Default Value: 0
3 : 0	IO0_SEL	Selects connection for Pin 0. Default Value: 0

18.1.3 HSIOM_PORT_SEL2 (continued)

Note that the availability of Active and Deep Sleep source depends on the pin. See the Pin Outs section of the device datasheet to know the functions available for each pin.

0x0: GPIO:
Pin is regular firmware-controlled I/O or connected to dedicated hardware block

0x1: GPIO_DSI:
Output is firmware controlled, but OE is controlled from DSI.

0x2: DSI_DSI:
Both output and OE are controlled from DSI.

0x3: DSI_GPIO:
Output is controlled from DSI, but OE is firmware controlled

0x4: CSD_SENSE:
Pin is a CSD sense pin (analog mode)

0x5: CSD_SHIELD:
Pin is a CSD shield pin (analog mode).

0x6: AMUXA:
Pin is connected to AMUXBUS-A.

0x7: AMUXB:
Pin is connected to AMUXBUS-B. This mode is also used for CSD I/O charging. When CSD I/O charging is enabled in CSD_CONTROL, digital I/O driver is connected to csd_charge signal (pin is still connected to AMUXBUS-B).

0x8: ACT_0:
Pin-specific Active source #0 (TCPWM, EXT CLOCK). See the device datasheet for details.

0x9: ACT_1:
Pin-specific Active source #1 (SCB-UART). See the device datasheet for details.

0xa: ACT_2:
Pin-specific Active source #2 (CAN)
See the device datasheet for details.

0xb: ACT_3:
Reserved

0xc: DS_0:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xe: DS_2:
Chip specific DeepSleep source 2 connection(SCB-I2C, TCPWM, SWD, LPComp, Wakeup). See the device datasheet for details.

0xf: DS_3:
Chip specific DeepSleep source 3 connection(SCB-SPI). See the device datasheet for details.

18.1.4 HSIOM_PORT_SEL3

Port selection register

Address: 0x40020300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for Pin 7. Default Value: 0
27 : 24	IO6_SEL	Selects connection for Pin 6. Default Value: 0
23 : 20	IO5_SEL	Selects connection for Pin 5. Default Value: 0
19 : 16	IO4_SEL	Selects connection for Pin 4. Default Value: 0
15 : 12	IO3_SEL	Selects connection for Pin 3. Default Value: 0
11 : 8	IO2_SEL	Selects connection for Pin 2. Default Value: 0
7 : 4	IO1_SEL	Selects connection for Pin 1. Default Value: 0
3 : 0	IO0_SEL	Selects connection for Pin 0. Default Value: 0

18.1.4 HSIOM_PORT_SEL3 (continued)

Note that the availability of Active and Deep Sleep source depends on the pin. See the Pin Outs section of the device datasheet to know the functions available for each pin.

0x0: GPIO:
Pin is regular firmware-controlled I/O or connected to dedicated hardware block

0x1: GPIO_DSI:
Output is firmware controlled, but OE is controlled from DSI.

0x2: DSI_DSI:
Both output and OE are controlled from DSI.

0x3: DSI_GPIO:
Output is controlled from DSI, but OE is firmware controlled

0x4: CSD_SENSE:
Pin is a CSD sense pin (analog mode)

0x5: CSD_SHIELD:
Pin is a CSD shield pin (analog mode).

0x6: AMUXA:
Pin is connected to AMUXBUS-A.

0x7: AMUXB:
Pin is connected to AMUXBUS-B. This mode is also used for CSD I/O charging. When CSD I/O charging is enabled in CSD_CONTROL, digital I/O driver is connected to csd_charge signal (pin is still connected to AMUXBUS-B).

0x8: ACT_0:
Pin-specific Active source #0 (TCPWM, EXT CLOCK). See the device datasheet for details.

0x9: ACT_1:
Pin-specific Active source #1 (SCB-UART). See the device datasheet for details.

0xa: ACT_2:
Pin-specific Active source #2 (CAN)
See the device datasheet for details.

0xb: ACT_3:
Reserved

0xc: DS_0:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xe: DS_2:
Chip specific DeepSleep source 2 connection(SCB-I2C, TCPWM, SWD, LPComp, Wakeup). See the device datasheet for details.

0xf: DS_3:
Chip specific DeepSleep source 3 connection(SCB-SPI). See the device datasheet for details.

18.1.5 HSIOM_PORT_SEL4

Port selection register

Address: 0x40020400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for Pin 7. Default Value: 0
27 : 24	IO6_SEL	Selects connection for Pin 6. Default Value: 0
23 : 20	IO5_SEL	Selects connection for Pin 5. Default Value: 0
19 : 16	IO4_SEL	Selects connection for Pin 4. Default Value: 0
15 : 12	IO3_SEL	Selects connection for Pin 3. Default Value: 0
11 : 8	IO2_SEL	Selects connection for Pin 2. Default Value: 0
7 : 4	IO1_SEL	Selects connection for Pin 1. Default Value: 0
3 : 0	IO0_SEL	Selects connection for Pin 0. Default Value: 0

18.1.5 HSIOM_PORT_SEL4 (continued)

Note that the availability of Active and Deep Sleep source depends on the pin. See the Pin Outs section of the device datasheet to know the functions available for each pin.

0x0: GPIO:
Pin is regular firmware-controlled I/O or connected to dedicated hardware block

0x1: GPIO_DSI:
Output is firmware controlled, but OE is controlled from DSI.

0x2: DSI_DSI:
Both output and OE are controlled from DSI.

0x3: DSI_GPIO:
Output is controlled from DSI, but OE is firmware controlled

0x4: CSD_SENSE:
Pin is a CSD sense pin (analog mode)

0x5: CSD_SHIELD:
Pin is a CSD shield pin (analog mode).

0x6: AMUXA:
Pin is connected to AMUXBUS-A.

0x7: AMUXB:
Pin is connected to AMUXBUS-B. This mode is also used for CSD I/O charging. When CSD I/O charging is enabled in CSD_CONTROL, digital I/O driver is connected to csd_charge signal (pin is still connected to AMUXBUS-B).

0x8: ACT_0:
Pin-specific Active source #0 (TCPWM, EXT CLOCK). See the device datasheet for details.

0x9: ACT_1:
Pin-specific Active source #1 (SCB-UART). See the device datasheet for details.

0xa: ACT_2:
Pin-specific Active source #2 (CAN)
See the device datasheet for details.

0xb: ACT_3:
Reserved

0xc: DS_0:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xe: DS_2:
Chip specific DeepSleep source 2 connection(SCB-I2C, TCPWM, SWD, LPComp, Wakeup). See the device datasheet for details.

0xf: DS_3:
Chip specific DeepSleep source 3 connection(SCB-SPI). See the device datasheet for details.

18.1.6 HSIOM_PORT_SEL5

Port selection register

Address: 0x40020500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for Pin 7. Default Value: 0
27 : 24	IO6_SEL	Selects connection for Pin 6. Default Value: 0
23 : 20	IO5_SEL	Selects connection for Pin 5. Default Value: 0
19 : 16	IO4_SEL	Selects connection for Pin 4. Default Value: 0
15 : 12	IO3_SEL	Selects connection for Pin 3. Default Value: 0
11 : 8	IO2_SEL	Selects connection for Pin 2. Default Value: 0
7 : 4	IO1_SEL	Selects connection for Pin 1. Default Value: 0
3 : 0	IO0_SEL	Selects connection for Pin 0. Default Value: 0

18.1.6 HSIOM_PORT_SEL5 (continued)

Note that the availability of Active and Deep Sleep source depends on the pin. See the Pin Outs section of the device datasheet to know the functions available for each pin.

0x0: GPIO:
Pin is regular firmware-controlled I/O or connected to dedicated hardware block

0x1: GPIO_DSI:
Output is firmware controlled, but OE is controlled from DSI.

0x2: DSI_DSI:
Both output and OE are controlled from DSI.

0x3: DSI_GPIO:
Output is controlled from DSI, but OE is firmware controlled

0x4: CSD_SENSE:
Pin is a CSD sense pin (analog mode)

0x5: CSD_SHIELD:
Pin is a CSD shield pin (analog mode).

0x6: AMUXA:
Pin is connected to AMUXBUS-A.

0x7: AMUXB:
Pin is connected to AMUXBUS-B. This mode is also used for CSD I/O charging. When CSD I/O charging is enabled in CSD_CONTROL, digital I/O driver is connected to csd_charge signal (pin is still connected to AMUXBUS-B).

0x8: ACT_0:
Pin-specific Active source #0 (TCPWM, EXT CLOCK). See the device datasheet for details.

0x9: ACT_1:
Pin-specific Active source #1 (SCB-UART). See the device datasheet for details.

0xa: ACT_2:
Pin-specific Active source #2 (CAN)
See the device datasheet for details.

0xb: ACT_3:
Reserved

0xc: DS_0:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xe: DS_2:
Chip specific DeepSleep source 2 connection(SCB-I2C, TCPWM, SWD, LPComp, Wakeup). See the device datasheet for details.

0xf: DS_3:
Chip specific DeepSleep source 3 connection(SCB-SPI). See the device datasheet for details.

18.1.7 HSIOM_PORT_SEL6

Port selection register

Address: 0x40020600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 20	IO5_SEL	Selects connection for Pin 5. Default Value: 0
19 : 16	IO4_SEL	Selects connection for Pin 4. Default Value: 0
15 : 12	IO3_SEL	Selects connection for Pin 3. Default Value: 0
11 : 8	IO2_SEL	Selects connection for Pin 2. Default Value: 0
7 : 4	IO1_SEL	Selects connection for Pin 1. Default Value: 0
3 : 0	IO0_SEL	Selects connection for Pin 0. Default Value: 0
		Note that the availability of Active and Deep Sleep source depends on the pin. See the Pin Outs section of the device datasheet to know the functions available for each pin.
		0x0: GPIO: Pin is regular firmware-controlled I/O or connected to dedicated hardware block

18.1.7 HSIOM_PORT_SEL6 (continued)

0x1: GPIO_DSI:
Output is firmware controlled, but OE is controlled from DSI.

0x2: DSI_DSI:
Both output and OE are controlled from DSI.

0x3: DSI_GPIO:
Output is controlled from DSI, but OE is firmware controlled

0x4: CSD_SENSE:
Pin is a CSD sense pin (analog mode)

0x5: CSD_SHIELD:
Pin is a CSD shield pin (analog mode).

0x6: AMUXA:
Pin is connected to AMUXBUS-A.

0x7: AMUXB:
Pin is connected to AMUXBUS-B. This mode is also used for CSD I/O charging. When CSD I/O charging is enabled in CSD_CONTROL, digital I/O driver is connected to csd_charge signal (pin is still connected to AMUXBUS-B).

0x8: ACT_0:
Pin-specific Active source #0 (TCPWM, EXT CLOCK). See the device datasheet for details.

0x9: ACT_1:
Pin-specific Active source #1 (SCB-UART). See the device datasheet for details.

0xa: ACT_2:
Pin-specific Active source #2 (CAN)
See the device datasheet for details.

0xb: ACT_3:
Reserved

0xc: DS_0:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xe: DS_2:
Chip specific DeepSleep source 2 connection(SCB-I2C, TCPWM, SWD, LPComp, Wakeup). See the device datasheet for details.

0xf: DS_3:
Chip specific DeepSleep source 3 connection(SCB-SPI). See the device datasheet for details.

18.1.8 HSIOM_PORT_SEL7

Port selection register

Address: 0x40020700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				RW			
Name	None [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	IO2_SEL	Selects connection for Pin 2. Default Value: 0
7 : 4	IO1_SEL	Selects connection for Pin 1. Default Value: 0
3 : 0	IO0_SEL	Selects connection for Pin 0. Default Value: 0
		Note that the availability of Active and Deep Sleep source depends on the pin. See the Pin Outs section of the device datasheet to know the functions available for each pin. **0x0: GPIO:** Pin is regular firmware-controlled I/O or connected to dedicated hardware block **0x1: GPIO_DSI:** Output is firmware controlled, but OE is controlled from DSI. **0x2: DSI_DSI:** Both output and OE are controlled from DSI. **0x3: DSI_GPIO:** Output is controlled from DSI, but OE is firmware controlled

18.1.8 HSIOM_PORT_SEL7 (continued)

0x4: CSD_SENSE:
Pin is a CSD sense pin (analog mode)

0x5: CSD_SHIELD:
Pin is a CSD shield pin (analog mode).

0x6: AMUXA:
Pin is connected to AMUXBUS-A.

0x7: AMUXB:
Pin is connected to AMUXBUS-B. This mode is also used for CSD I/O charging. When CSD I/O charging is enabled in CSD_CONTROL, digital I/O driver is connected to csd_charge signal (pin is still connected to AMUXBUS-B).

0x8: ACT_0:
Pin-specific Active source #0 (TCPWM, EXT CLOCK). See the device datasheet for details.

0x9: ACT_1:
Pin-specific Active source #1 (SCB-UART). See the device datasheet for details.

0xa: ACT_2:
Pin-specific Active source #2 (CAN)
See the device datasheet for details.

0xb: ACT_3:
Reserved

0xc: DS_0:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xe: DS_2:
Chip specific DeepSleep source 2 connection(SCB-I2C, TCPWM, SWD, LPComp, Wakeup). See the device datasheet for details.

0xf: DS_3:
Chip specific DeepSleep source 3 connection(SCB-SPI). See the device datasheet for details.

19 LCD Registers

This section discusses the LCD registers. It lists all the registers in mapping tables, in address order.

19.1 Register Details

Register Name	Address
LCD_ID	0x402A0000
LCD_DIVIDER	0x402A0004
LCD_CONTROL	0x402A0008
LCD_DATA00	0x402A0100
LCD_DATA01	0x402A0104
LCD_DATA02	0x402A0108
LCD_DATA03	0x402A010C
LCD_DATA04	0x402A0110
LCD_DATA05	0x402A0114
LCD_DATA06	0x402A0118
LCD_DATA07	0x402A011C
LCD_DATA10	0x402A0200
LCD_DATA11	0x402A0204
LCD_DATA12	0x402A0208
LCD_DATA13	0x402A020C
LCD_DATA14	0x402A0210
LCD_DATA15	0x402A0214
LCD_DATA16	0x402A0218
LCD_DATA17	0x402A021C

19.1.1 LCD_ID

ID & Revision

Address: 0x402A0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	REVISION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	REVISION [31:24]							

Bits	Name	Description
31 : 16	REVISION	the version number is 0x0001 Default Value: 1
15 : 0	ID	the ID of LCD controller peripheral is 0xF0F0 Default Value: 61680

19.1.2 LCD_DIVIDER

LCD Divider Register

Address: 0x402A0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SUBFR_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SUBFR_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEAD_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DEAD_DIV [31:24]							

Bits	Name	Description
31 : 16	DEAD_DIV	Length of the dead time period in cycles. When set to zero, no dead time period exists. Default Value: 0
15 : 0	SUBFR_DIV	Input clock frequency divide value, to generate the 1/4 sub-frame period. The sub-frame period is 4*(SUBFR_DIV+1) cycles long. Default Value: 0

19.1.3 LCD_CONTROL

LCD Configuration Register

Address: 0x402A0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW	RW	RW	RW	RW
HW Access	None	R		R	R	R	R	R
Name	None	BIAS [6:5]		OP_MODE	TYPE	LCD_MODE	HS_EN	LS_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				COM_NUM [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	LS_EN_STAT	None [30:24]						

Bits	Name	Description
31	LS_EN_STAT	LS enable status bit. This bit is a copy of LS_EN that is synchronized to the low speed clock domain and back to the system clock domain. Firmware can use this bit to observe whether LS_EN has taken effect in the low speed clock domain. Firmware should never change the configuration for the LS generator without ensuring this bit is 0. The following procedure should be followed to disable the LS generator: 1. If LS_EN=0 we are done. Exit the procedure. 2. Check that LS_EN_STAT=1. If not, wait until it is. This will catch the case of a recent enable (LS_EN=1) that has not taken effect yet. 3. Set LS_EN=0. 4. Wait until LS_EN_STAT=0. Default Value: 0

19.1.3 LCD_CONTROL (continued)

11 : 8	COM_NUM	The number of COM connections minus 2. So: 0: 2 COM's 1: 3 COM's ... 13: 15 COM's 14: 16 COM's 15: undefined Default Value: 0
6 : 5	BIAS	PWM bias selection Default Value: 0 **0x0: HALF:** 1/2 Bias **0x1: THIRD:** 1/3 Bias **0x2: FOURTH:** 1/4 Bias (not supported by LS generator) **0x3: FIFTH:** 1/5 Bias (not supported by LS generator)
4	OP_MODE	Driving mode configuration Default Value: 0 **0x0: PWM:** PWM Mode **0x1: CORRELATION:** Digital Correlation Mode
3	TYPE	LCD driving waveform type configuration. Default Value: 0 **0x0: TYPE_A:** Type A - Each frame addresses each COM pin only once with a balanced (DC=0) waveform. **0x1: TYPE_B:** Type B - Each frame addresses each COM pin twice in sequence with a positive and negative waveform that together are balanced (DC=0).
2	LCD_MODE	HS/LS Mode selection Default Value: 0 **0x0: LS:** Select Low Speed (32kHz) Generator (Works in Active, Sleep and DeepSleep power modes). **0x1: HS:** Select High Speed (system clock) Generator (Works in Active and Sleep power modes only).
1	HS_EN	High speed (HS) generator enable 1: enable 0: disable Default Value: 0
0	LS_EN	Low speed (LS) generator enable 1: enable 0: disable Default Value: 0

19.1.4 LCD_DATA00

LCD Pin Data Registers

Address: 0x402A0100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

19.1.5 LCD_DATA01

LCD Pin Data Registers

Address: 0x402A0104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

19.1.6 LCD_DATA02

LCD Pin Data Registers

Address: 0x402A0108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

19.1.7 LCD_DATA03

LCD Pin Data Registers

Address: 0x402A010C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

19.1.8 LCD_DATA04

LCD Pin Data Registers

Address: 0x402A0110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

19.1.9 LCD_DATA05

LCD Pin Data Registers

Address: 0x402A0114

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

19.1.10 LCD_DATA06

LCD Pin Data Registers

Address: 0x402A0118

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

19.1.11 LCD_DATA07

LCD Pin Data Registers

Address: 0x402A011C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

19.1.12 LCD_DATA10

LCD Pin Data Registers

Address: 0x402A0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

19.1.13 LCD_DATA11

LCD Pin Data Registers

Address: 0x402A0204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

19.1.14 LCD_DATA12

LCD Pin Data Registers

Address: 0x402A0208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

19.1.15 LCD_DATA13

LCD Pin Data Registers

Address: 0x402A020C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

19.1.16 LCD_DATA14

LCD Pin Data Registers

Address: 0x402A0210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

19.1.17 LCD_DATA15

LCD Pin Data Registers

Address: 0x402A0214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

19.1.18 LCD_DATA16

LCD Pin Data Registers

Address: 0x402A0218

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

19.1.19 LCD_DATA17

LCD Pin Data Registers

Address: 0x402A021C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

20 Low Power Comparator (LPCOMP) Registers

This section discusses the LPCOMP registers. It lists all the registers in mapping tables, in address order.

20.1 Register Details

Register Name	Address
LPCOMP_ID	0x402B0000
LPCOMP_CONFIG	0x402B0004
LPCOMP_INTR	0x402B0010
LPCOMP_INTR_SET	0x402B0014
LPCOMP_INTR_MASK	0x402B0018
LPCOMP_INTR_MASKED	0x402B001C
LPCOMP_TRIM1	0x402BFF00
LPCOMP_TRIM2	0x402BFF04
LPCOMP_TRIM3	0x402BFF08
LPCOMP_TRIM4	0x402BFF0C

20.1.1 LPCOMP_ID

ID & Revision

Address: 0x402B0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	REVISION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	REVISION [31:24]							

Bits	Name	Description
31 : 16	REVISION	the version number is 0x0001 Default Value: 1
15 : 0	ID	the ID of LPCOMP peripheral is 0xE0E0 Default Value: 57568

20.1.2 LPCOMP_CONFIG

LPCOMP Configuration Register

Address: 0x402B0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	R	RW		RW	RW	RW	
HW Access	R	RW	R		R	R	R	
Name	ENABLE1	OUT1	INTTYPE1 [5:4]		FILTER1	HYST1	MODE1 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	R	RW		RW	RW	RW	
HW Access	R	RW	R		R	R	R	
Name	ENABLE2	OUT2	INTTYPE2 [13:12]		FILTER2	HYST2	MODE2 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW	RW	None		RW	RW
HW Access	None		R	R	None		R	R
Name	None [23:22]		DSI_LEVEL2	DSI_BYPASS2	None [19:18]		DSI_LEVEL1	DSI_BYPASS1

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	DSI_LEVEL2	Opamp2 comparator DSI (trigger) out level : 0=pulse, 1=level Default Value: 0
20	DSI_BYPASS2	Opamp2 bypass comparator output synchronization for DSI output: 0=synchronize (level or pulse), 1=bypass (output async) Default Value: 0
17	DSI_LEVEL1	Opamp1 comparator DSI (trigger) out level : 0=pulse, 1=level Default Value: 0
16	DSI_BYPASS1	Opamp1 bypass comparator output synchronization for DSI output: 0=synchronize (level or pulse), 1=bypass (output async) Default Value: 0
15	ENABLE2	Enable comparator #2 Default Value: 0
14	OUT2	Current output value of the comparator. Default Value: 0
13 : 12	INTTYPE2	Sets which edge will trigger an IRQ Default Value: 0

20.1.2 LPCOMP_CONFIG (continued)

		0x0: DISABLE: Disabled, no interrupts will be detected
		0x1: RISING: Rising edge
		0x2: FALLING: Falling edge
		0x3: BOTH: Both rising and falling edges
11	FILTER2	Deprecated, Reserved, must be written 0 Default Value: 0
10	HYST2	Add 10mV hysteresis to the comparator - 0: Enable Hysteresis - 1: Disable Hysteresis Default Value: 0
9 : 8	MODE2	Operating mode for the comparator Default Value: 0
		0x0: SLOW: Slow operating mode (uses less power, <50uA)
		0x1: FAST: Fast operating mode (uses more power, <400uA)
		0x2: ULP: Ultra low power operting mode (uses ~2-4uA)
7	ENABLE1	Enable comparator #1 Default Value: 0
6	OUT1	Current output value of the comparator. Default Value: 0
5 : 4	INTTYPE1	Sets which edge will trigger an IRQ Default Value: 0
		0x0: DISABLE: Disabled, no interrupts will be detected
		0x1: RISING: Rising edge
		0x2: FALLING: Falling edge
		0x3: BOTH: Both rising and falling edges
3	FILTER1	Deprecated, Reserved, must be written 0 Default Value: 0
2	HYST1	Add 10mV hysteresis to the comparator - 0: Enable Hysteresis - 1: Disable Hysteresis Default Value: 0
1 : 0	MODE1	Operating mode for the comparator Default Value: 0
		0x0: SLOW: Slow operating mode (uses less power, <50uA)

20.1.2 LPCOMP_CONFIG (continued)

0x1: FAST:
Fast operating mode (uses more power, <400uA)

0x2: ULP:
Ultra low power operting mode (uses ~2-4uA)

20.1.3 LPCOMP_INTR

LPCOMP Interrupt request register

Address: 0x402B0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						COMP2	COMP1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP2	Comparator 2 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0
0	COMP1	Comparator 1 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0

20.1.4 LPCOMP_INTR_SET

LPCOMP Interrupt set register

Address: 0x402B0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						COMP2	COMP1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP2	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	COMP1	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

20.1.5 LPCOMP_INTR_MASK

LPCOMP Interrupt request mask

Address: 0x402B0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						COMP2_MASK	COMP1_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP2_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

20.1.6 LPCOMP_INTR_MASKED

LPCOMP Interrupt request masked

Address: 0x402B001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						COMP2_MASKED	COMP1_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP2_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

20.1.7 LPCOMP_TRIM1

LPCOMP Trim Register

Address: 0x402BFF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			COMP1_TRIMA [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	COMP1_TRIMA	Trim A for Comparator #1 Default Value: 0

20.1.8 LPCOMP_TRIM2

LPCOMP Trim Register

Address: 0x402BFF04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			COMP1_TRIMB [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	COMP1_TRIMB	Trim B for Comparator #1 Default Value: 0

20.1.9 LPCOMP_TRIM3

LPCOMP Trim Register

Address: 0x402BFF08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			COMP2_TRIMA [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	COMP2_TRIMA	Trim A for Comparator #2 Default Value: 0

20.1.10 LPCOMP_TRIM4

LPCOMP Trim Register

Address: 0x402BFF0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			COMP2_TRIMB [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	COMP2_TRIMB	Trim B for Comparator #2 Default Value: 0

21 Port Adaptor (PA) Registers

This section discusses the PA registers. It lists all the registers in mapping tables, in address order.

21.1 Register Details

Register Name	Address
UDB_PA0_CFG0	0x400F5000
UDB_PA0_CFG1	0x400F5001
UDB_PA0_CFG2	0x400F5002
UDB_PA0_CFG3	0x400F5003
UDB_PA0_CFG4	0x400F5004
UDB_PA0_CFG5	0x400F5005
UDB_PA0_CFG6	0x400F5006
UDB_PA0_CFG7	0x400F5007
UDB_PA0_CFG8	0x400F5008
UDB_PA0_CFG9	0x400F5009
UDB_PA0_CFG10	0x400F500A
UDB_PA0_CFG11	0x400F500B
UDB_PA0_CFG12	0x400F500C
UDB_PA0_CFG13	0x400F500D
UDB_PA0_CFG14	0x400F500E
UDB_PA1_CFG0	0x400F5010
UDB_PA1_CFG1	0x400F5011
UDB_PA1_CFG2	0x400F5012
UDB_PA1_CFG3	0x400F5013
UDB_PA1_CFG4	0x400F5014
UDB_PA1_CFG5	0x400F5015
UDB_PA1_CFG6	0x400F5016
UDB_PA1_CFG7	0x400F5017
UDB_PA1_CFG8	0x400F5018
UDB_PA1_CFG9	0x400F5019
UDB_PA1_CFG10	0x400F501A
UDB_PA1_CFG11	0x400F501B

Register Name	Address
UDB_PA1_CFG12	0x400F501C
UDB_PA1_CFG13	0x400F501D
UDB_PA1_CFG14	0x400F501E
UDB_PA2_CFG0	0x400F5020
UDB_PA2_CFG1	0x400F5021
UDB_PA2_CFG2	0x400F5022
UDB_PA2_CFG3	0x400F5023
UDB_PA2_CFG4	0x400F5024
UDB_PA2_CFG5	0x400F5025
UDB_PA2_CFG6	0x400F5026
UDB_PA2_CFG7	0x400F5027
UDB_PA2_CFG8	0x400F5028
UDB_PA2_CFG9	0x400F5029
UDB_PA2_CFG10	0x400F502A
UDB_PA2_CFG11	0x400F502B
UDB_PA2_CFG12	0x400F502C
UDB_PA2_CFG13	0x400F502D
UDB_PA2_CFG14	0x400F502E
UDB_PA3_CFG0	0x400F5030
UDB_PA3_CFG1	0x400F5031
UDB_PA3_CFG2	0x400F5032
UDB_PA3_CFG3	0x400F5033
UDB_PA3_CFG4	0x400F5034
UDB_PA3_CFG5	0x400F5035
UDB_PA3_CFG6	0x400F5036
UDB_PA3_CFG7	0x400F5037
UDB_PA3_CFG8	0x400F5038
UDB_PA3_CFG9	0x400F5039
UDB_PA3_CFG10	0x400F503A
UDB_PA3_CFG11	0x400F503B
UDB_PA3_CFG12	0x400F503C
UDB_PA3_CFG13	0x400F503D
UDB_PA3_CFG14	0x400F503E

21.1.1 UDB_PA0_CFG0

PA Data In Clock Control Register

Address: 0x400F5000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	NC [7:6]		CLKIN_INV	CLKIN_EN_INV	CLKIN_EN_MODE [3:2]		CLKIN_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	NC	Spare register bits Default Value: 0
5	CLKIN_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	CLKIN_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	CLKIN_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKIN_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4]

21.1.1 UDB_PA0_CFG0 (continued)

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

21.1.2 UDB_PA0_CFG1

PA Data Out Clock Control Register

Address: 0x400F5001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	NC [7:6]		CLKOUT_INV	CLKOUT_EN_INV	CLKOUT_EN_MODE [3:2]		CLKOUT_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	NC	Spare register bits Default Value: 0
5	CLKOUT_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	CLKOUT_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	CLKOUT_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKOUT_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4]

21.1.2 UDB_PA0_CFG1 (continued)

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

21.1.3 UDB_PA0_CFG2

PA Clock Select Register

Address: 0x400F5002

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	CLKOUT_SEL [7:4]				CLKIN_SEL [3:0]			

Bits	Name	Description
7 : 4	CLKOUT_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x9: BUS_CLK_APP:** bus_clk_app **0xc: PIN_RC:** pin_rc - port pin multiplexer output **0xd: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0xe: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0xf: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3 : 0	CLKIN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0]

21.1.3 UDB_PA0_CFG2 (continued)

0x1: GCLK1:
gclk[1]

0x2: GCLK2:
gclk[2]

0x3: GCLK3:
gclk[3]

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x9: BUS_CLK_APP:
bus_clk_app

0xc: PIN_RC:
pin_rc - port pin multiplexer output

0xd: DSI_RC_0:
dsi_rc[0] - dsi_xx_out_p[4]

0xe: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0xf: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

21.1.4 UDB_PA0_CFG3

PA Reset Select Register

Address: 0x400F5003

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	
HW Access	R	R	R		R	R	R	
Name	NC7	RES_OUT_INV	RES_OUT_SEL [5:4]		NC0	RES_IN_INV	RES_IN_SEL [1:0]	

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6	RES_OUT_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
5 : 4	RES_OUT_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0x2: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0x3: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3	NC0	Spare register bit Default Value: 0
2	RES_IN_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
1 : 0	RES_IN_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output

21.1.4 UDB_PA0_CFG3 (continued)

0x1: DSI_RC_0:
dsi_rc[0] - dsi_xx_out_p[4]

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

21.1.5 UDB_PA0_CFG4

PA Reset Enable Register

Address: 0x400F5004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	RW
HW Access	R					R	R	R
Name	NC7654 [7:3]					RES_OE_EN	RES_OUT_EN	RES_IN_EN

Bits	Name	Description
7 : 3	NC7654	Spare register bits Default Value: 0
2	RES_OE_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
1	RES_OUT_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
0	RES_IN_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled

21.1.6 UDB_PA0_CFG5

PA Reset Pin Select Register

Address: 0x400F5005

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		RW
HW Access	R					None		R
Name	NC7654 [7:3]					None [2:1]		PIN_SEL

Bits	Name	Description
7 : 3	NC7654	Spare register bits Default Value: 0
0	PIN_SEL	Select port input to route to reset multiplexer (dsi_xx_input_p[7:0]) Default Value: 0 **0x0: PIN0:** dsi_from_port_pin[0] **0x1: PIN1:** dsi_from_port_pin[1] **0x2: PIN2:** dsi_from_port_pin[2] **0x3: PIN3:** dsi_from_port_pin[3] **0x4: PIN4:** dsi_from_port_pin[4] **0x5: PIN5:** dsi_from_port_pin[5] **0x6: PIN6:** dsi_from_port_pin[6] **0x7: PIN7:** dsi_from_port_pin[7]

21.1.7 UDB_PA0_CFG6

PA Input Data Sync Control Register - Low

Address: 0x400F5006

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC3 [7:6]		IN_SYNC2 [5:4]		IN_SYNC1 [3:2]		IN_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	IN_SYNC3	Synchronization selection for PA input 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	IN_SYNC2	Synchronization selection for PA input 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	IN_SYNC1	Synchronization selection for PA input 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	IN_SYNC0	Synchronization selection for PA input 0 Default Value: 0

21.1.7 UDB_PA0_CFG6 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

21.1.8 UDB_PA0_CFG7

PA Input Data Sync Control Register - High

Address: 0x400F5007

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC7 [7:6]		IN_SYNC6 [5:4]		IN_SYNC5 [3:2]		IN_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	IN_SYNC7	Synchronization selection for PA input 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	IN_SYNC6	Synchronization selection for PA input 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	IN_SYNC5	Synchronization selection for PA input 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	IN_SYNC4	Synchronization selection for PA input 4 Default Value: 0

21.1.8 UDB_PA0_CFG7 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

21.1.9 UDB_PA0_CFG8

PA Output Data Sync Control Register - Low

Address: 0x400F5008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC3 [7:6]		OUT_SYNC2 [5:4]		OUT_SYNC1 [3:2]		OUT_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	OUT_SYNC3	Synchronization selection for PA output 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	OUT_SYNC2	Synchronization selection for PA output 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	OUT_SYNC1	Synchronization selection for PA output 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	OUT_SYNC0	Synchronization selection for PA output 0 Default Value: 0

21.1.9 UDB_PA0_CFG8 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

21.1.10 UDB_PA0_CFG9

PA Output Data Sync Control Register - High

Address: 0x400F5009

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC7 [7:6]		OUT_SYNC6 [5:4]		OUT_SYNC5 [3:2]		OUT_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	OUT_SYNC7	Synchronization selection for PA output 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	OUT_SYNC6	Synchronization selection for PA output 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	OUT_SYNC5	Synchronization selection for PA output 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	OUT_SYNC4	Synchronization selection for PA output 4 Default Value: 0

21.1.10 UDB_PA0_CFG9 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

21.1.11 UDB_PA0_CFG10

PA Output Data Select Register - Low

Address: 0x400F500A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL3 [7:6]		DATA_SEL2 [5:4]		DATA_SEL1 [3:2]		DATA_SEL0 [1:0]	

Bits	Name	Description
7 : 6	DATA_SEL3	Data selection for PA output 3 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	DATA_SEL2	Data selection for PA output 2 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	DATA_SEL1	Data selection for PA output 1 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	DATA_SEL0	Data selection for PA output 0 Default Value: 0

21.1.11 UDB_PA0_CFG10 (continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

21.1.12 UDB_PA0_CFG11

PA Output Data Select Register - High

Address: 0x400F500B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL7 [7:6]		DATA_SEL6 [5:4]		DATA_SEL5 [3:2]		DATA_SEL4 [1:0]	

Bits	Name	Description
7 : 6	DATA_SEL7	Data selection for PA output 7 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	DATA_SEL6	Data selection for PA output 6 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	DATA_SEL5	Data selection for PA output 5 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	DATA_SEL4	Data selection for PA output 4 Default Value: 0

21.1.12 UDB_PA0_CFG11 (continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

21.1.13 UDB_PA0_CFG12

PA OE Select Register - Low

Address: 0x400F500C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL3 [7:6]		OE_SEL2 [5:4]		OE_SEL1 [3:2]		OE_SEL0 [1:0]	

Bits	Name	Description
7 : 6	OE_SEL3	Data selection for PA oe 3 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	OE_SEL2	Data selection for PA oe 2 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	OE_SEL1	Data selection for PA oe 1 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	OE_SEL0	Data selection for PA oe 0 Default Value: 0

21.1.13 UDB_PA0_CFG12 (continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

21.1.14 UDB_PA0_CFG13

PA OE Select Register - High

Address: 0x400F500D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL7 [7:6]		OE_SEL6 [5:4]		OE_SEL5 [3:2]		OE_SEL4 [1:0]	

Bits	Name	Description
7 : 6	OE_SEL7	Data selection for PA oe 7 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	OE_SEL6	Data selection for PA oe 6 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	OE_SEL5	Data selection for PA oe 5 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	OE_SEL4	Data selection for PA oe 4 Default Value: 0

21.1.14 UDB_PA0_CFG13 (continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

21.1.15 UDB_PA0_CFG14

PA OE Sync Register

Address: 0x400F500E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SYNC3 [7:6]		OE_SYNC2 [5:4]		OE_SYNC1 [3:2]		OE_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	OE_SYNC3	Synchronization options for dsi_to_oe[3] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
5 : 4	OE_SYNC2	Synchronization options for dsi_to_oe[2] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
3 : 2	OE_SYNC1	Synchronization options for dsi_to_oe[1] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
1 : 0	OE_SYNC0	Synchronization options for dsi_to_oe[0] Default Value: 0

21.1.15 UDB_PA0_CFG14 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CONSTANT1:
1

0x3: CONSTANT0:
0

21.1.16 UDB_PA1_CFG0

PA Data In Clock Control Register

Address: 0x400F5010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	NC [7:6]		CLKIN_INV	CLKIN_EN_INV	CLKIN_EN_MODE [3:2]		CLKIN_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	NC	Spare register bits Default Value: 0
5	CLKIN_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	CLKIN_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	CLKIN_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKIN_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4]

21.1.16 UDB_PA1_CFG0 (continued)

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

21.1.17 UDB_PA1_CFG1

PA Data Out Clock Control Register

Address: 0x400F5011

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	NC [7:6]		CLKOUT_INV	CLKOUT_EN_INV	CLKOUT_EN_MODE [3:2]		CLKOUT_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	NC	Spare register bits Default Value: 0
5	CLKOUT_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	CLKOUT_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	CLKOUT_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKOUT_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4]

21.1.17 UDB_PA1_CFG1 (continued)

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

21.1.18 UDB_PA1_CFG2

PA Clock Select Register

Address: 0x400F5012

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	CLKOUT_SEL [7:4]				CLKIN_SEL [3:0]			

Bits	Name	Description
7 : 4	CLKOUT_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x9: BUS_CLK_APP:** bus_clk_app **0xc: PIN_RC:** pin_rc - port pin multiplexer output **0xd: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0xe: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0xf: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3 : 0	CLKIN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0]

21.1.18 UDB_PA1_CFG2 (continued)

0x1: GCLK1:
gclk[1]

0x2: GCLK2:
gclk[2]

0x3: GCLK3:
gclk[3]

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x9: BUS_CLK_APP:
bus_clk_app

0xc: PIN_RC:
pin_rc - port pin multiplexer output

0xd: DSI_RC_0:
dsi_rc[0] - dsi_xx_out_p[4]

0xe: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0xf: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

21.1.19 UDB_PA1_CFG3

PA Reset Select Register

Address: 0x400F5013

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	
HW Access	R	R	R		R	R	R	
Name	NC7	RES_OUT_INV	RES_OUT_SEL [5:4]		NC0	RES_IN_INV	RES_IN_SEL [1:0]	

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6	RES_OUT_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
5 : 4	RES_OUT_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0x2: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0x3: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3	NC0	Spare register bit Default Value: 0
2	RES_IN_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
1 : 0	RES_IN_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output

21.1.19 UDB_PA1_CFG3 (continued)

0x1: DSI_RC_0:
dsi_rc[0] - dsi_xx_out_p[4]

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

21.1.20 UDB_PA1_CFG4

PA Reset Enable Register

Address: 0x400F5014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	RW
HW Access	R					R	R	R
Name	NC7654 [7:3]					RES_OE_EN	RES_OUT_EN	RES_IN_EN

Bits	Name	Description
7 : 3	NC7654	Spare register bits Default Value: 0
2	RES_OE_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
1	RES_OUT_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
0	RES_IN_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled

21.1.21 UDB_PA1_CFG5

PA Reset Pin Select Register

Address: 0x400F5015

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		RW
HW Access	R					None		R
Name	NC7654 [7:3]					None [2:1]		PIN_SEL

Bits	Name	Description
7 : 3	NC7654	Spare register bits Default Value: 0
0	PIN_SEL	Select port input to route to reset multiplexer (dsi_xx_input_p[7:0]) Default Value: 0 **0x0: PIN0:** dsi_from_port_pin[0] **0x1: PIN1:** dsi_from_port_pin[1] **0x2: PIN2:** dsi_from_port_pin[2] **0x3: PIN3:** dsi_from_port_pin[3] **0x4: PIN4:** dsi_from_port_pin[4] **0x5: PIN5:** dsi_from_port_pin[5] **0x6: PIN6:** dsi_from_port_pin[6] **0x7: PIN7:** dsi_from_port_pin[7]

21.1.22 UDB_PA1_CFG6

PA Input Data Sync Control Register - Low

Address: 0x400F5016

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC3 [7:6]		IN_SYNC2 [5:4]		IN_SYNC1 [3:2]		IN_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	IN_SYNC3	Synchronization selection for PA input 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	IN_SYNC2	Synchronization selection for PA input 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	IN_SYNC1	Synchronization selection for PA input 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	IN_SYNC0	Synchronization selection for PA input 0 Default Value: 0

21.1.22 UDB_PA1_CFG6 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

21.1.23 UDB_PA1_CFG7

PA Input Data Sync Control Register - High

Address: 0x400F5017

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC7 [7:6]		IN_SYNC6 [5:4]		IN_SYNC5 [3:2]		IN_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	IN_SYNC7	Synchronization selection for PA input 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	IN_SYNC6	Synchronization selection for PA input 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	IN_SYNC5	Synchronization selection for PA input 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	IN_SYNC4	Synchronization selection for PA input 4 Default Value: 0

21.1.23 UDB_PA1_CFG7 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

21.1.24 UDB_PA1_CFG8

PA Output Data Sync Control Register - Low

Address: 0x400F5018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC3 [7:6]		OUT_SYNC2 [5:4]		OUT_SYNC1 [3:2]		OUT_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	OUT_SYNC3	Synchronization selection for PA output 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	OUT_SYNC2	Synchronization selection for PA output 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	OUT_SYNC1	Synchronization selection for PA output 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	OUT_SYNC0	Synchronization selection for PA output 0 Default Value: 0

21.1.24 UDB_PA1_CFG8 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

21.1.25 UDB_PA1_CFG9

PA Output Data Sync Control Register - High

Address: 0x400F5019

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC7 [7:6]		OUT_SYNC6 [5:4]		OUT_SYNC5 [3:2]		OUT_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	OUT_SYNC7	Synchronization selection for PA output 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	OUT_SYNC6	Synchronization selection for PA output 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	OUT_SYNC5	Synchronization selection for PA output 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	OUT_SYNC4	Synchronization selection for PA output 4 Default Value: 0

21.1.25 UDB_PA1_CFG9 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

21.1.26 UDB_PA1_CFG10

PA Output Data Select Register - Low

Address: 0x400F501A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL3 [7:6]		DATA_SEL2 [5:4]		DATA_SEL1 [3:2]		DATA_SEL0 [1:0]	

Bits	Name	Description
7 : 6	DATA_SEL3	Data selection for PA output 3 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	DATA_SEL2	Data selection for PA output 2 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	DATA_SEL1	Data selection for PA output 1 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	DATA_SEL0	Data selection for PA output 0 Default Value: 0

21.1.26 UDB_PA1_CFG10 (continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

21.1.27 UDB_PA1_CFG11

PA Output Data Select Register - High

Address: 0x400F501B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL7 [7:6]		DATA_SEL6 [5:4]		DATA_SEL5 [3:2]		DATA_SEL4 [1:0]	

Bits	Name	Description
7 : 6	DATA_SEL7	Data selection for PA output 7 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	DATA_SEL6	Data selection for PA output 6 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	DATA_SEL5	Data selection for PA output 5 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	DATA_SEL4	Data selection for PA output 4 Default Value: 0

21.1.27 UDB_PA1_CFG11 (continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

21.1.28 UDB_PA1_CFG12

PA OE Select Register - Low

Address: 0x400F501C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL3 [7:6]		OE_SEL2 [5:4]		OE_SEL1 [3:2]		OE_SEL0 [1:0]	

Bits	Name	Description
7 : 6	OE_SEL3	Data selection for PA oe 3 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	OE_SEL2	Data selection for PA oe 2 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	OE_SEL1	Data selection for PA oe 1 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	OE_SEL0	Data selection for PA oe 0 Default Value: 0

21.1.28 UDB_PA1_CFG12 (continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

21.1.29 UDB_PA1_CFG13

PA OE Select Register - High

Address: 0x400F501D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL7 [7:6]		OE_SEL6 [5:4]		OE_SEL5 [3:2]		OE_SEL4 [1:0]	

Bits	Name	Description
7 : 6	OE_SEL7	Data selection for PA oe 7 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	OE_SEL6	Data selection for PA oe 6 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	OE_SEL5	Data selection for PA oe 5 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	OE_SEL4	Data selection for PA oe 4 Default Value: 0

21.1.29 UDB_PA1_CFG13 (continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

21.1.30 UDB_PA1_CFG14

PA OE Sync Register

Address: 0x400F501E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SYNC3 [7:6]		OE_SYNC2 [5:4]		OE_SYNC1 [3:2]		OE_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	OE_SYNC3	Synchronization options for dsi_to_oe[3] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
5 : 4	OE_SYNC2	Synchronization options for dsi_to_oe[2] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
3 : 2	OE_SYNC1	Synchronization options for dsi_to_oe[1] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
1 : 0	OE_SYNC0	Synchronization options for dsi_to_oe[0] Default Value: 0

21.1.30 UDB_PA1_CFG14 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CONSTANT1:
1

0x3: CONSTANT0:
0

21.1.31 UDB_PA2_CFG0

PA Data In Clock Control Register

Address: 0x400F5020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	NC [7:6]		CLKIN_INV	CLKIN_EN_INV	CLKIN_EN_MODE [3:2]		CLKIN_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	NC	Spare register bits Default Value: 0
5	CLKIN_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	CLKIN_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	CLKIN_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKIN_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4]

21.1.31 UDB_PA2_CFG0 (continued)

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

21.1.32 UDB_PA2_CFG1

PA Data Out Clock Control Register

Address: 0x400F5021

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	NC [7:6]		CLKOUT_INV	CLKOUT_EN_INV	CLKOUT_EN_MODE [3:2]		CLKOUT_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	NC	Spare register bits Default Value: 0
5	CLKOUT_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	CLKOUT_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	CLKOUT_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKOUT_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4]

21.1.32 UDB_PA2_CFG1 (continued)

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

21.1.33 UDB_PA2_CFG2

PA Clock Select Register

Address: 0x400F5022

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	CLKOUT_SEL [7:4]				CLKIN_SEL [3:0]			

Bits	Name	Description
7 : 4	CLKOUT_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x9: BUS_CLK_APP:** bus_clk_app **0xc: PIN_RC:** pin_rc - port pin multiplexer output **0xd: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0xe: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0xf: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3 : 0	CLKIN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0]

21.1.33 UDB_PA2_CFG2 (continued)

0x1: GCLK1:
gclk[1]

0x2: GCLK2:
gclk[2]

0x3: GCLK3:
gclk[3]

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x9: BUS_CLK_APP:
bus_clk_app

0xc: PIN_RC:
pin_rc - port pin multiplexer output

0xd: DSI_RC_0:
dsi_rc[0] - dsi_xx_out_p[4]

0xe: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0xf: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

21.1.34 UDB_PA2_CFG3

PA Reset Select Register

Address: 0x400F5023

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	
HW Access	R	R	R		R	R	R	
Name	NC7	RES_OUT_INV	RES_OUT_SEL [5:4]		NC0	RES_IN_INV	RES_IN_SEL [1:0]	

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6	RES_OUT_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
5 : 4	RES_OUT_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0x2: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0x3: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3	NC0	Spare register bit Default Value: 0
2	RES_IN_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
1 : 0	RES_IN_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output

21.1.34 UDB_PA2_CFG3 (continued)

0x1: DSI_RC_0:
dsi_rc[0] - dsi_xx_out_p[4]

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

21.1.35 UDB_PA2_CFG4

PA Reset Enable Register

Address: 0x400F5024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	RW
HW Access	R					R	R	R
Name	NC7654 [7:3]					RES_OE_EN	RES_OUT_EN	RES_IN_EN

Bits	Name	Description
7 : 3	NC7654	Spare register bits Default Value: 0
2	RES_OE_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
1	RES_OUT_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
0	RES_IN_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled

21.1.36 UDB_PA2_CFG5

PA Reset Pin Select Register

Address: 0x400F5025

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		RW
HW Access	R					None		R
Name	NC7654 [7:3]					None [2:1]		PIN_SEL

Bits	Name	Description
7 : 3	NC7654	Spare register bits Default Value: 0
0	PIN_SEL	Select port input to route to reset multiplexer (dsi_xx_input_p[7:0]) Default Value: 0 **0x0: PIN0:** dsi_from_port_pin[0] **0x1: PIN1:** dsi_from_port_pin[1] **0x2: PIN2:** dsi_from_port_pin[2] **0x3: PIN3:** dsi_from_port_pin[3] **0x4: PIN4:** dsi_from_port_pin[4] **0x5: PIN5:** dsi_from_port_pin[5] **0x6: PIN6:** dsi_from_port_pin[6] **0x7: PIN7:** dsi_from_port_pin[7]

21.1.37 UDB_PA2_CFG6

PA Input Data Sync Control Register - Low

Address: 0x400F5026

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC3 [7:6]		IN_SYNC2 [5:4]		IN_SYNC1 [3:2]		IN_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	IN_SYNC3	Synchronization selection for PA input 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	IN_SYNC2	Synchronization selection for PA input 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	IN_SYNC1	Synchronization selection for PA input 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	IN_SYNC0	Synchronization selection for PA input 0 Default Value: 0

21.1.37 UDB_PA2_CFG6 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

21.1.38 UDB_PA2_CFG7

PA Input Data Sync Control Register - High

Address: 0x400F5027

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC7 [7:6]		IN_SYNC6 [5:4]		IN_SYNC5 [3:2]		IN_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	IN_SYNC7	Synchronization selection for PA input 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	IN_SYNC6	Synchronization selection for PA input 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	IN_SYNC5	Synchronization selection for PA input 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	IN_SYNC4	Synchronization selection for PA input 4 Default Value: 0

21.1.38 UDB_PA2_CFG7 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

21.1.39 UDB_PA2_CFG8

PA Output Data Sync Control Register - Low

Address: 0x400F5028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC3 [7:6]		OUT_SYNC2 [5:4]		OUT_SYNC1 [3:2]		OUT_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	OUT_SYNC3	Synchronization selection for PA output 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	OUT_SYNC2	Synchronization selection for PA output 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	OUT_SYNC1	Synchronization selection for PA output 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	OUT_SYNC0	Synchronization selection for PA output 0 Default Value: 0

21.1.39 UDB_PA2_CFG8 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

21.1.40 UDB_PA2_CFG9

PA Output Data Sync Control Register - High

Address: 0x400F5029

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC7 [7:6]		OUT_SYNC6 [5:4]		OUT_SYNC5 [3:2]		OUT_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	OUT_SYNC7	Synchronization selection for PA output 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	OUT_SYNC6	Synchronization selection for PA output 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	OUT_SYNC5	Synchronization selection for PA output 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	OUT_SYNC4	Synchronization selection for PA output 4 Default Value: 0

21.1.40 UDB_PA2_CFG9 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

21.1.41 UDB_PA2_CFG10

PA Output Data Select Register - Low

Address: 0x400F502A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL3 [7:6]		DATA_SEL2 [5:4]		DATA_SEL1 [3:2]		DATA_SEL0 [1:0]	

Bits	Name	Description
7 : 6	DATA_SEL3	Data selection for PA output 3 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	DATA_SEL2	Data selection for PA output 2 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	DATA_SEL1	Data selection for PA output 1 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	DATA_SEL0	Data selection for PA output 0 Default Value: 0

21.1.41 UDB_PA2_CFG10 (continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

21.1.42 UDB_PA2_CFG11

PA Output Data Select Register - High

Address: 0x400F502B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL7 [7:6]		DATA_SEL6 [5:4]		DATA_SEL5 [3:2]		DATA_SEL4 [1:0]	

Bits	Name	Description
7 : 6	DATA_SEL7	Data selection for PA output 7 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	DATA_SEL6	Data selection for PA output 6 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	DATA_SEL5	Data selection for PA output 5 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	DATA_SEL4	Data selection for PA output 4 Default Value: 0

21.1.42 UDB_PA2_CFG11 (continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

21.1.43 UDB_PA2_CFG12

PA OE Select Register - Low

Address: 0x400F502C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL3 [7:6]		OE_SEL2 [5:4]		OE_SEL1 [3:2]		OE_SEL0 [1:0]	

Bits	Name	Description
7 : 6	OE_SEL3	Data selection for PA oe 3 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	OE_SEL2	Data selection for PA oe 2 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	OE_SEL1	Data selection for PA oe 1 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	OE_SEL0	Data selection for PA oe 0 Default Value: 0

21.1.43 UDB_PA2_CFG12 (continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

21.1.44 UDB_PA2_CFG13

PA OE Select Register - High

Address: 0x400F502D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL7 [7:6]		OE_SEL6 [5:4]		OE_SEL5 [3:2]		OE_SEL4 [1:0]	

Bits	Name	Description
7 : 6	OE_SEL7	Data selection for PA oe 7 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	OE_SEL6	Data selection for PA oe 6 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	OE_SEL5	Data selection for PA oe 5 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	OE_SEL4	Data selection for PA oe 4 Default Value: 0

21.1.44 UDB_PA2_CFG13 (continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

21.1.45 UDB_PA2_CFG14

PA OE Sync Register

Address: 0x400F502E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SYNC3 [7:6]		OE_SYNC2 [5:4]		OE_SYNC1 [3:2]		OE_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	OE_SYNC3	Synchronization options for dsi_to_oe[3] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
5 : 4	OE_SYNC2	Synchronization options for dsi_to_oe[2] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
3 : 2	OE_SYNC1	Synchronization options for dsi_to_oe[1] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
1 : 0	OE_SYNC0	Synchronization options for dsi_to_oe[0] Default Value: 0

21.1.45 UDB_PA2_CFG14 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CONSTANT1:
1

0x3: CONSTANT0:
0

21.1.46 UDB_PA3_CFG0

PA Data In Clock Control Register

Address: 0x400F5030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	NC [7:6]		CLKIN_INV	CLKIN_EN_INV	CLKIN_EN_MODE [3:2]		CLKIN_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	NC	Spare register bits Default Value: 0
5	CLKIN_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	CLKIN_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	CLKIN_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKIN_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4]

21.1.46 UDB_PA3_CFG0 (continued)

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

21.1.47 UDB_PA3_CFG1

PA Data Out Clock Control Register

Address: 0x400F5031

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	NC [7:6]		CLKOUT_INV	CLKOUT_EN_INV	CLKOUT_EN_MODE [3:2]		CLKOUT_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	NC	Spare register bits Default Value: 0
5	CLKOUT_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	CLKOUT_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	CLKOUT_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKOUT_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4]

21.1.47 UDB_PA3_CFG1 (continued)

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

21.1.48 UDB_PA3_CFG2

PA Clock Select Register

Address: 0x400F5032

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	CLKOUT_SEL [7:4]				CLKIN_SEL [3:0]			

Bits	Name	Description
7 : 4	CLKOUT_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x9: BUS_CLK_APP:** bus_clk_app **0xc: PIN_RC:** pin_rc - port pin multiplexer output **0xd: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0xe: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0xf: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3 : 0	CLKIN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0]

21.1.48 UDB_PA3_CFG2 (continued)

0x1: GCLK1:
gclk[1]

0x2: GCLK2:
gclk[2]

0x3: GCLK3:
gclk[3]

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x9: BUS_CLK_APP:
bus_clk_app

0xc: PIN_RC:
pin_rc - port pin multiplexer output

0xd: DSI_RC_0:
dsi_rc[0] - dsi_xx_out_p[4]

0xe: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0xf: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

21.1.49 UDB_PA3_CFG3

PA Reset Select Register

Address: 0x400F5033

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	
HW Access	R	R	R		R	R	R	
Name	NC7	RES_OUT_INV	RES_OUT_SEL [5:4]		NC0	RES_IN_INV	RES_IN_SEL [1:0]	

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6	RES_OUT_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
5 : 4	RES_OUT_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0x2: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0x3: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3	NC0	Spare register bit Default Value: 0
2	RES_IN_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
1 : 0	RES_IN_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output

21.1.49 UDB_PA3_CFG3 (continued)

0x1: DSI_RC_0:
dsi_rc[0] - dsi_xx_out_p[4]

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

21.1.50 UDB_PA3_CFG4

PA Reset Enable Register

Address: 0x400F5034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	RW
HW Access	R					R	R	R
Name	NC7654 [7:3]					RES_OE_EN	RES_OUT_EN	RES_IN_EN

Bits	Name	Description
7 : 3	NC7654	Spare register bits Default Value: 0
2	RES_OE_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
1	RES_OUT_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
0	RES_IN_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled

21.1.51 UDB_PA3_CFG5

PA Reset Pin Select Register

Address: 0x400F5035

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		RW
HW Access	R					None		R
Name	NC7654 [7:3]					None [2:1]		PIN_SEL

Bits	Name	Description
7 : 3	NC7654	Spare register bits Default Value: 0
0	PIN_SEL	Select port input to route to reset multiplexer (dsi_xx_input_p[7:0]) Default Value: 0 **0x0: PIN0:** dsi_from_port_pin[0] **0x1: PIN1:** dsi_from_port_pin[1] **0x2: PIN2:** dsi_from_port_pin[2] **0x3: PIN3:** dsi_from_port_pin[3] **0x4: PIN4:** dsi_from_port_pin[4] **0x5: PIN5:** dsi_from_port_pin[5] **0x6: PIN6:** dsi_from_port_pin[6] **0x7: PIN7:** dsi_from_port_pin[7]

21.1.52 UDB_PA3_CFG6

PA Input Data Sync Control Register - Low

Address: 0x400F5036

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC3 [7:6]		IN_SYNC2 [5:4]		IN_SYNC1 [3:2]		IN_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	IN_SYNC3	Synchronization selection for PA input 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	IN_SYNC2	Synchronization selection for PA input 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	IN_SYNC1	Synchronization selection for PA input 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	IN_SYNC0	Synchronization selection for PA input 0 Default Value: 0

21.1.52 UDB_PA3_CFG6 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

21.1.53 UDB_PA3_CFG7

PA Input Data Sync Control Register - High

Address: 0x400F5037

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC7 [7:6]		IN_SYNC6 [5:4]		IN_SYNC5 [3:2]		IN_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	IN_SYNC7	Synchronization selection for PA input 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	IN_SYNC6	Synchronization selection for PA input 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	IN_SYNC5	Synchronization selection for PA input 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	IN_SYNC4	Synchronization selection for PA input 4 Default Value: 0

21.1.53 UDB_PA3_CFG7 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

21.1.54 UDB_PA3_CFG8

PA Output Data Sync Control Register - Low

Address: 0x400F5038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC3 [7:6]		OUT_SYNC2 [5:4]		OUT_SYNC1 [3:2]		OUT_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	OUT_SYNC3	Synchronization selection for PA output 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	OUT_SYNC2	Synchronization selection for PA output 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	OUT_SYNC1	Synchronization selection for PA output 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	OUT_SYNC0	Synchronization selection for PA output 0 Default Value: 0

21.1.54 UDB_PA3_CFG8 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

21.1.55 UDB_PA3_CFG9

PA Output Data Sync Control Register - High

Address: 0x400F5039

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC7 [7:6]		OUT_SYNC6 [5:4]		OUT_SYNC5 [3:2]		OUT_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	OUT_SYNC7	Synchronization selection for PA output 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	OUT_SYNC6	Synchronization selection for PA output 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	OUT_SYNC5	Synchronization selection for PA output 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	OUT_SYNC4	Synchronization selection for PA output 4 Default Value: 0

21.1.55 UDB_PA3_CFG9 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

21.1.56 UDB_PA3_CFG10

PA Output Data Select Register - Low

Address: 0x400F503A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL3 [7:6]		DATA_SEL2 [5:4]		DATA_SEL1 [3:2]		DATA_SEL0 [1:0]	

Bits	Name	Description
7 : 6	DATA_SEL3	Data selection for PA output 3 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	DATA_SEL2	Data selection for PA output 2 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	DATA_SEL1	Data selection for PA output 1 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	DATA_SEL0	Data selection for PA output 0 Default Value: 0

21.1.56 UDB_PA3_CFG10 (continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

21.1.57 UDB_PA3_CFG11

PA Output Data Select Register - High

Address: 0x400F503B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL7 [7:6]		DATA_SEL6 [5:4]		DATA_SEL5 [3:2]		DATA_SEL4 [1:0]	

Bits	Name	Description
7 : 6	DATA_SEL7	Data selection for PA output 7 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	DATA_SEL6	Data selection for PA output 6 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	DATA_SEL5	Data selection for PA output 5 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	DATA_SEL4	Data selection for PA output 4 Default Value: 0

21.1.57 UDB_PA3_CFG11 (continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

21.1.58 UDB_PA3_CFG12

PA OE Select Register - Low

Address: 0x400F503C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL3 [7:6]		OE_SEL2 [5:4]		OE_SEL1 [3:2]		OE_SEL0 [1:0]	

Bits	Name	Description
7 : 6	OE_SEL3	Data selection for PA oe 3 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	OE_SEL2	Data selection for PA oe 2 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	OE_SEL1	Data selection for PA oe 1 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	OE_SEL0	Data selection for PA oe 0 Default Value: 0

21.1.58 UDB_PA3_CFG12 (continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

21.1.59 UDB_PA3_CFG13

PA OE Select Register - High

Address: 0x400F503D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL7 [7:6]		OE_SEL6 [5:4]		OE_SEL5 [3:2]		OE_SEL4 [1:0]	

Bits	Name	Description
7 : 6	OE_SEL7	Data selection for PA oe 7 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	OE_SEL6	Data selection for PA oe 6 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	OE_SEL5	Data selection for PA oe 5 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	OE_SEL4	Data selection for PA oe 4 Default Value: 0

21.1.59 UDB_PA3_CFG13 (continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

21.1.60 UDB_PA3_CFG14

PA OE Sync Register

Address: 0x400F503E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SYNC3 [7:6]		OE_SYNC2 [5:4]		OE_SYNC1 [3:2]		OE_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	OE_SYNC3	Synchronization options for dsi_to_oe[3] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
5 : 4	OE_SYNC2	Synchronization options for dsi_to_oe[2] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
3 : 2	OE_SYNC1	Synchronization options for dsi_to_oe[1] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
1 : 0	OE_SYNC0	Synchronization options for dsi_to_oe[0] Default Value: 0

21.1.60 UDB_PA3_CFG14 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CONSTANT1:
1

0x3: CONSTANT0:
0

22 PASS MMIO Registers

This section discusses the Programmable Analog Sub System Memory Mapped IO (PASS MMIO) registers. It lists all the registers in mapping tables, in address order.

22.1 Register Details

Register Name	Address
PASS_INTR_CAUSE	0x403F0000
PASS_DSAB_TRIM	0x403F0F00

22.1.1 PASS_INTR_CAUSE

Interrupt cause register

Address: 0x403F0000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CTB1_INT	CTB0_INT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CTB1_INT	CTB1 interrupt pending Default Value: 0
0	CTB0_INT	CTB0 interrupt pending Default Value: 0

22.1.2 PASS_DSAB_TRIM

DSAB Trim bits

Address: 0x403F0F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				IBIAS_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	IBIAS_TRIM	1111=lowest, 0000=highest Default Value: 0

23 Peripheral Interconnect (PERI) Registers

This section discusses the PERI registers. It lists all the registers in mapping tables, in address order.

23.1 Register Details

Register Name	Address
PERI_DIV_CMD	0x40010000
PERI_PCLK_CTL0	0x40010100
PERI_PCLK_CTL1	0x40010104
PERI_PCLK_CTL2	0x40010108
PERI_PCLK_CTL3	0x4001010C
PERI_PCLK_CTL4	0x40010110
PERI_PCLK_CTL5	0x40010114
PERI_PCLK_CTL6	0x40010118
PERI_PCLK_CTL7	0x4001011C
PERI_PCLK_CTL8	0x40010120
PERI_PCLK_CTL9	0x40010124
PERI_PCLK_CTL10	0x40010128
PERI_PCLK_CTL11	0x4001012C
PERI_PCLK_CTL12	0x40010130
PERI_PCLK_CTL13	0x40010134
PERI_PCLK_CTL14	0x40010138
PERI_PCLK_CTL15	0x4001013C
PERI_PCLK_CTL16	0x40010140
PERI_PCLK_CTL17	0x40010144
PERI_PCLK_CTL18	0x40010148
PERI_PCLK_CTL19	0x4001014C
PERI_PCLK_CTL20	0x40010150
PERI_PCLK_CTL21	0x40010154
PERI_PCLK_CTL22	0x40010158
PERI_PCLK_CTL23	0x4001015C
PERI_DIV_16_CTL0	0x40010300
PERI_DIV_16_CTL1	0x40010304

Register Name	Address
PERI_DIV_16_CTL2	0x40010308
PERI_DIV_16_CTL3	0x4001030C
PERI_DIV_16_CTL4	0x40010310
PERI_DIV_16_CTL5	0x40010314
PERI_DIV_16_CTL6	0x40010318
PERI_DIV_16_CTL7	0x4001031C
PERI_DIV_16_CTL8	0x40010320
PERI_DIV_16_CTL9	0x40010324
PERI_DIV_16_CTL10	0x40010328
PERI_DIV_16_CTL11	0x4001032C
PERI_DIV_16_CTL12	0x40010330
PERI_DIV_16_CTL13	0x40010334
PERI_DIV_16_CTL14	0x40010338
PERI_DIV_16_CTL15	0x4001033C
PERI_DIV_16_5_CTL0	0x40010400
PERI_DIV_16_5_CTL1	0x40010404
PERI_DIV_16_5_CTL2	0x40010408
PERI_DIV_16_5_CTL3	0x4001040C
PERI_TR_CTL	0x40010600

23.1.1 PERI_DIV_CMD

Divider command register

Address: 0x40010000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	SEL_TYPE [7:6]		SEL_DIV [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW					
HW Access	R		R					
Name	PA_SEL_TYPE [15:14]		PA_SEL_DIV [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	RW1C	RW1C	None					
Name	ENABLE	DISABLE	None [29:24]					

Bits	Name	Description

23.1.1 PERI_DIV_CMD (continued)

31	ENABLE	Clock divider enable command (mutually exclusive with DISABLE). Typically, SW sets this field to '1' to enable a divider and HW sets this field to '0' to indicate that divider enabling has completed. When a divider is enabled, its integer and fractional (if present) counters are initialized to "0". If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps: 0: Disable the divider using the DIV_CMD.DISABLE field. 1: Configure the divider's DIV_XXX_CTL register. 2: Enable the divider using the DIV_CMD_ENABLE field. The SEL_DIV and SEL_TYPE fields specify which divider is to be enabled. The enabled divider may be phase aligned to either "clk_hf" (typical usage) or to ANY enabled divider. The PA_SEL_DIV and P_SEL_TYPE fields specify the reference divider. The HW sets the ENABLE field to '0' when the enabling is performed and the HW set the DIV_XXX_CTL.EN field of the divider to '1' when the enabling is performed. Note that enabling with phase alignment to a low frequency divider takes time. E.g. To align to a divider that generates a clock of "clk_hf"/n (with n being the integer divider value INT_DIV+1), up to n cycles may be required to perform alignment. Phase alignment to "clk_hf" takes affect immediately. SW can set this field to '0' during phase alignment to abort the enabling process. Default Value: 0
30	DISABLE	Clock divider disable command (mutually exlusive with ENABLE). SW sets this field to '1' and HW sets this field to '0'. The SEL_DIV and SEL_TYPE fields specify which divider is to be disabled. The HW sets the DISABLE field to '0' immediately and the HW sets the DIV_XXX_CTL.EN field of the divider to '0' immediately. Default Value: 0
15 : 14	PA_SEL_TYPE	Specifies the divider type of the divider to which phase alignment is performed for the clock enable command: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
13 : 8	PA_SEL_DIV	(PA_SEL_TYPE, PA_SEL_DIV) pecifies the divider to which phase alignment is performed for the clock enable command. Any enabled divider can be used as reference. This allows all dividers to be aligned with each other, even when they are enabled at different times. If PA_SEL_DIV is "63" and "PA_SEL_TYPE" is "3", "clk_hf" is used as reference. Default Value: 63
7 : 6	SEL_TYPE	Specifies the divider type of the divider on which the command is performed: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
5 : 0	SEL_DIV	(SEL_TYPE, SEL_DIV) specifies the divider on which the command (DISABLE/ENABLE) is performed. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock signal(s) are generated. Default Value: 63

23.1.2 PERI_PCLK_CTL0

Programmable clock control register

Address: 0x40010100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.3 PERI_PCLK_CTL1

Programmable clock control register

Address: 0x40010104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.4 PERI_PCLK_CTL2

Programmable clock control register

Address: 0x40010108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.5 PERI_PCLK_CTL3

Programmable clock control register

Address: 0x4001010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.6 PERI_PCLK_CTL4

Programmable clock control register

Address: 0x40010110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.7 PERI_PCLK_CTL5

Programmable clock control register

Address: 0x40010114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.8 PERI_PCLK_CTL6

Programmable clock control register

Address: 0x40010118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.9 PERI_PCLK_CTL7

Programmable clock control register

Address: 0x4001011C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.10 PERI_PCLK_CTL8

Programmable clock control register

Address: 0x40010120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.11 PERI_PCLK_CTL9

Programmable clock control register

Address: 0x40010124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.12 PERI_PCLK_CTL10

Programmable clock control register

Address: 0x40010128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.13 PERI_PCLK_CTL11

Programmable clock control register

Address: 0x4001012C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.14 PERI_PCLK_CTL12

Programmable clock control register

Address: 0x40010130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.15 PERI_PCLK_CTL13

Programmable clock control register

Address: 0x40010134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.16 PERI_PCLK_CTL14

Programmable clock control register

Address: 0x40010138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.17 PERI_PCLK_CTL15

Programmable clock control register

Address: 0x4001013C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.18 PERI_PCLK_CTL16

Programmable clock control register

Address: 0x40010140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.19 PERI_PCLK_CTL17

Programmable clock control register

Address: 0x40010144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.20 PERI_PCLK_CTL18

Programmable clock control register

Address: 0x40010148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.21 PERI_PCLK_CTL19

Programmable clock control register

Address: 0x4001014C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.22 PERI_PCLK_CTL20

Programmable clock control register

Address: 0x40010150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.23 PERI_PCLK_CTL21

Programmable clock control register

Address: 0x40010154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.24 PERI_PCLK_CTL22

Programmable clock control register

Address: 0x40010158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.25 PERI_PCLK_CTL23

Programmable clock control register

Address: 0x4001015C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one ¡°clk_hf¡ cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

23.1.26 PERI_DIV_16_CTL0

Divider control register (for 16.0 divider)

Address: 0x40010300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.27 PERI_DIV_16_CTL1

Divider control register (for 16.0 divider)

Address: 0x40010304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.28 PERI_DIV_16_CTL2

Divider control register (for 16.0 divider)

Address: 0x40010308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.29 PERI_DIV_16_CTL3

Divider control register (for 16.0 divider)

Address: 0x4001030C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.30 PERI_DIV_16_CTL4

Divider control register (for 16.0 divider)

Address: 0x40010310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.31 PERI_DIV_16_CTL5

Divider control register (for 16.0 divider)

Address: 0x40010314

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.32 PERI_DIV_16_CTL6

Divider control register (for 16.0 divider)

Address: 0x40010318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.33 PERI_DIV_16_CTL7

Divider control register (for 16.0 divider)

Address: 0x4001031C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.34 PERI_DIV_16_CTL8

Divider control register (for 16.0 divider)

Address: 0x40010320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.35 PERI_DIV_16_CTL9

Divider control register (for 16.0 divider)

Address: 0x40010324

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.36 PERI_DIV_16_CTL10

Divider control register (for 16.0 divider)

Address: 0x40010328

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.37 PERI_DIV_16_CTL11

Divider control register (for 16.0 divider)

Address: 0x4001032C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.38 PERI_DIV_16_CTL12

Divider control register (for 16.0 divider)

Address: 0x40010330

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.39 PERI_DIV_16_CTL13

Divider control register (for 16.0 divider)

Address: 0x40010334

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.40 PERI_DIV_16_CTL14

Divider control register (for 16.0 divider)

Address: 0x40010338

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.41 PERI_DIV_16_CTL15

Divider control register (for 16.0 divider)

Address: 0x4001033C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.42 PERI_DIV_16_5_CTL0

Divider control register (for 16.5 divider)

Address: 0x40010400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_hf" cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.42 PERI_DIV_16_5_CTL0 (continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.43 PERI_DIV_16_5_CTL1

Divider control register (for 16.5 divider)

Address: 0x40010404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_hf" cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.43 PERI_DIV_16_5_CTL1 (continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.44 PERI_DIV_16_5_CTL2

Divider control register (for 16.5 divider)

Address: 0x40010408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_hf" cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.44 PERI_DIV_16_5_CTL2 (continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.45 PERI_DIV_16_5_CTL3

Divider control register (for 16.5 divider)

Address: 0x4001040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_hf" cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.45 PERI_DIV_16_5_CTL3 (continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

23.1.46 PERI_TR_CTL

Trigger control register

Address: 0x40010600

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TR_SEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				TR_GROUP [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	TR_COUNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	RW1C	R	None					
Name	TR_ACT	TR_OUT	None [29:24]					

Bits	Name	Description
31	TR_ACT	SW sets this field to '1' by to activate (set to '1') a trigger as identified by TR_SEL and TR_OUT for TR_COUNT cycles. HW sets this field to '0' when the cycle counter is decremented to "0". Note: a TR_COUNT value of 255 is a special case and trigger activation is under direct control of the TR_ACT field (the counter is not decremented). Default Value: 0
30	TR_OUT	Specifies whether trigger activation is for a specific input or ouput trigger of the trigger multiplexer. Activation of a specific input trigger, will result in activation of all output triggers that have the specific input trigger selected through their TR_OUT_CTL.SEL field. Activation of a specific output trigger, will result in activation of the specified TR_SEL output trigger only. '0': TR_SEL selection and trigger activation is for an input trigger to the trigger multiplexer. '1': TR_SEL selection and trigger activation is for an output trigger from the trigger multiplexer. Default Value: 0
23 : 16	TR_COUNT	Amount of cycles a specific trigger is activated. During activation (TR_ACT is '1'), HW decrements this field to "0" using a cycle counter. During activation, SW should not modify this register field. A value of 255 is a special case: HW does NOT decrement this field to "0" and trigger activation is under direct control of TR_ACT: when TR_ACT is '1' the trigger is activated and when TR_ACT is '0' the trigger is deactivated. Default Value: 0

23.1.46 PERI_TR_CTL (continued)

11 : 8	TR_GROUP	Specifies the trigger group. Default Value: 0
6 : 0	TR_SEL	Specifies the activated trigger when TR_ACT is '1'. TR_OUT specifies whether the activated trigger is an input trigger or output trigger to the trigger multiplexer. During activation (TR_ACT is '1'), SW should not modify this register field. If the specified trigger is not present, the trigger activation has no effect. Default Value: 0

24 ROM Table Registers

This section discusses the ROM Table registers. It lists all the registers in mapping tables, in address order.

24.1 Register Details

Register Name	Address
ROMTABLE_ADDR	0xF0000000
ROMTABLE_DID	0xF0000FCC
ROMTABLE_PID4	0xF0000FD0
ROMTABLE_PID5	0xF0000FD4
ROMTABLE_PID6	0xF0000FD8
ROMTABLE_PID7	0xF0000FDC
ROMTABLE_PID0	0xF0000FE0
ROMTABLE_PID1	0xF0000FE4
ROMTABLE_PID2	0xF0000FE8
ROMTABLE_PID3	0xF0000FEC
ROMTABLE_CID0	0xF0000FF0
ROMTABLE_CID1	0xF0000FF4
ROMTABLE_CID2	0xF0000FF8
ROMTABLE_CID3	0xF0000FFC

24.1.1 ROMTABLE_ADDR

Link to Cortex M0 ROM Table.

Address: 0xF0000000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						R	R
Name	None [7:2]						FORMAT_32BIT	PRESENT

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			
HW Access	R				None			
Name	ADDR_OFFSET [15:12]				None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [31:24]							

Bits	Name	Description
31 : 12	ADDR_OFFSET	Address offset of the Cortex-M0 ROM Table base address (0xe00f:f000) wrt. Cypress chip specific ROM Table base address (0xf000:0000). ADDR_OFFSET[19:0] = 0xe00f:f - 0xf000:0 = 0xf00f:f. Default Value: 983295
1	FORMAT_32BIT	ROM Table format: '0: 8-bit format. '1': 32-bit format. Default Value: 1
0	PRESENT	Entry present. Default Value: 1

24.1.2 ROMTABLE_DID

Device Type Identifier register.

Address: 0xF0000FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 1

24.1.3 ROMTABLE_PID4

Peripheral Identification Register 4.

Address: 0xF0000FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	COUNT [7:4]				JEP_CONTINUATION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	COUNT	Size of ROM Table is 2^COUNT * 4 KByte. Default Value: 0
3 : 0	JEP_CONTINUATION	JEP106 continuation code. This value is product specific and specified as part of the product definition in the CPUSS.JEPCONTINUATION parameter. Default Value: Undefined

24.1.4 ROMTABLE_PID5

Peripheral Identification Register 5.

Address: 0xF0000FD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

24.1.5 ROMTABLE_PID6

Peripheral Identification Register 6.

Address: 0xF0000FD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

24.1.6 ROMTABLE_PID7

Peripheral Identification Register 7.

Address: 0xF0000FDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

24.1.7 ROMTABLE_PID0

Peripheral Identification Register 0.

Address: 0xF0000FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	PN_MIN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PN_MIN	JEP106 part number. 4 lsbs of CPUSS.PARTNUMBER parameter. These part numbers are maintained in spec 40-9500. Default Value: Undefined

24.1.8 ROMTABLE_PID1

Peripheral Identification Register 1.

Address: 0xF0000FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	JEPID_MIN [7:4]				PN_MAJ [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	JEPID_MIN	JEP106 vendor id. 4 lsbs of CPUSS.JEPID parameter. This number is maintained in spec 40-9500. Default Value: Undefined
3 : 0	PN_MAJ	JEP106 part number. 4 msbs of CPUSS.PARTNUMBER parameter. These part numbers are maintained in spec 40-9500. Default Value: Undefined

24.1.9 ROMTABLE_PID2

Peripheral Identification Register 2.

Address: 0xF0000FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None	R		
HW Access	R				None	R		
Name	REV [7:4]				None	JEPID_MAJ [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV	Major REVision number (chip specific). Identifies the design iteration of the component. For first tape out: 0x1. This field is implemented in RTL by an ECO-able tie-off structure and is incremented on subsequent tape outs. Default Value: Undefined
2 : 0	JEPID_MAJ	JEP106 vendor id. 4 msbs of CPUSS.JEPID parameter. This number is maintained in spec 40-9500. Default Value: Undefined

24.1.10 ROMTABLE_PID3

Peripheral Identification Register 3.

Address: 0xF0000FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	REV_AND [7:4]				CM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV_AND	Minor REVision number (chip specific). For first tape out: 0x1. This field is implemented in RTL by an ECO-able tie-off structure and is incremented on subsequent tape outs. Default Value: Undefined
3 : 0	CM	Customer modified field. This field is used to track modifications to the original component design as a result of componenet IP reuse. Default Value: 0

24.1.11 ROMTABLE_CID0

Component Identification Register 0.

Address: 0xF0000FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 0 of 4-byte component identification 0xB105:100D. Default Value: 13

24.1.12 ROMTABLE_CID1

Component Identification Register 1.

Address: 0xF0000FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 1 of 4-byte component identification 0xB105:100D. Component class: "ROM Table". Default Value: 16

24.1.13 ROMTABLE_CID2

Component Identification Register 2.

Address: 0xF0000FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 2 of 4-byte component identification 0xB105:100D. Default Value: 5

24.1.14 ROMTABLE_CID3

Component Identification Register 3.

Address: 0xF0000FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 3 of 4-byte component identification 0xB105:100D. Default Value: 177

25 ROUTE Registers

This section discusses the ROUTE registers. It lists all the registers in mapping tables, in address order.

25.1 Register Details

Register Name	Address
UDB_P0_ROUTE_HC0	0x400F3100
UDB_P0_ROUTE_HC1	0x400F3101
UDB_P0_ROUTE_HC2	0x400F3102
UDB_P0_ROUTE_HC3	0x400F3103
UDB_P0_ROUTE_HC4	0x400F3104
UDB_P0_ROUTE_HC5	0x400F3105
UDB_P0_ROUTE_HC6	0x400F3106
UDB_P0_ROUTE_HC7	0x400F3107
UDB_P0_ROUTE_HC8	0x400F3108
UDB_P0_ROUTE_HC9	0x400F3109
UDB_P0_ROUTE_HC10	0x400F310A
UDB_P0_ROUTE_HC11	0x400F310B
UDB_P0_ROUTE_HC12	0x400F310C
UDB_P0_ROUTE_HC13	0x400F310D
UDB_P0_ROUTE_HC14	0x400F310E
UDB_P0_ROUTE_HC15	0x400F310F
UDB_P0_ROUTE_HC16	0x400F3110
UDB_P0_ROUTE_HC17	0x400F3111
UDB_P0_ROUTE_HC18	0x400F3112
UDB_P0_ROUTE_HC19	0x400F3113
UDB_P0_ROUTE_HC20	0x400F3114
UDB_P0_ROUTE_HC21	0x400F3115
UDB_P0_ROUTE_HC22	0x400F3116
UDB_P0_ROUTE_HC23	0x400F3117
UDB_P0_ROUTE_HC24	0x400F3118
UDB_P0_ROUTE_HC25	0x400F3119
UDB_P0_ROUTE_HC26	0x400F311A

Register Name	Address
UDB_P0_ROUTE_HC27	0x400F311B
UDB_P0_ROUTE_HC28	0x400F311C
UDB_P0_ROUTE_HC29	0x400F311D
UDB_P0_ROUTE_HC30	0x400F311E
UDB_P0_ROUTE_HC31	0x400F311F
UDB_P0_ROUTE_HC32	0x400F3120
UDB_P0_ROUTE_HC33	0x400F3121
UDB_P0_ROUTE_HC34	0x400F3122
UDB_P0_ROUTE_HC35	0x400F3123
UDB_P0_ROUTE_HC36	0x400F3124
UDB_P0_ROUTE_HC37	0x400F3125
UDB_P0_ROUTE_HC38	0x400F3126
UDB_P0_ROUTE_HC39	0x400F3127
UDB_P0_ROUTE_HC40	0x400F3128
UDB_P0_ROUTE_HC41	0x400F3129
UDB_P0_ROUTE_HC42	0x400F312A
UDB_P0_ROUTE_HC43	0x400F312B
UDB_P0_ROUTE_HC44	0x400F312C
UDB_P0_ROUTE_HC45	0x400F312D
UDB_P0_ROUTE_HC46	0x400F312E
UDB_P0_ROUTE_HC47	0x400F312F
UDB_P0_ROUTE_HC48	0x400F3130
UDB_P0_ROUTE_HC49	0x400F3131
UDB_P0_ROUTE_HC50	0x400F3132
UDB_P0_ROUTE_HC51	0x400F3133
UDB_P0_ROUTE_HC52	0x400F3134
UDB_P0_ROUTE_HC53	0x400F3135
UDB_P0_ROUTE_HC54	0x400F3136
UDB_P0_ROUTE_HC55	0x400F3137
UDB_P0_ROUTE_HC56	0x400F3138
UDB_P0_ROUTE_HC57	0x400F3139
UDB_P0_ROUTE_HC58	0x400F313A
UDB_P0_ROUTE_HC59	0x400F313B
UDB_P0_ROUTE_HC60	0x400F313C
UDB_P0_ROUTE_HC61	0x400F313D
UDB_P0_ROUTE_HC62	0x400F313E
UDB_P0_ROUTE_HC63	0x400F313F
UDB_P0_ROUTE_HC64	0x400F3140
UDB_P0_ROUTE_HC65	0x400F3141
UDB_P0_ROUTE_HC66	0x400F3142
UDB_P0_ROUTE_HC67	0x400F3143
UDB_P0_ROUTE_HC68	0x400F3144

Register Name	Address
UDB_P0_ROUTE_HC69	0x400F3145
UDB_P0_ROUTE_HC70	0x400F3146
UDB_P0_ROUTE_HC71	0x400F3147
UDB_P0_ROUTE_HC72	0x400F3148
UDB_P0_ROUTE_HC73	0x400F3149
UDB_P0_ROUTE_HC74	0x400F314A
UDB_P0_ROUTE_HC75	0x400F314B
UDB_P0_ROUTE_HC76	0x400F314C
UDB_P0_ROUTE_HC77	0x400F314D
UDB_P0_ROUTE_HC78	0x400F314E
UDB_P0_ROUTE_HC79	0x400F314F
UDB_P0_ROUTE_HC80	0x400F3150
UDB_P0_ROUTE_HC81	0x400F3151
UDB_P0_ROUTE_HC82	0x400F3152
UDB_P0_ROUTE_HC83	0x400F3153
UDB_P0_ROUTE_HC84	0x400F3154
UDB_P0_ROUTE_HC85	0x400F3155
UDB_P0_ROUTE_HC86	0x400F3156
UDB_P0_ROUTE_HC87	0x400F3157
UDB_P0_ROUTE_HC88	0x400F3158
UDB_P0_ROUTE_HC89	0x400F3159
UDB_P0_ROUTE_HC90	0x400F315A
UDB_P0_ROUTE_HC91	0x400F315B
UDB_P0_ROUTE_HC92	0x400F315C
UDB_P0_ROUTE_HC93	0x400F315D
UDB_P0_ROUTE_HC94	0x400F315E
UDB_P0_ROUTE_HC95	0x400F315F
UDB_P0_ROUTE_HC96	0x400F3160
UDB_P0_ROUTE_HC97	0x400F3161
UDB_P0_ROUTE_HC98	0x400F3162
UDB_P0_ROUTE_HC99	0x400F3163
UDB_P0_ROUTE_HC100	0x400F3164
UDB_P0_ROUTE_HC101	0x400F3165
UDB_P0_ROUTE_HC102	0x400F3166
UDB_P0_ROUTE_HC103	0x400F3167
UDB_P0_ROUTE_HC104	0x400F3168
UDB_P0_ROUTE_HC105	0x400F3169
UDB_P0_ROUTE_HC106	0x400F316A
UDB_P0_ROUTE_HC107	0x400F316B
UDB_P0_ROUTE_HC108	0x400F316C
UDB_P0_ROUTE_HC109	0x400F316D
UDB_P0_ROUTE_HC110	0x400F316E

Register Name	Address
UDB_P0_ROUTE_HC111	0x400F316F
UDB_P0_ROUTE_HC112	0x400F3170
UDB_P0_ROUTE_HC113	0x400F3171
UDB_P0_ROUTE_HC114	0x400F3172
UDB_P0_ROUTE_HC115	0x400F3173
UDB_P0_ROUTE_HC116	0x400F3174
UDB_P0_ROUTE_HC117	0x400F3175
UDB_P0_ROUTE_HC118	0x400F3176
UDB_P0_ROUTE_HC119	0x400F3177
UDB_P0_ROUTE_HC120	0x400F3178
UDB_P0_ROUTE_HC121	0x400F3179
UDB_P0_ROUTE_HC122	0x400F317A
UDB_P0_ROUTE_HC123	0x400F317B
UDB_P0_ROUTE_HC124	0x400F317C
UDB_P0_ROUTE_HC125	0x400F317D
UDB_P0_ROUTE_HC126	0x400F317E
UDB_P0_ROUTE_HC127	0x400F317F
UDB_P0_ROUTE_HV_L0	0x400F3180
UDB_P0_ROUTE_HV_L1	0x400F3181
UDB_P0_ROUTE_HV_L2	0x400F3182
UDB_P0_ROUTE_HV_L3	0x400F3183
UDB_P0_ROUTE_HV_L4	0x400F3184
UDB_P0_ROUTE_HV_L5	0x400F3185
UDB_P0_ROUTE_HV_L6	0x400F3186
UDB_P0_ROUTE_HV_L7	0x400F3187
UDB_P0_ROUTE_HV_L8	0x400F3188
UDB_P0_ROUTE_HV_L9	0x400F3189
UDB_P0_ROUTE_HV_L10	0x400F318A
UDB_P0_ROUTE_HV_L11	0x400F318B
UDB_P0_ROUTE_HV_L12	0x400F318C
UDB_P0_ROUTE_HV_L13	0x400F318D
UDB_P0_ROUTE_HV_L14	0x400F318E
UDB_P0_ROUTE_HV_L15	0x400F318F
UDB_P0_ROUTE_HS0	0x400F3190
UDB_P0_ROUTE_HS1	0x400F3191
UDB_P0_ROUTE_HS2	0x400F3192
UDB_P0_ROUTE_HS3	0x400F3193
UDB_P0_ROUTE_HS4	0x400F3194
UDB_P0_ROUTE_HS5	0x400F3195
UDB_P0_ROUTE_HS6	0x400F3196
UDB_P0_ROUTE_HS7	0x400F3197
UDB_P0_ROUTE_HS8	0x400F3198

Register Name	Address
UDB_P0_ROUTE_HS9	0x400F3199
UDB_P0_ROUTE_HS10	0x400F319A
UDB_P0_ROUTE_HS11	0x400F319B
UDB_P0_ROUTE_HS12	0x400F319C
UDB_P0_ROUTE_HS13	0x400F319D
UDB_P0_ROUTE_HS14	0x400F319E
UDB_P0_ROUTE_HS15	0x400F319F
UDB_P0_ROUTE_HS16	0x400F31A0
UDB_P0_ROUTE_HS17	0x400F31A1
UDB_P0_ROUTE_HS18	0x400F31A2
UDB_P0_ROUTE_HS19	0x400F31A3
UDB_P0_ROUTE_HS20	0x400F31A4
UDB_P0_ROUTE_HS21	0x400F31A5
UDB_P0_ROUTE_HS22	0x400F31A6
UDB_P0_ROUTE_HS23	0x400F31A7
UDB_P0_ROUTE_HV_R0	0x400F31A8
UDB_P0_ROUTE_HV_R1	0x400F31A9
UDB_P0_ROUTE_HV_R2	0x400F31AA
UDB_P0_ROUTE_HV_R3	0x400F31AB
UDB_P0_ROUTE_HV_R4	0x400F31AC
UDB_P0_ROUTE_HV_R5	0x400F31AD
UDB_P0_ROUTE_HV_R6	0x400F31AE
UDB_P0_ROUTE_HV_R7	0x400F31AF
UDB_P0_ROUTE_HV_R8	0x400F31B0
UDB_P0_ROUTE_HV_R9	0x400F31B1
UDB_P0_ROUTE_HV_R10	0x400F31B2
UDB_P0_ROUTE_HV_R11	0x400F31B3
UDB_P0_ROUTE_HV_R12	0x400F31B4
UDB_P0_ROUTE_HV_R13	0x400F31B5
UDB_P0_ROUTE_HV_R14	0x400F31B6
UDB_P0_ROUTE_HV_R15	0x400F31B7
UDB_P0_ROUTE_PLD0IN0	0x400F31C0
UDB_P0_ROUTE_PLD0IN1	0x400F31C2
UDB_P0_ROUTE_PLD0IN2	0x400F31C4
UDB_P0_ROUTE_PLD1IN0	0x400F31CA
UDB_P0_ROUTE_PLD1IN1	0x400F31CC
UDB_P0_ROUTE_PLD1IN2	0x400F31CE
UDB_P0_ROUTE_DPIN0	0x400F31D0
UDB_P0_ROUTE_DPIN1	0x400F31D2
UDB_P0_ROUTE_SCIN	0x400F31D6
UDB_P0_ROUTE_SCIOIN	0x400F31D8
UDB_P0_ROUTE_RCIN	0x400F31DE

Register Name	Address
UDB_P0_ROUTE_VS0	0x400F31E0
UDB_P0_ROUTE_VS1	0x400F31E2
UDB_P0_ROUTE_VS2	0x400F31E4
UDB_P0_ROUTE_VS3	0x400F31E6
UDB_P0_ROUTE_VS4	0x400F31E8
UDB_P0_ROUTE_VS5	0x400F31EA
UDB_P0_ROUTE_VS6	0x400F31EC
UDB_P0_ROUTE_VS7	0x400F31EE
UDB_P1_ROUTE_HC0	0x400F3300
UDB_P1_ROUTE_HC1	0x400F3301
UDB_P1_ROUTE_HC2	0x400F3302
UDB_P1_ROUTE_HC3	0x400F3303
UDB_P1_ROUTE_HC4	0x400F3304
UDB_P1_ROUTE_HC5	0x400F3305
UDB_P1_ROUTE_HC6	0x400F3306
UDB_P1_ROUTE_HC7	0x400F3307
UDB_P1_ROUTE_HC8	0x400F3308
UDB_P1_ROUTE_HC9	0x400F3309
UDB_P1_ROUTE_HC10	0x400F330A
UDB_P1_ROUTE_HC11	0x400F330B
UDB_P1_ROUTE_HC12	0x400F330C
UDB_P1_ROUTE_HC13	0x400F330D
UDB_P1_ROUTE_HC14	0x400F330E
UDB_P1_ROUTE_HC15	0x400F330F
UDB_P1_ROUTE_HC16	0x400F3310
UDB_P1_ROUTE_HC17	0x400F3311
UDB_P1_ROUTE_HC18	0x400F3312
UDB_P1_ROUTE_HC19	0x400F3313
UDB_P1_ROUTE_HC20	0x400F3314
UDB_P1_ROUTE_HC21	0x400F3315
UDB_P1_ROUTE_HC22	0x400F3316
UDB_P1_ROUTE_HC23	0x400F3317
UDB_P1_ROUTE_HC24	0x400F3318
UDB_P1_ROUTE_HC25	0x400F3319
UDB_P1_ROUTE_HC26	0x400F331A
UDB_P1_ROUTE_HC27	0x400F331B
UDB_P1_ROUTE_HC28	0x400F331C
UDB_P1_ROUTE_HC29	0x400F331D
UDB_P1_ROUTE_HC30	0x400F331E
UDB_P1_ROUTE_HC31	0x400F331F
UDB_P1_ROUTE_HC32	0x400F3320
UDB_P1_ROUTE_HC33	0x400F3321

Register Name	Address
UDB_P1_ROUTE_HC34	0x400F3322
UDB_P1_ROUTE_HC35	0x400F3323
UDB_P1_ROUTE_HC36	0x400F3324
UDB_P1_ROUTE_HC37	0x400F3325
UDB_P1_ROUTE_HC38	0x400F3326
UDB_P1_ROUTE_HC39	0x400F3327
UDB_P1_ROUTE_HC40	0x400F3328
UDB_P1_ROUTE_HC41	0x400F3329
UDB_P1_ROUTE_HC42	0x400F332A
UDB_P1_ROUTE_HC43	0x400F332B
UDB_P1_ROUTE_HC44	0x400F332C
UDB_P1_ROUTE_HC45	0x400F332D
UDB_P1_ROUTE_HC46	0x400F332E
UDB_P1_ROUTE_HC47	0x400F332F
UDB_P1_ROUTE_HC48	0x400F3330
UDB_P1_ROUTE_HC49	0x400F3331
UDB_P1_ROUTE_HC50	0x400F3332
UDB_P1_ROUTE_HC51	0x400F3333
UDB_P1_ROUTE_HC52	0x400F3334
UDB_P1_ROUTE_HC53	0x400F3335
UDB_P1_ROUTE_HC54	0x400F3336
UDB_P1_ROUTE_HC55	0x400F3337
UDB_P1_ROUTE_HC56	0x400F3338
UDB_P1_ROUTE_HC57	0x400F3339
UDB_P1_ROUTE_HC58	0x400F333A
UDB_P1_ROUTE_HC59	0x400F333B
UDB_P1_ROUTE_HC60	0x400F333C
UDB_P1_ROUTE_HC61	0x400F333D
UDB_P1_ROUTE_HC62	0x400F333E
UDB_P1_ROUTE_HC63	0x400F333F
UDB_P1_ROUTE_HC64	0x400F3340
UDB_P1_ROUTE_HC65	0x400F3341
UDB_P1_ROUTE_HC66	0x400F3342
UDB_P1_ROUTE_HC67	0x400F3343
UDB_P1_ROUTE_HC68	0x400F3344
UDB_P1_ROUTE_HC69	0x400F3345
UDB_P1_ROUTE_HC70	0x400F3346
UDB_P1_ROUTE_HC71	0x400F3347
UDB_P1_ROUTE_HC72	0x400F3348
UDB_P1_ROUTE_HC73	0x400F3349
UDB_P1_ROUTE_HC74	0x400F334A
UDB_P1_ROUTE_HC75	0x400F334B

Register Name	Address
UDB_P1_ROUTE_HC76	0x400F334C
UDB_P1_ROUTE_HC77	0x400F334D
UDB_P1_ROUTE_HC78	0x400F334E
UDB_P1_ROUTE_HC79	0x400F334F
UDB_P1_ROUTE_HC80	0x400F3350
UDB_P1_ROUTE_HC81	0x400F3351
UDB_P1_ROUTE_HC82	0x400F3352
UDB_P1_ROUTE_HC83	0x400F3353
UDB_P1_ROUTE_HC84	0x400F3354
UDB_P1_ROUTE_HC85	0x400F3355
UDB_P1_ROUTE_HC86	0x400F3356
UDB_P1_ROUTE_HC87	0x400F3357
UDB_P1_ROUTE_HC88	0x400F3358
UDB_P1_ROUTE_HC89	0x400F3359
UDB_P1_ROUTE_HC90	0x400F335A
UDB_P1_ROUTE_HC91	0x400F335B
UDB_P1_ROUTE_HC92	0x400F335C
UDB_P1_ROUTE_HC93	0x400F335D
UDB_P1_ROUTE_HC94	0x400F335E
UDB_P1_ROUTE_HC95	0x400F335F
UDB_P1_ROUTE_HC96	0x400F3360
UDB_P1_ROUTE_HC97	0x400F3361
UDB_P1_ROUTE_HC98	0x400F3362
UDB_P1_ROUTE_HC99	0x400F3363
UDB_P1_ROUTE_HC100	0x400F3364
UDB_P1_ROUTE_HC101	0x400F3365
UDB_P1_ROUTE_HC102	0x400F3366
UDB_P1_ROUTE_HC103	0x400F3367
UDB_P1_ROUTE_HC104	0x400F3368
UDB_P1_ROUTE_HC105	0x400F3369
UDB_P1_ROUTE_HC106	0x400F336A
UDB_P1_ROUTE_HC107	0x400F336B
UDB_P1_ROUTE_HC108	0x400F336C
UDB_P1_ROUTE_HC109	0x400F336D
UDB_P1_ROUTE_HC110	0x400F336E
UDB_P1_ROUTE_HC111	0x400F336F
UDB_P1_ROUTE_HC112	0x400F3370
UDB_P1_ROUTE_HC113	0x400F3371
UDB_P1_ROUTE_HC114	0x400F3372
UDB_P1_ROUTE_HC115	0x400F3373
UDB_P1_ROUTE_HC116	0x400F3374
UDB_P1_ROUTE_HC117	0x400F3375

Register Name	Address
UDB_P1_ROUTE_HC118	0x400F3376
UDB_P1_ROUTE_HC119	0x400F3377
UDB_P1_ROUTE_HC120	0x400F3378
UDB_P1_ROUTE_HC121	0x400F3379
UDB_P1_ROUTE_HC122	0x400F337A
UDB_P1_ROUTE_HC123	0x400F337B
UDB_P1_ROUTE_HC124	0x400F337C
UDB_P1_ROUTE_HC125	0x400F337D
UDB_P1_ROUTE_HC126	0x400F337E
UDB_P1_ROUTE_HC127	0x400F337F
UDB_P1_ROUTE_HV_L0	0x400F3380
UDB_P1_ROUTE_HV_L1	0x400F3381
UDB_P1_ROUTE_HV_L2	0x400F3382
UDB_P1_ROUTE_HV_L3	0x400F3383
UDB_P1_ROUTE_HV_L4	0x400F3384
UDB_P1_ROUTE_HV_L5	0x400F3385
UDB_P1_ROUTE_HV_L6	0x400F3386
UDB_P1_ROUTE_HV_L7	0x400F3387
UDB_P1_ROUTE_HV_L8	0x400F3388
UDB_P1_ROUTE_HV_L9	0x400F3389
UDB_P1_ROUTE_HV_L10	0x400F338A
UDB_P1_ROUTE_HV_L11	0x400F338B
UDB_P1_ROUTE_HV_L12	0x400F338C
UDB_P1_ROUTE_HV_L13	0x400F338D
UDB_P1_ROUTE_HV_L14	0x400F338E
UDB_P1_ROUTE_HV_L15	0x400F338F
UDB_P1_ROUTE_HS0	0x400F3390
UDB_P1_ROUTE_HS1	0x400F3391
UDB_P1_ROUTE_HS2	0x400F3392
UDB_P1_ROUTE_HS3	0x400F3393
UDB_P1_ROUTE_HS4	0x400F3394
UDB_P1_ROUTE_HS5	0x400F3395
UDB_P1_ROUTE_HS6	0x400F3396
UDB_P1_ROUTE_HS7	0x400F3397
UDB_P1_ROUTE_HS8	0x400F3398
UDB_P1_ROUTE_HS9	0x400F3399
UDB_P1_ROUTE_HS10	0x400F339A
UDB_P1_ROUTE_HS11	0x400F339B
UDB_P1_ROUTE_HS12	0x400F339C
UDB_P1_ROUTE_HS13	0x400F339D
UDB_P1_ROUTE_HS14	0x400F339E
UDB_P1_ROUTE_HS15	0x400F339F

Register Name	Address
UDB_P1_ROUTE_HS16	0x400F33A0
UDB_P1_ROUTE_HS17	0x400F33A1
UDB_P1_ROUTE_HS18	0x400F33A2
UDB_P1_ROUTE_HS19	0x400F33A3
UDB_P1_ROUTE_HS20	0x400F33A4
UDB_P1_ROUTE_HS21	0x400F33A5
UDB_P1_ROUTE_HS22	0x400F33A6
UDB_P1_ROUTE_HS23	0x400F33A7
UDB_P1_ROUTE_HV_R0	0x400F33A8
UDB_P1_ROUTE_HV_R1	0x400F33A9
UDB_P1_ROUTE_HV_R2	0x400F33AA
UDB_P1_ROUTE_HV_R3	0x400F33AB
UDB_P1_ROUTE_HV_R4	0x400F33AC
UDB_P1_ROUTE_HV_R5	0x400F33AD
UDB_P1_ROUTE_HV_R6	0x400F33AE
UDB_P1_ROUTE_HV_R7	0x400F33AF
UDB_P1_ROUTE_HV_R8	0x400F33B0
UDB_P1_ROUTE_HV_R9	0x400F33B1
UDB_P1_ROUTE_HV_R10	0x400F33B2
UDB_P1_ROUTE_HV_R11	0x400F33B3
UDB_P1_ROUTE_HV_R12	0x400F33B4
UDB_P1_ROUTE_HV_R13	0x400F33B5
UDB_P1_ROUTE_HV_R14	0x400F33B6
UDB_P1_ROUTE_HV_R15	0x400F33B7
UDB_P1_ROUTE_PLD0IN0	0x400F33C0
UDB_P1_ROUTE_PLD0IN1	0x400F33C2
UDB_P1_ROUTE_PLD0IN2	0x400F33C4
UDB_P1_ROUTE_PLD1IN0	0x400F33CA
UDB_P1_ROUTE_PLD1IN1	0x400F33CC
UDB_P1_ROUTE_PLD1IN2	0x400F33CE
UDB_P1_ROUTE_DPIN0	0x400F33D0
UDB_P1_ROUTE_DPIN1	0x400F33D2
UDB_P1_ROUTE_SCIN	0x400F33D6
UDB_P1_ROUTE_SCIOIN	0x400F33D8
UDB_P1_ROUTE_RCIN	0x400F33DE
UDB_P1_ROUTE_VS0	0x400F33E0
UDB_P1_ROUTE_VS1	0x400F33E2
UDB_P1_ROUTE_VS2	0x400F33E4
UDB_P1_ROUTE_VS3	0x400F33E6
UDB_P1_ROUTE_VS4	0x400F33E8
UDB_P1_ROUTE_VS5	0x400F33EA
UDB_P1_ROUTE_VS6	0x400F33EC

Register Name	Address
UDB_P1_ROUTE_VS7	0x400F33EE

25.1.1 UDB_P0_ROUTE_HC0

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.2 UDB_P0_ROUTE_HC1

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3101

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.3 UDB_P0_ROUTE_HC2

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3102

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.4 UDB_P0_ROUTE_HC3

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3103

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.5 UDB_P0_ROUTE_HC4

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.6 UDB_P0_ROUTE_HC5

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3105

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.7 UDB_P0_ROUTE_HC6

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3106

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.8 UDB_P0_ROUTE_HC7

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3107

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.9 UDB_P0_ROUTE_HC8

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.10 UDB_P0_ROUTE_HC9

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3109

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.11 UDB_P0_ROUTE_HC10

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F310A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.12 UDB_P0_ROUTE_HC11

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F310B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.13 UDB_P0_ROUTE_HC12

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F310C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.14 UDB_P0_ROUTE_HC13

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F310D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.15 UDB_P0_ROUTE_HC14

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F310E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.16 UDB_P0_ROUTE_HC15

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F310F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.17 UDB_P0_ROUTE_HC16

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.18 UDB_P0_ROUTE_HC17

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3111

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.19 UDB_P0_ROUTE_HC18

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3112

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.20 UDB_P0_ROUTE_HC19

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3113

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.21 UDB_P0_ROUTE_HC20

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.22 UDB_P0_ROUTE_HC21

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3115

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.23 UDB_P0_ROUTE_HC22

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3116

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.24 UDB_P0_ROUTE_HC23

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3117

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.25 UDB_P0_ROUTE_HC24

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.26 UDB_P0_ROUTE_HC25

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3119

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.27 UDB_P0_ROUTE_HC26

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F311A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.28 UDB_P0_ROUTE_HC27

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F311B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.29 UDB_P0_ROUTE_HC28

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F311C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.30 UDB_P0_ROUTE_HC29

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F311D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.31 UDB_P0_ROUTE_HC30

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F311E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.32 UDB_P0_ROUTE_HC31

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F311F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.33 UDB_P0_ROUTE_HC32

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.34 UDB_P0_ROUTE_HC33

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3121

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.35 UDB_P0_ROUTE_HC34

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3122

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.36 UDB_P0_ROUTE_HC35

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3123

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.37 UDB_P0_ROUTE_HC36

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.38 UDB_P0_ROUTE_HC37

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3125

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.39 UDB_P0_ROUTE_HC38

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3126

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.40 UDB_P0_ROUTE_HC39

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3127

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.41 UDB_P0_ROUTE_HC40

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.42 UDB_P0_ROUTE_HC41

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3129

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.43 UDB_P0_ROUTE_HC42

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F312A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.44 UDB_P0_ROUTE_HC43

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F312B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.45 UDB_P0_ROUTE_HC44

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F312C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.46 UDB_P0_ROUTE_HC45

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F312D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.47 UDB_P0_ROUTE_HC46

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F312E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.48 UDB_P0_ROUTE_HC47

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F312F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.49 UDB_P0_ROUTE_HC48

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.50 UDB_P0_ROUTE_HC49

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3131

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.51 UDB_P0_ROUTE_HC50

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3132

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.52 UDB_P0_ROUTE_HC51

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3133

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.53 UDB_P0_ROUTE_HC52

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.54 UDB_P0_ROUTE_HC53

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3135

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.55 UDB_P0_ROUTE_HC54

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3136

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.56 UDB_P0_ROUTE_HC55

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3137

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.57 UDB_P0_ROUTE_HC56

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.58 UDB_P0_ROUTE_HC57

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3139

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.59 UDB_P0_ROUTE_HC58

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F313A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.60 UDB_P0_ROUTE_HC59

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F313B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.61 UDB_P0_ROUTE_HC60

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F313C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.62 UDB_P0_ROUTE_HC61

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F313D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.63 UDB_P0_ROUTE_HC62

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F313E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.64 UDB_P0_ROUTE_HC63

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F313F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.65 UDB_P0_ROUTE_HC64

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.66 UDB_P0_ROUTE_HC65

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3141

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.67 UDB_P0_ROUTE_HC66

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3142

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.68 UDB_P0_ROUTE_HC67

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3143

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.69 UDB_P0_ROUTE_HC68

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.70 UDB_P0_ROUTE_HC69

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3145

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.71 UDB_P0_ROUTE_HC70

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3146

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.72 UDB_P0_ROUTE_HC71

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3147

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.73 UDB_P0_ROUTE_HC72

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.74 UDB_P0_ROUTE_HC73

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3149

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.75 UDB_P0_ROUTE_HC74

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F314A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.76 UDB_P0_ROUTE_HC75

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F314B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.77 UDB_P0_ROUTE_HC76

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F314C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.78 UDB_P0_ROUTE_HC77

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F314D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.79 UDB_P0_ROUTE_HC78

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F314E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.80 UDB_P0_ROUTE_HC79

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F314F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.81 UDB_P0_ROUTE_HC80

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.82 UDB_P0_ROUTE_HC81

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3151

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.83 UDB_P0_ROUTE_HC82

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3152

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.84 UDB_P0_ROUTE_HC83

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3153

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.85 UDB_P0_ROUTE_HC84

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.86 UDB_P0_ROUTE_HC85

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3155

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.87 UDB_P0_ROUTE_HC86

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3156

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.88 UDB_P0_ROUTE_HC87

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3157

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.89 UDB_P0_ROUTE_HC88

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.90 UDB_P0_ROUTE_HC89

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3159

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.91 UDB_P0_ROUTE_HC90

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F315A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.92 UDB_P0_ROUTE_HC91

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F315B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.93 UDB_P0_ROUTE_HC92

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F315C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.94 UDB_P0_ROUTE_HC93

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F315D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.95 UDB_P0_ROUTE_HC94

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F315E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.96 UDB_P0_ROUTE_HC95

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F315F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.97 UDB_P0_ROUTE_HC96

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.98 UDB_P0_ROUTE_HC97

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3161

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.99 UDB_P0_ROUTE_HC98

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3162

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.100 UDB_P0_ROUTE_HC99

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3163

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.101 UDB_P0_ROUTE_HC100

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.102 UDB_P0_ROUTE_HC101

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3165

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.103 UDB_P0_ROUTE_HC102

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3166

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.104 UDB_P0_ROUTE_HC103

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3167

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.105 UDB_P0_ROUTE_HC104

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3168

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.106 UDB_P0_ROUTE_HC105

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3169

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.107 UDB_P0_ROUTE_HC106

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F316A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.108 UDB_P0_ROUTE_HC107

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F316B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.109 UDB_P0_ROUTE_HC108

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F316C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.110 UDB_P0_ROUTE_HC109

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F316D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.111 UDB_P0_ROUTE_HC110

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F316E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.112 UDB_P0_ROUTE_HC111

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F316F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.113 UDB_P0_ROUTE_HC112

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.114 UDB_P0_ROUTE_HC113

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3171

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.115 UDB_P0_ROUTE_HC114

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3172

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.116 UDB_P0_ROUTE_HC115

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3173

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.117 UDB_P0_ROUTE_HC116

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.118 UDB_P0_ROUTE_HC117

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3175

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.119 UDB_P0_ROUTE_HC118

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3176

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.120 UDB_P0_ROUTE_HC119

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3177

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.121 UDB_P0_ROUTE_HC120

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.122 UDB_P0_ROUTE_HC121

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3179

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.123 UDB_P0_ROUTE_HC122

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F317A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.124 UDB_P0_ROUTE_HC123

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F317B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.125 UDB_P0_ROUTE_HC124

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F317C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.126 UDB_P0_ROUTE_HC125

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F317D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.127 UDB_P0_ROUTE_HC126

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F317E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.128 UDB_P0_ROUTE_HC127

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F317F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.129 UDB_P0_ROUTE_HV_L0

UDB Channel HV Tile Configuration; Left

Address: 0x400F3180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.130 UDB_P0_ROUTE_HV_L1

UDB Channel HV Tile Configuration; Left

Address: 0x400F3181

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.131 UDB_P0_ROUTE_HV_L2

UDB Channel HV Tile Configuration; Left

Address: 0x400F3182

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.132 UDB_P0_ROUTE_HV_L3

UDB Channel HV Tile Configuration; Left

Address: 0x400F3183

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.133 UDB_P0_ROUTE_HV_L4

UDB Channel HV Tile Configuration; Left

Address: 0x400F3184

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.134 UDB_P0_ROUTE_HV_L5

UDB Channel HV Tile Configuration; Left

Address: 0x400F3185

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.135 UDB_P0_ROUTE_HV_L6

UDB Channel HV Tile Configuration; Left

Address: 0x400F3186

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.136 UDB_P0_ROUTE_HV_L7

UDB Channel HV Tile Configuration; Left

Address: 0x400F3187

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.137 UDB_P0_ROUTE_HV_L8

UDB Channel HV Tile Configuration; Left

Address: 0x400F3188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.138 UDB_P0_ROUTE_HV_L9

UDB Channel HV Tile Configuration; Left

Address: 0x400F3189

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.139 UDB_P0_ROUTE_HV_L10

UDB Channel HV Tile Configuration; Left

Address: 0x400F318A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.140 UDB_P0_ROUTE_HV_L11

UDB Channel HV Tile Configuration; Left

Address: 0x400F318B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.141 UDB_P0_ROUTE_HV_L12

UDB Channel HV Tile Configuration; Left

Address: 0x400F318C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.142 UDB_P0_ROUTE_HV_L13

UDB Channel HV Tile Configuration; Left

Address: 0x400F318D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.143 UDB_P0_ROUTE_HV_L14

UDB Channel HV Tile Configuration; Left

Address: 0x400F318E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.144 UDB_P0_ROUTE_HV_L15

UDB Channel HV Tile Configuration; Left

Address: 0x400F318F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.145 UDB_P0_ROUTE_HS0

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.146 UDB_P0_ROUTE_HS1

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3191

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.147 UDB_P0_ROUTE_HS2

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3192

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.148 UDB_P0_ROUTE_HS3

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3193

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.149 UDB_P0_ROUTE_HS4

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3194

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.150 UDB_P0_ROUTE_HS5

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3195

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.151 UDB_P0_ROUTE_HS6

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3196

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.152 UDB_P0_ROUTE_HS7

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3197

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.153 UDB_P0_ROUTE_HS8

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3198

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.154 UDB_P0_ROUTE_HS9

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3199

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.155 UDB_P0_ROUTE_HS10

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F319A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.156 UDB_P0_ROUTE_HS11

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F319B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.157 UDB_P0_ROUTE_HS12

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F319C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.158 UDB_P0_ROUTE_HS13

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F319D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.159 UDB_P0_ROUTE_HS14

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F319E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.160 UDB_P0_ROUTE_HS15

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F319F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.161 UDB_P0_ROUTE_HS16

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F31A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.162 UDB_P0_ROUTE_HS17

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F31A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.163 UDB_P0_ROUTE_HS18

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F31A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.164 UDB_P0_ROUTE_HS19

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F31A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.165 UDB_P0_ROUTE_HS20

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F31A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.166 UDB_P0_ROUTE_HS21

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F31A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.167 UDB_P0_ROUTE_HS22

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F31A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.168 UDB_P0_ROUTE_HS23

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F31A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.169 UDB_P0_ROUTE_HV_R0

UDB Channel HV Tile Configuration; Right

Address: 0x400F31A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.170 UDB_P0_ROUTE_HV_R1

UDB Channel HV Tile Configuration; Right

Address: 0x400F31A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.171 UDB_P0_ROUTE_HV_R2

UDB Channel HV Tile Configuration; Right

Address: 0x400F31AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.172 UDB_P0_ROUTE_HV_R3

UDB Channel HV Tile Configuration; Right

Address: 0x400F31AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.173 UDB_P0_ROUTE_HV_R4

UDB Channel HV Tile Configuration; Right

Address: 0x400F31AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.174 UDB_P0_ROUTE_HV_R5

UDB Channel HV Tile Configuration; Right

Address: 0x400F31AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.175 UDB_P0_ROUTE_HV_R6

UDB Channel HV Tile Configuration; Right

Address: 0x400F31AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.176 UDB_P0_ROUTE_HV_R7

UDB Channel HV Tile Configuration; Right

Address: 0x400F31AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.177 UDB_P0_ROUTE_HV_R8

UDB Channel HV Tile Configuration; Right

Address: 0x400F31B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.178 UDB_P0_ROUTE_HV_R9

UDB Channel HV Tile Configuration; Right

Address: 0x400F31B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.179 UDB_P0_ROUTE_HV_R10

UDB Channel HV Tile Configuration; Right

Address: 0x400F31B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.180 UDB_P0_ROUTE_HV_R11

UDB Channel HV Tile Configuration; Right

Address: 0x400F31B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.181 UDB_P0_ROUTE_HV_R12

UDB Channel HV Tile Configuration; Right

Address: 0x400F31B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.182 UDB_P0_ROUTE_HV_R13

UDB Channel HV Tile Configuration; Right

Address: 0x400F31B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.183 UDB_P0_ROUTE_HV_R14

UDB Channel HV Tile Configuration; Right

Address: 0x400F31B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.184 UDB_P0_ROUTE_HV_R15

UDB Channel HV Tile Configuration; Right

Address: 0x400F31B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.185 UDB_P0_ROUTE_PLD0IN0

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F31C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.186 UDB_P0_ROUTE_PLD0IN1

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F31C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.187 UDB_P0_ROUTE_PLD0IN2

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F31C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.188 UDB_P0_ROUTE_PLD1IN0

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F31CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.189 UDB_P0_ROUTE_PLD1IN1

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F31CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.190 UDB_P0_ROUTE_PLD1IN2

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F31CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.191 UDB_P0_ROUTE_DPIN0

UDB Channel PI Tile Configuration; Datapath Input

Address: 0x400F31D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.192 UDB_P0_ROUTE_DPIN1

UDB Channel PI Tile Configuration; Datapath Input

Address: 0x400F31D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		None	
HW Access	None		R		R		None	
Name	None [7:6]		PI_BOT2 [5:4]		PI_TOP2 [3:2]		None [1:0]	

Bits	Name	Description
5 : 4	PI_BOT2	RAM configuration bits (2) for BOTTOM UDB port interface configuration Default Value: X
3 : 2	PI_TOP2	RAM configuration bits (2) for TOP UDB port interface configuration Default Value: X

25.1.193 UDB_P0_ROUTE_SCIN

UDB Channel PI Tile Configuration; Status / Control Blocks Input Control

Address: 0x400F31D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.194 UDB_P0_ROUTE_SCIOIN

UDB Channel PI Tile Configuration; Status / Control Blocks Input / Output Control

Address: 0x400F31D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.195 UDB_P0_ROUTE_RCIN

UDB Channel PI Tile Configuration; Reset and Clock Blocks Input Control

Address: 0x400F31DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.196 UDB_P0_ROUTE_VS0

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F31E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

25.1.197 UDB_P0_ROUTE_VS1

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F31E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

25.1.198 UDB_P0_ROUTE_VS2

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F31E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

25.1.199 UDB_P0_ROUTE_VS3

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F31E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

25.1.200 UDB_P0_ROUTE_VS4

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F31E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

25.1.201 UDB_P0_ROUTE_VS5

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F31EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

25.1.202 UDB_P0_ROUTE_VS6

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F31EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

25.1.203 UDB_P0_ROUTE_VS7

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F31EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

25.1.204 UDB_P1_ROUTE_HC0

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.205 UDB_P1_ROUTE_HC1

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3301

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.206 UDB_P1_ROUTE_HC2

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3302

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.207 UDB_P1_ROUTE_HC3

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3303

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.208 UDB_P1_ROUTE_HC4

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.209 UDB_P1_ROUTE_HC5

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3305

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.210 UDB_P1_ROUTE_HC6

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3306

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.211 UDB_P1_ROUTE_HC7

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3307

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.212 UDB_P1_ROUTE_HC8

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.213 UDB_P1_ROUTE_HC9

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3309

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.214 UDB_P1_ROUTE_HC10

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F330A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.215 UDB_P1_ROUTE_HC11

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F330B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.216 UDB_P1_ROUTE_HC12

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F330C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.217 UDB_P1_ROUTE_HC13

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F330D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.218 UDB_P1_ROUTE_HC14

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F330E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.219 UDB_P1_ROUTE_HC15

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F330F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.220 UDB_P1_ROUTE_HC16

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.221 UDB_P1_ROUTE_HC17

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3311

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.222 UDB_P1_ROUTE_HC18

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3312

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.223 UDB_P1_ROUTE_HC19

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3313

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.224 UDB_P1_ROUTE_HC20

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3314

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.225 UDB_P1_ROUTE_HC21

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3315

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.226 UDB_P1_ROUTE_HC22

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3316

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.227 UDB_P1_ROUTE_HC23

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3317

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.228 UDB_P1_ROUTE_HC24

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.229 UDB_P1_ROUTE_HC25

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3319

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.230 UDB_P1_ROUTE_HC26

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F331A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.231 UDB_P1_ROUTE_HC27

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F331B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.232 UDB_P1_ROUTE_HC28

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F331C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.233 UDB_P1_ROUTE_HC29

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F331D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.234 UDB_P1_ROUTE_HC30

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F331E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.235 UDB_P1_ROUTE_HC31

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F331F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.236 UDB_P1_ROUTE_HC32

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.237 UDB_P1_ROUTE_HC33

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3321

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.238 UDB_P1_ROUTE_HC34

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3322

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.239 UDB_P1_ROUTE_HC35

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3323

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.240 UDB_P1_ROUTE_HC36

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3324

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.241 UDB_P1_ROUTE_HC37

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3325

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.242 UDB_P1_ROUTE_HC38

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3326

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.243 UDB_P1_ROUTE_HC39

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3327

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.244 UDB_P1_ROUTE_HC40

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3328

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.245 UDB_P1_ROUTE_HC41

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3329

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.246 UDB_P1_ROUTE_HC42

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F332A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.247 UDB_P1_ROUTE_HC43

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F332B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.248 UDB_P1_ROUTE_HC44

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F332C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.249 UDB_P1_ROUTE_HC45

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F332D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.250 UDB_P1_ROUTE_HC46

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F332E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.251 UDB_P1_ROUTE_HC47

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F332F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.252 UDB_P1_ROUTE_HC48

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3330

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.253 UDB_P1_ROUTE_HC49

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3331

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.254 UDB_P1_ROUTE_HC50

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3332

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.255 UDB_P1_ROUTE_HC51

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3333

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.256 UDB_P1_ROUTE_HC52

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3334

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.257 UDB_P1_ROUTE_HC53

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3335

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.258 UDB_P1_ROUTE_HC54

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3336

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.259 UDB_P1_ROUTE_HC55

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3337

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.260 UDB_P1_ROUTE_HC56

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3338

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.261 UDB_P1_ROUTE_HC57

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3339

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.262 UDB_P1_ROUTE_HC58

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F333A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.263 UDB_P1_ROUTE_HC59

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F333B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.264 UDB_P1_ROUTE_HC60

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F333C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.265 UDB_P1_ROUTE_HC61

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F333D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.266 UDB_P1_ROUTE_HC62

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F333E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.267 UDB_P1_ROUTE_HC63

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F333F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.268 UDB_P1_ROUTE_HC64

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.269 UDB_P1_ROUTE_HC65

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3341

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.270 UDB_P1_ROUTE_HC66

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3342

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.271 UDB_P1_ROUTE_HC67

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3343

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.272 UDB_P1_ROUTE_HC68

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3344

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.273 UDB_P1_ROUTE_HC69

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3345

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.274 UDB_P1_ROUTE_HC70

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3346

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.275 UDB_P1_ROUTE_HC71

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3347

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.276 UDB_P1_ROUTE_HC72

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.277 UDB_P1_ROUTE_HC73

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3349

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.278 UDB_P1_ROUTE_HC74

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F334A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.279 UDB_P1_ROUTE_HC75

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F334B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.280 UDB_P1_ROUTE_HC76

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F334C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.281 UDB_P1_ROUTE_HC77

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F334D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.282 UDB_P1_ROUTE_HC78

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F334E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.283 UDB_P1_ROUTE_HC79

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F334F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.284 UDB_P1_ROUTE_HC80

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3350

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.285 UDB_P1_ROUTE_HC81

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3351

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.286 UDB_P1_ROUTE_HC82

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3352

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.287 UDB_P1_ROUTE_HC83

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3353

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.288 UDB_P1_ROUTE_HC84

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3354

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.289 UDB_P1_ROUTE_HC85

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3355

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.290 UDB_P1_ROUTE_HC86

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3356

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.291 UDB_P1_ROUTE_HC87

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3357

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.292 UDB_P1_ROUTE_HC88

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3358

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.293 UDB_P1_ROUTE_HC89

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3359

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.294 UDB_P1_ROUTE_HC90

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F335A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.295 UDB_P1_ROUTE_HC91

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F335B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.296 UDB_P1_ROUTE_HC92

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F335C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.297 UDB_P1_ROUTE_HC93

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F335D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.298 UDB_P1_ROUTE_HC94

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F335E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.299 UDB_P1_ROUTE_HC95

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F335F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.300 UDB_P1_ROUTE_HC96

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.301 UDB_P1_ROUTE_HC97

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3361

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.302 UDB_P1_ROUTE_HC98

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3362

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.303 UDB_P1_ROUTE_HC99

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3363

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.304 UDB_P1_ROUTE_HC100

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3364

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.305 UDB_P1_ROUTE_HC101

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3365

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.306 UDB_P1_ROUTE_HC102

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3366

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.307 UDB_P1_ROUTE_HC103

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3367

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.308 UDB_P1_ROUTE_HC104

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3368

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.309 UDB_P1_ROUTE_HC105

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3369

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.310 UDB_P1_ROUTE_HC106

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F336A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.311 UDB_P1_ROUTE_HC107

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F336B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.312 UDB_P1_ROUTE_HC108

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F336C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.313 UDB_P1_ROUTE_HC109

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F336D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.314 UDB_P1_ROUTE_HC110

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F336E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.315 UDB_P1_ROUTE_HC111

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F336F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.316 UDB_P1_ROUTE_HC112

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3370

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.317 UDB_P1_ROUTE_HC113

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3371

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.318 UDB_P1_ROUTE_HC114

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3372

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.319 UDB_P1_ROUTE_HC115

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3373

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.320 UDB_P1_ROUTE_HC116

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3374

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.321 UDB_P1_ROUTE_HC117

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3375

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.322 UDB_P1_ROUTE_HC118

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3376

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.323 UDB_P1_ROUTE_HC119

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3377

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.324 UDB_P1_ROUTE_HC120

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3378

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.325 UDB_P1_ROUTE_HC121

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3379

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.326 UDB_P1_ROUTE_HC122

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F337A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.327 UDB_P1_ROUTE_HC123

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F337B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.328 UDB_P1_ROUTE_HC124

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F337C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.329 UDB_P1_ROUTE_HC125

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F337D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.330 UDB_P1_ROUTE_HC126

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F337E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.331 UDB_P1_ROUTE_HC127

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F337F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

25.1.332 UDB_P1_ROUTE_HV_L0

UDB Channel HV Tile Configuration; Left

Address: 0x400F3380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.333 UDB_P1_ROUTE_HV_L1

UDB Channel HV Tile Configuration; Left

Address: 0x400F3381

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.334 UDB_P1_ROUTE_HV_L2

UDB Channel HV Tile Configuration; Left

Address: 0x400F3382

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.335 UDB_P1_ROUTE_HV_L3

UDB Channel HV Tile Configuration; Left

Address: 0x400F3383

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.336 UDB_P1_ROUTE_HV_L4

UDB Channel HV Tile Configuration; Left

Address: 0x400F3384

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.337 UDB_P1_ROUTE_HV_L5

UDB Channel HV Tile Configuration; Left

Address: 0x400F3385

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.338 UDB_P1_ROUTE_HV_L6

UDB Channel HV Tile Configuration; Left

Address: 0x400F3386

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.339 UDB_P1_ROUTE_HV_L7

UDB Channel HV Tile Configuration; Left

Address: 0x400F3387

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.340 UDB_P1_ROUTE_HV_L8

UDB Channel HV Tile Configuration; Left

Address: 0x400F3388

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.341 UDB_P1_ROUTE_HV_L9

UDB Channel HV Tile Configuration; Left

Address: 0x400F3389

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.342 UDB_P1_ROUTE_HV_L10

UDB Channel HV Tile Configuration; Left

Address: 0x400F338A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.343 UDB_P1_ROUTE_HV_L11

UDB Channel HV Tile Configuration; Left

Address: 0x400F338B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.344 UDB_P1_ROUTE_HV_L12

UDB Channel HV Tile Configuration; Left

Address: 0x400F338C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.345 UDB_P1_ROUTE_HV_L13

UDB Channel HV Tile Configuration; Left

Address: 0x400F338D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.346 UDB_P1_ROUTE_HV_L14

UDB Channel HV Tile Configuration; Left

Address: 0x400F338E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.347 UDB_P1_ROUTE_HV_L15

UDB Channel HV Tile Configuration; Left

Address: 0x400F338F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.348 UDB_P1_ROUTE_HS0

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3390

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.349 UDB_P1_ROUTE_HS1

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3391

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.350 UDB_P1_ROUTE_HS2

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3392

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.351 UDB_P1_ROUTE_HS3

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3393

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.352 UDB_P1_ROUTE_HS4

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3394

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.353 UDB_P1_ROUTE_HS5

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3395

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.354 UDB_P1_ROUTE_HS6

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3396

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.355 UDB_P1_ROUTE_HS7

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3397

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.356 UDB_P1_ROUTE_HS8

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3398

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.357 UDB_P1_ROUTE_HS9

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3399

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.358 UDB_P1_ROUTE_HS10

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F339A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.359 UDB_P1_ROUTE_HS11

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F339B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.360 UDB_P1_ROUTE_HS12

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F339C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.361 UDB_P1_ROUTE_HS13

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F339D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.362 UDB_P1_ROUTE_HS14

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F339E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.363 UDB_P1_ROUTE_HS15

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F339F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.364 UDB_P1_ROUTE_HS16

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F33A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.365 UDB_P1_ROUTE_HS17

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F33A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.366 UDB_P1_ROUTE_HS18

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F33A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.367 UDB_P1_ROUTE_HS19

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F33A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.368 UDB_P1_ROUTE_HS20

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F33A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.369 UDB_P1_ROUTE_HS21

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F33A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.370 UDB_P1_ROUTE_HS22

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F33A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.371 UDB_P1_ROUTE_HS23

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F33A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

25.1.372 UDB_P1_ROUTE_HV_R0

UDB Channel HV Tile Configuration; Right

Address: 0x400F33A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.373 UDB_P1_ROUTE_HV_R1

UDB Channel HV Tile Configuration; Right

Address: 0x400F33A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.374 UDB_P1_ROUTE_HV_R2

UDB Channel HV Tile Configuration; Right

Address: 0x400F33AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.375 UDB_P1_ROUTE_HV_R3

UDB Channel HV Tile Configuration; Right

Address: 0x400F33AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.376 UDB_P1_ROUTE_HV_R4

UDB Channel HV Tile Configuration; Right

Address: 0x400F33AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.377 UDB_P1_ROUTE_HV_R5

UDB Channel HV Tile Configuration; Right

Address: 0x400F33AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.378 UDB_P1_ROUTE_HV_R6

UDB Channel HV Tile Configuration; Right

Address: 0x400F33AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.379 UDB_P1_ROUTE_HV_R7

UDB Channel HV Tile Configuration; Right

Address: 0x400F33AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.380 UDB_P1_ROUTE_HV_R8

UDB Channel HV Tile Configuration; Right

Address: 0x400F33B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.381 UDB_P1_ROUTE_HV_R9

UDB Channel HV Tile Configuration; Right

Address: 0x400F33B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.382 UDB_P1_ROUTE_HV_R10

UDB Channel HV Tile Configuration; Right

Address: 0x400F33B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.383 UDB_P1_ROUTE_HV_R11

UDB Channel HV Tile Configuration; Right

Address: 0x400F33B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.384 UDB_P1_ROUTE_HV_R12

UDB Channel HV Tile Configuration; Right

Address: 0x400F33B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.385 UDB_P1_ROUTE_HV_R13

UDB Channel HV Tile Configuration; Right

Address: 0x400F33B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.386 UDB_P1_ROUTE_HV_R14

UDB Channel HV Tile Configuration; Right

Address: 0x400F33B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.387 UDB_P1_ROUTE_HV_R15

UDB Channel HV Tile Configuration; Right

Address: 0x400F33B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

25.1.388 UDB_P1_ROUTE_PLD0IN0

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F33C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.389 UDB_P1_ROUTE_PLD0IN1

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F33C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.390 UDB_P1_ROUTE_PLD0IN2

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F33C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.391 UDB_P1_ROUTE_PLD1IN0

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F33CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.392 UDB_P1_ROUTE_PLD1IN1

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F33CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.393 UDB_P1_ROUTE_PLD1IN2

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F33CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.394 UDB_P1_ROUTE_DPIN0

UDB Channel PI Tile Configuration; Datapath Input

Address: 0x400F33D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.395 UDB_P1_ROUTE_DPIN1

UDB Channel PI Tile Configuration; Datapath Input

Address: 0x400F33D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		None	
HW Access	None		R		R		None	
Name	None [7:6]		PI_BOT2 [5:4]		PI_TOP2 [3:2]		None [1:0]	

Bits	Name	Description
5 : 4	PI_BOT2	RAM configuration bits (2) for BOTTOM UDB port interface configuration Default Value: X
3 : 2	PI_TOP2	RAM configuration bits (2) for TOP UDB port interface configuration Default Value: X

25.1.396 UDB_P1_ROUTE_SCIN

UDB Channel PI Tile Configuration; Status / Control Blocks Input Control

Address: 0x400F33D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.397 UDB_P1_ROUTE_SCIOIN

UDB Channel PI Tile Configuration; Status / Control Blocks Input / Output Control

Address: 0x400F33D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.398 UDB_P1_ROUTE_RCIN

UDB Channel PI Tile Configuration; Reset and Clock Blocks Input Control

Address: 0x400F33DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

25.1.399 UDB_P1_ROUTE_VS0

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F33E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

25.1.400 UDB_P1_ROUTE_VS1

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F33E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

25.1.401 UDB_P1_ROUTE_VS2

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F33E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

25.1.402 UDB_P1_ROUTE_VS3

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F33E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

25.1.403 UDB_P1_ROUTE_VS4

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F33E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

25.1.404 UDB_P1_ROUTE_VS5

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F33EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

25.1.405 UDB_P1_ROUTE_VS6

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F33EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

25.1.406 UDB_P1_ROUTE_VS7

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F33EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

26 SAR Registers

This section discusses the SAR registers. It lists all the registers in mapping tables, in address order.

26.1 Register Details

Register Name	Address
SAR_CTRL	0x403A0000
SAR_SAMPLE_CTRL	0x403A0004
SAR_SAMPLE_TIME01	0x403A0010
SAR_SAMPLE_TIME23	0x403A0014
SAR_RANGE_THRES	0x403A0018
SAR_RANGE_COND	0x403A001C
SAR_CHAN_EN	0x403A0020
SAR_START_CTRL	0x403A0024
SAR_CHAN_CONFIG0	0x403A0080
SAR_CHAN_CONFIG1	0x403A0084
SAR_CHAN_CONFIG2	0x403A0088
SAR_CHAN_CONFIG3	0x403A008C
SAR_CHAN_CONFIG4	0x403A0090
SAR_CHAN_CONFIG5	0x403A0094
SAR_CHAN_CONFIG6	0x403A0098
SAR_CHAN_CONFIG7	0x403A009C
SAR_CHAN_CONFIG8	0x403A00A0
SAR_CHAN_CONFIG9	0x403A00A4
SAR_CHAN_CONFIG10	0x403A00A8
SAR_CHAN_CONFIG11	0x403A00AC
SAR_CHAN_CONFIG12	0x403A00B0
SAR_CHAN_CONFIG13	0x403A00B4
SAR_CHAN_CONFIG14	0x403A00B8
SAR_CHAN_CONFIG15	0x403A00BC
SAR_CHAN_WORK0	0x403A0100
SAR_CHAN_WORK1	0x403A0104

Register Name	Address
SAR_CHAN_WORK2	0x403A0108
SAR_CHAN_WORK3	0x403A010C
SAR_CHAN_WORK4	0x403A0110
SAR_CHAN_WORK5	0x403A0114
SAR_CHAN_WORK6	0x403A0118
SAR_CHAN_WORK7	0x403A011C
SAR_CHAN_WORK8	0x403A0120
SAR_CHAN_WORK9	0x403A0124
SAR_CHAN_WORK10	0x403A0128
SAR_CHAN_WORK11	0x403A012C
SAR_CHAN_WORK12	0x403A0130
SAR_CHAN_WORK13	0x403A0134
SAR_CHAN_WORK14	0x403A0138
SAR_CHAN_WORK15	0x403A013C
SAR_CHAN_RESULT0	0x403A0180
SAR_CHAN_RESULT1	0x403A0184
SAR_CHAN_RESULT2	0x403A0188
SAR_CHAN_RESULT3	0x403A018C
SAR_CHAN_RESULT4	0x403A0190
SAR_CHAN_RESULT5	0x403A0194
SAR_CHAN_RESULT6	0x403A0198
SAR_CHAN_RESULT7	0x403A019C
SAR_CHAN_RESULT8	0x403A01A0
SAR_CHAN_RESULT9	0x403A01A4
SAR_CHAN_RESULT10	0x403A01A8
SAR_CHAN_RESULT11	0x403A01AC
SAR_CHAN_RESULT12	0x403A01B0
SAR_CHAN_RESULT13	0x403A01B4
SAR_CHAN_RESULT14	0x403A01B8
SAR_CHAN_RESULT15	0x403A01BC
SAR_CHAN_WORK_VALID	0x403A0200
SAR_CHAN_RESULT_VALID	0x403A0204
SAR_STATUS	0x403A0208
SAR_AVG_STAT	0x403A020C
SAR_INTR	0x403A0210
SAR_INTR_SET	0x403A0214
SAR_INTR_MASK	0x403A0218
SAR_INTR_MASKED	0x403A021C
SAR_SATURATE_INTR	0x403A0220
SAR_SATURATE_INTR_SET	0x403A0224

Register Name	Address
SAR_SATURATE_INTR_MASK	0x403A0228
SAR_SATURATE_INTR_MASKED	0x403A022C
SAR_RANGE_INTR	0x403A0230
SAR_RANGE_INTR_SET	0x403A0234
SAR_RANGE_INTR_MASK	0x403A0238
SAR_RANGE_INTR_MASKED	0x403A023C
SAR_INTR_CAUSE	0x403A0240
SAR_INJ_CHAN_CONFIG	0x403A0280
SAR_INJ_RESULT	0x403A0290
SAR_MUX_SWITCH0	0x403A0300
SAR_MUX_SWITCH_CLEAR0	0x403A0304
SAR_MUX_SWITCH_HW_CTRL	0x403A0340
SAR_MUX_SWITCH_STATUS	0x403A0348
SAR_PUMP_CTRL	0x403A0380
SAR_ANA_TRIM	0x403A0F00

26.1.1 SAR_CTRL

Analog control register.

Address: 0x403A0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			None			
HW Access	R	R			None			
Name	VREF_BYP_CAP_EN	VREF_SEL [6:4]			None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	None	RW			None
HW Access	R		R	None	R			None
Name	PWR_CTRL_VREF [15:14]		SAR_HW_CTRL_NEGVREF	None	NEG_SEL [11:9]			None

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [23:21]			BOOSTPUMP_EN	SPARE [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	None	RW	
HW Access	R	R	R	R	R	None	R	
Name	ENABLED	SWITCH_DISABLE	DSI_MODE	DSI_SYNC_CONFIG	DEEPSLEEP_ON	None	ICONT_LV [25:24]	

Bits	Name	Description
31	ENABLED	Before enabling always make sure the SAR is idle (STATUS.BUSY==0) - 0: SAR IP disabled (put analog in power down and stop clocks), also can clear FW_TRIGGER and INJ_START_EN (if not tailgaiting) on write. - 1: SAR IP enabled. Default Value: 0
30	SWITCH_DISABLE	Disable SAR sequencer from enabling routing switches (note DSI and firmware can always close switches independent of this control) - 0: Normal mode, SAR sequencer changes switches according to pin address in channel configurations - 1: Switches disabled, SAR sequencer does not enable any switches, it is the responsibility of the firmware or UDBs (through DSI) to set the switches to route the signal to be converted through the SARMUX Default Value: 0

26.1.1 SAR_CTRL (continued)

29	DSI_MODE	SAR sequencer takes configuration from DSI signals (note this also has the same effect as SWITCH_DISABLE==1) - 0: Normal mode, SAR sequencer operates according to CHAN_EN enables and CHAN_CONFIG channel configurations - 1: CHAN_EN, INJ_START_EN and channel configurations in CHAN_CONFIG and INJ_CHAN_CONFIG are ignored Default Value: 0
28	DSI_SYNC_CONFIG	- 0: bypass clock domain synchronisation of the DSI config signals. - 1: synchronize the DSI config signals to peripheral clock domain. Default Value: 1
27	DEEPSLEEP_ON	- 0: SARMUX IP disabled off during DeepSleep power mode - 1: SARMUX IP remains enabled during DeepSleep power mode (if ENABLED=1) Default Value: 0
25 : 24	ICONT_LV	SARADC low power mode. Default Value: 0 **0x0: NORMAL_PWR:** normal power (default), max clk_sar is 18MHz. **0x1: HALF_PWR:** 1/2 power mode, max clk_sar is 9MHz. **0x2: MORE_PWR:** 1.333 power mode, max clk_sar is 18MHz. **0x3: QUARTER_PWR:** 1/4 power mode, max clk_sar is 4.5MHz.
20	BOOSTPUMP_EN	SARADC internal pump: 0=disabled: pump output is VDDA, 1=enabled: pump output is boosted. Default Value: 0
19 : 16	SPARE	Spare controls, not yet designated, for late changes done with an ECO Default Value: 0
15 : 14	PWR_CTRL_VREF	VREF buffer low power mode. Default Value: 0 **0x0: NORMAL_PWR:** normal power (default), bypass cap, max clk_sar is 18MHz. **0x1: HALF_PWR:** deprecated **0x2: THIRD_PWR:** Invalid for PSoC4A, otherwise 2X power, no bypass cap, max clk_sar is 1.8MHz **0x3: QUARTER_PWR:** deprecated
13	SAR_HW_CTRL_NEGVREF	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for VREF to NEG switch. Default Value: 0
11 : 9	NEG_SEL	SARADC internal NEG selection for Single ended conversion Default Value: 0 **0x0: VSSA_KELVIN:** NEG input of SARADC is connected to "vssa_kelvin", gives more precision around zero. Note this opens both SARADC internal switches, therefore use this value to insert a break-before-make cycle on those switches when SWITCH_DISABLE is high.

26.1.1 SAR_CTRL (continued)

		0x1: ART_VSSA: NEG input of SARADC is connected to VSSA in AROUTE close to the SARADC **0x2: P1:** NEG input of SARADC is connected to P1 pin of SARMUX **0x3: P3:** NEG input of SARADC is connected to P3 pin of SARMUX **0x4: P5:** NEG input of SARADC is connected to P5 pin of SARMUX **0x5: P7:** NEG input of SARADC is connected to P7 pin of SARMUX **0x6: ACORE:** NEG input of SARADC is connected to an ACORE in AROUTE **0x7: VREF:** NEG input of SARADC is shorted with VREF input of SARADC.
7	VREF_BYP_CAP_EN	VREF bypass cap enable for when VREF buffer is on Default Value: 0
6 : 4	VREF_SEL	SARADC internal VREF selection. Default Value: 0 **0x0: VREF0:** VREF0 from PRB (VREF buffer on) **0x1: VREF1:** VREF1 from PRB (VREF buffer on) **0x2: VREF2:** VREF2 from PRB (VREF buffer on) **0x3: VREF_AROUTE:** VREF from AROUTE (VREF buffer on) **0x4: VBGR:** 1.024V from BandGap (VREF buffer on) **0x5: VREF_EXT:** External precision Vref direct from a pin (low impedance path). **0x6: VDDA_DIV_2:** Vdda/2 (VREF buffer on) **0x7: VDDA:** Vdda.

26.1.2 SAR_SAMPLE_CTRL

Sample control register.

Address: 0x403A0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW	RW	RW
HW Access	R	R			R	R	R	R
Name	AVG_SHIFT	AVG_CNT [6:4]			DIFFERENTIAL_SIGNED	SINGLE_ENDED_SIGNED	LEFT_ALIGN	SUB_RESOLUTION

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [23:20]				DSI_SYNC_TRIGGER	DSI_TRIGGER_LEVEL	DSI_TRIGGER_EN	CONTINU-OUS

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	EOS_DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	EOS_DSI_OUT_EN	Enable to output EOS_INTR to DSI. When enabled each time EOS_INTR is set by the hardware also a pulse is send on the dsi_eos signal. Default Value: 0
19	DSI_SYNC_TRIGGER	- 0: bypass clock domain synchronisation of the DSI trigger signal. - 1: synchronize the DSI trigger signal to the SAR clock domain, if needed an edge detect is done in the peripheral clock domain. Default Value: 1
18	DSI_TRIGGER_LEVEL	- 0: DSI trigger signal is a pulse input, a positive edge detected on the DSI trigger signal triggers a new scan. - 1: DSI trigger signal is a level input, as long as the DSI trigger signal remains high the SAR will do continuous scans. Default Value: 0
17	DSI_TRIGGER_EN	- 0: firmware trigger only: disable hardware (DSI) trigger. - 1: enable hardware (DSI) trigger (e.g. from TCPWM, GPIO or UDB). Default Value: 0

26.1.2 SAR_SAMPLE_CTRL (continued)

16	CONTINUOUS	- 0: Wait for next FW_TRIGGER (one shot) or hardware (DSI) trigger (e.g. from TPWM for periodic triggering) before scanning enabled channels. - 1: Continuously scan enabled channels, ignore triggers. Default Value: 0
7	AVG_SHIFT	Averaging shifting: after averaging the result is shifted right to fit in the sample resolution. Default Value: 0
6 : 4	AVG_CNT	Averaging Count for channels that have over sampling enabled (AVG_EN). A channel will be sampled back to back (1<<(AVG_CNT+1)) = [2..256] times before the result is stored and the next enabled channel is sampled (1st order accumulate and dump filter). If shifting is not enabled (AVG_SHIFT=0) then the result is forced to shift right so that is fits in 16 bits, so right shift is done by max(0,AVG_CNT-3). Default Value: 0
3	DIFFERENTIAL_SIGNED	Output data from a differential conversion as a signed value Default Value: 1 **0x0: UNSIGNED:** result data is unsigned (zero extended if needed) **0x1: SIGNED:** Default: result data is signed (sign extended if needed)
2	SINGLE_ENDED_SIGNED	Output data from a single ended conversion as a signed value Default Value: 0 **0x0: UNSIGNED:** Default: result data is unsigned (zero extended if needed) **0x1: SIGNED:** result data is signed (sign extended if needed)
1	LEFT_ALIGN	Left align data in data[15:0], default data is right aligned in data[11:0], with sign extension to 16 bits if the channel is differential. Default Value: 0
0	SUB_RESOLUTION	Conversion resolution for channels that have sub-resolution enabled (RESOLUTION=1) (otherwise resolution is 12-bit). Default Value: 0 **0x0: 8B:** 8-bit. **0x1: 10B:** 10-bit.

26.1.3 SAR_SAMPLE_TIME01

Sample time specification ST0 and ST1

Address: 0x403A0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SAMPLE_TIME0 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SAMPLE_TIME1 [25:24]	

Bits	Name	Description
25 : 16	SAMPLE_TIME1	Sample time1 Default Value: 4
9 : 0	SAMPLE_TIME0	Sample time0 (aperture) in ADC clock cycles. Note that actual sample time is half a clock less than specified here. The minimum sample time is 194ns, which is 3.5 cycles (4 in this field) with an 18MHz clock. Minimum legal value in this register is 2. Default Value: 4

26.1.4 SAR_SAMPLE_TIME23

Sample time specification ST2 and ST3

Address: 0x403A0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SAMPLE_TIME2 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SAMPLE_TIME3 [25:24]	

Bits	Name	Description
25 : 16	SAMPLE_TIME3	Sample time3 Default Value: 4
9 : 0	SAMPLE_TIME2	Sample time2 Default Value: 4

26.1.5 SAR_RANGE_THRES

Global range detect threshold register.

Address: 0x403A0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [31:24]							

Bits	Name	Description
31 : 16	RANGE_HIGH	High threshold for range detect. Default Value: 0
15 : 0	RANGE_LOW	Low threshold for range detect. Default Value: 0

26.1.6 SAR_RANGE_COND

Global range detect mode register.

Address: 0x403A001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	RANGE_COND [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	RANGE_COND	Range condition select. Default Value: 0 **0x0: BELOW:** result < RANGE_LOW **0x1: INSIDE:** RANGE_LOW <= result < RANGE_HIGH **0x2: ABOVE:** RANGE_HIGH <= result **0x3: OUTSIDE:** result < RANGE_LOW || RANGE_HIGH <= result

26.1.7 SAR_CHAN_EN

Enable bits for the channels

Address: 0x403A0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CHAN_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CHAN_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_EN	Channel enable. - 0: the corresponding channel is disabled. - 1: the corresponding channel is enabled, it will be included in the next scan. Default Value: 0

26.1.8 SAR_START_CTRL

Start control register (firmware trigger).

Address: 0x403A0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							FW_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FW_TRIGGER	When firmware writes a 1 here it will trigger the next scan of enabled channels, hardware clears this bit when the scan started with this trigger is completed. If scanning continuously the trigger is ignored and hardware clears this bit after the next scan is done. This bit is also cleared when the SAR is disabled. Default Value: 0

26.1.9 SAR_CHAN_CONFIG0

Channel configuration register.

Address: 0x403A0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0

26.1.9 SAR_CHAN_CONFIG0 (continued)

		0x0: MAXRES: The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

26.1.10 SAR_CHAN_CONFIG1

Channel configuration register.

Address: 0x403A0084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0

26.1.10 SAR_CHAN_CONFIG1 (continued)

		0x0: MAXRES: The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

26.1.11 SAR_CHAN_CONFIG2

Channel configuration register.

Address: 0x403A0088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0

26.1.11 SAR_CHAN_CONFIG2 (continued)

		0x0: MAXRES: The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

26.1.12 SAR_CHAN_CONFIG3

Channel configuration register.

Address: 0x403A008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0

26.1.12 SAR_CHAN_CONFIG3 (continued)

		0x0: MAXRES: The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

26.1.13 SAR_CHAN_CONFIG4

Channel configuration register.

Address: 0x403A0090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0

26.1.13 SAR_CHAN_CONFIG4 (continued)

		0x0: MAXRES: The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

26.1.14 SAR_CHAN_CONFIG5

Channel configuration register.

Address: 0x403A0094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0

26.1.14 SAR_CHAN_CONFIG5 (continued)

		0x0: MAXRES: The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

26.1.15 SAR_CHAN_CONFIG6

Channel configuration register.

Address: 0x403A0098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0

26.1.15 SAR_CHAN_CONFIG6 (continued)

		0x0: MAXRES: The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

26.1.16 SAR_CHAN_CONFIG7

Channel configuration register.

Address: 0x403A009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0

26.1.16 SAR_CHAN_CONFIG7 (continued)

		0x0: MAXRES: The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

26.1.17 SAR_CHAN_CONFIG8

Channel configuration register.

Address: 0x403A00A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0

26.1.17 SAR_CHAN_CONFIG8 (continued)

		0x0: MAXRES: The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

26.1.18 SAR_CHAN_CONFIG9

Channel configuration register.

Address: 0x403A00A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0

26.1.18 SAR_CHAN_CONFIG9 (continued)

		0x0: MAXRES: The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

26.1.19 SAR_CHAN_CONFIG10

Channel configuration register.

Address: 0x403A00A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0

26.1.19 SAR_CHAN_CONFIG10 (continued)

		0x0: MAXRES: The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

26.1.20 SAR_CHAN_CONFIG11

Channel configuration register.

Address: 0x403A00AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0

26.1.20 SAR_CHAN_CONFIG11 (continued)

		0x0: MAXRES: The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

26.1.21 SAR_CHAN_CONFIG12

Channel configuration register.

Address: 0x403A00B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0

26.1.21 SAR_CHAN_CONFIG12 (continued)

		0x0: MAXRES: The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

26.1.22 SAR_CHAN_CONFIG13

Channel configuration register.

Address: 0x403A00B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0

26.1.22 SAR_CHAN_CONFIG13 (continued)

		0x0: MAXRES: The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

26.1.23 SAR_CHAN_CONFIG14

Channel configuration register.

Address: 0x403A00B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0

26.1.23 SAR_CHAN_CONFIG14 (continued)

		0x0: MAXRES: The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

26.1.24 SAR_CHAN_CONFIG15

Channel configuration register.

Address: 0x403A00BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0

26.1.24 SAR_CHAN_CONFIG15 (continued)

		0x0: MAXRES: The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

26.1.25 SAR_CHAN_WORK0

Channel working data register

Address: 0x403A0100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

26.1.26 SAR_CHAN_WORK1

Channel working data register

Address: 0x403A0104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

26.1.27 SAR_CHAN_WORK2

Channel working data register

Address: 0x403A0108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

26.1.28 SAR_CHAN_WORK3

Channel working data register

Address: 0x403A010C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

26.1.29 SAR_CHAN_WORK4

Channel working data register

Address: 0x403A0110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

26.1.30 SAR_CHAN_WORK5

Channel working data register

Address: 0x403A0114

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

26.1.31 SAR_CHAN_WORK6

Channel working data register

Address: 0x403A0118

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

26.1.32 SAR_CHAN_WORK7

Channel working data register

Address: 0x403A011C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

26.1.33 SAR_CHAN_WORK8

Channel working data register

Address: 0x403A0120

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

26.1.34 SAR_CHAN_WORK9

Channel working data register

Address: 0x403A0124

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

26.1.35 SAR_CHAN_WORK10

Channel working data register

Address: 0x403A0128

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

26.1.36 SAR_CHAN_WORK11

Channel working data register

Address: 0x403A012C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

26.1.37 SAR_CHAN_WORK12

Channel working data register

Address: 0x403A0130

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

26.1.38 SAR_CHAN_WORK13

Channel working data register

Address: 0x403A0134

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

26.1.39 SAR_CHAN_WORK14

Channel working data register

Address: 0x403A0138

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

26.1.40 SAR_CHAN_WORK15

Channel working data register

Address: 0x403A013C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

26.1.41 SAR_CHAN_RESULT0

Channel result data register

Address: 0x403A0180

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

26.1.42 SAR_CHAN_RESULT1

Channel result data register

Address: 0x403A0184

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

26.1.43 SAR_CHAN_RESULT2

Channel result data register

Address: 0x403A0188

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

26.1.44 SAR_CHAN_RESULT3

Channel result data register

Address: 0x403A018C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

26.1.45 SAR_CHAN_RESULT4

Channel result data register

Address: 0x403A0190

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

26.1.46 SAR_CHAN_RESULT5

Channel result data register

Address: 0x403A0194

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

26.1.47 SAR_CHAN_RESULT6

Channel result data register

Address: 0x403A0198

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

26.1.48 SAR_CHAN_RESULT7

Channel result data register

Address: 0x403A019C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

26.1.49 SAR_CHAN_RESULT8

Channel result data register

Address: 0x403A01A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

26.1.50 SAR_CHAN_RESULT9

Channel result data register

Address: 0x403A01A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

26.1.51 SAR_CHAN_RESULT10

Channel result data register

Address: 0x403A01A8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

26.1.52 SAR_CHAN_RESULT11

Channel result data register

Address: 0x403A01AC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

26.1.53 SAR_CHAN_RESULT12

Channel result data register

Address: 0x403A01B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

26.1.54 SAR_CHAN_RESULT13

Channel result data register

Address: 0x403A01B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

26.1.55 SAR_CHAN_RESULT14

Channel result data register

Address: 0x403A01B8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

26.1.56 SAR_CHAN_RESULT15

Channel result data register

Address: 0x403A01BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

26.1.57 SAR_CHAN_WORK_VALID

Channel working data register valid bits

Address: 0x403A0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CHAN_WORK_VALID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CHAN_WORK_VALID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_WORK_VALID	If set the corresponding WORK data is valid, i.e. was already sampled during the current scan. Default Value: 0

26.1.58 SAR_CHAN_RESULT_VALID

Channel result data register valid bits

Address: 0x403A0204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CHAN_RESULT_VALID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CHAN_RESULT_VALID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_RESULT_VALID	If set the corresponding RESULT data is valid, i.e. was sampled during the last scan. Default Value: 0

26.1.59 SAR_STATUS

Current status of internal SAR registers (mostly for debug)

Address: 0x403A0208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			CUR_CHAN [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	BUSY	SW_VREF_NEG	None [29:24]					

Bits	Name	Description
31	BUSY	If high then the SAR is busy with a conversion. This bit is always high when CONTINUOUS is set. Firmware should wait for this bit to be low before putting the SAR in power down. Default Value: 0
30	SW_VREF_NEG	the current switch status, including DSI and sequencer controls, of the switch in the SARADC that shorts NEG with VREF input (see NEG_SEL). Default Value: 0
4 : 0	CUR_CHAN	current channel being sampled (channel 16 indicates the injection channel), only valid if BUSY. Default Value: 0

26.1.60 SAR_AVG_STAT

Current averaging status (for debug)

Address: 0x403A020C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CUR_AVG_ACCU [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CUR_AVG_ACCU [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				CUR_AVG_ACCU [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	CUR_AVG_CNT [31:24]							

Bits	Name	Description
31 : 24	CUR_AVG_CNT	the current value of the averaging counter. Note that the value shown is updated after the sampling time and therefore runs ahead of the accumulator update. Default Value: 0
19 : 0	CUR_AVG_ACCU	the current value of the averaging accumulator Default Value: 0

26.1.61 SAR_INTR

Interrupt request register.

Address: 0x403A0210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	INJ_COLLISION_INTR	INJ_RANGE_INTR	INJ_SATURATE_INTR	INJ_EOC_INTR	DSI_COLLISION_INTR	FW_COLLISION_INTR	OVERFLOW_INTR	EOS_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_INTR	Injection Collision Interrupt: hardware sets this interrupt when the injection trigger signal is asserted (INJ_START_EN==1 && INJ_TAILGATING==0) while the SAR is BUSY. Raising this interrupt is delayed to when the sampling of the injection channel has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the injection channel was sampled later than was intended. Write with '1' to clear bit. Default Value: 0
6	INJ_RANGE_INTR	Injection Range detect Interrupt: hardware sets this interrupt if the injection conversion result (after averaging) met the condition specified by the SAR_RANGE registers. Write with '1' to clear bit. Default Value: 0
5	INJ_SATURATE_INTR	Injection Saturation Interrupt: hardware sets this interrupt if an injection conversion result (before averaging) is either 0x000 or 0xFFF (for 12-bit resolution), this is an indication that the ADC likely saturated. Write with '1' to clear bit. Default Value: 0
4	INJ_EOC_INTR	Injection End of Conversion Interrupt: hardware sets this interrupt after completing the conversion for the injection channel (irrespective of if tailgating was used). Write with '1' to clear bit. Default Value: 0

26.1.61 SAR_INTR (continued)

3	DSI_COLLISION_INTR	DSI Collision Interrupt: hardware sets this interrupt when the DSI trigger signal is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the DSI trigger has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit. Default Value: 0
2	FW_COLLISION_INTR	Firmware Collision Interrupt: hardware sets this interrupt when FW_TRIGGER is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the FW_TRIGGER has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit. Default Value: 0
1	OVERFLOW_INTR	Overflow Interrupt: hardware sets this interrupt when it sets a new EOS_INTR while that bit was not yet cleared by the firmware. Write with '1' to clear bit. Default Value: 0
0	EOS_INTR	End Of Scan Interrupt: hardware sets this interrupt after completing a scan of all the enabled channels. Write with '1' to clear bit. Default Value: 0

26.1.62 SAR_INTR_SET

Interrupt set request register

Address: 0x403A0214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	INJ_COLLISION_SET	INJ_RANGE_SET	INJ_SATURATE_SET	INJ_EOC_SET	DSI_COLLISION_SET	FW_COLLISION_SET	OVERFLOW_SET	EOS_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	INJ_RANGE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	INJ_SATURATE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	INJ_EOC_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	DSI_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	FW_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	OVERFLOW_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

26.1.62 SAR_INTR_SET (continued)

0	EOS_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

26.1.63 SAR_INTR_MASK

Interrupt mask register.

Address: 0x403A0218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INJ_COLLISION_MASK	INJ_RANGE_MASK	INJ_SATURATE_MASK	INJ_EOC_MASK	DSI_COLLISION_MASK	FW_COLLISION_MASK	OVERFLOW_MASK	EOS_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	INJ_RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	INJ_SATURATE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	INJ_EOC_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	DSI_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	FW_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	OVERFLOW_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

26.1.63 SAR_INTR_MASK (continued)

0	EOS_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

26.1.64 SAR_INTR_MASKED

Interrupt masked request register

Address: 0x403A021C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	INJ_COLLISION_MASKED	INJ_RANGE_MASKED	INJ_SATURATE_MASKED	INJ_EOC_MASKED	DSI_COLLISION_MASKED	FW_COLLISION_MASKED	OVERFLOW_MASKED	EOS_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
6	INJ_RANGE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
5	INJ_SATURATE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
4	INJ_EOC_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
3	DSI_COLLISION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
2	FW_COLLISION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
1	OVERFLOW_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

26.1.64 SAR_INTR_MASKED (continued)

0	EOS_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

26.1.65 SAR_SATURATE_INTR

Saturate interrupt request register.

Address: 0x403A0220

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	SATURATE_INTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	SATURATE_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_INTR	Saturate Interrupt: hardware sets this interrupt for each channel if a conversion result (before averaging) of that channel is either 0x000 or 0xFFF (for 12-bit resolution), this is an indication that the ADC likely saturated. Write with '1' to clear bit. Default Value: 0

26.1.66 SAR_SATURATE_INTR_SET

Saturate interrupt set request register

Address: 0x403A0224

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	SATURATE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	SATURATE_SET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

26.1.67 SAR_SATURATE_INTR_MASK

Saturate interrupt mask register.

Address: 0x403A0228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SATURATE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SATURATE_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

26.1.68 SAR_SATURATE_INTR_MASKED

Saturate interrupt masked request register

Address: 0x403A022C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SATURATE_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SATURATE_MASKED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

26.1.69 SAR_RANGE_INTR

Range detect interrupt request register.

Address: 0x403A0230

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	RANGE_INTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	RANGE_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_INTR	Range detect Interrupt: hardware sets this interrupt for each channel if the conversion result (after averaging) of that channel met the condition specified by the SAR_RANGE registers. Write with '1' to clear bit. Default Value: 0

26.1.70 SAR_RANGE_INTR_SET

Range detect interrupt set request register

Address: 0x403A0234

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	RANGE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	RANGE_SET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

26.1.71 SAR_RANGE_INTR_MASK

Range detect interrupt mask register.

Address: 0x403A0238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

26.1.72 SAR_RANGE_INTR_MASKED

Range interrupt masked request register

Address: 0x403A023C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RANGE_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RANGE_MASKED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

26.1.73 SAR_INTR_CAUSE

Interrupt cause register

Address: 0x403A0240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	INJ_COLLISION_MASKED_MIR	INJ_RANGE_MASKED_MIR	INJ_SATURATE_MASKED_MIR	INJ_EOC_MASKED_MIR	DSI_COLLISION_MASKED_MIR	FW_COLLISION_MASKED_MIR	OVERFLOW_MASKED_MIR	EOS_MASKED_MIR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	RANGE_MASKED_RED	SATURATE_MASKED_RED	None [29:24]					

Bits	Name	Description
31	RANGE_MASKED_RED	Reduction OR of all SAR_RANGE_INTR_MASKED bits Default Value: 0
30	SATURATE_MASKED_RED	Reduction OR of all SAR_SATURATION_INTR_MASKED bits Default Value: 0
7	INJ_COLLISION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
6	INJ_RANGE_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
5	INJ_SATURATE_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
4	INJ_EOC_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0

26.1.73 SAR_INTR_CAUSE (continued)

3	DSI_COLLISION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
2	FW_COLLISION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
1	OVERFLOW_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
0	EOS_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0

26.1.74 SAR_INJ_CHAN_CONFIG

Injection channel configuration register.

Address: 0x403A0280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	INJ_PORT_ADDR [6:4]			None	INJ_PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		INJ_SAMPLE_TIME_SEL [13:12]		None	INJ_AVG_EN	INJ_RESOLUTION	INJ_DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	RW	None					
HW Access	RW1C	R	None					
Name	INJ_START_EN	INJ_TAILGATING	None [29:24]					

Bits	Name	Description
31	INJ_START_EN	Set by firmware to enable the injection channel. If INJ_TAILGATING is not set this bit also functions as trigger for this channel. Cleared by hardware after this channel has been sampled (i.e. this channel is always one shot even if CONTINUOUS is set). Also cleared if the SAR is disabled. Default Value: 0
30	INJ_TAILGATING	Injection channel tailgating. - 0: no tailgating for this channel, SAR is immediately triggered when the INJ_START_EN bit is set. - 1: injection channel tailgating. The addressed pin is sampled after the next trigger and after all enabled channels have been scanned. Default Value: 0
13 : 12	INJ_SAMPLE_TIME_SEL	Injection sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	INJ_AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0

26.1.74 SAR_INJ_CHAN_CONFIG (continued)

9	INJ_RESOLUTION	Resolution for this channel. Default Value: 0 **0x0: 12B:** 12-bit resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	INJ_DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (INJ_PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	INJ_PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x6: AROUTE_VIRT:** AROUTE virtual port **0x7: SARMUX_VIRT:** SARMUX virtual port
2 : 0	INJ_PIN_ADDR	Address of the pin to be sampled by this injection channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. Default Value: 0

26.1.75 SAR_INJ_RESULT

Injection channel result register

Address: 0x403A0290

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	INJ_RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	INJ_RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	None			
HW Access	W	W	W	W	None			
Name	INJ_EOC_INTR_MIR	INJ_RANGE_INTR_MIR	INJ_SATURATE_INTR_MIR	INJ_COLLISION_INTR_MIR	None [27:24]			

Bits	Name	Description
31	INJ_EOC_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
30	INJ_RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
29	INJ_SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
28	INJ_COLLISION_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
15 : 0	INJ_RESULT	SAR conversion result of the channel. Default Value: Undefined

26.1.76 SAR_MUX_SWITCH0

SARMUX Firmware switch controls

Address: 0x403A0300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_FW_P7_VPLUS	MUX_FW_P6_VPLUS	MUX_FW_P5_VPLUS	MUX_FW_P4_VPLUS	MUX_FW_P3_VPLUS	MUX_FW_P2_VPLUS	MUX_FW_P1_VPLUS	MUX_FW_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_FW_P7_VMINUS	MUX_FW_P6_VMINUS	MUX_FW_P5_VMINUS	MUX_FW_P4_VMINUS	MUX_FW_P3_VMINUS	MUX_FW_P2_VMINUS	MUX_FW_P1_VMINUS	MUX_FW_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_FW_SARBUS1_VPLUS	MUX_FW_SARBUS0_VPLUS	MUX_FW_AMUXBUSB_VMINUS	MUX_FW_AMUXBUSA_VMINUS	MUX_FW_AMUXBUSB_VPLUS	MUX_FW_AMUXBUSA_VPLUS	MUX_FW_TEMP_VPLUS	MUX_FW_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [31:30]		MUX_FW_P7_COREIO3	MUX_FW_P6_COREIO2	MUX_FW_P5_COREIO1	MUX_FW_P4_COREIO0	MUX_FW_SARBUS1_VMINUS	MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
29	MUX_FW_P7_COREIO3	Firmware control: 0=open, 1=close switch between P7 and coreio3 signal. Write with '1' to set bit. Default Value: 0
28	MUX_FW_P6_COREIO2	Firmware control: 0=open, 1=close switch between P6 and coreio2 signal. Write with '1' to set bit. Default Value: 0
27	MUX_FW_P5_COREIO1	Firmware control: 0=open, 1=close switch between P5 and coreio1 signal. Write with '1' to set bit. Default Value: 0
26	MUX_FW_P4_COREIO0	Firmware control: 0=open, 1=close switch between P4 and coreio0 signal. Write with '1' to set bit. Default Value: 0
25	MUX_FW_SARBUS1_VMINUS	Firmware control: 0=open, 1=close switch between sarbus1 and vminus signal. Write with '1' to set bit. Default Value: 0

26.1.76 SAR_MUX_SWITCH0 (continued)

24	MUX_FW_SARBUS0_VMINUS	Firmware control: 0=open, 1=close switch between sarbus0 and vminus signal. Write with '1' to set bit. Default Value: 0
23	MUX_FW_SARBUS1_VPLUS	Firmware control: 0=open, 1=close switch between sarbus1 and vplus signal. Write with '1' to set bit. Default Value: 0
22	MUX_FW_SARBUS0_VPLUS	Firmware control: 0=open, 1=close switch between sarbus0 and vplus signal. Write with '1' to set bit. Default Value: 0
21	MUX_FW_AMUXBUSB_VMINUS	Firmware control: 0=open, 1=close switch between amuxbusb and vminus signal. Write with '1' to set bit. Default Value: 0
20	MUX_FW_AMUXBUSA_VMINUS	Firmware control: 0=open, 1=close switch between amuxbusa and vminus signal. Write with '1' to set bit. Default Value: 0
19	MUX_FW_AMUXBUSB_VPLUS	Firmware control: 0=open, 1=close switch between amuxbusb and vplus signal. Write with '1' to set bit. Default Value: 0
18	MUX_FW_AMUXBUSA_VPLUS	Firmware control: 0=open, 1=close switch between amuxbusa and vplus signal. Write with '1' to set bit. Default Value: 0
17	MUX_FW_TEMP_VPLUS	Firmware control: 0=open, 1=close switch between temperature sensor and vplus signal, also powers on the temperature sensor. Write with '1' to set bit. Default Value: 0
16	MUX_FW_VSSA_VMINUS	Firmware control: 0=open, 1=close switch between vssa_kelvin and vminus signal. Write with '1' to set bit. Default Value: 0
15	MUX_FW_P7_VMINUS	Firmware control: 0=open, 1=close switch between pin P7 and vminus signal. Write with '1' to set bit. Default Value: 0
14	MUX_FW_P6_VMINUS	Firmware control: 0=open, 1=close switch between pin P6 and vminus signal. Write with '1' to set bit. Default Value: 0
13	MUX_FW_P5_VMINUS	Firmware control: 0=open, 1=close switch between pin P5 and vminus signal. Write with '1' to set bit. Default Value: 0
12	MUX_FW_P4_VMINUS	Firmware control: 0=open, 1=close switch between pin P4 and vminus signal. Write with '1' to set bit. Default Value: 0
11	MUX_FW_P3_VMINUS	Firmware control: 0=open, 1=close switch between pin P3 and vminus signal. Write with '1' to set bit. Default Value: 0
10	MUX_FW_P2_VMINUS	Firmware control: 0=open, 1=close switch between pin P2 and vminus signal. Write with '1' to set bit. Default Value: 0
9	MUX_FW_P1_VMINUS	Firmware control: 0=open, 1=close switch between pin P1 and vminus signal. Write with '1' to set bit. Default Value: 0

26.1.76 SAR_MUX_SWITCH0 (continued)

8	MUX_FW_P0_VMINUS	Firmware control: 0=open, 1=close switch between pin P0 and vminus signal. Write with '1' to set bit. Default Value: 0
7	MUX_FW_P7_VPLUS	Firmware control: 0=open, 1=close switch between pin P7 and vplus signal. Write with '1' to set bit. Default Value: 0
6	MUX_FW_P6_VPLUS	Firmware control: 0=open, 1=close switch between pin P6 and vplus signal. Write with '1' to set bit. Default Value: 0
5	MUX_FW_P5_VPLUS	Firmware control: 0=open, 1=close switch between pin P5 and vplus signal. Write with '1' to set bit. Default Value: 0
4	MUX_FW_P4_VPLUS	Firmware control: 0=open, 1=close switch between pin P4 and vplus signal. Write with '1' to set bit. Default Value: 0
3	MUX_FW_P3_VPLUS	Firmware control: 0=open, 1=close switch between pin P3 and vplus signal. Write with '1' to set bit. Default Value: 0
2	MUX_FW_P2_VPLUS	Firmware control: 0=open, 1=close switch between pin P2 and vplus signal. Write with '1' to set bit. Default Value: 0
1	MUX_FW_P1_VPLUS	Firmware control: 0=open, 1=close switch between pin P1 and vplus signal. Write with '1' to set bit. Default Value: 0
0	MUX_FW_P0_VPLUS	Firmware control: 0=open, 1=close switch between pin P0 and vplus signal. Write with '1' to set bit. Default Value: 0

26.1.77 SAR_MUX_SWITCH_CLEAR0

SARMUX Firmware switch control clear

Address: 0x403A0304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_FW_P7_VPLUS	MUX_FW_P6_VPLUS	MUX_FW_P5_VPLUS	MUX_FW_P4_VPLUS	MUX_FW_P3_VPLUS	MUX_FW_P2_VPLUS	MUX_FW_P1_VPLUS	MUX_FW_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_FW_P7_VMINUS	MUX_FW_P6_VMINUS	MUX_FW_P5_VMINUS	MUX_FW_P4_VMINUS	MUX_FW_P3_VMINUS	MUX_FW_P2_VMINUS	MUX_FW_P1_VMINUS	MUX_FW_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_FW_SARBUS1_VPLUS	MUX_FW_SARBUS0_VPLUS	MUX_FW_AMUXBUSB_VMINUS	MUX_FW_AMUXBUSA_VMINUS	MUX_FW_AMUXBUSB_VPLUS	MUX_FW_AMUXBUSA_VPLUS	MUX_FW_TEMP_VPLUS	MUX_FW_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		A	A	A	A	A	A
Name	None [31:30]		MUX_FW_P7_COREIO3	MUX_FW_P6_COREIO2	MUX_FW_P5_COREIO1	MUX_FW_P4_COREIO0	MUX_FW_SARBUS1_VMINUS	MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
29	MUX_FW_P7_COREIO3	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
28	MUX_FW_P6_COREIO2	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
27	MUX_FW_P5_COREIO1	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
26	MUX_FW_P4_COREIO0	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
25	MUX_FW_SARBUS1_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

26.1.77 SAR_MUX_SWITCH_CLEAR0 (continued)

24	MUX_FW_SARBUS0_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
23	MUX_FW_SARBUS1_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
22	MUX_FW_SARBUS0_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
21	MUX_FW_AMUXBUSB_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
20	MUX_FW_AMUXBUSA_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
19	MUX_FW_AMUXBUSB_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
18	MUX_FW_AMUXBUSA_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
17	MUX_FW_TEMP_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
16	MUX_FW_VSSA_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
15	MUX_FW_P7_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
14	MUX_FW_P6_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
13	MUX_FW_P5_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
12	MUX_FW_P4_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
11	MUX_FW_P3_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
10	MUX_FW_P2_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
9	MUX_FW_P1_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
8	MUX_FW_P0_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
7	MUX_FW_P7_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
6	MUX_FW_P6_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
5	MUX_FW_P5_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
4	MUX_FW_P4_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
3	MUX_FW_P3_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

26.1.77 SAR_MUX_SWITCH_CLEAR0 (continued)

2	MUX_FW_P2_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
1	MUX_FW_P1_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
0	MUX_FW_P0_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

26.1.78 SAR_MUX_SWITCH_HW_CTRL

SARMUX switch hardware control

Address: 0x403A0340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	MUX_HW_CTRL_P7	MUX_HW_CTRL_P6	MUX_HW_CTRL_P5	MUX_HW_CTRL_P4	MUX_HW_CTRL_P3	MUX_HW_CTRL_P2	MUX_HW_CTRL_P1	MUX_HW_CTRL_P0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	None		RW	RW	RW	RW
HW Access	R	R	None		R	R	R	R
Name	MUX_HW_CTRL_SARBUS1	MUX_HW_CTRL_SARBUS0	None [21:20]		MUX_HW_CTRL_AMUXBUSB	MUX_HW_CTRL_AMUXBUSA	MUX_HW_CTRL_TEMP	MUX_HW_CTRL_VSSA

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	MUX_HW_CTRL_SARBUS1	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for sarbus1 switches. Default Value: 0
22	MUX_HW_CTRL_SARBUS0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for sarbus0 switches. Default Value: 0
19	MUX_HW_CTRL_AMUXBUSB	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for amuxbusb switches. Default Value: 0
18	MUX_HW_CTRL_AMUXBUSA	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for amuxbusa switches. Default Value: 0
17	MUX_HW_CTRL_TEMP	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for temp switch. Default Value: 0

26.1.78 SAR_MUX_SWITCH_HW_CTRL (continued)

16	MUX_HW_CTRL_VSSA	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for vssa switch. Default Value: 0
7	MUX_HW_CTRL_P7	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P7 switches. Default Value: 0
6	MUX_HW_CTRL_P6	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P6 switches. Default Value: 0
5	MUX_HW_CTRL_P5	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P5 switches. Default Value: 0
4	MUX_HW_CTRL_P4	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P4 switches. Default Value: 0
3	MUX_HW_CTRL_P3	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P3 switches. Default Value: 0
2	MUX_HW_CTRL_P2	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P2 switches. Default Value: 0
1	MUX_HW_CTRL_P1	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P1 switches. Default Value: 0
0	MUX_HW_CTRL_P0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P0 switches. Default Value: 0

26.1.79 SAR_MUX_SWITCH_STATUS

SARMUX switch status

Address: 0x403A0348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_FW_P7_VPLUS	MUX_FW_P6_VPLUS	MUX_FW_P5_VPLUS	MUX_FW_P4_VPLUS	MUX_FW_P3_VPLUS	MUX_FW_P2_VPLUS	MUX_FW_P1_VPLUS	MUX_FW_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_FW_P7_VMINUS	MUX_FW_P6_VMINUS	MUX_FW_P5_VMINUS	MUX_FW_P4_VMINUS	MUX_FW_P3_VMINUS	MUX_FW_P2_VMINUS	MUX_FW_P1_VMINUS	MUX_FW_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_FW_SARBUS1_VPLUS	MUX_FW_SARBUS0_VPLUS	MUX_FW_AMUXBUSB_VMINUS	MUX_FW_AMUXBUSA_VMINUS	MUX_FW_AMUXBUSB_VPLUS	MUX_FW_AMUXBUSA_VPLUS	MUX_FW_TEMP_VPLUS	MUX_FW_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						W	W
Name	None [31:26]						MUX_FW_SARBUS1_VMINUS	MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
25	MUX_FW_SARBUS1_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
24	MUX_FW_SARBUS0_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
23	MUX_FW_SARBUS1_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
22	MUX_FW_SARBUS0_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
21	MUX_FW_AMUXBUSB_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0

26.1.79 SAR_MUX_SWITCH_STATUS (continued)

20	MUX_FW_AMUXBUSA_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
19	MUX_FW_AMUXBUSB_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
18	MUX_FW_AMUXBUSA_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
17	MUX_FW_TEMP_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
16	MUX_FW_VSSA_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
15	MUX_FW_P7_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
14	MUX_FW_P6_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
13	MUX_FW_P5_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
12	MUX_FW_P4_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
11	MUX_FW_P3_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
10	MUX_FW_P2_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
9	MUX_FW_P1_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
8	MUX_FW_P0_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
7	MUX_FW_P7_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
6	MUX_FW_P6_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
5	MUX_FW_P5_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
4	MUX_FW_P4_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
3	MUX_FW_P3_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
2	MUX_FW_P2_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
1	MUX_FW_P1_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
0	MUX_FW_P0_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0

26.1.80 SAR_PUMP_CTRL

Switch pump control

Address: 0x403A0380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							CLOCK_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	0=disabled: pump output is VDDA_PUMP, 1=enabled: pump output is boosted. Default Value: 0
0	CLOCK_SEL	Clock select: 0=external clock, 1=internal clock (deprecated). Default Value: 0

26.1.81 SAR_ANA_TRIM

Analog trim register.

Address: 0x403A0F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW		
HW Access	None				R	R		
Name	None [7:4]				TRIMUNIT	CAP_TRIM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	TRIMUNIT	Attenuation cap trimming Default Value: 0
2 : 0	CAP_TRIM	Attenuation cap trimming Default Value: 0

27 SCB Registers

This section discusses the SCB registers. It lists all the registers in mapping tables, in address order.

27.1 Register Details

Register Name	Address
SCB0_CTRL	0x40240000
SCB0_STATUS	0x40240004
SCB0_SPI_CTRL	0x40240020
SCB0_SPI_STATUS	0x40240024
SCB0_UART_CTRL	0x40240040
SCB0_UART_TX_CTRL	0x40240044
SCB0_UART_RX_CTRL	0x40240048
SCB0_UART_RX_STATUS	0x4024004C
SCB0_UART_FLOW_CTRL	0x40240050
SCB0_I2C_CTRL	0x40240060
SCB0_I2C_STATUS	0x40240064
SCB0_I2C_M_CMD	0x40240068
SCB0_I2C_S_CMD	0x4024006C
SCB0_I2C_CFG	0x40240070
SCB0_TX_CTRL	0x40240200
SCB0_TX_FIFO_CTRL	0x40240204
SCB0_TX_FIFO_STATUS	0x40240208
SCB0_TX_FIFO_WR	0x40240240
SCB0_RX_CTRL	0x40240300
SCB0_RX_FIFO_CTRL	0x40240304
SCB0_RX_FIFO_STATUS	0x40240308
SCB0_RX_MATCH	0x40240310
SCB0_RX_FIFO_RD	0x40240340
SCB0_RX_FIFO_RD_SILENT	0x40240344
SCB0_EZ_DATA0	0x40240400
SCB0_EZ_DATA1	0x40240404
SCB0_EZ_DATA2	0x40240408

Register Name	Address
SCB0_EZ_DATA3	0x4024040C
SCB0_EZ_DATA4	0x40240410
SCB0_EZ_DATA5	0x40240414
SCB0_EZ_DATA6	0x40240418
SCB0_EZ_DATA7	0x4024041C
SCB0_EZ_DATA8	0x40240420
SCB0_EZ_DATA9	0x40240424
SCB0_EZ_DATA10	0x40240428
SCB0_EZ_DATA11	0x4024042C
SCB0_EZ_DATA12	0x40240430
SCB0_EZ_DATA13	0x40240434
SCB0_EZ_DATA14	0x40240438
SCB0_EZ_DATA15	0x4024043C
SCB0_EZ_DATA16	0x40240440
SCB0_EZ_DATA17	0x40240444
SCB0_EZ_DATA18	0x40240448
SCB0_EZ_DATA19	0x4024044C
SCB0_EZ_DATA20	0x40240450
SCB0_EZ_DATA21	0x40240454
SCB0_EZ_DATA22	0x40240458
SCB0_EZ_DATA23	0x4024045C
SCB0_EZ_DATA24	0x40240460
SCB0_EZ_DATA25	0x40240464
SCB0_EZ_DATA26	0x40240468
SCB0_EZ_DATA27	0x4024046C
SCB0_EZ_DATA28	0x40240470
SCB0_EZ_DATA29	0x40240474
SCB0_EZ_DATA30	0x40240478
SCB0_EZ_DATA31	0x4024047C
SCB0_INTR_CAUSE	0x40240E00
SCB0_INTR_I2C_EC	0x40240E80
SCB0_INTR_I2C_EC_MASK	0x40240E88
SCB0_INTR_I2C_EC_MASKED	0x40240E8C
SCB0_INTR_SPI_EC	0x40240EC0
SCB0_INTR_SPI_EC_MASK	0x40240EC8
SCB0_INTR_SPI_EC_MASKED	0x40240ECC
SCB0_INTR_M	0x40240F00
SCB0_INTR_M_SET	0x40240F04
SCB0_INTR_M_MASK	0x40240F08
SCB0_INTR_M_MASKED	0x40240F0C
SCB0_INTR_S	0x40240F40
SCB0_INTR_S_SET	0x40240F44

Register Name	Address
SCB0_INTR_S_MASK	0x40240F48
SCB0_INTR_S_MASKED	0x40240F4C
SCB0_INTR_TX	0x40240F80
SCB0_INTR_TX_SET	0x40240F84
SCB0_INTR_TX_MASK	0x40240F88
SCB0_INTR_TX_MASKED	0x40240F8C
SCB0_INTR_RX	0x40240FC0
SCB0_INTR_RX_SET	0x40240FC4
SCB0_INTR_RX_MASK	0x40240FC8
SCB0_INTR_RX_MASKED	0x40240FCC
SCB1_CTRL	0x40250000
SCB1_STATUS	0x40250004
SCB1_SPI_CTRL	0x40250020
SCB1_SPI_STATUS	0x40250024
SCB1_UART_CTRL	0x40250040
SCB1_UART_TX_CTRL	0x40250044
SCB1_UART_RX_CTRL	0x40250048
SCB1_UART_RX_STATUS	0x4025004C
SCB1_UART_FLOW_CTRL	0x40250050
SCB1_I2C_CTRL	0x40250060
SCB1_I2C_STATUS	0x40250064
SCB1_I2C_M_CMD	0x40250068
SCB1_I2C_S_CMD	0x4025006C
SCB1_I2C_CFG	0x40250070
SCB1_TX_CTRL	0x40250200
SCB1_TX_FIFO_CTRL	0x40250204
SCB1_TX_FIFO_STATUS	0x40250208
SCB1_TX_FIFO_WR	0x40250240
SCB1_RX_CTRL	0x40250300
SCB1_RX_FIFO_CTRL	0x40250304
SCB1_RX_FIFO_STATUS	0x40250308
SCB1_RX_MATCH	0x40250310
SCB1_RX_FIFO_RD	0x40250340
SCB1_RX_FIFO_RD_SILENT	0x40250344
SCB1_EZ_DATA0	0x40250400
SCB1_EZ_DATA1	0x40250404
SCB1_EZ_DATA2	0x40250408
SCB1_EZ_DATA3	0x4025040C
SCB1_EZ_DATA4	0x40250410
SCB1_EZ_DATA5	0x40250414
SCB1_EZ_DATA6	0x40250418
SCB1_EZ_DATA7	0x4025041C

Register Name	Address
SCB1_EZ_DATA8	0x40250420
SCB1_EZ_DATA9	0x40250424
SCB1_EZ_DATA10	0x40250428
SCB1_EZ_DATA11	0x4025042C
SCB1_EZ_DATA12	0x40250430
SCB1_EZ_DATA13	0x40250434
SCB1_EZ_DATA14	0x40250438
SCB1_EZ_DATA15	0x4025043C
SCB1_EZ_DATA16	0x40250440
SCB1_EZ_DATA17	0x40250444
SCB1_EZ_DATA18	0x40250448
SCB1_EZ_DATA19	0x4025044C
SCB1_EZ_DATA20	0x40250450
SCB1_EZ_DATA21	0x40250454
SCB1_EZ_DATA22	0x40250458
SCB1_EZ_DATA23	0x4025045C
SCB1_EZ_DATA24	0x40250460
SCB1_EZ_DATA25	0x40250464
SCB1_EZ_DATA26	0x40250468
SCB1_EZ_DATA27	0x4025046C
SCB1_EZ_DATA28	0x40250470
SCB1_EZ_DATA29	0x40250474
SCB1_EZ_DATA30	0x40250478
SCB1_EZ_DATA31	0x4025047C
SCB1_INTR_CAUSE	0x40250E00
SCB1_INTR_I2C_EC	0x40250E80
SCB1_INTR_I2C_EC_MASK	0x40250E88
SCB1_INTR_I2C_EC_MASKED	0x40250E8C
SCB1_INTR_SPI_EC	0x40250EC0
SCB1_INTR_SPI_EC_MASK	0x40250EC8
SCB1_INTR_SPI_EC_MASKED	0x40250ECC
SCB1_INTR_M	0x40250F00
SCB1_INTR_M_SET	0x40250F04
SCB1_INTR_M_MASK	0x40250F08
SCB1_INTR_M_MASKED	0x40250F0C
SCB1_INTR_S	0x40250F40
SCB1_INTR_S_SET	0x40250F44
SCB1_INTR_S_MASK	0x40250F48
SCB1_INTR_S_MASKED	0x40250F4C
SCB1_INTR_TX	0x40250F80
SCB1_INTR_TX_SET	0x40250F84
SCB1_INTR_TX_MASK	0x40250F88

Register Name	Address
SCB1_INTR_TX_MASKED	0x40250F8C
SCB1_INTR_RX	0x40250FC0
SCB1_INTR_RX_SET	0x40250FC4
SCB1_INTR_RX_MASK	0x40250FC8
SCB1_INTR_RX_MASKED	0x40250FCC
SCB2_CTRL	0x40260000
SCB2_STATUS	0x40260004
SCB2_SPI_CTRL	0x40260020
SCB2_SPI_STATUS	0x40260024
SCB2_UART_CTRL	0x40260040
SCB2_UART_TX_CTRL	0x40260044
SCB2_UART_RX_CTRL	0x40260048
SCB2_UART_RX_STATUS	0x4026004C
SCB2_UART_FLOW_CTRL	0x40260050
SCB2_I2C_CTRL	0x40260060
SCB2_I2C_STATUS	0x40260064
SCB2_I2C_M_CMD	0x40260068
SCB2_I2C_S_CMD	0x4026006C
SCB2_I2C_CFG	0x40260070
SCB2_TX_CTRL	0x40260200
SCB2_TX_FIFO_CTRL	0x40260204
SCB2_TX_FIFO_STATUS	0x40260208
SCB2_TX_FIFO_WR	0x40260240
SCB2_RX_CTRL	0x40260300
SCB2_RX_FIFO_CTRL	0x40260304
SCB2_RX_FIFO_STATUS	0x40260308
SCB2_RX_MATCH	0x40260310
SCB2_RX_FIFO_RD	0x40260340
SCB2_RX_FIFO_RD_SILENT	0x40260344
SCB2_EZ_DATA0	0x40260400
SCB2_EZ_DATA1	0x40260404
SCB2_EZ_DATA2	0x40260408
SCB2_EZ_DATA3	0x4026040C
SCB2_EZ_DATA4	0x40260410
SCB2_EZ_DATA5	0x40260414
SCB2_EZ_DATA6	0x40260418
SCB2_EZ_DATA7	0x4026041C
SCB2_EZ_DATA8	0x40260420
SCB2_EZ_DATA9	0x40260424
SCB2_EZ_DATA10	0x40260428
SCB2_EZ_DATA11	0x4026042C
SCB2_EZ_DATA12	0x40260430

Register Name	Address
SCB2_EZ_DATA13	0x40260434
SCB2_EZ_DATA14	0x40260438
SCB2_EZ_DATA15	0x4026043C
SCB2_EZ_DATA16	0x40260440
SCB2_EZ_DATA17	0x40260444
SCB2_EZ_DATA18	0x40260448
SCB2_EZ_DATA19	0x4026044C
SCB2_EZ_DATA20	0x40260450
SCB2_EZ_DATA21	0x40260454
SCB2_EZ_DATA22	0x40260458
SCB2_EZ_DATA23	0x4026045C
SCB2_EZ_DATA24	0x40260460
SCB2_EZ_DATA25	0x40260464
SCB2_EZ_DATA26	0x40260468
SCB2_EZ_DATA27	0x4026046C
SCB2_EZ_DATA28	0x40260470
SCB2_EZ_DATA29	0x40260474
SCB2_EZ_DATA30	0x40260478
SCB2_EZ_DATA31	0x4026047C
SCB2_INTR_CAUSE	0x40260E00
SCB2_INTR_I2C_EC	0x40260E80
SCB2_INTR_I2C_EC_MASK	0x40260E88
SCB2_INTR_I2C_EC_MASKED	0x40260E8C
SCB2_INTR_SPI_EC	0x40260EC0
SCB2_INTR_SPI_EC_MASK	0x40260EC8
SCB2_INTR_SPI_EC_MASKED	0x40260ECC
SCB2_INTR_M	0x40260F00
SCB2_INTR_M_SET	0x40260F04
SCB2_INTR_M_MASK	0x40260F08
SCB2_INTR_M_MASKED	0x40260F0C
SCB2_INTR_S	0x40260F40
SCB2_INTR_S_SET	0x40260F44
SCB2_INTR_S_MASK	0x40260F48
SCB2_INTR_S_MASKED	0x40260F4C
SCB2_INTR_TX	0x40260F80
SCB2_INTR_TX_SET	0x40260F84
SCB2_INTR_TX_MASK	0x40260F88
SCB2_INTR_TX_MASKED	0x40260F8C
SCB2_INTR_RX	0x40260FC0
SCB2_INTR_RX_SET	0x40260FC4
SCB2_INTR_RX_MASK	0x40260FC8
SCB2_INTR_RX_MASKED	0x40260FCC

Register Name	Address
SCB3_CTRL	0x40270000
SCB3_STATUS	0x40270004
SCB3_SPI_CTRL	0x40270020
SCB3_SPI_STATUS	0x40270024
SCB3_UART_CTRL	0x40270040
SCB3_UART_TX_CTRL	0x40270044
SCB3_UART_RX_CTRL	0x40270048
SCB3_UART_RX_STATUS	0x4027004C
SCB3_UART_FLOW_CTRL	0x40270050
SCB3_I2C_CTRL	0x40270060
SCB3_I2C_STATUS	0x40270064
SCB3_I2C_M_CMD	0x40270068
SCB3_I2C_S_CMD	0x4027006C
SCB3_I2C_CFG	0x40270070
SCB3_TX_CTRL	0x40270200
SCB3_TX_FIFO_CTRL	0x40270204
SCB3_TX_FIFO_STATUS	0x40270208
SCB3_TX_FIFO_WR	0x40270240
SCB3_RX_CTRL	0x40270300
SCB3_RX_FIFO_CTRL	0x40270304
SCB3_RX_FIFO_STATUS	0x40270308
SCB3_RX_MATCH	0x40270310
SCB3_RX_FIFO_RD	0x40270340
SCB3_RX_FIFO_RD_SILENT	0x40270344
SCB3_EZ_DATA0	0x40270400
SCB3_EZ_DATA1	0x40270404
SCB3_EZ_DATA2	0x40270408
SCB3_EZ_DATA3	0x4027040C
SCB3_EZ_DATA4	0x40270410
SCB3_EZ_DATA5	0x40270414
SCB3_EZ_DATA6	0x40270418
SCB3_EZ_DATA7	0x4027041C
SCB3_EZ_DATA8	0x40270420
SCB3_EZ_DATA9	0x40270424
SCB3_EZ_DATA10	0x40270428
SCB3_EZ_DATA11	0x4027042C
SCB3_EZ_DATA12	0x40270430
SCB3_EZ_DATA13	0x40270434
SCB3_EZ_DATA14	0x40270438
SCB3_EZ_DATA15	0x4027043C
SCB3_EZ_DATA16	0x40270440
SCB3_EZ_DATA17	0x40270444

Register Name	Address
SCB3_EZ_DATA18	0x40270448
SCB3_EZ_DATA19	0x4027044C
SCB3_EZ_DATA20	0x40270450
SCB3_EZ_DATA21	0x40270454
SCB3_EZ_DATA22	0x40270458
SCB3_EZ_DATA23	0x4027045C
SCB3_EZ_DATA24	0x40270460
SCB3_EZ_DATA25	0x40270464
SCB3_EZ_DATA26	0x40270468
SCB3_EZ_DATA27	0x4027046C
SCB3_EZ_DATA28	0x40270470
SCB3_EZ_DATA29	0x40270474
SCB3_EZ_DATA30	0x40270478
SCB3_EZ_DATA31	0x4027047C
SCB3_INTR_CAUSE	0x40270E00
SCB3_INTR_I2C_EC	0x40270E80
SCB3_INTR_I2C_EC_MASK	0x40270E88
SCB3_INTR_I2C_EC_MASKED	0x40270E8C
SCB3_INTR_SPI_EC	0x40270EC0
SCB3_INTR_SPI_EC_MASK	0x40270EC8
SCB3_INTR_SPI_EC_MASKED	0x40270ECC
SCB3_INTR_M	0x40270F00
SCB3_INTR_M_SET	0x40270F04
SCB3_INTR_M_MASK	0x40270F08
SCB3_INTR_M_MASKED	0x40270F0C
SCB3_INTR_S	0x40270F40
SCB3_INTR_S_SET	0x40270F44
SCB3_INTR_S_MASK	0x40270F48
SCB3_INTR_S_MASKED	0x40270F4C
SCB3_INTR_TX	0x40270F80
SCB3_INTR_TX_SET	0x40270F84
SCB3_INTR_TX_MASK	0x40270F88
SCB3_INTR_TX_MASKED	0x40270F8C
SCB3_INTR_RX	0x40270FC0
SCB3_INTR_RX_SET	0x40270FC4
SCB3_INTR_RX_MASK	0x40270FC8
SCB3_INTR_RX_MASKED	0x40270FCC

27.1.1 SCB0_CTRL

Generic control register.

Address: 0x40240000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BYTE_MODE	EZ_MODE	EC_OP_MODE	EC_AM_MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_ACCEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	IP enabled ('1') or not ('0'). The proper order in which to initialize the IP is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL to enable IP, select the specific operation mode and oversampling factor. When the IP is enabled, no control information should be changed. Changes should be made AFTER disabling the IP, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the IP is re-enabled. Note that disabling the IP will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3 **0x0: I2C:** Inter-Integrated Circuits (I2C) mode.

27.1.1 SCB0_CTRL (continued)

		0x1: SPI: Serial Peripheral Interface (SPI) mode. **0x2: UART:** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the MMIO SW accesses to EZ memory coincide/collide, this bit determines whether a SW access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is ¡®0¡¯ and the accesses collide, MMIO read operations return 0xffff:ffff and MMIO write operations are ignored. Colliding accesses are registered as interrupt causes: field BLOCKED of MMIO registers INTR_TX and INTR_RX. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when ADDR_ACCEPT is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
11	BYTE_MODE	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. Default Value: 0
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames mot seperated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0
9	EC_OP_MODE	Internally clocked mode ('0') or externally clocked mode ('1') operation. In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0

27.1.1 SCB0_CTRL (continued)

8	EC_AM_MODE	Internally clocked mode ('0') or externally clocked mode ('1') address matching (I2C) or selection (SPI). In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'. Default Value: 0
3 : 0	OVS	Serial interface bit period oversampling factor expressed in IP clock cycles. Used for SPI and UART functionality. OVS + 1 IP clock cycles constitute a single serial interface clock/bit cycle. The IP clock is provided by the programmable clock IP. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the first and second phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the first phase of the interface clock period is 1 peripheral clock cycle longer than the second phase of the interface clock period. In SPI master mode, the valid range is [3, 15]. At an IP frequency of 48 MHz, the maximum IP bit rate is 12 Mbps. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock "spi_clk_out" to SPI MISO input "spi_miso_in" round trip delay is introducing significant delays (multiple "spi_clk_out" cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. The maximum IP bit rate of 12 Mbps provides an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the IP clock wrt. the interface (IF) clock to guarantee functional correct behavior. This requirement is expressed as a ratio: IP clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 6. At a IP frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 3. At a IP frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 8. At a IP frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 4. At a IP frequency of 48 MHz, the maximum bit rate is 12 Mbps. The maximum bit rates provide an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account.

27.1.1 SCB0_CTRL (continued)

In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15].

In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value:
- 0: 16 times oversampling.
  IP clock frequency of 16*115.2 KHz for 115.2 Kbps.
  IP clock frequency of 16*57.6 KHz for 57.6 Kbps.
  IP clock frequency of 16*38.4 KHz for 38.4 Kbps.
  IP clock frequency of 16*19.2 KHz for 19.2 Kbps.
  IP clock frequency of 16*9.6 KHz for 9.6 Kbps.
  IP clock frequency of 16*2.4 KHz for 2.4 Kbps.
  IP clock frequency of 16*1.2 KHz for 1.2 Kbps.
- all other values are not used in normal mode.

In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two IP clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two IP clock cycles and greater or equal than one IP clock cycle may be detected by the receiver. Pulse widths less than one IP clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The IP clock (as provided by the programmable clock IP) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required IP clock frequency):
- 0: 16 times oversampling.
  IP clock frequency of 16*115.2 KHz for 115.2 Kbps.
  IP clock frequency of 16*57.6 KHz for 57.6 Kbps.
  IP clock frequency of 16*38.4 KHz for 38.4 Kbps.
  IP clock frequency of 16*19.2 KHz for 19.2 Kbps.
  IP clock frequency of 16*9.6 KHz for 9.6 Kbps.
  IP clock frequency of 16*2.4 KHz for 2.4 Kbps.
  IP clock frequency of 16*1.2 KHz for 1.2 Kbps.
- all other values are not used in normal mode.

Low power mode, OVS field values (with the required IP clock frequency):
- 0: 16 times oversampling.
  IP clock frequency of 16*115.2 KHz for 115.2 Kbps.
- 1: 32 times oversampling.
  IP clock frequency of 32*57.6 KHz for 57.6 Kbps.
- 2: 48 times oversampling.
  IP clock frequency of 48*38.4 KHz for 38.4 Kbps.
- 3: 96 times oversampling.
  IP clock frequency of 96*19.2 KHz for 19.2 Kbps.
- 4: 192 times oversampling.
  IP clock frequency of 192*9.6 KHz for 9.6 Kbps.
- 5: 768 times oversampling.
  IP clock frequency of 768*2.4 KHz for 2.4 Kbps.
- 6: 1536 times oversampling.
  IP clock frequency of 1536*1.2 KHz for 1.2 Kbps.
- all other values are not used in low power mode.

Default Value: 15

27.1.2 SCB0_STATUS

Generic status register.

Address: 0x40240004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

27.1.3 SCB0_SPI_CTRL

SPI control register.

Address: 0x40240020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_CONTINUOUS	LATE_MISO_SAMPLE	CPOL	CPHA	SELECT_PRECEDE	CONTINU-OUS

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SSEL_POLARITY3	SSEL_POLARITY2	SSEL_POLARITY1	SSEL_POLARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_MODE	None [30:28]			SLAVE_SELECT [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SLAVE_SELECT	Selects one of the four outgoing SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. The IP should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

27.1.3 SCB0_SPI_CTRL (continued)

		0x0: SPI_MOTOROLA: SPI Motorola submode. In master mode, when not transmitting data (SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive. **0x1: SPI_TI:** SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS:** SPI National Semiconducturs submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': the SPI master MISO line "spi_miso_in" is connected to the SPI MISO pin. '1': the SPI master MISO line "spi_miso_in" is connected to the SPI master MOSI line "spi_mosi_out". In other words, in loopback mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. SSEL_POLARITY3 applies to the outgoing SPI slave select signal 3 (master mode). Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. SSEL_POLARITY2 applies to the outgoing SPI slave select signal 2 (master mode). Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. SSEL_POLARITY1 applies to the outgoing SPI slave select signal 1 (master mode). Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Istruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0

27.1.3 SCB0_SPI_CTRL (continued)

4	LATE_MISO_SAMPLE	Changes the SCLK edge on which MISO is captured. Only used in master mode. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 0
3	CPOL	Indicates the clock polarity. Only used in SPI Motorola submode. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is ¡®0¡¯: SCLK is ¡®0¡¯ when not transmitting data. - CPOL is ¡®1¡¯: SCLK is ¡®1¡¯ when not transmitting data. Default Value: 0
2	CPHA	Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is ¡®0¡¯, CPHA is ¡®0¡¯: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is ¡®0¡¯, CPHA is ¡®1¡¯: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is ¡®1¡¯, CPHA is ¡®0¡¯: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is ¡®1¡¯, CPHA is ¡®1¡¯: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. Default Value: 0
1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0
0	CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled individual data frame transfers are not necessarily seperated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always seperated by slave deselection: independent of the availability of TX FIFO data frames, data+G65 frames are send out with slave deselection. Default Value: 0

27.1.4 SCB0_SPI_STATUS

SPI status register.

Address: 0x40240024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
1	SPI_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection (low active) is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

27.1.5 SCB0_UART_CTRL

UART control register.

Address: 0x40240040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD:** Standard UART submode. **0x1: UART_SMARTCARD:** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA:** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS is 15.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). When '0', the transmitter TX line "uart_tx_out" is connected to the TX pin and the receiver RX line "uart_rx_in" is connected to the RX pin. When '1', the transmitter TX line "uart_tx_out" is connected to the receiver RX line "uart_rx_in". A similar connections scheme is followed for "uart_rts_out" and "uart_cts_in". This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

27.1.6 SCB0_UART_TX_CTRL

UART transmitter control register.

Address: 0x40240044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

27.1.7 SCB0_UART_RX_CTRL

UART receiver control register.

Address: 0x40240048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SKIP_START	LIN_MODE	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

27.1.7 SCB0_UART_RX_CTRL (continued)

13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame seperates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	DROP_ON_FRAME_ERROR	Behaviour when an error is detected in a start or stop period. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	DROP_ON_PARITY_ERROR	Behaviour when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal "uart_rx_in". Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

27.1.7 SCB0_UART_RX_CTRL (continued)

2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle ('1') time between data frames and the data frame value. Default Value: 2

27.1.8 SCB0_UART_RX_STATUS

UART receiver status register.

Address: 0x4024004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	Amount of peripheral clock periods that constitute the transmission of a 0x55 data frame (sent least signficant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of peripheral clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

27.1.9 SCB0_UART_FLOW_CTRL

UART flow control register

Address: 0x40240050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	Enable use of CTS input signal "uart_cts_in" by the UART transmitter: '0': Disabled. The UART transmitter ignores "uart_cts_in", and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses "uart_cts_in" to qualify the transmission of data. It transmits when "uart_cts_in" is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', "uart_cts_in" is connected to "uart_rts_out" in the IP (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY). Default Value: 0
24	CTS_POLARITY	Polarity of the CTS input signal "uart_cts_in": '0': CTS is low/'0' active; "uart_cts_in" is '0' when active and "uart_cts_in" is '1' when inactive. '1': CTS is high/'1' active; "uart_cts_in" is '1' when active and "uart_cts_in" is '0' when inactive. Default Value: 0

27.1.9 SCB0_UART_FLOW_CTRL (continued)

16	RTS_POLARITY	Polarity of the RTS output signal "uart_rts_out": '0': RTS is low/'0' active; "uart_rts_out" is '0' when active and "uart_rts_out" is '1' when inactive. '1': RTS is high/'1' active; "uart_rts_out" is '1' when active and "uart_rts_out" is '0' when inactive. During IP reset (Hibernate system power mode), "uart_rts_out" is '1'. This represents an inactive state assuming a low/'0' active polarity. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal "uart_rts_out" is activated. By setting this field to "0", flow control is effectively SW disabled (may be useful for debug purposes). Default Value: 0

27.1.10 SCB0_I2C_CTRL

I2C control register.

Address: 0x40240060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_READY_DATA_NACK	S_NOT_READY_ADDR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENERAL_IGNORE	None	M_NOT_READY_DATA_NACK	M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_MODE	SLAVE_MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', the I2C SCL and SDA lines are connected to the I2C SCL and SDA pins. When '1', I2C SCL and SDA lines are routed internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0
15	S_NOT_READY_DATA_NACK	For internally clocked logic only. Only used when: - non EZ mode. Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1

27.1.10 SCB0_I2C_CTRL (continued)

14	S_NOT_READY_ADDR_NACK	For internally clocked logic (EC_AM is '0' and EC_OP is '0') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when: - EC_AM is '0', EC_OP is '0' and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the internally clocked logic is enabled (we are in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2). the internally clocked logic is not enabled (we are in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the internally clocked logic takes over). The internally clocked logic will handle the ongoing transfer as soon as it is enabled. Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	M_NOT_READY_DATA_NACK	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1
7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 peripheral clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular (no stretching) interface (IF) low time to guarantee functional correct behavior. With input signal median filtering, the IF low time should be >= 8 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 IP clock cycles and <= 16 IP clock cycles. Default Value: 8

27.1.10 SCB0_I2C_CTRL (continued)

3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 peripheral clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF high time should be >= 5 IP clock cycles and <= 16 IP clock cycles. Default Value: 8

27.1.11 SCB0_I2C_STATUS

I2C status register.

Address: 0x40240064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	R
HW Access	None		W	W	None		W	W
Name	None [7:6]		M_READ	S_READ	None [3:2]		I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0

27.1.11 SCB0_I2C_STATUS (continued)

1	I2C_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If the IP is disabled, BUS_BUSY is '0'. After enabling the IP, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

27.1.12 SCB0_I2C_M_CMD

I2C master command register.

Address: 0x40240068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. This command has a higher priority than I2C_M_CMD.M_START: in situations where both a STOP and a REPEATED START could be transmitted, M_STOP takes precedence over M_START. Default Value: 0
3	M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0

27.1.12 SCB0_I2C_M_CMD (continued)

0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

27.1.13 SCB0_I2C_S_CMD

I2C slave command register.

Address: 0x4024006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

27.1.14 SCB0_I2C_CFG

I2C configuration register.

Address: 0x40240070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_FILT_SEL	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_FILT_SEL	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative "i2c_sda_out" filter delay: "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 2. Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 1. Default Value: 2
17 : 16	SDA_OUT_FILT0_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 0. Default Value: 2

27.1.14 SCB0_I2C_CFG (continued)

12	SCL_IN_FILT_SEL	Selection of "i2c_scl_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim bits for "i2c_scl_in" 50 ns filter. Default Value: 0
4	SDA_IN_FILT_SEL	Selection of "i2c_sda_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim bits for "i2c_sda_in" 50 ns filter. Default Value: 3

27.1.15 SCB0_TX_CTRL

Transmitter control register.

Address: 0x40240200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. Default Value: 7

27.1.16 SCB0_TX_FIFO_CTRL

Transmitter FIFO control register.

Address: 0x40240204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

27.1.17 SCB0_TX_FIFO_STATUS

Transmitter FIFO status register.

Address: 0x40240208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:5]				USED [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is tranmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

27.1.18 SCB0_TX_FIFO_WR

Transmitter FIFO write register.

Address: 0x40240240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when TX_FIFO_CTRL.DATA_8BIT is '1', only DATA[7:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

27.1.19 SCB0_RX_CTRL

Receiver control register.

Address: 0x40240300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptability to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

27.1.20 SCB0_RX_FIFO_CTRL

Receiver FIFO control register.

Address: 0x40240304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event is generated. Default Value: 0

27.1.21 SCB0_RX_FIFO_STATUS

Receiver FIFO status register.

Address: 0x40240308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:5]				USED [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

27.1.22 SCB0_RX_MATCH

Slave address and mask register.

Address: 0x40240310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the ADDR field bits in the ADDR field take part in the matching of the slave address: MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

27.1.23 SCB0_RX_FIFO_RD

Receiver FIFO read register.

Address: 0x40240340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when RX_FIFO_CTRL.DATA_8BIT is '1', only DATA[7:0] are used. This register has a side effect when read by software: a data frame is removed from the FIFO. This may be undesirable during debug; i.e. a read during debug should NOT have a side effect. To this end, the IP uses the AHB-Lite "hmaster[0]" input signal. When this signal is '1' in the address cycle of a bus transfer, a read transfer will not have a side effect. As a result, a read from this register will not remove a data frame from the FIFO. As a result, a read from this register behaves as a read from the SCB_RX_FIFO_RD_SILENT register. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

27.1.24 SCB0_RX_FIFO_RD_SILENT

Receiver FIFO read register.

Address: 0x40240344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when RX_FIFO_CTRL.DATA_8BIT is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

27.1.25 SCB0_EZ_DATA0

Memory buffer registers.

Address: 0x40240400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.26 SCB0_EZ_DATA1

Memory buffer registers.

Address: 0x40240404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.27 SCB0_EZ_DATA2

Memory buffer registers.

Address: 0x40240408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.28 SCB0_EZ_DATA3

Memory buffer registers.

Address: 0x4024040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.29 SCB0_EZ_DATA4

Memory buffer registers.

Address: 0x40240410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.30 SCB0_EZ_DATA5

Memory buffer registers.

Address: 0x40240414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.31 SCB0_EZ_DATA6

Memory buffer registers.

Address: 0x40240418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.32 SCB0_EZ_DATA7

Memory buffer registers.

Address: 0x4024041C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.33 SCB0_EZ_DATA8

Memory buffer registers.

Address: 0x40240420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.34 SCB0_EZ_DATA9

Memory buffer registers.

Address: 0x40240424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.35 SCB0_EZ_DATA10

Memory buffer registers.

Address: 0x40240428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.36 SCB0_EZ_DATA11

Memory buffer registers.

Address: 0x4024042C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.37 SCB0_EZ_DATA12

Memory buffer registers.

Address: 0x40240430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.38 SCB0_EZ_DATA13

Memory buffer registers.

Address: 0x40240434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.39 SCB0_EZ_DATA14

Memory buffer registers.

Address: 0x40240438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.40 SCB0_EZ_DATA15

Memory buffer registers.

Address: 0x4024043C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.41 SCB0_EZ_DATA16

Memory buffer registers.

Address: 0x40240440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.42 SCB0_EZ_DATA17

Memory buffer registers.

Address: 0x40240444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.43 SCB0_EZ_DATA18

Memory buffer registers.

Address: 0x40240448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.44 SCB0_EZ_DATA19

Memory buffer registers.

Address: 0x4024044C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.45 SCB0_EZ_DATA20

Memory buffer registers.

Address: 0x40240450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.46 SCB0_EZ_DATA21

Memory buffer registers.

Address: 0x40240454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.47 SCB0_EZ_DATA22

Memory buffer registers.

Address: 0x40240458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.48 SCB0_EZ_DATA23

Memory buffer registers.

Address: 0x4024045C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.49 SCB0_EZ_DATA24

Memory buffer registers.

Address: 0x40240460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.50 SCB0_EZ_DATA25

Memory buffer registers.

Address: 0x40240464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.51 SCB0_EZ_DATA26

Memory buffer registers.

Address: 0x40240468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.52 SCB0_EZ_DATA27

Memory buffer registers.

Address: 0x4024046C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.53 SCB0_EZ_DATA28

Memory buffer registers.

Address: 0x40240470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.54 SCB0_EZ_DATA29

Memory buffer registers.

Address: 0x40240474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.55 SCB0_EZ_DATA30

Memory buffer registers.

Address: 0x40240478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.56 SCB0_EZ_DATA31

Memory buffer registers.

Address: 0x4024047C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.57 SCB0_INTR_CAUSE

Active clocked interrupt signal register

Address: 0x40240E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

27.1.58 SCB0_INTR_I2C_EC

Externally clocked I2C interrupt request register

Address: 0x40240E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0

27.1.58 SCB0_INTR_I2C_EC (continued)

0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when EC_AM is '1'. Default Value: 0

27.1.59 SCB0_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask register

Address: 0x40240E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.60 SCB0_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked register

Address: 0x40240E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

27.1.61 SCB0_INTR_SPI_EC

Externally clocked SPI interrupt request register

Address: 0x40240EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI de-selection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI de-selection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when EC_OP is '1'. Default Value: 0

27.1.61 SCB0_INTR_SPI_EC (continued)

0	WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when EC_AM is '1'. Default Value: 0

27.1.62 SCB0_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask register

Address: 0x40240EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.63 SCB0_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked register

Address: 0x40240ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

27.1.64 SCB0_INTR_M

Master interrupt request register.

Address: 0x40240F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO is empty. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0

27.1.64 SCB0_INTR_M (continued)

0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Default Value: 0

27.1.65 SCB0_INTR_M_SET

Master interrupt set request register

Address: 0x40240F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.66 SCB0_INTR_M_MASK

Master interrupt mask register.

Address: 0x40240F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.67 SCB0_INTR_M_MASKED

Master interrupt masked request register

Address: 0x40240F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

27.1.68 SCB0_INTR_S

Slave interrupt request register.

Address: 0x40240F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

27.1.68 SCB0_INTR_S (continued)

7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (till the internally clocked logic takes over) (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

27.1.69 SCB0_INTR_S_SET

Slave interrupt set request register.

Address: 0x40240F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.69 SCB0_INTR_S_SET (continued)

4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.70 SCB0_INTR_S_MASK

Slave interrupt mask register.

Address: 0x40240F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.70 SCB0_INTR_S_MASK (continued)

4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.71 SCB0_INTR_S_MASKED

Slave interrupt masked request register

Address: 0x40240F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0

27.1.71 SCB0_INTR_S_MASKED (continued)

4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

27.1.72 SCB0_INTR_TX

Transmitter interrupt request register.

Address: 0x40240F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is '1'. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	BLOCKED	AHB-Lite write transfer can not get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0

27.1.72 SCB0_INTR_TX (continued)

6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when the IP is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on TX_FIFO_CTRL.DATA_8BIT: DATA_8BIT is '0': # entries != FF_DATA_NR/2. DATA_8BIT is '1': # entries != FF_DATA_NR. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL. Only used in FIFO mode. Default Value: 0

27.1.73 SCB0_INTR_TX_SET

Transmitter interrupt set request register

Address: 0x40240F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.73 SCB0_INTR_TX_SET (continued)

1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.74 SCB0_INTR_TX_MASK

Transmitter interrupt mask register.

Address: 0x40240F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.74 SCB0_INTR_TX_MASK (continued)

1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.75 SCB0_INTR_TX_MASKED

Transmitter interrupt masked request register

Address: 0x40240F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0

27.1.75 SCB0_INTR_TX_MASKED (continued)

1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

27.1.76 SCB0_INTR_RX

Receiver interrupt request register.

Address: 0x40240FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is ecpected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STATUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

27.1.76 SCB0_INTR_RX (continued)

9	PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0
8	FRAME_ERROR	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
7	BLOCKED	AHB-Lite read transfer can not get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on RX_FIFO_CTRL.DATA_8BIT: DATA_8BIT is '0': # entries == FF_DATA_NR/2. DATA_8BIT is '1': # entries == FF_DATA_NR. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FIFO_CTL. Only used in FIFO mode. Default Value: 0

27.1.77 SCB0_INTR_RX_SET

Receiver interrupt set request register.

Address: 0x40240FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

27.1.77 SCB0_INTR_RX_SET (continued)

3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.78 SCB0_INTR_RX_MASK

Receiver interrupt mask register.

Address: 0x40240FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.78 SCB0_INTR_RX_MASK (continued)

3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.79 SCB0_INTR_RX_MASKED

Receiver interrupt masked request register

Address: 0x40240FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

27.1.79 SCB0_INTR_RX_MASKED (continued)

3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

27.1.80 SCB1_CTRL

Generic control register.

Address: 0x40250000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BYTE_MODE	EZ_MODE	EC_OP_MODE	EC_AM_MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_ACCEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	IP enabled ('1') or not ('0'). The proper order in which to initialize the IP is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL to enable IP, select the specific operation mode and oversampling factor. When the IP is enabled, no control information should be changed. Changes should be made AFTER disabling the IP, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the IP is re-enabled. Note that disabling the IP will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3 **0x0: I2C:** Inter-Integrated Circuits (I2C) mode.

27.1.80 SCB1_CTRL (continued)

		0x1: SPI: Serial Peripheral Interface (SPI) mode. **0x2: UART:** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the MMIO SW accesses to EZ memory coincide/collide, this bit determines whether a SW access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is ¡®0¡¯ and the accesses collide, MMIO read operations return 0xffff:ffff and MMIO write operations are ignored. Colliding accesses are registered as interrupt causes: field BLOCKED of MMIO registers INTR_TX and INTR_RX. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when ADDR_ACCEPT is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
11	BYTE_MODE	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. Default Value: 0
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames mot seperated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0
9	EC_OP_MODE	Internally clocked mode ('0') or externally clocked mode ('1') operation. In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0

27.1.80 SCB1_CTRL (continued)

8	EC_AM_MODE	Internally clocked mode ('0') or externally clocked mode ('1') address matching (I2C) or selection (SPI). In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'. Default Value: 0
3 : 0	OVS	Serial interface bit period oversampling factor expressed in IP clock cycles. Used for SPI and UART functionality. OVS + 1 IP clock cycles constitute a single serial interface clock/bit cycle. The IP clock is provided by the programmable clock IP. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the first and second phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the first phase of the interface clock period is 1 peripheral clock cycle longer than the second phase of the interface clock period. In SPI master mode, the valid range is [3, 15]. At an IP frequency of 48 MHz, the maximum IP bit rate is 12 Mbps. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock "spi_clk_out" to SPI MISO input "spi_miso_in" round trip delay is introducing significant delays (multiple "spi_clk_out" cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. The maximum IP bit rate of 12 Mbps provides an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the IP clock wrt. the interface (IF) clock to guarantee functional correct behavior. This requirement is expressed as a ratio: IP clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 6. At a IP frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 3. At a IP frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 8. At a IP frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 4. At a IP frequency of 48 MHz, the maximum bit rate is 12 Mbps. The maximum bit rates provide an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account.

27.1.80 SCB1_CTRL (continued)

In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15].

In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value:
- 0: 16 times oversampling.
  IP clock frequency of 16*115.2 KHz for 115.2 Kbps.
  IP clock frequency of 16*57.6 KHz for 57.6 Kbps.
  IP clock frequency of 16*38.4 KHz for 38.4 Kbps.
  IP clock frequency of 16*19.2 KHz for 19.2 Kbps.
  IP clock frequency of 16*9.6 KHz for 9.6 Kbps.
  IP clock frequency of 16*2.4 KHz for 2.4 Kbps.
  IP clock frequency of 16*1.2 KHz for 1.2 Kbps.
- all other values are not used in normal mode.

In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two IP clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two IP clock cycles and greater or equal than one IP clock cycle may be detected by the receiver. Pulse widths less than one IP clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The IP clock (as provided by the programmable clock IP) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required IP clock frequency):
- 0: 16 times oversampling.
  IP clock frequency of 16*115.2 KHz for 115.2 Kbps.
  IP clock frequency of 16*57.6 KHz for 57.6 Kbps.
  IP clock frequency of 16*38.4 KHz for 38.4 Kbps.
  IP clock frequency of 16*19.2 KHz for 19.2 Kbps.
  IP clock frequency of 16*9.6 KHz for 9.6 Kbps.
  IP clock frequency of 16*2.4 KHz for 2.4 Kbps.
  IP clock frequency of 16*1.2 KHz for 1.2 Kbps.
- all other values are not used in normal mode.

Low power mode, OVS field values (with the required IP clock frequency):
- 0: 16 times oversampling.
  IP clock frequency of 16*115.2 KHz for 115.2 Kbps.
- 1: 32 times oversampling.
  IP clock frequency of 32*57.6 KHz for 57.6 Kbps.
- 2: 48 times oversampling.
  IP clock frequency of 48*38.4 KHz for 38.4 Kbps.
- 3: 96 times oversampling.
  IP clock frequency of 96*19.2 KHz for 19.2 Kbps.
- 4: 192 times oversampling.
  IP clock frequency of 192*9.6 KHz for 9.6 Kbps.
- 5: 768 times oversampling.
  IP clock frequency of 768*2.4 KHz for 2.4 Kbps.
- 6: 1536 times oversampling.
  IP clock frequency of 1536*1.2 KHz for 1.2 Kbps.
- all other values are not used in low power mode.

Default Value: 15

27.1.81 SCB1_STATUS

Generic status register.

Address: 0x40250004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

27.1.82 SCB1_SPI_CTRL

SPI control register.

Address: 0x40250020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_CONTINUOUS	LATE_MISO_SAMPLE	CPOL	CPHA	SELECT_PRECEDE	CONTINU-OUS

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SSEL_POLARITY3	SSEL_POLARITY2	SSEL_POLARITY1	SSEL_POLARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_MODE	None [30:28]			SLAVE_SELECT [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SLAVE_SELECT	Selects one of the four outgoing SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. The IP should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

27.1.82 SCB1_SPI_CTRL (continued)

		0x0: SPI_MOTOROLA: SPI Motorola submode. In master mode, when not transmitting data (SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive. **0x1: SPI_TI:** SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS:** SPI National Semiconducturs submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': the SPI master MISO line "spi_miso_in" is connected to the SPI MISO pin. '1': the SPI master MISO line "spi_miso_in" is connected to the SPI master MOSI line "spi_mosi_out". In other words, in loopback mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. SSEL_POLARITY3 applies to the outgoing SPI slave select signal 3 (master mode). Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. SSEL_POLARITY2 applies to the outgoing SPI slave select signal 2 (master mode). Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. SSEL_POLARITY1 applies to the outgoing SPI slave select signal 1 (master mode). Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Istruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0

27.1.82 SCB1_SPI_CTRL (continued)

4	LATE_MISO_SAMPLE	Changes the SCLK edge on which MISO is captured. Only used in master mode. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 0
3	CPOL	Indicates the clock polarity. Only used in SPI Motorola submode. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is ¡®0¡¯: SCLK is ¡®0¡¯ when not transmitting data. - CPOL is ¡®1¡¯: SCLK is ¡®1¡¯ when not transmitting data. Default Value: 0
2	CPHA	Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is ¡®0¡¯, CPHA is ¡®0¡¯: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is ¡®0¡¯, CPHA is ¡®1¡¯: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is ¡®1¡¯, CPHA is ¡®0¡¯: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is ¡®1¡¯, CPHA is ¡®1¡¯: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. Default Value: 0
1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0
0	CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled individual data frame transfers are not necessarily seperated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always seperated by slave deselection: independent of the availability of TX FIFO data frames, data+G65 frames are send out with slave deselection. Default Value: 0

27.1.83 SCB1_SPI_STATUS

SPI status register.

Address: 0x40250024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
1	SPI_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection (low active) is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

27.1.84 SCB1_UART_CTRL

UART control register.

Address: 0x40250040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD:** Standard UART submode. **0x1: UART_SMARTCARD:** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA:** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS is 15.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). When '0', the transmitter TX line "uart_tx_out" is connected to the TX pin and the receiver RX line "uart_rx_in" is connected to the RX pin. When '1', the transmitter TX line "uart_tx_out" is connected to the receiver RX line "uart_rx_in". A similar connections scheme is followed for "uart_rts_out" and "uart_cts_in". This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

27.1.85 SCB1_UART_TX_CTRL

UART transmitter control register.

Address: 0x40250044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

27.1.86 SCB1_UART_RX_CTRL

UART receiver control register.

Address: 0x40250048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SKIP_START	LIN_MODE	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

27.1.86 SCB1_UART_RX_CTRL (continued)

13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame seperates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	DROP_ON_FRAME_ERROR	Behaviour when an error is detected in a start or stop period. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	DROP_ON_PARITY_ERROR	Behaviour when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal "uart_rx_in". Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

27.1.86 SCB1_UART_RX_CTRL (continued)

2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle ('1') time between data frames and the data frame value. Default Value: 2

27.1.87 SCB1_UART_RX_STATUS

UART receiver status register.

Address: 0x4025004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	Amount of peripheral clock periods that constitute the transmission of a 0x55 data frame (sent least signficant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of peripheral clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

27.1.88 SCB1_UART_FLOW_CTRL

UART flow control register

Address: 0x40250050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	Enable use of CTS input signal "uart_cts_in" by the UART transmitter: '0': Disabled. The UART transmitter ignores "uart_cts_in", and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses "uart_cts_in" to qualify the transmission of data. It transmits when "uart_cts_in" is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', "uart_cts_in" is connected to "uart_rts_out" in the IP (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY). Default Value: 0
24	CTS_POLARITY	Polarity of the CTS input signal "uart_cts_in": '0': CTS is low/'0' active; "uart_cts_in" is '0' when active and "uart_cts_in" is '1' when inactive. '1': CTS is high/'1' active; "uart_cts_in" is '1' when active and "uart_cts_in" is '0' when inactive. Default Value: 0

27.1.88 SCB1_UART_FLOW_CTRL (continued)

16	RTS_POLARITY	Polarity of the RTS output signal "uart_rts_out": '0': RTS is low/'0' active; "uart_rts_out" is '0' when active and "uart_rts_out" is '1' when inactive. '1': RTS is high/'1' active; "uart_rts_out" is '1' when active and "uart_rts_out" is '0' when inactive. During IP reset (Hibernate system power mode), "uart_rts_out" is '1'. This represents an inactive state assuming a low/'0' active polarity. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal "uart_rts_out" is activated. By setting this field to "0", flow control is effectively SW disabled (may be useful for debug purposes). Default Value: 0

27.1.89 SCB1_I2C_CTRL

I2C control register.

Address: 0x40250060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_READY_DATA_NACK	S_NOT_READY_ADDR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENERAL_IGNORE	None	M_NOT_READY_DATA_NACK	M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_MODE	SLAVE_MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', the I2C SCL and SDA lines are connected to the I2C SCL and SDA pins. When '1', I2C SCL and SDA lines are routed internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0
15	S_NOT_READY_DATA_NACK	For internally clocked logic only. Only used when: - non EZ mode. Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1

27.1.89 SCB1_I2C_CTRL (continued)

14	S_NOT_READY_ADDR_NACK	For internally clocked logic (EC_AM is '0' and EC_OP is '0') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when: - EC_AM is '0', EC_OP is '0' and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the internally clocked logic is enabled (we are in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2). the internally clocked logic is not enabled (we are in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the internally clocked logic takes over). The internally clocked logic will handle the ongoing transfer as soon as it is enabled. Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	M_NOT_READY_DATA_NACK	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1
7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 peripheral clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular (no stretching) interface (IF) low time to guarantee functional correct behavior. With input signal median filtering, the IF low time should be >= 8 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 IP clock cycles and <= 16 IP clock cycles. Default Value: 8

27.1.89 SCB1_I2C_CTRL (continued)

3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 peripheral clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF high time should be >= 5 IP clock cycles and <= 16 IP clock cycles. Default Value: 8

27.1.90 SCB1_I2C_STATUS

I2C status register.

Address: 0x40250064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	R
HW Access	None		W	W	None		W	W
Name	None [7:6]		M_READ	S_READ	None [3:2]		I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0

27.1.90 SCB1_I2C_STATUS (continued)

1	I2C_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If the IP is disabled, BUS_BUSY is '0'. After enabling the IP, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

27.1.91 SCB1_I2C_M_CMD

I2C master command register.

Address: 0x40250068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. This command has a higher priority than I2C_M_CMD.M_START: in situations where both a STOP and a REPEATED START could be transmitted, M_STOP takes precedence over M_START. Default Value: 0
3	M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0

27.1.91 SCB1_I2C_M_CMD (continued)

0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

27.1.92 SCB1_I2C_S_CMD

I2C slave command register.

Address: 0x4025006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

27.1.93 SCB1_I2C_CFG

I2C configuration register.

Address: 0x40250070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_FILT_SEL	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_FILT_SEL	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative "i2c_sda_out" filter delay: "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 2. Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 1. Default Value: 2
17 : 16	SDA_OUT_FILT0_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 0. Default Value: 2

27.1.93 SCB1_I2C_CFG (continued)

12	SCL_IN_FILT_SEL	Selection of "i2c_scl_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim bits for "i2c_scl_in" 50 ns filter. Default Value: 0
4	SDA_IN_FILT_SEL	Selection of "i2c_sda_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim bits for "i2c_sda_in" 50 ns filter. Default Value: 3

27.1.94 SCB1_TX_CTRL

Transmitter control register.

Address: 0x40250200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. Default Value: 7

27.1.95 SCB1_TX_FIFO_CTRL

Transmitter FIFO control register.

Address: 0x40250204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

27.1.96 SCB1_TX_FIFO_STATUS

Transmitter FIFO status register.

Address: 0x40250208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:5]				USED [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is tranmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

27.1.97 SCB1_TX_FIFO_WR

Transmitter FIFO write register.

Address: 0x40250240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when TX_FIFO_CTRL.DATA_8BIT is '1', only DATA[7:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

27.1.98 SCB1_RX_CTRL

Receiver control register.

Address: 0x40250300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptability to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

27.1.99 SCB1_RX_FIFO_CTRL

Receiver FIFO control register.

Address: 0x40250304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event is generated. Default Value: 0

27.1.100 SCB1_RX_FIFO_STATUS

Receiver FIFO status register.

Address: 0x40250308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:5]				USED [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

27.1.101 SCB1_RX_MATCH

Slave address and mask register.

Address: 0x40250310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the ADDR field bits in the ADDR field take part in the matching of the slave address: MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

27.1.102 SCB1_RX_FIFO_RD

Receiver FIFO read register.

Address: 0x40250340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when RX_FIFO_CTRL.DATA_8BIT is '1', only DATA[7:0] are used. This register has a side effect when read by software: a data frame is removed from the FIFO. This may be undesirable during debug; i.e. a read during debug should NOT have a side effect. To this end, the IP uses the AHB-Lite "hmaster[0]" input signal. When this signal is '1' in the address cycle of a bus transfer, a read transfer will not have a side effect. As a result, a read from this register will not remove a data frame from the FIFO. As a result, a read from this register behaves as a read from the SCB_RX_FIFO_RD_SILENT register. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

27.1.103 SCB1_RX_FIFO_RD_SILENT

Receiver FIFO read register.

Address: 0x40250344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when RX_FIFO_CTRL.DATA_8BIT is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

27.1.104 SCB1_EZ_DATA0

Memory buffer registers.

Address: 0x40250400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.105 SCB1_EZ_DATA1

Memory buffer registers.

Address: 0x40250404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.106 SCB1_EZ_DATA2

Memory buffer registers.

Address: 0x40250408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.107 SCB1_EZ_DATA3

Memory buffer registers.

Address: 0x4025040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.108 SCB1_EZ_DATA4

Memory buffer registers.

Address: 0x40250410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.109 SCB1_EZ_DATA5

Memory buffer registers.

Address: 0x40250414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.110 SCB1_EZ_DATA6

Memory buffer registers.

Address: 0x40250418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.111 SCB1_EZ_DATA7

Memory buffer registers.

Address: 0x4025041C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.112 SCB1_EZ_DATA8

Memory buffer registers.

Address: 0x40250420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.113 SCB1_EZ_DATA9

Memory buffer registers.

Address: 0x40250424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.114 SCB1_EZ_DATA10

Memory buffer registers.

Address: 0x40250428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.115 SCB1_EZ_DATA11

Memory buffer registers.

Address: 0x4025042C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.116 SCB1_EZ_DATA12

Memory buffer registers.

Address: 0x40250430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.117 SCB1_EZ_DATA13

Memory buffer registers.

Address: 0x40250434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.118 SCB1_EZ_DATA14

Memory buffer registers.

Address: 0x40250438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.119 SCB1_EZ_DATA15

Memory buffer registers.

Address: 0x4025043C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.120 SCB1_EZ_DATA16

Memory buffer registers.

Address: 0x40250440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.121 SCB1_EZ_DATA17

Memory buffer registers.

Address: 0x40250444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.122 SCB1_EZ_DATA18

Memory buffer registers.

Address: 0x40250448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.123 SCB1_EZ_DATA19

Memory buffer registers.

Address: 0x4025044C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.124 SCB1_EZ_DATA20

Memory buffer registers.

Address: 0x40250450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.125 SCB1_EZ_DATA21

Memory buffer registers.

Address: 0x40250454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.126 SCB1_EZ_DATA22

Memory buffer registers.

Address: 0x40250458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.127 SCB1_EZ_DATA23

Memory buffer registers.

Address: 0x4025045C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.128 SCB1_EZ_DATA24

Memory buffer registers.

Address: 0x40250460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.129 SCB1_EZ_DATA25

Memory buffer registers.

Address: 0x40250464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.130 SCB1_EZ_DATA26

Memory buffer registers.

Address: 0x40250468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.131 SCB1_EZ_DATA27

Memory buffer registers.

Address: 0x4025046C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.132 SCB1_EZ_DATA28

Memory buffer registers.

Address: 0x40250470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.133 SCB1_EZ_DATA29

Memory buffer registers.

Address: 0x40250474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.134 SCB1_EZ_DATA30

Memory buffer registers.

Address: 0x40250478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.135 SCB1_EZ_DATA31

Memory buffer registers.

Address: 0x4025047C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.136 SCB1_INTR_CAUSE

Active clocked interrupt signal register

Address: 0x40250E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

27.1.137 SCB1_INTR_I2C_EC

Externally clocked I2C interrupt request register

Address: 0x40250E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0

27.1.137 SCB1_INTR_I2C_EC (continued)

0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when EC_AM is '1'. Default Value: 0

27.1.138 SCB1_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask register

Address: 0x40250E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.139 SCB1_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked register

Address: 0x40250E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

27.1.140 SCB1_INTR_SPI_EC

Externally clocked SPI interrupt request register

Address: 0x40250EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI de-selection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI de-selection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when EC_OP is '1'. Default Value: 0

27.1.140 SCB1_INTR_SPI_EC (continued)

0	WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when EC_AM is '1'. Default Value: 0

27.1.141 SCB1_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask register

Address: 0x40250EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.142 SCB1_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked register

Address: 0x40250ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

27.1.143 SCB1_INTR_M

Master interrupt request register.

Address: 0x40250F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO is empty. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0

27.1.143 SCB1_INTR_M (continued)

0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Default Value: 0

27.1.144 SCB1_INTR_M_SET

Master interrupt set request register

Address: 0x40250F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.145 SCB1_INTR_M_MASK

Master interrupt mask register.

Address: 0x40250F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.146 SCB1_INTR_M_MASKED

Master interrupt masked request register

Address: 0x40250F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

27.1.147 SCB1_INTR_S

Slave interrupt request register.

Address: 0x40250F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

27.1.147 SCB1_INTR_S (continued)

7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (till the internally clocked logic takes over) (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

27.1.148 SCB1_INTR_S_SET

Slave interrupt set request register.

Address: 0x40250F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.148 SCB1_INTR_S_SET (continued)

4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.149 SCB1_INTR_S_MASK

Slave interrupt mask register.

Address: 0x40250F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.149 SCB1_INTR_S_MASK (continued)

4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.150 SCB1_INTR_S_MASKED

Slave interrupt masked request register

Address: 0x40250F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0

27.1.150 SCB1_INTR_S_MASKED (continued)

4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

27.1.151 SCB1_INTR_TX

Transmitter interrupt request register.

Address: 0x40250F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is '1'. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	BLOCKED	AHB-Lite write transfer can not get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0

27.1.151 SCB1_INTR_TX (continued)

6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when the IP is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on TX_FIFO_CTRL.DATA_8BIT: DATA_8BIT is '0': # entries != FF_DATA_NR/2. DATA_8BIT is '1': # entries != FF_DATA_NR. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL. Only used in FIFO mode. Default Value: 0

27.1.152 SCB1_INTR_TX_SET

Transmitter interrupt set request register

Address: 0x40250F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.152 SCB1_INTR_TX_SET (continued)

1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.153 SCB1_INTR_TX_MASK

Transmitter interrupt mask register.

Address: 0x40250F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.153 SCB1_INTR_TX_MASK (continued)

1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.154 SCB1_INTR_TX_MASKED

Transmitter interrupt masked request register

Address: 0x40250F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0

27.1.154 SCB1_INTR_TX_MASKED (continued)

1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

27.1.155 SCB1_INTR_RX

Receiver interrupt request register.

Address: 0x40250FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is ecpected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STATUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

27.1.155 SCB1_INTR_RX (continued)

9	PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0
8	FRAME_ERROR	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
7	BLOCKED	AHB-Lite read transfer can not get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on RX_FIFO_CTRL.DATA_8BIT: DATA_8BIT is '0': # entries == FF_DATA_NR/2. DATA_8BIT is '1': # entries == FF_DATA_NR. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FIFO_CTL. Only used in FIFO mode. Default Value: 0

27.1.156 SCB1_INTR_RX_SET

Receiver interrupt set request register.

Address: 0x40250FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

27.1.156 SCB1_INTR_RX_SET (continued)

3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.157 SCB1_INTR_RX_MASK

Receiver interrupt mask register.

Address: 0x40250FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.157 SCB1_INTR_RX_MASK (continued)

3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.158 SCB1_INTR_RX_MASKED

Receiver interrupt masked request register

Address: 0x40250FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

27.1.158 SCB1_INTR_RX_MASKED (continued)

3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

27.1.159 SCB2_CTRL

Generic control register.

Address: 0x40260000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BYTE_MODE	EZ_MODE	EC_OP_MODE	EC_AM_MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_ACCEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	IP enabled ('1') or not ('0'). The proper order in which to initialize the IP is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL to enable IP, select the specific operation mode and oversampling factor. When the IP is enabled, no control information should be changed. Changes should be made AFTER disabling the IP, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the IP is re-enabled. Note that disabling the IP will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3 **0x0: I2C:** Inter-Integrated Circuits (I2C) mode.

27.1.159 SCB2_CTRL (continued)

		0x1: SPI: Serial Peripheral Interface (SPI) mode. **0x2: UART:** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the MMIO SW accesses to EZ memory coincide/collide, this bit determines whether a SW access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is ¡®0¡¯ and the accesses collide, MMIO read operations return 0xffff:ffff and MMIO write operations are ignored. Colliding accesses are registered as interrupt causes: field BLOCKED of MMIO registers INTR_TX and INTR_RX. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when ADDR_ACCEPT is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
11	BYTE_MODE	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. Default Value: 0
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames mot seperated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0
9	EC_OP_MODE	Internally clocked mode ('0') or externally clocked mode ('1') operation. In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0

27.1.159 SCB2_CTRL (continued)

8	EC_AM_MODE	Internally clocked mode ('0') or externally clocked mode ('1') address matching (I2C) or selection (SPI). In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'. Default Value: 0
3 : 0	OVS	Serial interface bit period oversampling factor expressed in IP clock cycles. Used for SPI and UART functionality. OVS + 1 IP clock cycles constitute a single serial interface clock/bit cycle. The IP clock is provided by the programmable clock IP. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the first and second phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the first phase of the interface clock period is 1 peripheral clock cycle longer than the second phase of the interface clock period. In SPI master mode, the valid range is [3, 15]. At an IP frequency of 48 MHz, the maximum IP bit rate is 12 Mbps. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock "spi_clk_out" to SPI MISO input "spi_miso_in" round trip delay is introducing significant delays (multiple "spi_clk_out" cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. The maximum IP bit rate of 12 Mbps provides an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the IP clock wrt. the interface (IF) clock to guarantee functional correct behavior. This requirement is expressed as a ratio: IP clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 6. At a IP frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 3. At a IP frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 8. At a IP frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 4. At a IP frequency of 48 MHz, the maximum bit rate is 12 Mbps. The maximum bit rates provide an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account.

27.1.159 SCB2_CTRL (continued)

In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15].

In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value:
- 0: 16 times oversampling.
  IP clock frequency of 16*115.2 KHz for 115.2 Kbps.
  IP clock frequency of 16*57.6 KHz for 57.6 Kbps.
  IP clock frequency of 16*38.4 KHz for 38.4 Kbps.
  IP clock frequency of 16*19.2 KHz for 19.2 Kbps.
  IP clock frequency of 16*9.6 KHz for 9.6 Kbps.
  IP clock frequency of 16*2.4 KHz for 2.4 Kbps.
  IP clock frequency of 16*1.2 KHz for 1.2 Kbps.
- all other values are not used in normal mode.

In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two IP clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two IP clock cycles and greater or equal than one IP clock cycle may be detected by the receiver. Pulse widths less than one IP clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The IP clock (as provided by the programmable clock IP) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required IP clock frequency):
- 0: 16 times oversampling.
  IP clock frequency of 16*115.2 KHz for 115.2 Kbps.
  IP clock frequency of 16*57.6 KHz for 57.6 Kbps.
  IP clock frequency of 16*38.4 KHz for 38.4 Kbps.
  IP clock frequency of 16*19.2 KHz for 19.2 Kbps.
  IP clock frequency of 16*9.6 KHz for 9.6 Kbps.
  IP clock frequency of 16*2.4 KHz for 2.4 Kbps.
  IP clock frequency of 16*1.2 KHz for 1.2 Kbps.
- all other values are not used in normal mode.

Low power mode, OVS field values (with the required IP clock frequency):
- 0: 16 times oversampling.
  IP clock frequency of 16*115.2 KHz for 115.2 Kbps.
- 1: 32 times oversampling.
  IP clock frequency of 32*57.6 KHz for 57.6 Kbps.
- 2: 48 times oversampling.
  IP clock frequency of 48*38.4 KHz for 38.4 Kbps.
- 3: 96 times oversampling.
  IP clock frequency of 96*19.2 KHz for 19.2 Kbps.
- 4: 192 times oversampling.
  IP clock frequency of 192*9.6 KHz for 9.6 Kbps.
- 5: 768 times oversampling.
  IP clock frequency of 768*2.4 KHz for 2.4 Kbps.
- 6: 1536 times oversampling.
  IP clock frequency of 1536*1.2 KHz for 1.2 Kbps.
- all other values are not used in low power mode.

Default Value: 15

27.1.160 SCB2_STATUS

Generic status register.

Address: 0x40260004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

27.1.161 SCB2_SPI_CTRL

SPI control register.

Address: 0x40260020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_CONTINUOUS	LATE_MISO_SAMPLE	CPOL	CPHA	SELECT_PRECEDE	CONTINU-OUS

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SSEL_POLARITY3	SSEL_POLARITY2	SSEL_POLARITY1	SSEL_POLARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_MODE	None [30:28]			SLAVE_SELECT [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SLAVE_SELECT	Selects one of the four outgoing SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. The IP should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

27.1.161 SCB2_SPI_CTRL (continued)

		0x0: SPI_MOTOROLA: SPI Motorola submode. In master mode, when not transmitting data (SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive. **0x1: SPI_TI:** SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS:** SPI National Semiconducturs submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': the SPI master MISO line "spi_miso_in" is connected to the SPI MISO pin. '1': the SPI master MISO line "spi_miso_in" is connected to the SPI master MOSI line "spi_mosi_out". In other words, in loopback mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. SSEL_POLARITY3 applies to the outgoing SPI slave select signal 3 (master mode). Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. SSEL_POLARITY2 applies to the outgoing SPI slave select signal 2 (master mode). Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. SSEL_POLARITY1 applies to the outgoing SPI slave select signal 1 (master mode). Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Istruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0

27.1.161 SCB2_SPI_CTRL (continued)

4	LATE_MISO_SAMPLE	Changes the SCLK edge on which MISO is captured. Only used in master mode. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 0
3	CPOL	Indicates the clock polarity. Only used in SPI Motorola submode. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is ¡®0¡¯: SCLK is ¡®0¡¯ when not transmitting data. - CPOL is ¡®1¡¯: SCLK is ¡®1¡¯ when not transmitting data. Default Value: 0
2	CPHA	Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is ¡®0¡¯, CPHA is ¡®0¡¯: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is ¡®0¡¯, CPHA is ¡®1¡¯: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is ¡®1¡¯, CPHA is ¡®0¡¯: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is ¡®1¡¯, CPHA is ¡®1¡¯: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. Default Value: 0
1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0
0	CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled individual data frame transfers are not necessarily seperated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always seperated by slave deselection: independent of the availability of TX FIFO data frames, data+G65 frames are send out with slave deselection. Default Value: 0

27.1.162 SCB2_SPI_STATUS

SPI status register.

Address: 0x40260024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
1	SPI_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection (low active) is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

27.1.163 SCB2_UART_CTRL

UART control register.

Address: 0x40260040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD:** Standard UART submode. **0x1: UART_SMARTCARD:** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA:** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS is 15.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). When '0', the transmitter TX line "uart_tx_out" is connected to the TX pin and the receiver RX line "uart_rx_in" is connected to the RX pin. When '1', the transmitter TX line "uart_tx_out" is connected to the receiver RX line "uart_rx_in". A similar connections scheme is followed for "uart_rts_out" and "uart_cts_in". This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

27.1.164 SCB2_UART_TX_CTRL

UART transmitter control register.

Address: 0x40260044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

27.1.165 SCB2_UART_RX_CTRL

UART receiver control register.

Address: 0x40260048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SKIP_START	LIN_MODE	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

27.1.165 SCB2_UART_RX_CTRL (continued)

13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame seperates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	DROP_ON_FRAME_ERROR	Behaviour when an error is detected in a start or stop period. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	DROP_ON_PARITY_ERROR	Behaviour when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal "uart_rx_in". Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

27.1.165 SCB2_UART_RX_CTRL (continued)

2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle ('1') time between data frames and the data frame value. Default Value: 2

27.1.166 SCB2_UART_RX_STATUS

UART receiver status register.

Address: 0x4026004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	Amount of peripheral clock periods that constitute the transmission of a 0x55 data frame (sent least signficant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of peripheral clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

27.1.167 SCB2_UART_FLOW_CTRL

UART flow control register

Address: 0x40260050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	Enable use of CTS input signal "uart_cts_in" by the UART transmitter: '0': Disabled. The UART transmitter ignores "uart_cts_in", and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses "uart_cts_in" to qualify the transmission of data. It transmits when "uart_cts_in" is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', "uart_cts_in" is connected to "uart_rts_out" in the IP (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY). Default Value: 0
24	CTS_POLARITY	Polarity of the CTS input signal "uart_cts_in": '0': CTS is low/'0' active; "uart_cts_in" is '0' when active and "uart_cts_in" is '1' when inactive. '1': CTS is high/'1' active; "uart_cts_in" is '1' when active and "uart_cts_in" is '0' when inactive. Default Value: 0

27.1.167 SCB2_UART_FLOW_CTRL (continued)

16	RTS_POLARITY	Polarity of the RTS output signal "uart_rts_out": '0': RTS is low/'0' active; "uart_rts_out" is '0' when active and "uart_rts_out" is '1' when inactive. '1': RTS is high/'1' active; "uart_rts_out" is '1' when active and "uart_rts_out" is '0' when inactive. During IP reset (Hibernate system power mode), "uart_rts_out" is '1'. This represents an inactive state assuming a low/'0' active polarity. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal "uart_rts_out" is activated. By setting this field to "0", flow control is effectively SW disabled (may be useful for debug purposes). Default Value: 0

27.1.168 SCB2_I2C_CTRL

I2C control register.

Address: 0x40260060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_READY_DATA_NACK	S_NOT_READY_ADDR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENERAL_IGNORE	None	M_NOT_READY_DATA_NACK	M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_MODE	SLAVE_MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', the I2C SCL and SDA lines are connected to the I2C SCL and SDA pins. When '1', I2C SCL and SDA lines are routed internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0
15	S_NOT_READY_DATA_NACK	For internally clocked logic only. Only used when: - non EZ mode. Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1

27.1.168 SCB2_I2C_CTRL (continued)

14	S_NOT_READY_ADDR_NACK	For internally clocked logic (EC_AM is '0' and EC_OP is '0') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when: - EC_AM is '0', EC_OP is '0' and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the internally clocked logic is enabled (we are in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2). the internally clocked logic is not enabled (we are in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the internally clocked logic takes over). The internally clocked logic will handle the ongoing transfer as soon as it is enabled. Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	M_NOT_READY_DATA_NACK	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1
7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 peripheral clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular (no stretching) interface (IF) low time to guarantee functional correct behavior. With input signal median filtering, the IF low time should be >= 8 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 IP clock cycles and <= 16 IP clock cycles. Default Value: 8

27.1.168 SCB2_I2C_CTRL (continued)

3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 peripheral clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF high time should be >= 5 IP clock cycles and <= 16 IP clock cycles. Default Value: 8

27.1.169 SCB2_I2C_STATUS

I2C status register.

Address: 0x40260064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	R
HW Access	None		W	W	None		W	W
Name	None [7:6]		M_READ	S_READ	None [3:2]		I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0

27.1.169 SCB2_I2C_STATUS (continued)

1	I2C_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If the IP is disabled, BUS_BUSY is '0'. After enabling the IP, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

27.1.170 SCB2_I2C_M_CMD

I2C master command register.

Address: 0x40260068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. This command has a higher priority than I2C_M_CMD.M_START: in situations where both a STOP and a REPEATED START could be transmitted, M_STOP takes precedence over M_START. Default Value: 0
3	M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0

27.1.170 SCB2_I2C_M_CMD (continued)

0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

27.1.171 SCB2_I2C_S_CMD

I2C slave command register.

Address: 0x4026006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

27.1.172 SCB2_I2C_CFG

I2C configuration register.

Address: 0x40260070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_FILT_SEL	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_FILT_SEL	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative "i2c_sda_out" filter delay: "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 2. Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 1. Default Value: 2
17 : 16	SDA_OUT_FILT0_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 0. Default Value: 2

27.1.172 SCB2_I2C_CFG (continued)

12	SCL_IN_FILT_SEL	Selection of "i2c_scl_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim bits for "i2c_scl_in" 50 ns filter. Default Value: 0
4	SDA_IN_FILT_SEL	Selection of "i2c_sda_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim bits for "i2c_sda_in" 50 ns filter. Default Value: 3

27.1.173 SCB2_TX_CTRL

Transmitter control register.

Address: 0x40260200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. Default Value: 7

27.1.174 SCB2_TX_FIFO_CTRL

Transmitter FIFO control register.

Address: 0x40260204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

27.1.175 SCB2_TX_FIFO_STATUS

Transmitter FIFO status register.

Address: 0x40260208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:5]				USED [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is tranmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

27.1.176 SCB2_TX_FIFO_WR

Transmitter FIFO write register.

Address: 0x40260240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when TX_FIFO_CTRL.DATA_8BIT is '1', only DATA[7:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

27.1.177 SCB2_RX_CTRL

Receiver control register.

Address: 0x40260300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptability to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

27.1.178 SCB2_RX_FIFO_CTRL

Receiver FIFO control register.

Address: 0x40260304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event is generated. Default Value: 0

27.1.179 SCB2_RX_FIFO_STATUS

Receiver FIFO status register.

Address: 0x40260308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:5]				USED [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

27.1.180 SCB2_RX_MATCH

Slave address and mask register.

Address: 0x40260310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the ADDR field bits in the ADDR field take part in the matching of the slave address: MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

27.1.181 SCB2_RX_FIFO_RD

Receiver FIFO read register.

Address: 0x40260340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when RX_FIFO_CTRL.DATA_8BIT is '1', only DATA[7:0] are used. This register has a side effect when read by software: a data frame is removed from the FIFO. This may be undesirable during debug; i.e. a read during debug should NOT have a side effect. To this end, the IP uses the AHB-Lite "hmaster[0]" input signal. When this signal is '1' in the address cycle of a bus transfer, a read transfer will not have a side effect. As a result, a read from this register will not remove a data frame from the FIFO. As a result, a read from this register behaves as a read from the SCB_RX_FIFO_RD_SILENT register. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

27.1.182 SCB2_RX_FIFO_RD_SILENT

Receiver FIFO read register.

Address: 0x40260344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when RX_FIFO_CTRL.DATA_8BIT is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

27.1.183 SCB2_EZ_DATA0

Memory buffer registers.

Address: 0x40260400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.184 SCB2_EZ_DATA1

Memory buffer registers.

Address: 0x40260404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.185 SCB2_EZ_DATA2

Memory buffer registers.

Address: 0x40260408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.186 SCB2_EZ_DATA3

Memory buffer registers.

Address: 0x4026040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.187 SCB2_EZ_DATA4

Memory buffer registers.

Address: 0x40260410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.188 SCB2_EZ_DATA5

Memory buffer registers.

Address: 0x40260414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.189 SCB2_EZ_DATA6

Memory buffer registers.

Address: 0x40260418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.190 SCB2_EZ_DATA7

Memory buffer registers.

Address: 0x4026041C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.191 SCB2_EZ_DATA8

Memory buffer registers.

Address: 0x40260420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.192 SCB2_EZ_DATA9

Memory buffer registers.

Address: 0x40260424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.193 SCB2_EZ_DATA10

Memory buffer registers.

Address: 0x40260428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.194 SCB2_EZ_DATA11

Memory buffer registers.

Address: 0x4026042C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.195 SCB2_EZ_DATA12

Memory buffer registers.

Address: 0x40260430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.196 SCB2_EZ_DATA13

Memory buffer registers.

Address: 0x40260434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.197 SCB2_EZ_DATA14

Memory buffer registers.

Address: 0x40260438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.198 SCB2_EZ_DATA15

Memory buffer registers.

Address: 0x4026043C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.199 SCB2_EZ_DATA16

Memory buffer registers.

Address: 0x40260440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.200 SCB2_EZ_DATA17

Memory buffer registers.

Address: 0x40260444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.201 SCB2_EZ_DATA18

Memory buffer registers.

Address: 0x40260448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.202 SCB2_EZ_DATA19

Memory buffer registers.

Address: 0x4026044C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.203 SCB2_EZ_DATA20

Memory buffer registers.

Address: 0x40260450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.204 SCB2_EZ_DATA21

Memory buffer registers.

Address: 0x40260454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.205 SCB2_EZ_DATA22

Memory buffer registers.

Address: 0x40260458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.206 SCB2_EZ_DATA23

Memory buffer registers.

Address: 0x4026045C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.207 SCB2_EZ_DATA24

Memory buffer registers.

Address: 0x40260460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.208 SCB2_EZ_DATA25

Memory buffer registers.

Address: 0x40260464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.209 SCB2_EZ_DATA26

Memory buffer registers.

Address: 0x40260468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.210 SCB2_EZ_DATA27

Memory buffer registers.

Address: 0x4026046C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.211 SCB2_EZ_DATA28

Memory buffer registers.

Address: 0x40260470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.212 SCB2_EZ_DATA29

Memory buffer registers.

Address: 0x40260474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.213 SCB2_EZ_DATA30

Memory buffer registers.

Address: 0x40260478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.214 SCB2_EZ_DATA31

Memory buffer registers.

Address: 0x4026047C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.215 SCB2_INTR_CAUSE

Active clocked interrupt signal register

Address: 0x40260E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

27.1.216 SCB2_INTR_I2C_EC

Externally clocked I2C interrupt request register

Address: 0x40260E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0

27.1.216 SCB2_INTR_I2C_EC (continued)

0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when EC_AM is '1'. Default Value: 0

27.1.217 SCB2_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask register

Address: 0x40260E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.218 SCB2_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked register

Address: 0x40260E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

27.1.219 SCB2_INTR_SPI_EC

Externally clocked SPI interrupt request register

Address: 0x40260EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI de-selection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI de-selection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when EC_OP is '1'. Default Value: 0

27.1.219 SCB2_INTR_SPI_EC (continued)

0	WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when EC_AM is '1'. Default Value: 0

27.1.220 SCB2_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask register

Address: 0x40260EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.221 SCB2_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked register

Address: 0x40260ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

27.1.222 SCB2_INTR_M

Master interrupt request register.

Address: 0x40260F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO is empty. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0

27.1.222 SCB2_INTR_M (continued)

0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Default Value: 0

27.1.223 SCB2_INTR_M_SET

Master interrupt set request register

Address: 0x40260F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.224 SCB2_INTR_M_MASK

Master interrupt mask register.

Address: 0x40260F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.225 SCB2_INTR_M_MASKED

Master interrupt masked request register

Address: 0x40260F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

27.1.226 SCB2_INTR_S

Slave interrupt request register.

Address: 0x40260F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

27.1.226 SCB2_INTR_S (continued)

7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (till the internally clocked logic takes over) (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

27.1.227 SCB2_INTR_S_SET

Slave interrupt set request register.

Address: 0x40260F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.227 SCB2_INTR_S_SET (continued)

4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.228 SCB2_INTR_S_MASK

Slave interrupt mask register.

Address: 0x40260F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.228 SCB2_INTR_S_MASK (continued)

4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.229 SCB2_INTR_S_MASKED

Slave interrupt masked request register

Address: 0x40260F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0

27.1.229 SCB2_INTR_S_MASKED (continued)

4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

27.1.230 SCB2_INTR_TX

Transmitter interrupt request register.

Address: 0x40260F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is '1'. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	BLOCKED	AHB-Lite write transfer can not get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0

27.1.230 SCB2_INTR_TX (continued)

6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when the IP is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on TX_FIFO_CTRL.DATA_8BIT: DATA_8BIT is '0': # entries != FF_DATA_NR/2. DATA_8BIT is '1': # entries != FF_DATA_NR. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL. Only used in FIFO mode. Default Value: 0

27.1.231 SCB2_INTR_TX_SET

Transmitter interrupt set request register

Address: 0x40260F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.231 SCB2_INTR_TX_SET (continued)

1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.232 SCB2_INTR_TX_MASK

Transmitter interrupt mask register.

Address: 0x40260F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.232 SCB2_INTR_TX_MASK (continued)

1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.233 SCB2_INTR_TX_MASKED

Transmitter interrupt masked request register

Address: 0x40260F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0

27.1.233 SCB2_INTR_TX_MASKED (continued)

1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

27.1.234 SCB2_INTR_RX

Receiver interrupt request register.

Address: 0x40260FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is ecpected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STATUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

27.1.234 SCB2_INTR_RX (continued)

9	PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0
8	FRAME_ERROR	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
7	BLOCKED	AHB-Lite read transfer can not get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on RX_FIFO_CTRL.DATA_8BIT: DATA_8BIT is '0': # entries == FF_DATA_NR/2. DATA_8BIT is '1': # entries == FF_DATA_NR. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FIFO_CTL. Only used in FIFO mode. Default Value: 0

27.1.235 SCB2_INTR_RX_SET

Receiver interrupt set request register.

Address: 0x40260FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

27.1.235 SCB2_INTR_RX_SET (continued)

3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.236 SCB2_INTR_RX_MASK

Receiver interrupt mask register.

Address: 0x40260FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.236 SCB2_INTR_RX_MASK (continued)

3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.237 SCB2_INTR_RX_MASKED

Receiver interrupt masked request register

Address: 0x40260FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

27.1.237 SCB2_INTR_RX_MASKED (continued)

3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

27.1.238 SCB3_CTRL

Generic control register.

Address: 0x40270000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BYTE_MODE	EZ_MODE	EC_OP_MODE	EC_AM_MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_ACCEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	IP enabled ('1') or not ('0'). The proper order in which to initialize the IP is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL to enable IP, select the specific operation mode and oversampling factor. When the IP is enabled, no control information should be changed. Changes should be made AFTER disabling the IP, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the IP is re-enabled. Note that disabling the IP will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3 **0x0: I2C:** Inter-Integrated Circuits (I2C) mode.

27.1.238 SCB3_CTRL (continued)

		0x1: SPI: Serial Peripheral Interface (SPI) mode. **0x2: UART:** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the MMIO SW accesses to EZ memory coincide/collide, this bit determines whether a SW access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is ¡®0¡¯ and the accesses collide, MMIO read operations return 0xffff:ffff and MMIO write operations are ignored. Colliding accesses are registered as interrupt causes: field BLOCKED of MMIO registers INTR_TX and INTR_RX. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when ADDR_ACCEPT is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
11	BYTE_MODE	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. Default Value: 0
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames mot seperated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0
9	EC_OP_MODE	Internally clocked mode ('0') or externally clocked mode ('1') operation. In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0

27.1.238 SCB3_CTRL (continued)

8	EC_AM_MODE	Internally clocked mode ('0') or externally clocked mode ('1') address matching (I2C) or selection (SPI). In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'. Default Value: 0
3 : 0	OVS	Serial interface bit period oversampling factor expressed in IP clock cycles. Used for SPI and UART functionality. OVS + 1 IP clock cycles constitute a single serial interface clock/bit cycle. The IP clock is provided by the programmable clock IP. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the first and second phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the first phase of the interface clock period is 1 peripheral clock cycle longer than the second phase of the interface clock period. In SPI master mode, the valid range is [3, 15]. At an IP frequency of 48 MHz, the maximum IP bit rate is 12 Mbps. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock "spi_clk_out" to SPI MISO input "spi_miso_in" round trip delay is introducing significant delays (multiple "spi_clk_out" cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. The maximum IP bit rate of 12 Mbps provides an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the IP clock wrt. the interface (IF) clock to guarantee functional correct behavior. This requirement is expressed as a ratio: IP clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 6. At a IP frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 3. At a IP frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 8. At a IP frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 4. At a IP frequency of 48 MHz, the maximum bit rate is 12 Mbps. The maximum bit rates provide an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account.

27.1.238 SCB3_CTRL (continued)

In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15].

In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value:
- 0: 16 times oversampling.
  IP clock frequency of 16*115.2 KHz for 115.2 Kbps.
  IP clock frequency of 16*57.6 KHz for 57.6 Kbps.
  IP clock frequency of 16*38.4 KHz for 38.4 Kbps.
  IP clock frequency of 16*19.2 KHz for 19.2 Kbps.
  IP clock frequency of 16*9.6 KHz for 9.6 Kbps.
  IP clock frequency of 16*2.4 KHz for 2.4 Kbps.
  IP clock frequency of 16*1.2 KHz for 1.2 Kbps.
- all other values are not used in normal mode.

In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two IP clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two IP clock cycles and greater or equal than one IP clock cycle may be detected by the receiver. Pulse widths less than one IP clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The IP clock (as provided by the programmable clock IP) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required IP clock frequency):
- 0: 16 times oversampling.
  IP clock frequency of 16*115.2 KHz for 115.2 Kbps.
  IP clock frequency of 16*57.6 KHz for 57.6 Kbps.
  IP clock frequency of 16*38.4 KHz for 38.4 Kbps.
  IP clock frequency of 16*19.2 KHz for 19.2 Kbps.
  IP clock frequency of 16*9.6 KHz for 9.6 Kbps.
  IP clock frequency of 16*2.4 KHz for 2.4 Kbps.
  IP clock frequency of 16*1.2 KHz for 1.2 Kbps.
- all other values are not used in normal mode.

Low power mode, OVS field values (with the required IP clock frequency):
- 0: 16 times oversampling.
  IP clock frequency of 16*115.2 KHz for 115.2 Kbps.
- 1: 32 times oversampling.
  IP clock frequency of 32*57.6 KHz for 57.6 Kbps.
- 2: 48 times oversampling.
  IP clock frequency of 48*38.4 KHz for 38.4 Kbps.
- 3: 96 times oversampling.
  IP clock frequency of 96*19.2 KHz for 19.2 Kbps.
- 4: 192 times oversampling.
  IP clock frequency of 192*9.6 KHz for 9.6 Kbps.
- 5: 768 times oversampling.
  IP clock frequency of 768*2.4 KHz for 2.4 Kbps.
- 6: 1536 times oversampling.
  IP clock frequency of 1536*1.2 KHz for 1.2 Kbps.
- all other values are not used in low power mode.

Default Value: 15

27.1.239 SCB3_STATUS

Generic status register.

Address: 0x40270004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

27.1.240 SCB3_SPI_CTRL

SPI control register.

Address: 0x40270020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_CONTINUOUS	LATE_MISO_SAMPLE	CPOL	CPHA	SELECT_PRECEDE	CONTINU-OUS

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SSEL_POLARITY3	SSEL_POLARITY2	SSEL_POLARITY1	SSEL_POLARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_MODE	None [30:28]			SLAVE_SELECT [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SLAVE_SELECT	Selects one of the four outgoing SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. The IP should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

27.1.240 SCB3_SPI_CTRL (continued)

		0x0: SPI_MOTOROLA: SPI Motorola submode. In master mode, when not transmitting data (SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive. **0x1: SPI_TI:** SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS:** SPI National Semiconducturs submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': the SPI master MISO line "spi_miso_in" is connected to the SPI MISO pin. '1': the SPI master MISO line "spi_miso_in" is connected to the SPI master MOSI line "spi_mosi_out". In other words, in loopback mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. SSEL_POLARITY3 applies to the outgoing SPI slave select signal 3 (master mode). Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. SSEL_POLARITY2 applies to the outgoing SPI slave select signal 2 (master mode). Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. SSEL_POLARITY1 applies to the outgoing SPI slave select signal 1 (master mode). Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Istruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0

27.1.240 SCB3_SPI_CTRL (continued)

4	LATE_MISO_SAMPLE	Changes the SCLK edge on which MISO is captured. Only used in master mode. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 0
3	CPOL	Indicates the clock polarity. Only used in SPI Motorola submode. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is ¡®0¡¯: SCLK is ¡®0¡¯ when not transmitting data. - CPOL is ¡®1¡¯: SCLK is ¡®1¡¯ when not transmitting data. Default Value: 0
2	CPHA	Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is ¡®0¡¯, CPHA is ¡®0¡¯: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is ¡®0¡¯, CPHA is ¡®1¡¯: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is ¡®1¡¯, CPHA is ¡®0¡¯: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is ¡®1¡¯, CPHA is ¡®1¡¯: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. Default Value: 0
1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0
0	CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled individual data frame transfers are not necessarily seperated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always seperated by slave deselection: independent of the availability of TX FIFO data frames, data+G65 frames are send out with slave deselection. Default Value: 0

27.1.241 SCB3_SPI_STATUS

SPI status register.

Address: 0x40270024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
1	SPI_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection (low active) is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

27.1.242 SCB3_UART_CTRL

UART control register.

Address: 0x40270040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD:** Standard UART submode. **0x1: UART_SMARTCARD:** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA:** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS is 15.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). When '0', the transmitter TX line "uart_tx_out" is connected to the TX pin and the receiver RX line "uart_rx_in" is connected to the RX pin. When '1', the transmitter TX line "uart_tx_out" is connected to the receiver RX line "uart_rx_in". A similar connections scheme is followed for "uart_rts_out" and "uart_cts_in". This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

27.1.243 SCB3_UART_TX_CTRL

UART transmitter control register.

Address: 0x40270044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

27.1.244 SCB3_UART_RX_CTRL

UART receiver control register.

Address: 0x40270048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SKIP_START	LIN_MODE	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

27.1.244 SCB3_UART_RX_CTRL (continued)

13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame seperates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	DROP_ON_FRAME_ERROR	Behaviour when an error is detected in a start or stop period. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	DROP_ON_PARITY_ERROR	Behaviour when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal "uart_rx_in". Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

27.1.244 SCB3_UART_RX_CTRL (continued)

2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle ('1') time between data frames and the data frame value. Default Value: 2

27.1.245 SCB3_UART_RX_STATUS

UART receiver status register.

Address: 0x4027004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	Amount of peripheral clock periods that constitute the transmission of a 0x55 data frame (sent least signficant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of peripheral clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

27.1.246 SCB3_UART_FLOW_CTRL

UART flow control register

Address: 0x40270050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	Enable use of CTS input signal "uart_cts_in" by the UART transmitter: '0': Disabled. The UART transmitter ignores "uart_cts_in", and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses "uart_cts_in" to qualify the transmission of data. It transmits when "uart_cts_in" is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', "uart_cts_in" is connected to "uart_rts_out" in the IP (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY). Default Value: 0
24	CTS_POLARITY	Polarity of the CTS input signal "uart_cts_in": '0': CTS is low/'0' active; "uart_cts_in" is '0' when active and "uart_cts_in" is '1' when inactive. '1': CTS is high/'1' active; "uart_cts_in" is '1' when active and "uart_cts_in" is '0' when inactive. Default Value: 0

27.1.246 SCB3_UART_FLOW_CTRL (continued)

16	RTS_POLARITY	Polarity of the RTS output signal "uart_rts_out": '0': RTS is low/'0' active; "uart_rts_out" is '0' when active and "uart_rts_out" is '1' when inactive. '1': RTS is high/'1' active; "uart_rts_out" is '1' when active and "uart_rts_out" is '0' when inactive. During IP reset (Hibernate system power mode), "uart_rts_out" is '1'. This represents an inactive state assuming a low/'0' active polarity. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal "uart_rts_out" is activated. By setting this field to "0", flow control is effectively SW disabled (may be useful for debug purposes). Default Value: 0

27.1.247 SCB3_I2C_CTRL

I2C control register.

Address: 0x40270060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_READY_DATA_NACK	S_NOT_READY_ADDR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENERAL_IGNORE	None	M_NOT_READY_DATA_NACK	M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_MODE	SLAVE_MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', the I2C SCL and SDA lines are connected to the I2C SCL and SDA pins. When '1', I2C SCL and SDA lines are routed internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0
15	S_NOT_READY_DATA_NACK	For internally clocked logic only. Only used when: - non EZ mode. Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1

27.1.247 SCB3_I2C_CTRL (continued)

14	S_NOT_READY_ADDR_NACK	For internally clocked logic (EC_AM is '0' and EC_OP is '0') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when: - EC_AM is '0', EC_OP is '0' and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the internally clocked logic is enabled (we are in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2). the internally clocked logic is not enabled (we are in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the internally clocked logic takes over). The internally clocked logic will handle the ongoing transfer as soon as it is enabled. Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	M_NOT_READY_DATA_NACK	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1
7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 peripheral clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular (no stretching) interface (IF) low time to guarantee functional correct behavior. With input signal median filtering, the IF low time should be >= 8 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 IP clock cycles and <= 16 IP clock cycles. Default Value: 8

27.1.247 SCB3_I2C_CTRL (continued)

3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 peripheral clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF high time should be >= 5 IP clock cycles and <= 16 IP clock cycles. Default Value: 8

27.1.248 SCB3_I2C_STATUS

I2C status register.

Address: 0x40270064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	R
HW Access	None		W	W	None		W	W
Name	None [7:6]		M_READ	S_READ	None [3:2]		I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0

27.1.248 SCB3_I2C_STATUS (continued)

1	I2C_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If the IP is disabled, BUS_BUSY is '0'. After enabling the IP, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

27.1.249 SCB3_I2C_M_CMD

I2C master command register.

Address: 0x40270068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. This command has a higher priority than I2C_M_CMD.M_START: in situations where both a STOP and a REPEATED START could be transmitted, M_STOP takes precedence over M_START. Default Value: 0
3	M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0

27.1.249 SCB3_I2C_M_CMD (continued)

0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

27.1.250 SCB3_I2C_S_CMD

I2C slave command register.

Address: 0x4027006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

27.1.251 SCB3_I2C_CFG

I2C configuration register.

Address: 0x40270070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_FILT_SEL	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_FILT_SEL	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative "i2c_sda_out" filter delay: "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 2. Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 1. Default Value: 2
17 : 16	SDA_OUT_FILT0_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 0. Default Value: 2

27.1.251 SCB3_I2C_CFG (continued)

12	SCL_IN_FILT_SEL	Selection of "i2c_scl_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim bits for "i2c_scl_in" 50 ns filter. Default Value: 0
4	SDA_IN_FILT_SEL	Selection of "i2c_sda_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim bits for "i2c_sda_in" 50 ns filter. Default Value: 3

27.1.252 SCB3_TX_CTRL

Transmitter control register.

Address: 0x40270200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. Default Value: 7

27.1.253 SCB3_TX_FIFO_CTRL

Transmitter FIFO control register.

Address: 0x40270204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

27.1.254 SCB3_TX_FIFO_STATUS

Transmitter FIFO status register.

Address: 0x40270208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:5]				USED [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is tranmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

27.1.255 SCB3_TX_FIFO_WR

Transmitter FIFO write register.

Address: 0x40270240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when TX_FIFO_CTRL.DATA_8BIT is '1', only DATA[7:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

27.1.256 SCB3_RX_CTRL

Receiver control register.

Address: 0x40270300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptability to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

27.1.257 SCB3_RX_FIFO_CTRL

Receiver FIFO control register.

Address: 0x40270304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event is generated. Default Value: 0

27.1.258 SCB3_RX_FIFO_STATUS

Receiver FIFO status register.

Address: 0x40270308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:5]				USED [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

27.1.259 SCB3_RX_MATCH

Slave address and mask register.

Address: 0x40270310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the ADDR field bits in the ADDR field take part in the matching of the slave address: MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

27.1.260 SCB3_RX_FIFO_RD

Receiver FIFO read register.

Address: 0x40270340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when RX_FIFO_CTRL.DATA_8BIT is '1', only DATA[7:0] are used. This register has a side effect when read by software: a data frame is removed from the FIFO. This may be undesirable during debug; i.e. a read during debug should NOT have a side effect. To this end, the IP uses the AHB-Lite "hmaster[0]" input signal. When this signal is '1' in the address cycle of a bus transfer, a read transfer will not have a side effect. As a result, a read from this register will not remove a data frame from the FIFO. As a result, a read from this register behaves as a read from the SCB_RX_FIFO_RD_SILENT register. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

27.1.261 SCB3_RX_FIFO_RD_SILENT

Receiver FIFO read register.

Address: 0x40270344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when RX_FIFO_CTRL.DATA_8BIT is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

27.1.262 SCB3_EZ_DATA0

Memory buffer registers.

Address: 0x40270400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.263 SCB3_EZ_DATA1

Memory buffer registers.

Address: 0x40270404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.264 SCB3_EZ_DATA2

Memory buffer registers.

Address: 0x40270408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.265 SCB3_EZ_DATA3

Memory buffer registers.

Address: 0x4027040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.266 SCB3_EZ_DATA4

Memory buffer registers.

Address: 0x40270410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.267 SCB3_EZ_DATA5

Memory buffer registers.

Address: 0x40270414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.268 SCB3_EZ_DATA6

Memory buffer registers.

Address: 0x40270418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.269 SCB3_EZ_DATA7

Memory buffer registers.

Address: 0x4027041C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.270 SCB3_EZ_DATA8

Memory buffer registers.

Address: 0x40270420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.271 SCB3_EZ_DATA9

Memory buffer registers.

Address: 0x40270424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.272 SCB3_EZ_DATA10

Memory buffer registers.

Address: 0x40270428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.273 SCB3_EZ_DATA11

Memory buffer registers.

Address: 0x4027042C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.274 SCB3_EZ_DATA12

Memory buffer registers.

Address: 0x40270430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.275 SCB3_EZ_DATA13

Memory buffer registers.

Address: 0x40270434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.276 SCB3_EZ_DATA14

Memory buffer registers.

Address: 0x40270438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.277 SCB3_EZ_DATA15

Memory buffer registers.

Address: 0x4027043C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.278 SCB3_EZ_DATA16

Memory buffer registers.

Address: 0x40270440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.279 SCB3_EZ_DATA17

Memory buffer registers.

Address: 0x40270444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.280 SCB3_EZ_DATA18

Memory buffer registers.

Address: 0x40270448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.281 SCB3_EZ_DATA19

Memory buffer registers.

Address: 0x4027044C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.282 SCB3_EZ_DATA20

Memory buffer registers.

Address: 0x40270450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.283 SCB3_EZ_DATA21

Memory buffer registers.

Address: 0x40270454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.284 SCB3_EZ_DATA22

Memory buffer registers.

Address: 0x40270458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.285 SCB3_EZ_DATA23

Memory buffer registers.

Address: 0x4027045C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.286 SCB3_EZ_DATA24

Memory buffer registers.

Address: 0x40270460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.287 SCB3_EZ_DATA25

Memory buffer registers.

Address: 0x40270464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.288 SCB3_EZ_DATA26

Memory buffer registers.

Address: 0x40270468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.289 SCB3_EZ_DATA27

Memory buffer registers.

Address: 0x4027046C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.290 SCB3_EZ_DATA28

Memory buffer registers.

Address: 0x40270470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.291 SCB3_EZ_DATA29

Memory buffer registers.

Address: 0x40270474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.292 SCB3_EZ_DATA30

Memory buffer registers.

Address: 0x40270478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.293 SCB3_EZ_DATA31

Memory buffer registers.

Address: 0x4027047C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

27.1.294 SCB3_INTR_CAUSE

Active clocked interrupt signal register

Address: 0x40270E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

27.1.295 SCB3_INTR_I2C_EC

Externally clocked I2C interrupt request register

Address: 0x40270E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0

27.1.295 SCB3_INTR_I2C_EC (continued)

0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when EC_AM is '1'. Default Value: 0

27.1.296 SCB3_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask register

Address: 0x40270E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.297 SCB3_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked register

Address: 0x40270E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

27.1.298 SCB3_INTR_SPI_EC

Externally clocked SPI interrupt request register

Address: 0x40270EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI de-selection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI de-selection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when EC_OP is '1'. Default Value: 0

27.1.298 SCB3_INTR_SPI_EC (continued)

0	WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when EC_AM is '1'. Default Value: 0

27.1.299 SCB3_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask register

Address: 0x40270EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.300 SCB3_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked register

Address: 0x40270ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

27.1.301 SCB3_INTR_M

Master interrupt request register.

Address: 0x40270F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO is empty. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0

27.1.301 SCB3_INTR_M (continued)

0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Default Value: 0

27.1.302 SCB3_INTR_M_SET

Master interrupt set request register

Address: 0x40270F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.303 SCB3_INTR_M_MASK

Master interrupt mask register.

Address: 0x40270F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.304 SCB3_INTR_M_MASKED

Master interrupt masked request register

Address: 0x40270F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

27.1.305 SCB3_INTR_S

Slave interrupt request register.

Address: 0x40270F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

27.1.305 SCB3_INTR_S (continued)

7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (till the internally clocked logic takes over) (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

27.1.306 SCB3_INTR_S_SET

Slave interrupt set request register.

Address: 0x40270F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.306 SCB3_INTR_S_SET (continued)

4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.307 SCB3_INTR_S_MASK

Slave interrupt mask register.

Address: 0x40270F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.307 SCB3_INTR_S_MASK (continued)

4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.308 SCB3_INTR_S_MASKED

Slave interrupt masked request register

Address: 0x40270F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0

27.1.308 SCB3_INTR_S_MASKED (continued)

4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

27.1.309 SCB3_INTR_TX

Transmitter interrupt request register.

Address: 0x40270F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is '1'. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	BLOCKED	AHB-Lite write transfer can not get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0

27.1.309 SCB3_INTR_TX (continued)

6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when the IP is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on TX_FIFO_CTRL.DATA_8BIT: DATA_8BIT is '0': # entries != FF_DATA_NR/2. DATA_8BIT is '1': # entries != FF_DATA_NR. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL. Only used in FIFO mode. Default Value: 0

27.1.310 SCB3_INTR_TX_SET

Transmitter interrupt set request register

Address: 0x40270F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.310 SCB3_INTR_TX_SET (continued)

1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.311 SCB3_INTR_TX_MASK

Transmitter interrupt mask register.

Address: 0x40270F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.311 SCB3_INTR_TX_MASK (continued)

1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.312 SCB3_INTR_TX_MASKED

Transmitter interrupt masked request register

Address: 0x40270F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0

27.1.312 SCB3_INTR_TX_MASKED (continued)

1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

27.1.313 SCB3_INTR_RX

Receiver interrupt request register.

Address: 0x40270FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is ecpected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STATUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

27.1.313 SCB3_INTR_RX (continued)

9	PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0
8	FRAME_ERROR	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
7	BLOCKED	AHB-Lite read transfer can not get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on RX_FIFO_CTRL.DATA_8BIT: DATA_8BIT is '0': # entries == FF_DATA_NR/2. DATA_8BIT is '1': # entries == FF_DATA_NR. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FIFO_CTL. Only used in FIFO mode. Default Value: 0

27.1.314 SCB3_INTR_RX_SET

Receiver interrupt set request register.

Address: 0x40270FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

27.1.314 SCB3_INTR_RX_SET (continued)

3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.315 SCB3_INTR_RX_MASK

Receiver interrupt mask register.

Address: 0x40270FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.315 SCB3_INTR_RX_MASK (continued)

3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.316 SCB3_INTR_RX_MASKED

Receiver interrupt masked request register

Address: 0x40270FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

27.1.316 SCB3_INTR_RX_MASKED (continued)

3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

28 Supervisory Flash (SFLASH) Registers

This section discusses the SFLASH registers. It lists all the registers in mapping tables, in address order.

28.1 Register Details

Register Name	Address
SFLASH_PROT_ROW0	0x0FFFF000
SFLASH_PROT_ROW1	0x0FFFF001
SFLASH_PROT_ROW2	0x0FFFF002
SFLASH_PROT_ROW3	0x0FFFF003
SFLASH_PROT_ROW4	0x0FFFF004
SFLASH_PROT_ROW5	0x0FFFF005
SFLASH_PROT_ROW6	0x0FFFF006
SFLASH_PROT_ROW7	0x0FFFF007
SFLASH_PROT_ROW8	0x0FFFF008
SFLASH_PROT_ROW9	0x0FFFF009
SFLASH_PROT_ROW10	0x0FFFF00A
SFLASH_PROT_ROW11	0x0FFFF00B
SFLASH_PROT_ROW12	0x0FFFF00C
SFLASH_PROT_ROW13	0x0FFFF00D
SFLASH_PROT_ROW14	0x0FFFF00E
SFLASH_PROT_ROW15	0x0FFFF00F
SFLASH_PROT_ROW16	0x0FFFF010
SFLASH_PROT_ROW17	0x0FFFF011
SFLASH_PROT_ROW18	0x0FFFF012
SFLASH_PROT_ROW19	0x0FFFF013
SFLASH_PROT_ROW20	0x0FFFF014
SFLASH_PROT_ROW21	0x0FFFF015
SFLASH_PROT_ROW22	0x0FFFF016
SFLASH_PROT_ROW23	0x0FFFF017
SFLASH_PROT_ROW24	0x0FFFF018
SFLASH_PROT_ROW25	0x0FFFF019
SFLASH_PROT_ROW26	0x0FFFF01A

Register Name	Address
SFLASH_PROT_ROW27	0x0FFFF01B
SFLASH_PROT_ROW28	0x0FFFF01C
SFLASH_PROT_ROW29	0x0FFFF01D
SFLASH_PROT_ROW30	0x0FFFF01E
SFLASH_PROT_ROW31	0x0FFFF01F
SFLASH_PROT_ROW32	0x0FFFF020
SFLASH_PROT_ROW33	0x0FFFF021
SFLASH_PROT_ROW34	0x0FFFF022
SFLASH_PROT_ROW35	0x0FFFF023
SFLASH_PROT_ROW36	0x0FFFF024
SFLASH_PROT_ROW37	0x0FFFF025
SFLASH_PROT_ROW38	0x0FFFF026
SFLASH_PROT_ROW39	0x0FFFF027
SFLASH_PROT_ROW40	0x0FFFF028
SFLASH_PROT_ROW41	0x0FFFF029
SFLASH_PROT_ROW42	0x0FFFF02A
SFLASH_PROT_ROW43	0x0FFFF02B
SFLASH_PROT_ROW44	0x0FFFF02C
SFLASH_PROT_ROW45	0x0FFFF02D
SFLASH_PROT_ROW46	0x0FFFF02E
SFLASH_PROT_ROW47	0x0FFFF02F
SFLASH_PROT_ROW48	0x0FFFF030
SFLASH_PROT_ROW49	0x0FFFF031
SFLASH_PROT_ROW50	0x0FFFF032
SFLASH_PROT_ROW51	0x0FFFF033
SFLASH_PROT_ROW52	0x0FFFF034
SFLASH_PROT_ROW53	0x0FFFF035
SFLASH_PROT_ROW54	0x0FFFF036
SFLASH_PROT_ROW55	0x0FFFF037
SFLASH_PROT_ROW56	0x0FFFF038
SFLASH_PROT_ROW57	0x0FFFF039
SFLASH_PROT_ROW58	0x0FFFF03A
SFLASH_PROT_ROW59	0x0FFFF03B
SFLASH_PROT_ROW60	0x0FFFF03C
SFLASH_PROT_ROW61	0x0FFFF03D
SFLASH_PROT_ROW62	0x0FFFF03E
SFLASH_PROT_ROW63	0x0FFFF03F
SFLASH_PROT_PROTECTION	0x0FFFF07F
SFLASH_AV_PAIRS_8B0	0x0FFFF080
SFLASH_AV_PAIRS_8B1	0x0FFFF081
SFLASH_AV_PAIRS_8B2	0x0FFFF082
SFLASH_AV_PAIRS_8B3	0x0FFFF083

Register Name	Address
SFLASH_AV_PAIRS_8B4	0x0FFFF084
SFLASH_AV_PAIRS_8B5	0x0FFFF085
SFLASH_AV_PAIRS_8B6	0x0FFFF086
SFLASH_AV_PAIRS_8B7	0x0FFFF087
SFLASH_AV_PAIRS_8B8	0x0FFFF088
SFLASH_AV_PAIRS_8B9	0x0FFFF089
SFLASH_AV_PAIRS_8B10	0x0FFFF08A
SFLASH_AV_PAIRS_8B11	0x0FFFF08B
SFLASH_AV_PAIRS_8B12	0x0FFFF08C
SFLASH_AV_PAIRS_8B13	0x0FFFF08D
SFLASH_AV_PAIRS_8B14	0x0FFFF08E
SFLASH_AV_PAIRS_8B15	0x0FFFF08F
SFLASH_AV_PAIRS_8B16	0x0FFFF090
SFLASH_AV_PAIRS_8B17	0x0FFFF091
SFLASH_AV_PAIRS_8B18	0x0FFFF092
SFLASH_AV_PAIRS_8B19	0x0FFFF093
SFLASH_AV_PAIRS_8B20	0x0FFFF094
SFLASH_AV_PAIRS_8B21	0x0FFFF095
SFLASH_AV_PAIRS_8B22	0x0FFFF096
SFLASH_AV_PAIRS_8B23	0x0FFFF097
SFLASH_AV_PAIRS_8B24	0x0FFFF098
SFLASH_AV_PAIRS_8B25	0x0FFFF099
SFLASH_AV_PAIRS_8B26	0x0FFFF09A
SFLASH_AV_PAIRS_8B27	0x0FFFF09B
SFLASH_AV_PAIRS_8B28	0x0FFFF09C
SFLASH_AV_PAIRS_8B29	0x0FFFF09D
SFLASH_AV_PAIRS_8B30	0x0FFFF09E
SFLASH_AV_PAIRS_8B31	0x0FFFF09F
SFLASH_AV_PAIRS_8B32	0x0FFFF0A0
SFLASH_AV_PAIRS_8B33	0x0FFFF0A1
SFLASH_AV_PAIRS_8B34	0x0FFFF0A2
SFLASH_AV_PAIRS_8B35	0x0FFFF0A3
SFLASH_AV_PAIRS_8B36	0x0FFFF0A4
SFLASH_AV_PAIRS_8B37	0x0FFFF0A5
SFLASH_AV_PAIRS_8B38	0x0FFFF0A6
SFLASH_AV_PAIRS_8B39	0x0FFFF0A7
SFLASH_AV_PAIRS_8B40	0x0FFFF0A8
SFLASH_AV_PAIRS_8B41	0x0FFFF0A9
SFLASH_AV_PAIRS_8B42	0x0FFFF0AA
SFLASH_AV_PAIRS_8B43	0x0FFFF0AB
SFLASH_AV_PAIRS_8B44	0x0FFFF0AC
SFLASH_AV_PAIRS_8B45	0x0FFFF0AD

Register Name	Address
SFLASH_AV_PAIRS_8B46	0x0FFFF0AE
SFLASH_AV_PAIRS_8B47	0x0FFFF0AF
SFLASH_AV_PAIRS_8B48	0x0FFFF0B0
SFLASH_AV_PAIRS_8B49	0x0FFFF0B1
SFLASH_AV_PAIRS_8B50	0x0FFFF0B2
SFLASH_AV_PAIRS_8B51	0x0FFFF0B3
SFLASH_AV_PAIRS_8B52	0x0FFFF0B4
SFLASH_AV_PAIRS_8B53	0x0FFFF0B5
SFLASH_AV_PAIRS_8B54	0x0FFFF0B6
SFLASH_AV_PAIRS_8B55	0x0FFFF0B7
SFLASH_AV_PAIRS_8B56	0x0FFFF0B8
SFLASH_AV_PAIRS_8B57	0x0FFFF0B9
SFLASH_AV_PAIRS_8B58	0x0FFFF0BA
SFLASH_AV_PAIRS_8B59	0x0FFFF0BB
SFLASH_AV_PAIRS_8B60	0x0FFFF0BC
SFLASH_AV_PAIRS_8B61	0x0FFFF0BD
SFLASH_AV_PAIRS_8B62	0x0FFFF0BE
SFLASH_AV_PAIRS_8B63	0x0FFFF0BF
SFLASH_AV_PAIRS_8B64	0x0FFFF0C0
SFLASH_AV_PAIRS_8B65	0x0FFFF0C1
SFLASH_AV_PAIRS_8B66	0x0FFFF0C2
SFLASH_AV_PAIRS_8B67	0x0FFFF0C3
SFLASH_AV_PAIRS_8B68	0x0FFFF0C4
SFLASH_AV_PAIRS_8B69	0x0FFFF0C5
SFLASH_AV_PAIRS_8B70	0x0FFFF0C6
SFLASH_AV_PAIRS_8B71	0x0FFFF0C7
SFLASH_AV_PAIRS_8B72	0x0FFFF0C8
SFLASH_AV_PAIRS_8B73	0x0FFFF0C9
SFLASH_AV_PAIRS_8B74	0x0FFFF0CA
SFLASH_AV_PAIRS_8B75	0x0FFFF0CB
SFLASH_AV_PAIRS_8B76	0x0FFFF0CC
SFLASH_AV_PAIRS_8B77	0x0FFFF0CD
SFLASH_AV_PAIRS_8B78	0x0FFFF0CE
SFLASH_AV_PAIRS_8B79	0x0FFFF0CF
SFLASH_AV_PAIRS_8B80	0x0FFFF0D0
SFLASH_AV_PAIRS_8B81	0x0FFFF0D1
SFLASH_AV_PAIRS_8B82	0x0FFFF0D2
SFLASH_AV_PAIRS_8B83	0x0FFFF0D3
SFLASH_AV_PAIRS_8B84	0x0FFFF0D4
SFLASH_AV_PAIRS_8B85	0x0FFFF0D5
SFLASH_AV_PAIRS_8B86	0x0FFFF0D6
SFLASH_AV_PAIRS_8B87	0x0FFFF0D7

Register Name	Address
SFLASH_AV_PAIRS_8B88	0x0FFFF0D8
SFLASH_AV_PAIRS_8B89	0x0FFFF0D9
SFLASH_AV_PAIRS_8B90	0x0FFFF0DA
SFLASH_AV_PAIRS_8B91	0x0FFFF0DB
SFLASH_AV_PAIRS_8B92	0x0FFFF0DC
SFLASH_AV_PAIRS_8B93	0x0FFFF0DD
SFLASH_AV_PAIRS_8B94	0x0FFFF0DE
SFLASH_AV_PAIRS_8B95	0x0FFFF0DF
SFLASH_AV_PAIRS_8B96	0x0FFFF0E0
SFLASH_AV_PAIRS_8B97	0x0FFFF0E1
SFLASH_AV_PAIRS_8B98	0x0FFFF0E2
SFLASH_AV_PAIRS_8B99	0x0FFFF0E3
SFLASH_AV_PAIRS_8B100	0x0FFFF0E4
SFLASH_AV_PAIRS_8B101	0x0FFFF0E5
SFLASH_AV_PAIRS_8B102	0x0FFFF0E6
SFLASH_AV_PAIRS_8B103	0x0FFFF0E7
SFLASH_AV_PAIRS_8B104	0x0FFFF0E8
SFLASH_AV_PAIRS_8B105	0x0FFFF0E9
SFLASH_AV_PAIRS_8B106	0x0FFFF0EA
SFLASH_AV_PAIRS_8B107	0x0FFFF0EB
SFLASH_AV_PAIRS_8B108	0x0FFFF0EC
SFLASH_AV_PAIRS_8B109	0x0FFFF0ED
SFLASH_AV_PAIRS_8B110	0x0FFFF0EE
SFLASH_AV_PAIRS_8B111	0x0FFFF0EF
SFLASH_AV_PAIRS_8B112	0x0FFFF0F0
SFLASH_AV_PAIRS_8B113	0x0FFFF0F1
SFLASH_AV_PAIRS_8B114	0x0FFFF0F2
SFLASH_AV_PAIRS_8B115	0x0FFFF0F3
SFLASH_AV_PAIRS_8B116	0x0FFFF0F4
SFLASH_AV_PAIRS_8B117	0x0FFFF0F5
SFLASH_AV_PAIRS_8B118	0x0FFFF0F6
SFLASH_AV_PAIRS_8B119	0x0FFFF0F7
SFLASH_AV_PAIRS_8B120	0x0FFFF0F8
SFLASH_AV_PAIRS_8B121	0x0FFFF0F9
SFLASH_AV_PAIRS_8B122	0x0FFFF0FA
SFLASH_AV_PAIRS_8B123	0x0FFFF0FB
SFLASH_AV_PAIRS_8B124	0x0FFFF0FC
SFLASH_AV_PAIRS_8B125	0x0FFFF0FD
SFLASH_AV_PAIRS_8B126	0x0FFFF0FE
SFLASH_AV_PAIRS_8B127	0x0FFFF0FF
SFLASH_AV_PAIRS_32B0	0x0FFFF100
SFLASH_AV_PAIRS_32B1	0x0FFFF104

Register Name	Address
SFLASH_AV_PAIRS_32B2	0x0FFFF108
SFLASH_AV_PAIRS_32B3	0x0FFFF10C
SFLASH_AV_PAIRS_32B4	0x0FFFF110
SFLASH_AV_PAIRS_32B5	0x0FFFF114
SFLASH_AV_PAIRS_32B6	0x0FFFF118
SFLASH_AV_PAIRS_32B7	0x0FFFF11C
SFLASH_AV_PAIRS_32B8	0x0FFFF120
SFLASH_AV_PAIRS_32B9	0x0FFFF124
SFLASH_AV_PAIRS_32B10	0x0FFFF128
SFLASH_AV_PAIRS_32B11	0x0FFFF12C
SFLASH_AV_PAIRS_32B12	0x0FFFF130
SFLASH_AV_PAIRS_32B13	0x0FFFF134
SFLASH_AV_PAIRS_32B14	0x0FFFF138
SFLASH_AV_PAIRS_32B15	0x0FFFF13C
SFLASH_SILICON_ID	0x0FFFF144
SFLASH_CPUSS_PRIV_RAM	0x0FFFF148
SFLASH_CPUSS_PRIV_ROM_BROM	0x0FFFF14A
SFLASH_CPUSS_PRIV_FLASH	0x0FFFF14C
SFLASH_CPUSS_PRIV_ROM_SROM	0x0FFFF14E
SFLASH_HIB_KEY_DELAY	0x0FFFF150
SFLASH_DPSLP_KEY_DELAY	0x0FFFF152
SFLASH_SWD_CONFIG	0x0FFFF154
SFLASH_INITIAL_SPCIF_TRIM_M1_DAC0	0x0FFFF155
SFLASH_SWD_LISTEN	0x0FFFF158
SFLASH_FLASH_START	0x0FFFF15C
SFLASH_CSD_TRIM1_HVIDAC	0x0FFFF160
SFLASH_CSD_TRIM2_HVIDAC	0x0FFFF161
SFLASH_CSD_TRIM1_CSD	0x0FFFF162
SFLASH_CSD_TRIM2_CSD	0x0FFFF163
SFLASH_SAR_TEMP_MULTIPLIER	0x0FFFF164
SFLASH_SAR_TEMP_OFFSET	0x0FFFF166
SFLASH_SKIP_CHECKSUM	0x0FFFF169
SFLASH_PROT_VIRGINKEY0	0x0FFFF170
SFLASH_PROT_VIRGINKEY1	0x0FFFF171
SFLASH_PROT_VIRGINKEY2	0x0FFFF172
SFLASH_PROT_VIRGINKEY3	0x0FFFF173
SFLASH_PROT_VIRGINKEY4	0x0FFFF174
SFLASH_PROT_VIRGINKEY5	0x0FFFF175
SFLASH_PROT_VIRGINKEY6	0x0FFFF176
SFLASH_PROT_VIRGINKEY7	0x0FFFF177
SFLASH_DIE_LOT0	0x0FFFF178
SFLASH_DIE_LOT1	0x0FFFF179

Register Name	Address
SFLASH_DIE_LOT2	0x0FFFF17A
SFLASH_DIE_WAFER	0x0FFFF17B
SFLASH_DIE_X	0x0FFFF17C
SFLASH_DIE_Y	0x0FFFF17D
SFLASH_DIE_SORT	0x0FFFF17E
SFLASH_DIE_MINOR	0x0FFFF17F
SFLASH_PE_TE_DATA0	0x0FFFF180
SFLASH_PE_TE_DATA1	0x0FFFF181
SFLASH_PE_TE_DATA2	0x0FFFF182
SFLASH_PE_TE_DATA3	0x0FFFF183
SFLASH_PE_TE_DATA4	0x0FFFF184
SFLASH_PE_TE_DATA5	0x0FFFF185
SFLASH_PE_TE_DATA6	0x0FFFF186
SFLASH_PE_TE_DATA7	0x0FFFF187
SFLASH_PE_TE_DATA8	0x0FFFF188
SFLASH_PE_TE_DATA9	0x0FFFF189
SFLASH_PE_TE_DATA10	0x0FFFF18A
SFLASH_PE_TE_DATA11	0x0FFFF18B
SFLASH_PE_TE_DATA12	0x0FFFF18C
SFLASH_PE_TE_DATA13	0x0FFFF18D
SFLASH_PE_TE_DATA14	0x0FFFF18E
SFLASH_PE_TE_DATA15	0x0FFFF18F
SFLASH_PE_TE_DATA16	0x0FFFF190
SFLASH_PE_TE_DATA17	0x0FFFF191
SFLASH_PE_TE_DATA18	0x0FFFF192
SFLASH_PE_TE_DATA19	0x0FFFF193
SFLASH_PE_TE_DATA20	0x0FFFF194
SFLASH_PE_TE_DATA21	0x0FFFF195
SFLASH_PE_TE_DATA22	0x0FFFF196
SFLASH_PE_TE_DATA23	0x0FFFF197
SFLASH_PE_TE_DATA24	0x0FFFF198
SFLASH_PE_TE_DATA25	0x0FFFF199
SFLASH_PE_TE_DATA26	0x0FFFF19A
SFLASH_PE_TE_DATA27	0x0FFFF19B
SFLASH_PE_TE_DATA28	0x0FFFF19C
SFLASH_PE_TE_DATA29	0x0FFFF19D
SFLASH_PE_TE_DATA30	0x0FFFF19E
SFLASH_PE_TE_DATA31	0x0FFFF19F
SFLASH_PP	0x0FFFF1A0
SFLASH_E	0x0FFFF1A4
SFLASH_P	0x0FFFF1A8
SFLASH_EA_E	0x0FFFF1AC

Register Name	Address
SFLASH_EA_P	0x0FFFF1B0
SFLASH_ES_E	0x0FFFF1B4
SFLASH_ES_P_EO	0x0FFFF1B8
SFLASH_E_VCTAT	0x0FFFF1BC
SFLASH_P_VCTAT	0x0FFFF1BD
SFLASH_IMO_MAXF0	0x0FFFF1C0
SFLASH_IMO_ABS0	0x0FFFF1C1
SFLASH_IMO_TMPCO0	0x0FFFF1C2
SFLASH_IMO_MAXF1	0x0FFFF1C3
SFLASH_IMO_ABS1	0x0FFFF1C4
SFLASH_IMO_TMPCO1	0x0FFFF1C5
SFLASH_IMO_MAXF2	0x0FFFF1C6
SFLASH_IMO_ABS2	0x0FFFF1C7
SFLASH_IMO_TMPCO2	0x0FFFF1C8
SFLASH_IMO_MAXF3	0x0FFFF1C9
SFLASH_IMO_ABS3	0x0FFFF1CA
SFLASH_IMO_TMPCO3	0x0FFFF1CB
SFLASH_IMO_ABS4	0x0FFFF1CC
SFLASH_IMO_TMPCO4	0x0FFFF1CD
SFLASH_IMO_TRIM0	0x0FFFF1D0
SFLASH_IMO_TRIM1	0x0FFFF1D1
SFLASH_IMO_TRIM2	0x0FFFF1D2
SFLASH_IMO_TRIM3	0x0FFFF1D3
SFLASH_IMO_TRIM4	0x0FFFF1D4
SFLASH_IMO_TRIM5	0x0FFFF1D5
SFLASH_IMO_TRIM6	0x0FFFF1D6
SFLASH_IMO_TRIM7	0x0FFFF1D7
SFLASH_IMO_TRIM8	0x0FFFF1D8
SFLASH_IMO_TRIM9	0x0FFFF1D9
SFLASH_IMO_TRIM10	0x0FFFF1DA
SFLASH_IMO_TRIM11	0x0FFFF1DB
SFLASH_IMO_TRIM12	0x0FFFF1DC
SFLASH_IMO_TRIM13	0x0FFFF1DD
SFLASH_IMO_TRIM14	0x0FFFF1DE
SFLASH_IMO_TRIM15	0x0FFFF1DF
SFLASH_IMO_TRIM16	0x0FFFF1E0
SFLASH_IMO_TRIM17	0x0FFFF1E1
SFLASH_IMO_TRIM18	0x0FFFF1E2
SFLASH_IMO_TRIM19	0x0FFFF1E3
SFLASH_IMO_TRIM20	0x0FFFF1E4
SFLASH_IMO_TRIM21	0x0FFFF1E5
SFLASH_IMO_TRIM22	0x0FFFF1E6

Register Name	Address
SFLASH_IMO_TRIM23	0x0FFFF1E7
SFLASH_IMO_TRIM24	0x0FFFF1E8
SFLASH_IMO_TRIM25	0x0FFFF1E9
SFLASH_IMO_TRIM26	0x0FFFF1EA
SFLASH_IMO_TRIM27	0x0FFFF1EB
SFLASH_IMO_TRIM28	0x0FFFF1EC
SFLASH_IMO_TRIM29	0x0FFFF1ED
SFLASH_IMO_TRIM30	0x0FFFF1EE
SFLASH_IMO_TRIM31	0x0FFFF1EF
SFLASH_IMO_TRIM32	0x0FFFF1F0
SFLASH_IMO_TRIM33	0x0FFFF1F1
SFLASH_IMO_TRIM34	0x0FFFF1F2
SFLASH_IMO_TRIM35	0x0FFFF1F3
SFLASH_IMO_TRIM36	0x0FFFF1F4
SFLASH_IMO_TRIM37	0x0FFFF1F5
SFLASH_IMO_TRIM38	0x0FFFF1F6
SFLASH_IMO_TRIM39	0x0FFFF1F7
SFLASH_IMO_TRIM40	0x0FFFF1F8
SFLASH_IMO_TRIM41	0x0FFFF1F9
SFLASH_IMO_TRIM42	0x0FFFF1FA
SFLASH_IMO_TRIM43	0x0FFFF1FB
SFLASH_IMO_TRIM44	0x0FFFF1FC
SFLASH_IMO_TRIM45	0x0FFFF1FD
SFLASH_CHECKSUM	0x0FFFF1FE
SFLASH_ALT_PROT_ROW0	0x0FFFF400
SFLASH_ALT_PROT_ROW1	0x0FFFF401
SFLASH_ALT_PROT_ROW2	0x0FFFF402
SFLASH_ALT_PROT_ROW3	0x0FFFF403
SFLASH_ALT_PROT_ROW4	0x0FFFF404
SFLASH_ALT_PROT_ROW5	0x0FFFF405
SFLASH_ALT_PROT_ROW6	0x0FFFF406
SFLASH_ALT_PROT_ROW7	0x0FFFF407
SFLASH_ALT_PROT_ROW8	0x0FFFF408
SFLASH_ALT_PROT_ROW9	0x0FFFF409
SFLASH_ALT_PROT_ROW10	0x0FFFF40A
SFLASH_ALT_PROT_ROW11	0x0FFFF40B
SFLASH_ALT_PROT_ROW12	0x0FFFF40C
SFLASH_ALT_PROT_ROW13	0x0FFFF40D
SFLASH_ALT_PROT_ROW14	0x0FFFF40E
SFLASH_ALT_PROT_ROW15	0x0FFFF40F
SFLASH_ALT_PROT_ROW16	0x0FFFF410
SFLASH_ALT_PROT_ROW17	0x0FFFF411

Register Name	Address
SFLASH_ALT_PROT_ROW18	0x0FFFF412
SFLASH_ALT_PROT_ROW19	0x0FFFF413
SFLASH_ALT_PROT_ROW20	0x0FFFF414
SFLASH_ALT_PROT_ROW21	0x0FFFF415
SFLASH_ALT_PROT_ROW22	0x0FFFF416
SFLASH_ALT_PROT_ROW23	0x0FFFF417
SFLASH_ALT_PROT_ROW24	0x0FFFF418
SFLASH_ALT_PROT_ROW25	0x0FFFF419
SFLASH_ALT_PROT_ROW26	0x0FFFF41A
SFLASH_ALT_PROT_ROW27	0x0FFFF41B
SFLASH_ALT_PROT_ROW28	0x0FFFF41C
SFLASH_ALT_PROT_ROW29	0x0FFFF41D
SFLASH_ALT_PROT_ROW30	0x0FFFF41E
SFLASH_ALT_PROT_ROW31	0x0FFFF41F
SFLASH_ALT_PROT_ROW32	0x0FFFF420
SFLASH_ALT_PROT_ROW33	0x0FFFF421
SFLASH_ALT_PROT_ROW34	0x0FFFF422
SFLASH_ALT_PROT_ROW35	0x0FFFF423
SFLASH_ALT_PROT_ROW36	0x0FFFF424
SFLASH_ALT_PROT_ROW37	0x0FFFF425
SFLASH_ALT_PROT_ROW38	0x0FFFF426
SFLASH_ALT_PROT_ROW39	0x0FFFF427
SFLASH_ALT_PROT_ROW40	0x0FFFF428
SFLASH_ALT_PROT_ROW41	0x0FFFF429
SFLASH_ALT_PROT_ROW42	0x0FFFF42A
SFLASH_ALT_PROT_ROW43	0x0FFFF42B
SFLASH_ALT_PROT_ROW44	0x0FFFF42C
SFLASH_ALT_PROT_ROW45	0x0FFFF42D
SFLASH_ALT_PROT_ROW46	0x0FFFF42E
SFLASH_ALT_PROT_ROW47	0x0FFFF42F
SFLASH_ALT_PROT_ROW48	0x0FFFF430
SFLASH_ALT_PROT_ROW49	0x0FFFF431
SFLASH_ALT_PROT_ROW50	0x0FFFF432
SFLASH_ALT_PROT_ROW51	0x0FFFF433
SFLASH_ALT_PROT_ROW52	0x0FFFF434
SFLASH_ALT_PROT_ROW53	0x0FFFF435
SFLASH_ALT_PROT_ROW54	0x0FFFF436
SFLASH_ALT_PROT_ROW55	0x0FFFF437
SFLASH_ALT_PROT_ROW56	0x0FFFF438
SFLASH_ALT_PROT_ROW57	0x0FFFF439
SFLASH_ALT_PROT_ROW58	0x0FFFF43A
SFLASH_ALT_PROT_ROW59	0x0FFFF43B

Register Name	Address
SFLASH_ALT_PROT_ROW60	0x0FFFF43C
SFLASH_ALT_PROT_ROW61	0x0FFFF43D
SFLASH_ALT_PROT_ROW62	0x0FFFF43E
SFLASH_ALT_PROT_ROW63	0x0FFFF43F
SFLASH_ALT_PROT_ROW64	0x0FFFF440
SFLASH_ALT_PROT_ROW65	0x0FFFF441
SFLASH_ALT_PROT_ROW66	0x0FFFF442
SFLASH_ALT_PROT_ROW67	0x0FFFF443
SFLASH_ALT_PROT_ROW68	0x0FFFF444
SFLASH_ALT_PROT_ROW69	0x0FFFF445
SFLASH_ALT_PROT_ROW70	0x0FFFF446
SFLASH_ALT_PROT_ROW71	0x0FFFF447
SFLASH_ALT_PROT_ROW72	0x0FFFF448
SFLASH_ALT_PROT_ROW73	0x0FFFF449
SFLASH_ALT_PROT_ROW74	0x0FFFF44A
SFLASH_ALT_PROT_ROW75	0x0FFFF44B
SFLASH_ALT_PROT_ROW76	0x0FFFF44C
SFLASH_ALT_PROT_ROW77	0x0FFFF44D
SFLASH_ALT_PROT_ROW78	0x0FFFF44E
SFLASH_ALT_PROT_ROW79	0x0FFFF44F
SFLASH_ALT_PROT_ROW80	0x0FFFF450
SFLASH_ALT_PROT_ROW81	0x0FFFF451
SFLASH_ALT_PROT_ROW82	0x0FFFF452
SFLASH_ALT_PROT_ROW83	0x0FFFF453
SFLASH_ALT_PROT_ROW84	0x0FFFF454
SFLASH_ALT_PROT_ROW85	0x0FFFF455
SFLASH_ALT_PROT_ROW86	0x0FFFF456
SFLASH_ALT_PROT_ROW87	0x0FFFF457
SFLASH_ALT_PROT_ROW88	0x0FFFF458
SFLASH_ALT_PROT_ROW89	0x0FFFF459
SFLASH_ALT_PROT_ROW90	0x0FFFF45A
SFLASH_ALT_PROT_ROW91	0x0FFFF45B
SFLASH_ALT_PROT_ROW92	0x0FFFF45C
SFLASH_ALT_PROT_ROW93	0x0FFFF45D
SFLASH_ALT_PROT_ROW94	0x0FFFF45E
SFLASH_ALT_PROT_ROW95	0x0FFFF45F
SFLASH_ALT_PROT_ROW96	0x0FFFF460
SFLASH_ALT_PROT_ROW97	0x0FFFF461
SFLASH_ALT_PROT_ROW98	0x0FFFF462
SFLASH_ALT_PROT_ROW99	0x0FFFF463
SFLASH_ALT_PROT_ROW100	0x0FFFF464
SFLASH_ALT_PROT_ROW101	0x0FFFF465

Register Name	Address
SFLASH_ALT_PROT_ROW102	0x0FFFF466
SFLASH_ALT_PROT_ROW103	0x0FFFF467
SFLASH_ALT_PROT_ROW104	0x0FFFF468
SFLASH_ALT_PROT_ROW105	0x0FFFF469
SFLASH_ALT_PROT_ROW106	0x0FFFF46A
SFLASH_ALT_PROT_ROW107	0x0FFFF46B
SFLASH_ALT_PROT_ROW108	0x0FFFF46C
SFLASH_ALT_PROT_ROW109	0x0FFFF46D
SFLASH_ALT_PROT_ROW110	0x0FFFF46E
SFLASH_ALT_PROT_ROW111	0x0FFFF46F
SFLASH_ALT_PROT_ROW112	0x0FFFF470
SFLASH_ALT_PROT_ROW113	0x0FFFF471
SFLASH_ALT_PROT_ROW114	0x0FFFF472
SFLASH_ALT_PROT_ROW115	0x0FFFF473
SFLASH_ALT_PROT_ROW116	0x0FFFF474
SFLASH_ALT_PROT_ROW117	0x0FFFF475
SFLASH_ALT_PROT_ROW118	0x0FFFF476
SFLASH_ALT_PROT_ROW119	0x0FFFF477
SFLASH_ALT_PROT_ROW120	0x0FFFF478
SFLASH_ALT_PROT_ROW121	0x0FFFF479
SFLASH_ALT_PROT_ROW122	0x0FFFF47A
SFLASH_ALT_PROT_ROW123	0x0FFFF47B
SFLASH_ALT_PROT_ROW124	0x0FFFF47C
SFLASH_ALT_PROT_ROW125	0x0FFFF47D
SFLASH_ALT_PROT_ROW126	0x0FFFF47E
SFLASH_ALT_PROT_ROW127	0x0FFFF47F
SFLASH_ALT_PROT_ROW128	0x0FFFF480
SFLASH_ALT_PROT_ROW129	0x0FFFF481
SFLASH_ALT_PROT_ROW130	0x0FFFF482
SFLASH_ALT_PROT_ROW131	0x0FFFF483
SFLASH_ALT_PROT_ROW132	0x0FFFF484
SFLASH_ALT_PROT_ROW133	0x0FFFF485
SFLASH_ALT_PROT_ROW134	0x0FFFF486
SFLASH_ALT_PROT_ROW135	0x0FFFF487
SFLASH_ALT_PROT_ROW136	0x0FFFF488
SFLASH_ALT_PROT_ROW137	0x0FFFF489
SFLASH_ALT_PROT_ROW138	0x0FFFF48A
SFLASH_ALT_PROT_ROW139	0x0FFFF48B
SFLASH_ALT_PROT_ROW140	0x0FFFF48C
SFLASH_ALT_PROT_ROW141	0x0FFFF48D
SFLASH_ALT_PROT_ROW142	0x0FFFF48E
SFLASH_ALT_PROT_ROW143	0x0FFFF48F

Register Name	Address
SFLASH_ALT_PROT_ROW144	0x0FFFF490
SFLASH_ALT_PROT_ROW145	0x0FFFF491
SFLASH_ALT_PROT_ROW146	0x0FFFF492
SFLASH_ALT_PROT_ROW147	0x0FFFF493
SFLASH_ALT_PROT_ROW148	0x0FFFF494
SFLASH_ALT_PROT_ROW149	0x0FFFF495
SFLASH_ALT_PROT_ROW150	0x0FFFF496
SFLASH_ALT_PROT_ROW151	0x0FFFF497
SFLASH_ALT_PROT_ROW152	0x0FFFF498
SFLASH_ALT_PROT_ROW153	0x0FFFF499
SFLASH_ALT_PROT_ROW154	0x0FFFF49A
SFLASH_ALT_PROT_ROW155	0x0FFFF49B
SFLASH_ALT_PROT_ROW156	0x0FFFF49C
SFLASH_ALT_PROT_ROW157	0x0FFFF49D
SFLASH_ALT_PROT_ROW158	0x0FFFF49E
SFLASH_ALT_PROT_ROW159	0x0FFFF49F
SFLASH_ALT_PROT_ROW160	0x0FFFF4A0
SFLASH_ALT_PROT_ROW161	0x0FFFF4A1
SFLASH_ALT_PROT_ROW162	0x0FFFF4A2
SFLASH_ALT_PROT_ROW163	0x0FFFF4A3
SFLASH_ALT_PROT_ROW164	0x0FFFF4A4
SFLASH_ALT_PROT_ROW165	0x0FFFF4A5
SFLASH_ALT_PROT_ROW166	0x0FFFF4A6
SFLASH_ALT_PROT_ROW167	0x0FFFF4A7
SFLASH_ALT_PROT_ROW168	0x0FFFF4A8
SFLASH_ALT_PROT_ROW169	0x0FFFF4A9
SFLASH_ALT_PROT_ROW170	0x0FFFF4AA
SFLASH_ALT_PROT_ROW171	0x0FFFF4AB
SFLASH_ALT_PROT_ROW172	0x0FFFF4AC
SFLASH_ALT_PROT_ROW173	0x0FFFF4AD
SFLASH_ALT_PROT_ROW174	0x0FFFF4AE
SFLASH_ALT_PROT_ROW175	0x0FFFF4AF
SFLASH_ALT_PROT_ROW176	0x0FFFF4B0
SFLASH_ALT_PROT_ROW177	0x0FFFF4B1
SFLASH_ALT_PROT_ROW178	0x0FFFF4B2
SFLASH_ALT_PROT_ROW179	0x0FFFF4B3
SFLASH_ALT_PROT_ROW180	0x0FFFF4B4
SFLASH_ALT_PROT_ROW181	0x0FFFF4B5
SFLASH_ALT_PROT_ROW182	0x0FFFF4B6
SFLASH_ALT_PROT_ROW183	0x0FFFF4B7
SFLASH_ALT_PROT_ROW184	0x0FFFF4B8
SFLASH_ALT_PROT_ROW185	0x0FFFF4B9

Register Name	Address
SFLASH_ALT_PROT_ROW186	0x0FFFF4BA
SFLASH_ALT_PROT_ROW187	0x0FFFF4BB
SFLASH_ALT_PROT_ROW188	0x0FFFF4BC
SFLASH_ALT_PROT_ROW189	0x0FFFF4BD
SFLASH_ALT_PROT_ROW190	0x0FFFF4BE
SFLASH_ALT_PROT_ROW191	0x0FFFF4BF
SFLASH_ALT_PROT_ROW192	0x0FFFF4C0
SFLASH_ALT_PROT_ROW193	0x0FFFF4C1
SFLASH_ALT_PROT_ROW194	0x0FFFF4C2
SFLASH_ALT_PROT_ROW195	0x0FFFF4C3
SFLASH_ALT_PROT_ROW196	0x0FFFF4C4
SFLASH_ALT_PROT_ROW197	0x0FFFF4C5
SFLASH_ALT_PROT_ROW198	0x0FFFF4C6
SFLASH_ALT_PROT_ROW199	0x0FFFF4C7
SFLASH_ALT_PROT_ROW200	0x0FFFF4C8
SFLASH_ALT_PROT_ROW201	0x0FFFF4C9
SFLASH_ALT_PROT_ROW202	0x0FFFF4CA
SFLASH_ALT_PROT_ROW203	0x0FFFF4CB
SFLASH_ALT_PROT_ROW204	0x0FFFF4CC
SFLASH_ALT_PROT_ROW205	0x0FFFF4CD
SFLASH_ALT_PROT_ROW206	0x0FFFF4CE
SFLASH_ALT_PROT_ROW207	0x0FFFF4CF
SFLASH_ALT_PROT_ROW208	0x0FFFF4D0
SFLASH_ALT_PROT_ROW209	0x0FFFF4D1
SFLASH_ALT_PROT_ROW210	0x0FFFF4D2
SFLASH_ALT_PROT_ROW211	0x0FFFF4D3
SFLASH_ALT_PROT_ROW212	0x0FFFF4D4
SFLASH_ALT_PROT_ROW213	0x0FFFF4D5
SFLASH_ALT_PROT_ROW214	0x0FFFF4D6
SFLASH_ALT_PROT_ROW215	0x0FFFF4D7
SFLASH_ALT_PROT_ROW216	0x0FFFF4D8
SFLASH_ALT_PROT_ROW217	0x0FFFF4D9
SFLASH_ALT_PROT_ROW218	0x0FFFF4DA
SFLASH_ALT_PROT_ROW219	0x0FFFF4DB
SFLASH_ALT_PROT_ROW220	0x0FFFF4DC
SFLASH_ALT_PROT_ROW221	0x0FFFF4DD
SFLASH_ALT_PROT_ROW222	0x0FFFF4DE
SFLASH_ALT_PROT_ROW223	0x0FFFF4DF
SFLASH_ALT_PROT_ROW224	0x0FFFF4E0
SFLASH_ALT_PROT_ROW225	0x0FFFF4E1
SFLASH_ALT_PROT_ROW226	0x0FFFF4E2
SFLASH_ALT_PROT_ROW227	0x0FFFF4E3

Register Name	Address
SFLASH_ALT_PROT_ROW228	0x0FFFF4E4
SFLASH_ALT_PROT_ROW229	0x0FFFF4E5
SFLASH_ALT_PROT_ROW230	0x0FFFF4E6
SFLASH_ALT_PROT_ROW231	0x0FFFF4E7
SFLASH_ALT_PROT_ROW232	0x0FFFF4E8
SFLASH_ALT_PROT_ROW233	0x0FFFF4E9
SFLASH_ALT_PROT_ROW234	0x0FFFF4EA
SFLASH_ALT_PROT_ROW235	0x0FFFF4EB
SFLASH_ALT_PROT_ROW236	0x0FFFF4EC
SFLASH_ALT_PROT_ROW237	0x0FFFF4ED
SFLASH_ALT_PROT_ROW238	0x0FFFF4EE
SFLASH_ALT_PROT_ROW239	0x0FFFF4EF
SFLASH_ALT_PROT_ROW240	0x0FFFF4F0
SFLASH_ALT_PROT_ROW241	0x0FFFF4F1
SFLASH_ALT_PROT_ROW242	0x0FFFF4F2
SFLASH_ALT_PROT_ROW243	0x0FFFF4F3
SFLASH_ALT_PROT_ROW244	0x0FFFF4F4
SFLASH_ALT_PROT_ROW245	0x0FFFF4F5
SFLASH_ALT_PROT_ROW246	0x0FFFF4F6
SFLASH_ALT_PROT_ROW247	0x0FFFF4F7
SFLASH_ALT_PROT_ROW248	0x0FFFF4F8
SFLASH_ALT_PROT_ROW249	0x0FFFF4F9
SFLASH_ALT_PROT_ROW250	0x0FFFF4FA
SFLASH_ALT_PROT_ROW251	0x0FFFF4FB
SFLASH_ALT_PROT_ROW252	0x0FFFF4FC
SFLASH_ALT_PROT_ROW253	0x0FFFF4FD
SFLASH_ALT_PROT_ROW254	0x0FFFF4FE
SFLASH_ALT_PROT_ROW255	0x0FFFF4FF
SFLASH_ALT_PP	0x0FFFF5A0
SFLASH_ALT_E	0x0FFFF5A4
SFLASH_ALT_P	0x0FFFF5A8
SFLASH_ALT_EA_E	0x0FFFF5AC
SFLASH_ALT_EA_P	0x0FFFF5B0
SFLASH_ALT_ES_E	0x0FFFF5B4
SFLASH_ALT_ES_P_EO	0x0FFFF5B8
SFLASH_ALT_E_VCTAT	0x0FFFF5BC
SFLASH_ALT_P_VCTAT	0x0FFFF5BD

28.1.1 SFLASH_PROT_ROW0

Per Page Write Protection

Address: 0x0FFFF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.2 SFLASH_PROT_ROW1

Per Page Write Protection

Address: 0x0FFFF001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.3 SFLASH_PROT_ROW2

Per Page Write Protection

Address: 0x0FFFF002

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.4 SFLASH_PROT_ROW3

Per Page Write Protection

Address: 0x0FFFF003

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.5 SFLASH_PROT_ROW4

Per Page Write Protection

Address: 0x0FFFF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.6 SFLASH_PROT_ROW5

Per Page Write Protection

Address: 0x0FFFF005

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.7 SFLASH_PROT_ROW6

Per Page Write Protection

Address: 0x0FFFF006

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.8 SFLASH_PROT_ROW7

Per Page Write Protection

Address: 0x0FFFF007

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.9 SFLASH_PROT_ROW8

Per Page Write Protection

Address: 0x0FFFF008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.10 SFLASH_PROT_ROW9

Per Page Write Protection

Address: 0x0FFFF009

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.11 SFLASH_PROT_ROW10

Per Page Write Protection

Address: 0x0FFFF00A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.12 SFLASH_PROT_ROW11

Per Page Write Protection

Address: 0x0FFFF00B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.13 SFLASH_PROT_ROW12

Per Page Write Protection

Address: 0x0FFFF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.14 SFLASH_PROT_ROW13

Per Page Write Protection

Address: 0x0FFFF00D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.15 SFLASH_PROT_ROW14

Per Page Write Protection

Address: 0x0FFFF00E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.16 SFLASH_PROT_ROW15

Per Page Write Protection

Address: 0x0FFFF00F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.17 SFLASH_PROT_ROW16

Per Page Write Protection

Address: 0x0FFFF010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.18 SFLASH_PROT_ROW17

Per Page Write Protection

Address: 0x0FFFF011

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.19 SFLASH_PROT_ROW18

Per Page Write Protection

Address: 0x0FFFF012

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.20 SFLASH_PROT_ROW19

Per Page Write Protection

Address: 0x0FFFF013

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.21 SFLASH_PROT_ROW20

Per Page Write Protection

Address: 0x0FFFF014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.22 SFLASH_PROT_ROW21

Per Page Write Protection

Address: 0x0FFFF015

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.23 SFLASH_PROT_ROW22

Per Page Write Protection

Address: 0x0FFFF016

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.24 SFLASH_PROT_ROW23

Per Page Write Protection

Address: 0x0FFFF017

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.25 SFLASH_PROT_ROW24

Per Page Write Protection

Address: 0x0FFFF018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.26 SFLASH_PROT_ROW25

Per Page Write Protection

Address: 0x0FFFF019

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.27 SFLASH_PROT_ROW26

Per Page Write Protection

Address: 0x0FFFF01A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.28 SFLASH_PROT_ROW27

Per Page Write Protection

Address: 0x0FFFF01B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.29 SFLASH_PROT_ROW28

Per Page Write Protection

Address: 0x0FFFF01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.30 SFLASH_PROT_ROW29

Per Page Write Protection

Address: 0x0FFFF01D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.31 SFLASH_PROT_ROW30

Per Page Write Protection

Address: 0x0FFFF01E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.32 SFLASH_PROT_ROW31

Per Page Write Protection

Address: 0x0FFFF01F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.33 SFLASH_PROT_ROW32

Per Page Write Protection

Address: 0x0FFFF020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.34 SFLASH_PROT_ROW33

Per Page Write Protection

Address: 0x0FFFF021

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.35 SFLASH_PROT_ROW34

Per Page Write Protection

Address: 0x0FFFF022

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.36 SFLASH_PROT_ROW35

Per Page Write Protection

Address: 0x0FFFF023

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.37 SFLASH_PROT_ROW36

Per Page Write Protection

Address: 0x0FFFF024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.38 SFLASH_PROT_ROW37

Per Page Write Protection

Address: 0x0FFFF025

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.39 SFLASH_PROT_ROW38

Per Page Write Protection

Address: 0x0FFFF026

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.40 SFLASH_PROT_ROW39

Per Page Write Protection

Address: 0x0FFFF027

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.41 SFLASH_PROT_ROW40

Per Page Write Protection

Address: 0x0FFFF028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.42 SFLASH_PROT_ROW41

Per Page Write Protection

Address: 0x0FFFF029

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.43 SFLASH_PROT_ROW42

Per Page Write Protection

Address: 0x0FFFF02A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.44 SFLASH_PROT_ROW43

Per Page Write Protection

Address: 0x0FFFF02B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.45 SFLASH_PROT_ROW44

Per Page Write Protection

Address: 0x0FFFF02C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.46 SFLASH_PROT_ROW45

Per Page Write Protection

Address: 0x0FFFF02D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.47 SFLASH_PROT_ROW46

Per Page Write Protection

Address: 0x0FFFF02E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.48 SFLASH_PROT_ROW47

Per Page Write Protection

Address: 0x0FFFF02F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.49 SFLASH_PROT_ROW48

Per Page Write Protection

Address: 0x0FFFF030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.50 SFLASH_PROT_ROW49

Per Page Write Protection

Address: 0x0FFFF031

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.51 SFLASH_PROT_ROW50

Per Page Write Protection

Address: 0x0FFFF032

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.52 SFLASH_PROT_ROW51

Per Page Write Protection

Address: 0x0FFFF033

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.53 SFLASH_PROT_ROW52

Per Page Write Protection

Address: 0x0FFFF034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.54 SFLASH_PROT_ROW53

Per Page Write Protection

Address: 0x0FFFF035

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.55 SFLASH_PROT_ROW54

Per Page Write Protection

Address: 0x0FFFF036

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.56 SFLASH_PROT_ROW55

Per Page Write Protection

Address: 0x0FFFF037

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.57 SFLASH_PROT_ROW56

Per Page Write Protection

Address: 0x0FFFF038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.58 SFLASH_PROT_ROW57

Per Page Write Protection

Address: 0x0FFFF039

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.59 SFLASH_PROT_ROW58

Per Page Write Protection

Address: 0x0FFFF03A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.60 SFLASH_PROT_ROW59

Per Page Write Protection

Address: 0x0FFFF03B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.61 SFLASH_PROT_ROW60

Per Page Write Protection

Address: 0x0FFFF03C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.62 SFLASH_PROT_ROW61

Per Page Write Protection

Address: 0x0FFFF03D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.63 SFLASH_PROT_ROW62

Per Page Write Protection

Address: 0x0FFFF03E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.64 SFLASH_PROT_ROW63

Per Page Write Protection

Address: 0x0FFFF03F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.65 SFLASH_PROT_PROTECTION

Protection Level

Address: 0x0FFFF07F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						None	
Name	None [7:2]						PROT_LEVEL [1:0]	

Bits	Name	Description
1 : 0	PROT_LEVEL	Current Protection Mode - note that encoding is different from CPUSS_PROTECTION !! Default Value: X **0x0: OPEN:** System is in OPEN mode **0x1: VIRGIN:** System is in VIRGIN mode **0x2: PROTECTED:** System is in PROTECTED mode **0x3: KILL:** System is in KILL mode

28.1.66 SFLASH_AV_PAIRS_8B0

8b Addr/Value pair Section

Address: 0x0FFFF080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.67 SFLASH_AV_PAIRS_8B1

8b Addr/Value pair Section

Address: 0x0FFFF081

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.68 SFLASH_AV_PAIRS_8B2

8b Addr/Value pair Section

Address: 0x0FFFF082

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.69 SFLASH_AV_PAIRS_8B3

8b Addr/Value pair Section

Address: 0x0FFFF083

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.70 SFLASH_AV_PAIRS_8B4

8b Addr/Value pair Section

Address: 0x0FFFF084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.71 SFLASH_AV_PAIRS_8B5

8b Addr/Value pair Section

Address: 0x0FFFF085

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.72 SFLASH_AV_PAIRS_8B6

8b Addr/Value pair Section

Address: 0x0FFFF086

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.73 SFLASH_AV_PAIRS_8B7

8b Addr/Value pair Section

Address: 0x0FFFF087

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.74 SFLASH_AV_PAIRS_8B8

8b Addr/Value pair Section

Address: 0x0FFFF088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.75 SFLASH_AV_PAIRS_8B9

8b Addr/Value pair Section

Address: 0x0FFFF089

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.76 SFLASH_AV_PAIRS_8B10

8b Addr/Value pair Section

Address: 0x0FFFF08A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.77 SFLASH_AV_PAIRS_8B11

8b Addr/Value pair Section

Address: 0x0FFFF08B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.78 SFLASH_AV_PAIRS_8B12

8b Addr/Value pair Section

Address: 0x0FFFF08C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.79 SFLASH_AV_PAIRS_8B13

8b Addr/Value pair Section

Address: 0x0FFFF08D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.80 SFLASH_AV_PAIRS_8B14

8b Addr/Value pair Section

Address: 0x0FFFF08E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.81 SFLASH_AV_PAIRS_8B15

8b Addr/Value pair Section

Address: 0x0FFFF08F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.82 SFLASH_AV_PAIRS_8B16

8b Addr/Value pair Section

Address: 0x0FFFF090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.83 SFLASH_AV_PAIRS_8B17

8b Addr/Value pair Section

Address: 0x0FFFF091

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.84 SFLASH_AV_PAIRS_8B18

8b Addr/Value pair Section

Address: 0x0FFFF092

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.85 SFLASH_AV_PAIRS_8B19

8b Addr/Value pair Section

Address: 0x0FFFF093

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.86 SFLASH_AV_PAIRS_8B20

8b Addr/Value pair Section

Address: 0x0FFFF094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.87 SFLASH_AV_PAIRS_8B21

8b Addr/Value pair Section

Address: 0x0FFFF095

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.88 SFLASH_AV_PAIRS_8B22

8b Addr/Value pair Section

Address: 0x0FFFF096

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.89 SFLASH_AV_PAIRS_8B23

8b Addr/Value pair Section

Address: 0x0FFFF097

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.90 SFLASH_AV_PAIRS_8B24

8b Addr/Value pair Section

Address: 0x0FFFF098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.91 SFLASH_AV_PAIRS_8B25

8b Addr/Value pair Section

Address: 0x0FFFF099

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.92 SFLASH_AV_PAIRS_8B26

8b Addr/Value pair Section

Address: 0x0FFFF09A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.93 SFLASH_AV_PAIRS_8B27

8b Addr/Value pair Section

Address: 0x0FFFF09B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.94 SFLASH_AV_PAIRS_8B28

8b Addr/Value pair Section

Address: 0x0FFFF09C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.95 SFLASH_AV_PAIRS_8B29

8b Addr/Value pair Section

Address: 0x0FFFF09D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.96 SFLASH_AV_PAIRS_8B30

8b Addr/Value pair Section

Address: 0x0FFFF09E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.97 SFLASH_AV_PAIRS_8B31

8b Addr/Value pair Section

Address: 0x0FFFF09F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.98 SFLASH_AV_PAIRS_8B32

8b Addr/Value pair Section

Address: 0x0FFFF0A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.99 SFLASH_AV_PAIRS_8B33

8b Addr/Value pair Section

Address: 0x0FFFF0A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.100 SFLASH_AV_PAIRS_8B34

8b Addr/Value pair Section

Address: 0x0FFFF0A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.101 SFLASH_AV_PAIRS_8B35

8b Addr/Value pair Section

Address: 0x0FFFF0A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.102 SFLASH_AV_PAIRS_8B36

8b Addr/Value pair Section

Address: 0x0FFFF0A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.103 SFLASH_AV_PAIRS_8B37

8b Addr/Value pair Section

Address: 0x0FFFF0A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.104 SFLASH_AV_PAIRS_8B38

8b Addr/Value pair Section

Address: 0x0FFFF0A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.105 SFLASH_AV_PAIRS_8B39

8b Addr/Value pair Section

Address: 0x0FFFF0A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.106 SFLASH_AV_PAIRS_8B40

8b Addr/Value pair Section

Address: 0x0FFFF0A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.107 SFLASH_AV_PAIRS_8B41

8b Addr/Value pair Section

Address: 0x0FFFF0A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.108 SFLASH_AV_PAIRS_8B42

8b Addr/Value pair Section

Address: 0x0FFFF0AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.109 SFLASH_AV_PAIRS_8B43

8b Addr/Value pair Section

Address: 0x0FFFF0AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.110 SFLASH_AV_PAIRS_8B44

8b Addr/Value pair Section

Address: 0x0FFFF0AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.111 SFLASH_AV_PAIRS_8B45

8b Addr/Value pair Section

Address: 0x0FFFF0AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.112 SFLASH_AV_PAIRS_8B46

8b Addr/Value pair Section

Address: 0x0FFFF0AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.113 SFLASH_AV_PAIRS_8B47

8b Addr/Value pair Section

Address: 0x0FFFF0AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.114 SFLASH_AV_PAIRS_8B48

8b Addr/Value pair Section

Address: 0x0FFFF0B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.115 SFLASH_AV_PAIRS_8B49

8b Addr/Value pair Section

Address: 0x0FFFF0B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.116 SFLASH_AV_PAIRS_8B50

8b Addr/Value pair Section

Address: 0x0FFFF0B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.117 SFLASH_AV_PAIRS_8B51

8b Addr/Value pair Section

Address: 0x0FFFF0B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.118 SFLASH_AV_PAIRS_8B52

8b Addr/Value pair Section

Address: 0x0FFFF0B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.119 SFLASH_AV_PAIRS_8B53

8b Addr/Value pair Section

Address: 0x0FFFF0B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.120 SFLASH_AV_PAIRS_8B54

8b Addr/Value pair Section

Address: 0x0FFFF0B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.121 SFLASH_AV_PAIRS_8B55

8b Addr/Value pair Section

Address: 0x0FFFF0B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.122 SFLASH_AV_PAIRS_8B56

8b Addr/Value pair Section

Address: 0x0FFFF0B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.123 SFLASH_AV_PAIRS_8B57

8b Addr/Value pair Section

Address: 0x0FFFF0B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.124 SFLASH_AV_PAIRS_8B58

8b Addr/Value pair Section

Address: 0x0FFFF0BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.125 SFLASH_AV_PAIRS_8B59

8b Addr/Value pair Section

Address: 0x0FFFF0BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.126 SFLASH_AV_PAIRS_8B60

8b Addr/Value pair Section

Address: 0x0FFFF0BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.127 SFLASH_AV_PAIRS_8B61

8b Addr/Value pair Section

Address: 0x0FFFF0BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.128 SFLASH_AV_PAIRS_8B62

8b Addr/Value pair Section

Address: 0x0FFFF0BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.129 SFLASH_AV_PAIRS_8B63

8b Addr/Value pair Section

Address: 0x0FFFF0BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.130 SFLASH_AV_PAIRS_8B64

8b Addr/Value pair Section

Address: 0x0FFFF0C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.131 SFLASH_AV_PAIRS_8B65

8b Addr/Value pair Section

Address: 0x0FFFF0C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.132 SFLASH_AV_PAIRS_8B66

8b Addr/Value pair Section

Address: 0x0FFFF0C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.133 SFLASH_AV_PAIRS_8B67

8b Addr/Value pair Section

Address: 0x0FFFF0C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.134 SFLASH_AV_PAIRS_8B68

8b Addr/Value pair Section

Address: 0x0FFFF0C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.135 SFLASH_AV_PAIRS_8B69

8b Addr/Value pair Section

Address: 0x0FFFF0C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.136 SFLASH_AV_PAIRS_8B70

8b Addr/Value pair Section

Address: 0x0FFFF0C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.137 SFLASH_AV_PAIRS_8B71

8b Addr/Value pair Section

Address: 0x0FFFF0C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.138 SFLASH_AV_PAIRS_8B72

8b Addr/Value pair Section

Address: 0x0FFFF0C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.139 SFLASH_AV_PAIRS_8B73

8b Addr/Value pair Section

Address: 0x0FFFF0C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.140 SFLASH_AV_PAIRS_8B74

8b Addr/Value pair Section

Address: 0x0FFFF0CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.141 SFLASH_AV_PAIRS_8B75

8b Addr/Value pair Section

Address: 0x0FFFF0CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.142 SFLASH_AV_PAIRS_8B76

8b Addr/Value pair Section

Address: 0x0FFFF0CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.143 SFLASH_AV_PAIRS_8B77

8b Addr/Value pair Section

Address: 0x0FFFF0CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.144 SFLASH_AV_PAIRS_8B78

8b Addr/Value pair Section

Address: 0x0FFFF0CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.145 SFLASH_AV_PAIRS_8B79

8b Addr/Value pair Section

Address: 0x0FFFF0CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.146 SFLASH_AV_PAIRS_8B80

8b Addr/Value pair Section

Address: 0x0FFFF0D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.147 SFLASH_AV_PAIRS_8B81

8b Addr/Value pair Section

Address: 0x0FFFF0D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.148 SFLASH_AV_PAIRS_8B82

8b Addr/Value pair Section

Address: 0x0FFFF0D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.149 SFLASH_AV_PAIRS_8B83

8b Addr/Value pair Section

Address: 0x0FFFF0D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.150 SFLASH_AV_PAIRS_8B84

8b Addr/Value pair Section

Address: 0x0FFFF0D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.151 SFLASH_AV_PAIRS_8B85

8b Addr/Value pair Section

Address: 0x0FFFF0D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.152 SFLASH_AV_PAIRS_8B86

8b Addr/Value pair Section

Address: 0x0FFFF0D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.153 SFLASH_AV_PAIRS_8B87

8b Addr/Value pair Section

Address: 0x0FFFF0D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.154 SFLASH_AV_PAIRS_8B88

8b Addr/Value pair Section

Address: 0x0FFFF0D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.155 SFLASH_AV_PAIRS_8B89

8b Addr/Value pair Section

Address: 0x0FFFF0D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.156 SFLASH_AV_PAIRS_8B90

8b Addr/Value pair Section

Address: 0x0FFFF0DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.157 SFLASH_AV_PAIRS_8B91

8b Addr/Value pair Section

Address: 0x0FFFF0DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.158 SFLASH_AV_PAIRS_8B92

8b Addr/Value pair Section

Address: 0x0FFFF0DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.159 SFLASH_AV_PAIRS_8B93

8b Addr/Value pair Section

Address: 0x0FFFF0DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.160 SFLASH_AV_PAIRS_8B94

8b Addr/Value pair Section

Address: 0x0FFFF0DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.161 SFLASH_AV_PAIRS_8B95

8b Addr/Value pair Section

Address: 0x0FFFF0DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.162 SFLASH_AV_PAIRS_8B96

8b Addr/Value pair Section

Address: 0x0FFFF0E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.163 SFLASH_AV_PAIRS_8B97

8b Addr/Value pair Section

Address: 0x0FFFF0E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.164 SFLASH_AV_PAIRS_8B98

8b Addr/Value pair Section

Address: 0x0FFFF0E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.165 SFLASH_AV_PAIRS_8B99

8b Addr/Value pair Section

Address: 0x0FFFF0E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.166 SFLASH_AV_PAIRS_8B100

8b Addr/Value pair Section

Address: 0x0FFFF0E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.167 SFLASH_AV_PAIRS_8B101

8b Addr/Value pair Section

Address: 0x0FFFF0E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.168 SFLASH_AV_PAIRS_8B102

8b Addr/Value pair Section

Address: 0x0FFFF0E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.169 SFLASH_AV_PAIRS_8B103

8b Addr/Value pair Section

Address: 0x0FFFF0E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.170 SFLASH_AV_PAIRS_8B104

8b Addr/Value pair Section

Address: 0x0FFFF0E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.171 SFLASH_AV_PAIRS_8B105

8b Addr/Value pair Section

Address: 0x0FFFF0E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.172 SFLASH_AV_PAIRS_8B106

8b Addr/Value pair Section

Address: 0x0FFFF0EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.173 SFLASH_AV_PAIRS_8B107

8b Addr/Value pair Section

Address: 0x0FFFF0EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.174 SFLASH_AV_PAIRS_8B108

8b Addr/Value pair Section

Address: 0x0FFFF0EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.175 SFLASH_AV_PAIRS_8B109

8b Addr/Value pair Section

Address: 0x0FFFF0ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.176 SFLASH_AV_PAIRS_8B110

8b Addr/Value pair Section

Address: 0x0FFFF0EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.177 SFLASH_AV_PAIRS_8B111

8b Addr/Value pair Section

Address: 0x0FFFF0EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.178 SFLASH_AV_PAIRS_8B112

8b Addr/Value pair Section

Address: 0x0FFFF0F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.179 SFLASH_AV_PAIRS_8B113

8b Addr/Value pair Section

Address: 0x0FFFF0F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.180 SFLASH_AV_PAIRS_8B114

8b Addr/Value pair Section

Address: 0x0FFFF0F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.181 SFLASH_AV_PAIRS_8B115

8b Addr/Value pair Section

Address: 0x0FFFF0F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.182 SFLASH_AV_PAIRS_8B116

8b Addr/Value pair Section

Address: 0x0FFFF0F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.183 SFLASH_AV_PAIRS_8B117

8b Addr/Value pair Section

Address: 0x0FFFF0F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.184 SFLASH_AV_PAIRS_8B118

8b Addr/Value pair Section

Address: 0x0FFFF0F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.185 SFLASH_AV_PAIRS_8B119

8b Addr/Value pair Section

Address: 0x0FFFF0F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.186 SFLASH_AV_PAIRS_8B120

8b Addr/Value pair Section

Address: 0x0FFFF0F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.187 SFLASH_AV_PAIRS_8B121

8b Addr/Value pair Section

Address: 0x0FFFF0F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.188 SFLASH_AV_PAIRS_8B122

8b Addr/Value pair Section

Address: 0x0FFFF0FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.189 SFLASH_AV_PAIRS_8B123

8b Addr/Value pair Section

Address: 0x0FFFF0FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.190 SFLASH_AV_PAIRS_8B124

8b Addr/Value pair Section

Address: 0x0FFFF0FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.191 SFLASH_AV_PAIRS_8B125

8b Addr/Value pair Section

Address: 0x0FFFF0FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.192 SFLASH_AV_PAIRS_8B126

8b Addr/Value pair Section

Address: 0x0FFFF0FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.193 SFLASH_AV_PAIRS_8B127

8b Addr/Value pair Section

Address: 0x0FFFF0FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

28.1.194 SFLASH_AV_PAIRS_32B0

32b Addr/Value pair Section

Address: 0x0FFFF100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

28.1.195 SFLASH_AV_PAIRS_32B1

32b Addr/Value pair Section

Address: 0x0FFFF104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

28.1.196 SFLASH_AV_PAIRS_32B2

32b Addr/Value pair Section

Address: 0x0FFFF108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

28.1.197 SFLASH_AV_PAIRS_32B3

32b Addr/Value pair Section

Address: 0x0FFFF10C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

28.1.198 SFLASH_AV_PAIRS_32B4

32b Addr/Value pair Section

Address: 0x0FFFF110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

28.1.199 SFLASH_AV_PAIRS_32B5

32b Addr/Value pair Section

Address: 0x0FFFF114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

28.1.200 SFLASH_AV_PAIRS_32B6

32b Addr/Value pair Section

Address: 0x0FFFF118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

28.1.201 SFLASH_AV_PAIRS_32B7

32b Addr/Value pair Section

Address: 0x0FFFF11C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

28.1.202 SFLASH_AV_PAIRS_32B8

32b Addr/Value pair Section

Address: 0x0FFFF120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

28.1.203 SFLASH_AV_PAIRS_32B9

32b Addr/Value pair Section

Address: 0x0FFFF124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

28.1.204 SFLASH_AV_PAIRS_32B10

32b Addr/Value pair Section

Address: 0x0FFFF128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

28.1.205 SFLASH_AV_PAIRS_32B11

32b Addr/Value pair Section

Address: 0x0FFFF12C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

28.1.206 SFLASH_AV_PAIRS_32B12

32b Addr/Value pair Section

Address: 0x0FFFF130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

28.1.207 SFLASH_AV_PAIRS_32B13

32b Addr/Value pair Section

Address: 0x0FFFF134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

28.1.208 SFLASH_AV_PAIRS_32B14

32b Addr/Value pair Section

Address: 0x0FFFF138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

28.1.209 SFLASH_AV_PAIRS_32B15

32b Addr/Value pair Section

Address: 0x0FFFF13C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

28.1.210 SFLASH_SILICON_ID

Silicon ID

Address: 0x0FFFF144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ID	Silicon ID Default Value: X

28.1.211 SFLASH_CPUSS_PRIV_RAM

RAM Privileged Limit

Address: 0x0FFFF148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RAM_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RAM_PROT_LIMIT

Bits	Name	Description
8 : 0	RAM_PROT_LIMIT	Indicates the limit where the privileged area of SRAM starts in increments of 256 Bytes. "0": Entire SRAM is Privileged. "1": First 256 Bytes are User accessable. Any number larger than the size of the SRAM indicates that the entire SRAM is user mode accessible. Default Value: 0

28.1.212 SFLASH_CPUSS_PRIV_ROM_BROM

Boot ROM Privileged Limit

Address: 0x0FFFF14A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BROM_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 0	BROM_PROT_LIMIT	Indicates the limit where the privileged area of the Boot ROM partition starts in increments of 256 Bytes. "0": Entire Boot ROM is Privileged. "1": First 256 Bytes are User accessable. ... BROM_PROT_LIMIT >= "Boot ROM partition capacity": Entire Boot ROM partition is user mode accessible. Default Value: 0

28.1.213 SFLASH_CPUSS_PRIV_FLASH

Flash Privileged Limit

Address: 0x0FFFF14C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FLASH_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					FLASH_PROT_LIMIT [10:8]		

Bits	Name	Description
10 : 0	FLASH_PROT_LIMIT	Indicates the limit where the privileged area of flash starts in increments of 256 Bytes. "0": Entire flash is Privileged. "1": First 256 Bytes are User accessable. Any number larger than the size of the flash indicates that the entire flash is user mode accessible. Note that SuperVisory rows are always User accessable. If FLASH_PROT_LIMIT defines a non-empty privileged area, the boot ROM will assume that a system call table exists at the beginning of the Flash privileged area and use it for all SystemCalls made using SYSREQ. Default Value: 0

28.1.214 SFLASH_CPUSS_PRIV_ROM_SROM

System ROM Privileged Limit

Address: 0x0FFFF14E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SROM_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SROM_PROT_LIMIT [9:8]	

Bits	Name	Description
9 : 0	SROM_PROT_LIMIT	Indicates the limit where the privileged area of System ROM partition starts in increments of 256 Bytes. The limit is wrt. the start of the ROM memory (start of the Boot ROM partition). SROM_PROT_LIMIT * 256 Byte <= "Boot ROM partition capacity": Entire System ROM is Privileged. SROM_PROT_LIMIT * 256 Byte > "Boot ROM partition capacity": First SROM_PROT_LIMIT * 256 - "Boot ROM partition capacity" Bytes are User accessable. ... SROM_PROT_LIMIT >= "ROM capacity": Entire System ROM is user mode accessible. Default Value: 0

28.1.215 SFLASH_HIB_KEY_DELAY

Hibernate wakeup value for PWR_KEY_DELAY

Address: 0x0FFFF150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

28.1.216 SFLASH_DPSLP_KEY_DELAY

DeepSleep wakeup value for PWR_KEY_DELAY

Address: 0x0FFFF152

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

28.1.217 SFLASH_SWD_CONFIG

SWD pinout selector

Address: 0x0FFFF154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							None
Name	None [7:1]							SWD_SELECT

Bits	Name	Description
0	SWD_SELECT	0: Use Primary SWD location 1: Use Alternate SWD location Default Value: X

28.1.218 SFLASH_INITIAL_SPCIF_TRIM_M1_DAC0

FLASH IDAC trim used during boot

Address: 0x0FFFF155

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	SLOPE [7:5]			IDAC [4:0]				

Bits	Name	Description
7 : 5	SLOPE	See SPCIF_TRIM1 Default Value: 0
4 : 0	IDAC	See SPCIF_TRIM1 Default Value: 0

28.1.219 SFLASH_SWD_LISTEN

Listen Window Length

Address: 0x0FFFF158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	CYCLES [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	CYCLES [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	CYCLES [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	CYCLES [31:24]							

Bits	Name	Description
31 : 0	CYCLES	Number of clock cycles Default Value: X

28.1.220 SFLASH_FLASH_START

Flash Image Start Address

Address: 0x0FFFF15C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	ADDRESS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	ADDRESS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	ADDRESS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	ADDRESS [31:24]							

Bits	Name	Description
31 : 0	ADDRESS	Start Address Default Value: X

28.1.221 SFLASH_CSD_TRIM1_HVIDAC

CSD Trim Data for HVIDAC operation

Address: 0x0FFFF160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

28.1.222 SFLASH_CSD_TRIM2_HVIDAC

CSD Trim Data for HVIDAC operation

Address: 0x0FFFF161

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

28.1.223 SFLASH_CSD_TRIM1_CSD

CSD Trim Data for (normal) CSD operation

Address: 0x0FFFF162

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

28.1.224 SFLASH_CSD_TRIM2_CSD

CSD Trim Data for (normal) CSD operation

Address: 0x0FFFF163

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

28.1.225 SFLASH_SAR_TEMP_MULTIPLIER

SAR Temperature Sensor Multiplication Factor

Address: 0x0FFFF164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TEMP_MULTIPLIER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	TEMP_MULTIPLIER [15:8]							

Bits	Name	Description
15 : 0	TEMP_MULTIPLIER	Multiplier value for SAR temperature sensor in fixed point 0.16 format. Default Value: X

28.1.226 SFLASH_SAR_TEMP_OFFSET

SAR Temperature Sensor Offset

Address: 0x0FFFF166

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TEMP_OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	TEMP_OFFSET [15:8]							

Bits	Name	Description
15 : 0	TEMP_OFFSET	Offset value for SAR temperature sensor in fixed point 10.6 format. Default Value: X

28.1.227 SFLASH_SKIP_CHECKSUM

Checksum Skip Option Register

Address: 0x0FFFF169

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SKIP [7:0]							

Bits	Name	Description
7 : 0	SKIP	0: Perform checksum check (see CHECKSUM fueld below) 1: Skip checksum check >1: Undefined - do not use Default Value: X

28.1.228 SFLASH_PROT_VIRGINKEY0

Virgin Protection Mode Key

Address: 0x0FFFF170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

28.1.229 SFLASH_PROT_VIRGINKEY1

Virgin Protection Mode Key

Address: 0x0FFFF171

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

28.1.230 SFLASH_PROT_VIRGINKEY2

Virgin Protection Mode Key

Address: 0x0FFFF172

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

28.1.231 SFLASH_PROT_VIRGINKEY3

Virgin Protection Mode Key

Address: 0x0FFFF173

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

28.1.232 SFLASH_PROT_VIRGINKEY4

Virgin Protection Mode Key

Address: 0x0FFFF174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

28.1.233 SFLASH_PROT_VIRGINKEY5

Virgin Protection Mode Key

Address: 0x0FFFF175

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

28.1.234 SFLASH_PROT_VIRGINKEY6

Virgin Protection Mode Key

Address: 0x0FFFF176

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

28.1.235 SFLASH_PROT_VIRGINKEY7

Virgin Protection Mode Key

Address: 0x0FFFF177

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

28.1.236 SFLASH_DIE_LOT0

Lot Number (3 bytes)

Address: 0x0FFFF178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	LOT [7:0]							

Bits	Name	Description
7 : 0	LOT	Lot Number Byte Default Value: X

28.1.237 SFLASH_DIE_LOT1

Lot Number (3 bytes)

Address: 0x0FFFF179

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	LOT [7:0]							

Bits	Name	Description
7 : 0	LOT	Lot Number Byte Default Value: X

28.1.238 SFLASH_DIE_LOT2

Lot Number (3 bytes)

Address: 0x0FFFF17A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	LOT [7:0]							

Bits	Name	Description
7 : 0	LOT	Lot Number Byte Default Value: X

28.1.239 SFLASH_DIE_WAFER

Wafer Number

Address: 0x0FFFF17B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	WAFER [7:0]							

Bits	Name	Description
7 : 0	WAFER	Wafer Number Default Value: X

28.1.240 SFLASH_DIE_X

X Position on Wafer, CRI Pass/Fail Bin

Address: 0x0FFFF17C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	X [7:0]							

Bits	Name	Description
7 : 0	X	X Position Default Value: X

28.1.241 SFLASH_DIE_Y

Y Position on Wafer, CHI Pass/Fail Bin

Address: 0x0FFFF17D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	Y [7:0]							

Bits	Name	Description
7 : 0	Y	Y Position Default Value: X

28.1.242 SFLASH_DIE_SORT

Sort1/2/3 Pass/Fail Bin

Address: 0x0FFFF17E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		None	None	None	None	None	None
Name	None [7:6]		ENG_PASS	CHI_PASS	CRI_PASS	S3_PASS	S2_PASS	S1_PASS

Bits	Name	Description
5	ENG_PASS	ENG Pass Bin Default Value: X
4	CHI_PASS	CHI Pass Bin (1) or 0 (Fail Bin) Default Value: X
3	CRI_PASS	CRI Pass Bin (1) or 0 (Fail Bin) Default Value: X
2	S3_PASS	SORT3 Pass Bin (1) or 0 (Fail Bin) Default Value: X
1	S2_PASS	SORT2 Pass Bin (1) or 0 (Fail Bin) Default Value: X
0	S1_PASS	SORT1 Pass Bin (1) or 0 (Fail Bin) Default Value: X

28.1.243 SFLASH_DIE_MINOR

Minor Revision Number

Address: 0x0FFFF17F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	MINOR [7:0]							

Bits	Name	Description
7 : 0	MINOR	Minor revision number Default Value: X

28.1.244 SFLASH_PE_TE_DATA0

PE/TE Data

Address: 0x0FFFF180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.245 SFLASH_PE_TE_DATA1

PE/TE Data

Address: 0x0FFFF181

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.246 SFLASH_PE_TE_DATA2

PE/TE Data

Address: 0x0FFFF182

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.247 SFLASH_PE_TE_DATA3

PE/TE Data

Address: 0x0FFFF183

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.248 SFLASH_PE_TE_DATA4

PE/TE Data

Address: 0x0FFFF184

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.249 SFLASH_PE_TE_DATA5

PE/TE Data

Address: 0x0FFFF185

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.250 SFLASH_PE_TE_DATA6

PE/TE Data

Address: 0x0FFFF186

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.251 SFLASH_PE_TE_DATA7

PE/TE Data

Address: 0x0FFFF187

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.252 SFLASH_PE_TE_DATA8

PE/TE Data

Address: 0x0FFFF188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.253 SFLASH_PE_TE_DATA9

PE/TE Data

Address: 0x0FFFF189

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.254 SFLASH_PE_TE_DATA10

PE/TE Data

Address: 0x0FFFF18A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.255 SFLASH_PE_TE_DATA11

PE/TE Data

Address: 0x0FFFF18B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.256 SFLASH_PE_TE_DATA12

PE/TE Data

Address: 0x0FFFF18C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.257 SFLASH_PE_TE_DATA13

PE/TE Data

Address: 0x0FFFF18D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.258 SFLASH_PE_TE_DATA14

PE/TE Data

Address: 0x0FFFF18E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.259 SFLASH_PE_TE_DATA15

PE/TE Data

Address: 0x0FFFF18F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.260 SFLASH_PE_TE_DATA16

PE/TE Data

Address: 0x0FFFF190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.261 SFLASH_PE_TE_DATA17

PE/TE Data

Address: 0x0FFFF191

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.262 SFLASH_PE_TE_DATA18

PE/TE Data

Address: 0x0FFFF192

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.263 SFLASH_PE_TE_DATA19

PE/TE Data

Address: 0x0FFFF193

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.264 SFLASH_PE_TE_DATA20

PE/TE Data

Address: 0x0FFFF194

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.265 SFLASH_PE_TE_DATA21

PE/TE Data

Address: 0x0FFFF195

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.266 SFLASH_PE_TE_DATA22

PE/TE Data

Address: 0x0FFFF196

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.267 SFLASH_PE_TE_DATA23

PE/TE Data

Address: 0x0FFFF197

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.268 SFLASH_PE_TE_DATA24

PE/TE Data

Address: 0x0FFFF198

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.269 SFLASH_PE_TE_DATA25

PE/TE Data

Address: 0x0FFFF199

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.270 SFLASH_PE_TE_DATA26

PE/TE Data

Address: 0x0FFFF19A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.271 SFLASH_PE_TE_DATA27

PE/TE Data

Address: 0x0FFFF19B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.272 SFLASH_PE_TE_DATA28

PE/TE Data

Address: 0x0FFFF19C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.273 SFLASH_PE_TE_DATA29

PE/TE Data

Address: 0x0FFFF19D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.274 SFLASH_PE_TE_DATA30

PE/TE Data

Address: 0x0FFFF19E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.275 SFLASH_PE_TE_DATA31

PE/TE Data

Address: 0x0FFFF19F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

28.1.276 SFLASH_PP

Preprogram Settings

Address: 0x0FFFF1A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

28.1.277 SFLASH_E

Erase Settings

Address: 0x0FFFF1A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

28.1.278 SFLASH_P

Program Settings

Address: 0x0FFFF1A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

28.1.279 SFLASH_EA_E

Erase All - Erase Settings

Address: 0x0FFFF1AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

28.1.280 SFLASH_EA_P

Erase All - Program Settings

Address: 0x0FFFF1B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

28.1.281 SFLASH_ES_E

Erase Sector - Erase Settings

Address: 0x0FFFF1B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

28.1.282 SFLASH_ES_P_EO

Erase Sector - Program EO Settings

Address: 0x0FFFF1B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

28.1.283 SFLASH_E_VCTAT

Bandgap Trim Register

Address: 0x0FFFF1BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW		RW			
HW Access	None	None	None		None			
Name	None	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

28.1.284 SFLASH_P_VCTAT

Bandgap Trim Register

Address: 0x0FFFF1BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW		RW			
HW Access	None	None	None		None			
Name	None	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

28.1.285 SFLASH_IMO_MAXF0

Max frequency for trim pair

Address: 0x0FFFF1C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

28.1.286 SFLASH_IMO_ABS0

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF1C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

28.1.287 SFLASH_IMO_TMPCO0

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF1C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

28.1.288 SFLASH_IMO_MAXF1

Max frequency for trim pair

Address: 0x0FFFF1C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

28.1.289 SFLASH_IMO_ABS1

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF1C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

28.1.290 SFLASH_IMO_TMPCO1

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF1C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

28.1.291 SFLASH_IMO_MAXF2

Max frequency for trim pair

Address: 0x0FFFF1C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

28.1.292 SFLASH_IMO_ABS2

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF1C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

28.1.293 SFLASH_IMO_TMPCO2

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF1C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

28.1.294 SFLASH_IMO_MAXF3

Max frequency for trim pair

Address: 0x0FFFF1C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

28.1.295 SFLASH_IMO_ABS3

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF1CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

28.1.296 SFLASH_IMO_TMPCO3

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF1CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

28.1.297 SFLASH_IMO_ABS4

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF1CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

28.1.298 SFLASH_IMO_TMPCO4

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF1CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

28.1.299 SFLASH_IMO_TRIM0

IMO Trim Register

Address: 0x0FFFF1D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.300 SFLASH_IMO_TRIM1

IMO Trim Register

Address: 0x0FFFF1D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.301 SFLASH_IMO_TRIM2

IMO Trim Register

Address: 0x0FFFF1D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.302 SFLASH_IMO_TRIM3

IMO Trim Register

Address: 0x0FFFF1D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.303 SFLASH_IMO_TRIM4

IMO Trim Register

Address: 0x0FFFF1D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.304 SFLASH_IMO_TRIM5

IMO Trim Register

Address: 0x0FFFF1D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.305 SFLASH_IMO_TRIM6

IMO Trim Register

Address: 0x0FFFF1D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.306 SFLASH_IMO_TRIM7

IMO Trim Register

Address: 0x0FFFF1D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.307 SFLASH_IMO_TRIM8

IMO Trim Register

Address: 0x0FFFF1D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.308 SFLASH_IMO_TRIM9

IMO Trim Register

Address: 0x0FFFF1D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.309 SFLASH_IMO_TRIM10

IMO Trim Register

Address: 0x0FFFF1DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.310 SFLASH_IMO_TRIM11

IMO Trim Register

Address: 0x0FFFF1DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.311 SFLASH_IMO_TRIM12

IMO Trim Register

Address: 0x0FFFF1DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.312 SFLASH_IMO_TRIM13

IMO Trim Register

Address: 0x0FFFF1DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.313 SFLASH_IMO_TRIM14

IMO Trim Register

Address: 0x0FFFF1DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.314 SFLASH_IMO_TRIM15

IMO Trim Register

Address: 0x0FFFF1DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.315 SFLASH_IMO_TRIM16

IMO Trim Register

Address: 0x0FFFF1E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.316 SFLASH_IMO_TRIM17

IMO Trim Register

Address: 0x0FFFF1E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.317 SFLASH_IMO_TRIM18

IMO Trim Register

Address: 0x0FFFF1E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.318 SFLASH_IMO_TRIM19

IMO Trim Register

Address: 0x0FFFF1E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.319 SFLASH_IMO_TRIM20

IMO Trim Register

Address: 0x0FFFF1E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.320 SFLASH_IMO_TRIM21

IMO Trim Register

Address: 0x0FFFF1E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.321 SFLASH_IMO_TRIM22

IMO Trim Register

Address: 0x0FFFF1E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.322 SFLASH_IMO_TRIM23

IMO Trim Register

Address: 0x0FFFF1E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.323 SFLASH_IMO_TRIM24

IMO Trim Register

Address: 0x0FFFF1E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.324 SFLASH_IMO_TRIM25

IMO Trim Register

Address: 0x0FFFF1E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.325 SFLASH_IMO_TRIM26

IMO Trim Register

Address: 0x0FFFF1EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.326 SFLASH_IMO_TRIM27

IMO Trim Register

Address: 0x0FFFF1EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.327 SFLASH_IMO_TRIM28

IMO Trim Register

Address: 0x0FFFF1EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.328 SFLASH_IMO_TRIM29

IMO Trim Register

Address: 0x0FFFF1ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.329 SFLASH_IMO_TRIM30

IMO Trim Register

Address: 0x0FFFF1EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.330 SFLASH_IMO_TRIM31

IMO Trim Register

Address: 0x0FFFF1EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.331 SFLASH_IMO_TRIM32

IMO Trim Register

Address: 0x0FFFF1F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.332 SFLASH_IMO_TRIM33

IMO Trim Register

Address: 0x0FFFF1F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.333 SFLASH_IMO_TRIM34

IMO Trim Register

Address: 0x0FFFF1F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.334 SFLASH_IMO_TRIM35

IMO Trim Register

Address: 0x0FFFF1F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.335 SFLASH_IMO_TRIM36

IMO Trim Register

Address: 0x0FFFF1F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.336 SFLASH_IMO_TRIM37

IMO Trim Register

Address: 0x0FFFF1F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.337 SFLASH_IMO_TRIM38

IMO Trim Register

Address: 0x0FFFF1F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.338 SFLASH_IMO_TRIM39

IMO Trim Register

Address: 0x0FFFF1F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.339 SFLASH_IMO_TRIM40

IMO Trim Register

Address: 0x0FFFF1F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.340 SFLASH_IMO_TRIM41

IMO Trim Register

Address: 0x0FFFF1F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.341 SFLASH_IMO_TRIM42

IMO Trim Register

Address: 0x0FFFF1FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.342 SFLASH_IMO_TRIM43

IMO Trim Register

Address: 0x0FFFF1FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.343 SFLASH_IMO_TRIM44

IMO Trim Register

Address: 0x0FFFF1FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.344 SFLASH_IMO_TRIM45

IMO Trim Register

Address: 0x0FFFF1FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

28.1.345 SFLASH_CHECKSUM

Boot Checksum

Address: 0x0FFFF1FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	CHECKSUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	CHECKSUM [15:8]							

Bits	Name	Description
15 : 0	CHECKSUM	Checksum of fixed data checked during boot. This checksum covers all of rows 1,2,3 of macro 0 + row 3 of macro 1 (except this checksum, and row 3 of macro 1 only if it exists). Default Value: X

28.1.346 SFLASH_ALT_PROT_ROW0

Per Page Write Protection

Address: 0x0FFFF400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.347 SFLASH_ALT_PROT_ROW1

Per Page Write Protection

Address: 0x0FFFF401

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.348 SFLASH_ALT_PROT_ROW2

Per Page Write Protection

Address: 0x0FFFF402

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.349 SFLASH_ALT_PROT_ROW3

Per Page Write Protection

Address: 0x0FFFF403

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.350 SFLASH_ALT_PROT_ROW4

Per Page Write Protection

Address: 0x0FFFF404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.351 SFLASH_ALT_PROT_ROW5

Per Page Write Protection

Address: 0x0FFFF405

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.352 SFLASH_ALT_PROT_ROW6

Per Page Write Protection

Address: 0x0FFFF406

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.353 SFLASH_ALT_PROT_ROW7

Per Page Write Protection

Address: 0x0FFFF407

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.354 SFLASH_ALT_PROT_ROW8

Per Page Write Protection

Address: 0x0FFFF408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.355 SFLASH_ALT_PROT_ROW9

Per Page Write Protection

Address: 0x0FFFF409

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.356 SFLASH_ALT_PROT_ROW10

Per Page Write Protection

Address: 0x0FFFF40A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.357 SFLASH_ALT_PROT_ROW11

Per Page Write Protection

Address: 0x0FFFF40B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.358 SFLASH_ALT_PROT_ROW12

Per Page Write Protection

Address: 0x0FFFF40C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.359 SFLASH_ALT_PROT_ROW13

Per Page Write Protection

Address: 0x0FFFF40D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.360 SFLASH_ALT_PROT_ROW14

Per Page Write Protection

Address: 0x0FFFF40E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.361 SFLASH_ALT_PROT_ROW15

Per Page Write Protection

Address: 0x0FFFF40F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.362 SFLASH_ALT_PROT_ROW16

Per Page Write Protection

Address: 0x0FFFF410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.363 SFLASH_ALT_PROT_ROW17

Per Page Write Protection

Address: 0x0FFFF411

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.364 SFLASH_ALT_PROT_ROW18

Per Page Write Protection

Address: 0x0FFFF412

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.365 SFLASH_ALT_PROT_ROW19

Per Page Write Protection

Address: 0x0FFFF413

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.366 SFLASH_ALT_PROT_ROW20

Per Page Write Protection

Address: 0x0FFFF414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.367 SFLASH_ALT_PROT_ROW21

Per Page Write Protection

Address: 0x0FFFF415

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.368 SFLASH_ALT_PROT_ROW22

Per Page Write Protection

Address: 0x0FFFF416

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.369 SFLASH_ALT_PROT_ROW23

Per Page Write Protection

Address: 0x0FFFF417

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.370 SFLASH_ALT_PROT_ROW24

Per Page Write Protection

Address: 0x0FFFF418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.371 SFLASH_ALT_PROT_ROW25

Per Page Write Protection

Address: 0x0FFFF419

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.372 SFLASH_ALT_PROT_ROW26

Per Page Write Protection

Address: 0x0FFFF41A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.373 SFLASH_ALT_PROT_ROW27

Per Page Write Protection

Address: 0x0FFFF41B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.374 SFLASH_ALT_PROT_ROW28

Per Page Write Protection

Address: 0x0FFFF41C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.375 SFLASH_ALT_PROT_ROW29

Per Page Write Protection

Address: 0x0FFFF41D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.376 SFLASH_ALT_PROT_ROW30

Per Page Write Protection

Address: 0x0FFFF41E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.377 SFLASH_ALT_PROT_ROW31

Per Page Write Protection

Address: 0x0FFFF41F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.378 SFLASH_ALT_PROT_ROW32

Per Page Write Protection

Address: 0x0FFFF420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.379 SFLASH_ALT_PROT_ROW33

Per Page Write Protection

Address: 0x0FFFF421

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.380 SFLASH_ALT_PROT_ROW34

Per Page Write Protection

Address: 0x0FFFF422

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.381 SFLASH_ALT_PROT_ROW35

Per Page Write Protection

Address: 0x0FFFF423

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.382 SFLASH_ALT_PROT_ROW36

Per Page Write Protection

Address: 0x0FFFF424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.383 SFLASH_ALT_PROT_ROW37

Per Page Write Protection

Address: 0x0FFFF425

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.384 SFLASH_ALT_PROT_ROW38

Per Page Write Protection

Address: 0x0FFFF426

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.385 SFLASH_ALT_PROT_ROW39

Per Page Write Protection

Address: 0x0FFFF427

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.386 SFLASH_ALT_PROT_ROW40

Per Page Write Protection

Address: 0x0FFFF428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.387 SFLASH_ALT_PROT_ROW41

Per Page Write Protection

Address: 0x0FFFF429

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.388 SFLASH_ALT_PROT_ROW42

Per Page Write Protection

Address: 0x0FFFF42A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.389 SFLASH_ALT_PROT_ROW43

Per Page Write Protection

Address: 0x0FFFF42B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.390 SFLASH_ALT_PROT_ROW44

Per Page Write Protection

Address: 0x0FFFF42C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.391 SFLASH_ALT_PROT_ROW45

Per Page Write Protection

Address: 0x0FFFF42D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.392 SFLASH_ALT_PROT_ROW46

Per Page Write Protection

Address: 0x0FFFF42E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.393 SFLASH_ALT_PROT_ROW47

Per Page Write Protection

Address: 0x0FFFF42F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.394 SFLASH_ALT_PROT_ROW48

Per Page Write Protection

Address: 0x0FFFF430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.395 SFLASH_ALT_PROT_ROW49

Per Page Write Protection

Address: 0x0FFFF431

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.396 SFLASH_ALT_PROT_ROW50

Per Page Write Protection

Address: 0x0FFFF432

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.397 SFLASH_ALT_PROT_ROW51

Per Page Write Protection

Address: 0x0FFFF433

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.398 SFLASH_ALT_PROT_ROW52

Per Page Write Protection

Address: 0x0FFFF434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.399 SFLASH_ALT_PROT_ROW53

Per Page Write Protection

Address: 0x0FFFF435

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.400 SFLASH_ALT_PROT_ROW54

Per Page Write Protection

Address: 0x0FFFF436

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.401 SFLASH_ALT_PROT_ROW55

Per Page Write Protection

Address: 0x0FFFF437

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.402 SFLASH_ALT_PROT_ROW56

Per Page Write Protection

Address: 0x0FFFF438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.403 SFLASH_ALT_PROT_ROW57

Per Page Write Protection

Address: 0x0FFFF439

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.404 SFLASH_ALT_PROT_ROW58

Per Page Write Protection

Address: 0x0FFFF43A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.405 SFLASH_ALT_PROT_ROW59

Per Page Write Protection

Address: 0x0FFFF43B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.406 SFLASH_ALT_PROT_ROW60

Per Page Write Protection

Address: 0x0FFFF43C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.407 SFLASH_ALT_PROT_ROW61

Per Page Write Protection

Address: 0x0FFFF43D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.408 SFLASH_ALT_PROT_ROW62

Per Page Write Protection

Address: 0x0FFFF43E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.409 SFLASH_ALT_PROT_ROW63

Per Page Write Protection

Address: 0x0FFFF43F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.410 SFLASH_ALT_PROT_ROW64

Per Page Write Protection

Address: 0x0FFFF440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.411 SFLASH_ALT_PROT_ROW65

Per Page Write Protection

Address: 0x0FFFF441

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.412 SFLASH_ALT_PROT_ROW66

Per Page Write Protection

Address: 0x0FFFF442

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.413 SFLASH_ALT_PROT_ROW67

Per Page Write Protection

Address: 0x0FFFF443

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.414 SFLASH_ALT_PROT_ROW68

Per Page Write Protection

Address: 0x0FFFF444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.415 SFLASH_ALT_PROT_ROW69

Per Page Write Protection

Address: 0x0FFFF445

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.416 SFLASH_ALT_PROT_ROW70

Per Page Write Protection

Address: 0x0FFFF446

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.417 SFLASH_ALT_PROT_ROW71

Per Page Write Protection

Address: 0x0FFFF447

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.418 SFLASH_ALT_PROT_ROW72

Per Page Write Protection

Address: 0x0FFFF448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.419 SFLASH_ALT_PROT_ROW73

Per Page Write Protection

Address: 0x0FFFF449

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.420 SFLASH_ALT_PROT_ROW74

Per Page Write Protection

Address: 0x0FFFF44A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.421 SFLASH_ALT_PROT_ROW75

Per Page Write Protection

Address: 0x0FFFF44B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.422 SFLASH_ALT_PROT_ROW76

Per Page Write Protection

Address: 0x0FFFF44C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.423 SFLASH_ALT_PROT_ROW77

Per Page Write Protection

Address: 0x0FFFF44D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.424 SFLASH_ALT_PROT_ROW78

Per Page Write Protection

Address: 0x0FFFF44E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.425 SFLASH_ALT_PROT_ROW79

Per Page Write Protection

Address: 0x0FFFF44F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.426 SFLASH_ALT_PROT_ROW80

Per Page Write Protection

Address: 0x0FFFF450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.427 SFLASH_ALT_PROT_ROW81

Per Page Write Protection

Address: 0x0FFFF451

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.428 SFLASH_ALT_PROT_ROW82

Per Page Write Protection

Address: 0x0FFFF452

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.429 SFLASH_ALT_PROT_ROW83

Per Page Write Protection

Address: 0x0FFFF453

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.430 SFLASH_ALT_PROT_ROW84

Per Page Write Protection

Address: 0x0FFFF454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.431 SFLASH_ALT_PROT_ROW85

Per Page Write Protection

Address: 0x0FFFF455

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.432 SFLASH_ALT_PROT_ROW86

Per Page Write Protection

Address: 0x0FFFF456

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.433 SFLASH_ALT_PROT_ROW87

Per Page Write Protection

Address: 0x0FFFF457

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.434 SFLASH_ALT_PROT_ROW88

Per Page Write Protection

Address: 0x0FFFF458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.435 SFLASH_ALT_PROT_ROW89

Per Page Write Protection

Address: 0x0FFFF459

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.436 SFLASH_ALT_PROT_ROW90

Per Page Write Protection

Address: 0x0FFFF45A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.437 SFLASH_ALT_PROT_ROW91

Per Page Write Protection

Address: 0x0FFFF45B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.438 SFLASH_ALT_PROT_ROW92

Per Page Write Protection

Address: 0x0FFFF45C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.439 SFLASH_ALT_PROT_ROW93

Per Page Write Protection

Address: 0x0FFFF45D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.440 SFLASH_ALT_PROT_ROW94

Per Page Write Protection

Address: 0x0FFFF45E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.441 SFLASH_ALT_PROT_ROW95

Per Page Write Protection

Address: 0x0FFFF45F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.442 SFLASH_ALT_PROT_ROW96

Per Page Write Protection

Address: 0x0FFFF460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.443 SFLASH_ALT_PROT_ROW97

Per Page Write Protection

Address: 0x0FFFF461

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.444 SFLASH_ALT_PROT_ROW98

Per Page Write Protection

Address: 0x0FFFF462

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.445 SFLASH_ALT_PROT_ROW99

Per Page Write Protection

Address: 0x0FFFF463

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.446 SFLASH_ALT_PROT_ROW100

Per Page Write Protection

Address: 0x0FFFF464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.447 SFLASH_ALT_PROT_ROW101

Per Page Write Protection

Address: 0x0FFFF465

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.448 SFLASH_ALT_PROT_ROW102

Per Page Write Protection

Address: 0x0FFFF466

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.449 SFLASH_ALT_PROT_ROW103

Per Page Write Protection

Address: 0x0FFFF467

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.450 SFLASH_ALT_PROT_ROW104

Per Page Write Protection

Address: 0x0FFFF468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.451 SFLASH_ALT_PROT_ROW105

Per Page Write Protection

Address: 0x0FFFF469

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.452 SFLASH_ALT_PROT_ROW106

Per Page Write Protection

Address: 0x0FFFF46A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.453 SFLASH_ALT_PROT_ROW107

Per Page Write Protection

Address: 0x0FFFF46B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.454 SFLASH_ALT_PROT_ROW108

Per Page Write Protection

Address: 0x0FFFF46C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.455 SFLASH_ALT_PROT_ROW109

Per Page Write Protection

Address: 0x0FFFF46D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.456 SFLASH_ALT_PROT_ROW110

Per Page Write Protection

Address: 0x0FFFF46E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.457 SFLASH_ALT_PROT_ROW111

Per Page Write Protection

Address: 0x0FFFF46F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.458 SFLASH_ALT_PROT_ROW112

Per Page Write Protection

Address: 0x0FFFF470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.459 SFLASH_ALT_PROT_ROW113

Per Page Write Protection

Address: 0x0FFFF471

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.460 SFLASH_ALT_PROT_ROW114

Per Page Write Protection

Address: 0x0FFFF472

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.461 SFLASH_ALT_PROT_ROW115

Per Page Write Protection

Address: 0x0FFFF473

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.462 SFLASH_ALT_PROT_ROW116

Per Page Write Protection

Address: 0x0FFFF474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.463 SFLASH_ALT_PROT_ROW117

Per Page Write Protection

Address: 0x0FFFF475

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.464 SFLASH_ALT_PROT_ROW118

Per Page Write Protection

Address: 0x0FFFF476

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.465 SFLASH_ALT_PROT_ROW119

Per Page Write Protection

Address: 0x0FFFF477

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.466 SFLASH_ALT_PROT_ROW120

Per Page Write Protection

Address: 0x0FFFF478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.467 SFLASH_ALT_PROT_ROW121

Per Page Write Protection

Address: 0x0FFFF479

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.468 SFLASH_ALT_PROT_ROW122

Per Page Write Protection

Address: 0x0FFFF47A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.469 SFLASH_ALT_PROT_ROW123

Per Page Write Protection

Address: 0x0FFFF47B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.470 SFLASH_ALT_PROT_ROW124

Per Page Write Protection

Address: 0x0FFFF47C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.471 SFLASH_ALT_PROT_ROW125

Per Page Write Protection

Address: 0x0FFFF47D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.472 SFLASH_ALT_PROT_ROW126

Per Page Write Protection

Address: 0x0FFFF47E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.473 SFLASH_ALT_PROT_ROW127

Per Page Write Protection

Address: 0x0FFFF47F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.474 SFLASH_ALT_PROT_ROW128

Per Page Write Protection

Address: 0x0FFFF480

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.475 SFLASH_ALT_PROT_ROW129

Per Page Write Protection

Address: 0x0FFFF481

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.476 SFLASH_ALT_PROT_ROW130

Per Page Write Protection

Address: 0x0FFFF482

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.477 SFLASH_ALT_PROT_ROW131

Per Page Write Protection

Address: 0x0FFFF483

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.478 SFLASH_ALT_PROT_ROW132

Per Page Write Protection

Address: 0x0FFFF484

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.479 SFLASH_ALT_PROT_ROW133

Per Page Write Protection

Address: 0x0FFFF485

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.480 SFLASH_ALT_PROT_ROW134

Per Page Write Protection

Address: 0x0FFFF486

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.481 SFLASH_ALT_PROT_ROW135

Per Page Write Protection

Address: 0x0FFFF487

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.482 SFLASH_ALT_PROT_ROW136

Per Page Write Protection

Address: 0x0FFFF488

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.483 SFLASH_ALT_PROT_ROW137

Per Page Write Protection

Address: 0x0FFFF489

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.484 SFLASH_ALT_PROT_ROW138

Per Page Write Protection

Address: 0x0FFFF48A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.485 SFLASH_ALT_PROT_ROW139

Per Page Write Protection

Address: 0x0FFFF48B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.486 SFLASH_ALT_PROT_ROW140

Per Page Write Protection

Address: 0x0FFFF48C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.487 SFLASH_ALT_PROT_ROW141

Per Page Write Protection

Address: 0x0FFFF48D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.488 SFLASH_ALT_PROT_ROW142

Per Page Write Protection

Address: 0x0FFFF48E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.489 SFLASH_ALT_PROT_ROW143

Per Page Write Protection

Address: 0x0FFFF48F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.490 SFLASH_ALT_PROT_ROW144

Per Page Write Protection

Address: 0x0FFFF490

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.491 SFLASH_ALT_PROT_ROW145

Per Page Write Protection

Address: 0x0FFFF491

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.492 SFLASH_ALT_PROT_ROW146

Per Page Write Protection

Address: 0x0FFFF492

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.493 SFLASH_ALT_PROT_ROW147

Per Page Write Protection

Address: 0x0FFFF493

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.494 SFLASH_ALT_PROT_ROW148

Per Page Write Protection

Address: 0x0FFFF494

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.495 SFLASH_ALT_PROT_ROW149

Per Page Write Protection

Address: 0x0FFFF495

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.496 SFLASH_ALT_PROT_ROW150

Per Page Write Protection

Address: 0x0FFFF496

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.497 SFLASH_ALT_PROT_ROW151

Per Page Write Protection

Address: 0x0FFFF497

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.498 SFLASH_ALT_PROT_ROW152

Per Page Write Protection

Address: 0x0FFFF498

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.499 SFLASH_ALT_PROT_ROW153

Per Page Write Protection

Address: 0x0FFFF499

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.500 SFLASH_ALT_PROT_ROW154

Per Page Write Protection

Address: 0x0FFFF49A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.501 SFLASH_ALT_PROT_ROW155

Per Page Write Protection

Address: 0x0FFFF49B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.502 SFLASH_ALT_PROT_ROW156

Per Page Write Protection

Address: 0x0FFFF49C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.503 SFLASH_ALT_PROT_ROW157

Per Page Write Protection

Address: 0x0FFFF49D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.504 SFLASH_ALT_PROT_ROW158

Per Page Write Protection

Address: 0x0FFFF49E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.505 SFLASH_ALT_PROT_ROW159

Per Page Write Protection

Address: 0x0FFFF49F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.506 SFLASH_ALT_PROT_ROW160

Per Page Write Protection

Address: 0x0FFFF4A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.507 SFLASH_ALT_PROT_ROW161

Per Page Write Protection

Address: 0x0FFFF4A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.508 SFLASH_ALT_PROT_ROW162

Per Page Write Protection

Address: 0x0FFFF4A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.509 SFLASH_ALT_PROT_ROW163

Per Page Write Protection

Address: 0x0FFFF4A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.510 SFLASH_ALT_PROT_ROW164

Per Page Write Protection

Address: 0x0FFFF4A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.511 SFLASH_ALT_PROT_ROW165

Per Page Write Protection

Address: 0x0FFFF4A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.512 SFLASH_ALT_PROT_ROW166

Per Page Write Protection

Address: 0x0FFFF4A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.513 SFLASH_ALT_PROT_ROW167

Per Page Write Protection

Address: 0x0FFFF4A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.514 SFLASH_ALT_PROT_ROW168

Per Page Write Protection

Address: 0x0FFFF4A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.515 SFLASH_ALT_PROT_ROW169

Per Page Write Protection

Address: 0x0FFFF4A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.516 SFLASH_ALT_PROT_ROW170

Per Page Write Protection

Address: 0x0FFFF4AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.517 SFLASH_ALT_PROT_ROW171

Per Page Write Protection

Address: 0x0FFFF4AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.518 SFLASH_ALT_PROT_ROW172

Per Page Write Protection

Address: 0x0FFFF4AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.519 SFLASH_ALT_PROT_ROW173

Per Page Write Protection

Address: 0x0FFFF4AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.520 SFLASH_ALT_PROT_ROW174

Per Page Write Protection

Address: 0x0FFFF4AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.521 SFLASH_ALT_PROT_ROW175

Per Page Write Protection

Address: 0x0FFFF4AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.522 SFLASH_ALT_PROT_ROW176

Per Page Write Protection

Address: 0x0FFFF4B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.523 SFLASH_ALT_PROT_ROW177

Per Page Write Protection

Address: 0x0FFFF4B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.524 SFLASH_ALT_PROT_ROW178

Per Page Write Protection

Address: 0x0FFFF4B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.525 SFLASH_ALT_PROT_ROW179

Per Page Write Protection

Address: 0x0FFFF4B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.526 SFLASH_ALT_PROT_ROW180

Per Page Write Protection

Address: 0x0FFFF4B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.527 SFLASH_ALT_PROT_ROW181

Per Page Write Protection

Address: 0x0FFFF4B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.528 SFLASH_ALT_PROT_ROW182

Per Page Write Protection

Address: 0x0FFFF4B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.529 SFLASH_ALT_PROT_ROW183

Per Page Write Protection

Address: 0x0FFFF4B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.530 SFLASH_ALT_PROT_ROW184

Per Page Write Protection

Address: 0x0FFFF4B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.531 SFLASH_ALT_PROT_ROW185

Per Page Write Protection

Address: 0x0FFFF4B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.532 SFLASH_ALT_PROT_ROW186

Per Page Write Protection

Address: 0x0FFFF4BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.533 SFLASH_ALT_PROT_ROW187

Per Page Write Protection

Address: 0x0FFFF4BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.534 SFLASH_ALT_PROT_ROW188

Per Page Write Protection

Address: 0x0FFFF4BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.535 SFLASH_ALT_PROT_ROW189

Per Page Write Protection

Address: 0x0FFFF4BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.536 SFLASH_ALT_PROT_ROW190

Per Page Write Protection

Address: 0x0FFFF4BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.537 SFLASH_ALT_PROT_ROW191

Per Page Write Protection

Address: 0x0FFFF4BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.538 SFLASH_ALT_PROT_ROW192

Per Page Write Protection

Address: 0x0FFFF4C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.539 SFLASH_ALT_PROT_ROW193

Per Page Write Protection

Address: 0x0FFFF4C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.540 SFLASH_ALT_PROT_ROW194

Per Page Write Protection

Address: 0x0FFFF4C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.541 SFLASH_ALT_PROT_ROW195

Per Page Write Protection

Address: 0x0FFFF4C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.542 SFLASH_ALT_PROT_ROW196

Per Page Write Protection

Address: 0x0FFFF4C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.543 SFLASH_ALT_PROT_ROW197

Per Page Write Protection

Address: 0x0FFFF4C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.544 SFLASH_ALT_PROT_ROW198

Per Page Write Protection

Address: 0x0FFFF4C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.545 SFLASH_ALT_PROT_ROW199

Per Page Write Protection

Address: 0x0FFFF4C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.546 SFLASH_ALT_PROT_ROW200

Per Page Write Protection

Address: 0x0FFFF4C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.547 SFLASH_ALT_PROT_ROW201

Per Page Write Protection

Address: 0x0FFFF4C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.548 SFLASH_ALT_PROT_ROW202

Per Page Write Protection

Address: 0x0FFFF4CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.549 SFLASH_ALT_PROT_ROW203

Per Page Write Protection

Address: 0x0FFFF4CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.550 SFLASH_ALT_PROT_ROW204

Per Page Write Protection

Address: 0x0FFFF4CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.551 SFLASH_ALT_PROT_ROW205

Per Page Write Protection

Address: 0x0FFFF4CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.552 SFLASH_ALT_PROT_ROW206

Per Page Write Protection

Address: 0x0FFFF4CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.553 SFLASH_ALT_PROT_ROW207

Per Page Write Protection

Address: 0x0FFFF4CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.554 SFLASH_ALT_PROT_ROW208

Per Page Write Protection

Address: 0x0FFFF4D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.555 SFLASH_ALT_PROT_ROW209

Per Page Write Protection

Address: 0x0FFFF4D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.556 SFLASH_ALT_PROT_ROW210

Per Page Write Protection

Address: 0x0FFFF4D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.557 SFLASH_ALT_PROT_ROW211

Per Page Write Protection

Address: 0x0FFFF4D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.558 SFLASH_ALT_PROT_ROW212

Per Page Write Protection

Address: 0x0FFFF4D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.559 SFLASH_ALT_PROT_ROW213

Per Page Write Protection

Address: 0x0FFFF4D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.560 SFLASH_ALT_PROT_ROW214

Per Page Write Protection

Address: 0x0FFFF4D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.561 SFLASH_ALT_PROT_ROW215

Per Page Write Protection

Address: 0x0FFFF4D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.562 SFLASH_ALT_PROT_ROW216

Per Page Write Protection

Address: 0x0FFFF4D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.563 SFLASH_ALT_PROT_ROW217

Per Page Write Protection

Address: 0x0FFFF4D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.564 SFLASH_ALT_PROT_ROW218

Per Page Write Protection

Address: 0x0FFFF4DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.565 SFLASH_ALT_PROT_ROW219

Per Page Write Protection

Address: 0x0FFFF4DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.566 SFLASH_ALT_PROT_ROW220

Per Page Write Protection

Address: 0x0FFFF4DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.567 SFLASH_ALT_PROT_ROW221

Per Page Write Protection

Address: 0x0FFFF4DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.568 SFLASH_ALT_PROT_ROW222

Per Page Write Protection

Address: 0x0FFFF4DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.569 SFLASH_ALT_PROT_ROW223

Per Page Write Protection

Address: 0x0FFFF4DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.570 SFLASH_ALT_PROT_ROW224

Per Page Write Protection

Address: 0x0FFFF4E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.571 SFLASH_ALT_PROT_ROW225

Per Page Write Protection

Address: 0x0FFFF4E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.572 SFLASH_ALT_PROT_ROW226

Per Page Write Protection

Address: 0x0FFFF4E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.573 SFLASH_ALT_PROT_ROW227

Per Page Write Protection

Address: 0x0FFFF4E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.574 SFLASH_ALT_PROT_ROW228

Per Page Write Protection

Address: 0x0FFFF4E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.575 SFLASH_ALT_PROT_ROW229

Per Page Write Protection

Address: 0x0FFFF4E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.576 SFLASH_ALT_PROT_ROW230

Per Page Write Protection

Address: 0x0FFFF4E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.577 SFLASH_ALT_PROT_ROW231

Per Page Write Protection

Address: 0x0FFFF4E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.578 SFLASH_ALT_PROT_ROW232

Per Page Write Protection

Address: 0x0FFFF4E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.579 SFLASH_ALT_PROT_ROW233

Per Page Write Protection

Address: 0x0FFFF4E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.580 SFLASH_ALT_PROT_ROW234

Per Page Write Protection

Address: 0x0FFFF4EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.581 SFLASH_ALT_PROT_ROW235

Per Page Write Protection

Address: 0x0FFFF4EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.582 SFLASH_ALT_PROT_ROW236

Per Page Write Protection

Address: 0x0FFFF4EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.583 SFLASH_ALT_PROT_ROW237

Per Page Write Protection

Address: 0x0FFFF4ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.584 SFLASH_ALT_PROT_ROW238

Per Page Write Protection

Address: 0x0FFFF4EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.585 SFLASH_ALT_PROT_ROW239

Per Page Write Protection

Address: 0x0FFFF4EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.586 SFLASH_ALT_PROT_ROW240

Per Page Write Protection

Address: 0x0FFFF4F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.587 SFLASH_ALT_PROT_ROW241

Per Page Write Protection

Address: 0x0FFFF4F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.588 SFLASH_ALT_PROT_ROW242

Per Page Write Protection

Address: 0x0FFFF4F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.589 SFLASH_ALT_PROT_ROW243

Per Page Write Protection

Address: 0x0FFFF4F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.590 SFLASH_ALT_PROT_ROW244

Per Page Write Protection

Address: 0x0FFFF4F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.591 SFLASH_ALT_PROT_ROW245

Per Page Write Protection

Address: 0x0FFFF4F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.592 SFLASH_ALT_PROT_ROW246

Per Page Write Protection

Address: 0x0FFFF4F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.593 SFLASH_ALT_PROT_ROW247

Per Page Write Protection

Address: 0x0FFFF4F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.594 SFLASH_ALT_PROT_ROW248

Per Page Write Protection

Address: 0x0FFFF4F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.595 SFLASH_ALT_PROT_ROW249

Per Page Write Protection

Address: 0x0FFFF4F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.596 SFLASH_ALT_PROT_ROW250

Per Page Write Protection

Address: 0x0FFFF4FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.597 SFLASH_ALT_PROT_ROW251

Per Page Write Protection

Address: 0x0FFFF4FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.598 SFLASH_ALT_PROT_ROW252

Per Page Write Protection

Address: 0x0FFFF4FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.599 SFLASH_ALT_PROT_ROW253

Per Page Write Protection

Address: 0x0FFFF4FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.600 SFLASH_ALT_PROT_ROW254

Per Page Write Protection

Address: 0x0FFFF4FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.601 SFLASH_ALT_PROT_ROW255

Per Page Write Protection

Address: 0x0FFFF4FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

28.1.602 SFLASH_ALT_PP

Preprogram Settings

Address: 0x0FFFF5A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

28.1.603 SFLASH_ALT_E

Erase Settings

Address: 0x0FFFF5A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

28.1.604 SFLASH_ALT_P

Program Settings

Address: 0x0FFFF5A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

28.1.605 SFLASH_ALT_EA_E

Erase All - Erase Settings

Address: 0x0FFFF5AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

28.1.606 SFLASH_ALT_EA_P

Erase All - Program Settings

Address: 0x0FFFF5B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

28.1.607 SFLASH_ALT_ES_E

Erase Sector - Erase Settings

Address: 0x0FFFF5B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

28.1.608 SFLASH_ALT_ES_P_EO

Erase Sector - Program EO Settings

Address: 0x0FFFF5B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

28.1.609 SFLASH_ALT_E_VCTAT

Bandgap Trim Register

Address: 0x0FFFF5BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW		RW			
HW Access	None	None	None		None			
Name	None	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

28.1.610 SFLASH_ALT_P_VCTAT

Bandgap Trim Register

Address: 0x0FFFF5BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW		RW			
HW Access	None	None	None		None			
Name	None	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

29 SPC Interface (SPCIF) Registers

This section discusses the SPCIF registers. It lists all the registers in mapping tables, in address order.

29.1 Register Details

Register Name	Address
SPCIF_GEOMETRY	0x40110000
SPCIF_INTR	0x401107F0
SPCIF_INTR_SET	0x401107F4
SPCIF_INTR_MASK	0x401107F8
SPCIF_INTR_MASKED	0x401107FC

29.1.1 SPCIF_GEOMETRY

Flash/NVL geometry information

Address: 0x40110000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	FLASH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	FLASH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R		R		R			
HW Access	W		W		W			
Name	FLASH_ROW [23:22]		NUM_FLASH [21:20]		SFLASH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	R						
HW Access	None	W						
Name	DE_CPD_LP	NVL [30:24]						

Bits	Name	Description
31	DE_CPD_LP	0': SRAM busy wait loop has not been copied. '1': Busy wait loop has been written into SRAM. Default Value: 0
30 : 24	NVL	NVLatch size in Byte multiples (chip dependent): "0": 0 Bytes "1": 1 Byte ... "127": 127 Bytes Default Value: Undefined

29.1.1 SPCIF_GEOMETRY (continued)

23 : 22	FLASH_ROW	Page size in 64 Byte multiples (chip dependent): "0": 64 byte "1": 128 byte "2": 192 byte "3": 256 byte The page size is used to detemine the number of Bytes in a page for Flash page based operations (e.g. PGM_PAGE). Note: the field name FLASH_ROW is misleading, as this field specifies the number of Bytes in a page, rather than the number of Bytes in a row. In a single plane flash macro architecture, a page consists of a single row. However, in a multi plane flash macro architecture, a page consists of multiple rows from different planes. Default Value: Undefined
21 : 20	NUM_FLASH	Number of flash macros (chip dependent): "0": 1 flash macro "1": 2 flash macros "2": 3 flash macros "3": 4 flash macros Default Value: Undefined
19 : 16	SFLASH	Supervisory flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the supervisory flash capacity of all flash macros together: "0": 256 Bytes. "1": 2*256 Bytes. ... "15": 16*256 Bytes. Default Value: Undefined
15 : 0	FLASH	Regular flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the flash capacity of all flash macros together: "0": 256 Bytes. "1": 2*256 Bytes. ... "65535": 65536*256 Bytes. Default Value: Undefined

29.1.2 SPCIF_INTR

SPCIF interrupt request register

Address: 0x401107F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Timer counter value reaches "0". Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit. Default Value: 0

29.1.3 SPCIF_INTR_SET

SPCIF interrupt set request register

Address: 0x401107F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Write INTR_SET field with '1' to set corresponding INTR field. Default Value: 0

29.1.4 SPCIF_INTR_MASK

SPCIF interrupt mask register

Address: 0x401107F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Mask for corresponding field in INTR register. Default Value: 0

29.1.5 SPCIF_INTR_MASKED

SPCIF interrupt masked request register

Address: 0x401107FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Logical and of corresponding request and mask fields. Default Value: 0

30 TCPWM Registers

This section discusses the TCPWM registers. It lists all the registers in mapping tables, in address order.

30.1 Register Details

Register Name	Address
TCPWM_CTRL	0x40200000
TCPWM_CMD	0x40200008
TCPWM_INTR_CAUSE	0x4020000C

30.1.1 TCPWM_CTRL

TCPWM control register 0.

Address: 0x40200000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COUNTER_ENABLED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	COUNTER_ENABLED	Counter enables for counters 0 up to CNT_NR-1. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_CTRL0, TR_CTRL1, and TR_CTRL2 register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_overflow", "tr_underflow" and "tr_compare_match"). - the counter's line outputs ("line_out" and "line_compl_out"). Default Value: 0

30.1.2 TCPWM_CMD

TCPWM command register.

Address: 0x40200008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_CAPTURE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_RELOAD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_STOP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_START [31:24]							

Bits	Name	Description
31 : 24	COUNTER_START	Counters SW start trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
23 : 16	COUNTER_STOP	Counters SW stop trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
15 : 8	COUNTER_RELOAD	Counters SW reload trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
7 : 0	COUNTER_CAPTURE	Counters SW capture trigger. When written with '1', a capture trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.COUNTER_ENABLED, the field is immediately set to '0'. Default Value: 0

30.1.3 TCPWM_INTR_CAUSE

TCPWM Counter interrupt cause register.

Address: 0x4020000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	COUNTER_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	COUNTER_INT	Counters interrupt signal active. If the counter is disabled through CTRL.COUNTER_ENABLED, the associated interrupt field is immediately set to '0'. Default Value: 0

31 TR_GROUP Registers

This section discusses the TR_GROUP registers. It lists all the registers in mapping tables, in address order.

31.1 Register Details

Register Name	Address
PERI_TR_GROUP_TR_OUT_CTL1	0x40012000
PERI_TR_GROUP_TR_OUT_CTL1	0x40012004
PERI_TR_GROUP_TR_OUT_CTL2	0x40012008
PERI_TR_GROUP_TR_OUT_CTL3	0x4001200C
PERI_TR_GROUP_TR_OUT_CTL4	0x40012010
PERI_TR_GROUP_TR_OUT_CTL5	0x40012014
PERI_TR_GROUP_TR_OUT_CTL6	0x40012018
PERI_TR_GROUP_TR_OUT_CTL7	0x4001201C

31.1.1 PERI_TR_GROUP_TR_OUT_CTL0

Trigger control register

Address: 0x40012000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

31.1.2 PERI_TR_GROUP_TR_OUT_CTL1

Trigger control register

Address: 0x40012004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

31.1.3 PERI_TR_GROUP_TR_OUT_CTL2

Trigger control register

Address: 0x40012008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

31.1.4 PERI_TR_GROUP_TR_OUT_CTL3

Trigger control register

Address: 0x4001200C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

31.1.5 PERI_TR_GROUP_TR_OUT_CTL4

Trigger control register

Address: 0x40012010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

31.1.6 PERI_TR_GROUP_TR_OUT_CTL5

Trigger control register

Address: 0x40012014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

31.1.7 PERI_TR_GROUP_TR_OUT_CTL6

Trigger control register

Address: 0x40012018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

31.1.8 PERI_TR_GROUP_TR_OUT_CTL7

Trigger control register

Address: 0x4001201C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

32 Test (TST) Registers

This section discusses the TST registers. It lists all the registers in mapping tables, in address order.

32.1 Register Details

Register Name	Address
TST_MODE	0x40030014

32.1.1 TST_MODE

Test Mode Control Register

Address: 0x40030014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	None	
HW Access	None					RW	None	
Name	None [7:3]					SWD_CONNECTED	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	R	None					
HW Access	R	RW	None					
Name	TEST_MODE	POR_BYPASS	None [29:24]					

Bits	Name	Description
31	TEST_MODE	0: Normal operation mode 1: Test mode (any test mode) Setting this bit will prevent BootROM from yielding execution to Flash image. Default Value: 0
30	POR_BYPASS	This bit is set during POR bypass mode. When this bit is set, the BootROM will not yield execution to the FLASH image (same function as setting TEST_MODE bit below). Default Value: 0
2	SWD_CONNECTED	0: SWD not active 1: SWD activated (Line Reset & Connect sequence passed) Default Value: 0

33 Watch Crystal Oscillator (WCO) Registers

This section discusses the WRK8 registers. It lists all the registers in mapping tables, in address order.

33.1 Register Details

Register Name	Address
WCO_CONFIG	0x40220000
WCO_DPLL	0x40220008
WCO_TRIM	0x40220F00

33.1.1 WCO_CONFIG

WCO Configuration Register

Address: 0x40220000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					EXT_INPUT_EN	LPM_AUTO	LPM_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ENBUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	IP_ENABLE	DPLL_ENABLE	None [29:24]					

Bits	Name	Description
31	IP_ENABLE	Master enable for IP - disables both WCO and DPLL Default Value: 0
30	DPLL_ENABLE	Enable DPLL operation. The Oscillator is specified to be stable after 0.28 sec (max) thus the DPLL should be asserted no sooner than 0.28 sec after IP_ENABLE is set. Default Value: 0
23 : 16	ENBUS	Test Mode Control bits enbus[7] - N/A enbus[6] - 1=enable both primary Beta Multipliers enbus[5] - N/A enbus[4] - N/A enbus[3] - Load Resistor Control enbus[2] - Load Resistor Control enbus[1] - Load Resistor Control enbus[0] - Load Resistor Control Default Value: 71
2	EXT_INPUT_EN	Disables the load resistor and allows external clock input for pad_xin Default Value: 0

33.1.1 WCO_CONFIG (continued)

1	LPM_AUTO	Automatically control low power mode (only relevant when LPM_EN=0): 0: Do not enter low power mode (LPM) in DeepSleep 1: Enter low power mode (LPM) in DeepSleep. The logic monitors !act_power_en to determine the device has entered DeepSleep. Default Value: 1
0	LPM_EN	Force block into Low Power Mode: 0: Do not force low power mode (LPM) on 1: Force low power mode (LPM) on Default Value: 0

33.1.2 WCO_DPLL

WCO DPLL Register

Address: 0x40220008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DPLL_MULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					DPLL_MULT [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DPLL_LF_LIMIT [23:22]		DPLL_LF_PGAIN [21:19]			DPLL_LF_IGAIN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW					
HW Access	None		R					
Name	None [31:30]		DPLL_LF_LIMIT [29:24]					

Bits	Name	Description
29 : 22	DPLL_LF_LIMIT	Maximum IMO offset allowed (used to prevent DPLL dynamics from selecting an IMO frequency that the logic cannot support) Default Value: 255
21 : 19	DPLL_LF_PGAIN	DPLL Loop Filter Proportionial Gain Setting 0x0 - 0.0625 0x1 - 0.125 0x2 - 0.25 0x3 - 0.5 0x4 - 1.0 0x5 - 2.0 0x6 - 4.0 0x7 - 8.0 Default Value: 0

33.1.2 WCO_DPLL (continued)

18 : 16	DPLL_LF_IGAIN	DPLL Loop Filter Integral Gain Setting 0x0 - 0.0625 0x1 - 0.125 0x2 - 0.25 0x3 - 0.5 0x4 - 1.0 0x5 - 2.0 0x6 - 4.0 0x7 - 8.0 Default Value: 0
10 : 0	DPLL_MULT	Multiplier to determine IMO frequency in multiples of the WCO frequency Fimo = DPLL_MULT * Fwco Default Value: 0

33.1.3 WCO_TRIM

WCO Trim Register

Address: 0x40220F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		None	RW		
HW Access	None		R		None	R		
Name	None [7:6]		LPM_GM [5:4]		None	XGM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW		
HW Access	None		R		None	R		
Name	None [15:14]		LPM_GM_FOR_LPM_AUTO [13:12]		None	XGM_FOR_LPM_AUTO [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 12	LPM_GM_FOR_LPM_AUTO	GM setting for LPM (bandwidth = DC/ms) - Used when WCO.LPM_AUTO=1 and in DeepSleep mode Default Value: 2
10 : 8	XGM_FOR_LPM_AUTO	Amplifier GM setting - Used when WCO.LPM_AUTO=1 and in DeepSleep mode 0x0 - 3370 nA 0x1 - 2620 nA 0x2 - 2250 nA 0x3 - 1500 nA 0x4 - 1870 nA 0x5 - 1120 nA 0x6 - 750 nA 0x7 - 0 nA Default Value: 2
5 : 4	LPM_GM	GM setting for LPM (bandwidth = DC/ms) - Used when WCO.LPM_AUTO=0 or when LPM_AUTO=1 and not in DeepSleep mode. Default Value: 1

33.1.3 WCO_TRIM (continued)

2 : 0	XGM	Amplifier GM setting - Used when WCO.LPM_AUTO=0 or when LPM_AUTO=1 and not in Deep-Sleep mode. 0x0 - 3370 nA 0x1 - 2620 nA 0x2 - 2250 nA 0x3 - 1500 nA 0x4 - 1870 nA 0x5 - 1120 nA 0x6 - 750 nA 0x7 - 0 nA Default Value: 1

34 UDB Interface (UDBIF) Registers

This section discusses the UDBIF registers. It lists all the registers in mapping tables, in address order.

34.1 Register Details

Register Name	Address
UDB_UDBIF_BANK_CTL	0x400F7000
UDB_UDBIF_WAIT_CFG	0x400F7001
UDB_UDBIF_INT_CLK_CTL	0x400F701C

34.1.1 UDB_UDBIF_BANK_CTL

Bank Control

Address: 0x400F7000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None		RW	RW	RW	RW	RW
HW Access	R	None		R	R	R	R	R
Name	GLBL_WR	None [6:5]		PIPE	LOCK	BANK_EN	ROUTE_EN	DIS_COR

Bits	Name	Description
7	GLBL_WR	UDB Array Global Writing Option Default Value: 0 **0x0: DISABLE:** Global Writes disabled **0x1: ENABLE:** Global Writes enabled
4	PIPE	Pipelining Control Default Value: 0 **0x0: BYPASS:** Pipelining bypassed **0x1: PIPELINED:** Pipelining enabled
3	LOCK	UDB Array Configuration Locking Default Value: 0 **0x0: MUTABLE:** UDB Array configuration is writable **0x1: LOCKED:** UDB Array configuration is locked
2	BANK_EN	Enable Bank Default Value: 0 **0x0: DISABLE:** Bank disabled **0x1: ENABLE:** Bank enabled
1	ROUTE_EN	Enable Routing Default Value: 0 **0x0: DISABLE:** Routing disabled **0x1: ENABLE:** Routing enabled
0	DIS_COR	Selection of Clear-On-Read Default Value: 0

34.1.1 UDB_UDBIF_BANK_CTL (continued)

0x0: NORMAL:
Clear-On-Read enabled

0x1: DISABLE:
Clear-On-Read disabled

34.1.2 UDB_UDBIF_WAIT_CFG

Wait States Configuration

Address: 0x400F7001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	WR_WRK_WAIT [7:6]		RD_WRK_WAIT [5:4]		WR_CFG_WAIT [3:2]		RD_CFG_WAIT [1:0]	

Bits	Name	Description
7 : 6	WR_WRK_WAIT	Write Work Wait States Default Value: 0 **0x0: ONE_WAIT:** 1 wait states **0x1: TWO_WAITS:** 2 wait states **0x2: THREE_WAITS:** 3 wait states **0x3: ZERO_WAITS:** 0 wait state
5 : 4	RD_WRK_WAIT	Read Work Wait States Default Value: 0 **0x0: ONE_WAIT:** 1 wait states **0x1: TWO_WAITS:** 2 wait states **0x2: THREE_WAITS:** 3 wait states **0x3: ZERO_WAITS:** 0 wait state
3 : 2	WR_CFG_WAIT	Write Configuration Wait States Default Value: 0 **0x0: ONE_WAIT:** 1 wait states **0x1: TWO_WAITS:** 2 wait states **0x2: THREE_WAITS:** 3 wait states **0x3: ZERO_WAITS:** 0 wait state
1 : 0	RD_CFG_WAIT	Read Configuration Wait States Default Value: 0

34.1.2 UDB_UDBIF_WAIT_CFG (continued)

0x0: FIVE_WAITS:
5 wait states

0x1: FOUR_WAITS:
4 wait states

0x2: THREE_WAITS:
3 wait states

0x3: ONE_WAIT:
1 wait state

34.1.3 UDB_UDBIF_INT_CLK_CTL

Interrupt Synchronizer Clock Control

Address: 0x400F701C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							EN_HFCLK

Bits	Name	Description
0	EN_HFCLK	This bit enables the interrupt synchronizer in the UDB interface. It needs to be set whenever UDB/DSI interrupts are used. Disabling the interrupt synchronizer saves power in Active/Sleep mode. Default Value: 0

35 UDB Registers

This section discusses the UDB registers. It lists all the registers in mapping tables, in address order.

35.1 Register Details

Register Name	Address
UDB_INT_CFG	0x400F8000

35.1.1 UDB_INT_CFG

UDB Subsystem Interrupt Configuration

Address: 0x400F8000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INT_MODE_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							INT_MODE_CFG

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8 : 0	INT_MODE_CFG	Interrupt Mode; bit position corresponds to interrupt Default Value: 0 **0x0: LEVEL:** Level **0x1: PULSE:** Pulse

36 Single UDB (UDBSNG) Registers

This section discusses the UDBSNG registers. It lists all the registers in mapping tables, in address order.

36.1 Register Details

Register Name	Address
UDB_P0_U0_PLD_IT0	0x400F3000
UDB_P0_U0_PLD_IT1	0x400F3004
UDB_P0_U0_PLD_IT2	0x400F3008
UDB_P0_U0_PLD_IT3	0x400F300C
UDB_P0_U0_PLD_IT4	0x400F3010
UDB_P0_U0_PLD_IT5	0x400F3014
UDB_P0_U0_PLD_IT6	0x400F3018
UDB_P0_U0_PLD_IT7	0x400F301C
UDB_P0_U0_PLD_IT8	0x400F3020
UDB_P0_U0_PLD_IT9	0x400F3024
UDB_P0_U0_PLD_IT10	0x400F3028
UDB_P0_U0_PLD_IT11	0x400F302C
UDB_P0_U0_PLD_ORT0	0x400F3030
UDB_P0_U0_PLD_ORT1	0x400F3032
UDB_P0_U0_PLD_ORT2	0x400F3034
UDB_P0_U0_PLD_ORT3	0x400F3036
UDB_P0_U0_PLD_MC_CFG_CEN_CONST	0x400F3038
UDB_P0_U0_PLD_MC_CFG_XORFB	0x400F303A
UDB_P0_U0_PLD_MC_SET_RESET	0x400F303C
UDB_P0_U0_PLD_MC_CFG_BYPASS	0x400F303E
UDB_P0_U0_CFG0	0x400F3040
UDB_P0_U0_CFG1	0x400F3041
UDB_P0_U0_CFG2	0x400F3042
UDB_P0_U0_CFG3	0x400F3043
UDB_P0_U0_CFG4	0x400F3044
UDB_P0_U0_CFG5	0x400F3045
UDB_P0_U0_CFG6	0x400F3046

Register Name	Address
UDB_P0_U0_CFG7	0x400F3047
UDB_P0_U0_CFG8	0x400F3048
UDB_P0_U0_CFG9	0x400F3049
UDB_P0_U0_CFG10	0x400F304A
UDB_P0_U0_CFG11	0x400F304B
UDB_P0_U0_CFG12	0x400F304C
UDB_P0_U0_CFG13	0x400F304D
UDB_P0_U0_CFG14	0x400F304E
UDB_P0_U0_CFG15	0x400F304F
UDB_P0_U0_CFG16	0x400F3050
UDB_P0_U0_CFG17	0x400F3051
UDB_P0_U0_CFG18	0x400F3052
UDB_P0_U0_CFG19	0x400F3053
UDB_P0_U0_CFG20	0x400F3054
UDB_P0_U0_CFG21	0x400F3055
UDB_P0_U0_CFG22	0x400F3056
UDB_P0_U0_CFG23	0x400F3057
UDB_P0_U0_CFG24	0x400F3058
UDB_P0_U0_CFG25	0x400F3059
UDB_P0_U0_CFG26	0x400F305A
UDB_P0_U0_CFG27	0x400F305B
UDB_P0_U0_CFG28	0x400F305C
UDB_P0_U0_CFG29	0x400F305D
UDB_P0_U0_CFG30	0x400F305E
UDB_P0_U0_CFG31	0x400F305F
UDB_P0_U0_DCFG0	0x400F3060
UDB_P0_U0_DCFG1	0x400F3062
UDB_P0_U0_DCFG2	0x400F3064
UDB_P0_U0_DCFG3	0x400F3066
UDB_P0_U0_DCFG4	0x400F3068
UDB_P0_U0_DCFG5	0x400F306A
UDB_P0_U0_DCFG6	0x400F306C
UDB_P0_U0_DCFG7	0x400F306E
UDB_P0_U1_PLD_IT0	0x400F3080
UDB_P0_U1_PLD_IT1	0x400F3084
UDB_P0_U1_PLD_IT2	0x400F3088
UDB_P0_U1_PLD_IT3	0x400F308C
UDB_P0_U1_PLD_IT4	0x400F3090
UDB_P0_U1_PLD_IT5	0x400F3094
UDB_P0_U1_PLD_IT6	0x400F3098
UDB_P0_U1_PLD_IT7	0x400F309C
UDB_P0_U1_PLD_IT8	0x400F30A0

Register Name	Address
UDB_P0_U1_PLD_IT9	0x400F30A4
UDB_P0_U1_PLD_IT10	0x400F30A8
UDB_P0_U1_PLD_IT11	0x400F30AC
UDB_P0_U1_PLD_ORT0	0x400F30B0
UDB_P0_U1_PLD_ORT1	0x400F30B2
UDB_P0_U1_PLD_ORT2	0x400F30B4
UDB_P0_U1_PLD_ORT3	0x400F30B6
UDB_P0_U1_PLD_MC_CFG_CEN_CONST	0x400F30B8
UDB_P0_U1_PLD_MC_CFG_XORFB	0x400F30BA
UDB_P0_U1_PLD_MC_SET_RESET	0x400F30BC
UDB_P0_U1_PLD_MC_CFG_BYPASS	0x400F30BE
UDB_P0_U1_CFG0	0x400F30C0
UDB_P0_U1_CFG1	0x400F30C1
UDB_P0_U1_CFG2	0x400F30C2
UDB_P0_U1_CFG3	0x400F30C3
UDB_P0_U1_CFG4	0x400F30C4
UDB_P0_U1_CFG5	0x400F30C5
UDB_P0_U1_CFG6	0x400F30C6
UDB_P0_U1_CFG7	0x400F30C7
UDB_P0_U1_CFG8	0x400F30C8
UDB_P0_U1_CFG9	0x400F30C9
UDB_P0_U1_CFG10	0x400F30CA
UDB_P0_U1_CFG11	0x400F30CB
UDB_P0_U1_CFG12	0x400F30CC
UDB_P0_U1_CFG13	0x400F30CD
UDB_P0_U1_CFG14	0x400F30CE
UDB_P0_U1_CFG15	0x400F30CF
UDB_P0_U1_CFG16	0x400F30D0
UDB_P0_U1_CFG17	0x400F30D1
UDB_P0_U1_CFG18	0x400F30D2
UDB_P0_U1_CFG19	0x400F30D3
UDB_P0_U1_CFG20	0x400F30D4
UDB_P0_U1_CFG21	0x400F30D5
UDB_P0_U1_CFG22	0x400F30D6
UDB_P0_U1_CFG23	0x400F30D7
UDB_P0_U1_CFG24	0x400F30D8
UDB_P0_U1_CFG25	0x400F30D9
UDB_P0_U1_CFG26	0x400F30DA
UDB_P0_U1_CFG27	0x400F30DB
UDB_P0_U1_CFG28	0x400F30DC
UDB_P0_U1_CFG29	0x400F30DD
UDB_P0_U1_CFG30	0x400F30DE

Register Name	Address
UDB_P0_U1_CFG31	0x400F30DF
UDB_P0_U1_DCFG0	0x400F30E0
UDB_P0_U1_DCFG1	0x400F30E2
UDB_P0_U1_DCFG2	0x400F30E4
UDB_P0_U1_DCFG3	0x400F30E6
UDB_P0_U1_DCFG4	0x400F30E8
UDB_P0_U1_DCFG5	0x400F30EA
UDB_P0_U1_DCFG6	0x400F30EC
UDB_P0_U1_DCFG7	0x400F30EE
UDB_P1_U0_PLD_IT0	0x400F3200
UDB_P1_U0_PLD_IT1	0x400F3204
UDB_P1_U0_PLD_IT2	0x400F3208
UDB_P1_U0_PLD_IT3	0x400F320C
UDB_P1_U0_PLD_IT4	0x400F3210
UDB_P1_U0_PLD_IT5	0x400F3214
UDB_P1_U0_PLD_IT6	0x400F3218
UDB_P1_U0_PLD_IT7	0x400F321C
UDB_P1_U0_PLD_IT8	0x400F3220
UDB_P1_U0_PLD_IT9	0x400F3224
UDB_P1_U0_PLD_IT10	0x400F3228
UDB_P1_U0_PLD_IT11	0x400F322C
UDB_P1_U0_PLD_ORT0	0x400F3230
UDB_P1_U0_PLD_ORT1	0x400F3232
UDB_P1_U0_PLD_ORT2	0x400F3234
UDB_P1_U0_PLD_ORT3	0x400F3236
UDB_P1_U0_PLD_MC_CFG_CEN_CONST	0x400F3238
UDB_P1_U0_PLD_MC_CFG_XORFB	0x400F323A
UDB_P1_U0_PLD_MC_SET_RESET	0x400F323C
UDB_P1_U0_PLD_MC_CFG_BYPASS	0x400F323E
UDB_P1_U0_CFG0	0x400F3240
UDB_P1_U0_CFG1	0x400F3241
UDB_P1_U0_CFG2	0x400F3242
UDB_P1_U0_CFG3	0x400F3243
UDB_P1_U0_CFG4	0x400F3244
UDB_P1_U0_CFG5	0x400F3245
UDB_P1_U0_CFG6	0x400F3246
UDB_P1_U0_CFG7	0x400F3247
UDB_P1_U0_CFG8	0x400F3248
UDB_P1_U0_CFG9	0x400F3249
UDB_P1_U0_CFG10	0x400F324A
UDB_P1_U0_CFG11	0x400F324B
UDB_P1_U0_CFG12	0x400F324C

Register Name	Address
UDB_P1_U0_CFG13	0x400F324D
UDB_P1_U0_CFG14	0x400F324E
UDB_P1_U0_CFG15	0x400F324F
UDB_P1_U0_CFG16	0x400F3250
UDB_P1_U0_CFG17	0x400F3251
UDB_P1_U0_CFG18	0x400F3252
UDB_P1_U0_CFG19	0x400F3253
UDB_P1_U0_CFG20	0x400F3254
UDB_P1_U0_CFG21	0x400F3255
UDB_P1_U0_CFG22	0x400F3256
UDB_P1_U0_CFG23	0x400F3257
UDB_P1_U0_CFG24	0x400F3258
UDB_P1_U0_CFG25	0x400F3259
UDB_P1_U0_CFG26	0x400F325A
UDB_P1_U0_CFG27	0x400F325B
UDB_P1_U0_CFG28	0x400F325C
UDB_P1_U0_CFG29	0x400F325D
UDB_P1_U0_CFG30	0x400F325E
UDB_P1_U0_CFG31	0x400F325F
UDB_P1_U0_DCFG0	0x400F3260
UDB_P1_U0_DCFG1	0x400F3262
UDB_P1_U0_DCFG2	0x400F3264
UDB_P1_U0_DCFG3	0x400F3266
UDB_P1_U0_DCFG4	0x400F3268
UDB_P1_U0_DCFG5	0x400F326A
UDB_P1_U0_DCFG6	0x400F326C
UDB_P1_U0_DCFG7	0x400F326E
UDB_P1_U1_PLD_IT0	0x400F3280
UDB_P1_U1_PLD_IT1	0x400F3284
UDB_P1_U1_PLD_IT2	0x400F3288
UDB_P1_U1_PLD_IT3	0x400F328C
UDB_P1_U1_PLD_IT4	0x400F3290
UDB_P1_U1_PLD_IT5	0x400F3294
UDB_P1_U1_PLD_IT6	0x400F3298
UDB_P1_U1_PLD_IT7	0x400F329C
UDB_P1_U1_PLD_IT8	0x400F32A0
UDB_P1_U1_PLD_IT9	0x400F32A4
UDB_P1_U1_PLD_IT10	0x400F32A8
UDB_P1_U1_PLD_IT11	0x400F32AC
UDB_P1_U1_PLD_ORT0	0x400F32B0
UDB_P1_U1_PLD_ORT1	0x400F32B2
UDB_P1_U1_PLD_ORT2	0x400F32B4

Register Name	Address
UDB_P1_U1_PLD_ORT3	0x400F32B6
UDB_P1_U1_PLD_MC_CFG_CEN_CONST	0x400F32B8
UDB_P1_U1_PLD_MC_CFG_XORFB	0x400F32BA
UDB_P1_U1_PLD_MC_SET_RESET	0x400F32BC
UDB_P1_U1_PLD_MC_CFG_BYPASS	0x400F32BE
UDB_P1_U1_CFG0	0x400F32C0
UDB_P1_U1_CFG1	0x400F32C1
UDB_P1_U1_CFG2	0x400F32C2
UDB_P1_U1_CFG3	0x400F32C3
UDB_P1_U1_CFG4	0x400F32C4
UDB_P1_U1_CFG5	0x400F32C5
UDB_P1_U1_CFG6	0x400F32C6
UDB_P1_U1_CFG7	0x400F32C7
UDB_P1_U1_CFG8	0x400F32C8
UDB_P1_U1_CFG9	0x400F32C9
UDB_P1_U1_CFG10	0x400F32CA
UDB_P1_U1_CFG11	0x400F32CB
UDB_P1_U1_CFG12	0x400F32CC
UDB_P1_U1_CFG13	0x400F32CD
UDB_P1_U1_CFG14	0x400F32CE
UDB_P1_U1_CFG15	0x400F32CF
UDB_P1_U1_CFG16	0x400F32D0
UDB_P1_U1_CFG17	0x400F32D1
UDB_P1_U1_CFG18	0x400F32D2
UDB_P1_U1_CFG19	0x400F32D3
UDB_P1_U1_CFG20	0x400F32D4
UDB_P1_U1_CFG21	0x400F32D5
UDB_P1_U1_CFG22	0x400F32D6
UDB_P1_U1_CFG23	0x400F32D7
UDB_P1_U1_CFG24	0x400F32D8
UDB_P1_U1_CFG25	0x400F32D9
UDB_P1_U1_CFG26	0x400F32DA
UDB_P1_U1_CFG27	0x400F32DB
UDB_P1_U1_CFG28	0x400F32DC
UDB_P1_U1_CFG29	0x400F32DD
UDB_P1_U1_CFG30	0x400F32DE
UDB_P1_U1_CFG31	0x400F32DF
UDB_P1_U1_DCFG0	0x400F32E0
UDB_P1_U1_DCFG1	0x400F32E2
UDB_P1_U1_DCFG2	0x400F32E4
UDB_P1_U1_DCFG3	0x400F32E6
UDB_P1_U1_DCFG4	0x400F32E8

Register Name	Address
UDB_P1_U1_DCFG5	0x400F32EA
UDB_P1_U1_DCFG6	0x400F32EC
UDB_P1_U1_DCFG7	0x400F32EE

36.1.1 UDB_P0_U0_PLD_IT0

PLD Input Terms

Address: 0x400F3000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.1 UDB_P0_U0_PLD_IT0 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.1 UDB_P0_U0_PLD_IT0 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.2 UDB_P0_U0_PLD_IT1

PLD Input Terms

Address: 0x400F3004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.2 UDB_P0_U0_PLD_IT1 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.2 UDB_P0_U0_PLD_IT1 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.3 UDB_P0_U0_PLD_IT2

PLD Input Terms

Address: 0x400F3008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.3 UDB_P0_U0_PLD_IT2 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.3 UDB_P0_U0_PLD_IT2 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.4 UDB_P0_U0_PLD_IT3

PLD Input Terms

Address: 0x400F300C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.4 UDB_P0_U0_PLD_IT3 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.4 UDB_P0_U0_PLD_IT3 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.5 UDB_P0_U0_PLD_IT4

PLD Input Terms

Address: 0x400F3010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.5 UDB_P0_U0_PLD_IT4 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.5 UDB_P0_U0_PLD_IT4 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.6 UDB_P0_U0_PLD_IT5

PLD Input Terms

Address: 0x400F3014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.6 UDB_P0_U0_PLD_IT5 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.6 UDB_P0_U0_PLD_IT5 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.7 UDB_P0_U0_PLD_IT6

PLD Input Terms

Address: 0x400F3018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.7 UDB_P0_U0_PLD_IT6 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.7 UDB_P0_U0_PLD_IT6 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.8 UDB_P0_U0_PLD_IT7

PLD Input Terms

Address: 0x400F301C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.8 UDB_P0_U0_PLD_IT7 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.8 UDB_P0_U0_PLD_IT7 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.9 UDB_P0_U0_PLD_IT8

PLD Input Terms

Address: 0x400F3020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.9 UDB_P0_U0_PLD_IT8 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.9 UDB_P0_U0_PLD_IT8 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.10 UDB_P0_U0_PLD_IT9

PLD Input Terms

Address: 0x400F3024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.10 UDB_P0_U0_PLD_IT9 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.10 UDB_P0_U0_PLD_IT9 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.11 UDB_P0_U0_PLD_IT10

PLD Input Terms

Address: 0x400F3028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.11 UDB_P0_U0_PLD_IT10 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.11 UDB_P0_U0_PLD_IT10 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.12 UDB_P0_U0_PLD_IT11

PLD Input Terms

Address: 0x400F302C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.12 UDB_P0_U0_PLD_IT11 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.12 UDB_P0_U0_PLD_IT11 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.13 UDB_P0_U0_PLD_ORT0

PLD OR Terms

Address: 0x400F3030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

36.1.13 UDB_P0_U0_PLD_ORT0 (continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.14 UDB_P0_U0_PLD_ORT1

PLD OR Terms

Address: 0x400F3032

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

36.1.14 UDB_P0_U0_PLD_ORT1 (continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.15 UDB_P0_U0_PLD_ORT2

PLD OR Terms

Address: 0x400F3034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

36.1.15 UDB_P0_U0_PLD_ORT2 (continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.16 UDB_P0_U0_PLD_ORT3

PLD OR Terms

Address: 0x400F3036

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

36.1.16 UDB_P0_U0_PLD_ORT3 (continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.17 UDB_P0_U0_PLD_MC_CFG_CEN_CONST

Macrocell configuration for Carry Enable and Constant

Address: 0x400F3038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_DFF_C	PLD0_MC3_CEN	PLD0_MC2_DFF_C	PLD0_MC2_CEN	PLD0_MC1_DFF_C	PLD0_MC1_CEN	PLD0_MC0_DFF_C	PLD0_MC0_CEN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_DFF_C	PLD1_MC3_CEN	PLD1_MC2_DFF_C	PLD1_MC2_CEN	PLD1_MC1_DFF_C	PLD1_MC1_CEN	PLD1_MC0_DFF_C	PLD1_MC0_CEN

Bits	Name	Description
15	PLD1_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
14	PLD1_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
13	PLD1_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
12	PLD1_MC2_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

36.1.17 UDB_P0_U0_PLD_MC_CFG_CEN_CONST (continued)

11	PLD1_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
10	PLD1_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
9	PLD1_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
8	PLD1_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
7	PLD0_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
6	PLD0_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
5	PLD0_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
4	PLD0_MC2_CEN	Carry enable Default Value: X

36.1.17 UDB_P0_U0_PLD_MC_CFG_CEN_CONST (continued)

		0x0: DISABLE: Disabled **0x1: ENABLE:** Enabled
3	PLD0_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
2	PLD0_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
1	PLD0_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
0	PLD0_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

36.1.18 UDB_P0_U0_PLD_MC_CFG_XORFB

PLD Macro cell XOR feedback

Address: 0x400F303A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD0_MC3_XORFB [7:6]		PLD0_MC2_XORFB [5:4]		PLD0_MC1_XORFB [3:2]		PLD0_MC0_XORFB [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD1_MC3_XORFB [15:14]		PLD1_MC2_XORFB [13:12]		PLD1_MC1_XORFB [11:10]		PLD1_MC0_XORFB [9:8]	

Bits	Name	Description
15 : 14	PLD1_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
13 : 12	PLD1_MC2_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
11 : 10	PLD1_MC1_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry

36.1.18 UDB_P0_U0_PLD_MC_CFG_XORFB (continued)

		0x2: TFF_H: TFF on high **0x3: TFF_L:** TFF on low
9 : 8	PLD1_MC0_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
7 : 6	PLD0_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
5 : 4	PLD0_MC2_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
3 : 2	PLD0_MC1_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low

36.1.18 UDB_P0_U0_PLD_MC_CFG_XORFB (continued)

1 : 0	PLD0_MC0_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low

36.1.19 UDB_P0_U0_PLD_MC_SET_RESET

PLD Macro cell Set Reset Selection

Address: 0x400F303C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_RESET_SEL	PLD0_MC3_SET_SEL	PLD0_MC2_RESET_SEL	PLD0_MC2_SET_SEL	PLD0_MC1_RESET_SEL	PLD0_MC1_SET_SEL	PLD0_MC0_RESET_SEL	PLD0_MC0_SET_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_RESET_SEL	PLD1_MC3_SET_SEL	PLD1_MC2_RESET_SEL	PLD1_MC2_SET_SEL	PLD1_MC1_RESET_SEL	PLD1_MC1_SET_SEL	PLD1_MC0_RESET_SEL	PLD1_MC0_SET_SEL

Bits	Name	Description
15	PLD1_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
14	PLD1_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
13	PLD1_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
12	PLD1_MC2_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

36.1.19 UDB_P0_U0_PLD_MC_SET_RESET (continued)

11	PLD1_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
10	PLD1_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
9	PLD1_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
8	PLD1_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
7	PLD0_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
6	PLD0_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
5	PLD0_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
4	PLD0_MC2_SET_SEL	Set select enable Default Value: X

36.1.19 UDB_P0_U0_PLD_MC_SET_RESET (continued)

		0x0: DISABLE: Set not used **0x1: ENABLE:** Set enabled
3	PLD0_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
2	PLD0_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
1	PLD0_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
0	PLD0_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

36.1.20 UDB_P0_U0_PLD_MC_CFG_BYPASS

PLD Macro cell Bypass control

Address: 0x400F303E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	NC7	PLD0_MC3_BYPASS	NC5	PLD0_MC2_BYPASS	NC3	PLD0_MC1_BYPASS	NC1	PLD0_MC0_BYPASS

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	NC15	PLD1_MC3_BYPASS	NC13	PLD1_MC2_BYPASS	NC11	PLD1_MC1_BYPASS	NC9	PLD1_MC0_BYPASS

Bits	Name	Description
15	NC15	Spare register bit Default Value: X
14	PLD1_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
13	NC13	Spare register bit Default Value: X
12	PLD1_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
11	NC11	Spare register bit Default Value: X
10	PLD1_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output

36.1.20 UDB_P0_U0_PLD_MC_CFG_BYPASS (continued)

9	NC9	Spare register bit Default Value: X
8	PLD1_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
7	NC7	Spare register bit Default Value: X
6	PLD0_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
5	NC5	Spare register bit Default Value: X
4	PLD0_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
3	NC3	Spare register bit Default Value: X
2	PLD0_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
1	NC1	Spare register bit Default Value: X
0	PLD0_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output

36.1.21 UDB_P0_U0_CFG0

Datapath Input Selection - RAD1 RAD0. Address bits 0 and 1 to the dynamic configuration RAM

Address: 0x400F3040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	RAD1 [6:4]			None	RAD0 [2:0]		

Bits	Name	Description
6 : 4	RAD1	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	RAD0	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

36.1.21 UDB_P0_U0_CFG0 (continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.22 UDB_P0_U0_CFG1

Datapath Input Selection - RAD2. Address bit 2 to the dynamic configuration RAM

Address: 0x400F3041

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW		
HW Access	R	R	R	R	R	R		
Name	DP_RTE_BYPASS4	DP_RTE_BYPASS3	DP_RTE_BYPASS2	DP_RTE_BYPASS1	DP_RTE_BYPASS0	RAD2 [2:0]		

Bits	Name	Description
7	DP_RTE_BYPASS4	DP_In bypass control Default Value: 0 **0x0: DP_IN4_ROUTE:** Use dp_in[4] **0x1: DP_IN4_BYPASS:** Use dp_out[4] as input via bypass
6	DP_RTE_BYPASS3	DP_In bypass control Default Value: 0 **0x0: DP_IN3_ROUTE:** Use dp_in[3] **0x1: DP_IN3_BYPASS:** Use dp_out[3] as input via bypass
5	DP_RTE_BYPASS2	DP_In bypass control Default Value: 0 **0x0: DP_IN2_ROUTE:** Use dp_in[2] **0x1: DP_IN2_BYPASS:** Use dp_out[2] as input via bypass
4	DP_RTE_BYPASS1	DP_In bypass control Default Value: 0 **0x0: DP_IN1_ROUTE:** Use dp_in[1] **0x1: DP_IN1_BYPASS:** Use dp_out[1] as input via bypass
3	DP_RTE_BYPASS0	DP_In bypass control Default Value: 0 **0x0: DP_IN0_ROUTE:** Use dp_in[0] **0x1: DP_IN0_BYPASS:** Use dp_out[0] as input via bypass

36.1.22 UDB_P0_U0_CFG1 (continued)

2 : 0	RAD2	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved

36.1.23 UDB_P0_U0_CFG2

Datapath Input Selection - F1_LD, F0_LD.

Address: 0x400F3042

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	NC7	F1_LD [6:4]			DP_RTE_BYPASS5	F0_LD [2:0]		

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6 : 4	F1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
3	DP_RTE_BYPASS5	DP_In bypass control Default Value: 0 **0x0: DP_IN5_ROUTE:** Use dp_in[5] **0x1: DP_IN5_BYPASS:** Use dp_out[5] via bypass
2 : 0	F0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off

36.1.23 UDB_P0_U0_CFG2 (continued)

0x1: DP_IN0:
Set to dp_in[0]

0x2: DP_IN1:
Set to dp_in[1]

0x3: DP_IN2:
Set to dp_in[2]

0x4: DP_IN3:
Set to dp_in[3]

0x5: DP_IN4:
Set to dp_in[4]

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.24 UDB_P0_U0_CFG3

Datapath Input Selection - D1_LD, D0_LD.

Address: 0x400F3043

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	D1_LD [6:4]			None	D0_LD [2:0]		

Bits	Name	Description
6 : 4	D1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	D0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

36.1.24 UDB_P0_U0_CFG3 (continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.25 UDB_P0_U0_CFG4

Datapath Input Selection - CI_MUX SI_MUX.

Address: 0x400F3044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	CI_MUX [6:4]			None	SI_MUX [2:0]		

Bits	Name	Description
6 : 4	CI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	SI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

36.1.25 UDB_P0_U0_CFG4 (continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.26 UDB_P0_U0_CFG5

Datapath Output Selection for OUT1 OUT0

Address: 0x400F3045

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT1 [7:4]				OUT0 [3:0]			

Bits	Name	Description
7 : 4	OUT1	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

36.1.26 UDB_P0_U0_CFG5 (continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT0	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.27 UDB_P0_U0_CFG6

Datapath Output Selection for OUT3 OUT2

Address: 0x400F3046

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT3 [7:4]				OUT2 [3:0]			

Bits	Name	Description
7 : 4	OUT3	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

36.1.27 UDB_P0_U0_CFG6 (continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT2	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.28 UDB_P0_U0_CFG7

Datapath Output Selection for OUT5 OUT4

Address: 0x400F3047

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT5 [7:4]				OUT4 [3:0]			

Bits	Name	Description
7 : 4	OUT5	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

36.1.28 UDB_P0_U0_CFG7 (continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT4	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.29 UDB_P0_U0_CFG8

Datapath Output Synchronization Option

Address: 0x400F3048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW					
HW Access	R	R	R					
Name	NC7	NC6	OUT_SYNC [5:0]					

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6	NC6	Spare register bit Default Value: 0
5 : 0	OUT_SYNC	Datapath Output Synchronization. Each datapath output can be registered (default,0), or combinational (1) Default Value: 0 **0x0: REGISTERED:** registered **0x1: COMBINATIONAL:** combinational

36.1.30 UDB_P0_U0_CFG9

Datapath ALU Mask

Address: 0x400F3049

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	AMASK [7:0]							

Bits	Name	Description
7 : 0	AMASK	Datapath ALU Mask. The mask value in this register is applied to the output of the Datapath ALU result before the result is stored. The AMASK_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.31 UDB_P0_U0_CFG10

Datapath Compare 0 Mask

Address: 0x400F304A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMASK0 [7:0]							

Bits	Name	Description
7 : 0	CMASK0	Datapath Compare 0 Mask. The mask value in this register is applied to the output of the Accumulator 0 before it is used for comparison in Compare block 0. The CMASK0_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.32 UDB_P0_U0_CFG11

Datapath Compare 1 Mask

Address: 0x400F304B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMASK0 [7:0]							

Bits	Name	Description
7 : 0	CMASK0	Datapath Compare 1 Mask. The mask value in this register is applied to the selected Compare 1 block input (Accumulator 0 or Accumulator 1) before it is used for comparison. The CMASK1_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.33 UDB_P0_U0_CFG12

Datapath mask enables and shift in configuration

Address: 0x400F304C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	CMASK1_EN	CMASK0_EN	AMASK_EN	DEF_SI	SI_SELB [3:2]		SI_SELA [1:0]	

Bits	Name	Description
7	CMASK1_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
6	CMASK0_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
5	AMASK_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
4	DEF_SI	Datapath default shift value Default Value: 0 **0x0: DEFAULT_0:** Default shift is 0 **0x1: DEFAULT_1:** Default shift is 1
3 : 2	SI_SELB	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle

36.1.33 UDB_P0_U0_CFG12 (continued)

		0x2: ROUTE: Shift in is selected from datapath routing input **0x3: CHAIN:** Shift in is chained from the previous datapath
1 : 0	SI_SELA	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle **0x2: ROUTE:** Shift in is selected from datapath routing input **0x3: CHAIN:** Shift in is chained from the previous datapath

36.1.34 UDB_P0_U0_CFG13

Datapath carry in and compare configuration

Address: 0x400F304D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CMP_SELB [7:6]		CMP_SELA [5:4]		CI_SELB [3:2]		CI_SELA [1:0]	

Bits	Name	Description
7 : 6	CMP_SELB	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
5 : 4	CMP_SELA	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
3 : 2	CI_SELB	Datapath carry in source select Default Value: 0 **0x0: DEFAULT:** Default arithmetic mode **0x1: REGISTERED:** Carry in is the carry out registered from previous cycle **0x2: ROUTE:** Carry in is selected from datapath routing input **0x3: CHAIN:** Carry in is chained from the previous datapath
1 : 0	CI_SELA	Datapath carry in source select Default Value: 0

36.1.34 UDB_P0_U0_CFG13 (continued)

0x0: DEFAULT:
Default arithmetic mode

0x1: REGISTERED:
Carry in is the carry out registered from previous cycle

0x2: ROUTE:
Carry in is selected from datapath routing input

0x3: CHAIN:
Carry in is chained from the previous datapath

36.1.35 UDB_P0_U0_CFG14

Datapath chaining and MSB configuration

Address: 0x400F304E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW	RW	RW
HW Access	R	R			R	R	R	R
Name	MSB_EN	MSB_SEL [6:4]			CHAIN_CMSB	CHAIN_FB	CHAIN1	CHAIN0

Bits	Name	Description
7	MSB_EN	Datapath MSB selection enable Default Value: 0 **0x0: DISABLE:** MSB selection is disabled, MSB is bit 7 **0x1: ENABLE:** MSB selection is controlled by MSB_SEL
6 : 4	MSB_SEL	Datapath MSB Selection Default Value: 0 **0x0: BIT0:** MSB is bit 0 **0x1: BIT1:** MSB is bit 1 **0x2: BIT2:** MSB is bit 2 **0x3: BIT3:** MSB is bit 3 **0x4: BIT4:** MSB is bit 4 **0x5: BIT5:** MSB is bit 5 **0x6: BIT6:** MSB is bit 6 **0x7: BIT7:** MSB is bit 7 - equivalent to MSB_EN=0
3	CHAIN_CMSB	Datapath CRC MSB chaining enable Default Value: 0 **0x0: DISABLE:** CRC MSB is not chained **0x1: ENABLE:** CRC MSB is chained from the next (MSB) datapath

36.1.35 UDB_P0_U0_CFG14 (continued)

2	CHAIN_FB	Datapath CRC feedback chaining enable Default Value: 0 **0x0: DISABLE:** CRC feedback is not chained **0x1: ENABLE:** CRC feedback is chained from the previous (LSB) datapath
1	CHAIN1	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath
0	CHAIN0	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath

36.1.36 UDB_P0_U0_CFG15

Datapath FIFO, shift and parallel input control

Address: 0x400F304F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	PI_SEL	SHIFT_SEL	PI_DYN	MSB_SI	F1_INSEL [3:2]		F0_INSEL [1:0]	

Bits	Name	Description
7	PI_SEL	Datapath parallel input selection Default Value: 0 **0x0: NORMAL:** Normal operation, ALU source is from accumulator selection **0x1: PARALLEL:** ALU source A input is from the parallel data input
6	SHIFT_SEL	Datapath shift out selection Default Value: 0 **0x0: SOL_MSB:** Routed shift out is shift out left (sol_msb) **0x1: SOR:** Routed shift out is shift out right (sor)
5	PI_DYN	Enable for dynamic control of parallel data input (PI) mux. Default Value: 0 **0x0: DISABLE:** Parallel input mux select is only controlled by static configuration (PI_SEL). **0x1: ENABLE:** Parallel input mux to the Datapath is controlled by CFB_EN field in Datapath Dynamic RAM. When this mode is enabled, the CFB_EN usage for CRC/PRS functionality is disabled.
4	MSB_SI	Arithmetic shift right operation shift in selection Default Value: 0 **0x0: DEFAULT:** Shift in default value (when SI_SELA and/or SI_SELB == 0) **0x1: MSB:** Override default and shift in MSB value
3 : 2	F1_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus

36.1.36 UDB_P0_U0_CFG15 (continued)

		0x2: OUTPUT_A1: Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus
1 : 0	F0_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus **0x2: OUTPUT_A1:** Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus

36.1.37 UDB_P0_U0_CFG16

Datapath FIFO and register access configuration control

Address: 0x400F3050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	F1_CK_INV	F0_CK_INV	FIFO_FAST	FIFO_CAP	FIFO_EDGE	FIFO_ASYNC	EXT_CRCPRS	WRK16_CONCAT

Bits	Name	Description
7	F1_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
6	F0_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
5	FIFO_FAST	FIFO Fast Mode. When this bit is set, the FIFO write logic is clocked by the application bus clock. Lowers the latency of capture timing, at the expense of additional power. Default Value: 0 **0x0: DISABLE:** FIFO is clocked with selected Datapath clock. **0x1: ENABLE:** FIFO is clocked with application bus clock. Master and quadrant bus clock gating must be enabled.
4	FIFO_CAP	FIFO Software Capture Mode. When this bit is set, a read of A0 or A1 triggers a capture into F0 or F1 respectively. This function follows the chaining configuration. All accumulators in the chain from a given block to the MS block in the chain are capture Default Value: 0 **0x0: DISABLE:** FIFO capture is disabled. **0x1: ENABLE:** FIFO capture is enabled (FIFO must be in output mode). A read of A0 or A1 will write into F0 or F1.
3	FIFO_EDGE	Edge/level sensitive FIFO write control (Fx_LD). Only applies to FIFO configured in output mode Default Value: 0

36.1.37 UDB_P0_U0_CFG16 (continued)

		0x0: LEVEL: FIFO write from accumulators/ALU is level sensitive. FIFO write occurs on a clock edge whenever the write control is sampled high on that edge. **0x1: EDGE:** FIFO write from accumulators/ALU is edge sensitive. FIFO write occurs on a clock edge folloing a 0 to 1 transition on the write control. The write control must be negated for at least one full cycle of the FIFO clock for a subsequent transition to be dete
2	FIFO_ASYNC	Asynchronous FIFO clocking support Default Value: 0 **0x0: DISABLE:** FIFO clocks are synchronous **0x1: ENABLE:** FIFO clocks are asynchronous
1	EXT_CRCPRS	External CRC/PRS mode Default Value: 0 **0x0: INTERNAL:** Internal CRC/PRS routing **0x1: EXTERNAL:** External CRC/PRS routing
0	WRK16_CONCAT	Datapath register access mode Default Value: 0 **0x0: DEFAULT:** 16-bit default access mode: selects registers in two consecutive UDBs in chaining order **0x1: CONCATENATE:** 16-bit concat access mode: selects concatenated registers in a single UDB

36.1.38 UDB_P0_U0_CFG17

Datapath FIFO control

Address: 0x400F3051

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			FIFO_ADD_SYNC	NC3	NC2	F1_DYN	F0_DYN

Bits	Name	Description
4	FIFO_ADD_SYNC	Adds an additional sync flip-flop to FIFO block status. Default Value: 0 **0x0: DISABLE:** Compatible Mode: FIFO block status sync configuration is 'none' (FIFO_ASYNC = 0) and 1 sync flip-flop (FIFO_ASYNC = 1) **0x1: ENABLE:** Add Sync Mode: FIFO block status sync configuration 1 sync flip-flop (FIFO_ASYNC = 0) and 2 sync flip-flops (FIFO_ASYNC = 1)
3	NC3	Spare register bit Default Value: 0
2	NC2	Spare register bit Default Value: 0
1	F1_DYN	Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest
0	F0_DYN	When this bit is set, the associated FIFO configuration may be dynamically controlled. Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest

36.1.39 UDB_P0_U0_CFG18

Control Register Mode 0 (used in conjunction with Control Register Mode 1)

Address: 0x400F3052

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_MD0 [7:0]							

Bits	Name	Description
7 : 0	CTL_MD0	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

36.1.40 UDB_P0_U0_CFG19

Control Register Mode 1 (used in conjunction with Control Register Mode 0)

Address: 0x400F3053

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_MD1 [7:0]							

Bits	Name	Description
7 : 0	CTL_MD1	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

36.1.41 UDB_P0_U0_CFG20

Status Register input mode selection

Address: 0x400F3054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	STAT_MD [7:0]							

Bits	Name	Description
7 : 0	STAT_MD	Mode selection for each bit of the status register. A '0' is transparent mode, where internal routing is read idrectly by CPU firmware. A '1' is sticky-clear-on-read mode, where once the given bit is set, it will stay set until the CPU reads the bit. Default Value: 0

36.1.42 UDB_P0_U0_CFG21

Spare register bits

Address: 0x400F3055

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NC1	NC0

Bits	Name	Description
1	NC1	Spare register bit Default Value: 0
0	NC0	Spare register bit Default Value: 0

36.1.43 UDB_P0_U0_CFG22

SC block configuration control

Address: 0x400F3056

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	
HW Access	None			R	R	R	R	
Name	None [7:5]			SC_EXT_RES	SC_SYNC_MD	SC_INT_MD	SC_OUT_CTL [1:0]	

Bits	Name	Description
4	SC_EXT_RES	Control register external reset operation. This bit supports autonomous usage of the control register, where a routed reset should clear the writable input registers. By default this is off because the CPU writable register can be cleared in firmware. Default Value: 0 **0x0: DISABLED:** When a routed reset is applied to the control register, only embedded state (sampling registers) are cleared **0x1: ENABLED:** When a routed reset is applied to the control register, all state is cleared, including the CPU writable control bits.
3	SC_SYNC_MD	SC Sync Mode - controls when the status register operates as a 4-bit double synchronizer module Default Value: 0 **0x0: NORMAL:** Normal Mode - Status register operation **0x1: SYNC_MODE:** Sync Mode - Routing inputs sc_in[3:0] are the 4 sync inputs, and connections sc_io[3:0] operate as the sync outputs
2	SC_INT_MD	SC Interrupt Mode - controls when the UDB driving an interrupt generated from the masked OR reduction of status bits 6 to 0 Default Value: 0 **0x0: NORMAL:** Normal Mode - Routing connection sc_io[3] is a normal input to the status register **0x1: INT_MODE:** Interrupt Mode - Routing connection sc_io[3] operates as the UDB interrupt output
1 : 0	SC_OUT_CTL	Selects the output source for the Status and Control routing connections Default Value: 0 **0x0: CONTROL:** Control out, 8-bits of control are driven to the routing connections **0x1: PARALLEL:** Datapath parallel output, 8-bits of datapath parallel output data are driven to the routing connections

36.1.43 UDB_P0_U0_CFG22 (continued)

0x2: COUNTER:
Counter out, 7-bits of count and 1 bit (MSB) of terminal count are driven to the routing connections

0x3: RESERVED:
Reserved

36.1.44 UDB_P0_U0_CFG23

Counter Control

Address: 0x400F3057

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW		RW	
HW Access	None	R	R	R	R		R	
Name	None	ALT_CNT	ROUTE_EN	ROUTE_LD	CNT_EN_SEL [3:2]		CNT_LD_SEL [1:0]	

Bits	Name	Description
6	ALT_CNT	Configure the alternate operating mode of the counter Default Value: 0 **0x0: DEFAULT_MODE:** Default counter operating mode **0x1: ALT_MODE:** Alternate counter operating mode
5	ROUTE_EN	Configure the counter enable signal for routing input Default Value: 0 **0x0: DISABLE:** Routed EN signal is not used. EN signal is only controlled by firmware CNT START (ACTL register) **0x1: ROUTED:** Routed EN signal is used, CNT START must be set
4	ROUTE_LD	Configure the counter load signal for routing input Default Value: 0 **0x0: DISABLE:** Routed LD signal is not used **0x1: ROUTED:** Routed LD signal is used
3 : 2	CNT_EN_SEL	Selects the routing inputs for the counter enable signal Default Value: 0 **0x0: SC_IN4:** sc_io_in[0] **0x1: SC_IN5:** sc_io_in[1] **0x2: SC_IN6:** sc_io_in[2] **0x3: SC_IO:** sc_io_in[3]
1 : 0	CNT_LD_SEL	Selects the routing inputs for the counter load signal Default Value: 0

36.1.44 UDB_P0_U0_CFG23 (continued)

0x0: SC_IN0:
sc_in[0]

0x1: SC_IN1:
sc_in[1]

0x2: SC_IN2:
sc_in[2]

0x3: SC_IN3:
sc_in[3]

36.1.45 UDB_P0_U0_CFG24

PLD0 Clock and Reset control

Address: 0x400F3058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

36.1.45 UDB_P0_U0_CFG24 (continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.46 UDB_P0_U0_CFG25

PLD1 Clock and Reset control

Address: 0x400F3059

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

36.1.46 UDB_P0_U0_CFG25 (continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.47 UDB_P0_U0_CFG26

Datapath Clock and Reset control

Address: 0x400F305A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

36.1.47 UDB_P0_U0_CFG26 (continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.48 UDB_P0_U0_CFG27

Status/Control Clock and Reset control

Address: 0x400F305B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

36.1.48 UDB_P0_U0_CFG27 (continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.49 UDB_P0_U0_CFG28

Clock Selection for PLD1 and PLD0

Address: 0x400F305C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PLD1_CK_SEL [7:4]				PLD0_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	PLD1_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	PLD0_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

36.1.49 UDB_P0_U0_CFG28 (continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

36.1.50 UDB_P0_U0_CFG29

Clock Selection for Datapath, Status and Control

Address: 0x400F305D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SC_CK_SEL [7:4]				DP_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	SC_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	DP_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

36.1.50 UDB_P0_U0_CFG29 (continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

36.1.51 UDB_P0_U0_CFG30

Reset control

Address: 0x400F305E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None	RW	RW	RW	RW	
HW Access	R	R	None	R	R	R	R	
Name	SC_RES_POL	DP_RES_POL	None	GUDB_WR	EN_RES_CNTCTL	RES_POL	RES_SEL [1:0]	

Bits	Name	Description
7	SC_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected SC routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Status and Control block is true polarity. **0x1: INVERT:** Routed reset to the Status and Control block is inverted polarity.
6	DP_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected Datapath routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Datapath block is true polarity. **0x1: INVERT:** Routed reset to the Datapath block is inverted polarity.
4	GUDB_WR	Enable global write operation for the configuration and working registers in this UDB. When this bit is set, the UDB ID select decoding is bypassed. Default Value: 0 **0x0: DISABLE:** Global UDB configuration/working register write is disabled **0x1: ENABLE:** Global UDB configuration/working register write is enabled
3	EN_RES_CNTCTL	This bit gates the routed reset to the counter/control register. By default, the operation is compatible, i.e., it only applies to the counter. However, if the updated control regisiter modes are used (sync mode, pulse mode, or the ext res bit) then the routed reset applies to the control register also. Default Value: 0 **0x0: DISABLE:** Routed reset is not applied to counter/control register **0x1: ENABLE:** Routed reset is applied to the counter/control register

36.1.51 UDB_P0_U0_CFG30 (continued)

2	RES_POL	The meaning of this bit depends on the value of the ALT RES bit in CFG31. When ALT RES is '0' (compatible mode), this bit sets the polarity of the routed reset. When ALT RES is '1', this bit is unused. Default Value: 0 **0x0: NEGATED:** Polarity of the routed reset is true. **0x1: ASSERTED:** Polarity of the routed reset is inverted.
1 : 0	RES_SEL	The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES is '0' (compatible mode), this 2 bit field selects the RC routing input for the compatible reset scheme. When the ALT RES bit is '1', these bits are not used. Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.52 UDB_P0_U0_CFG31

Reset control

Address: 0x400F305F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	RW
HW Access	R	R	R		R	R	R	R
Name	PLD1_RES_POL	PLD0_RES_POL	EXT_CK_SEL [5:4]		EN_RES_DP	EN_RES_STAT	EXT_SYNC	ALT_RES

Bits	Name	Description
7	PLD1_RES_POL	Not connected. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Default Value: 0 **0x0: NOINV:** Not Used **0x1: INVERT:** Not Used
6	PLD0_RES_POL	The meaning of this bit depends on the value of ALT RES. When ALT RES (CFG31) is '1', this bit controls the polarity of the selected PLD0 routed reset. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Default Value: 0 **0x0: NOINV:** Routed reset to the PLD0/PLD1 block is true polarity. **0x1: INVERT:** Routed reset to the PLD0/PLD1 block is inverted polarity.
5 : 4	EXT_CK_SEL	External clock selection Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]
3	EN_RES_DP	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the Datapath block. Default Value: 0 **0x0: DISABLE:** Routed reset to the Datapath block is gated off. **0x1: ENABLE:** Routed reset to the Datapath block is on. ALT RES must be '1' and routed reset must be selected in CFG26

36.1.52 UDB_P0_U0_CFG31 (continued)

2	EN_RES_STAT	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the status register. Default Value: 0 **0x0: NEGATED:** Status register routed reset is gated off **0x1: ASSERTED:** Status register routed reset is on
1	EXT_SYNC	Enable synchronization of selected external clock Default Value: 0 **0x0: DISABLE:** Selected external clock input is not synchronized **0x1: ENABLE:** Selected external clock input is synchronized
0	ALT_RES	This bit toggles between two reset configurations. When this bit is '0', one routed reset is shared by all components in this UDB (compatible mode). When this bit is a 1, each block can select a unique routed reset from the available RC inputs. Default Value: 0 **0x0: COMPATIBLE:** All UDB blocks share a common routed reset. **0x1: ALTERNATE:** Each UDB component block can select and control its individual routed reset.

36.1.53 UDB_P0_U0_DCFG0

Dynamic Configuration RAM

Address: 0x400F3060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.53 UDB_P0_U0_DCFG0 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.53 UDB_P0_U0_DCFG0 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.54 UDB_P0_U0_DCFG1

Dynamic Configuration RAM

Address: 0x400F3062

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.54 UDB_P0_U0_DCFG1 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.54 UDB_P0_U0_DCFG1 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.55 UDB_P0_U0_DCFG2

Dynamic Configuration RAM

Address: 0x400F3064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.55 UDB_P0_U0_DCFG2 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.55 UDB_P0_U0_DCFG2 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.56 UDB_P0_U0_DCFG3

Dynamic Configuration RAM

Address: 0x400F3066

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.56 UDB_P0_U0_DCFG3 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.56 UDB_P0_U0_DCFG3 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.57 UDB_P0_U0_DCFG4

Dynamic Configuration RAM

Address: 0x400F3068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.57 UDB_P0_U0_DCFG4 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.57 UDB_P0_U0_DCFG4 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.58 UDB_P0_U0_DCFG5

Dynamic Configuration RAM

Address: 0x400F306A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.58 UDB_P0_U0_DCFG5 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.58 UDB_P0_U0_DCFG5 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.59 UDB_P0_U0_DCFG6

Dynamic Configuration RAM

Address: 0x400F306C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.59 UDB_P0_U0_DCFG6 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.59 UDB_P0_U0_DCFG6 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.60 UDB_P0_U0_DCFG7

Dynamic Configuration RAM

Address: 0x400F306E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.60 UDB_P0_U0_DCFG7 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.60 UDB_P0_U0_DCFG7 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.61 UDB_P0_U1_PLD_IT0

PLD Input Terms

Address: 0x400F3080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.61 UDB_P0_U1_PLD_IT0 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.61 UDB_P0_U1_PLD_IT0 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.62 UDB_P0_U1_PLD_IT1

PLD Input Terms

Address: 0x400F3084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.62 UDB_P0_U1_PLD_IT1 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.62 UDB_P0_U1_PLD_IT1 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.63 UDB_P0_U1_PLD_IT2

PLD Input Terms

Address: 0x400F3088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.63 UDB_P0_U1_PLD_IT2 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.63 UDB_P0_U1_PLD_IT2 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.64 UDB_P0_U1_PLD_IT3

PLD Input Terms

Address: 0x400F308C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.64 UDB_P0_U1_PLD_IT3 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.64 UDB_P0_U1_PLD_IT3 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.65 UDB_P0_U1_PLD_IT4

PLD Input Terms

Address: 0x400F3090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.65 UDB_P0_U1_PLD_IT4 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.65 UDB_P0_U1_PLD_IT4 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.66 UDB_P0_U1_PLD_IT5

PLD Input Terms

Address: 0x400F3094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.66 UDB_P0_U1_PLD_IT5 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.66 UDB_P0_U1_PLD_IT5 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.67 UDB_P0_U1_PLD_IT6

PLD Input Terms

Address: 0x400F3098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.67 UDB_P0_U1_PLD_IT6 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.67 UDB_P0_U1_PLD_IT6 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.68 UDB_P0_U1_PLD_IT7

PLD Input Terms

Address: 0x400F309C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.68 UDB_P0_U1_PLD_IT7 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.68 UDB_P0_U1_PLD_IT7 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.69 UDB_P0_U1_PLD_IT8

PLD Input Terms

Address: 0x400F30A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.69 UDB_P0_U1_PLD_IT8 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.69 UDB_P0_U1_PLD_IT8 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.70 UDB_P0_U1_PLD_IT9

PLD Input Terms

Address: 0x400F30A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.70 UDB_P0_U1_PLD_IT9 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.70 UDB_P0_U1_PLD_IT9 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.71 UDB_P0_U1_PLD_IT10

PLD Input Terms

Address: 0x400F30A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.71 UDB_P0_U1_PLD_IT10 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.71 UDB_P0_U1_PLD_IT10 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.72 UDB_P0_U1_PLD_IT11

PLD Input Terms

Address: 0x400F30AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.72 UDB_P0_U1_PLD_IT11 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.72 UDB_P0_U1_PLD_IT11 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.73 UDB_P0_U1_PLD_ORT0

PLD OR Terms

Address: 0x400F30B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

36.1.73 UDB_P0_U1_PLD_ORT0 (continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.74 UDB_P0_U1_PLD_ORT1

PLD OR Terms

Address: 0x400F30B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

36.1.74 UDB_P0_U1_PLD_ORT1 (continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.75 UDB_P0_U1_PLD_ORT2

PLD OR Terms

Address: 0x400F30B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

36.1.75 UDB_P0_U1_PLD_ORT2 (continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.76 UDB_P0_U1_PLD_ORT3

PLD OR Terms

Address: 0x400F30B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

36.1.76 UDB_P0_U1_PLD_ORT3 (continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.77 UDB_P0_U1_PLD_MC_CFG_CEN_CONST

Macrocell configuration for Carry Enable and Constant

Address: 0x400F30B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_DFF_C	PLD0_MC3_CEN	PLD0_MC2_DFF_C	PLD0_MC2_CEN	PLD0_MC1_DFF_C	PLD0_MC1_CEN	PLD0_MC0_DFF_C	PLD0_MC0_CEN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_DFF_C	PLD1_MC3_CEN	PLD1_MC2_DFF_C	PLD1_MC2_CEN	PLD1_MC1_DFF_C	PLD1_MC1_CEN	PLD1_MC0_DFF_C	PLD1_MC0_CEN

Bits	Name	Description
15	PLD1_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
14	PLD1_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
13	PLD1_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
12	PLD1_MC2_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

36.1.77 UDB_P0_U1_PLD_MC_CFG_CEN_CONST (continued)

11	PLD1_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
10	PLD1_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
9	PLD1_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
8	PLD1_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
7	PLD0_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
6	PLD0_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
5	PLD0_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
4	PLD0_MC2_CEN	Carry enable Default Value: X

36.1.77 UDB_P0_U1_PLD_MC_CFG_CEN_CONST (continued)

		0x0: DISABLE: Disabled **0x1: ENABLE:** Enabled
3	PLD0_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
2	PLD0_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
1	PLD0_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
0	PLD0_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

36.1.78 UDB_P0_U1_PLD_MC_CFG_XORFB

PLD Macro cell XOR feedback

Address: 0x400F30BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD0_MC3_XORFB [7:6]		PLD0_MC2_XORFB [5:4]		PLD0_MC1_XORFB [3:2]		PLD0_MC0_XORFB [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD1_MC3_XORFB [15:14]		PLD1_MC2_XORFB [13:12]		PLD1_MC1_XORFB [11:10]		PLD1_MC0_XORFB [9:8]	

Bits	Name	Description
15 : 14	PLD1_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
13 : 12	PLD1_MC2_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
11 : 10	PLD1_MC1_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry

36.1.78 UDB_P0_U1_PLD_MC_CFG_XORFB (continued)

		0x2: TFF_H: TFF on high **0x3: TFF_L:** TFF on low
9 : 8	PLD1_MC0_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
7 : 6	PLD0_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
5 : 4	PLD0_MC2_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
3 : 2	PLD0_MC1_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low

36.1.78 UDB_P0_U1_PLD_MC_CFG_XORFB (continued)

1 : 0	PLD0_MC0_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low

36.1.79 UDB_P0_U1_PLD_MC_SET_RESET

PLD Macro cell Set Reset Selection

Address: 0x400F30BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_RESET_SEL	PLD0_MC3_SET_SEL	PLD0_MC2_RESET_SEL	PLD0_MC2_SET_SEL	PLD0_MC1_RESET_SEL	PLD0_MC1_SET_SEL	PLD0_MC0_RESET_SEL	PLD0_MC0_SET_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_RESET_SEL	PLD1_MC3_SET_SEL	PLD1_MC2_RESET_SEL	PLD1_MC2_SET_SEL	PLD1_MC1_RESET_SEL	PLD1_MC1_SET_SEL	PLD1_MC0_RESET_SEL	PLD1_MC0_SET_SEL

Bits	Name	Description
15	PLD1_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
14	PLD1_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
13	PLD1_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
12	PLD1_MC2_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

36.1.79 UDB_P0_U1_PLD_MC_SET_RESET (continued)

11	PLD1_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
10	PLD1_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
9	PLD1_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
8	PLD1_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
7	PLD0_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
6	PLD0_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
5	PLD0_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
4	PLD0_MC2_SET_SEL	Set select enable Default Value: X

36.1.79 UDB_P0_U1_PLD_MC_SET_RESET (continued)

		0x0: DISABLE: Set not used **0x1: ENABLE:** Set enabled
3	PLD0_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
2	PLD0_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
1	PLD0_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
0	PLD0_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

36.1.80 UDB_P0_U1_PLD_MC_CFG_BYPASS

PLD Macro cell Bypass control

Address: 0x400F30BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	NC7	PLD0_MC3_BYPASS	NC5	PLD0_MC2_BYPASS	NC3	PLD0_MC1_BYPASS	NC1	PLD0_MC0_BYPASS

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	NC15	PLD1_MC3_BYPASS	NC13	PLD1_MC2_BYPASS	NC11	PLD1_MC1_BYPASS	NC9	PLD1_MC0_BYPASS

Bits	Name	Description
15	NC15	Spare register bit Default Value: X
14	PLD1_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
13	NC13	Spare register bit Default Value: X
12	PLD1_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
11	NC11	Spare register bit Default Value: X
10	PLD1_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output

36.1.80 UDB_P0_U1_PLD_MC_CFG_BYPASS (continued)

9	NC9	Spare register bit Default Value: X
8	PLD1_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
7	NC7	Spare register bit Default Value: X
6	PLD0_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
5	NC5	Spare register bit Default Value: X
4	PLD0_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
3	NC3	Spare register bit Default Value: X
2	PLD0_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
1	NC1	Spare register bit Default Value: X
0	PLD0_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output

36.1.81 UDB_P0_U1_CFG0

Datapath Input Selection - RAD1 RAD0. Address bits 0 and 1 to the dynamic configuration RAM

Address: 0x400F30C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	RAD1 [6:4]			None	RAD0 [2:0]		

Bits	Name	Description
6 : 4	RAD1	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	RAD0	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

36.1.81 UDB_P0_U1_CFG0 (continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.82 UDB_P0_U1_CFG1

Datapath Input Selection - RAD2. Address bit 2 to the dynamic configuration RAM

Address: 0x400F30C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW		
HW Access	R	R	R	R	R	R		
Name	DP_RTE_BYPASS4	DP_RTE_BYPASS3	DP_RTE_BYPASS2	DP_RTE_BYPASS1	DP_RTE_BYPASS0	RAD2 [2:0]		

Bits	Name	Description
7	DP_RTE_BYPASS4	DP_In bypass control Default Value: 0 **0x0: DP_IN4_ROUTE:** Use dp_in[4] **0x1: DP_IN4_BYPASS:** Use dp_out[4] as input via bypass
6	DP_RTE_BYPASS3	DP_In bypass control Default Value: 0 **0x0: DP_IN3_ROUTE:** Use dp_in[3] **0x1: DP_IN3_BYPASS:** Use dp_out[3] as input via bypass
5	DP_RTE_BYPASS2	DP_In bypass control Default Value: 0 **0x0: DP_IN2_ROUTE:** Use dp_in[2] **0x1: DP_IN2_BYPASS:** Use dp_out[2] as input via bypass
4	DP_RTE_BYPASS1	DP_In bypass control Default Value: 0 **0x0: DP_IN1_ROUTE:** Use dp_in[1] **0x1: DP_IN1_BYPASS:** Use dp_out[1] as input via bypass
3	DP_RTE_BYPASS0	DP_In bypass control Default Value: 0 **0x0: DP_IN0_ROUTE:** Use dp_in[0] **0x1: DP_IN0_BYPASS:** Use dp_out[0] as input via bypass

36.1.82 UDB_P0_U1_CFG1 (continued)

2 : 0	RAD2	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved

36.1.83 UDB_P0_U1_CFG2

Datapath Input Selection - F1_LD, F0_LD.

Address: 0x400F30C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	NC7	F1_LD [6:4]			DP_RTE_BYPASS5	F0_LD [2:0]		

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6 : 4	F1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
3	DP_RTE_BYPASS5	DP_In bypass control Default Value: 0 **0x0: DP_IN5_ROUTE:** Use dp_in[5] **0x1: DP_IN5_BYPASS:** Use dp_out[5] via bypass
2 : 0	F0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off

36.1.83 UDB_P0_U1_CFG2 (continued)

0x1: DP_IN0:
Set to dp_in[0]

0x2: DP_IN1:
Set to dp_in[1]

0x3: DP_IN2:
Set to dp_in[2]

0x4: DP_IN3:
Set to dp_in[3]

0x5: DP_IN4:
Set to dp_in[4]

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.84 UDB_P0_U1_CFG3

Datapath Input Selection - D1_LD, D0_LD.

Address: 0x400F30C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	D1_LD [6:4]			None	D0_LD [2:0]		

Bits	Name	Description
6 : 4	D1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	D0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

36.1.84 UDB_P0_U1_CFG3 (continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.85 UDB_P0_U1_CFG4

Datapath Input Selection - CI_MUX SI_MUX.

Address: 0x400F30C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	CI_MUX [6:4]			None	SI_MUX [2:0]		

Bits	Name	Description
6 : 4	CI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	SI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

36.1.85 UDB_P0_U1_CFG4 (continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.86 UDB_P0_U1_CFG5

Datapath Output Selection for OUT1 OUT0

Address: 0x400F30C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT1 [7:4]				OUT0 [3:0]			

Bits	Name	Description
7 : 4	OUT1	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

36.1.86 UDB_P0_U1_CFG5 (continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT0	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.87 UDB_P0_U1_CFG6

Datapath Output Selection for OUT3 OUT2

Address: 0x400F30C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT3 [7:4]				OUT2 [3:0]			

Bits	Name	Description
7 : 4	OUT3	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

36.1.87 UDB_P0_U1_CFG6 (continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT2	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.88 UDB_P0_U1_CFG7

Datapath Output Selection for OUT5 OUT4

Address: 0x400F30C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT5 [7:4]				OUT4 [3:0]			

Bits	Name	Description
7 : 4	OUT5	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

36.1.88 UDB_P0_U1_CFG7 (continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT4	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.89 UDB_P0_U1_CFG8

Datapath Output Synchronization Option

Address: 0x400F30C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW					
HW Access	R	R	R					
Name	NC7	NC6	OUT_SYNC [5:0]					

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6	NC6	Spare register bit Default Value: 0
5 : 0	OUT_SYNC	Datapath Output Synchronization. Each datapath output can be registered (default,0), or combinational (1) Default Value: 0 **0x0: REGISTERED:** registered **0x1: COMBINATIONAL:** combinational

36.1.90 UDB_P0_U1_CFG9

Datapath ALU Mask

Address: 0x400F30C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	AMASK [7:0]							

Bits	Name	Description
7 : 0	AMASK	Datapath ALU Mask. The mask value in this register is applied to the output of the Datapath ALU result before the result is stored. The AMASK_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.91 UDB_P0_U1_CFG10

Datapath Compare 0 Mask

Address: 0x400F30CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMASK0 [7:0]							

Bits	Name	Description
7 : 0	CMASK0	Datapath Compare 0 Mask. The mask value in this register is applied to the output of the Accumulator 0 before it is used for comparison in Compare block 0. The CMASK0_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.92 UDB_P0_U1_CFG11

Datapath Compare 1 Mask

Address: 0x400F30CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMASK0 [7:0]							

Bits	Name	Description
7 : 0	CMASK0	Datapath Compare 1 Mask. The mask value in this register is applied to the selected Compare 1 block input (Accumulator 0 or Accumulator 1) before it is used for comparison. The CMASK1_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.93 UDB_P0_U1_CFG12

Datapath mask enables and shift in configuration

Address: 0x400F30CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	CMASK1_EN	CMASK0_EN	AMASK_EN	DEF_SI	SI_SELB [3:2]		SI_SELA [1:0]	

Bits	Name	Description
7	CMASK1_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
6	CMASK0_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
5	AMASK_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
4	DEF_SI	Datapath default shift value Default Value: 0 **0x0: DEFAULT_0:** Default shift is 0 **0x1: DEFAULT_1:** Default shift is 1
3 : 2	SI_SELB	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle

36.1.93 UDB_P0_U1_CFG12 (continued)

		0x2: ROUTE: Shift in is selected from datapath routing input **0x3: CHAIN:** Shift in is chained from the previous datapath
1 : 0	SI_SELA	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle **0x2: ROUTE:** Shift in is selected from datapath routing input **0x3: CHAIN:** Shift in is chained from the previous datapath

36.1.94 UDB_P0_U1_CFG13

Datapath carry in and compare configuration

Address: 0x400F30CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CMP_SELB [7:6]		CMP_SELA [5:4]		CI_SELB [3:2]		CI_SELA [1:0]	

Bits	Name	Description
7 : 6	CMP_SELB	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
5 : 4	CMP_SELA	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
3 : 2	CI_SELB	Datapath carry in source select Default Value: 0 **0x0: DEFAULT:** Default arithmetic mode **0x1: REGISTERED:** Carry in is the carry out registered from previous cycle **0x2: ROUTE:** Carry in is selected from datapath routing input **0x3: CHAIN:** Carry in is chained from the previous datapath
1 : 0	CI_SELA	Datapath carry in source select Default Value: 0

36.1.94 UDB_P0_U1_CFG13 (continued)

0x0: DEFAULT:
Default arithmetic mode

0x1: REGISTERED:
Carry in is the carry out registered from previous cycle

0x2: ROUTE:
Carry in is selected from datapath routing input

0x3: CHAIN:
Carry in is chained from the previous datapath

36.1.95 UDB_P0_U1_CFG14

Datapath chaining and MSB configuration

Address: 0x400F30CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW	RW	RW
HW Access	R	R			R	R	R	R
Name	MSB_EN	MSB_SEL [6:4]			CHAIN_CMSB	CHAIN_FB	CHAIN1	CHAIN0

Bits	Name	Description
7	MSB_EN	Datapath MSB selection enable Default Value: 0 **0x0: DISABLE:** MSB selection is disabled, MSB is bit 7 **0x1: ENABLE:** MSB selection is controlled by MSB_SEL
6 : 4	MSB_SEL	Datapath MSB Selection Default Value: 0 **0x0: BIT0:** MSB is bit 0 **0x1: BIT1:** MSB is bit 1 **0x2: BIT2:** MSB is bit 2 **0x3: BIT3:** MSB is bit 3 **0x4: BIT4:** MSB is bit 4 **0x5: BIT5:** MSB is bit 5 **0x6: BIT6:** MSB is bit 6 **0x7: BIT7:** MSB is bit 7 - equivalent to MSB_EN=0
3	CHAIN_CMSB	Datapath CRC MSB chaining enable Default Value: 0 **0x0: DISABLE:** CRC MSB is not chained **0x1: ENABLE:** CRC MSB is chained from the next (MSB) datapath

36.1.95 UDB_P0_U1_CFG14 (continued)

2	CHAIN_FB	Datapath CRC feedback chaining enable Default Value: 0 **0x0: DISABLE:** CRC feedback is not chained **0x1: ENABLE:** CRC feedback is chained from the previous (LSB) datapath
1	CHAIN1	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath
0	CHAIN0	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath

36.1.96 UDB_P0_U1_CFG15

Datapath FIFO, shift and parallel input control

Address: 0x400F30CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	PI_SEL	SHIFT_SEL	PI_DYN	MSB_SI	F1_INSEL [3:2]		F0_INSEL [1:0]	

Bits	Name	Description
7	PI_SEL	Datapath parallel input selection Default Value: 0 **0x0: NORMAL:** Normal operation, ALU source is from accumulator selection **0x1: PARALLEL:** ALU source A input is from the parallel data input
6	SHIFT_SEL	Datapath shift out selection Default Value: 0 **0x0: SOL_MSB:** Routed shift out is shift out left (sol_msb) **0x1: SOR:** Routed shift out is shift out right (sor)
5	PI_DYN	Enable for dynamic control of parallel data input (PI) mux. Default Value: 0 **0x0: DISABLE:** Parallel input mux select is only controlled by static configuration (PI_SEL). **0x1: ENABLE:** Parallel input mux to the Datapath is controlled by CFB_EN field in Datapath Dynamic RAM. When this mode is enabled, the CFB_EN usage for CRC/PRS functionality is disabled.
4	MSB_SI	Arithmetic shift right operation shift in selection Default Value: 0 **0x0: DEFAULT:** Shift in default value (when SI_SELA and/or SI_SELB == 0) **0x1: MSB:** Override default and shift in MSB value
3 : 2	F1_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus

36.1.96 UDB_P0_U1_CFG15 (continued)

		0x2: OUTPUT_A1: Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus
1 : 0	F0_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus **0x2: OUTPUT_A1:** Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus

36.1.97 UDB_P0_U1_CFG16

Datapath FIFO and register access configuration control

Address: 0x400F30D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	F1_CK_INV	F0_CK_INV	FIFO_FAST	FIFO_CAP	FIFO_EDGE	FIFO_ASYNC	EXT_CRCPRS	WRK16_CONCAT

Bits	Name	Description
7	F1_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
6	F0_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
5	FIFO_FAST	FIFO Fast Mode. When this bit is set, the FIFO write logic is clocked by the application bus clock. Lowers the latency of capture timing, at the expense of additional power. Default Value: 0 **0x0: DISABLE:** FIFO is clocked with selected Datapath clock. **0x1: ENABLE:** FIFO is clocked with application bus clock. Master and quadrant bus clock gating must be enabled.
4	FIFO_CAP	FIFO Software Capture Mode. When this bit is set, a read of A0 or A1 triggers a capture into F0 or F1 respectively. This function follows the chaining configuration. All accumulators in the chain from a given block to the MS block in the chain are capture Default Value: 0 **0x0: DISABLE:** FIFO capture is disabled. **0x1: ENABLE:** FIFO capture is enabled (FIFO must be in output mode). A read of A0 or A1 will write into F0 or F1.
3	FIFO_EDGE	Edge/level sensitive FIFO write control (Fx_LD). Only applies to FIFO configured in output mode Default Value: 0

36.1.97 UDB_P0_U1_CFG16 (continued)

		0x0: LEVEL: FIFO write from accumulators/ALU is level sensitive. FIFO write occurs on a clock edge whenever the write control is sampled high on that edge. **0x1: EDGE:** FIFO write from accumulators/ALU is edge sensitive. FIFO write occurs on a clock edge folloing a 0 to 1 transition on the write control. The write control must be negated for at least one full cycle of the FIFO clock for a subsequent transition to be dete
2	FIFO_ASYNC	Asynchronous FIFO clocking support Default Value: 0 **0x0: DISABLE:** FIFO clocks are synchronous **0x1: ENABLE:** FIFO clocks are asynchronous
1	EXT_CRCPRS	External CRC/PRS mode Default Value: 0 **0x0: INTERNAL:** Internal CRC/PRS routing **0x1: EXTERNAL:** External CRC/PRS routing
0	WRK16_CONCAT	Datapath register access mode Default Value: 0 **0x0: DEFAULT:** 16-bit default access mode: selects registers in two consecutive UDBs in chaining order **0x1: CONCATENATE:** 16-bit concat access mode: selects concatenated registers in a single UDB

36.1.98 UDB_P0_U1_CFG17

Datapath FIFO control

Address: 0x400F30D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			FIFO_ADD_SYNC	NC3	NC2	F1_DYN	F0_DYN

Bits	Name	Description
4	FIFO_ADD_SYNC	Adds an additional sync flip-flop to FIFO block status. Default Value: 0 **0x0: DISABLE:** Compatible Mode: FIFO block status sync configuration is 'none' (FIFO_ASYNC = 0) and 1 sync flip-flop (FIFO_ASYNC = 1) **0x1: ENABLE:** Add Sync Mode: FIFO block status sync configuration 1 sync flip-flop (FIFO_ASYNC = 0) and 2 sync flip-flops (FIFO_ASYNC = 1)
3	NC3	Spare register bit Default Value: 0
2	NC2	Spare register bit Default Value: 0
1	F1_DYN	Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest
0	F0_DYN	When this bit is set, the associated FIFO configuration may be dynamically controlled. Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest

36.1.99 UDB_P0_U1_CFG18

Control Register Mode 0 (used in conjunction with Control Register Mode 1)

Address: 0x400F30D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_MD0 [7:0]							

Bits	Name	Description
7 : 0	CTL_MD0	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

36.1.100 UDB_P0_U1_CFG19

Control Register Mode 1 (used in conjunction with Control Register Mode 0)

Address: 0x400F30D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_MD1 [7:0]							

Bits	Name	Description
7 : 0	CTL_MD1	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

36.1.101 UDB_P0_U1_CFG20

Status Register input mode selection

Address: 0x400F30D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	STAT_MD [7:0]							

Bits	Name	Description
7 : 0	STAT_MD	Mode selection for each bit of the status register. A '0' is transparent mode, where internal routing is read idrectly by CPU firmware. A '1' is sticky-clear-on-read mode, where once the given bit is set, it will stay set until the CPU reads the bit. Default Value: 0

36.1.102 UDB_P0_U1_CFG21

Spare register bits

Address: 0x400F30D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NC1	NC0

Bits	Name	Description
1	NC1	Spare register bit Default Value: 0
0	NC0	Spare register bit Default Value: 0

36.1.103 UDB_P0_U1_CFG22

SC block configuration control

Address: 0x400F30D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	
HW Access	None			R	R	R	R	
Name	None [7:5]			SC_EXT_RES	SC_SYNC_MD	SC_INT_MD	SC_OUT_CTL [1:0]	

Bits	Name	Description
4	SC_EXT_RES	Control register external reset operation. This bit supports autonomous usage of the control register, where a routed reset should clear the writable input registers. By default this is off because the CPU writable register can be cleared in firmware. Default Value: 0 **0x0: DISABLED:** When a routed reset is applied to the control register, only embedded state (sampling registers) are cleared **0x1: ENABLED:** When a routed reset is applied to the control register, all state is cleared, including the CPU writable control bits.
3	SC_SYNC_MD	SC Sync Mode - controls when the status register operates as a 4-bit double synchronizer module Default Value: 0 **0x0: NORMAL:** Normal Mode - Status register operation **0x1: SYNC_MODE:** Sync Mode - Routing inputs sc_in[3:0] are the 4 sync inputs, and connections sc_io[3:0] operate as the sync outputs
2	SC_INT_MD	SC Interrupt Mode - controls when the UDB driving an interrupt generated from the masked OR reduction of status bits 6 to 0 Default Value: 0 **0x0: NORMAL:** Normal Mode - Routing connection sc_io[3] is a normal input to the status register **0x1: INT_MODE:** Interrupt Mode - Routing connection sc_io[3] operates as the UDB interrupt output
1 : 0	SC_OUT_CTL	Selects the output source for the Status and Control routing connections Default Value: 0 **0x0: CONTROL:** Control out, 8-bits of control are driven to the routing connections **0x1: PARALLEL:** Datapath parallel output, 8-bits of datapath parallel output data are driven to the routing connections

36.1.103 UDB_P0_U1_CFG22 (continued)

0x2: COUNTER:
Counter out, 7-bits of count and 1 bit (MSB) of terminal count are driven to the routing connections

0x3: RESERVED:
Reserved

36.1.104 UDB_P0_U1_CFG23

Counter Control

Address: 0x400F30D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW		RW	
HW Access	None	R	R	R	R		R	
Name	None	ALT_CNT	ROUTE_EN	ROUTE_LD	CNT_EN_SEL [3:2]		CNT_LD_SEL [1:0]	

Bits	Name	Description
6	ALT_CNT	Configure the alternate operating mode of the counter Default Value: 0 **0x0: DEFAULT_MODE:** Default counter operating mode **0x1: ALT_MODE:** Alternate counter operating mode
5	ROUTE_EN	Configure the counter enable signal for routing input Default Value: 0 **0x0: DISABLE:** Routed EN signal is not used. EN signal is only controlled by firmware CNT START (ACTL register) **0x1: ROUTED:** Routed EN signal is used, CNT START must be set
4	ROUTE_LD	Configure the counter load signal for routing input Default Value: 0 **0x0: DISABLE:** Routed LD signal is not used **0x1: ROUTED:** Routed LD signal is used
3 : 2	CNT_EN_SEL	Selects the routing inputs for the counter enable signal Default Value: 0 **0x0: SC_IN4:** sc_io_in[0] **0x1: SC_IN5:** sc_io_in[1] **0x2: SC_IN6:** sc_io_in[2] **0x3: SC_IO:** sc_io_in[3]
1 : 0	CNT_LD_SEL	Selects the routing inputs for the counter load signal Default Value: 0

36.1.104 UDB_P0_U1_CFG23 (continued)

0x0: SC_IN0:
sc_in[0]

0x1: SC_IN1:
sc_in[1]

0x2: SC_IN2:
sc_in[2]

0x3: SC_IN3:
sc_in[3]

36.1.105 UDB_P0_U1_CFG24

PLD0 Clock and Reset control

Address: 0x400F30D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

36.1.105 UDB_P0_U1_CFG24 (continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.106 UDB_P0_U1_CFG25

PLD1 Clock and Reset control

Address: 0x400F30D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

36.1.106 UDB_P0_U1_CFG25 (continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.107 UDB_P0_U1_CFG26

Datapath Clock and Reset control

Address: 0x400F30DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

36.1.107 UDB_P0_U1_CFG26 (continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.108 UDB_P0_U1_CFG27

Status/Control Clock and Reset control

Address: 0x400F30DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

36.1.108 UDB_P0_U1_CFG27 (continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.109 UDB_P0_U1_CFG28

Clock Selection for PLD1 and PLD0

Address: 0x400F30DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PLD1_CK_SEL [7:4]				PLD0_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	PLD1_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	PLD0_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

36.1.109 UDB_P0_U1_CFG28 (continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

36.1.110 UDB_P0_U1_CFG29

Clock Selection for Datapath, Status and Control

Address: 0x400F30DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SC_CK_SEL [7:4]				DP_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	SC_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	DP_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

36.1.110 UDB_P0_U1_CFG29 (continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

36.1.111 UDB_P0_U1_CFG30

Reset control

Address: 0x400F30DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None	RW	RW	RW	RW	
HW Access	R	R	None	R	R	R	R	
Name	SC_RES_POL	DP_RES_POL	None	GUDB_WR	EN_RES_CNTCTL	RES_POL	RES_SEL [1:0]	

Bits	Name	Description
7	SC_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected SC routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Status and Control block is true polarity. **0x1: INVERT:** Routed reset to the Status and Control block is inverted polarity.
6	DP_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected Datapath routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Datapath block is true polarity. **0x1: INVERT:** Routed reset to the Datapath block is inverted polarity.
4	GUDB_WR	Enable global write operation for the configuration and working registers in this UDB. When this bit is set, the UDB ID select decoding is bypassed. Default Value: 0 **0x0: DISABLE:** Global UDB configuration/working register write is disabled **0x1: ENABLE:** Global UDB configuration/working register write is enabled
3	EN_RES_CNTCTL	This bit gates the routed reset to the counter/control register. By default, the operation is compatible, i.e., it only applies to the counter. However, if the updated control regisiter modes are used (sync mode, pulse mode, or the ext res bit) then the routed reset applies to the control register also. Default Value: 0 **0x0: DISABLE:** Routed reset is not applied to counter/control register **0x1: ENABLE:** Routed reset is applied to the counter/control register

36.1.111 UDB_P0_U1_CFG30 (continued)

2	RES_POL	The meaning of this bit depends on the value of the ALT RES bit in CFG31. When ALT RES is '0' (compatible mode), this bit sets the polarity of the routed reset. When ALT RES is '1', this bit is unused. Default Value: 0 **0x0: NEGATED:** Polarity of the routed reset is true. **0x1: ASSERTED:** Polarity of the routed reset is inverted.
1 : 0	RES_SEL	The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES is '0' (compatible mode), this 2 bit field selects the RC routing input for the compatible reset scheme. When the ALT RES bit is '1', these bits are not used. Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.112 UDB_P0_U1_CFG31

Reset control

Address: 0x400F30DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	RW
HW Access	R	R	R		R	R	R	R
Name	PLD1_RES_POL	PLD0_RES_POL	EXT_CK_SEL [5:4]		EN_RES_DP	EN_RES_STAT	EXT_SYNC	ALT_RES

Bits	Name	Description
7	PLD1_RES_POL	Not connected. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Default Value: 0 **0x0: NOINV:** Not Used **0x1: INVERT:** Not Used
6	PLD0_RES_POL	The meaning of this bit depends on the value of ALT RES. When ALT RES (CFG31) is '1', this bit controls the polarity of the selected PLD0 routed reset. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Default Value: 0 **0x0: NOINV:** Routed reset to the PLD0/PLD1 block is true polarity. **0x1: INVERT:** Routed reset to the PLD0/PLD1 block is inverted polarity.
5 : 4	EXT_CK_SEL	External clock selection Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]
3	EN_RES_DP	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the Datapath block. Default Value: 0 **0x0: DISABLE:** Routed reset to the Datapath block is gated off. **0x1: ENABLE:** Routed reset to the Datapath block is on. ALT RES must be '1' and routed reset must be selected in CFG26

36.1.112 UDB_P0_U1_CFG31 (continued)

2	EN_RES_STAT	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the status register. Default Value: 0 **0x0: NEGATED:** Status register routed reset is gated off **0x1: ASSERTED:** Status register routed reset is on
1	EXT_SYNC	Enable synchronization of selected external clock Default Value: 0 **0x0: DISABLE:** Selected external clock input is not synchronized **0x1: ENABLE:** Selected external clock input is synchronized
0	ALT_RES	This bit toggles between two reset configurations. When this bit is '0', one routed reset is shared by all components in this UDB (compatible mode). When this bit is a 1, each block can select a unique routed reset from the available RC inputs. Default Value: 0 **0x0: COMPATIBLE:** All UDB blocks share a common routed reset. **0x1: ALTERNATE:** Each UDB component block can select and control its individual routed reset.

36.1.113 UDB_P0_U1_DCFG0

Dynamic Configuration RAM

Address: 0x400F30E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.113 UDB_P0_U1_DCFG0 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.113 UDB_P0_U1_DCFG0 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.114 UDB_P0_U1_DCFG1

Dynamic Configuration RAM

Address: 0x400F30E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.114 UDB_P0_U1_DCFG1 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.114 UDB_P0_U1_DCFG1 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.115 UDB_P0_U1_DCFG2

Dynamic Configuration RAM

Address: 0x400F30E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.115 UDB_P0_U1_DCFG2 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.115 UDB_P0_U1_DCFG2 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.116 UDB_P0_U1_DCFG3

Dynamic Configuration RAM

Address: 0x400F30E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.116 UDB_P0_U1_DCFG3 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.116 UDB_P0_U1_DCFG3 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.117 UDB_P0_U1_DCFG4

Dynamic Configuration RAM

Address: 0x400F30E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.117 UDB_P0_U1_DCFG4 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.117 UDB_P0_U1_DCFG4 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.118 UDB_P0_U1_DCFG5

Dynamic Configuration RAM

Address: 0x400F30EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.118 UDB_P0_U1_DCFG5 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.118 UDB_P0_U1_DCFG5 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.119 UDB_P0_U1_DCFG6

Dynamic Configuration RAM

Address: 0x400F30EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.119 UDB_P0_U1_DCFG6 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.119 UDB_P0_U1_DCFG6 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.120 UDB_P0_U1_DCFG7

Dynamic Configuration RAM

Address: 0x400F30EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.120 UDB_P0_U1_DCFG7 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.120 UDB_P0_U1_DCFG7 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.121 UDB_P1_U0_PLD_IT0

PLD Input Terms

Address: 0x400F3200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.121 UDB_P1_U0_PLD_IT0 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.121 UDB_P1_U0_PLD_IT0 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.122 UDB_P1_U0_PLD_IT1

PLD Input Terms

Address: 0x400F3204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.122 UDB_P1_U0_PLD_IT1 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.122 UDB_P1_U0_PLD_IT1 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.123 UDB_P1_U0_PLD_IT2

PLD Input Terms

Address: 0x400F3208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.123 UDB_P1_U0_PLD_IT2 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.123 UDB_P1_U0_PLD_IT2 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.124 UDB_P1_U0_PLD_IT3

PLD Input Terms

Address: 0x400F320C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.124 UDB_P1_U0_PLD_IT3 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.124 UDB_P1_U0_PLD_IT3 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.125 UDB_P1_U0_PLD_IT4

PLD Input Terms

Address: 0x400F3210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.125 UDB_P1_U0_PLD_IT4 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.125 UDB_P1_U0_PLD_IT4 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.126 UDB_P1_U0_PLD_IT5

PLD Input Terms

Address: 0x400F3214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.126 UDB_P1_U0_PLD_IT5 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.126 UDB_P1_U0_PLD_IT5 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.127 UDB_P1_U0_PLD_IT6

PLD Input Terms

Address: 0x400F3218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.127 UDB_P1_U0_PLD_IT6 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.127 UDB_P1_U0_PLD_IT6 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.128 UDB_P1_U0_PLD_IT7

PLD Input Terms

Address: 0x400F321C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.128 UDB_P1_U0_PLD_IT7 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.128 UDB_P1_U0_PLD_IT7 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.129 UDB_P1_U0_PLD_IT8

PLD Input Terms

Address: 0x400F3220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.129 UDB_P1_U0_PLD_IT8 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.129 UDB_P1_U0_PLD_IT8 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.130 UDB_P1_U0_PLD_IT9

PLD Input Terms

Address: 0x400F3224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.130 UDB_P1_U0_PLD_IT9 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.130 UDB_P1_U0_PLD_IT9 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.131 UDB_P1_U0_PLD_IT10

PLD Input Terms

Address: 0x400F3228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.131 UDB_P1_U0_PLD_IT10 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.131 UDB_P1_U0_PLD_IT10 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.132 UDB_P1_U0_PLD_IT11

PLD Input Terms

Address: 0x400F322C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.132 UDB_P1_U0_PLD_IT11 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.132 UDB_P1_U0_PLD_IT11 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.133 UDB_P1_U0_PLD_ORT0

PLD OR Terms

Address: 0x400F3230

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

36.1.133 UDB_P1_U0_PLD_ORT0 (continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.134 UDB_P1_U0_PLD_ORT1

PLD OR Terms

Address: 0x400F3232

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

36.1.134 UDB_P1_U0_PLD_ORT1 (continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.135 UDB_P1_U0_PLD_ORT2

PLD OR Terms

Address: 0x400F3234

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

36.1.135 UDB_P1_U0_PLD_ORT2 (continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.136 UDB_P1_U0_PLD_ORT3

PLD OR Terms

Address: 0x400F3236

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

36.1.136 UDB_P1_U0_PLD_ORT3 (continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.137 UDB_P1_U0_PLD_MC_CFG_CEN_CONST

Macrocell configuration for Carry Enable and Constant

Address: 0x400F3238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_DFF_C	PLD0_MC3_CEN	PLD0_MC2_DFF_C	PLD0_MC2_CEN	PLD0_MC1_DFF_C	PLD0_MC1_CEN	PLD0_MC0_DFF_C	PLD0_MC0_CEN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_DFF_C	PLD1_MC3_CEN	PLD1_MC2_DFF_C	PLD1_MC2_CEN	PLD1_MC1_DFF_C	PLD1_MC1_CEN	PLD1_MC0_DFF_C	PLD1_MC0_CEN

Bits	Name	Description
15	PLD1_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
14	PLD1_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
13	PLD1_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
12	PLD1_MC2_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

36.1.137 UDB_P1_U0_PLD_MC_CFG_CEN_CONST (continued)

11	PLD1_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
10	PLD1_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
9	PLD1_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
8	PLD1_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
7	PLD0_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
6	PLD0_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
5	PLD0_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
4	PLD0_MC2_CEN	Carry enable Default Value: X

36.1.137 UDB_P1_U0_PLD_MC_CFG_CEN_CONST (continued)

		0x0: DISABLE: Disabled **0x1: ENABLE:** Enabled
3	PLD0_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
2	PLD0_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
1	PLD0_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
0	PLD0_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

36.1.138 UDB_P1_U0_PLD_MC_CFG_XORFB

PLD Macro cell XOR feedback

Address: 0x400F323A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD0_MC3_XORFB [7:6]		PLD0_MC2_XORFB [5:4]		PLD0_MC1_XORFB [3:2]		PLD0_MC0_XORFB [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD1_MC3_XORFB [15:14]		PLD1_MC2_XORFB [13:12]		PLD1_MC1_XORFB [11:10]		PLD1_MC0_XORFB [9:8]	

Bits	Name	Description
15 : 14	PLD1_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
13 : 12	PLD1_MC2_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
11 : 10	PLD1_MC1_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry

36.1.138 UDB_P1_U0_PLD_MC_CFG_XORFB (continued)

		0x2: TFF_H: TFF on high **0x3: TFF_L:** TFF on low
9 : 8	PLD1_MC0_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
7 : 6	PLD0_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
5 : 4	PLD0_MC2_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
3 : 2	PLD0_MC1_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low

36.1.138 UDB_P1_U0_PLD_MC_CFG_XORFB (continued)

1 : 0	PLD0_MC0_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low

36.1.139 UDB_P1_U0_PLD_MC_SET_RESET

PLD Macro cell Set Reset Selection

Address: 0x400F323C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_RESET_SEL	PLD0_MC3_SET_SEL	PLD0_MC2_RESET_SEL	PLD0_MC2_SET_SEL	PLD0_MC1_RESET_SEL	PLD0_MC1_SET_SEL	PLD0_MC0_RESET_SEL	PLD0_MC0_SET_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_RESET_SEL	PLD1_MC3_SET_SEL	PLD1_MC2_RESET_SEL	PLD1_MC2_SET_SEL	PLD1_MC1_RESET_SEL	PLD1_MC1_SET_SEL	PLD1_MC0_RESET_SEL	PLD1_MC0_SET_SEL

Bits	Name	Description
15	PLD1_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
14	PLD1_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
13	PLD1_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
12	PLD1_MC2_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

36.1.139 UDB_P1_U0_PLD_MC_SET_RESET (continued)

11	PLD1_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
10	PLD1_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
9	PLD1_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
8	PLD1_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
7	PLD0_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
6	PLD0_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
5	PLD0_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
4	PLD0_MC2_SET_SEL	Set select enable Default Value: X

36.1.139 UDB_P1_U0_PLD_MC_SET_RESET (continued)

		0x0: DISABLE: Set not used **0x1: ENABLE:** Set enabled
3	PLD0_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
2	PLD0_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
1	PLD0_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
0	PLD0_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

36.1.140 UDB_P1_U0_PLD_MC_CFG_BYPASS

PLD Macro cell Bypass control

Address: 0x400F323E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	NC7	PLD0_MC3_BYPASS	NC5	PLD0_MC2_BYPASS	NC3	PLD0_MC1_BYPASS	NC1	PLD0_MC0_BYPASS

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	NC15	PLD1_MC3_BYPASS	NC13	PLD1_MC2_BYPASS	NC11	PLD1_MC1_BYPASS	NC9	PLD1_MC0_BYPASS

Bits	Name	Description
15	NC15	Spare register bit Default Value: X
14	PLD1_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
13	NC13	Spare register bit Default Value: X
12	PLD1_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
11	NC11	Spare register bit Default Value: X
10	PLD1_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output

36.1.140 UDB_P1_U0_PLD_MC_CFG_BYPASS (continued)

9	NC9	Spare register bit Default Value: X
8	PLD1_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
7	NC7	Spare register bit Default Value: X
6	PLD0_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
5	NC5	Spare register bit Default Value: X
4	PLD0_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
3	NC3	Spare register bit Default Value: X
2	PLD0_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
1	NC1	Spare register bit Default Value: X
0	PLD0_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output

36.1.141 UDB_P1_U0_CFG0

Datapath Input Selection - RAD1 RAD0. Address bits 0 and 1 to the dynamic configuration RAM

Address: 0x400F3240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	RAD1 [6:4]			None	RAD0 [2:0]		

Bits	Name	Description
6 : 4	RAD1	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	RAD0	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

36.1.141 UDB_P1_U0_CFG0 (continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.142 UDB_P1_U0_CFG1

Datapath Input Selection - RAD2. Address bit 2 to the dynamic configuration RAM

Address: 0x400F3241

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW		
HW Access	R	R	R	R	R	R		
Name	DP_RTE_BYPASS4	DP_RTE_BYPASS3	DP_RTE_BYPASS2	DP_RTE_BYPASS1	DP_RTE_BYPASS0	RAD2 [2:0]		

Bits	Name	Description
7	DP_RTE_BYPASS4	DP_In bypass control Default Value: 0 **0x0: DP_IN4_ROUTE:** Use dp_in[4] **0x1: DP_IN4_BYPASS:** Use dp_out[4] as input via bypass
6	DP_RTE_BYPASS3	DP_In bypass control Default Value: 0 **0x0: DP_IN3_ROUTE:** Use dp_in[3] **0x1: DP_IN3_BYPASS:** Use dp_out[3] as input via bypass
5	DP_RTE_BYPASS2	DP_In bypass control Default Value: 0 **0x0: DP_IN2_ROUTE:** Use dp_in[2] **0x1: DP_IN2_BYPASS:** Use dp_out[2] as input via bypass
4	DP_RTE_BYPASS1	DP_In bypass control Default Value: 0 **0x0: DP_IN1_ROUTE:** Use dp_in[1] **0x1: DP_IN1_BYPASS:** Use dp_out[1] as input via bypass
3	DP_RTE_BYPASS0	DP_In bypass control Default Value: 0 **0x0: DP_IN0_ROUTE:** Use dp_in[0] **0x1: DP_IN0_BYPASS:** Use dp_out[0] as input via bypass

36.1.142 UDB_P1_U0_CFG1 (continued)

2 : 0	RAD2	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved

36.1.143 UDB_P1_U0_CFG2

Datapath Input Selection - F1_LD, F0_LD.

Address: 0x400F3242

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	NC7	F1_LD [6:4]			DP_RTE_BYPASS5	F0_LD [2:0]		

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6 : 4	F1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
3	DP_RTE_BYPASS5	DP_In bypass control Default Value: 0 **0x0: DP_IN5_ROUTE:** Use dp_in[5] **0x1: DP_IN5_BYPASS:** Use dp_out[5] via bypass
2 : 0	F0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off

36.1.143 UDB_P1_U0_CFG2 (continued)

0x1: DP_IN0:
Set to dp_in[0]

0x2: DP_IN1:
Set to dp_in[1]

0x3: DP_IN2:
Set to dp_in[2]

0x4: DP_IN3:
Set to dp_in[3]

0x5: DP_IN4:
Set to dp_in[4]

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.144 UDB_P1_U0_CFG3

Datapath Input Selection - D1_LD, D0_LD.

Address: 0x400F3243

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	D1_LD [6:4]			None	D0_LD [2:0]		

Bits	Name	Description
6 : 4	D1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	D0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

36.1.144 UDB_P1_U0_CFG3 (continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.145 UDB_P1_U0_CFG4

Datapath Input Selection - CI_MUX SI_MUX.

Address: 0x400F3244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	CI_MUX [6:4]			None	SI_MUX [2:0]		

Bits	Name	Description
6 : 4	CI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	SI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

36.1.145 UDB_P1_U0_CFG4 (continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.146 UDB_P1_U0_CFG5

Datapath Output Selection for OUT1 OUT0

Address: 0x400F3245

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT1 [7:4]				OUT0 [3:0]			

Bits	Name	Description
7 : 4	OUT1	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

36.1.146 UDB_P1_U0_CFG5 (continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT0	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.147 UDB_P1_U0_CFG6

Datapath Output Selection for OUT3 OUT2

Address: 0x400F3246

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT3 [7:4]				OUT2 [3:0]			

Bits	Name	Description
7 : 4	OUT3	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

36.1.147 UDB_P1_U0_CFG6 (continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT2	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.148 UDB_P1_U0_CFG7

Datapath Output Selection for OUT5 OUT4

Address: 0x400F3247

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT5 [7:4]				OUT4 [3:0]			

Bits	Name	Description
7 : 4	OUT5	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

36.1.148 UDB_P1_U0_CFG7 (continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT4	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.149 UDB_P1_U0_CFG8

Datapath Output Synchronization Option

Address: 0x400F3248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW					
HW Access	R	R	R					
Name	NC7	NC6	OUT_SYNC [5:0]					

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6	NC6	Spare register bit Default Value: 0
5 : 0	OUT_SYNC	Datapath Output Synchronization. Each datapath output can be registered (default,0), or combinational (1) Default Value: 0 **0x0: REGISTERED:** registered **0x1: COMBINATIONAL:** combinational

36.1.150 UDB_P1_U0_CFG9

Datapath ALU Mask

Address: 0x400F3249

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	AMASK [7:0]							

Bits	Name	Description
7 : 0	AMASK	Datapath ALU Mask. The mask value in this register is applied to the output of the Datapath ALU result before the result is stored. The AMASK_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.151 UDB_P1_U0_CFG10

Datapath Compare 0 Mask

Address: 0x400F324A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMASK0 [7:0]							

Bits	Name	Description
7 : 0	CMASK0	Datapath Compare 0 Mask. The mask value in this register is applied to the output of the Accumulator 0 before it is used for comparison in Compare block 0. The CMASK0_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.152 UDB_P1_U0_CFG11

Datapath Compare 1 Mask

Address: 0x400F324B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMASK0 [7:0]							

Bits	Name	Description
7 : 0	CMASK0	Datapath Compare 1 Mask. The mask value in this register is applied to the selected Compare 1 block input (Accumulator 0 or Accumulator 1) before it is used for comparison. The CMASK1_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.153 UDB_P1_U0_CFG12

Datapath mask enables and shift in configuration

Address: 0x400F324C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	CMASK1_EN	CMASK0_EN	AMASK_EN	DEF_SI	SI_SELB [3:2]		SI_SELA [1:0]	

Bits	Name	Description
7	CMASK1_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
6	CMASK0_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
5	AMASK_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
4	DEF_SI	Datapath default shift value Default Value: 0 **0x0: DEFAULT_0:** Default shift is 0 **0x1: DEFAULT_1:** Default shift is 1
3 : 2	SI_SELB	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle

36.1.153 UDB_P1_U0_CFG12 (continued)

		0x2: ROUTE: Shift in is selected from datapath routing input **0x3: CHAIN:** Shift in is chained from the previous datapath
1 : 0	SI_SELA	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle **0x2: ROUTE:** Shift in is selected from datapath routing input **0x3: CHAIN:** Shift in is chained from the previous datapath

36.1.154 UDB_P1_U0_CFG13

Datapath carry in and compare configuration

Address: 0x400F324D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CMP_SELB [7:6]		CMP_SELA [5:4]		CI_SELB [3:2]		CI_SELA [1:0]	

Bits	Name	Description
7 : 6	CMP_SELB	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
5 : 4	CMP_SELA	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
3 : 2	CI_SELB	Datapath carry in source select Default Value: 0 **0x0: DEFAULT:** Default arithmetic mode **0x1: REGISTERED:** Carry in is the carry out registered from previous cycle **0x2: ROUTE:** Carry in is selected from datapath routing input **0x3: CHAIN:** Carry in is chained from the previous datapath
1 : 0	CI_SELA	Datapath carry in source select Default Value: 0

36.1.154 UDB_P1_U0_CFG13 (continued)

0x0: DEFAULT:
Default arithmetic mode

0x1: REGISTERED:
Carry in is the carry out registered from previous cycle

0x2: ROUTE:
Carry in is selected from datapath routing input

0x3: CHAIN:
Carry in is chained from the previous datapath

36.1.155 UDB_P1_U0_CFG14

Datapath chaining and MSB configuration

Address: 0x400F324E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW	RW	RW
HW Access	R	R			R	R	R	R
Name	MSB_EN	MSB_SEL [6:4]			CHAIN_CMSB	CHAIN_FB	CHAIN1	CHAIN0

Bits	Name	Description
7	MSB_EN	Datapath MSB selection enable Default Value: 0 **0x0: DISABLE:** MSB selection is disabled, MSB is bit 7 **0x1: ENABLE:** MSB selection is controlled by MSB_SEL
6 : 4	MSB_SEL	Datapath MSB Selection Default Value: 0 **0x0: BIT0:** MSB is bit 0 **0x1: BIT1:** MSB is bit 1 **0x2: BIT2:** MSB is bit 2 **0x3: BIT3:** MSB is bit 3 **0x4: BIT4:** MSB is bit 4 **0x5: BIT5:** MSB is bit 5 **0x6: BIT6:** MSB is bit 6 **0x7: BIT7:** MSB is bit 7 - equivalent to MSB_EN=0
3	CHAIN_CMSB	Datapath CRC MSB chaining enable Default Value: 0 **0x0: DISABLE:** CRC MSB is not chained **0x1: ENABLE:** CRC MSB is chained from the next (MSB) datapath

36.1.155 UDB_P1_U0_CFG14 (continued)

2	CHAIN_FB	Datapath CRC feedback chaining enable Default Value: 0 **0x0: DISABLE:** CRC feedback is not chained **0x1: ENABLE:** CRC feedback is chained from the previous (LSB) datapath
1	CHAIN1	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath
0	CHAIN0	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath

36.1.156 UDB_P1_U0_CFG15

Datapath FIFO, shift and parallel input control

Address: 0x400F324F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	PI_SEL	SHIFT_SEL	PI_DYN	MSB_SI	F1_INSEL [3:2]		F0_INSEL [1:0]	

Bits	Name	Description
7	PI_SEL	Datapath parallel input selection Default Value: 0 **0x0: NORMAL:** Normal operation, ALU source is from accumulator selection **0x1: PARALLEL:** ALU source A input is from the parallel data input
6	SHIFT_SEL	Datapath shift out selection Default Value: 0 **0x0: SOL_MSB:** Routed shift out is shift out left (sol_msb) **0x1: SOR:** Routed shift out is shift out right (sor)
5	PI_DYN	Enable for dynamic control of parallel data input (PI) mux. Default Value: 0 **0x0: DISABLE:** Parallel input mux select is only controlled by static configuration (PI_SEL). **0x1: ENABLE:** Parallel input mux to the Datapath is controlled by CFB_EN field in Datapath Dynamic RAM. When this mode is enabled, the CFB_EN usage for CRC/PRS functionality is disabled.
4	MSB_SI	Arithmetic shift right operation shift in selection Default Value: 0 **0x0: DEFAULT:** Shift in default value (when SI_SELA and/or SI_SELB == 0) **0x1: MSB:** Override default and shift in MSB value
3 : 2	F1_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus

36.1.156 UDB_P1_U0_CFG15 (continued)

		0x2: OUTPUT_A1: Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus
1 : 0	F0_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus **0x2: OUTPUT_A1:** Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus

36.1.157 UDB_P1_U0_CFG16

Datapath FIFO and register access configuration control

Address: 0x400F3250

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	F1_CK_INV	F0_CK_INV	FIFO_FAST	FIFO_CAP	FIFO_EDGE	FIFO_ASYNC	EXT_CRCPRS	WRK16_CONCAT

Bits	Name	Description
7	F1_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
6	F0_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
5	FIFO_FAST	FIFO Fast Mode. When this bit is set, the FIFO write logic is clocked by the application bus clock. Lowers the latency of capture timing, at the expense of additional power. Default Value: 0 **0x0: DISABLE:** FIFO is clocked with selected Datapath clock. **0x1: ENABLE:** FIFO is clocked with application bus clock. Master and quadrant bus clock gating must be enabled.
4	FIFO_CAP	FIFO Software Capture Mode. When this bit is set, a read of A0 or A1 triggers a capture into F0 or F1 respectively. This function follows the chaining configuration. All accumulators in the chain from a given block to the MS block in the chain are capture Default Value: 0 **0x0: DISABLE:** FIFO capture is disabled. **0x1: ENABLE:** FIFO capture is enabled (FIFO must be in output mode). A read of A0 or A1 will write into F0 or F1.
3	FIFO_EDGE	Edge/level sensitive FIFO write control (Fx_LD). Only applies to FIFO configured in output mode Default Value: 0

36.1.157 UDB_P1_U0_CFG16 (continued)

		0x0: LEVEL: FIFO write from accumulators/ALU is level sensitive. FIFO write occurs on a clock edge whenever the write control is sampled high on that edge. **0x1: EDGE:** FIFO write from accumulators/ALU is edge sensitive. FIFO write occurs on a clock edge folloing a 0 to 1 transition on the write control. The write control must be negated for at least one full cycle of the FIFO clock for a subsequent transition to be dete
2	FIFO_ASYNC	Asynchronous FIFO clocking support Default Value: 0 **0x0: DISABLE:** FIFO clocks are synchronous **0x1: ENABLE:** FIFO clocks are asynchronous
1	EXT_CRCPRS	External CRC/PRS mode Default Value: 0 **0x0: INTERNAL:** Internal CRC/PRS routing **0x1: EXTERNAL:** External CRC/PRS routing
0	WRK16_CONCAT	Datapath register access mode Default Value: 0 **0x0: DEFAULT:** 16-bit default access mode: selects registers in two consecutive UDBs in chaining order **0x1: CONCATENATE:** 16-bit concat access mode: selects concatenated registers in a single UDB

36.1.158 UDB_P1_U0_CFG17

Datapath FIFO control

Address: 0x400F3251

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			FIFO_ADD_SYNC	NC3	NC2	F1_DYN	F0_DYN

Bits	Name	Description
4	FIFO_ADD_SYNC	Adds an additional sync flip-flop to FIFO block status. Default Value: 0 **0x0: DISABLE:** Compatible Mode: FIFO block status sync configuration is 'none' (FIFO_ASYNC = 0) and 1 sync flip-flop (FIFO_ASYNC = 1) **0x1: ENABLE:** Add Sync Mode: FIFO block status sync configuration 1 sync flip-flop (FIFO_ASYNC = 0) and 2 sync flip-flops (FIFO_ASYNC = 1)
3	NC3	Spare register bit Default Value: 0
2	NC2	Spare register bit Default Value: 0
1	F1_DYN	Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest
0	F0_DYN	When this bit is set, the associated FIFO configuration may be dynamically controlled. Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest

36.1.159 UDB_P1_U0_CFG18

Control Register Mode 0 (used in conjunction with Control Register Mode 1)

Address: 0x400F3252

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_MD0 [7:0]							

Bits	Name	Description
7 : 0	CTL_MD0	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

36.1.160 UDB_P1_U0_CFG19

Control Register Mode 1 (used in conjunction with Control Register Mode 0)

Address: 0x400F3253

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_MD1 [7:0]							

Bits	Name	Description
7 : 0	CTL_MD1	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

36.1.161 UDB_P1_U0_CFG20

Status Register input mode selection

Address: 0x400F3254

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	STAT_MD [7:0]							

Bits	Name	Description
7 : 0	STAT_MD	Mode selection for each bit of the status register. A '0' is transparent mode, where internal routing is read idrectly by CPU firmware. A '1' is sticky-clear-on-read mode, where once the given bit is set, it will stay set until the CPU reads the bit. Default Value: 0

36.1.162 UDB_P1_U0_CFG21

Spare register bits

Address: 0x400F3255

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NC1	NC0

Bits	Name	Description
1	NC1	Spare register bit Default Value: 0
0	NC0	Spare register bit Default Value: 0

36.1.163 UDB_P1_U0_CFG22

SC block configuration control

Address: 0x400F3256

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	
HW Access	None			R	R	R	R	
Name	None [7:5]			SC_EXT_RES	SC_SYNC_MD	SC_INT_MD	SC_OUT_CTL [1:0]	

Bits	Name	Description
4	SC_EXT_RES	Control register external reset operation. This bit supports autonomous usage of the control register, where a routed reset should clear the writable input registers. By default this is off because the CPU writable register can be cleared in firmware. Default Value: 0 **0x0: DISABLED:** When a routed reset is applied to the control register, only embedded state (sampling registers) are cleared **0x1: ENABLED:** When a routed reset is applied to the control register, all state is cleared, including the CPU writable control bits.
3	SC_SYNC_MD	SC Sync Mode - controls when the status register operates as a 4-bit double synchronizer module Default Value: 0 **0x0: NORMAL:** Normal Mode - Status register operation **0x1: SYNC_MODE:** Sync Mode - Routing inputs sc_in[3:0] are the 4 sync inputs, and connections sc_io[3:0] operate as the sync outputs
2	SC_INT_MD	SC Interrupt Mode - controls when the UDB driving an interrupt generated from the masked OR reduction of status bits 6 to 0 Default Value: 0 **0x0: NORMAL:** Normal Mode - Routing connection sc_io[3] is a normal input to the status register **0x1: INT_MODE:** Interrupt Mode - Routing connection sc_io[3] operates as the UDB interrupt output
1 : 0	SC_OUT_CTL	Selects the output source for the Status and Control routing connections Default Value: 0 **0x0: CONTROL:** Control out, 8-bits of control are driven to the routing connections **0x1: PARALLEL:** Datapath parallel output, 8-bits of datapath parallel output data are driven to the routing connections

36.1.163 UDB_P1_U0_CFG22 (continued)

0x2: COUNTER:
Counter out, 7-bits of count and 1 bit (MSB) of terminal count are driven to the routing connections

0x3: RESERVED:
Reserved

36.1.164 UDB_P1_U0_CFG23

Counter Control

Address: 0x400F3257

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW		RW	
HW Access	None	R	R	R	R		R	
Name	None	ALT_CNT	ROUTE_EN	ROUTE_LD	CNT_EN_SEL [3:2]		CNT_LD_SEL [1:0]	

Bits	Name	Description
6	ALT_CNT	Configure the alternate operating mode of the counter Default Value: 0 **0x0: DEFAULT_MODE:** Default counter operating mode **0x1: ALT_MODE:** Alternate counter operating mode
5	ROUTE_EN	Configure the counter enable signal for routing input Default Value: 0 **0x0: DISABLE:** Routed EN signal is not used. EN signal is only controlled by firmware CNT START (ACTL register) **0x1: ROUTED:** Routed EN signal is used, CNT START must be set
4	ROUTE_LD	Configure the counter load signal for routing input Default Value: 0 **0x0: DISABLE:** Routed LD signal is not used **0x1: ROUTED:** Routed LD signal is used
3 : 2	CNT_EN_SEL	Selects the routing inputs for the counter enable signal Default Value: 0 **0x0: SC_IN4:** sc_io_in[0] **0x1: SC_IN5:** sc_io_in[1] **0x2: SC_IN6:** sc_io_in[2] **0x3: SC_IO:** sc_io_in[3]
1 : 0	CNT_LD_SEL	Selects the routing inputs for the counter load signal Default Value: 0

36.1.164 UDB_P1_U0_CFG23 (continued)

0x0: SC_IN0:
sc_in[0]

0x1: SC_IN1:
sc_in[1]

0x2: SC_IN2:
sc_in[2]

0x3: SC_IN3:
sc_in[3]

36.1.165 UDB_P1_U0_CFG24

PLD0 Clock and Reset control

Address: 0x400F3258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

36.1.165 UDB_P1_U0_CFG24 (continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.166 UDB_P1_U0_CFG25

PLD1 Clock and Reset control

Address: 0x400F3259

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

36.1.166 UDB_P1_U0_CFG25 (continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.167 UDB_P1_U0_CFG26

Datapath Clock and Reset control

Address: 0x400F325A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

36.1.167 UDB_P1_U0_CFG26 (continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.168 UDB_P1_U0_CFG27

Status/Control Clock and Reset control

Address: 0x400F325B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

36.1.168 UDB_P1_U0_CFG27 (continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.169 UDB_P1_U0_CFG28

Clock Selection for PLD1 and PLD0

Address: 0x400F325C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PLD1_CK_SEL [7:4]				PLD0_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	PLD1_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	PLD0_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

36.1.169 UDB_P1_U0_CFG28 (continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

36.1.170 UDB_P1_U0_CFG29

Clock Selection for Datapath, Status and Control

Address: 0x400F325D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SC_CK_SEL [7:4]				DP_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	SC_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	DP_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

36.1.170 UDB_P1_U0_CFG29 (continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

36.1.171 UDB_P1_U0_CFG30

Reset control

Address: 0x400F325E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None	RW	RW	RW	RW	
HW Access	R	R	None	R	R	R	R	
Name	SC_RES_POL	DP_RES_POL	None	GUDB_WR	EN_RES_CNTCTL	RES_POL	RES_SEL [1:0]	

Bits	Name	Description
7	SC_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected SC routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Status and Control block is true polarity. **0x1: INVERT:** Routed reset to the Status and Control block is inverted polarity.
6	DP_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected Datapath routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Datapath block is true polarity. **0x1: INVERT:** Routed reset to the Datapath block is inverted polarity.
4	GUDB_WR	Enable global write operation for the configuration and working registers in this UDB. When this bit is set, the UDB ID select decoding is bypassed. Default Value: 0 **0x0: DISABLE:** Global UDB configuration/working register write is disabled **0x1: ENABLE:** Global UDB configuration/working register write is enabled
3	EN_RES_CNTCTL	This bit gates the routed reset to the counter/control register. By default, the operation is compatible, i.e., it only applies to the counter. However, if the updated control regisiter modes are used (sync mode, pulse mode, or the ext res bit) then the routed reset applies to the control register also. Default Value: 0 **0x0: DISABLE:** Routed reset is not applied to counter/control register **0x1: ENABLE:** Routed reset is applied to the counter/control register

36.1.171 UDB_P1_U0_CFG30 (continued)

2	RES_POL	The meaning of this bit depends on the value of the ALT RES bit in CFG31. When ALT RES is '0' (compatible mode), this bit sets the polarity of the routed reset. When ALT RES is '1', this bit is unused. Default Value: 0 **0x0: NEGATED:** Polarity of the routed reset is true. **0x1: ASSERTED:** Polarity of the routed reset is inverted.
1 : 0	RES_SEL	The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES is '0' (compatible mode), this 2 bit field selects the RC routing input for the compatible reset scheme. When the ALT RES bit is '1', these bits are not used. Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.172 UDB_P1_U0_CFG31

Reset control

Address: 0x400F325F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	RW
HW Access	R	R	R		R	R	R	R
Name	PLD1_RES_POL	PLD0_RES_POL	EXT_CK_SEL [5:4]		EN_RES_DP	EN_RES_STAT	EXT_SYNC	ALT_RES

Bits	Name	Description
7	PLD1_RES_POL	Not connected. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Default Value: 0 **0x0: NOINV:** Not Used **0x1: INVERT:** Not Used
6	PLD0_RES_POL	The meaning of this bit depends on the value of ALT RES. When ALT RES (CFG31) is '1', this bit controls the polarity of the selected PLD0 routed reset. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Default Value: 0 **0x0: NOINV:** Routed reset to the PLD0/PLD1 block is true polarity. **0x1: INVERT:** Routed reset to the PLD0/PLD1 block is inverted polarity.
5 : 4	EXT_CK_SEL	External clock selection Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]
3	EN_RES_DP	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the Datapath block. Default Value: 0 **0x0: DISABLE:** Routed reset to the Datapath block is gated off. **0x1: ENABLE:** Routed reset to the Datapath block is on. ALT RES must be '1' and routed reset must be selected in CFG26

36.1.172 UDB_P1_U0_CFG31 (continued)

2	EN_RES_STAT	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the status register. Default Value: 0 **0x0: NEGATED:** Status register routed reset is gated off **0x1: ASSERTED:** Status register routed reset is on
1	EXT_SYNC	Enable synchronization of selected external clock Default Value: 0 **0x0: DISABLE:** Selected external clock input is not synchronized **0x1: ENABLE:** Selected external clock input is synchronized
0	ALT_RES	This bit toggles between two reset configurations. When this bit is '0', one routed reset is shared by all components in this UDB (compatible mode). When this bit is a 1, each block can select a unique routed reset from the available RC inputs. Default Value: 0 **0x0: COMPATIBLE:** All UDB blocks share a common routed reset. **0x1: ALTERNATE:** Each UDB component block can select and control its individual routed reset.

36.1.173 UDB_P1_U0_DCFG0

Dynamic Configuration RAM

Address: 0x400F3260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.173 UDB_P1_U0_DCFG0 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.173 UDB_P1_U0_DCFG0 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.174 UDB_P1_U0_DCFG1

Dynamic Configuration RAM

Address: 0x400F3262

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.174 UDB_P1_U0_DCFG1 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.174 UDB_P1_U0_DCFG1 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.175 UDB_P1_U0_DCFG2

Dynamic Configuration RAM

Address: 0x400F3264

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.175 UDB_P1_U0_DCFG2 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.175 UDB_P1_U0_DCFG2 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.176 UDB_P1_U0_DCFG3

Dynamic Configuration RAM

Address: 0x400F3266

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.176 UDB_P1_U0_DCFG3 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.176 UDB_P1_U0_DCFG3 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.177 UDB_P1_U0_DCFG4

Dynamic Configuration RAM

Address: 0x400F3268

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.177 UDB_P1_U0_DCFG4 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.177 UDB_P1_U0_DCFG4 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.178 UDB_P1_U0_DCFG5

Dynamic Configuration RAM

Address: 0x400F326A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.178 UDB_P1_U0_DCFG5 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.178 UDB_P1_U0_DCFG5 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.179 UDB_P1_U0_DCFG6

Dynamic Configuration RAM

Address: 0x400F326C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.179 UDB_P1_U0_DCFG6 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.179 UDB_P1_U0_DCFG6 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.180 UDB_P1_U0_DCFG7

Dynamic Configuration RAM

Address: 0x400F326E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.180 UDB_P1_U0_DCFG7 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.180 UDB_P1_U0_DCFG7 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.181 UDB_P1_U1_PLD_IT0

PLD Input Terms

Address: 0x400F3280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.181 UDB_P1_U1_PLD_IT0 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.181 UDB_P1_U1_PLD_IT0 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.182 UDB_P1_U1_PLD_IT1

PLD Input Terms

Address: 0x400F3284

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.182 UDB_P1_U1_PLD_IT1 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.182 UDB_P1_U1_PLD_IT1 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.183 UDB_P1_U1_PLD_IT2

PLD Input Terms

Address: 0x400F3288

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.183 UDB_P1_U1_PLD_IT2 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.183 UDB_P1_U1_PLD_IT2 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.184 UDB_P1_U1_PLD_IT3

PLD Input Terms

Address: 0x400F328C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.184 UDB_P1_U1_PLD_IT3 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.184 UDB_P1_U1_PLD_IT3 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.185 UDB_P1_U1_PLD_IT4

PLD Input Terms

Address: 0x400F3290

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.185 UDB_P1_U1_PLD_IT4 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.185 UDB_P1_U1_PLD_IT4 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.186 UDB_P1_U1_PLD_IT5

PLD Input Terms

Address: 0x400F3294

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.186 UDB_P1_U1_PLD_IT5 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.186 UDB_P1_U1_PLD_IT5 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.187 UDB_P1_U1_PLD_IT6

PLD Input Terms

Address: 0x400F3298

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.187 UDB_P1_U1_PLD_IT6 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.187 UDB_P1_U1_PLD_IT6 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.188 UDB_P1_U1_PLD_IT7

PLD Input Terms

Address: 0x400F329C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.188 UDB_P1_U1_PLD_IT7 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.188 UDB_P1_U1_PLD_IT7 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.189 UDB_P1_U1_PLD_IT8

PLD Input Terms

Address: 0x400F32A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.189 UDB_P1_U1_PLD_IT8 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.189 UDB_P1_U1_PLD_IT8 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.190 UDB_P1_U1_PLD_IT9

PLD Input Terms

Address: 0x400F32A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.190 UDB_P1_U1_PLD_IT9 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.190 UDB_P1_U1_PLD_IT9 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.191 UDB_P1_U1_PLD_IT10

PLD Input Terms

Address: 0x400F32A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.191 UDB_P1_U1_PLD_IT10 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.191 UDB_P1_U1_PLD_IT10 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.192 UDB_P1_U1_PLD_IT11

PLD Input Terms

Address: 0x400F32AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	(ITx denotes input number of the PLD, where "x" varies from 0 to 12) True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

36.1.192 UDB_P1_U1_PLD_IT11 (continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

36.1.192 UDB_P1_U1_PLD_IT11 (continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.193 UDB_P1_U1_PLD_ORT0

PLD OR Terms

Address: 0x400F32B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

36.1.193 UDB_P1_U1_PLD_ORT0 (continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.194 UDB_P1_U1_PLD_ORT1

PLD OR Terms

Address: 0x400F32B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

36.1.194 UDB_P1_U1_PLD_ORT1 (continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.195 UDB_P1_U1_PLD_ORT2

PLD OR Terms

Address: 0x400F32B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

36.1.195 UDB_P1_U1_PLD_ORT2 (continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.196 UDB_P1_U1_PLD_ORT3

PLD OR Terms

Address: 0x400F32B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

36.1.196 UDB_P1_U1_PLD_ORT3 (continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.197 UDB_P1_U1_PLD_MC_CFG_CEN_CONST

Macrocell configuration for Carry Enable and Constant

Address: 0x400F32B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_DFF_C	PLD0_MC3_CEN	PLD0_MC2_DFF_C	PLD0_MC2_CEN	PLD0_MC1_DFF_C	PLD0_MC1_CEN	PLD0_MC0_DFF_C	PLD0_MC0_CEN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_DFF_C	PLD1_MC3_CEN	PLD1_MC2_DFF_C	PLD1_MC2_CEN	PLD1_MC1_DFF_C	PLD1_MC1_CEN	PLD1_MC0_DFF_C	PLD1_MC0_CEN

Bits	Name	Description
15	PLD1_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
14	PLD1_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
13	PLD1_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
12	PLD1_MC2_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

36.1.197 UDB_P1_U1_PLD_MC_CFG_CEN_CONST (continued)

11	PLD1_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
10	PLD1_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
9	PLD1_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
8	PLD1_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
7	PLD0_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
6	PLD0_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
5	PLD0_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
4	PLD0_MC2_CEN	Carry enable Default Value: X

36.1.197 UDB_P1_U1_PLD_MC_CFG_CEN_CONST (continued)

		0x0: DISABLE: Disabled **0x1: ENABLE:** Enabled
3	PLD0_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
2	PLD0_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
1	PLD0_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
0	PLD0_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

36.1.198 UDB_P1_U1_PLD_MC_CFG_XORFB

PLD Macro cell XOR feedback

Address: 0x400F32BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD0_MC3_XORFB [7:6]		PLD0_MC2_XORFB [5:4]		PLD0_MC1_XORFB [3:2]		PLD0_MC0_XORFB [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD1_MC3_XORFB [15:14]		PLD1_MC2_XORFB [13:12]		PLD1_MC1_XORFB [11:10]		PLD1_MC0_XORFB [9:8]	

Bits	Name	Description
15 : 14	PLD1_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
13 : 12	PLD1_MC2_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
11 : 10	PLD1_MC1_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry

36.1.198 UDB_P1_U1_PLD_MC_CFG_XORFB (continued)

		0x2: TFF_H: TFF on high **0x3: TFF_L:** TFF on low
9 : 8	PLD1_MC0_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
7 : 6	PLD0_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
5 : 4	PLD0_MC2_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
3 : 2	PLD0_MC1_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low

36.1.198 UDB_P1_U1_PLD_MC_CFG_XORFB (continued)

1 : 0	PLD0_MC0_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low

36.1.199 UDB_P1_U1_PLD_MC_SET_RESET

PLD Macro cell Set Reset Selection

Address: 0x400F32BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_RESET_SEL	PLD0_MC3_SET_SEL	PLD0_MC2_RESET_SEL	PLD0_MC2_SET_SEL	PLD0_MC1_RESET_SEL	PLD0_MC1_SET_SEL	PLD0_MC0_RESET_SEL	PLD0_MC0_SET_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_RESET_SEL	PLD1_MC3_SET_SEL	PLD1_MC2_RESET_SEL	PLD1_MC2_SET_SEL	PLD1_MC1_RESET_SEL	PLD1_MC1_SET_SEL	PLD1_MC0_RESET_SEL	PLD1_MC0_SET_SEL

Bits	Name	Description
15	PLD1_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
14	PLD1_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
13	PLD1_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
12	PLD1_MC2_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

36.1.199 UDB_P1_U1_PLD_MC_SET_RESET (continued)

11	PLD1_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
10	PLD1_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
9	PLD1_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
8	PLD1_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
7	PLD0_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
6	PLD0_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
5	PLD0_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
4	PLD0_MC2_SET_SEL	Set select enable Default Value: X

36.1.199 UDB_P1_U1_PLD_MC_SET_RESET (continued)

		0x0: DISABLE: Set not used **0x1: ENABLE:** Set enabled
3	PLD0_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
2	PLD0_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
1	PLD0_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
0	PLD0_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

36.1.200 UDB_P1_U1_PLD_MC_CFG_BYPASS

PLD Macro cell Bypass control

Address: 0x400F32BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	NC7	PLD0_MC3_BYPASS	NC5	PLD0_MC2_BYPASS	NC3	PLD0_MC1_BYPASS	NC1	PLD0_MC0_BYPASS

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	NC15	PLD1_MC3_BYPASS	NC13	PLD1_MC2_BYPASS	NC11	PLD1_MC1_BYPASS	NC9	PLD1_MC0_BYPASS

Bits	Name	Description
15	NC15	Spare register bit Default Value: X
14	PLD1_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
13	NC13	Spare register bit Default Value: X
12	PLD1_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
11	NC11	Spare register bit Default Value: X
10	PLD1_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output

36.1.200 UDB_P1_U1_PLD_MC_CFG_BYPASS (continued)

9	NC9	Spare register bit Default Value: X
8	PLD1_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
7	NC7	Spare register bit Default Value: X
6	PLD0_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
5	NC5	Spare register bit Default Value: X
4	PLD0_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
3	NC3	Spare register bit Default Value: X
2	PLD0_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
1	NC1	Spare register bit Default Value: X
0	PLD0_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output

36.1.201 UDB_P1_U1_CFG0

Datapath Input Selection - RAD1 RAD0. Address bits 0 and 1 to the dynamic configuration RAM

Address: 0x400F32C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	RAD1 [6:4]			None	RAD0 [2:0]		

Bits	Name	Description
6 : 4	RAD1	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	RAD0	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

36.1.201 UDB_P1_U1_CFG0 (continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.202 UDB_P1_U1_CFG1

Datapath Input Selection - RAD2. Address bit 2 to the dynamic configuration RAM

Address: 0x400F32C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW		
HW Access	R	R	R	R	R	R		
Name	DP_RTE_BYPASS4	DP_RTE_BYPASS3	DP_RTE_BYPASS2	DP_RTE_BYPASS1	DP_RTE_BYPASS0	RAD2 [2:0]		

Bits	Name	Description
7	DP_RTE_BYPASS4	DP_In bypass control Default Value: 0 **0x0: DP_IN4_ROUTE:** Use dp_in[4] **0x1: DP_IN4_BYPASS:** Use dp_out[4] as input via bypass
6	DP_RTE_BYPASS3	DP_In bypass control Default Value: 0 **0x0: DP_IN3_ROUTE:** Use dp_in[3] **0x1: DP_IN3_BYPASS:** Use dp_out[3] as input via bypass
5	DP_RTE_BYPASS2	DP_In bypass control Default Value: 0 **0x0: DP_IN2_ROUTE:** Use dp_in[2] **0x1: DP_IN2_BYPASS:** Use dp_out[2] as input via bypass
4	DP_RTE_BYPASS1	DP_In bypass control Default Value: 0 **0x0: DP_IN1_ROUTE:** Use dp_in[1] **0x1: DP_IN1_BYPASS:** Use dp_out[1] as input via bypass
3	DP_RTE_BYPASS0	DP_In bypass control Default Value: 0 **0x0: DP_IN0_ROUTE:** Use dp_in[0] **0x1: DP_IN0_BYPASS:** Use dp_out[0] as input via bypass

36.1.202 UDB_P1_U1_CFG1 (continued)

2 : 0	RAD2	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved

36.1.203 UDB_P1_U1_CFG2

Datapath Input Selection - F1_LD, F0_LD.

Address: 0x400F32C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	NC7	F1_LD [6:4]			DP_RTE_BYPASS5	F0_LD [2:0]		

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6 : 4	F1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
3	DP_RTE_BYPASS5	DP_In bypass control Default Value: 0 **0x0: DP_IN5_ROUTE:** Use dp_in[5] **0x1: DP_IN5_BYPASS:** Use dp_out[5] via bypass
2 : 0	F0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off

36.1.203 UDB_P1_U1_CFG2 (continued)

0x1: DP_IN0:
Set to dp_in[0]

0x2: DP_IN1:
Set to dp_in[1]

0x3: DP_IN2:
Set to dp_in[2]

0x4: DP_IN3:
Set to dp_in[3]

0x5: DP_IN4:
Set to dp_in[4]

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.204 UDB_P1_U1_CFG3

Datapath Input Selection - D1_LD, D0_LD.

Address: 0x400F32C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	D1_LD [6:4]			None	D0_LD [2:0]		

Bits	Name	Description
6 : 4	D1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	D0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

36.1.204 UDB_P1_U1_CFG3 (continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.205 UDB_P1_U1_CFG4

Datapath Input Selection - CI_MUX SI_MUX.

Address: 0x400F32C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	CI_MUX [6:4]			None	SI_MUX [2:0]		

Bits	Name	Description
6 : 4	CI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	SI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

36.1.205 UDB_P1_U1_CFG4 (continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.206 UDB_P1_U1_CFG5

Datapath Output Selection for OUT1 OUT0

Address: 0x400F32C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT1 [7:4]				OUT0 [3:0]			

Bits	Name	Description
7 : 4	OUT1	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

36.1.206 UDB_P1_U1_CFG5 (continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT0	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.207 UDB_P1_U1_CFG6

Datapath Output Selection for OUT3 OUT2

Address: 0x400F32C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT3 [7:4]				OUT2 [3:0]			

Bits	Name	Description
7 : 4	OUT3	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

36.1.207 UDB_P1_U1_CFG6 (continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT2	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.208 UDB_P1_U1_CFG7

Datapath Output Selection for OUT5 OUT4

Address: 0x400F32C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT5 [7:4]				OUT4 [3:0]			

Bits	Name	Description
7 : 4	OUT5	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

36.1.208 UDB_P1_U1_CFG7 (continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT4	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.209 UDB_P1_U1_CFG8

Datapath Output Synchronization Option

Address: 0x400F32C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW					
HW Access	R	R	R					
Name	NC7	NC6	OUT_SYNC [5:0]					

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6	NC6	Spare register bit Default Value: 0
5 : 0	OUT_SYNC	Datapath Output Synchronization. Each datapath output can be registered (default,0), or combinational (1) Default Value: 0 **0x0: REGISTERED:** registered **0x1: COMBINATIONAL:** combinational

36.1.210 UDB_P1_U1_CFG9

Datapath ALU Mask

Address: 0x400F32C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	AMASK [7:0]							

Bits	Name	Description
7 : 0	AMASK	Datapath ALU Mask. The mask value in this register is applied to the output of the Datapath ALU result before the result is stored. The AMASK_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.211 UDB_P1_U1_CFG10

Datapath Compare 0 Mask

Address: 0x400F32CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMASK0 [7:0]							

Bits	Name	Description
7 : 0	CMASK0	Datapath Compare 0 Mask. The mask value in this register is applied to the output of the Accumulator 0 before it is used for comparison in Compare block 0. The CMASK0_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.212 UDB_P1_U1_CFG11

Datapath Compare 1 Mask

Address: 0x400F32CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMASK0 [7:0]							

Bits	Name	Description
7 : 0	CMASK0	Datapath Compare 1 Mask. The mask value in this register is applied to the selected Compare 1 block input (Accumulator 0 or Accumulator 1) before it is used for comparison. The CMASK1_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.213 UDB_P1_U1_CFG12

Datapath mask enables and shift in configuration

Address: 0x400F32CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	CMASK1_EN	CMASK0_EN	AMASK_EN	DEF_SI	SI_SELB [3:2]		SI_SELA [1:0]	

Bits	Name	Description
7	CMASK1_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
6	CMASK0_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
5	AMASK_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
4	DEF_SI	Datapath default shift value Default Value: 0 **0x0: DEFAULT_0:** Default shift is 0 **0x1: DEFAULT_1:** Default shift is 1
3 : 2	SI_SELB	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle

36.1.213 UDB_P1_U1_CFG12 (continued)

		0x2: ROUTE: Shift in is selected from datapath routing input **0x3: CHAIN:** Shift in is chained from the previous datapath
1 : 0	SI_SELA	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle **0x2: ROUTE:** Shift in is selected from datapath routing input **0x3: CHAIN:** Shift in is chained from the previous datapath

36.1.214 UDB_P1_U1_CFG13

Datapath carry in and compare configuration

Address: 0x400F32CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CMP_SELB [7:6]		CMP_SELA [5:4]		CI_SELB [3:2]		CI_SELA [1:0]	

Bits	Name	Description
7 : 6	CMP_SELB	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
5 : 4	CMP_SELA	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
3 : 2	CI_SELB	Datapath carry in source select Default Value: 0 **0x0: DEFAULT:** Default arithmetic mode **0x1: REGISTERED:** Carry in is the carry out registered from previous cycle **0x2: ROUTE:** Carry in is selected from datapath routing input **0x3: CHAIN:** Carry in is chained from the previous datapath
1 : 0	CI_SELA	Datapath carry in source select Default Value: 0

36.1.214 UDB_P1_U1_CFG13 (continued)

0x0: DEFAULT:
Default arithmetic mode

0x1: REGISTERED:
Carry in is the carry out registered from previous cycle

0x2: ROUTE:
Carry in is selected from datapath routing input

0x3: CHAIN:
Carry in is chained from the previous datapath

36.1.215 UDB_P1_U1_CFG14

Datapath chaining and MSB configuration

Address: 0x400F32CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW	RW	RW
HW Access	R	R			R	R	R	R
Name	MSB_EN	MSB_SEL [6:4]			CHAIN_CMSB	CHAIN_FB	CHAIN1	CHAIN0

Bits	Name	Description
7	MSB_EN	Datapath MSB selection enable Default Value: 0 **0x0: DISABLE:** MSB selection is disabled, MSB is bit 7 **0x1: ENABLE:** MSB selection is controlled by MSB_SEL
6 : 4	MSB_SEL	Datapath MSB Selection Default Value: 0 **0x0: BIT0:** MSB is bit 0 **0x1: BIT1:** MSB is bit 1 **0x2: BIT2:** MSB is bit 2 **0x3: BIT3:** MSB is bit 3 **0x4: BIT4:** MSB is bit 4 **0x5: BIT5:** MSB is bit 5 **0x6: BIT6:** MSB is bit 6 **0x7: BIT7:** MSB is bit 7 - equivalent to MSB_EN=0
3	CHAIN_CMSB	Datapath CRC MSB chaining enable Default Value: 0 **0x0: DISABLE:** CRC MSB is not chained **0x1: ENABLE:** CRC MSB is chained from the next (MSB) datapath

36.1.215 UDB_P1_U1_CFG14 (continued)

2	CHAIN_FB	Datapath CRC feedback chaining enable Default Value: 0 **0x0: DISABLE:** CRC feedback is not chained **0x1: ENABLE:** CRC feedback is chained from the previous (LSB) datapath
1	CHAIN1	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath
0	CHAIN0	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath

36.1.216 UDB_P1_U1_CFG15

Datapath FIFO, shift and parallel input control

Address: 0x400F32CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	PI_SEL	SHIFT_SEL	PI_DYN	MSB_SI	F1_INSEL [3:2]		F0_INSEL [1:0]	

Bits	Name	Description
7	PI_SEL	Datapath parallel input selection Default Value: 0 **0x0: NORMAL:** Normal operation, ALU source is from accumulator selection **0x1: PARALLEL:** ALU source A input is from the parallel data input
6	SHIFT_SEL	Datapath shift out selection Default Value: 0 **0x0: SOL_MSB:** Routed shift out is shift out left (sol_msb) **0x1: SOR:** Routed shift out is shift out right (sor)
5	PI_DYN	Enable for dynamic control of parallel data input (PI) mux. Default Value: 0 **0x0: DISABLE:** Parallel input mux select is only controlled by static configuration (PI_SEL). **0x1: ENABLE:** Parallel input mux to the Datapath is controlled by CFB_EN field in Datapath Dynamic RAM. When this mode is enabled, the CFB_EN usage for CRC/PRS functionality is disabled.
4	MSB_SI	Arithmetic shift right operation shift in selection Default Value: 0 **0x0: DEFAULT:** Shift in default value (when SI_SELA and/or SI_SELB == 0) **0x1: MSB:** Override default and shift in MSB value
3 : 2	F1_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus

36.1.216 UDB_P1_U1_CFG15 (continued)

		0x2: OUTPUT_A1: Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus
1 : 0	F0_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus **0x2: OUTPUT_A1:** Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus

36.1.217 UDB_P1_U1_CFG16

Datapath FIFO and register access configuration control

Address: 0x400F32D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	F1_CK_INV	F0_CK_INV	FIFO_FAST	FIFO_CAP	FIFO_EDGE	FIFO_ASYNC	EXT_CRCPRS	WRK16_CONCAT

Bits	Name	Description
7	F1_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
6	F0_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
5	FIFO_FAST	FIFO Fast Mode. When this bit is set, the FIFO write logic is clocked by the application bus clock. Lowers the latency of capture timing, at the expense of additional power. Default Value: 0 **0x0: DISABLE:** FIFO is clocked with selected Datapath clock. **0x1: ENABLE:** FIFO is clocked with application bus clock. Master and quadrant bus clock gating must be enabled.
4	FIFO_CAP	FIFO Software Capture Mode. When this bit is set, a read of A0 or A1 triggers a capture into F0 or F1 respectively. This function follows the chaining configuration. All accumulators in the chain from a given block to the MS block in the chain are capture Default Value: 0 **0x0: DISABLE:** FIFO capture is disabled. **0x1: ENABLE:** FIFO capture is enabled (FIFO must be in output mode). A read of A0 or A1 will write into F0 or F1.
3	FIFO_EDGE	Edge/level sensitive FIFO write control (Fx_LD). Only applies to FIFO configured in output mode Default Value: 0

36.1.217 UDB_P1_U1_CFG16 (continued)

		0x0: LEVEL: FIFO write from accumulators/ALU is level sensitive. FIFO write occurs on a clock edge whenever the write control is sampled high on that edge. **0x1: EDGE:** FIFO write from accumulators/ALU is edge sensitive. FIFO write occurs on a clock edge folloing a 0 to 1 transition on the write control. The write control must be negated for at least one full cycle of the FIFO clock for a subsequent transition to be dete
2	FIFO_ASYNC	Asynchronous FIFO clocking support Default Value: 0 **0x0: DISABLE:** FIFO clocks are synchronous **0x1: ENABLE:** FIFO clocks are asynchronous
1	EXT_CRCPRS	External CRC/PRS mode Default Value: 0 **0x0: INTERNAL:** Internal CRC/PRS routing **0x1: EXTERNAL:** External CRC/PRS routing
0	WRK16_CONCAT	Datapath register access mode Default Value: 0 **0x0: DEFAULT:** 16-bit default access mode: selects registers in two consecutive UDBs in chaining order **0x1: CONCATENATE:** 16-bit concat access mode: selects concatenated registers in a single UDB

36.1.218 UDB_P1_U1_CFG17

Datapath FIFO control

Address: 0x400F32D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			FIFO_ADD_SYNC	NC3	NC2	F1_DYN	F0_DYN

Bits	Name	Description
4	FIFO_ADD_SYNC	Adds an additional sync flip-flop to FIFO block status. Default Value: 0 **0x0: DISABLE:** Compatible Mode: FIFO block status sync configuration is 'none' (FIFO_ASYNC = 0) and 1 sync flip-flop (FIFO_ASYNC = 1) **0x1: ENABLE:** Add Sync Mode: FIFO block status sync configuration 1 sync flip-flop (FIFO_ASYNC = 0) and 2 sync flip-flops (FIFO_ASYNC = 1)
3	NC3	Spare register bit Default Value: 0
2	NC2	Spare register bit Default Value: 0
1	F1_DYN	Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest
0	F0_DYN	When this bit is set, the associated FIFO configuration may be dynamically controlled. Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest

36.1.219 UDB_P1_U1_CFG18

Control Register Mode 0 (used in conjunction with Control Register Mode 1)

Address: 0x400F32D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_MD0 [7:0]							

Bits	Name	Description
7 : 0	CTL_MD0	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

36.1.220 UDB_P1_U1_CFG19

Control Register Mode 1 (used in conjunction with Control Register Mode 0)

Address: 0x400F32D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_MD1 [7:0]							

Bits	Name	Description
7 : 0	CTL_MD1	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

36.1.221 UDB_P1_U1_CFG20

Status Register input mode selection

Address: 0x400F32D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	STAT_MD [7:0]							

Bits	Name	Description
7 : 0	STAT_MD	Mode selection for each bit of the status register. A '0' is transparent mode, where internal routing is read idrectly by CPU firmware. A '1' is sticky-clear-on-read mode, where once the given bit is set, it will stay set until the CPU reads the bit. Default Value: 0

36.1.222 UDB_P1_U1_CFG21

Spare register bits

Address: 0x400F32D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NC1	NC0

Bits	Name	Description
1	NC1	Spare register bit Default Value: 0
0	NC0	Spare register bit Default Value: 0

36.1.223 UDB_P1_U1_CFG22

SC block configuration control

Address: 0x400F32D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	
HW Access	None			R	R	R	R	
Name	None [7:5]			SC_EXT_RES	SC_SYNC_MD	SC_INT_MD	SC_OUT_CTL [1:0]	

Bits	Name	Description
4	SC_EXT_RES	Control register external reset operation. This bit supports autonomous usage of the control register, where a routed reset should clear the writable input registers. By default this is off because the CPU writable register can be cleared in firmware. Default Value: 0 **0x0: DISABLED:** When a routed reset is applied to the control register, only embedded state (sampling registers) are cleared **0x1: ENABLED:** When a routed reset is applied to the control register, all state is cleared, including the CPU writable control bits.
3	SC_SYNC_MD	SC Sync Mode - controls when the status register operates as a 4-bit double synchronizer module Default Value: 0 **0x0: NORMAL:** Normal Mode - Status register operation **0x1: SYNC_MODE:** Sync Mode - Routing inputs sc_in[3:0] are the 4 sync inputs, and connections sc_io[3:0] operate as the sync outputs
2	SC_INT_MD	SC Interrupt Mode - controls when the UDB driving an interrupt generated from the masked OR reduction of status bits 6 to 0 Default Value: 0 **0x0: NORMAL:** Normal Mode - Routing connection sc_io[3] is a normal input to the status register **0x1: INT_MODE:** Interrupt Mode - Routing connection sc_io[3] operates as the UDB interrupt output
1 : 0	SC_OUT_CTL	Selects the output source for the Status and Control routing connections Default Value: 0 **0x0: CONTROL:** Control out, 8-bits of control are driven to the routing connections **0x1: PARALLEL:** Datapath parallel output, 8-bits of datapath parallel output data are driven to the routing connections

36.1.223 UDB_P1_U1_CFG22 (continued)

0x2: COUNTER:
Counter out, 7-bits of count and 1 bit (MSB) of terminal count are driven to the routing connections

0x3: RESERVED:
Reserved

36.1.224 UDB_P1_U1_CFG23

Counter Control

Address: 0x400F32D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW		RW	
HW Access	None	R	R	R	R		R	
Name	None	ALT_CNT	ROUTE_EN	ROUTE_LD	CNT_EN_SEL [3:2]		CNT_LD_SEL [1:0]	

Bits	Name	Description
6	ALT_CNT	Configure the alternate operating mode of the counter Default Value: 0 **0x0: DEFAULT_MODE:** Default counter operating mode **0x1: ALT_MODE:** Alternate counter operating mode
5	ROUTE_EN	Configure the counter enable signal for routing input Default Value: 0 **0x0: DISABLE:** Routed EN signal is not used. EN signal is only controlled by firmware CNT START (ACTL register) **0x1: ROUTED:** Routed EN signal is used, CNT START must be set
4	ROUTE_LD	Configure the counter load signal for routing input Default Value: 0 **0x0: DISABLE:** Routed LD signal is not used **0x1: ROUTED:** Routed LD signal is used
3 : 2	CNT_EN_SEL	Selects the routing inputs for the counter enable signal Default Value: 0 **0x0: SC_IN4:** sc_io_in[0] **0x1: SC_IN5:** sc_io_in[1] **0x2: SC_IN6:** sc_io_in[2] **0x3: SC_IO:** sc_io_in[3]
1 : 0	CNT_LD_SEL	Selects the routing inputs for the counter load signal Default Value: 0

36.1.224 UDB_P1_U1_CFG23 (continued)

0x0: SC_IN0:
sc_in[0]

0x1: SC_IN1:
sc_in[1]

0x2: SC_IN2:
sc_in[2]

0x3: SC_IN3:
sc_in[3]

36.1.225 UDB_P1_U1_CFG24

PLD0 Clock and Reset control

Address: 0x400F32D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

36.1.225 UDB_P1_U1_CFG24 (continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.226 UDB_P1_U1_CFG25

PLD1 Clock and Reset control

Address: 0x400F32D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

36.1.226 UDB_P1_U1_CFG25 (continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.227 UDB_P1_U1_CFG26

Datapath Clock and Reset control

Address: 0x400F32DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

36.1.227 UDB_P1_U1_CFG26 (continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.228 UDB_P1_U1_CFG27

Status/Control Clock and Reset control

Address: 0x400F32DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

36.1.228 UDB_P1_U1_CFG27 (continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.229 UDB_P1_U1_CFG28

Clock Selection for PLD1 and PLD0

Address: 0x400F32DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PLD1_CK_SEL [7:4]				PLD0_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	PLD1_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	PLD0_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

36.1.229 UDB_P1_U1_CFG28 (continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

36.1.230 UDB_P1_U1_CFG29

Clock Selection for Datapath, Status and Control

Address: 0x400F32DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SC_CK_SEL [7:4]				DP_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	SC_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	DP_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

36.1.230 UDB_P1_U1_CFG29 (continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

36.1.231 UDB_P1_U1_CFG30

Reset control

Address: 0x400F32DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None	RW	RW	RW	RW	
HW Access	R	R	None	R	R	R	R	
Name	SC_RES_POL	DP_RES_POL	None	GUDB_WR	EN_RES_CNTCTL	RES_POL	RES_SEL [1:0]	

Bits	Name	Description
7	SC_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected SC routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Status and Control block is true polarity. **0x1: INVERT:** Routed reset to the Status and Control block is inverted polarity.
6	DP_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected Datapath routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Datapath block is true polarity. **0x1: INVERT:** Routed reset to the Datapath block is inverted polarity.
4	GUDB_WR	Enable global write operation for the configuration and working registers in this UDB. When this bit is set, the UDB ID select decoding is bypassed. Default Value: 0 **0x0: DISABLE:** Global UDB configuration/working register write is disabled **0x1: ENABLE:** Global UDB configuration/working register write is enabled
3	EN_RES_CNTCTL	This bit gates the routed reset to the counter/control register. By default, the operation is compatible, i.e., it only applies to the counter. However, if the updated control regisiter modes are used (sync mode, pulse mode, or the ext res bit) then the routed reset applies to the control register also. Default Value: 0 **0x0: DISABLE:** Routed reset is not applied to counter/control register **0x1: ENABLE:** Routed reset is applied to the counter/control register

36.1.231 UDB_P1_U1_CFG30 (continued)

2	RES_POL	The meaning of this bit depends on the value of the ALT RES bit in CFG31. When ALT RES is '0' (compatible mode), this bit sets the polarity of the routed reset. When ALT RES is '1', this bit is unused. Default Value: 0 **0x0: NEGATED:** Polarity of the routed reset is true. **0x1: ASSERTED:** Polarity of the routed reset is inverted.
1 : 0	RES_SEL	The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES is '0' (compatible mode), this 2 bit field selects the RC routing input for the compatible reset scheme. When the ALT RES bit is '1', these bits are not used. Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.232 UDB_P1_U1_CFG31

Reset control

Address: 0x400F32DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	RW
HW Access	R	R	R		R	R	R	R
Name	PLD1_RES_POL	PLD0_RES_POL	EXT_CK_SEL [5:4]		EN_RES_DP	EN_RES_STAT	EXT_SYNC	ALT_RES

Bits	Name	Description
7	PLD1_RES_POL	Not connected. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Default Value: 0 **0x0: NOINV:** Not Used **0x1: INVERT:** Not Used
6	PLD0_RES_POL	The meaning of this bit depends on the value of ALT RES. When ALT RES (CFG31) is '1', this bit controls the polarity of the selected PLD0 routed reset. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Default Value: 0 **0x0: NOINV:** Routed reset to the PLD0/PLD1 block is true polarity. **0x1: INVERT:** Routed reset to the PLD0/PLD1 block is inverted polarity.
5 : 4	EXT_CK_SEL	External clock selection Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]
3	EN_RES_DP	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the Datapath block. Default Value: 0 **0x0: DISABLE:** Routed reset to the Datapath block is gated off. **0x1: ENABLE:** Routed reset to the Datapath block is on. ALT RES must be '1' and routed reset must be selected in CFG26

36.1.232 UDB_P1_U1_CFG31 (continued)

2	EN_RES_STAT	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the status register. Default Value: 0 **0x0: NEGATED:** Status register routed reset is gated off **0x1: ASSERTED:** Status register routed reset is on
1	EXT_SYNC	Enable synchronization of selected external clock Default Value: 0 **0x0: DISABLE:** Selected external clock input is not synchronized **0x1: ENABLE:** Selected external clock input is synchronized
0	ALT_RES	This bit toggles between two reset configurations. When this bit is '0', one routed reset is shared by all components in this UDB (compatible mode). When this bit is a 1, each block can select a unique routed reset from the available RC inputs. Default Value: 0 **0x0: COMPATIBLE:** All UDB blocks share a common routed reset. **0x1: ALTERNATE:** Each UDB component block can select and control its individual routed reset.

36.1.233 UDB_P1_U1_DCFG0

Dynamic Configuration RAM

Address: 0x400F32E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.233 UDB_P1_U1_DCFG0 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.233 UDB_P1_U1_DCFG0 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.234 UDB_P1_U1_DCFG1

Dynamic Configuration RAM

Address: 0x400F32E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.234 UDB_P1_U1_DCFG1 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.234 UDB_P1_U1_DCFG1 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.235 UDB_P1_U1_DCFG2

Dynamic Configuration RAM

Address: 0x400F32E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.235 UDB_P1_U1_DCFG2 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.235 UDB_P1_U1_DCFG2 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.236 UDB_P1_U1_DCFG3

Dynamic Configuration RAM

Address: 0x400F32E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.236 UDB_P1_U1_DCFG3 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.236 UDB_P1_U1_DCFG3 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.237 UDB_P1_U1_DCFG4

Dynamic Configuration RAM

Address: 0x400F32E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.237 UDB_P1_U1_DCFG4 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.237 UDB_P1_U1_DCFG4 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.238 UDB_P1_U1_DCFG5

Dynamic Configuration RAM

Address: 0x400F32EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.238 UDB_P1_U1_DCFG5 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.238 UDB_P1_U1_DCFG5 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.239 UDB_P1_U1_DCFG6

Dynamic Configuration RAM

Address: 0x400F32EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.239 UDB_P1_U1_DCFG6 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.239 UDB_P1_U1_DCFG6 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.240 UDB_P1_U1_DCFG7

Dynamic Configuration RAM

Address: 0x400F32EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

36.1.240 UDB_P1_U1_DCFG7 (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

36.1.240 UDB_P1_U1_DCFG7 (continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

37 UDB 8-Bit Working (WRK8) Registers

This section discusses the WRK8 registers. It lists all the registers in mapping tables, in address order.

37.1 Register Details

Register Name	Address
UDB_W8_A00	0x400F0000
UDB_W8_A01	0x400F0001
UDB_W8_A02	0x400F0002
UDB_W8_A03	0x400F0003
UDB_W8_A10	0x400F0010
UDB_W8_A11	0x400F0011
UDB_W8_A12	0x400F0012
UDB_W8_A13	0x400F0013
UDB_W8_D00	0x400F0020
UDB_W8_D01	0x400F0021
UDB_W8_D02	0x400F0022
UDB_W8_D03	0x400F0023
UDB_W8_D10	0x400F0030
UDB_W8_D11	0x400F0031
UDB_W8_D12	0x400F0032
UDB_W8_D13	0x400F0033
UDB_W8_F00	0x400F0040
UDB_W8_F01	0x400F0041
UDB_W8_F02	0x400F0042
UDB_W8_F03	0x400F0043
UDB_W8_F10	0x400F0050
UDB_W8_F11	0x400F0051
UDB_W8_F12	0x400F0052
UDB_W8_F13	0x400F0053
UDB_W8_ST0	0x400F0060
UDB_W8_ST1	0x400F0061

Register Name	Address
UDB_W8_ST2	0x400F0062
UDB_W8_ST3	0x400F0063
UDB_W8_CTL0	0x400F0070
UDB_W8_CTL1	0x400F0071
UDB_W8_CTL2	0x400F0072
UDB_W8_CTL3	0x400F0073
UDB_W8_MSK0	0x400F0080
UDB_W8_MSK1	0x400F0081
UDB_W8_MSK2	0x400F0082
UDB_W8_MSK3	0x400F0083
UDB_W8_ACTL0	0x400F0090
UDB_W8_ACTL1	0x400F0091
UDB_W8_ACTL2	0x400F0092
UDB_W8_ACTL3	0x400F0093
UDB_W8_MC0	0x400F00A0
UDB_W8_MC1	0x400F00A1
UDB_W8_MC2	0x400F00A2
UDB_W8_MC3	0x400F00A3

37.1.1 UDB_W8_A00

Accumulator 0

Address: 0x400F0000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0 [7:0]							

Bits	Name	Description
7 : 0	A0	Accumulator 0 Default Value: 0

37.1.2 UDB_W8_A01

Accumulator 0

Address: 0x400F0001

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0 [7:0]							

Bits	Name	Description
7 : 0	A0	Accumulator 0 Default Value: 0

37.1.3 UDB_W8_A02

Accumulator 0

Address: 0x400F0002

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0 [7:0]							

Bits	Name	Description
7 : 0	A0	Accumulator 0 Default Value: 0

37.1.4 UDB_W8_A03

Accumulator 0

Address: 0x400F0003

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0 [7:0]							

Bits	Name	Description
7 : 0	A0	Accumulator 0 Default Value: 0

37.1.5 UDB_W8_A10

Accumulator 1

Address: 0x400F0010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A1 [7:0]							

Bits	Name	Description
7 : 0	A1	Accumulator 1 Default Value: 0

37.1.6 UDB_W8_A11

Accumulator 1

Address: 0x400F0011

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A1 [7:0]							

Bits	Name	Description
7 : 0	A1	Accumulator 1 Default Value: 0

37.1.7 UDB_W8_A12

Accumulator 1

Address: 0x400F0012

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A1 [7:0]							

Bits	Name	Description
7 : 0	A1	Accumulator 1 Default Value: 0

37.1.8 UDB_W8_A13

Accumulator 1

Address: 0x400F0013

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A1 [7:0]							

Bits	Name	Description
7 : 0	A1	Accumulator 1 Default Value: 0

37.1.9 UDB_W8_D00

Data 0

Address: 0x400F0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0 [7:0]							

Bits	Name	Description
7 : 0	D0	Data 0 Default Value: 0

37.1.10 UDB_W8_D01

Data 0

Address: 0x400F0021

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0 [7:0]							

Bits	Name	Description
7 : 0	D0	Data 0 Default Value: 0

37.1.11 UDB_W8_D02

Data 0

Address: 0x400F0022

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0 [7:0]							

Bits	Name	Description
7 : 0	D0	Data 0 Default Value: 0

37.1.12 UDB_W8_D03

Data 0

Address: 0x400F0023

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0 [7:0]							

Bits	Name	Description
7 : 0	D0	Data 0 Default Value: 0

37.1.13 UDB_W8_D10

Data 1

Address: 0x400F0030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D1 [7:0]							

Bits	Name	Description
7 : 0	D1	Data 1 Default Value: 0

37.1.14 UDB_W8_D11

Data 1

Address: 0x400F0031

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D1 [7:0]							

Bits	Name	Description
7 : 0	D1	Data 1 Default Value: 0

37.1.15 UDB_W8_D12

Data 1

Address: 0x400F0032

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D1 [7:0]							

Bits	Name	Description
7 : 0	D1	Data 1 Default Value: 0

37.1.16 UDB_W8_D13

Data 1

Address: 0x400F0033

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D1 [7:0]							

Bits	Name	Description
7 : 0	D1	Data 1 Default Value: 0

37.1.17 UDB_W8_F00

FIFO 0

Address: 0x400F0040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0 [7:0]							

Bits	Name	Description
7 : 0	F0	Fifo 0 Default Value: X

37.1.18 UDB_W8_F01

FIFO 0

Address: 0x400F0041

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0 [7:0]							

Bits	Name	Description
7 : 0	F0	Fifo 0 Default Value: X

37.1.19 UDB_W8_F02

FIFO 0

Address: 0x400F0042

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0 [7:0]							

Bits	Name	Description
7 : 0	F0	Fifo 0 Default Value: X

37.1.20 UDB_W8_F03

FIFO 0

Address: 0x400F0043

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0 [7:0]							

Bits	Name	Description
7 : 0	F0	Fifo 0 Default Value: X

37.1.21 UDB_W8_F10

FIFO 1

Address: 0x400F0050

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F1 [7:0]							

Bits	Name	Description
7 : 0	F1	Fifo 1 Default Value: X

37.1.22 UDB_W8_F11

FIFO 1

Address: 0x400F0051

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F1 [7:0]							

Bits	Name	Description
7 : 0	F1	Fifo 1 Default Value: X

37.1.23 UDB_W8_F12

FIFO 1

Address: 0x400F0052

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F1 [7:0]							

Bits	Name	Description
7 : 0	F1	Fifo 1 Default Value: X

37.1.24 UDB_W8_F13

FIFO 1

Address: 0x400F0053

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F1 [7:0]							

Bits	Name	Description
7 : 0	F1	Fifo 1 Default Value: X

37.1.25 UDB_W8_ST0

Status Register

Address: 0x400F0060

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST [7:0]							

Bits	Name	Description
7 : 0	ST	Status register Default Value: 0

37.1.26 UDB_W8_ST1

Status Register

Address: 0x400F0061

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST [7:0]							

Bits	Name	Description
7 : 0	ST	Status register Default Value: 0

37.1.27 UDB_W8_ST2

Status Register

Address: 0x400F0062

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST [7:0]							

Bits	Name	Description
7 : 0	ST	Status register Default Value: 0

37.1.28 UDB_W8_ST3

Status Register

Address: 0x400F0063

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST [7:0]							

Bits	Name	Description
7 : 0	ST	Status register Default Value: 0

37.1.29 UDB_W8_CTL0

Control Register

Address: 0x400F0070

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL [7:0]							

Bits	Name	Description
7 : 0	CTL	Control register Default Value: 0

37.1.30 UDB_W8_CTL1

Control Register

Address: 0x400F0071

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL [7:0]							

Bits	Name	Description
7 : 0	CTL	Control register Default Value: 0

37.1.31 UDB_W8_CTL2

Control Register

Address: 0x400F0072

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL [7:0]							

Bits	Name	Description
7 : 0	CTL	Control register Default Value: 0

37.1.32 UDB_W8_CTL3

Control Register

Address: 0x400F0073

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL [7:0]							

Bits	Name	Description
7 : 0	CTL	Control register Default Value: 0

37.1.33 UDB_W8_MSK0

Interrupt Mask

Address: 0x400F0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK [6:0]						

Bits	Name	Description
6 : 0	MSK	Interrupt Mask Register Default Value: 0

37.1.34 UDB_W8_MSK1

Interrupt Mask

Address: 0x400F0081

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK [6:0]						

Bits	Name	Description
6 : 0	MSK	Interrupt Mask Register Default Value: 0

37.1.35 UDB_W8_MSK2

Interrupt Mask

Address: 0x400F0082

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK [6:0]						

Bits	Name	Description
6 : 0	MSK	Interrupt Mask Register Default Value: 0

37.1.36 UDB_W8_MSK3

Interrupt Mask

Address: 0x400F0083

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK [6:0]						

Bits	Name	Description
6 : 0	MSK	Interrupt Mask Register Default Value: 0

37.1.37 UDB_W8_ACTL0

Auxiliary Control

Address: 0x400F0090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Bits	Name	Description
5	CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
4	INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
3	FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	FIFO1_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state

37.1.37 UDB_W8_ACTL0 (continued)

0	FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state

37.1.38 UDB_W8_ACTL1

Auxiliary Control

Address: 0x400F0091

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Bits	Name	Description
5	CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
4	INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
3	FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	FIFO1_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state

37.1.38 UDB_W8_ACTL1 (continued)

0	FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state

37.1.39 UDB_W8_ACTL2

Auxiliary Control

Address: 0x400F0092

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Bits	Name	Description
5	CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
4	INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
3	FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	FIFO1_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state

37.1.39 UDB_W8_ACTL2 (continued)

0	FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state

37.1.40 UDB_W8_ACTL3

Auxiliary Control

Address: 0x400F0093

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Bits	Name	Description
5	CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
4	INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
3	FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	FIFO1_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state

37.1.40 UDB_W8_ACTL3 (continued)

0	FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state

37.1.41 UDB_W8_MC0

PLD Macrocell reading

Address: 0x400F00A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC [7:4]				PLD0_MC [3:0]			

Bits	Name	Description
7 : 4	PLD1_MC	Read Macrocell 1 Default Value: 0
3 : 0	PLD0_MC	Read Macrocell 0 Default Value: 0

37.1.42 UDB_W8_MC1

PLD Macrocell reading

Address: 0x400F00A1

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC [7:4]				PLD0_MC [3:0]			

Bits	Name	Description
7 : 4	PLD1_MC	Read Macrocell 1 Default Value: 0
3 : 0	PLD0_MC	Read Macrocell 0 Default Value: 0

37.1.43 UDB_W8_MC2

PLD Macrocell reading

Address: 0x400F00A2

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC [7:4]				PLD0_MC [3:0]			

Bits	Name	Description
7 : 4	PLD1_MC	Read Macrocell 1 Default Value: 0
3 : 0	PLD0_MC	Read Macrocell 0 Default Value: 0

37.1.44 UDB_W8_MC3

PLD Macrocell reading

Address: 0x400F00A3

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC [7:4]				PLD0_MC [3:0]			

Bits	Name	Description
7 : 4	PLD1_MC	Read Macrocell 1 Default Value: 0
3 : 0	PLD0_MC	Read Macrocell 0 Default Value: 0

38 WRK16CAT Registers

This section discusses the UDB 16-bit Concatenated Working (WRK16CAT) registers. It lists all the registers in mapping tables, in address order.

38.1 Register Details

Register Name	Address
UDB_CAT16_A0	0x400F1000
UDB_CAT16_A1	0x400F1002
UDB_CAT16_A2	0x400F1004
UDB_CAT16_A3	0x400F1006
UDB_CAT16_D0	0x400F1040
UDB_CAT16_D1	0x400F1042
UDB_CAT16_D2	0x400F1044
UDB_CAT16_D3	0x400F1046
UDB_CAT16_F0	0x400F1080
UDB_CAT16_F1	0x400F1082
UDB_CAT16_F2	0x400F1084
UDB_CAT16_F3	0x400F1086
UDB_CAT16_CTL_ST0	0x400F10C0
UDB_CAT16_CTL_ST1	0x400F10C2
UDB_CAT16_CTL_ST2	0x400F10C4
UDB_CAT16_CTL_ST3	0x400F10C6
UDB_CAT16_ACTL_MSK0	0x400F1100
UDB_CAT16_ACTL_MSK1	0x400F1102
UDB_CAT16_ACTL_MSK2	0x400F1104
UDB_CAT16_ACTL_MSK3	0x400F1106
UDB_CAT16_MC0	0x400F1140
UDB_CAT16_MC1	0x400F1142
UDB_CAT16_MC2	0x400F1144
UDB_CAT16_MC3	0x400F1146

38.1.1 UDB_CAT16_A0

Accumulator Registers {A1,A0}

Address: 0x400F1000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A1 [15:8]							

Bits	Name	Description
15 : 8	A1	Accumulator 1 Register Default Value: 0
7 : 0	A0	Accumulator 0 Register Default Value: 0

38.1.2 UDB_CAT16_A1

Accumulator Registers {A1,A0}

Address: 0x400F1002

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A1 [15:8]							

Bits	Name	Description
15 : 8	A1	Accumulator 1 Register Default Value: 0
7 : 0	A0	Accumulator 0 Register Default Value: 0

38.1.3 UDB_CAT16_A2

Accumulator Registers {A1,A0}

Address: 0x400F1004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A1 [15:8]							

Bits	Name	Description
15 : 8	A1	Accumulator 1 Register Default Value: 0
7 : 0	A0	Accumulator 0 Register Default Value: 0

38.1.4 UDB_CAT16_A3

Accumulator Registers {A1,A0}

Address: 0x400F1006

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A1 [15:8]							

Bits	Name	Description
15 : 8	A1	Accumulator 1 Register Default Value: 0
7 : 0	A0	Accumulator 0 Register Default Value: 0

38.1.5 UDB_CAT16_D0

Data Registers {D1,D0}

Address: 0x400F1040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1 [15:8]							

Bits	Name	Description
15 : 8	D1	Data 1 Register Default Value: 0
7 : 0	D0	Data 0 Register Default Value: 0

38.1.6 UDB_CAT16_D1

Data Registers {D1,D0}

Address: 0x400F1042

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1 [15:8]							

Bits	Name	Description
15 : 8	D1	Data 1 Register Default Value: 0
7 : 0	D0	Data 0 Register Default Value: 0

38.1.7 UDB_CAT16_D2

Data Registers {D1,D0}

Address: 0x400F1044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1 [15:8]							

Bits	Name	Description
15 : 8	D1	Data 1 Register Default Value: 0
7 : 0	D0	Data 0 Register Default Value: 0

38.1.8 UDB_CAT16_D3

Data Registers {D1,D0}

Address: 0x400F1046

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1 [15:8]							

Bits	Name	Description
15 : 8	D1	Data 1 Register Default Value: 0
7 : 0	D0	Data 0 Register Default Value: 0

38.1.9 UDB_CAT16_F0

FIFOs {F1,F0}

Address: 0x400F1080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1 [15:8]							

Bits	Name	Description
15 : 8	F1	FIFO 1 Default Value: X
7 : 0	F0	FIFO 0 Default Value: X

38.1.10 UDB_CAT16_F1

FIFOs {F1,F0}

Address: 0x400F1082

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1 [15:8]							

Bits	Name	Description
15 : 8	F1	FIFO 1 Default Value: X
7 : 0	F0	FIFO 0 Default Value: X

38.1.11 UDB_CAT16_F2

FIFOs {F1,F0}

Address: 0x400F1084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1 [15:8]							

Bits	Name	Description
15 : 8	F1	FIFO 1 Default Value: X
7 : 0	F0	FIFO 0 Default Value: X

38.1.12 UDB_CAT16_F3

FIFOs {F1,F0}

Address: 0x400F1086

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1 [15:8]							

Bits	Name	Description
15 : 8	F1	FIFO 1 Default Value: X
7 : 0	F0	FIFO 0 Default Value: X

38.1.13 UDB_CAT16_CTL_ST0

Status and Control Registers {CTL,ST}

Address: 0x400F10C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL [15:8]							

Bits	Name	Description
15 : 8	CTL	Control Register Default Value: 0
7 : 0	ST	Status Register Default Value: 0

38.1.14 UDB_CAT16_CTL_ST1

Status and Control Registers {CTL,ST}

Address: 0x400F10C2

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL [15:8]							

Bits	Name	Description
15 : 8	CTL	Control Register Default Value: 0
7 : 0	ST	Status Register Default Value: 0

38.1.15 UDB_CAT16_CTL_ST2

Status and Control Registers {CTL,ST}

Address: 0x400F10C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL [15:8]							

Bits	Name	Description
15 : 8	CTL	Control Register Default Value: 0
7 : 0	ST	Status Register Default Value: 0

38.1.16 UDB_CAT16_CTL_ST3

Status and Control Registers {CTL,ST}

Address: 0x400F10C6

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL [15:8]							

Bits	Name	Description
15 : 8	CTL	Control Register Default Value: 0
7 : 0	ST	Status Register Default Value: 0

38.1.17 UDB_CAT16_ACTL_MSK0

Mask and Auxiliary Control Registers {ACTL,MSK}

Address: 0x400F1100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MSK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Bits	Name	Description
13	CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
9	FIFO1_CLR	FIFO clear Default Value: 0

38.1.17 UDB_CAT16_ACTL_MSK0 (continued)

		0x0: NORMAL: Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
8	FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
7 : 0	MSK	Interrupt Mask Register Default Value: 0

38.1.18 UDB_CAT16_ACTL_MSK1

Mask and Auxiliary Control Registers {ACTL,MSK}

Address: 0x400F1102

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MSK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Bits	Name	Description
13	CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
9	FIFO1_CLR	FIFO clear Default Value: 0

38.1.18 UDB_CAT16_ACTL_MSK1 (continued)

		0x0: NORMAL: Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
8	FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
7 : 0	MSK	Interrupt Mask Register Default Value: 0

38.1.19 UDB_CAT16_ACTL_MSK2

Mask and Auxiliary Control Registers {ACTL,MSK}

Address: 0x400F1104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MSK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Bits	Name	Description
13	CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
9	FIFO1_CLR	FIFO clear Default Value: 0

38.1.19 UDB_CAT16_ACTL_MSK2 (continued)

		0x0: NORMAL: Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
8	FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
7 : 0	MSK	Interrupt Mask Register Default Value: 0

38.1.20 UDB_CAT16_ACTL_MSK3

Mask and Auxiliary Control Registers {ACTL,MSK}

Address: 0x400F1106

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MSK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Bits	Name	Description
13	CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
9	FIFO1_CLR	FIFO clear Default Value: 0

38.1.20 UDB_CAT16_ACTL_MSK3 (continued)

		0x0: NORMAL: Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
8	FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
7 : 0	MSK	Interrupt Mask Register Default Value: 0

38.1.21 UDB_CAT16_MC0

PLD Macrocell Read Registers {00,MC}

Address: 0x400F1140

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	PLD1_MC [7:4]				PLD0_MC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PLD1_MC	PLD1 Macrocell Read Register Default Value: 0
3 : 0	PLD0_MC	PLD0 Macrocell Read Register Default Value: 0

38.1.22 UDB_CAT16_MC1

PLD Macrocell Read Registers {00,MC}

Address: 0x400F1142

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	PLD1_MC [7:4]				PLD0_MC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PLD1_MC	PLD1 Macrocell Read Register Default Value: 0
3 : 0	PLD0_MC	PLD0 Macrocell Read Register Default Value: 0

38.1.23 UDB_CAT16_MC2

PLD Macrocell Read Registers {00,MC}

Address: 0x400F1144

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	PLD1_MC [7:4]				PLD0_MC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PLD1_MC	PLD1 Macrocell Read Register Default Value: 0
3 : 0	PLD0_MC	PLD0 Macrocell Read Register Default Value: 0

38.1.24 UDB_CAT16_MC3

PLD Macrocell Read Registers {00,MC}

Address: 0x400F1146

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	PLD1_MC [7:4]				PLD0_MC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PLD1_MC	PLD1 Macrocell Read Register Default Value: 0
3 : 0	PLD0_MC	PLD0 Macrocell Read Register Default Value: 0

39 UDB 16-Bit Working (WRK16DEF) Registers

This section discusses the WRK16DEF registers. It lists all the registers in mapping tables, in address order.

39.1 Register Details

Register Name	Address
UDB_W16_A00	0x400F1000
UDB_W16_A01	0x400F1002
UDB_W16_A02	0x400F1004
UDB_W16_A10	0x400F1020
UDB_W16_A11	0x400F1022
UDB_W16_A12	0x400F1024
UDB_W16_D00	0x400F1040
UDB_W16_D01	0x400F1042
UDB_W16_D02	0x400F1044
UDB_W16_D10	0x400F1060
UDB_W16_D11	0x400F1062
UDB_W16_D12	0x400F1064
UDB_W16_F00	0x400F1080
UDB_W16_F01	0x400F1082
UDB_W16_F02	0x400F1084
UDB_W16_F10	0x400F10A0
UDB_W16_F11	0x400F10A2
UDB_W16_F12	0x400F10A4
UDB_W16_ST0	0x400F10C0
UDB_W16_ST1	0x400F10C2
UDB_W16_ST2	0x400F10C4
UDB_W16_CTL0	0x400F10E0
UDB_W16_CTL1	0x400F10E2
UDB_W16_CTL2	0x400F10E4
UDB_W16_MSK0	0x400F1100
UDB_W16_MSK1	0x400F1102
UDB_W16_MSK2	0x400F1104

Register Name	Address
UDB_W16_ACTL0	0x400F1120
UDB_W16_ACTL1	0x400F1122
UDB_W16_ACTL2	0x400F1124
UDB_W16_MC0	0x400F1140
UDB_W16_MC1	0x400F1142
UDB_W16_MC2	0x400F1144

39.1.1 UDB_W16_A00

Accumulator 0

Address: 0x400F1000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A0_MS [15:8]							

Bits	Name	Description
15 : 8	A0_MS	Accumulator 0 for UDB[n+1] Default Value: 0
7 : 0	A0_LS	Accumulator 0 for UDB[n] Default Value: 0

39.1.2 UDB_W16_A01

Accumulator 0

Address: 0x400F1002

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A0_MS [15:8]							

Bits	Name	Description
15 : 8	A0_MS	Accumulator 0 for UDB[n+1] Default Value: 0
7 : 0	A0_LS	Accumulator 0 for UDB[n] Default Value: 0

39.1.3 UDB_W16_A02

Accumulator 0

Address: 0x400F1004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A0_MS [15:8]							

Bits	Name	Description
15 : 8	A0_MS	Accumulator 0 for UDB[n+1] Default Value: 0
7 : 0	A0_LS	Accumulator 0 for UDB[n] Default Value: 0

39.1.4 UDB_W16_A10

Accumulator 1

Address: 0x400F1020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A1_MS [15:8]							

Bits	Name	Description
15 : 8	A1_MS	Accumulator 1 for UDB[n+1] Default Value: 0
7 : 0	A1_LS	Accumulator 1 for UDB[n] Default Value: 0

39.1.5 UDB_W16_A11

Accumulator 1

Address: 0x400F1022

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A1_MS [15:8]							

Bits	Name	Description
15 : 8	A1_MS	Accumulator 1 for UDB[n+1] Default Value: 0
7 : 0	A1_LS	Accumulator 1 for UDB[n] Default Value: 0

39.1.6 UDB_W16_A12

Accumulator 1

Address: 0x400F1024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A1_MS [15:8]							

Bits	Name	Description
15 : 8	A1_MS	Accumulator 1 for UDB[n+1] Default Value: 0
7 : 0	A1_LS	Accumulator 1 for UDB[n] Default Value: 0

39.1.7 UDB_W16_D00

Data 0

Address: 0x400F1040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D0_MS [15:8]							

Bits	Name	Description
15 : 8	D0_MS	Data 0 for UDB[n+1] Default Value: 0
7 : 0	D0_LS	Data 0 for UDB[n] Default Value: 0

39.1.8 UDB_W16_D01

Data 0

Address: 0x400F1042

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D0_MS [15:8]							

Bits	Name	Description
15 : 8	D0_MS	Data 0 for UDB[n+1] Default Value: 0
7 : 0	D0_LS	Data 0 for UDB[n] Default Value: 0

39.1.9 UDB_W16_D02

Data 0

Address: 0x400F1044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D0_MS [15:8]							

Bits	Name	Description
15 : 8	D0_MS	Data 0 for UDB[n+1] Default Value: 0
7 : 0	D0_LS	Data 0 for UDB[n] Default Value: 0

39.1.10 UDB_W16_D10

Data 1

Address: 0x400F1060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1_MS [15:8]							

Bits	Name	Description
15 : 8	D1_MS	Data 1 for UDB[n+1] Default Value: 0
7 : 0	D1_LS	Data 1 for UDB[n] Default Value: 0

39.1.11 UDB_W16_D11

Data 1

Address: 0x400F1062

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1_MS [15:8]							

Bits	Name	Description
15 : 8	D1_MS	Data 1 for UDB[n+1] Default Value: 0
7 : 0	D1_LS	Data 1 for UDB[n] Default Value: 0

39.1.12 UDB_W16_D12

Data 1

Address: 0x400F1064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1_MS [15:8]							

Bits	Name	Description
15 : 8	D1_MS	Data 1 for UDB[n+1] Default Value: 0
7 : 0	D1_LS	Data 1 for UDB[n] Default Value: 0

39.1.13 UDB_W16_F00

FIFO 0

Address: 0x400F1080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F0_MS [15:8]							

Bits	Name	Description
15 : 8	F0_MS	Fifo 0 for UDB[n+1] Default Value: X
7 : 0	F0_LS	Fifo 0 for UDB[n] Default Value: X

39.1.14 UDB_W16_F01

FIFO 0

Address: 0x400F1082

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F0_MS [15:8]							

Bits	Name	Description
15 : 8	F0_MS	Fifo 0 for UDB[n+1] Default Value: X
7 : 0	F0_LS	Fifo 0 for UDB[n] Default Value: X

39.1.15 UDB_W16_F02

FIFO 0

Address: 0x400F1084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F0_MS [15:8]							

Bits	Name	Description
15 : 8	F0_MS	Fifo 0 for UDB[n+1] Default Value: X
7 : 0	F0_LS	Fifo 0 for UDB[n] Default Value: X

39.1.16 UDB_W16_F10

FIFO 1

Address: 0x400F10A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1_MS [15:8]							

Bits	Name	Description
15 : 8	F1_MS	Fifo 1 for UDB[n+1] Default Value: X
7 : 0	F1_LS	Fifo 1 for UDB[n] Default Value: X

39.1.17 UDB_W16_F11

FIFO 1

Address: 0x400F10A2

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1_MS [15:8]							

Bits	Name	Description
15 : 8	F1_MS	Fifo 1 for UDB[n+1] Default Value: X
7 : 0	F1_LS	Fifo 1 for UDB[n] Default Value: X

39.1.18 UDB_W16_F12

FIFO 1

Address: 0x400F10A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1_MS [15:8]							

Bits	Name	Description
15 : 8	F1_MS	Fifo 1 for UDB[n+1] Default Value: X
7 : 0	F1_LS	Fifo 1 for UDB[n] Default Value: X

39.1.19 UDB_W16_ST0

Status Register

Address: 0x400F10C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ST_MS [15:8]							

Bits	Name	Description
15 : 8	ST_MS	Status register for UDB[n+1] Default Value: 0
7 : 0	ST_LS	Status register for UDB[n] Default Value: 0

39.1.20 UDB_W16_ST1

Status Register

Address: 0x400F10C2

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ST_MS [15:8]							

Bits	Name	Description
15 : 8	ST_MS	Status register for UDB[n+1] Default Value: 0
7 : 0	ST_LS	Status register for UDB[n] Default Value: 0

39.1.21 UDB_W16_ST2

Status Register

Address: 0x400F10C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ST_MS [15:8]							

Bits	Name	Description
15 : 8	ST_MS	Status register for UDB[n+1] Default Value: 0
7 : 0	ST_LS	Status register for UDB[n] Default Value: 0

39.1.22 UDB_W16_CTL0

Control Register

Address: 0x400F10E0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL_MS [15:8]							

Bits	Name	Description
15 : 8	CTL_MS	Control register for UDB[n+1] Default Value: 0
7 : 0	CTL_LS	Control register for UDB[n] Default Value: 0

39.1.23 UDB_W16_CTL1

Control Register

Address: 0x400F10E2

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL_MS [15:8]							

Bits	Name	Description
15 : 8	CTL_MS	Control register for UDB[n+1] Default Value: 0
7 : 0	CTL_LS	Control register for UDB[n] Default Value: 0

39.1.24 UDB_W16_CTL2

Control Register

Address: 0x400F10E4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL_MS [15:8]							

Bits	Name	Description
15 : 8	CTL_MS	Control register for UDB[n+1] Default Value: 0
7 : 0	CTL_LS	Control register for UDB[n] Default Value: 0

39.1.25 UDB_W16_MSK0

Interrupt Mask

Address: 0x400F1100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_LS [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_MS [14:8]						

Bits	Name	Description
14 : 8	MSK_MS	Interrupt Mask Register Default Value: 0
6 : 0	MSK_LS	Interrupt Mask Register Default Value: 0

39.1.26 UDB_W16_MSK1

Interrupt Mask

Address: 0x400F1102

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_LS [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_MS [14:8]						

Bits	Name	Description
14 : 8	MSK_MS	Interrupt Mask Register Default Value: 0
6 : 0	MSK_LS	Interrupt Mask Register Default Value: 0

39.1.27 UDB_W16_MSK2

Interrupt Mask

Address: 0x400F1104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_LS [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_MS [14:8]						

Bits	Name	Description
14 : 8	MSK_MS	Interrupt Mask Register Default Value: 0
6 : 0	MSK_LS	Interrupt Mask Register Default Value: 0

39.1.28 UDB_W16_ACTL0

Auxiliary Control

Address: 0x400F1120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Bits	Name	Description
13	CNT_START_MS	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	INT_EN_MS	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	FIFO1_LVL_MS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL_MS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

39.1.28 UDB_W16_ACTL0 (continued)

9	FIFO1_CLR_MS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
8	FIFO0_CLR_MS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
5	CNT_START_LS	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
4	INT_EN_LS	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
3	FIFO1_LVL_LS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	FIFO0_LVL_LS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	FIFO1_CLR_LS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
0	FIFO0_CLR_LS	FIFO clear Default Value: 0

39.1.28 UDB_W16_ACTL0 (continued)

0x0: NORMAL:
Normal FIFO operation

0x1: CLEAR:
Clear FIFO state

39.1.29 UDB_W16_ACTL1

Auxiliary Control

Address: 0x400F1122

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Bits	Name	Description
13	CNT_START_MS	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	INT_EN_MS	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	FIFO1_LVL_MS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL_MS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

39.1.29 UDB_W16_ACTL1 (continued)

9	FIFO1_CLR_MS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
8	FIFO0_CLR_MS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
5	CNT_START_LS	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
4	INT_EN_LS	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
3	FIFO1_LVL_LS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	FIFO0_LVL_LS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	FIFO1_CLR_LS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
0	FIFO0_CLR_LS	FIFO clear Default Value: 0

39.1.29 UDB_W16_ACTL1 (continued)

0x0: NORMAL:
Normal FIFO operation

0x1: CLEAR:
Clear FIFO state

39.1.30 UDB_W16_ACTL2

Auxiliary Control

Address: 0x400F1124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Bits	Name	Description
13	CNT_START_MS	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	INT_EN_MS	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	FIFO1_LVL_MS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL_MS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

39.1.30 UDB_W16_ACTL2 (continued)

9	FIFO1_CLR_MS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
8	FIFO0_CLR_MS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
5	CNT_START_LS	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
4	INT_EN_LS	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
3	FIFO1_LVL_LS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	FIFO0_LVL_LS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	FIFO1_CLR_LS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
0	FIFO0_CLR_LS	FIFO clear Default Value: 0

39.1.30 UDB_W16_ACTL2 (continued)

0x0: NORMAL:
Normal FIFO operation

0x1: CLEAR:
Clear FIFO state

39.1.31 UDB_W16_MC0

PLD Macrocell reading

Address: 0x400F1140

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_LS [7:4]				PLD0_MC_LS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_MS [15:12]				PLD0_MC_MS [11:8]			

Bits	Name	Description
15 : 12	PLD1_MC_MS	Read Macrocell 1 for UDB[n+1] Default Value: 0
11 : 8	PLD0_MC_MS	Read Macrocell 0 for UDB[n+1] Default Value: 0
7 : 4	PLD1_MC_LS	Read Macrocell 1 for UDB[n] Default Value: 0
3 : 0	PLD0_MC_LS	Read Macrocell 0 for UDB[n] Default Value: 0

39.1.32 UDB_W16_MC1

PLD Macrocell reading

Address: 0x400F1142

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_LS [7:4]				PLD0_MC_LS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_MS [15:12]				PLD0_MC_MS [11:8]			

Bits	Name	Description
15 : 12	PLD1_MC_MS	Read Macrocell 1 for UDB[n+1] Default Value: 0
11 : 8	PLD0_MC_MS	Read Macrocell 0 for UDB[n+1] Default Value: 0
7 : 4	PLD1_MC_LS	Read Macrocell 1 for UDB[n] Default Value: 0
3 : 0	PLD0_MC_LS	Read Macrocell 0 for UDB[n] Default Value: 0

39.1.33 UDB_W16_MC2

PLD Macrocell reading

Address: 0x400F1144

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_LS [7:4]				PLD0_MC_LS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_MS [15:12]				PLD0_MC_MS [11:8]			

Bits	Name	Description
15 : 12	PLD1_MC_MS	Read Macrocell 1 for UDB[n+1] Default Value: 0
11 : 8	PLD0_MC_MS	Read Macrocell 0 for UDB[n+1] Default Value: 0
7 : 4	PLD1_MC_LS	Read Macrocell 1 for UDB[n] Default Value: 0
3 : 0	PLD0_MC_LS	Read Macrocell 0 for UDB[n] Default Value: 0

40 UDB 32-Bit Working (WRK32) Registers

This section discusses the WRK32 registers. It lists all the registers in mapping tables, in address order.

40.1 Register Details

Register Name	Address
UDB_W32_A0	0x400F2000
UDB_W32_A1	0x400F2040
UDB_W32_D0	0x400F2080
UDB_W32_D1	0x400F20C0
UDB_W32_F0	0x400F2100
UDB_W32_F1	0x400F2140
UDB_W32_ST	0x400F2180
UDB_W32_CTL	0x400F21C0
UDB_W32_MSK	0x400F2200
UDB_W32_ACTL	0x400F2240
UDB_W32_MC	0x400F2280

40.1.1 UDB_W32_A0

Accumulator 0

Address: 0x400F2000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A0_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	A0_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	A0_3 [31:24]							

Bits	Name	Description
31 : 24	A0_3	Accumulator 0 for UDB[n+3] Default Value: 0
23 : 16	A0_2	Accumulator 0 for UDB[n+2] Default Value: 0
15 : 8	A0_1	Accumulator 0 for UDB[n+1] Default Value: 0
7 : 0	A0_0	Accumulator 0 for UDB[n] Default Value: 0

40.1.2 UDB_W32_A1

Accumulator 1

Address: 0x400F2040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A1_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A1_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	A1_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	A1_3 [31:24]							

Bits	Name	Description
31 : 24	A1_3	Accumulator 1 for UDB[n+3] Default Value: 0
23 : 16	A1_2	Accumulator 1 for UDB[n+2] Default Value: 0
15 : 8	A1_1	Accumulator 1 for UDB[n+1] Default Value: 0
7 : 0	A1_0	Accumulator 1 for UDB[n] Default Value: 0

40.1.3 UDB_W32_D0

Data 0

Address: 0x400F2080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D0_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	D0_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	D0_3 [31:24]							

Bits	Name	Description
31 : 24	D0_3	Data 0 for UDB[n+3] Default Value: 0
23 : 16	D0_2	Data 0 for UDB[n+2] Default Value: 0
15 : 8	D0_1	Data 0 for UDB[n+1] Default Value: 0
7 : 0	D0_0	Data 0 for UDB[n] Default Value: 0

40.1.4 UDB_W32_D1

Data 1

Address: 0x400F20C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D1_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	D1_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	D1_3 [31:24]							

Bits	Name	Description
31 : 24	D1_3	Data 1 for UDB[n+3] Default Value: 0
23 : 16	D1_2	Data 1 for UDB[n+2] Default Value: 0
15 : 8	D1_1	Data 1 for UDB[n+1] Default Value: 0
7 : 0	D1_0	Data 1 for UDB[n] Default Value: 0

40.1.5 UDB_W32_F0

FIFO 0

Address: 0x400F2100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F0_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	F0_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	F0_3 [31:24]							

Bits	Name	Description
31 : 24	F0_3	Fifo 0 for UDB[n+3] Default Value: X
23 : 16	F0_2	Fifo 0 for UDB[n+2] Default Value: X
15 : 8	F0_1	Fifo 0 for UDB[n+1] Default Value: X
7 : 0	F0_0	Fifo 0 for UDB[n] Default Value: X

40.1.6 UDB_W32_F1

FIFO 1

Address: 0x400F2140

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F1_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	F1_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	F1_3 [31:24]							

Bits	Name	Description
31 : 24	F1_3	Fifo 1 for UDB[n+3] Default Value: X
23 : 16	F1_2	Fifo 1 for UDB[n+2] Default Value: X
15 : 8	F1_1	Fifo 1 for UDB[n+1] Default Value: X
7 : 0	F1_0	Fifo 1 for UDB[n] Default Value: X

40.1.7 UDB_W32_ST

Status Register

Address: 0x400F2180

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ST_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ST_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ST_3 [31:24]							

Bits	Name	Description
31 : 24	ST_3	Status register for UDB[n+3] Default Value: 0
23 : 16	ST_2	Status register for UDB[n+2] Default Value: 0
15 : 8	ST_1	Status register for UDB[n+1] Default Value: 0
7 : 0	ST_0	Status register for UDB[n] Default Value: 0

40.1.8 UDB_W32_CTL

Control Register

Address: 0x400F21C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CTL_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CTL_3 [31:24]							

Bits	Name	Description
31 : 24	CTL_3	Control register for UDB[n+3] Default Value: 0
23 : 16	CTL_2	Control register for UDB[n+2] Default Value: 0
15 : 8	CTL_1	Control register for UDB[n+1] Default Value: 0
7 : 0	CTL_0	Control register for UDB[n] Default Value: 0

40.1.9 UDB_W32_MSK

Interrupt Mask

Address: 0x400F2200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_0 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_1 [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_2 [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_3 [30:24]						

Bits	Name	Description
30 : 24	MSK_3	Interrupt Mask Register Default Value: 0
22 : 16	MSK_2	Interrupt Mask Register Default Value: 0
14 : 8	MSK_1	Interrupt Mask Register Default Value: 0
6 : 0	MSK_0	Interrupt Mask Register Default Value: 0

40.1.10 UDB_W32_ACTL

Auxiliary Control

Address: 0x400F2240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		CNT_START_0	INT_EN_0	FIFO1_LVL_0	FIFO0_LVL_0	FIFO1_CLR_0	FIFO0_CLR_0

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		CNT_START_1	INT_EN_1	FIFO1_LVL_1	FIFO0_LVL_1	FIFO1_CLR_1	FIFO0_CLR_1

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [23:22]		CNT_START_2	INT_EN_2	FIFO1_LVL_2	FIFO0_LVL_2	FIFO1_CLR_2	FIFO0_CLR_2

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [31:30]		CNT_START_3	INT_EN_3	FIFO1_LVL_3	FIFO0_LVL_3	FIFO1_CLR_3	FIFO0_CLR_3

Bits	Name	Description
29	CNT_START_3	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
28	INT_EN_3	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled

40.1.10 UDB_W32_ACTL (continued)

27	FIFO1_LVL_3	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
26	FIFO0_LVL_3	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
25	FIFO1_CLR_3	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
24	FIFO0_CLR_3	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
21	CNT_START_2	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
20	INT_EN_2	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
19	FIFO1_LVL_2	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
18	FIFO0_LVL_2	FIFO fill status level control Default Value: 0

40.1.10 UDB_W32_ACTL (continued)

		0x0: NORMAL: input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
17	FIFO1_CLR_2	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
16	FIFO0_CLR_2	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
13	CNT_START_1	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	INT_EN_1	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	FIFO1_LVL_1	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL_1	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
9	FIFO1_CLR_1	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation

40.1.10 UDB_W32_ACTL (continued)

		0x1: CLEAR: Clear FIFO state
8	FIFO0_CLR_1	FIFO clear Default Value: 0
		0x0: NORMAL: Normal FIFO operation
		0x1: CLEAR: Clear FIFO state
5	CNT_START_0	Control Register Counter Enable Default Value: 0
		0x0: DISABLE: Counter disabled
		0x1: ENABLE: Counter enabled
4	INT_EN_0	enable interrupt Default Value: 0
		0x0: DISABLE: Interrupt disabled
		0x1: ENABLE: Interrupt enabled
3	FIFO1_LVL_0	FIFO fill status level control Default Value: 0
		0x0: NORMAL: input mode: FIFO not full; output mode: FIFO not empty
		0x1: MID: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	FIFO0_LVL_0	FIFO fill status level control Default Value: 0
		0x0: NORMAL: input mode: FIFO not full; output mode: FIFO not empty
		0x1: MID: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	FIFO1_CLR_0	FIFO clear Default Value: 0
		0x0: NORMAL: Normal FIFO operation
		0x1: CLEAR: Clear FIFO state
0	FIFO0_CLR_0	FIFO clear Default Value: 0
		0x0: NORMAL: Normal FIFO operation
		0x1: CLEAR: Clear FIFO state

40.1.11 UDB_W32_MC

PLD Macrocell reading

Address: 0x400F2280

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_0 [7:4]				PLD0_MC_0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_1 [15:12]				PLD0_MC_1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_2 [23:20]				PLD0_MC_2 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_3 [31:28]				PLD0_MC_3 [27:24]			

Bits	Name	Description
31 : 28	PLD1_MC_3	Read Macrocell 1 for UDB[n+3] Default Value: 0
27 : 24	PLD0_MC_3	Read Macrocell 0 for UDB[n+3] Default Value: 0
23 : 20	PLD1_MC_2	Read Macrocell 1 for UDB[n+2] Default Value: 0
19 : 16	PLD0_MC_2	Read Macrocell 0 for UDB[n+2] Default Value: 0
15 : 12	PLD1_MC_1	Read Macrocell 1 for UDB[n+1] Default Value: 0
11 : 8	PLD0_MC_1	Read Macrocell 0 for UDB[n+1] Default Value: 0
7 : 4	PLD1_MC_0	Read Macrocell 1 for UDB[n] Default Value: 0
3 : 0	PLD0_MC_0	Read Macrocell 0 for UDB[n] Default Value: 0

Revision History

Revision History

Document Title: PSoC 4100M/4200M FAMILY PSoC(R) 4 Registers Technical Reference Manual (TRM) Document Number: 001-95235				
Revision	**ECN#**	**Issue Date**	**Origin of Change**	**Description of Change**
**	4579479	11/25/2014	NIDH	Specification for new silicon
*A	4748862	05/05/2014	NIDH	Added Acronyms Updated GPIO Port Registers section Removed PWR_BG_CONFIG register Updating HSIOM Port Registers section
*B	4878549	2/22/2016	NIDH	Updated Register General Conventions Added Acronyms Updated CapSense Sigma Delta (CSD) Registers Updated Watch Crystal Oscillator (WCO) Registers
*C	5760861	06/02/2017	SHEA	Updated logo and copyright information
*D	5993780	02/07/2018	NIDH	Sunset Review