Sl. No.	Section	Subsection	Change Description	Current Spec *E content	New Spec *F content	Reason for change	Customer Impact
1	All	All	Traveo™ II naming	Traveo™ II	TRAVEO™ T2G	Infineon standard naming alignment	None
2	All	All	Trigger MUX signal name	Generic signal	Signal name aligned with Datasheet	Update	None
3	1.1.4 Audio Subsystem		Correction	Inter-IC sound (I2S) interfaces based on NXP I2S bus specifications are supported to connect digital audio devices	Inter-IC sound (I2S) interfaces to connect digital audio devices	Correction	None
4	1.2.1 CPU Subsystem	1.2.2.4IMO Clock Source	IMO Tolerence removed	The IMO operates at a frequency of 8 MHz ±1%. The internal trim settings for the IMO can be dynamically updated to provide a tolerance of less than 1%.	The IMO operates at a frequency around 8 MHz.	To be referred to from device specific datasheet	None
5	7.1.8 P-DMA Descriptor Structure	Description	Added description	DESCR_X_CTL - Descriptor X loop control	DESCR_X_CTL - Descriptor X loop control This register is not present for a single transfer descriptor type.	Add information	None
6	7.1.8 P-DMA Descriptor Structure	Description	Added description	DESCR_NEXT_PTR - Descriptor next pointer Note: For a single transfer descriptor type, this register is at offset 0x0c. For a 1D transfer descriptor type, this register is at offset 0x.	DESCR_NEXT_PTR - Descriptor next pointer Note: For a single transfer descriptor type, this register is at offset 0x0c. For 1D and CRC transfer descriptor types, this register is at offset 0x10. For a 2D transfer descriptor type, this register is at offset 0x14.	Add information	None
7	7.3.2 Channels	Description	Added description	none	Trigger multiplexer may not offer for connecting the output triggers of the M-DMA controller and the P-DMA controller to the input triggers of the AXI DMA controller. These triggers can be performed in software, by chaining a descriptor that writes the AXI_DMAC_CHx_TR_CMD register of the AXI DMA controller channel.	Add information	None
8	7.1.6 P-DMA Controller Design	Figure 7-5. P-DMA Controller Design	Changed signal name	tr_in[] tr_out[]	PDMAx_TR_INy PDMAx_TR_OUTy	Synced with the Datasheets.	None
9	7.1.6 P-DMA Controller Design	Figure 7-6. P-DMA Controller Flow	Changed signal name	tr_in[] tr_out[]	PDMAx_TR_INy PDMAx_TR_OUTy	Synced with the Datasheets.	None
10	7.2.6 M-DMA Controller Design	Figure 7-14. M-DMA Controller Design	Changed signal name	tr_in[] tr_iin[0] tr_iin[1] tr_iin[CH_NR-1] tr_out[]	MDMA_TR_INy MDMA_TR_IN0 MDMA_TR_IN1 MDMA_TR_INy (y=CH_NR-1) MDMA_TR_OUTy	Synced with the Datasheets.	None
11	7.3.7 AXI DMA Controller Design	Figure 7-21. AXI DMA Controller Design	Changed signal name	tr_in[] tr_iin[0] tr_iin[1] tr_iin[CH_NR-1] tr_out[]	AXIDMA_TR_INy AXIDMA_TR_IN0 AXIDMA_TR_IN1 AXIDMA_TR_INy (y=CH_NR-1) AXIDMA_TR_OUTy	Synced with the Datasheets.	None
12	11.3.2 Multicore Boot	Description	Add content	None	In addition, the CPUSS_CM4_PWR_CTL register is used to check current power mode. Note: The CPUSS_IDENTITY and the CPUSS_CM4_PWR_CTL registers are read from the CM4 master in boot process. Therefore, these registers must allow read access from the CM4 master in boot process.	Clarify operation of CM4 during BootROM	None
13	11.3.4.5 Security Enhancement PPU Configuration in Sflash	Description	Add content	None	11.3.4.5 Security Enhancement PPU Configuration in SFlash	Allignning with Device Enhancement	None
14	18 Clocking System	PLL with SSCG and Fractional Operation (400-MHz PLL)	Add a sentence	-	The configuration of this PLL is the same as PLL without SSCG and fractional operation. See 18.3.1 PLL without SSCG and Fractional Operation for details.	Adding information	Minor impact
15	18 Clocking System	PLL with SSCG and Fractional Operation (400-MHz PLL)	Add a sentence	-	Note that you cannot operate SSCG and fractional operation together.	Adding information	Minor impact
16	24.3.5 TX Handling	24.3.5.2Dedicated TX Buffers	NA	If multiple Tx Buffers are configured with the same Message ID, the Tx Buffer with the lowest buffer number is transmitted first.	These Tx buffers shall be requested in ascending order with lowest buffer number first. Alternatively all Tx buffers configured with the same Message ID can be requested simultaneously by a single write access to CANFDx_CHy_TXBAR.	Correction	Minor impact
17	24.3.5 TX Handling	24.3.5.4TX Queue	NA	If multiple queue buffers are configured with the same Message ID, the queue buffer with the lowest buffer number is transmitted first.	In case that multiple Tx Queue buffers are configured with the same Message ID, the transmission order depends on numbers of the buffers where the messages were stored for transmission. As these buffer numbers depend on the then current states of the PUT index, a prediction of the transmission order is not possible.	Correction	Minor impact
18	24.3.5 TX Handling	24.3.5.4TX Queue	NA	An Add Request cyclically increments the Put Index to the next free TX buffer.	The Put Index always points to the free buffer of the Tx Queue with the lowest buffer number.	Correction	Minor impact

Sl. No.	Section	Subsection	Change Description	Current Spec *E content	New Spec *F content	Reason for change	Customer Impact
19	24.5 TTCAN Operation	24.5.3 TTCAN Gap Control	NA	In time-triggered operation, bit Next_is_Gap = '1' in the reference message will be ignored, and the bits CANFDx_CHy_TTOCN.NIG, CANFDx_CHy_TTOCN.FGP, and CANFDx_CHy_TTOCN.TMG will be considered.	In time-triggered operation, bit Next_is_Gap = '1' in the reference message will be ignored, as well as the bits CANFDx_CHy_TTOCN.NIG, CANFDx_CHy_TTOCN.FGP, and CANFDx_CHy_TTOCN.TMG.	Correction	Minor impact
20	26. LIN	Block Diagram	figure replaced			signal name alignment with DS	No
21	28. Event Generator (EVTGEN)	DeepSleep Interrupt Accuracy Analysis	new			signal name alignment with DS	No
22	28. Event Generator (EVTGEN	all	trigger signal name changed			signal name alignment with DS	No
23	29.3 Trigger Multiplexing	NA	Trigger MUX signal name	The debug mode is indicated by the level trigger input tr_debug_freeze, which is connected to a CPUSS CTI trigger output, sys.tr_cti_out.	The debug mode is indicated by the level trigger input x_DEBUG_FREEZE_TR_IN1 , which is connected to a CPUSS CTI trigger output, CTI_TR_OUTx.	Alignment as per the datasheet	None
24	30.15 TRAVEO T2G specific functions		Trigger MUX signal name	Generic signal	Signal name aligned with Datasheet	Update	None
25	34. Audio Subsystem	-	Updated description	The Inter-IC Sound Bus (I2S) is a serial bus interface standard used to connect digital audio devices together. The specification is from Philips® Semiconductor (I2S bus specification: February 1986, revised June 5, 1996). In addition to the standard I2S format, the I2S block also supports the Left Justified (LJ) format and the Time Division Multiplexed (TDM) format.	The Inter-IC Sound Bus (I2S) is a serial bus interface standard used to connect digital audio devices together. In addition to the standard I2S format, the I2S block also supports the Left Justified (LJ) format and the Time Division Multiplexed (TDM) format.	Updated description	None
26	34. Audio Subsystem	1	Updated description	■ Supports standard Philips I2S, LJ, and eight-channel TDM digital audio interface formats	■ Supports standard I2S, LJ, and eight-channel TDM digital audio interface formats	Updated description	None
27	35.3 Operation	Note before figure 35-2 ADC Core Block Diagram	The peripheral clock divider for ADC (CLK_PERI) must be at least 2. The ePass SAR requires a 50/50 duty cycle clock; this is generated only when CLK_PERI is at least 2. ■ Do not divide CLK_GR9; this makes CLK_GR9 = CLK_PERI, keeping all clocks coming to SAR ADC at the same frequency. If these clocks are not equal, it can cause the GRP_CANCELLED bit to be set	Was missing in the *E spec and was added in *F spec, but was not added in the change log	The description has been added	Was required for clarity and avoid mistakes from Users	Yes
28	35.2 Block Diagram	Figure 35-1	Added signal names in the naming format for the trigger input and output in the block diagram	Names were missing	The description has been added	Was required for better understanding	None
29	35.5 SAR Sequencer	Figure 35-5	Added signal names in the naming format for the trigger input and output in the block diagram	Names were missing	The description has been added	Was required for better understanding	None
30	35.5.4 Averaging		**Added more description as below:** For true averaging, the averaging count needs to be a power of 2 and the right shift needs to be set to the corresponding value. For non-power of 2 averaging counts the right shift can only approximate the required divide. If a true averaging result is required, the software will need to do a divide. Note that the acquisitions for averaging are considered to be atomic, i.e. when the channel is aborted due to a preemption then the results are discarded and on return the averaging starts from scratch. On the flip side when the FINISH_RESUME preemption type is used, or in case of a debug freeze trigger, all averaging acquisitions are completed before the preemption or freeze happens	Not available in *F spec	The description has been added	Was required for better understanding	Yes
31	35.5.5 Right Shifting	NA	Added a new section for Right Shifting	Not available in *F spec	The description has been added	It is required for averaging	Yes
32	35.5.5 Right Shifting	Before 35.5.6	**Sentence rephrased:** The right shift post processing step takes the 20-bit output from the averaging step, then right shift by 4, resulting in an output of a 16-bit result by eliminating the 4 least significant bits.	**Earlier sentence:** The Right shift post processing step takes the 20-bit output from the averaging step and after the Right shift outputs a 16-bit result by dropping the top 4.	The description has been added	Was required for better understanding	None

Sl. No.	Section	Subsection	Change Description	Current Spec *E content	New Spec *F content	Reason for change	Customer Impact
33	35.6.2 Triggers	Before table 35-10	**Signal naming convention description added:** The input trigger signal naming convention is given below. TCPWM: PASS[x]:PASSx_CH_TR_IN[y] where x is instance and y is the channel y varies between 0-19 for TCPWM0 group 0 and y varies between 20-31 for TCPWM0 group 1 GENERIC: PASS:PASS_GEN_TR_IN[y] where y varies between 0 to 3. Freeze Pass0 during Debug: PASS:PASS_DEBUG_FREEZE_TR_IN	Not available in *F spec	The description has been added	Was required for better understanding	None
34	35.7.1 Trigger Outputs	Before 35.7.1.1 Channel Done Trigger	**Signal naming convention description added:** The trigger output signal naming convention is given below: x : instance, y : channel Range Violation : PASS[x]:PASSx_CH_RANGEVIO_TR_OUT[y] Channel Done : PASS[x]:PASSx_CH_DONE_TR_OUT[y] Generic : PASS[x]:PASSx_GEN_TR_OUT[y]	Not available in *F spec	The description has been added	Was required for better understanding	None
35	36.2.4 Embedded Cross-Triggering	Note	update Trigger signals naming	sys.tr_cti_in[0:1]/sys.tr_cti_out[0:1]	CTI_TR_IN[0:1]/CTI_TR_OUT[0:1]	harmonize Trigger Label as per datasheets	None
36	36.5 Pin Configuration of Debug Interface on BootROM	Note	Add decription	Information not present	add information for Pin Configuration of Debug Interface on BootROM	update information	None
37	37.4 System Calls	ConfigureRegulator	Bits [12:8] shall be fixed to 0x10	Mentions these bits need to be calculated based on required voltage	VADJ trim value (VadjTrim) used in the regulator output trim. This value should be fixed to 0x10 and is valid only for the "External transistor" operating mode.	documentation bug	Yes
38	38.3.4.3 TOC2 Structure	None	Add description about security update marker TOC2_SECURITY_UPDATES_MARKER	No description	The description has been added	Add description of the recently added field	Yes
39	38.3.2.3 Initialization	None	Add description of configuration for PERI_MS_PPU_FX_PERI_GR2_BOOT	No description	The description has been added	Add description of the recently added change	Yes
40	38.3.4.3 TOC2 Structure	None	Fix the default adress of signature verification key	SFlash row 59	Zero	To fix the mistake in the description	Yes
41	38.3.3 Flash Boot Flow			38.3.3.26 Set Error Code (30) Flash boot sets an error code into the IPC_STRUCT[2].DATA0 register.	38.3.3.26 Set Error Code (30) Flash boot sets an error code into the -IPC_STRUCT[2].DATA0 register for CM4 based devices -IPC_STRUCT[3].DATA0 register for CM7 based devices		Yes