POWER ELECTRONICS NEWS

Improvements in Performance and Voltage Range of SiC MOSFETs

July 12, 2024 Sonu Daryanani

This article highlights the performance advantages obtained with the recently released CoolSiC™ SiC MOSFETs G2 by Infineon Technologies.

Silicon Carbide (SiC) devices are gaining widespread acceptance in industrial and automotive applications such as the electric vehicle (EV) traction inverter and on-board charger, fast EV charging infrastructure, motor drives, photovoltaics, energy storage, solid-state transformers, etc. Continuous improvements in the performance and cost of these devices are essential for their growth in these and other new applications. In this article, we will highlight the performance advantages obtained with the recently released CoolSiC™ MOSFETs G2 by Infineon Technologies, which now includes a broader portfolio with the industry's first 400 V-rated SiC MOSFET.

The CoolSiC™ MOSFET G2

Infineon's CoolSiC™ MOSFETs feature state-of-the-art trench gate technology that enables several advantages such as superior gate oxide reliability as well as improved conduction and switching loss metrics. The G1 family, first introduced in 2017, includes several features that give it competitive performance advantages in hard switching, soft switching, and partial load applications. The robust and reliable platform features a wide gate voltage (VGS) range, a high threshold voltage (Vth) that prevents parasitic turn-on even at 0 V gate turn-off voltage, and robust body diode operation under hard commutation.

The field reliability rate in defects per million (DPM) on millions of SiC power switches, which include discrete devices and power modules, is better even than that seen on their Si devices. With increased power densities, the device packaging can play a vital role in its overall performance. The junction to case thermal resistance ($R_{th,\ j\text{-}c}$) can typically set the maximum power range of the device for the allowed rise in junction temperature (T_{vj}), and a smaller rate of rise of this temperature

translates to improved efficiency under partial load conditions due to a correspondingly smaller rise in the device on-state resistance $R_{DS(on)}$.

For a given power capability, improved Rth, j-c on a package or module can be used to simplify its cooling and create cost benefits. The reliability of the device can be many times limited by the packaging. SiC, in particular, has a higher Young's modulus than Si, which can create thermomechanical stress on solder joints. To alleviate the stress and strain on the SiC die, which can result in die delamination from the lead-frame, the CoolSiC™ G1 and G2 families use Infineon's proprietary .XT package interconnect technology. This involves diffusion soldering for extremely robust die attach, which improves not only reliability but also the R_{th}.

The G2 family introduced earlier this year builds on the foundation of the G1 technology. A cell shrink creates a price-performance improvement, while some added features improve some of the key device features. A summary of the enhancements is listed below:

- Around 5-20% reduced power losses over typical user load conditions
- $R_{th,\ j\text{-}c}$ reduction of 12% through improvements in the .XT technology
- Single-digit $R_{DS(on)}$ devices now available at both 650 V and 1200 V
- Wide maximum transient V_{GS} range to -10 V – +25 V
- A guaranteed short circuit withstand time of at least 2 µs and overload operation to a T_{vj} of 200 °C, for the 1200 V devices, under datasheet listed conditions
- Maintain high reliability of the G1 devices, with very low DPM rates

The comparison of the Figure of Merit (FOM) performance of the 1200 V G2 versus the G1 as well as other competitor 1200 V SiC devices is shown in Figure 1. The G2 delivers significant efficiency advantages in hard switching, soft switching, and partial load conditions. The low total gate charge Q_G for a given $R_{DS(on)}$ also leads to a lower gate drive power loss.

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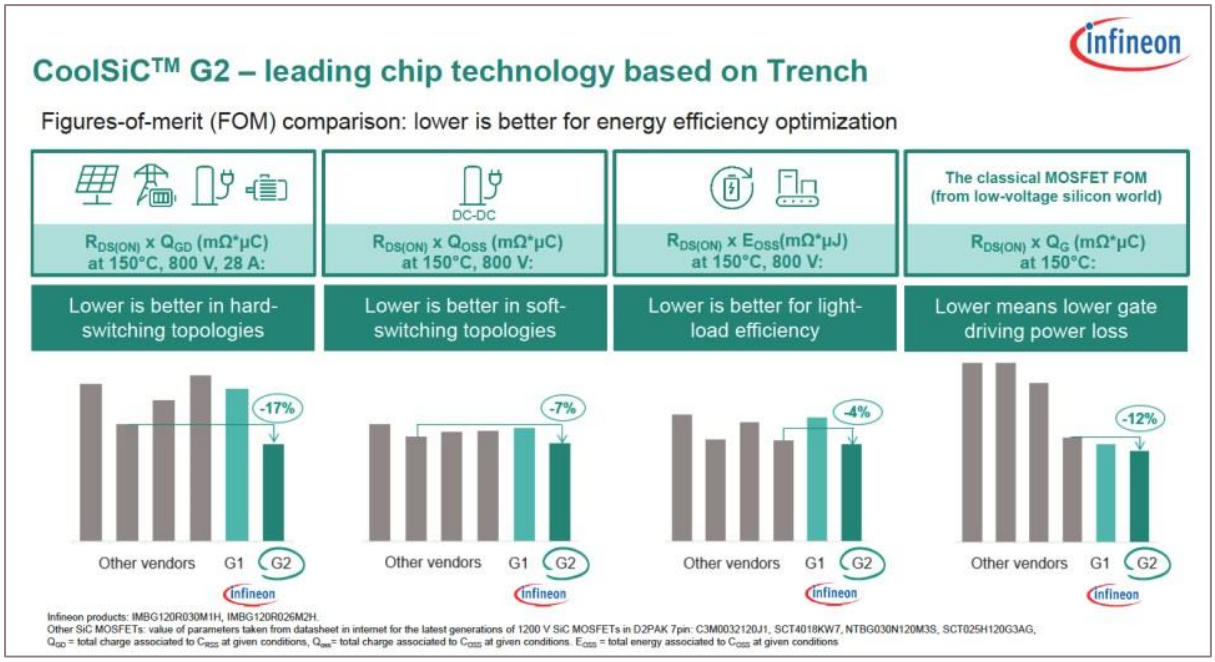


Figure 1: A comparison of some commonly used FOMs in power conversion (Source: Infineon Technologies)

The performance improvement obtained from the .XT package interconnect technology implemented on the G2 family is depicted in Figure 2. As shown, the improved $R_{th,\ j\text{-}c}$ of the G2 family enables a 6-7% increase in current or up to a 50% increase in switching frequency for a given T_{vj} or enables around a 5 K cooler temperature for the same power.

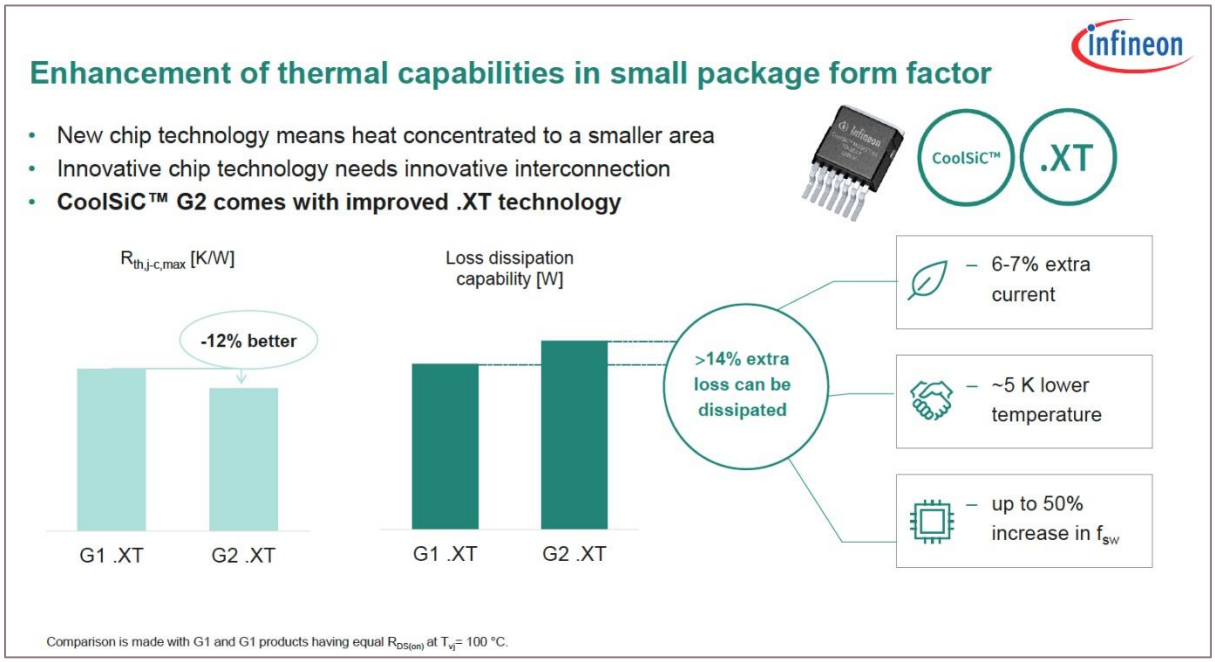


Figure 2: Improvements in the .XT packaging for the G2 family (Source: Infineon Technologies)

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The current release of the G2 family ranges from 400 V to 1200 V in a variety of packages that include the TOLL, D^{2}PAK-7, TO-247-3, TO-247-4 bottom side cooled, as well as the TOLT top side cooled package, the advantages of which are discussed below. Automotive grade Power HybridPACK™ Modules using the CoolSiC™ 750 V and 1200 V G2 devices are also in mass production for use in hybrid or fully electric vehicles and other motor drive applications.

Top Side Cooled Packages

The top side cooled (TSC) SMD, such as the TOLT package, combines the benefits of the robust thermal performance of the through-hole packages such as the TO-247 with the potential of fully automated handling available with SMD bottom side cooled packages. Another key advantage is that since the drain pad is now on top, the insulated bottom of the package allows it to be placed on a standard PCB that also includes digital ICs, gate drivers, and other magnetic components.

This eliminates the IMS board that would be used for the standard bottom cooled power device and hence simplifies the overall design, as depicted in Figure 3 for a servo motor drive application. Aside from the cost advantages, a reduction in stray inductances can lead to system performance advantages. A rollout of more TSC G2 CoolSiC™ products is planned for the near future, including a 650 V TSC Thin-TOLL 8×8, 1200 V Q-DPACK Half Bridge, and Q-DPACKs is a range of various $R_{DS(on)}$'s.

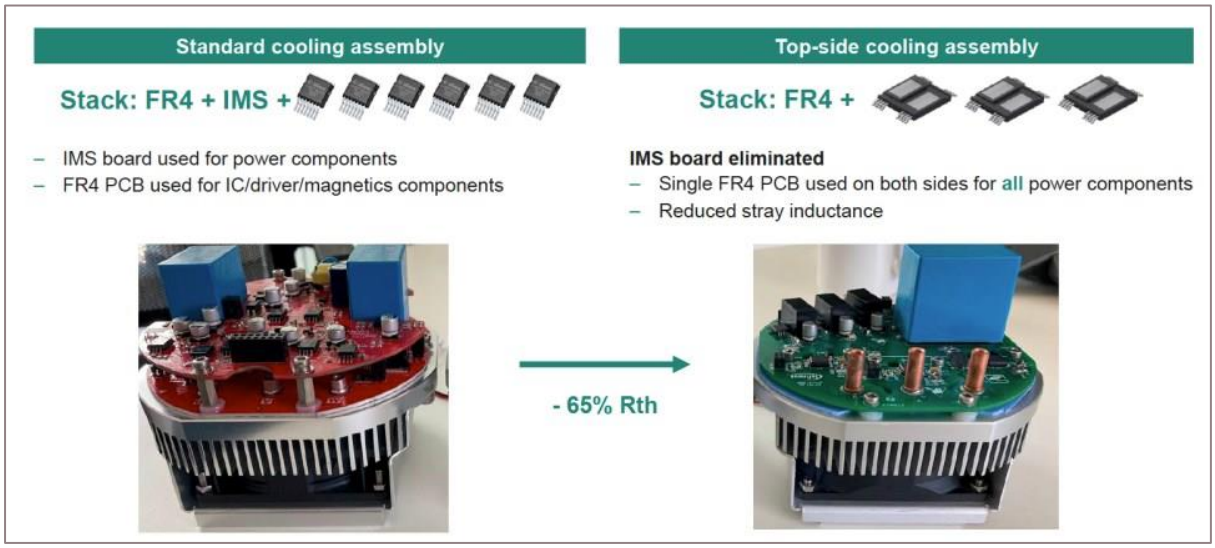


Figure 3: Advantages of the top side cooled package (Source: Infineon Technologies)

New CoolSiC™ 400 V G2 MOSFETs

Server power supplies increasingly need higher levels of power. Advanced GPUs for Artificial Intelligence (AI) training are forecasted to require as high as 3 kW per processor by the end of the decade. With multiple GPUs

per AI server rack, the power supply unit (PSU) power rating is consequently moving towards 8 kW and beyond.

The newly introduced CoolSiC™ MOSFET 400 V G2 is ideally suited to fulfill the future efficiency and power density requirements when used in multi-level Active Front End (AFE) topologies such as flying-capacitor totem-pole PFC.

Improved conduction and switching losses compared to their 650 V counterparts bring efficiency improvements of up to 0.3 %. A flatter RDS(on) vs Tvj curve, with an increase from 25 °C to 100 °C of only 11%, helps improve system cost/efficiency optimization, which is especially important when considering the extreme AI Server load profiles. Meanwhile, the body diode is optimized with a low reverse recovery charge (Q_{fr}) that allows for robust commutation even under high di/dt conditions seen in SMPS applications, with switching waveforms showing negligible dependence on both operating temperature and load current. The devices are 100 % avalanche tested.

The initial roll-out includes both D^2PAK and TOLL packages with $R_{DS(on)}$'s ranging from 11 mΩ to 45 mΩ. The low source resistance of the TOLL package, along with the low Miller charge Q_{gd}, output charge Q_{oss}, and Q_{fr} together allow for fast switching capability with much reduced V_{DS} overshoot and ringing, plus reduced dead time. These translate on the system level to higher power density, lower losses, and good EMI performance.

The recommended topology for CoolSiC™ 400 V devices within the Gen I and Gen II AI Server PSU space includes 3-level PFCs, with 400V V_{DSS} perfectly fitting 277 VAC RMS for Gen 1 servers and 347 VAC RMS for Gen II servers, as shown in Figure 4.

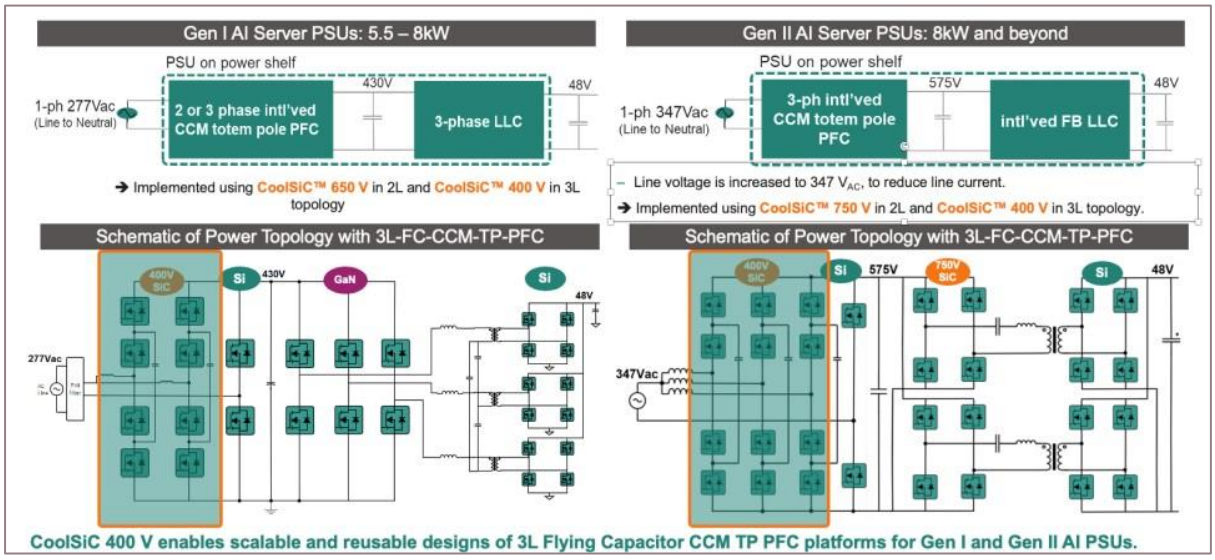


Figure 4: Basic schematics highlighting the flying capacitor 3-level totem pole PFC stage for AI server PSUs using CoolSiC ™ 400 V

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devices (Source: Infineon Technologies)

For the Gen I example shown in Figure 4, a comparison was made between a state-of-the-art 2-L totem pole PFC using 650 V SiC MOSFETs and a 3-L flying capacitor CCM totem-pole PFC using CoolSiC™ 400 V MOSFETs. The design consisted of two interleaved 2.8 kW high-frequency legs, with the devices switching at 80 kHz and the inductor at 160 kHz. As shown in Figure 5, the performance advantage of the 400 V devices helps achieve a flat efficiency curve, with efficiencies > 99.4% and a power density > 100W/in^3.

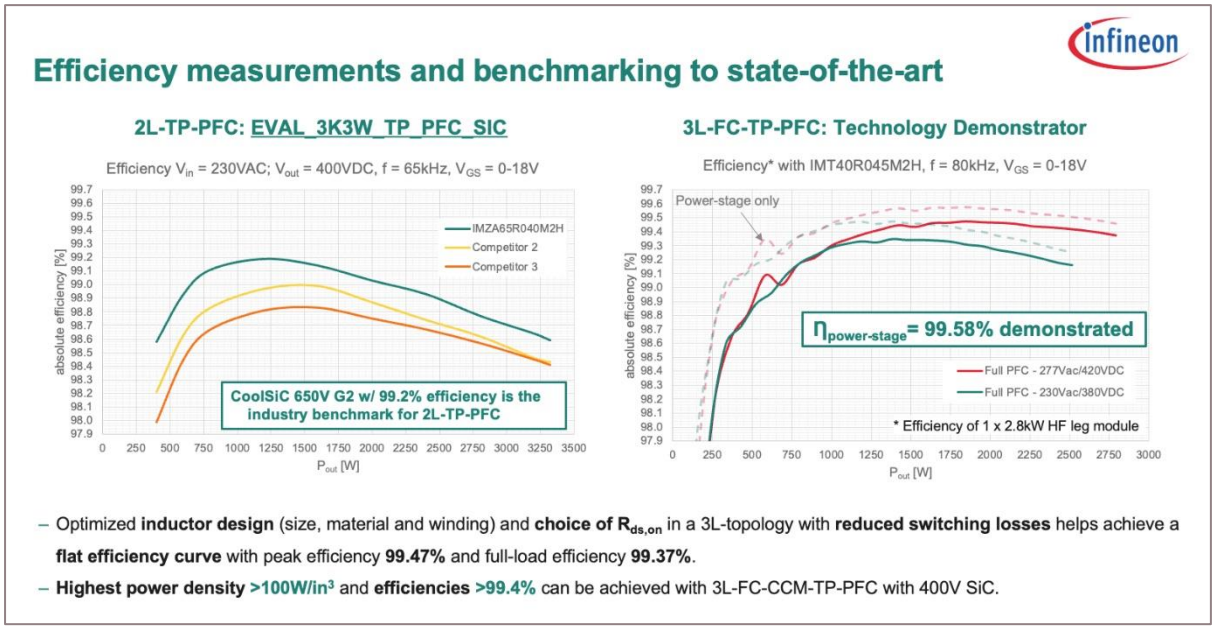


Figure 5: Efficiency comparison for the server PSU PFC stage (Source: Infineon Technologies)



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