PSoC® Creator™ Release Notes

Version 2.2 Service Pack 1
Revision Date: April 3, 2013

PSoC Creator 2.2 Service Pack 1 (SP1) is an update to the PSoC Creator 2.2 release of Cypress's PSoC 3, PSoC 5, and PSoC 5LP device configuration environment. PSoC Creator 2.2 added project datasheet generation, improved methods of importing/exporting components, and a number of improvements to existing features. SP1 primarily adds support for PSoC 4 devices. It also offers various defect fixes.

If you already have PSoC Creator 2.2, then your version will be updated with the SP1 features and fixes. If you do not already have version 2.2, then the complete PSoC Creator 2.2 SP1 release will be installed.

This production-quality release does not replace existing installations of PSoC Creator (e.g., 2.1 or 2.0); it installs alongside them. This enables you to move designs to the new version at your own pace. We guarantee that your existing designs can be opened in the new software. To ensure that you can always return to your previous setup, a backup of your project is automatically created when opening a project in a new version of the tool.

This document describes general software features and changes since the PSoC Creator 2.2 Service Pack 1 release.

If you have technical questions visit www.cypress.com/go/support or call 1-800-541-4736 and select 8.

Contents

SP1 Features/Fixes 2
PSoC 4 Support 2
Fixed Defects 2
Version 2.2 New Features 3
Project Datasheet Generation 3
Component Distribution (Import / Export) 4
Variable Vdda Parameter 4
New Binding Error Symbols 4
Peripheral Register Debug in IDEs 4
Datapath Configuration Tool 4
Components 5
New Components 5
Component Use Tracking 6
MISRA Support for Automotive Applications 6
UART Bootloader 7
Updated Components 7
Design Impact 7
Rename Annotation Components to External / Off-Chip 7
Include CMSIS Core Peripheral Library Parameter 7
New Pin Placer 7
Obsolete Components 7

Supported Devices 8
Supported Tool Chains 9
Toolchains for PSoC 3 (8051) 9
Toolchains for PSoC 4, PSoC 5 and PSoC 5LP (ARM) 9
Installation 10
Minimum and Recommended System Requirements 10
Software Update Instructions 12
Open Source 12
Installation Notes 12
Further Reading 13
Defects Fixed 14
Bootloading 14
Build System 14
Debugging/Programming 14
Framework 15
System 15

SP1 Features/Fixes

PSoC 4 Support

This service pack adds support for the newly-released PSoC 4 device families, which you will see in the New Project dialog and Device Selector.

Several components were updated solely to include support for PSoC 4. As a result, be sure to use the latest component versions in PSoC 4 designs.

Fixed Defects

Cypress ID	Defect	Fix and Impact
105007	Tool rejects PLL frequencies below 67MHz. Configuring the PLL to frequencies near 67MHz (the device peak frequency) causes a DRC error, even though the frequency plus tolerance is below the peak.	The DRC has been fixed. It was applying an extra 10ppm buffer to the calculation (a legacy of when there was no tolerance field in the GUI). Legal frequencies near the peak are now allowed.
143041	Using the Segment LCD low power mode can cause the chip to hang when going to sleep. A reset (XRES) was required to exit the hung state.	The low power mode ACK (lpack) from the LCD is driven correctly. However, when the device is trying to enter sleep mode the LCD's lpack stays de-asserted because the LCD is still working, and is unable to finish before the LCD clock is turned off by the power management system. Therefore the part hangs. The sleep mode logic prevents this scenario from occurring if DCLK[0] (digital clock) is used as the LCD clock. PSoC Creator now forces the segment LCD to use DCLK[0].

Cypress ID	Defect	Fix and Impact
143686	Projects that use either Vdda or Vdda/2 as the reference voltage to the SAR ADC will fail to route.	This was a regression from PSoC Creator 2.1. That release had a defect where the SAR would always consume a Vdda/2 reference voltage source even this was not needed. The fix in the 2.2 software introduced a new defect where the SAR would cause a project to fail to route if it really did use Vdda/2 (or Vdda) as the reference voltage. Both issues are now resolved.
143896	The Auto-Start checkbox in the clocks DWR editor has no impact (clocks are not started).	This was a regression from PSoC Creator 2.1 and has been fixed.
144418	Re-targeting PSoC 5 Bootloadable projects to PSoC 5LP causes unhandled exceptions when the project is opened and/or built.	During the migration from PSoC 5 to PSoC LP5, PSoC Creator tries to decide on the DMA configuration option based on whether the bootloader is associated with multiple bootloadables or not. However, the bootloader info is not available yet (when the project is opened or built) and a null exception is thrown. The tool can now correctly migrate the DMA setting from a PSoC 5 project to PSoC 5LP.
144921	The startup code for the PLL clock in cyfitter_cfg.c for PSoC 5 designs assumed incorrect functionality of the locked bit in the PLL status register. As a result it was possible for the code to proceed before the PLL was reliably stable. Note that stability would always be achieved soon after exiting the loop because there is a hard maximum settling time of 250us.	The startup code for PSoC 5 (not PSoC 5LP - it is not required) now enforces a 250 microsecond delay to enable the PLL to settle before proceeding.
145715	Some complex analog designs built with PSoC Creator 2.1 SP1 fail to build in the 2.2 software, giving the impression that the analog place & route algorithm deteriorated between releases.	Changes were made to the properties of switches in the delta-sigma modulator (DSM) to ensure good signal quality to the ADC. These changes exposed issues in the heuristic values used by the analog router, which have been updated to ensure that designs fit correctly and route faster.
146547	Erasing and Debugging fails in Keil Microvision with the message "Target DLL cancelled".	The MiniProg3 drivers were updated to support the erase function correctly (the same way they work for PSoC Creator connections). The MicroVision IDE can now erase and download correctly via MiniProg3.
148459	The PSoC 5LP datasheet for the 54xx family shows that DAC0 & DAC2 hardware blocks are available on the silicon but the Analog DWR editor in PSoC Creator 2.2 shows that DAC0 & DAC1.	PSoC Creator now displays and routes to the DACs that are actually available on the devices.

Version 2.2 New Features

Project Datasheet Generation

With this release, you can generate a datasheet for any PSoC Creator design, making it easier to share your ideas with colleagues. Just build your project as usual and then select the Build > Generate Project Datasheet option. A PDF document containing the system settings, clock and pin details, plus information

on all the components used in the schematic, is generated presented in the Workspace Explorer, under the "Datasheets" tab.

Note This release includes the initial phase of the feature. It supports the system-wide information but does not include all component configuration or API information.

Component Distribution (Import / Export)

This feature supports content developers who wish to share components without creating a new component library. By adding a library-free distribution method for components, you can more easily control your own libraries and dependencies. This feature is a pre-cursor to full support of a Component Store in a future PSoC Creator release. To use the feature, switch the Workspace Explorer to the Component tab and right-click on a project to import or on a component to export. Exported components are archived in a file with the extension “cycomp”.

Variable Vdda Parameter

This parameter complements the Vdda setting from the System tab of the Design-Wide Resource editor. It is used to control the generation of the analog resource boost clock (implemented in the PSoC Creator 2.1 release). It identifies projects that **may** need to run correctly at low Vdda settings, even if that is not the norm (i.e., Vdda is set greater than 2.7 V).

Previously, when the Vdda setting was high (above 2.7 V) the boost clock was not enabled in the system, leaving the clock block resource free for other uses. However, some designs, particularly battery-powered ones, may experience an occasional Vdda drop resulting in a degradation of analog performance. This parameter allows you to build the design for best performance (high Vdda), but retain the ability to switch on the boost clock should you detect a drop in voltage.

When this parameter is set, PSoC Creator creates the CyScBoostClk clock regardless of the Vdda setting. If Vdda is low, this parameter has no effect.

New Binding Error Symbols

Occasionally, schematics contain components that cannot be displayed. This is typically because a library location has moved, a dependency is incorrect, or the specific component version is not available in the version of the tool being used. In prior releases this situation was communicated by the component symbol being replaced by a scary box with a cross inside! These boxes have been replaced with new symbols and much more helpful text to guide you to a resolution.

Peripheral Register Debug in IDEs

In addition to the “normal” information contained in project files, PSoC Creator exports register information in CMSIS-SVD format, which is understood by the target IDE(s). This information is used by the IDE debuggers to display status for configured peripherals in the PSoC device and to allow user modification of those registers where appropriate.

Datapath Configuration Tool

The Datapath Configuration tool can now be launched from PSoC Creator Tools menu.

Components

This section contains information about new and updated components in this release. Refer to the applicable component datasheets (available in the PSoC Creator distribution and on the web) for additional information.

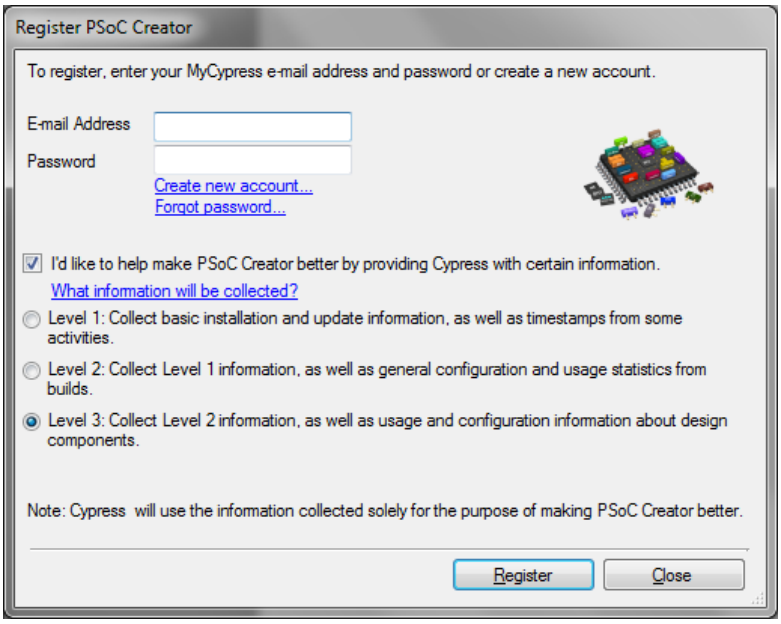
New Components

The following new components have been added as part of this release:

- **TMP05 Interface –** The TMP05 Interface adds another option for temperature calculation. It is used to easily interface with up to four TMP05/TMP06 digital temperature sensors.
- **Digital Constant –** The Digital Constant provides a convenient way of representing digital values in schematics.
- **D Flip Flop w/ Enable –** The D Flip Flop w/ Enable is like the DFF, but with an easy way to safely gate the clock.
- **SR Flip Flop –** The SR Flip Flop allows digital logic in schematics to use the Set/Reset paradigm, often capturing the intent of the design more clearly.
- **Toggle Flip Flop –** The Toggle Flip Flop is a flip-flop that changes its state when the input is high.
- **Digital Comparator –** The Digital Comparator is used to compare the values of two digital busses on a schematic, providing a single digital output for the result of the selected comparison.
- **Edge Detector –** The Edge Detector samples a signal for an edge (Rising Edge, Falling Edge, or Either Edge) and produces a pulse when the selected edge is detected.
- **Basic Counter –** The Basic Counter is a selectable width counter that provides the count value as a bus output for use in the schematic.
- **Pulse Converter –** The Pulse Converter samples a signal for any pulse, and produces an output pulse of guaranteed width.
- **Frequency Divider –** The Frequency Divider is used to divide a signal by a chosen divider, with the ability to also specify the duty cycle of the resulting signal.

Component Use Tracking

A third level of information was added to our registered user data collection system. While it does not record your design (resources, schematics, source code, etc.) it does track the components you use (library, name and version). We encourage you to check “Level 3” in the product registration dialog (available from the Help menu), shown below, so we can gather statistical data on the components that are most well-used.



We use this information to understand our customers better, improve our component roadmaps, and to focus our maintenance efforts on the most important components.

MISRA Support for Automotive Applications

As part of a project to support MISRA-compliant applications, PSoC Creator project code and the APIs for many components are being updated to adhere to that standard. The compliant components are listed below (latest versions only). All of these components include a section in the datasheet discussing their compliance and any (allowed) exceptions. Check the release notes in future releases for more MISRA-compliant components.

- ADC_SAR
- BoostConv
- CharLCD
- Counter
- CRC
- cy_boot
- cy_clock
- cy_dma
- cy_isr
- cy_pins
- CyControlReg
- CyStatusReg
- DFB
- DieTemp
- EEPROM
- EMIF
- I2C
- I2S
- IDAC8
- OpAmp
- PGA_Inv
- PGA
- PWM
- QuadDec
- Sample_Hold
- SegLCD
- SleepTimer
- SPDIF_Tx
- Timer
- UART
- VDAC8
- VectorCAN

UART Bootloader

The UART component now supports bootloading APIs. In addition, the bootloader host tool has been extended to support UART-based bootloading from your PC.

Updated Components

As mentioned previously, many components were updated for MISRA requirements. No other significant changes were made to any other components.

Design Impact

Rename Annotation Components to External / Off-Chip

The Component Catalog "Annotation" tab has been renamed to "Off-Chip." Also, most references to "Annotation" components and terminals have been renamed to "External."

These components do not implement actual functionality but do document the design on the context of the target board. The name "Annotation" did not convey that the intent is to document off-chip connectivity.

Note The actual CyAnnotationLibrary file name was not changed so that existing projects will not be impacted.

Include CMSIS Core Peripheral Library Parameter

This is a new parameter in the System tab of the Design-Wide Resource editor. The CMSIS (Cortex Microcontroller Software Interface Standard) Core Peripheral Library contains APIs to access ARM CPU core registers and peripherals. Checking this option will include the APIs from v1.30 of the standard in the project. Un-checking the box will omit the files from the project. If you wish to use a version of CMSIS other than 1.30, uncheck the box and add the files manually.

New Pin Placer

As part of our ongoing effort to improve the tool, a new pin placer has been introduced. When making analog designs all unlocked pins are now allocated to more PSoC-friendly physical locations, making it easier to fit the whole design. This change enables more complex designs to fit without manual intervention. Note that locked pins are unaffected by the new pin placer.

Obsolete Components

A number of very old versions of components were re-classified as Obsolete for all devices in the 2.1 release. These components are not shipped with the 2.2 software. In all cases there are newer versions of the component that are of a higher quality. You should update your designs to use these new components.

Using the obsolete components in PSoC Creator 2.2 will cause a design-rule error to be output to the Notice Window. This message shall request that you update the component version or, in a few cases, take alternative actions to get onto supported implementations.

The impacted components are as follows.

ADC_DelSig	v1.0	EEPROM	v0.0	SegLCD	v1.50
ADC_DelSig	v1.10	EEPROM	v1.10	SegLCD	v1.60
ADC_DelSig	v1.20	EZI2C	v1.0	SGPIO_Initiator	v1.20
ADC_DelSig	v1.21	EZI2C	v1.10	SGPIO_Target	v1.30
AMux	v1.0	FanController	v1.20	ShiftReg	v1.10
AMux	v1.10	Filter	v1.10	SleepTimer	v1.0
AMuxSeq	v1.10	I2C	v1.0	SleepTimer	v1.50
BoostConv	v1.0	I2C	v1.10	SPI_Master	v1.0
CAN	v0.5	IDAC8	v1.0	SPI_Master	v1.10
CAN	v1.10	IDAC8	v1.10	SPI_Slave	v1.0
CAN	v1.20	Mixer	v1.0	SPI_Slave	v1.10
CapSense	v0.5	PGA	v1.0	StaticSegLCD	v1.10
CapSense	v1.10	PGA	v1.10	StaticSegLCD	v1.20
CapSense	v1.20	PGA_Inv	v1.0	TIA	v0.5
CapSense	v1.30	PrISM	v1.10	Timer	v1.0
CharLCD	v0.2	PRS	v0.5	Timer	v1.10
CharLCD	v1.10	PRS	v1.10	UART	v1.0
CharLCD	v1.20	PRS	v1.20	UART	v1.10
Comp	v1.0	PWM	v1.0	UART	v1.20
Counter	v1.0	QuadDec	v1.10	USBFS	v0.2
Counter	v1.10	RTC	v0.5	USBFS	v1.10
CRC	v1.10	RTC	v1.10	USBFS	v1.20
cy_boot	v1.0	SegLCD	v1.0	USBFS	v1.30
cy_boot	v1.10	SegLCD	v1.10	VDAC8	v1.0
cy_boot	v1.20	SegLCD	v1.20	VDAC8	v1.10
DieTemp	v1.0	SegLCD	v1.30	VoltageSequencer	v1.50

Supported Devices

The design flow and tools available in PSoC Creator 2.2 support the following PSoC 3 (CY8C3x), PSoC 4 (CY8C4x), PSoC 5 (CY8C5x) and PSoC 5LP (CY8C5x-LP) families of devices.

PSoC 3:	CY8C32*	CY8C34*	CY8C36*	CY8C38*
PSoC 4:	CY8C41*	CY8C42*		
PSoC 5:	CY8C53*	CY8C54*	CY8C55*	CY8C56*
PSoC 5LP:	CY8C52*LP	CY8C54*LP	CY8C56*LP	CY8C58*LP

Supported Tool Chains

Toolchains for PSoC 3 (8051)

DP8051 Keil™ 9.03

The Keil PK51 Professional Developers Kit for PSoC is installed with PSoC Creator. It supports optimization levels 0 through 5. If you would like to use the compiler optimization levels above level 5, you should purchase the standard PK51 product by contacting Keil.

- In North, Central, or South America... sales.us@keil.com
- In Europe, Asia, Africa, or Australia... sales.intl@keil.com

The free toolchain comes with a 30 day evaluation license. You can extend the license, without cost, by registering the product from within PSoC Creator (Help > Register > Keil…). Note that the extended license is for one year and that you will need to re-register it on expiry.

DP8051 Keil Generic

This option can be used to select a separately-installed version of the Keil toolchain. While any version can be selected, the only version officially supported versions are 8.16 and 9.03.

Toolchains for PSoC 4, PSoC 5 and PSoC 5LP (ARM)

ARM GCC 4.4.1

The CodeSourcery Sourcery G++ Lite for ARM is installed with PSoC Creator. It has no use restrictions and does not require license activation (it is distributed under the terms of the GNU Public License).

ARM GCC Generic

This option can be used to select a separately-installed version of the Sourcery G++ toolchain.

ARM RVDS Generic

This option can be used to select a separately-installed version of the ARM RealView Development System. The officially supported versions are 4.0 (build 529) and 4.1 (build 791).

ARM MDK Generic

This option can be used to select a separately-installed version of the ARM Microcontroller Development Kit. The officially supported versions are 4.0 (build 524) and 4.1 (build 713).

Installation

Minimum and Recommended System Requirements

The following are system requirements to install and use PSoC Creator 2.2. Each requirement specifies a minimum that your system must meet or exceed.

PSoC Creator will execute correctly in highly resource-constrained systems. However, performance (startup time, project creation and opening, build times, and so on) may be impacted when resources are scarce. The most directly impacted performance metric is build time. The following sections provide examples of the resource scarcity impact.

Note During initial startup, PSoC Creator builds and caches component DLL files used to display the component parameter editors. As a result, the tool will launch slowly the first time after installation or a Windows® reboot. This is not indicative of a problem or a long-term performance degradation.

Summary

Hardware/Operation System Requirements	Minimum
▪ Processor	1 GHz or faster 32-bit (x86) or Intel 64/AMD64 64-bit
▪ RAM	512 MB (1 GB preferred)
▪ Free Hard Drive Space	2 GB
▪ Screen Resolution	1024x768
▪ USB	2.0

Software Prerequisites *	Minimum Version
▪ Microsoft Internet Explorer (not IE8 beta)	7
▪ .NET Framework	2.0 SP2
▪ Adobe Reader (for viewing PDF Documentation)	9.2 **
▪ Windows Installer	3.1
▪ PSoC Programmer	3.18
▪ Keil Compiler	8.16 (9.03 provided)

* To install and run PSoC Creator, you may also need to install additional software. The Cypress Installer will guide you through the process if the additional programs are not already installed.

** For Windows 7, the minimum required version of Adobe Reader is version 9.2. You can download the latest version here: http://get.adobe.com/reader/. You can also use a non-Adobe PDF reader if you prefer; however, Cypress has no recommendations for any particular non-Adobe reader or version.

Processor

1 GHz or faster 32-bit (x86) or Intel 64/AMD64 64-bit processor is required.

PSoC Creator exhibits a predictable relationship between CPU speed and build time above 1 GHz. Doubling the CPU speed, e.g., from 1 GHz to 2 GHz or 1.5 GHz to 3 GHz, almost halves the build time.

On a fast (3 GHz) PC, simple designs can build in about one minute. At low speeds even designs that fill the device and generate complex routing solutions will build in under 5 minutes.

Operating System

One of the following Windows platforms is required:

- Windows XP SP2 or SP3 (32-bit supported)
- Windows Vista (32- and 64-bit supported) and SP1
- Windows 7 (32- and 64-bit supported) and SP1
- Mac OS X with Parallels Desktop v6 or v7 running Windows XP 32-bit SP3
- Mac OS X with Parallels Desktop v6 or v7 running Windows 7 64-bit SP1

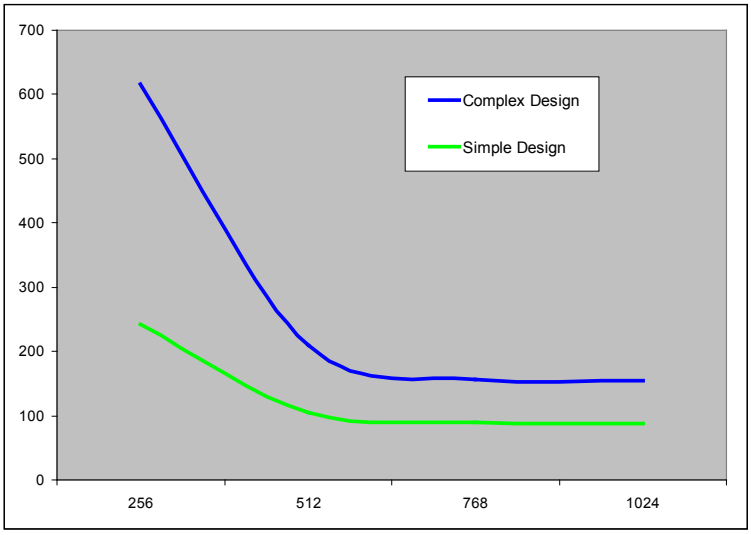
Memory

A minimum of 512 MB of RAM is required, but 1 GB is recommended.

Note Cypress does extensive performance testing on every PSoC Creator release. The minimum RAM configuration used in these tests is 1 GB. No guarantees of system performance are given below 1 GB.

With no other applications running, the minimum system configuration will ensure that the tool launches quickly, creates and opens projects in a few seconds, and responds to user input without feeling sluggish.

System RAM has the most direct impact on PSoC Creator build times. The following chart shows how insufficient RAM (i.e., below 512 MB) causes an excessive increase in build time, even for “empty” designs.



The graph shows that performance is heavily degraded below the threshold where memory paging is required but extra memory above that level does not generate a significant improvement.

Free Disk Space

PSoC Creator requires 2 GB of free disk space.

PSoC Creator will install and run with just 1 GB of free disk space. However, in order to allow Windows to do memory paging, we also require at least as much free disk space as you have RAM in your system, resulting in a minimum free disk space requirement of 2 GB.

If your disk is highly fragmented it will severely impact memory paging time and can result in very long build times. Disks that are nearly full are particularly prone to fragmentation. We recommend de-fragmenting your disk If you experience excessively long build times (10 minutes or more).

USB

PSoC Creator requires a USB 2.0-compliant host to program and debug.

Screen

A resolution of 1024x768 pixels or higher is required.

Note The build time examples given above were obtained with new product installations on minimally fragmented disks with no other applications running. If your build times exceed these expectations we recommend closing unnecessary applications, adding RAM to the system (to reduce paging) and ensuring that there is sufficient free and unfragmented disk space.

Software Update Instructions

As part of the installation process, the Cypress Update Manager utility will also be installed and located on the Start menu. You can use this utility to update all programs you have installed when updates for them become available.

Open Source

Portions of this software package are licensed under free and/or open source licenses such as the GNU General Public License. Such free and/or open source software is subject to the applicable license agreement and not the Cypress license agreement covering this software package. The applicable license terms will accompany each source code package. You may obtain the source code of such free and/or open source software at no charge from the following web site: www.cypress.com/go/opensource.

Installation Notes

The installation process is a set of wizards that walk you through installing various components. You can install PSoC Creator and various prerequisites from the web or from a CD. There are slight differences in the process, based on the medium used to install the software.

The CDs provide the necessary prerequisites and the wizards to guide you through installing the appropriate software. The following sections contain more specific installation details.

Note Do NOT plug in your Miniprog3 until all software installation is complete AND the PSoC Creator application has been opened.

PSoC Creator CD Installation

The PSoC Creator CD contains PSoC Creator and PSoC Programmer, as well as various prerequisites.

1. Load the CD. The main installer program should run automatically. If not, double-click the cyautorun.exe file to launch it.
2. On the main installer, click the **Install Software for PSoC…** button to launch the PSoC Creator InstallShield Wizard.
3. Follow the prompts on the wizard. The CyInstaller for PSoC Creator opens and displays steps to install PSoC Creator.
4. Click the hyperlink for any software that is not installed as indicated (such as, Acrobat Reader, etc.). Run the installer for that program as needed.
5. Continue following the prompts to install PSoC Creator.

Cypress PSoC Kit CD Installation

A kit CD contains PSoC Creator and PSoC Programmer, as well as projects, documentation, and prerequisites needed for the associated kit. Refer to kit instructions.

Web Installation

If you are downloading the software from the web (www.cypress.com/go/creator), run the PSoC Creator single package executable.

1. Double-click the PSoC Creator executable file to launch the installer.
2. If a non-Cypress prerequisite is missing (like .Net and Windows Installer, etc), a webpage with a download link will pop up. Download and install the prerequisites. Run the installer of those programs as needed.
3. Follow the prompts to install PSoC Creator. The CyInstaller for PSoC Creator opens and displays a series of steps to install PSoC Creator, and it will perform pre-requisite checks and install the prerequisites.
4. When complete, close the installer.

Further Reading

The primary documentation for PSoC Creator is provided in the Help, which you can open from the **Help** menu or by pressing [**F1**]. Other documents included with this release are also available from the **Help** menu, under **Documentation**. These documents include (but are not limited to):

- Quick Start Guide
- Known Problems and Solutions (KP&S)
- System Reference Guide
- Component Author Guide

The PSoC Creator KP&S document is a snapshot of the Knowledge Base issues available on online at the Cypress web site: http://www.cypress.com/go/creatoronlinekps.

Even more information is provided online at www.cypress.com/go/creator, including:

- PSoC 3, PSoC 4, PSoC 5, and PSoC 5LP Device Datasheets
- Device Architecture Technical Reference Manual (TRM)
- Device Registers TRM
- Migration Guides
- Application Notes
- Training

Contact your Cypress representative, as needed.

Defects Fixed

The following defects were fixed in this release. These defects are separated into different categories.

Bootloading

Cypress ID	Defect	Fix and Impact
131741	Bootloadable project slows down the PC in some designs.	The Bootloadable component was reading the bootloader hex file continuously, causing the PC to slow down in certain designs. This issue is now fixed.
134923	Bootloadable component not recognized when encapsulated in other components.	PSoC Creator searches for a bootloadable component only in the top-level schematic, causing the defect. The tool is fixed to recognize a bootloadable component in any level of hierarchy.
136099	Bootloader does not update bootloadable to the right address when using UDB-based I2C interface for bootloading.	Issue fixed in I2C v3.30 component.

Build System

Cypress ID	Defect	Fix and Impact
135819	Build errors seen for Interrupt APIs when an interrupt component in the design is connected to logic low.	The tool optimizes the interrupt component while the code generated for the interrupts remains, causing build errors. The interrupt routines are fixed to handle such optimizations.
133386	For a few designs retargeted from PSoC 5 to PSoC 5LP, incorrect resource usage is reported.	Build tools fixed to appropriately handle retargeting of any PSoC 5 design to PSoC 5LP device.
132709	PSoC Creator fails to build with "not routable" error for certain designs.	Build tool does not handle certain designs that contain net-tie components. Issue fixed to handle any net-tie component in designs.
132093	Designs with digital pins fixed at locations P15[6] and P15[7] fail to build.	P15[6] and P15[7] are USB assigned pins and hence were disallowed in the tool. The tool is fixed to allow designs to reuse P15[6] and P15[7] pins as appropriate.
118130	Designs with analog and digital pins do not build in some designs.	Router driven pin placement causes incorrect pin selections for analog pins, causing the design to not build. This issue is now fixed.

Debugging/Programming

Cypress ID	Defect	Fix and Impact
103154	The debugger does not stop at a breakpoint after wake up from sleep mode in certain designs.	The debugger was fixed to support debug in sleep mode.
132694	Keil uVision IDE stops working when Trace selection is made.	Trace is not a supported feature yet. The tool was fixed to disable Trace feature.

Cypress ID	Defect	Fix and Impact
132692	Keil uVision IDE stops working after configuration of FX2LP (USB) programming.	FX2LP programmers (USB-based) do not support any configuration. All FX2LP configuration options are disabled.

Framework

Cypress ID	Defect	Fix and Impact
137015	PSoC Creator crashes when referencing a custom component parameter in the "Advanced" configuration view of the PWM component.	Safeguard measures have been added to the tool to fix the issue.
118762	PSoC Creator crashes when closed within half a second after launch.	A race condition was observed when the tool was closed too soon after its launch. This issue is now fixed.
137618	A custom component using macros with busses does not work.	The tool used incorrect names for the wires of a bus, causing the macro to be broken. This is fixed.
132762	PSoC Creator fails when a terminal movement in the symbol designer is performed.	The symbol designer was incorrectly set to use rubber banding feature, causing the issue. The tool was fixed to ensure rubber banding feature is present only in the Schematic Editor.
131851	In some designs, lines get reversed in generated files when using "Find & Replace" functionality.	Find and Replace functionality is fixed for line reversals seen in files.

System

Cypress ID	Defect	Fix and Impact
140488	Cannot disable ILO on PSoC 5LP device when 32 kHz crystal is enabled.	ILO can be disabled now when 32 kHz crystal option is selected for PSoC 5LP designs.
140315	Automatic gain control (AGC) is disabled in code even when the "AGC Enabled" checkbox is selected for MHz ECO configuration.	The code generated for "AGC Enabled" selection in MHz ECO configuration correctly enables the appropriate register bits.
137789	A tool-generated hex file has bytes reversed incorrectly for write-once-latch initialization.	This is now fixed and the correct bytes are generated in the hex file for write-once-latch selection.
139419	The Analog Device Editor does not handle unnamed analog resources.	The Analog Device Editor handles only analog resources whose names are found in Top design. Hidden and generated analog resources were not handled correctly. This is now fixed.
133687	Inconsistency observed between the Analog Device Editor and the code generated in certain designs.	A minor issue found in the Analog Device Editor caused the tool to not reflect the generated code accurately. This is now fixed.

Cypress Semiconductor
198 Champion Ct.
San Jose, CA 95134-1709 USA
Tel: 408.943.2600
Fax: 408.943.4730
Application Support Hotline: 425.787.4814
www.cypress.com

© Cypress Semiconductor Corporation, 2013. All rights reserved.

The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

PSoC® and CapSense® are registered trademarks, and Programmable System-on-Chip™, PSoC Creator™, and SmartSense™ are trademarks of Cypress Semiconductor Corporation. All other trademarks or registered trademarks referenced herein are property of the respective corporations.

This Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.