PSoC Creator Release Notes

Version 1.0 Production

Revision Date: December 31, 2010

PSoC® Creator™ 1.0 is a complete Integrated Development Environment (IDE) for designing with PSoC 3 and PSoC 5 device families. This production-quality release is a complete software package for new users and an update (replacement) for all previous beta installations. This document describes general software features and changes since the previous release.

All current beta software users are strongly encouraged to update to this release, which contains fully characterized, production-quality components. To help you migrate from previous releases, a Migration Guide is available on the Cypress web site at:

http://www.cypress.com/?rID=39551

If you have technical questions visit www.cypress.com/go/support or call 1-800-541-4736 and select 8.

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New Features

Production-Ready Content

The latest revisions of all components in this release are of production quality and fully characterized. This means you can be confident that they will operate correctly and the datasheets contain all the data you need to complete reliable, full-featured designs. Cypress strongly recommends that you update your existing projects to the production-ready components with the Component Update Tool (**Project > Update Components**).

Component Improvements

In addition to being production-ready, several components have been updated in this release.

- The new **Mixer**, **PGA**, **Inverting PGA** and **TIA** components (all v1.60) no longer require you to set the low Vdda parameter when the voltage is below 2.7 V. If you are running the device at low voltage you just need to set Vdda in the Design-Wide Resources (DWR), System Editor; the components make sure the hardware is set up correctly.
- The new **Mixer** component (v1.60) has also dropped the need to specify a slow local oscillator. The component now detects this automatically and handles the hardware setup in firmware.

  You can also use an internal clock as local oscillator to save time setting up the reference frequency. External local oscillators (that is, schematic-based clocks) are still supported and there is an option to force a 50% duty cycle for distortion-free (UP) mixing.
- The latest **I2C** component (v2.10) adds multi-master support. It can be selected in the component customizer, from the Mode pull-down.
- The **USBFS** component (v1.60) contains several fixes for audio class handling.
- The **Opamp**, **Comparator**, **IDAC8**, and **VDAC8** components (v1.60) all have a new, easier-to-use parameter editor interface.
- The **ADC DelSig** (v2.10) and **CapSense® CSD** (v2.10) components have been updated to fix some defects in prior versions (see the individual component datasheet change logs for details).

  Note SmartSense™ has been disabled in the v2.0 CapSense CSD component, so you must update to the new version to continue using SmartSense functionality.
- The **Timer**, **Counter**, **PWM**, **PRS**, and **PrISM** components are all updated to v2.0 to add input synchronization in the fixed-function implementations, as well as output synchronization to prevent glitches. Earlier versions of these components now issue a warning about potential glitched outputs due to bad synchronization.

Static Timing Analyzer

A static timing feature has been added to the tool. It is an automatic post-build check on digital routing in the device that warns of potential timing violations. This will help make reliable products that behave correctly across the device's temperature range and manufacturing lots. Static timing is only available for production PSoC 3 devices, not ES2 samples or today's PSoC 5 devices.

Digital Clocking Implementation

PSoC Creator has enhanced the implementation of clocking circuitry used for digital logic. These changes were made to provide consistent and reliable operation along with simplifying the reporting of static timing violations.

Two new components were added to better control clocking and synchronization. These components can be found in the Component Catalog, in the “System” folder.

- The Sync component provides a double synchronizer that enables local synchronization of asynchronous signals.
- The UDBClkEn (UDB Clock Enable) component provides a means to control the implementation of clocking circuitry.

Refer to the Clocking section of the System Reference Guide for a detailed description of the clocking implementation.

PSoC 3 Instruction Cache

The Design-Wide Resources editor now has an option to enable the Instruction Cache for production PSoC 3 devices. Enabling the cache will improve the performance of PSoC 3 application code. The APIs to manage the cache are the same as those currently supporting PSoC 5 designs and are documented in the System Reference Guide. Note that this option is only available to production PSoC 3 devices, not the ES2 engineering samples.

Generate Application Command

A menu item called "Generate Application" has been added to the Build menu and toolbar. It starts the usual project build process but terminates after the API generation phase completes. This is a great new way to check your design is still good and to see the generated source files, without having to wait for a complete build.

Automated Problem Reporting

It is now possible to access technical support directly from the tool. A new Help menu gives you access to the online Knowledge Base (Help > Support > Knowledge Base…) where you can search for solutions to your problem and you can also create a Tech Support case (Help > Support > Create a Support Case…).

Notice Window Update

To make error handling simpler, two new buttons have been added to the Notice window; "Go To…" and "Details…". The first performs the same function as double-clicking on the message, namely to navigate to the source of the problem. The second launches the error dialog, which now shows more detail about the error. The buttons are only active when a message is selected in the Notice window.

Design Impact

More Warnings and Errors for Silicon and Component Incompatibility

Through various beta releases of PSoC Creator, there have component version updates. These updates have included adding new functionality, fixing defects, and adding more design-rule checks (DRCs). There are now a small set of defects on the "beta" components (fixed in the current versions) that are important you know about, specifically in the area of functionality that differs by silicon revision (PSoC 3 ES2 and ES3, for example).

Cypress has added new warnings and error messages to old component’s DRCs, without touching implementation code. Now you will be notified if you are using an unreliable component/silicon combination or accessing functionality that is not supported. The solution to such errors is generally to update your project to the latest components. Exceptions are described explicitly in the error messages.

Updating to Production-Ready Components

As mentioned previously, the latest versions of components are now production-ready. Cypress strongly recommends that you update your projects to use these new components. In most cases, all you need to do is to run the Component Update Tool to migrate to the new versions. Cypress recommends updating all components in one step.

There are, however, some known component update problems, as follows:

- The SegLCD is the only production component that does not support all silicon revisions. PSoC 3 ES2 and PSoC 5 ES1 are supported by v1.xx versions only. Production PSoC 3 silicon (that is, ES3) is supported by v2.xx versions only. If you need to update the SegLCD, make sure you do not jump to an unsupported major version. The most likely scenario is that you will update to a v2.xx component on a PSoC 3 ES2-targeted project. In that case, update only to v1.50 of the SegLCD.
- There was a parameter change in the ADC_DelSig between v1.xx to v2.xx, which causes validation errors when updating between the major versions. Depending on your previous ADC setup, you may see one of the following messages:

  "Evaluating parameter 'ADC_Input_Range' : Undefined identifier 'Vss_to_2Vref'"

  "Internal Vdda/3 Reference option is available only with PSoC3 ES3 / PSoC5 ES2 or later"

  Also, since the older components used the input range to determine whether the ADC was differential or single-ended, the validation problems on that parameter may lead to it being presented as differential when it was previously single-ended. This only happens if the input range was previously illegal but the old components did not detect the error.

  The resolution in these cases is to verify that the settings in the Configure dialog are as desired and save the new configuration. It may be necessary to toggle the Input Mode between Differential and Single-Ended radio buttons to clear the error before saving.
- The latest VDAC8 checks that the voltage range does not exceed the project's Vdda. Note that this is not an error condition but a Note is issued to inform you that the component will not be able to reach its peak output. For example, if Vdda is set to 3.3 V in the DWR System Editor and the DAC range is set to 0-4.080 V, the higher voltages will not be attainable.
- The Mixer v1.60 now checks the local oscillator frequency and forces you to keep it below 1 MHz. Updating old Mixer components may require you to change the LO frequency in the Configure dialog.
- The cy_isr component is easy to update, but the v1.10 revision is not compatible with new silicon. This component is frequently buried inside other components, like CapSense_CSD, UART, and USBFS. Do not be mistaken by the messages from Interrupts you did not put in your top design. Fixing the top-level components will address the errors about cy_isr too.
- The Counter v2.00 now requires a clock input, as opposed to just an asynchronous count. So updated components will contain an error that the count input requires a connection. Make sure you attach the appropriate signal on the count input and also have a clock that is twice as fast as the maximum expected rate of count events on the clock input.

Static Timing Messages

The static timing analyzer, which is enabled for PSoC 3 Production silicon only, will detect timing violations in your designs. Detailed timing violation warning messages will be generated when the design is built if the design is not able to reliably run at the given clock frequencies. Refer to the static timing analysis section of the report file (*.rpt) for the complete timing analysis for the design. This report includes a summary of the maximum clock frequency for each clock in the design.

Clocking Messages

With designs where all the clocks and signals in the system are not synchronous to the bus clock, you may see warnings that the design cannot be implemented safely. The Sync and UDBClkEn components are provided in the Component Catalog “System” folder to help you correct unsafe asynchronous designs.

A specific error you may encounter complains about the use of signals as clocks that are asynchronous to the bus clock:

> "Routing of asynchronous signal <Pin Resource> as a clock to UDB component <Name> is not supported unless a UDB Clock/Enable component is used."

Generally, PSoC devices are designed to operate in a synchronous environment. Refer to the Clocking section of the System Reference Guide for guidance.

Note for Kit Users

Some of the projects in our evaluation kits have been impacted by changes in the tool and content, exposing hidden design errors in the examples. Cypress is working to fix these issues and provide updates to the kit software on the web. In the meantime, Cypress is building archives of corrected kit projects and posting them on the web site for each kit. If you find that your kit projects no longer build after updating to this release, visit the download page for your kit in order to download a simple, archived copy of working examples. In due course you will receive a notification to update your kit formally with the new examples.

To help you migrate from previous releases, refer to the Migration Guide available on the web site at:

http://www.cypress.com/?rID=39551

Supported Devices

This release supports ES2 (engineering samples 2) and production PSoC 3 silicon. It also supports ES1 PSoC 5 silicon.

The design flow and tools available in PSoC Creator 1.0 support the following PSoC 3:CY8C3x and PSoC 5:CY8C5x families of devices:

PSoC 3	PSoC 5
• CY8C32*	• CY8C52*
• CY8C34*	• CY8C53*
• CY8C36*	• CY8C54*
• CY8C38*	• CY8C55*

Supported Tool Chains

Toolchains for PSoC 3 (8051)

1. **DP8051 Keil™ 8.16**

   This toolchain is installed with PSoC Creator. It supports optimization levels 0 through 5. If you would like to use the compiler optimization levels above level 5, you should purchase the PK51 compiler by contacting Keil.

   - In North, Central, or South America... sales.us@keil.com
   - In Europe, Asia, Africa, or Australia... sales.intl@keil.com

   The free toolchain comes with a 30 day evaluation license. You can extend the license, without cost, by registering the product from within PSoC Creator (**Help > Register > Keil…**). Note that the extended license is for one year and that you will need to re-register it upon expiration.

   This is the only officially supported version:

   - Keil PK51 Prof. Developers Kit for PSoC: Version 8.16

2. **DP8051 Keil Generic**

   This option can be used to select a separately-installed version of the Keil toolchain. While any version can be selected, the only version officially supported is Version 8.16.

Toolchains for PSoC 5 (ARM)

1. **ARM GCC 4.4.1**

   The following GNU toolchain is provided with PSoC Creator; it is the only officially supported version:

   - CodeSourcery Sourcery G++ Lite for ARM: Version 4.4.1 2010q1-188 (http://www.codesourcery.com)

2. **ARM GCC Generic**

   This option can be used to select a separately-installed version of the GNU toolchain.

   While no longer officially supported, the GNU toolchain provided with Beta1 through Beta4.1 can be downloaded and used as the generic toolchain (contact Cypress technical support for details). The older version is

   - CodeSourcery Sourcery G++ Lite for ARM: Version 4.2.1 2007q3-53

3. **ARM RVDS Generic**

   This option can be used to select a separately-installed version of the ARM RealView Development System. While any version can be selected, the only version officially supported is:

   - RealView Compilation Tools version 4.0, build 529, available in RVDS Version 4.0

4. **ARM MDK Generic**

   This option can be used to select a separately-installed version of the ARM Microcontroller Development Kit. While any version can be selected, the only version officially supported is:

   - MDK Compilation Tools version 4.0, build 524, available in MDK-ARM Version 3.70

Installation

Minimum and Recommended Requirements

Hardware/Operation System Requirements	Minimum	Recommended
• Processor Speed	2 GHz	2 GHz Dual Core
• RAM	2 GB	3 GB
• Free Hard Drive Space	1 GB	1 GB
• Screen Resolution	1024x768	1280x1024
• CD/DVD Drive	Not Req.	✓ *
• USB	Full Speed	2.0 Hi-Speed
• Windows® XP (SP2 or higher), Vista, or Windows 7 **	✓	✓

* CD/DVD drive is only required for installation with no web access.

** PSoC Creator 1.0 runs on Windows platforms only. Cypress does not test or support execution on virtualized platforms or emulated environments.

Software Prerequisites ***	Minimum Version
• Microsoft Internet Explorer (not IE8 beta)	7
• .NET Framework	2.0 SP1
• Adobe Reader (for viewing PDF Documentation)	6
• Windows Installer	3.1
• PSoC Programmer	3.12.3
• Keil Compiler	8.16

*** To install and run PSoC Creator, you may also need to install additional software. The Cypress Installer will guide you through the process if the additional programs are not already installed.

Software Update Instructions

As part of the installation process, the Cypress Update Manager utility will also be installed and located on the **Start** menu. You can use this utility to update all programs you have installed when updates for them become available.

Open Source

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Installation Notes

The installation process is a set of wizards that walk you through installing various components. You can install PSoC Creator and various prerequisites from the web, or from a CD. There are slight differences in the process, based on the medium used to install the software.

The CDs provide the necessary prerequisites and the wizards to guide you through installing the appropriate software. The following sections contain more specific installation details.

Note Do NOT plug in your Miniprog3 until all software installation is complete AND the PSoC Creator application has been opened.

PSoC Creator CD Installation

The PSoC Creator CD contains PSoC Creator and PSoC Programmer, as well as various prerequisites.

1. Load the CD. The main installer program should run automatically. If not, double-click the cyautorun.exe file to launch it.
2. On the main installer, click the **Install Software for PSoC…** button to launch the PSoC Creator InstallShield Wizard.
3. Follow the prompts on the wizard. The CyInstaller for PSoC Creator opens and displays steps to install PSoC Creator.
4. Click the hyperlink for any software that is not installed as indicated (such as, Acrobat Reader, etc.). Run the installer for that program as needed.
5. Continue following the prompts to install PSoC Creator.

Cypress PSoC Kit CD Installation

A kit CD contains PSoC Creator and PSoC Programmer, as well as projects, documentation, and prerequisites needed for the associated kit. Refer to kit instructions.

Web Installation

If you are downloading the software from the web (www.cypress.com/go/creator), run the PSoC Creator single package executable.

1. Double-click the PSoC Creator executable file to launch the installer.
2. If a non Cypress prerequisite is missing (like .Net and Windows Installer, etc), a webpage with a download link will pop up. Download and install the prerequisites. Run the installer of those programs as needed.
3. Follow the prompts to install PSoC Creator. The CyInstaller for PSoC Creator opens and displays a series of steps to install PSoC Creator, and it will perform pre-requisite checks and install the prerequisites.
4. When complete, close the installer.

Further Reading

The primary documentation for PSoC Creator is provided in the Help, which you can open from the **Help** menu or by pressing [**F1**]. Other documents included with this release are also available from the **Help** menu, under **Documentation**. These documents include (but are not limited to):

- Quick Start Guide
- Known Problems and Solutions (KP&S)
- System Reference Guide
- Component Author Guide

The PSoC Creator KP&S document is a snapshot of the Knowledge Base issues available on online at the Cypress web site: http://www.cypress.com/?id=4&rtID=383.

Even more information is provided online, including:

- PSoC 3, PSoC 5 Architecture Technical Reference Manual (TRM)
- PSoC 3 and PSoC 5 Registers TRM
- PSoC 3 and PSoC 5 Device Datasheets
- Application Notes
- Training

Contact your Cypress representative, as needed.

Defects Fixed

The following defects were fixed in this release. These defects are separated in different categories.

Framework

Cypress ID	Defect	Fix and Impact
75743	Builds of projects with very long paths fail on Windows 7 because the tool cannot write to its log file (get error about "Reached max tries of 1000 to open log file").	The log files were, by default, placed in a temp file in the project. Windows 7 detects that as being too long a path and replaces it with C:\Windows. Users without permission to write to that directory would see the exception because the tool could not open its log file. The log file is now stored in the user log directory which is unlikely to be so deep in the file system.
80700	GNU Linker cannot find a reference to an object in Generated Source.	Rearranged the order of objects and libraries in GNU-based projects to ensure that the linker can access the symbol(s).
82587	Start Page would not load on startup and could not be opened manually.	The plug-in for the Start Page was failing to load in some circumstances, causing sporadic non-appearance of their page for some users. This was caused by a now-fixed race condition between the Start Page and Kit plug-ins.
86087	Workspace in non-ASCII directory location fails to build.	Non-ASCII character file locations are not supported. The tool will no longer allow the creation or opening of a project if the path contains non-ASCII characters.
87509	Unable to print symbol, schematic or schematic macro files in 64-bit operating systems.	Implemented a Microsoft workaround for a .NET defect that enables printing on 64-bit systems.

Editors

Cypress ID	Defect	Fix and Impact
69324	The visual indication of selected items in a schematic is misleading. The dotted-line box around selected items does not show items that are enclosed but not selected.	The schematic editor now highlights all selected components with a shaded background so it is easy to see unselected items.
84186	Cache not enabled on production PSoC 3 silicon.	Modified the boot code to set both the CACHE_CR.SRAM_EN and CACHE_CR.CACHE_EN bits, enabling correct cache functionality.
84677	Tool warns the user that the design consumes the Opamp external reference pin even if it is used for the Opamp.	Informing users that a design uses a pin that is tightly associated with a specific resource is good - unless it is that actual resource that is consuming the pin. The tool no longer warns about a pin's usage if it is being used for one of its special purposes.

Debug / Program

Cypress ID	Defect	Fix and Impact
83267	Watch variables get forgotten every time the debugger is stopped.	Watch variables are now saved after a debugging session so users no longer need to add them back in at the start of the next session.

Build System

Cypress ID	Defect	Fix and Impact
75404	PSoC Creator projects must be in directories named with ASCII characters. Opening a project in an illegal directory outside of a workspace fails to generate an error,	The tool should not let you create or open a project if the path contains non-ASCII characters. This is already the case when opening a workspace, but there was a corner case where you could open a project that didn't have a containing workspace. This was fixed so that project opens will fail as well and generate a suitably helpful error message.
75621	The external 32 KHz crystal input is not correctly synchronized, giving runt pulses and missed transitions.	The external 32 KHz crystal was routed to UDB components incorrectly. This has been resolved by correcting how asynchronous clocks enter into the UDB array.
78760	Bootloader doesn't allow ECC to be enabled.	There were issues with how the bootloader and a bootloadable projects interacted with regard to ECC memory and ECC code. It is not legal for the bootloader to be stored in ECC memory. The bootloader may enable/disable the use of ECC code. However if ECC code is enabled in the bootloader it must also be enabled in the bootloadable project. Also if ECC code is enabled in the bootloader the bootloadable may not store its configuration in ECC memory and it must enable ECC code. The tool checks that ECC code matches in both projects.

Cypress ID	Defect	Fix and Impact
80652	During the rebuilding of projects in a workspace, breakpoints and watchpoints are lost in both the active and inactive projects.	All breakpoint data is now saved before a build. The user is no longer required to re-set their breakpoints and watchpoints.
82847	A design using more macrocells than the device can support does not generate an error about resources. Instead it reports that routing cannot be found.	Rather than wasting time in the fitter, the tool now detects and reports when macrocell requirements are exceeded.
83904	The mapper aborts the build of a design based on total product terms, failing to fit a design that "should" fit.	The mapper now checks unique, not total, pterms. The report file now shows no limit on total available pterms. Designs that have many non-unique pterms do not fail to fit now.
84297	Registered subtraction in Verilog generates the wrong configuration.	Corrected the detection of the clock property for carry chains so that registered subtraction now builds correctly.
84591	Bootloader fails to locate downloaded configuration data when it is stored in ECC memory (i.e., when normal ECC usage is disabled).	The bootloader looks for configuration data at the start of ECC memory but it is actually located in the ECC memory next the ACD flash image. The *cyfitter_cfg.c* constants were updated to reflect where the configuration information actually resides.
84592	Bootloading fails when ECC is enabled in the design.	If ECC is enabled, then the ECC memory should not be programmed by the bootloader. The defect is that the bootloadable image file (.cyacd file) is generated with the full row including both the normal flash and the ECC memory. When the bootloader host takes a row of information from this file and sends it to the bootloader the bootloader complains that the line is of the wrong length and it fails. The fix ensures that the .cyacd file does not include the unnecessary/offending ECC memory information.
87327	When Bus Clock is > 33 MHz and the IO synchronization is moved to inside the UDB array, the rules used for determining the sync clock are too confusing and do not provide a good experience.	All I/O synchronization has been changed to only use BUS CLOCK as the clock driving the synchronizer.
87415	The Bootloader Status/Error Codes in the System reference Guide do not match the #define values in *cybtldr.c*.	The source file data is correct and so the System Reference Guide for the v2.20 cy_boot component has been updated.

Installer

Cypress ID	Defect	Fix and Impact
85298	Opening a project that was last built on a previous release (e.g. 1.0 Beta 4) of PSoC Creator gives an error message stating that "Requested value 'PRODUCTION' was not found"	The 1.0 Beta 5 release added support for the Production/ES3 Si revision of PSoC 3. When opening older projects the tool would detect the default silicon revision, which changed from ES2 to PRODUCTION, and generated a misleading error about the mismatch. The project handling now detects mismatched silicon support and prompts the user to select the appropriate revision.

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