Release Notes SRN070

PSoC Designer Version™ 5.0 Service Pack 4

Release Date: April 3, 2009

Thank you for your interest in PSoC Designer™ version 5.0, Service Pack 4 (SP4). These release notes list installation requirements and describe software updates and changes. Major sections of this document include:

- System Requirements and Recommendations
- New for PSoC Designer 5.0 Service Pack 4
- Installation Notes
- New Product Support
- Known Problems/Limitations

System Requirements and Recommendations

System Requirements	Minimum	Recommended
Processor Speed	1 GHz	2 GHz Dual Core
MB of RAM	1 GB	2+ GB
MB of Free Hard Drive Space	600 MB	1 GB
Screen Resolution	1024x768	1280x1024
CD-ROM Drive	✓	✓
USB Port, preferably USB 2.0	✓	✓
Windows® XP (SP2 or 3), or Vista	✓	✓
Microsoft Internet Explorer (See note in the installation section)	6.0 (SP1)	7.0
.NET Framework	2.0	2.0 (SP1 or higher)
Adobe Reader (For Viewing of .PDF Documentation)	6	9
PSoC Programmer	3.05	3.05 or later

Updates

Check http://www.cypress.com/psocdesigner for the latest downloads of software and documentation.

New for PSoC Designer 5.0 Service Pack 4

Included in Service Pack 4 are many bug fixes, new features and support for many new products. With regards to bug fixes, specific emphasis has been placed on improving support for the ICE-Cube and the debugger.

Both PSoC Designer and PSoC Programmer no longer include the Microsoft .NET installation package. If required, a link to this package is provided in the install. This significantly reduces the download sizes. Though not available with the first release of service pack 4, we will soon have a patch level installer. Please check http://www.cypress.com/psocdesigner.

New products and new user modules are discussed in following sections. Please note that in many cases, new product support may be in the beta release phase. It will be explicitly stated in cases where support is at the beta level.

Installation Notes

If an ICE-Cube or MiniProg3 is connected to the installation machine it must be disconnected and then reconnected after installing PSoC Designer 5.0 SP4.

Note: PSoC Designer 5.0 SP4 is not presently compatible with the internet browser, Microsoft Internet Explorer 8 beta (any beta version). If Microsoft Internet Explorer 8 beta is installed on your system, it must be uninstalled and an earlier version of Microsoft Internet Explorer installed in its place.

To Install:

Shut down any currently running instances of PSoC Designer.

If PSoC Designer 5.0 is currently installed, uninstall it. Click Start, click Control Panel, and then double click Add or Remove Programs. (We anticipate a patch-level installer to be available soon. If you have downloaded this installer, you may skip step 2).

1. Download and install PSoC Designer 5.0 SP4 by running the provided installer.
2. Download and install the latest PSoC Programmer 3.05 by running the provided installer.

Note: During the installation, if you have not already installed the HI-TECH compiler v9.61 PL6, a dialog will present you with the option of upgrading to the new version. The patch is necessary to support new devices and features in PSoC Designer 5.0 SP4.

To revert to an earlier version of the HI-TECH compiler after an update is installed, select the compiler version under **Tools → Options → Compiler** in PSoC Designer.

> If you choose to decline the compiler update, you must manually update the psoc.ini file to add device support before you can compile projects that use the new devices. The HI-TECH "psoc.ini" file is found in the HI-Tech installation folder. The default location of the psoc.ini is here:
>
> `C:\Program Files\HI-TECH Software\HCPSOC\PRO\9.61\dat\psoc.ini`
>
> The default location of the replacement "psoc.ini" file that adds support for the new devices is here:
>
> `C:\Program Files\Cypress\Common\CypressSemiBuildMgr\tools\psoc.ini`

New Product Support Included in PSoC Designer 5.0 Service Pack 4

Support for the CY8C22x45 CapSense Family

The CY8C22x45 family of CapSense devices has been added in Service Pack 4. These devices provide enhanced digital resources, increased flash and SRAM size, and enhanced capacitive sensing circuitry as compared to the CY8C21x34 and CY8C24x94 family.

New Part Numbers
CY8C22345-24SXI
CY8C21345-24SXI
CY8C22545-24AXI

Support for the CY8C28XXX Family

The CY8C28xxx PSoC family has been added in Service Pack 4. This family is targeted at the upper range of performance of the 8-bit microcontroller market. It is designed to provide numerous peripheral resources for use in the wide range and varied applications found in the general-purpose microcontroller market. Applications include consumer, industrial, appliance, communication and data processing where improved measurement performance and CapSense are required to implement the customer's system.

New Part Number	Pin/Package
CY8C28433-24PVXI	28-pin SSOP
CY8C28533-24AXI	44-pin TQFP
CY8C28445-24PVXI	28-pin SSOP
CY8C28545-24AXI	44-pin TQFP
CY8C28645-24LTXI	48-pin 7x7 QFN
CY8C28623-24LTXI	48-pin 7x7 QFN

There are also extended temperature parts for each of the parts listed above.

Powerline Communications

Cypress' Powerline Communication (PLC) solution implements robust low-bandwidth communication over power lines. Typical applications include:

- Lighting Control
  - Residential Lighting
  - Commercial/Building Lighting
  - Underwater Pool Lighting
  - Industrial Signage
- Automatic Metering Infrastructure
- Smart Energy Management

Service Pack 4 introduces beta support for this part family. In this release, only the Hi-Tech compiler is supported. ImageCraft support will be in the next release (Service Pack 5). The parts supported include the following:

Part Number	LED Channels	Package
CY8CPLC20-28PVXI	NA	(210 Mil) SSOP
CY8CPLC20-48LFXI	NA	(7X7) QFN
CY8CLED16P01-28PVXI	16	(210 Mil) SSOP
CY8CLED16P01-48LFXI	16	(7X7) QFN

There is a new User Module to go along with this part - the Powerline Transceiver (PLT)

The PLT User Module allows implementation of an FSK Modem, FSK Modem with Network Stack, or FSK Modem with Network Stack and I2C Bridge.

Known Problems Limitations for PSoC Designer 5.0 Service 4

General Problems

	Problem	Work Around
1.	The monitor mode for High Brightness LED drivers exhibits slow performance. Performance of the communication interface with the target hardware and updates of the driver GUI widgets can be slow when in monitor mode for a project that includes a High Brightness LED driver. It can take from 1 to 2 seconds for keystrokes entered in a text box to be reflected in the GUI. Values entered in the text entry box to be sent to the target hardware can take from 3 to 5 seconds to be transmitted to the target hardware and be read back and displayed in the High Brightness LED driver monitor widget.	No work around at this time.
2.	In the DelSig User Module data sheet, Figure 2 and Figure 3 showing the first and second order modulator were inadvertently swapped. [40586]	None at this time.
3.	The SAR10 User Module does not directly support the Auto-Triggered sampling mode.	Auto-Triggered sampling mode can be implemented by modifying the correct SAR10 registers with user code. Contact Cypress Applications for more information.
4.	After you select the Port and Pin for an LED user module, the table in the Pinout window does not immediately update to reflect the changes to the corresponding pin.	Build/Generate the project. The table in the Pinout window will automatically update when you Generate/Build the project.
5.	The I^2C user modules have operating frequency options of 50 kHz, 100 kHz, and 400 kHz. However, these options assume that SysClk is nominally 24 MHz. If SysClk is less than nominal 24 MHz (when using SLIMO mode, for example), these I2C operating frequencies will vary with the SysClk frequency.	When SysClk is lower than 24 MHz (nominal), choose a higher frequency option for the user module than is actually desired on the I2C bus.

	Problem	Work Around
6.	The sample code in BootLdrI2C uses the Counter24 and E2PROM User Modules (UM), but those UMs are not supported by all devices. [40531]	The purpose of the E2PROM UM in the example is to show how the E2PROM User Module can be used with the bootloader. If your device does not support the E2PROM UM that section of code can be omitted from the example. The purpose of the other code is to provide a simple working application that can be bootloaded. The application blinks an LED with a timer. Substitute the Timer16 UM for the Timer24 UM in the example.
7.	Blank Part Catalog Blank Interconnect View The Part Catalog or Interconnect view shows nothing.	This issue may be a result of your local IT policy. It can be fixed by adding "psocdesigner.exe" and "cmx.exe" to the 'Allow List' in the following registry key: HKEY_LOCAL_MACHINE\SOFTWARE\Microsoft\Internet Explorer\Main\FeatureControl\FEATURE_LOCALMACHINE_LOCK
8.	PSoC Designer may not recognize that a MiniProg3 device is connected.	This is most often seen on powerful machines with Vista. Workarounds include: - Shut-down PSoC Designer and re-launch it. - Go to Project menu > Settings > Debugger tab > Select ICE Device and Click **OK** - Use a Host PC with Windows XP
9.	In the Code Editor, if you choose a proportional font, especially if you have a mix of fixed-width and proportional fonts chosen for various code items, you may notice that the text moves as you select or enter text.	By definition, the width of letters varies in proportional fonts. Changes in spacing are unavoidable with proportional fonts. For best results, use only fixed-width fonts in the code editor. Fixed-width fonts are highlighted in bold in the Font list.

Problems with Chip-Level Projects

	Problem	Work Around
10.	When cloning a project you must be aware that some devices do not share user module capabilities. If you clone a project for one device to another device certain user modules may not appear.	Check what user modules are available for the cloned device.
11.	The I2CHW and EZI2Cs User Modules are unable to detect whether I^2C-bus pins are consumed by the CSD User Module. Therefore, it is possible to configure the I2CHW or EZI2Cs User Module to use pins already consumed by the CSD User Module.	Place and configure the applicable I2CHW, or EZI2Cs User Module prior to placing the CSD User Module. The CSD User Module wizard will detect that the I^2C pins have been consumed.

Problems with Compilation and Debug

	Problem	Work Around
12.	Multiple instances of PSoC Designer and PSoC Programmer can be open at the same time, but only a single instance is allowed to access the ICE at a given time. An error message stating "ICE Unavailable" will result when instances of either application attempt to access the ICE if it is already connected.	Press the disconnect button in the application that is currently connected to the ICE or close it completely to free it for connection in one of the other open instances.
13.	PSoC Designer 5.0 may not recognize a second ICE-Cube.	Go to Project → Setting → Debugger where the new ICE-Cube is listed and select it for use.
14.	If you move a project from one location to another and you try to compile an individual file, the compile will fail because the compiler's path to the file is absolute. If you move the project from one location and then rebuild the entire project, the absolute file paths are regenerated and compilation will succeed. The bug only affects individual file compilation.	There are build files generated that include explicit paths. These files are rebuilt when the overall project is re-built. You should rebuild the entire project after copying the project before performing individual file compilation.
15.	For projects that use the HiTech compiler, the values of pointer variables shown in the Watch Window sometimes differ from what is reported in the memory window.	The value of the pointer shown in the Watch Window is the true value of the pointer variable. Use the value displayed in the Watch Window for debugging purposes.

	Problem	Work Around
16.	For projects that utilize the HiTech compiler, you may not be able to set breakpoints on some source code lines. Explanation: The HiTech compiler optimizes-out (removes from compiler output) statements that it deems of no consequence to the execution of the program.	Set the breakpoint on a subsequent source code line. Or, try using the Lite mode of the compiler (Mode setting is found in Project | Settings | Compiler).
17.	Projects that use the HiTech compiler and include one assembly source file (*.asm) within another (using the 'include' statement) will confuse the Debugger.	Only use the assembly language 'include' instruction to embed assembly language include (*.inc) files.

Device-Specific Problems

	Problem	Work Around
18.	OvationONS™ II I/O registers banks 2 and 3 may not be displayed during debug.	It may be necessary to add test code to read the relevant registers into a location that is readable for debug. Fix planned.

19.	There is no SPIS SCLK pin setting on P1_0 with CY7C64315/CY7C64316 devices.
	
	P1_0 is the SPIS SCLK pin for the CY7C64315/CY7C64316. However, when SPIS is placed, P1_0 is not automatically configured to be the SCLK input pin. The pin needs to be manually configured as a digital input, and a bit in the IO_CFG register needs to be set to select P1_0 as the SPI CLK.
	
	The other SPI pins are set up properly in these devices.
		1. In the pin editor, select "StdCPUInput" for P1_0.
		
		2. Set bit 2 of IO_CFG before starting SPIS. For example:
		
		`IO_CFG |= 0x04;`
		`SPIS_1_Start(SPIS_1_SPI_MODE_0 | SPIS_1_SPI_MSB_FIRST);`

	Problem	Work Around

20.	There is no SPIM SCLK pin setting on P1_0 with CY7C64315/CY7C64316 devices.
	
	P1_0 is the SPIM SCLK pin for the CY7C64315/CY7C64316. However, when SPIM is placed, P1_0 is not automatically configured to be the SCLK output pin. The pin needs to be manually configured as a digital output, and a bit in the IO_CFG register needs to be set to select P1_0 as the SPI CLK.
	
	The other SPI pins are set up properly in these devices.
		1. In the pin editor, select strong drive for P1_0.
		
		2. Set bit 2 of IO_CFG before starting SPIM. For example:
		
		`IO_CFG |= 0x04;`
		`SPIM_1_Start(SPIM_1_SPI_MODE_0 | SPIM_1_SPI_MSB_FIRST);`

21.	The CY8C28xxx family allows 2 placements for I^2C with 4 possible pin configurations (2 for each placement). Problems can occur if the block is moved around and different pin placements are selected without deleting and replacing the user module. The pins can be manually reconfigured but PSoC Designer does not automatically clear pins to a default state after they have been selected for I^2C.	Delete and re-place the I2C User Module.
22.	Input MUX connection not shown for INS AMP User Module (two op amp instrumentation amplifier) in the interconnect view of PD 5.0 for CY8C24x94 devices.	Though the connection is not shown in the interconnect view, the registers controlling the input to the CT blocks, ACBxxCR1, are modified to connect the input to the port pins. This is just not reflected in the interconnect view. This will be fixed in a future release.
23.	The chip-level view and pin-out view of the NVPSoC (CY8CNP102) in PSoC Designer 5.0 indicates that pin P1_4 is present and P1_6 is not. It should be the other way around. P1_6 is present in NVPSOC and P1_4 is not.	None at this time. This is scheduled to be fixed in the next release.

	Problem	Work Around
24.	Upon reopening and generating/building a CY8C20x34, CY8C20x46, or CY8C20x66 project, the generated code disables any connections to the Analog Mux Bus shown in the chip level view.	After reopening the project, but before generating/building, manually disconnect and reconnect each of the Analog Mux Bus connections shown in the chip level view. Alternatively, disconnect all Analog Mux Bus connections in the chip level view, and initialize the connections in application code by writing to the applicable MUX_CRx registers.

Documentation

User guides and key documents are located in the `\Documentation` subdirectory of the PSoC Designer installation directory. The default location is:

C:\Program Files\Cypress\PSoC Designer 5\Documentation

Also included in this documentation folder is a documentation guide which can assist you in understanding all the documentation that is included with PSoC Designer 5.0.

Supporting documents for PSoC Designer's public-domain functionality, using "Find in Files" text search (*grep.pdf*) and the build utility (*make.pdf* and *sed.pdf*), are located in:

…\Program Files\Cypress \PSoC Designer 5\Documentation\Supporting Documents

PSoC Training

We recommend that first time users download and take PSoC Designer *Module 1: Introduction to PSoC* for free by visiting www.cypress.com/psoctraining.

Silicon Errata

The most up-to-date versions of the silicon errata are available on the web site at http://www.cypress.com/psoc and navigating to **Errata Update → PSoC Mixed-Signal Array**.

For assistance go to http://www.cypress.com or contact our Applications Team at 425.787.4814.

Cypress Semiconductor
198 Champion Ct.
San Jose, CA 95134-1709 USA
Tel: 408.943.2600
Fax: 408.943.4730
Application Support Hotline: 425.787.4814
www.cypress.com

© Cypress Semiconductor Corporation, 2009. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

PSoC Designer™, Programmable System-on-Chip™, and PSoC Express™ are trademarks and PSoC® is a registered trademark of Cypress Semiconductor Corp. All other trademarks or registered trademarks referenced herein are property of the respective corporations.

This Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.