Release Notes srn015

PSoC Designer Version 4.3

Release Date: June 2, 2006

Thank you for your interest in PSoC Designer™ version 4.3. The information in this document lists installation requirements and describes software updates and changes.

System Requirements and Recommendations

System Requirement	Minimum	Recommended
▪ Processor Speed	500 MHz	1 GHz
▪ MB of RAM	256 MB	512 MB
▪ MB of Free Hard Drive Space	250 MB	300 MB
▪ Screen Resolution	1024x768	1280x1024
▪ CD-ROM Drive	✓	✓
▪ EPP Parallel Port		✓
▪ USB Port, preferably Open Host Controller or Universal	✓	✓
▪ Windows® 2000, XP (SP1)	✓	✓
▪ Microsoft Internet Explorer 6.0 (SP1)	✓	✓
▪ Adobe Reader (For Viewing of .PDF Documentation)	✓	✓

Updates

Check http://www.cypress.com/psocdesigner for the latest downloads of software and documentation.

New for 4.3

1. Changes to support the EP_CY8C20x34, which is the extension pack to add device support for CY8C20x34 devices.
2. Added support for CY8C24894 device.
3. New efficient math library routines that reduce Flash size and improve performance. The math library is documented in the "PSoC Designer: Libraries User Guide".
4. PSoC Power Estimator tool added for the CY8C24x94 family.
5. Inclusion of all PSoC Designer 4.2 service packs.
6. Improved Filter Design Wizard for the LPF and BPF User Modules
7. New Design Rule Check (DRC) that SC power is set to ON when ANY SC block is placed.
8. Design Rule Checks (DRCs) are now enabled by default.
9. PSoC Designer can now be used from a non-administrative account.

10. Extensibility support enables future Service packs and Extension packs to be incrementally installed and removed.

Defects Repaired in 4.3

1. (7219) Corrected a code generation error that caused the I2CCFG register to not reset when the I2CHW or EZI2C User Module unplaced or deleted.
2. (8270) Corrected code generation errors with Dynamic Reconfiguration that could leave the register bank setting in Bank 1 instead of Bank 0.
3. (6994) Corrected code generation errors that prevented the generation of psocgpioint.h and psocgpioint.inc when pin names were entered by the user, but no GPIO interrupt sources were enabled.
4. (7563/8256) Corrected code generation for the PRT5IE register for the CY8C24X94 and CY7C64215 devices.
5. Fixed in CY7C63300/m8c.h, CY7C63800/m8c.h, and CY7C63900/m8c.h. The defines for TCAPINTE and TCAPINTS have been given the same name TMRCR
6. (7318) Updated boot.tpl for CY7C603XX devices to remove 5V conditional code since these devices are spec'ed for 2.4-3.6V operation only.
7. (8240) Updated boot.tpl for CY8C29XXX devices to set the decimator into full algorithm mode at the start of the boot sequence. This saves 6 mA of power consumption if the decimator is not used by the application.
8. (8271) Updated boot.tpl for CY8C24x94 to set the ACB00CR0/ACB01CR0 to a preferred default state.
9. (8150) Previously, the entry of any character was allowed in the pin grid for pin names. Some special characters caused compiler/assembler errors. Those characters are now restricted.
10. (8246) The Compiler License Agreement Dialog Box works properly in most non-English Languages.

Updates and Enhancements to User Modules

1. Datasheets for most user modules are updated to correct documentation errors or to clarify user module characteristics.
2. (6492) USB and USBFS: Several defects are repaired. The USB and USBFS passed (USB 2.0 Spec) Chapter 8 and Chapter 9 testing
3. (8302) USBFS: Updated the ReadOUTEndpt() API function to change the CPU Clock to 12 MHz during when extracting data from the PMA Endpoint buffers.
4. (7766) AMPINV: Changed default RTapMux values to R15_1 for -47 gain and R14_2 for -23 gain.
5. (8363) I2CHW: Fixed the .h file definition of I2C_TX
6. (7494) I2CM: Prevent SDA and SCL assignment to the same pin.

New User Modules

Details on the following new user modules are available in the PSoC Designer Device Editor User Module Selection View.

New User Modules supporting all PSoC devices.

1. 7 Segment LED (LED7SEG)

2. Light Emitting Diode (LED)

New User Modules supporting CY8C42XXX PSoC devices.

1. Incremental ADC (ADCINC)
2. Fixed Function Counter/Timer (ATMRCTR16)
3. Analog Comparator (CMP)
4. Current DAC (IDAC)
5. Voltage DAC (VDAC)
6. Integrated 8- and 16-Bit PWM with Deadband (IPWMDB8/IPWMDB16)
7. Power Block (PBLOCK)

Updates That Can Affect Previous Projects

Floating-Point Math:
The floating-point implementation was completely rewritten. Except for one feature, the new version implements the IEEE-754 standard for floating-point numbers (single precision). The omission is that denormalized numbers are truncated to '0'.
Because the old implementation did not adhere to the IEEE standard, calculations using the new implementation are not necessarily binary identical to calculations using the old implementation.

CSR User Module for CY8C21x34:
This UM was updated, but it is not detected by the "Project Update" function. Regenerate the source "Config", "Generate Application" to bring in the latest UM, and then rebuild your project. The old API for a slider centroid position (CSR_1_bGetCentroidPos, where CSR_1 is the instance name) was removed and replaced with CSR_1_iGetCentroidPos. For old programs, the recommended change is to use the centroid value directly from the following global symbol:

```
extern WORD CSR_1_iCtrdPos;
```

Analog Comparator Update:
Before PSoC Designer 4.3 when using dynamic reconfiguration, analog comparators stayed connected from configuration to configuration. A manual overwrite was required to remove the connection when moving from one configuration to another. PSoC Designer 4.3 now clears analog comparator connections between configurations.

Analog Comparators Disconnected In Old Projects:
In projects created before PSoC Designer 4.3, if you used analog comparators, be aware that PSoC Designer 4.3 disconnects all connected analog comparators in all configurations except the base configuration. Check comparator connections in all configurations and reconnect any comparators that became disconnected when upgrading to PSoC Designer 4.3.

How to Protect Project from Unintentional Alteration:
In version 4.3, and new setting has been added to "Project", "Settings", "Device Editor" to lock-down a device configuration and prevent any device or user module updates. This is a check-box labeled "Lock device configuration". You may manually choose this or it is automatically set if you select "Cancel" or "Revert" from the "Project Update" dialog box.

Project Cloning Causes "Project Update" Dialog to Appear
The best thing to do is to choose "Update". If you choose "Cancel" or "Revert", the "Lock device configuration" check box is set. To regenerate the configuration, you must go to "Project", "Settings", "Device Editor" and uncheck "Lock device configuration".

PSoC Designer Project Migration Compatibility

1. Two dialog boxes are encountered when opening a project from an older release:
   - The first is the "Old Version" dialog box. It notifies the user about the necessity to update the current project in order to comply with the current version of PSoC Designer and gives the option to perform a project update immediately or postpone it until later. Any changes made in *boot.tpl*, such as added jumps in the interrupt vector table, must be migrated to the new *boot.tpl*.
   - The second dialog is the "Outdated User Modules" dialog box. This dialog provides users with the list of outdated User Modules. The update process happens automatically during the source generation. When source is generated, the new files are added to the project and the old file is moved to the backup directory. The interrupt files contain start and end markers for user code. User code placed within user code markers is automatically carried into the new file. For migration, make sure that user code is between user code markers following the first "Generate Application" invocation after upgrading to 4.2. You may need to modify the source code manually after the first application generation to avoid compilation errors.
   - You must generate the source before closing the updated project dialog box in order for the update to take effect. If source is not generated, old files remain in the project and the out-of-date status is lost. An updated file can be generated for your project at any time. Right click the file in the source tree and select Remove from Project. When source is generated, the new file is added to the project and the old file is moved to the backup directory.
2. When migrating projects to the CY8C29x66 using cloning, the compiler and linker default to using the small memory model (SMM). Use the Project >> Settings, Compiler tab to "Enable paging" for the large memory model (LMM).
3. When migrating projects to the CY8C29x66 using assembly language:
   - Additional code is required to manage RAM pages.
   - A small number of User Module API function calls may need changing. See AN2218 PSoC Large Memory Model Programming for details.
   - Reference Application Note AN2218 PSoC Large Memory Model Programming under …`\Program Files\Cypress MicroSystems\PSoC Designer\Documentation` or on http://www.cypress.com for guidance.
4. See the CY8C25xxx/26xxx to CY8C27xxx Project Migration Application Note AN2131 for migrating projects to a new product family. This process is mostly automatic, but may require some manual steps. (…`\Program Files\Cypress MicroSystems\PSoC Designer\Documentation\Migrating Projects to CY8C27`). Note that Ports 3 and 4 have swapped pins in the CY8C27xxx parts with respect to the CY8C26xxx parts. This affects any 44- or 48-pin project.
5. Projects from previous PSoC Designer releases have *projectname_globalparams.inc* and *projectnameapi.h* under the Library Source folder. These files were replaced with *globalparams.inc* and *psocapi.h* and are manually removed by right clicking the file icon and selecting Remove from Project.

Documentation

User guides and key documents are located in the `\Documentation` subdirectory of the PSoC Designer installation directory. The default location is `C:\Program Files\Cypress MicroSystems\PSoC Designer\Documentation`. This directory is accessed within PSoC Designer under Help >> Documentation. The documents are .PDF files and require Adobe Reader for viewing.

Documents include:

- *PSoC Designer: Integrated Development Environment User Guide*
- *PSoC Designer: Assembly Language User Guide*
- *PSoC Designer: C Language Compiler User Guide*
- *PSoC Designer: ICE-4000 USB Adapter Installation Guide*
- *PSoC Designer: ICE Connection Troubleshooting Guide*
- *PSoC Designer: PSoC Programmer User Guide*
- *PSoC Designer: Libraries User Guide*
- *CY8C29x66 PSoC Mixed-Signal Array Data Sheet*
- *CY8C27x43 PSoC Mixed-Signal Array Data Sheet*
- *CY8C25-26xxx PSoC Device Family Data Sheet*
- *CY8C24794 PSoC Mixed-Signal Array Data Sheet*
- *CY8C24x23A PSoC Mixed-Signal Array Data Sheet*
- *CY8C24x23 PSoC Mixed-Signal Array Data Sheet*
- *CY8C22x13 PSoC Mixed-Signal Array Data Sheet*
- *CY8C26xxx_Master.pdf Interface Diagram/Worksheet*
- *Web Help: Document Web Links*
- *PSoC Technical Reference Manual (TRM)*
- *Large Memory Programming*
- *Migrating to the Large Memory Model PSoC Devices*
- *PSoC Pod Compatibility Guide*
- *PSoC Device Selector Guide AN2209*

Supporting documents for PSoC Designer's public-domain functionality, such as "Find in Files" text search (*grep.pdf*) and the build utility (*make.pdf and sed.pdf*), are located in …`\Program Files\Cypress MicroSystems\PSoC Designer\Documentation\Supporting Documents`.

Tele-Training

We recommend that first time users attend the Module 1: Introductory Module of our Tele-Training program. The following Tele-Training modules are available:

PSoC Pre-Recorded Video Module 1: Introductory Module
PSoC Pre-Recorded Video Module 2: Getting Started Designing
PSoC Pre-Recorded Video Module 3: Getting Started Debugging
PSoC Pre-Recorded Video Module 4: Dynamic Re-configuration
PSoC Module 5: Advanced Analog Design
PSoC Pre-Recorded Video Module 1: Introduction to PSoC Express
PSoC Pre-Recorded Video Module 2: CY3210-ExpressDK PSoC Express Development Kit
PSoC Pre-Recorded Video Module 3: Hands On PSoC Express

Capacitive Touch Sensing with PSoC
Jazz-up your user interface with PSoC-enabled Capacitive Touch Sensing

Go to http://www.cypress.com/support/training.cfm for details.

Example Projects

It is instructive for a new user to view or test the Example Projects. They are located in three directories by product family:
`…\Program Files\Cypress MicroSystems\PSoC Designer\Examples\CY8C24`, `…\CY8C27`, and `…\CY8C29`, respectively. (This is the default installation path for PSoC Designer.) Example projects include:

Examples for the CY8C24x23A, CY8C27x43, and CY8C29x66 parts:

- ASM_Example_ADC_UART_LCD
- ASM_Example_Blink_LED
- ASM_Example_DAC_ADC
- ASM_Example_Dynamic_PWM_PRS
- ASM_Example_LED_Logic
- C_Example_ADC_UART_LCD

Installation Issues

Parallel Port Considerations

1. Proper installation of PSoC Designer on Windows NT/2000/XP requires a user to have local Administrator permission.
2. Windows Active Desktop is not supported. PSoC Designer may not function correctly if the Windows Active Desktop is enabled.
3. Windows XP compatibility mode causes problems for PSoC Designer's debugging with a parallel port. Do not enable compatibility mode.
4. Upgrading from Windows 95/98/Me to Windows NT/2000/XP requires uninstalling PSoC Designer before the upgrade and reinstalling PSoC Designer after the Windows upgrade. If this is not done, PSoC Designer's parallel port drivers are not updated to match the new operating system.
5. On Windows XP, logging off and on may cause problems with parallel port connections to the ICE. This is fixed by following these steps:

    - *Open the Start Menu*
    - *Select Settings*
    - *Open the Control Panel*
    - *Open Administrative Tools*
    - *Open Local Security Policy (may not be available in Windows XP Home Edition)*
    - *Open Local Policies*
    - *Open Security Options*
    - *Disable the "Strengthen default permissions of internal system objects" setting*
    - *Reboot PC*

6. The PSoC ICE-4000 provides significant debugging functionality that requires full two-way communication over the ICE-4000 to operate. There are several steps in the connection process, including both setting up hardware, and making a communications connection in the software. Making the software connection often requires changes in the BIOS settings for the LPT port. Some recent laptops do not support EPP and Bidirectional modes in the BIOS needed for full two-way communication over the ICE-4000. A relatively easy method that bypasses the need for changing the BIOS settings is to install a parallel port card.

   This has the added benefit of providing a dedicated port to the ICE without potential conflicts with other applications or printers a user may have on their computer. The *PSoC Designer: ICE Troubleshooting Guide* details parallel port cards for both desktops and laptops that were tested for compliance with the ICE-4000.
   The mode of operation for the parallel port is affected when some laptops return from sleep. Often, ICE connection cannot be resumed. Restarting the system rectifies this situation.

USB Considerations

1. If you have trouble connecting to the ICE-4000 via the USB Adapter or the ICE-Cube, see Debugger Subsystem and Debugger Error Messages in the PSoC Designer Help System and the *PSoC Designer: ICE Troubleshooting Guide* for more details. If the problems persist, contact Cypress MicroSystems.

   We want to assist you with the ICE connection. If the information in the PSoC Designer Help System or the *PSoC Designer: ICE Troubleshooting Guide* is not sufficient to resolve issues, please use the following resources:

   TightLink Email Support System
   You can enter a support request in this system with a guaranteed response-time of four hours: http://www.cypress.com/support/login.cfm.

   Support Forums
   View and participate in discussion threads about a wide variety of PSoC device topics: http://www.cypress.com/forums/.

2. The Open Host Controller Interface (OHCI) allows USB communication with the ICE to operate up to 30% faster than the Universal Host Controller Interface (UHCI). This improves download and debugging speed. To find out which interface you are using, in the “Device Manager,” look under the “Universal Serial Bus controllers” heading. You see one of these three Host Controllers: Universal, Open, or Enhanced. Based on the port to which you are connected, the USB Adapter will default to either Universal or Open. Typically, Intel motherboards have UHCI. Most PCI USB hubs are OHCI.

ICE and Pod Hardware

NOTE: ICE4000 Only Supports CY8C24x23 and CY8C27xxx Families
The older in-circuit emulator ICE4000 does not support new PSoC families. We recommend that you purchase a newer ICE Cube (which is sold as a kit called CY3215-DK) for best results.

1. Rev. A Pods are required for emulation of CY8C22x13, CY8C24x23, CY8C27x43, and CY8C29x66 parts.
2. Rev. G Pods, or later, are required for the CY8C25xxx/26xxx family devices. The ICE-Cube in-circuit emulator does not support the CY8C25/26xxx family. The ICE-4000 continues to support this family of PSoC devices.
3. YProgrammer boards are required for programming the CY8C22x13, CY8C24x23, CY8C24x23A, CY8C25xxx/26xxx, CY8C27x43, and CY8C29x66 family devices using the ICE-4000. The ICE-Cube, with attached ISSP cable, enables programming without the YProgrammer.

Device Editor Subsystem Notes and Errata

1. The device editor in general allows settings in combinations that are supported by the underlying hardware. In some cases, this means that mutually exclusive settings (such as selections for an output bus) are allowed by the device editor.
2. Cloning from a PSoC device to a PSoC device in which the number of analog resources is reduced (i.e., From a CY8C24xxx to a CY8C22xxx) may stop the placement of one or more analog user modules. It is necessary to delete the analog user module and then add the same user module back into the project.
3. The CPU Clock global resource setting for the PSoC devices that have the SLIMO feature now displays the CPU Clock frequency as “SysClk/N” where N is of the set {1,2,4,8,16,32,64,128 and 256}. For customers updating to 4.2 for CY8C29x66 and CY8C24x23 PSoC devices, the CPU Clock setting defaults to “SysClk/8” (3 MHz) when opening the project for the first time in this release. This is because of a GUI change. Changing the value and then saving the project restores the correct CPU Clock global parameter.
4. Printing the project data sheet of a very large project may result in missing user module parameters.
5. The Acer TravelMate 800 Notebook (with a MOBILITY RADEON 9000 Graphics Adapter) may cause the schematic area in the Interconnect View to go blank when the Navigation Help window appears. Closing the Navigation Help window causes the Interconnect View window divider to move.

Debugger Subsystem/ICE Errata

1. The Debugger does not detect Flash size limits during emulation. For parts that have less than 16K of Flash, exercise caution that designs work within the memory limits. The complex and sequential breakpoints offered by the Events feature in the Debugger subsystem provide a means for detecting stack and memory overflows during development.
2. Analog register display scrambled when Successive Approximation Register ADC (SAR) operation is enabled. Enabling SAR operation (i.e., SAR count > 0) in the Analog Synchronization Register (ASY_CR) scrambles the Debugger register Bank 0 and 1 analog register displays. Enabling the SAR stalls the M8C CPU until analog register data is ready, but does not stall the on-chip Debugger interface used by PSoC Designer. As a result, the analog register contents displayed by PSoC Designer are incorrect. M8C programs that read the registers still get the correct data. This only affects analog block registers.
3. On some machines, unplugging the pod from the ICE may result in the inability to reconnect. If this occurs, power cycling of the ICE may be required.

4. Adding a Flash watch variable will default to a RAM address. To correct this, reselect the FLASH memory space in the Flash Watch Variable's property dialog box.
5. You cannot set watch variables with values greater than 0x7FFFFFFF.

Debugger Subsystem/ICE Notes

1. The Debugger switches to 3 MHz CPU operation when halted. The status bar shows the user-selected CPU speed while halted but the on-chip digital PSoC blocks are running with SysClk at 3 MHz. This may affect external hardware.
2. System clock-jitter on the target circuit board may cause emulation to fail when PLL mode is enabled. The failure symptom is usually an Invalid Memory Reference.
3. The Debugger cannot halt immediately after an instruction that puts the M8C into sleep mode. This means that it cannot step over sleep, hit a breakpoint immediately after a sleep, or halt at an event point immediately after sleep.
   Placing a breakpoint further away from the sleep instruction is recommended. Clicking the Halt icon to exit sleep is okay, assuming that the sleep interrupt has been enabled. If the sleep interrupt has not been enabled and the part goes into sleep, the ICE disconnects when a halt is executed. Occasionally, with the USB Adapter, the ICE disconnects when debugging with sleep.
4. A breakpoint on the instruction immediately following the SSC_Action macro does not halt the debugger. The breakpoint halts on the second instruction after the SSC_Action macro.
5. When the CY8C29xxx/27xxx/24xxx/22xxx parts are debugging, the ICE enables the sysclk * 2 (doubler).
6. False event triggers occur. Setting the event to break on an Instruction Register (IR) with a NOP (opcode 0x40) triggers the event following a "go" from reset. Setting an event to break when the Program Counter (PC) is above the user code causes a halt to occur following a "go" from Reset.

C Compiler/Assembler/Build System Errata

1. Code compression settings (found in "Project" Settings", "Compiler") are not currently compatible with dynamic configuration.
2. For certain corner case input values (close to zero or infinity), the following functions found in *math.h* are known to return incorrect results: sinh(), cosh(), tanh(), atan2().
3. Internal references prevent API elimination from removing certain parts of functions that need removal.

C Compiler/Assembler/Build System Notes

1. The "TOP" area is reserved for the boot code (*boot.asm*) and has special linker implications. Do not create code within a "TOP" area declared in another source file, other than *boot.asm*.
2. In C, the total size of arrays and structures is limited to 256 bytes, even in the large memory model.
3. Use of the code compressor makes debugging very difficult when two or more blocks of code are combined into a single "subroutine." The problem is that the debugger does not know which chunk of associated source code to display. This can be partially mitigated

by using step assembly as necessary or, when possible, by turning code compression off.

Library Notes

New low-level arithmetic library routines are provided. They can be called from C as well as assembly language. The new routines are faster and more compact than the previous implementation. The routines are documented in PSoC Designer: Libraries User Guide.

User Module Errata

1. ADCINCVR iGetData API can result in data skewing if interrupt occurs in between LSB and MSB handling. The work around is to set the flag to check for mismatched data in between LSB and MSB.
2. (8362) A known issue in the Timer8, Timer16, Timer24, and Timer32 User Modules cause a build error for the CY8C42XXX device family. This will be fixed before the final release of PSoC Designer 4.3.
3. CSR UM was updated, but it is not detected by the “Project Update” function. We recommend that you regenerate the source “Config”, “Generate Application” to bring in the latest UM, and then rebuild your project. The old API for a slider centroid position (CSR_1_bGetCentroidPos, where CSR_1 is the instance name) was removed and replaced with CSR_1_iGetCentroidPos. For old programs, the recommended change that is to use the centroid value directly from the following global symbol:

   ```
   extern WORD CSR_1_iCtrdPos;
   ```

For assistance go to http://www.cypress.com or contact our Application Team at 425.787.4814.

Silicon Errata

The most up-to-date versions of the silicon errata are available on the web site by following the link and navigating to Software & Drivers >> Errata Update (tab) >> PSoC Mixed-Signal Array at http://www.cypress.com/psoc.

Cypress Semiconductor
2700 162nd Street SW, Building D
Lynnwood, WA 98037
Phone: 425.787.4400
Fax: 425.787.4641
Application Support Hotline: 425.787.4814
http://www.cypress.com/



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