Release Notes srn013

PSoC Designer Version 4.2 Release

Release Date: September 18, 2004

Thank you for your interest in PSoC™ Designer version 4.2. The information in this document lists installation requirements and describes software updates and changes.

System Requirements and Recommendations

System Requirement	Minimum	Recommended
▪ Processor Speed	500 MHz	1 GHz
▪ MB of RAM	256 MB	512 MB
▪ MB of Free Hard Drive Space	150 MB	200 MB
▪ Screen Resolution	1024x768	1280x1024
▪ CD-ROM Drive	✓	✓
▪ EPP Parallel Port		✓
▪ USB Port, preferably Open Host Controller or Universal	✓	✓
▪ Rev. A or Later - Emulation Flex-Pod for CY8C29x66 Product Family	✓	✓
▪ Rev. A or Later - Emulation Pod for CY8C27x43 Product Family	✓	✓
▪ Rev. A or Later - Emulation Pod for CY8C24x23 and CY8C22xxx Product Families	✓	✓
▪ Rev. G or Later - Emulation Pod for Product Family CY8C25xxx/26xxx	✓	✓
▪ Windows® 98, NT4.0 (SP6), 2000, Me, XP (SP1)	✓	✓
▪ Microsoft Internet Explorer 6.0 (SP1)	✓	✓
▪ Adobe Reader (For Viewing of .pdf Documentation)	✓	✓

Updates

Check http://www.cypress.com/ under PSoC Mixed-Signal Array >> Software & Drivers (and More Resources) for the latest downloads of software and documentation.

New for 4.2

1. Support for the new in-circuit emulator, ICE-Cube, for seamless connection, debugging, 5V, 3.3V and 2.7V operation, and programming. (ICE-Cube can supply power at 5V and 3.3V operations, but 2.7V operation requires board-supplied power.)

2. Support has been added for the new PSoC device families: CY8C29x66, CY8C27x43, and CY8C24x23A. This support includes the SLIMO feature of these chips, enabling lower SysClk clock values to save power.

3. New standalone device programming software, called “PSoC Programmer,” accessible from within PSoC Designer and as a standalone application. If the “Program Part” icon/menu item is inactive in PSoC Designer, the PSoC Programmer software needs to be installed. This program allows programming, checksum, verification, and reading of a PSoC device.

4. “Drag-to-move” capability in the Device Editor, Interconnect View, where you can use the mouse to move User Modules, thus saving time, especially with the larger number of digital PSoC blocks in the CY8C29x66 parts.

5. Under Tools >> Options >> Debugger tab you can choose to “Execute Go“ as part of “Execute Program” command. The Execute Program command takes the program automatically on through connection, downloading, and into debug run (if selected). It will execute for as long as it can without hitting an error in the process, a break point, or event break.

6. In the Device Editor, Interconnect View, the inactive target placers (blue highlights) of multi-block User Modules are now identified by a “group” name across the top.

7. In the Device Editor, Interconnect View, you can press the [**Space Bar**] to rotate and see the placement options around the anchor block of a multi-block User Module.

8. Upon selection of User Modules with multiple topologies, a selection wizard will appear from which you can specify a topology as well as print details.

9. You can now print from within the Filter Design Wizard (for User Modules that require additional options to be specified.)

10. Non-block resources that placed User Modules utilize are now identified in the Device Editor, Interconnect View (i.e., muxes).

11. Debugger subsystem supports multiple RAM memory pages for the CY8C29x66 device family.

12. The “About PSoC Designer” dialog box will now display Service Pack number.

Defects Repaired in 4.2

1. Floating point multiplication of very small (un-normalized) numbers has been fixed to no longer rapidly increase in size.
2. XP logoff and logon no longer causes “ICE port not open” failure.
3. Cloned projects no longer display non-existent output files duplicated from original project.
4. LoadConfig: C Frame pointer no longer gets unintentionally corrupted.
5. *boot.tpl* Link default re-locatable start address corrected.
6. Corrected base address and size of AREAs in .map file.
7. *int.asm* includes banners for entering user code sections to handle constants, includes, and exports.
8. Added ability to successfully step into an immediate macro inside a #pragma fastcall function.
9. Breakpoints can be set while program is running.
10. C math “pow” function fixed.
11. Last instruction in *main* is not RETI. If the last instruction in _main is a 1-instruction infinite loop, boot can jump to main rather than call, thus saving two bytes of stack space.

Updates That Can Affect Previous Projects

Analog Comparator Update:
Previous to PSoC Designer 4.2 when using dynamic re-configuration analog comparators stayed connected from configuration to configuration, a manual overwrite was required to remove connection when moving from one configuration to another. PSoC Designer 4.2 now clears analog comparator connections in between configurations.

How to Protect Project From Unintentional Alteration:
In projects created before PSoC Designer 4.2, if you used analog comparators, be aware that PSoC Designer 4.2 will disconnect all connected analog comparators in all configurations except the base configuration. Check comparator connections in all configurations and re-connect any comparators that may have become disconnected when upgrading to PSoC Designer 4.2.

Updates and Enhancements to User Modules

1. Paged SRAM support has been added to User Modules in the CY8C29x66 device family.
2. ADCINC12 first conversion has been fixed.
3. I2CHW – Multi-master support has been added.
4. TX8 and UART – New API, SetTxintMode, allows dynamic shift interrupt source at run time.
5. SPIS “Slave Select input” parameter accessible from the GUI in CY8C27143 (8-pin part).
6. DELSIG8, DELSIG11, and SPI .inc and .h define and equates are now equivalent.
7. TX8 and RX8 “data output” and “clock output” parameters added. These parameters are for when the TX8 is used with the CRC.
8. CMPPRG gain values 0.042 and 0.021 are now valid.
9. User Module data sheet updates:
    - I2CHW: “I2C Clock" and the "CPU_Clk_speed" parameters are described in the data sheet.
    - RX8 and TX8: “parity” parameter clarified.
    - ADCINVR: iGetData API includes explanation for avoiding data skewing.
    - AMUX4: CY8C22x13 MUX diagram clarified.
    - IrDATX: Output header and bit-timer header clarified.

New User Modules

1. ADCINC – family of 2 efficient, low-latency incremental converters with first and second order modulators. Six to 12-bit resolution with maximum sampling rates of 0.125K to 31.25K samples per second can be achieved.
2. DelSig – family of 8 efficient, low-latency Delta Sigma converters with first and second order modulators for the 8YC29x66 family of PSoC devices. Six to 14-bit resolution with maximum sampling rates of 7.8K to 62.5K samples per second can be achieved depending upon the decimation rate.
3. DigBuf – a two-input, two-output digital buffer that uses only one digital PSoC block.

IP Reference Designs for the Design Browser

Removal of the Modem 3000 Design IP:
The Modem 3000 Design IP project has been removed. It can be found on the Cypress web site.

PSoC Designer Project Migration Compatibility

1. See the CY8C29x66 Project Migration document for migrating projects to a new product family. This process is mostly automatic, but will likely require some manual steps. The document can be found within the `\Documentation` folder of the PSoC Designer installation directory.
2. When migrating projects to the CY8C29x66 using cloning, the compiler and linker will default to using the small memory model (SMM). Use the Project >> Settings, Compiler tab to "Enable paging" for the large memory model (LMM).
3. When migrating projects to the CY8C29x66 using assembly language:
   - Additional code is required to manage RAM pages.
   - A small number of User Module API function calls may need to be changed. See AN2218 PSoC Large Memory Model Programming for details.
   - Reference Application Note AN2218 PSoC Large Memory Model Programming under …`\Program Files\Cypress MicroSystems\PSoC Designer\Documentation` or on http://www.cypress.com for guidance.
4. See the CY8C25xxx/26xxx to CY8C27xxx Project Migration Application Note AN2131 for migrating projects to a new product family. This process is mostly automatic, but may require some manual steps. (…`\Program Files\Cypress MicroSystems\PSoC Designer\Documentation\Migrating Projects to CY8C27`). Note that Ports 3 and 4 have swapped pins in the CY8C27xxx parts with respect to the CY8C26xxx parts. This will affect any 44- or 48-pin project.
5. Two dialog boxes are encountered when opening a project from an older release:
   - The first is the "Old Version" dialog box. It notifies the user about the necessity to update the current project in order to comply with the current version of PSoC Designer and gives the option to perform a project update immediately or postpone it until later. Any changes made in *boot.tpl*, such as added jumps in the interrupt vector table, must be migrated to the new *boot.tpl*.
   - The second dialog is the "Outdated User Modules" dialog box. This dialog provides users with the list of outdated User Modules. The update process happens automatically during the source generation. When source is generated, the new files will be added to the project and the old file will be moved to the backup directory. The interrupt files contain start/end markers for user code. User code placed within user code markers will automatically be carried into the new file. For migration, make sure that user code is between user code markers following the first "Generate Application" invocation after upgrading to 4.2. You may have to modify the source code manually after the first application generation to avoid compilation errors.
   - Source must be generated before closing the updated project dialog box in order for the update to take effect. If source is not generated, old files will remain in the project and the out-of-date status will be lost. An updated file can be generated for your project at any time. Right-click on the file in the source tree and select Remove from Project. When source is generated, the new file will be added to the project and the old file will be moved to the backup directory.
6. Projects from previous PSoC Designer releases will have *projectname_globalparams.inc* and *projectnameapi.h* under the Library Source folder.

These files have been replaced with *globalparams.inc* and *psocapi.h* and can be manually removed by right-clicking on the file icon and selecting Remove from Project.

Documentation

User guides and key documents are located in the `\Documentation` subdirectory of the PSoC Designer installation directory. The default location is `C:\Program Files\Cypress MicroSystems\PSoC Designer\Documentation`. This directory can be accessed within PSoC Designer under Help >> Documentation. The documents are .pdf files that require Adobe Reader.

Documents include:

- *PSoC Designer: Integrated Development Environment User Guide*
- *PSoC Designer: Assembly Language User Guide*
- *PSoC Designer: C Language Compiler User Guide*
- *PSoC Designer: ICE-4000 USB Adapter Installation Guide*
- *PSoC Designer: ICE Connection Troubleshooting Guide*
- *PSoC Designer: PSoC Programmer User Guide*
- *CY8C29x66 PSoC Mixed-Signal Array Data Sheet*
- *CY8C27x43 PSoC Mixed-Signal Array Data Sheet*
- *CY8C25-26xxx PSoC Device Family Data Sheet*
- *CY8C24x23A PSoC Mixed-Signal Array Data Sheet*
- *CY8C24x23 PSoC Mixed-Signal Array Data Sheet*
- *CY8C22x13 PSoC Mixed-Signal Array Data Sheet*
- *CY8C26xxx_Master.pdf Interface Diagram/Worksheet*
- *Web Help: Document Web Links*
- *PSoC Technical Reference Manual (TRM)*
- *Large Memory Programming*
- *Migrating to the Large Memory Model PSoC Devices*
- *PSoC Pod Compatibility Guide*
- *PSoC Device Selector Guide AN2209*

Supporting documents for PSoC Designer's public-domain functionality, such as "Find in Files" text search (*grep.pdf*) and the build utility (*make.pdf*), are located in …`\Program Files\Cypress MicroSystems\PSoC Designer\Documentation\Supporting Documents`.

Tele-Training

It is recommended that first time users attend the Module 1: Introductory Module of our Tele-Training program. The following Tele-Training modules are available:

Module 1: Introductory Module
Module 2: Getting Started Designing
Module 3: Getting Started Debugging
Module 4: Dynamic Re-configuration
Module 5: Advanced Analog Design
LIN Bus Information Session
Pre-Recorded Video Module 1: Introductory Module
Pre-Recorded Video Module 2: Getting Started Designing
Pre-Recorded Video Module 3: Getting Started Debugging
Pre-Recorded Video Module 4: Dynamic Re-configuration

Go to http://www.cypress.com/support/training.cfm for details.

Example Projects

It is instructive for a new user to view or test the Example Projects. They are located in three directories by product family: …\Program Files\Cypress MicroSystems\PSoC Designer\Examples\CY8C24, …\CY8C27, and …\CY8C29, respectively. (This is the default installation path for PSoC Designer.) Example projects include:

Examples for the CY8C24x23A, CY8C27x43, and CY8C29x66 parts:

- ASM_Example_ADC_UART_LCD
- ASM_Example_Blink_LED
- ASM_Example_DAC_ADC
- ASM_Example_Dynamic_PWM_PRS
- ASM_Example_LED_Logic
- C_Example_ADC_UART_LCD

Installation Issues

Parallel Port Considerations

1. Proper installation of PSoC Designer on Windows NT/2000/XP requires a user to have local Administrator permission.
2. Windows Active Desktop is not supported. PSoC Designer may not function correctly if the Windows Active Desktop is enabled.
3. Windows XP compatibility mode causes problems for PSoC Designer's debugging with a parallel port. Compatibility mode should not be enabled.
4. Upgrading from Windows 95/98/Me to Windows NT/2000/XP requires uninstalling PSoC Designer before the upgrade and reinstalling PSoC Designer after the Windows upgrade. If this is not done, PSoC Designer's parallel port drivers will not be updated to match the new operating system.
5. On Windows XP, logging off and on may cause problems with parallel port connections to the ICE. This can be fixed by execution of the following steps:

    - *Open the Start Menu*
    - *Select Settings*
    - *Open the Control Panel*
    - *Open Administrative Tools*
    - *Open Local Security Policy (may not be available in Windows XP Home Edition)*
    - *Open Local Policies*
    - *Open Security Options*
    - *Disable the "Strengthen default permissions of internal system objects" setting*
    - *Reboot PC*

6. The PSoC ICE-4000 provides significant debugging functionality that requires full two-way communication over the ICE-4000 to operate. There are several steps in the connection process, including both setting up hardware, and making a communications connection in the software. Making the software connection will likely require changes in the BIOS settings for the LPT port. Some recent laptops do not support EPP and Bi-directional modes in the BIOS needed for full two-way communication over the ICE-4000. A relatively easy method that bypasses the need for changing the BIOS settings is to install a parallel port card.

This has the added benefit of providing a dedicated port to the ICE without potential conflicts with other applications or printers a user may have on their computer. The *PSoC Designer: ICE Troubleshooting Guide* details parallel port cards for both desktops and laptops that have been tested for compliance with the ICE-4000.
The mode of operation for the parallel port can be affected when some laptops return from sleep. Often, ICE connection cannot be resumed. Rebooting the system rectifies this situation.

USB Considerations

1. If you have trouble connecting to the ICE-4000 via the USB Adapter or the ICE-Cube, see Debugger Subsystem and Debugger Error Messages in the PSoC Designer Help System and the *PSoC Designer: ICE Troubleshooting Guide* for more details. If the problems persist, contact Cypress MicroSystems.

   We want to assist you with the ICE connection. If the information in the PSoC Designer Help System or the *PSoC Designer: ICE Troubleshooting Guide* is not sufficient to resolve issues, please use the following resources:

   TightLink Email Support System
   You can enter a support request in this system with a guaranteed response-time of four hours: http://www.cypress.com/support/login.cfm.

   Support Forums
   View and participate in discussion threads about a wide variety of PSoC device topics: http://www.cypress.com/forums/.

2. The Open Host Controller Interface (OHCI) allows USB communication with the ICE to operate up to 30% faster than the Universal Host Controller Interface (UHCI). This improves download and debugging speed. To find out which interface you are using, in the “Device Manager,” look under the “Universal Serial Bus controllers” heading. You will see one of these three Host Controllers: Universal, Open, or Enhanced. Based on the port to which you are connected, the USB Adapter will default to either Universal or Open. Typically, Intel motherboards have UHCI. Most PCI USB hubs are OHCI.
3. When installing PSoC Designer on a system with Windows Me, the USB Adapter and ICE-Cube in-circuit emulator must be unplugged.

ICE and Pod Hardware

1. Rev. A Pods are required for emulation of CY8C22x13, CY8C24x23, CY8C27x43, and CY8C29x66 parts.
2. Rev. G Pods, or later, are required for the CY8C25xxx/26xxx family devices. The ICE-Cube in-circuit emulator does not support the CY8C25/26xxx family. The ICE-4000 will continue to support this family of PSoC devices.
3. YProgrammer boards are required for programming the CY8C22x13, CY8C24x23, CY8C24x23A, CY8C25xxx/26xxx, CY8C27x43, and CY8C29x66 family devices using the ICE-4000. The ICE-Cube, with attached ISSP cable, will enable programming without the YProgrammer.
4. For current details regarding pods, go to:
   http://www.cypress.com/cfuploads/pub/PSoC_CY8C27X_DevToolsSelectorGuide.pdf
   http://www.cypress.com/cfuploads/pub/PSoC_CY8C25-26X_DevToolsSelectorGuide.pdf

Device Editor Subsystem Notes and Errata

1. Cloning from a PSoC device to a PSoC device in which the number of analog resources is reduced (i.e., From a CY8C24xxx to a CY8C22xxx) may cause one or more analog User Modules to be un-placeable. It will be required to delete the analog User Module and then add the same User Module back into the project.
2. The CPU Clock global resource setting for the PSoC devices that have the SLIMO feature now display the CPU Clock frequency as “SysClk/N” where N is of the set {1,2,4,8,16,32,64,128 and 256}. For customers updating to 4.2 for CY8C29x66 and CY8C24x23 PSoC devices, the CPU Clock setting will default to “SysClk/8” (3 MHz) upon opening the project for the first time in this release. This is due to a GUI change. Changing the value and then saving the project will restore the correct CPU Clock global parameter.
3. Printing the project data sheet of a very large project may result in missing user module parameters.
4. The Acer TravelMate 800 Notebook (with a MOBILITY RADEON 9000 Graphics Adapter) may cause the schematic area in the Interconnect View to go blank when the Navigation Help window appears. Closing the Navigation Help window causes the Interconnect View window divider to be moved.

Debugger Subsystem/ICE Errata

1. The Debugger does not detect Flash size limits during emulation. For parts that have less than 16K of Flash, the user must exercise caution that designs work within the memory limits. The complex/sequential breakpoints offered by the Events feature in the Debugger subsystem provide a means for detecting stack and memory overflows during development.
2. Analog register display scrambled when Successive Approximation Register ADC (SAR) operation is enabled. Enabling SAR operation (i.e., SAR count > 0) in the Analog Synchronization Register (ASY_CR) scrambles the Debugger register Bank 0 and 1 analog register displays. Enabling the SAR will stall the M8C CPU until analog register data is ready, but does not stall the on-chip Debugger interface used by PSoC Designer. As a result, the analog register contents displayed by PSoC Designer are incorrect. M8C programs that read the registers will still get the correct data. This only affects analog block registers.
3. On some machines, unplugging the pod from the ICE may result in the inability to reconnect. If this occurs, power cycling of the ICE may be required.
4. Adding a Flash watch variable will default to a RAM address. To correct this, re-select the FLASH memory space in the Flash Watch Variable’s property dialog box.
5. Watch variables cannot be set with values greater than 0x7FFFFFFF.

Debugger Subsystem/ICE Notes

1. The Debugger switches to 3 MHz CPU operation when halted. The status bar shows the user-selected CPU speed while halted but the on-chip digital PSoC blocks will be running with SysClk at 3 MHz. This may affect external hardware.
2. System clock-jitter on the target circuit board may cause emulation to fail when PLL mode is enabled. The failure symptom is usually an Invalid Memory Reference.
3. The Debugger cannot halt immediately after an instruction that puts the M8C into sleep mode. This means that it cannot step over sleep, hit a breakpoint immediately after a sleep, or halt at an event point immediately after sleep.

Placing a breakpoint further away from the sleep instruction is recommended. Clicking the Halt icon to exit sleep is okay, assuming that the sleep interrupt has been enabled. If the sleep interrupt has not been enabled and the part goes into sleep, the ICE will disconnect when a halt is executed. Occasionally, with the USB Adapter, the ICE will disconnect when debugging with sleep.

4. A breakpoint on the instruction immediately following the SSC_Action macro will not halt the debugger. The breakpoint will halt on the second instruction after the SSC_Action macro.
5. When the CY8C29xxx/27xxx/24xxx/22xxx parts are being debugged, the ICE enables the sysclk * 2 (doubler).
6. False event triggers can occur. Setting the event to break on an Instruction Register (IR) with a NOP (opcode 0x40) will trigger the event following a “go” from reset. Setting an event to break when the Program Counter (PC) is above the user code will cause a halt to occur following a “go” from Reset.

C Compiler/Assembler/Build System Errata

1. The Code Compressor and API elimination options do not appear in the large memory model due to frequent internal errors that will be corrected in a future update. In the meantime, use of the -O and -elim linker flags is possible by creating and modifying *local.mk* or *custom.lkp* but this practice is strongly discouraged. This will be corrected in a future release.
2. Returning array elements in C does not work correctly in the Large Memory Model for types that exceed 8 bits in size. Until corrected in the next release, an intermediate local variable can be used to work around the problem. In other words:

```
iTemp = iTable[k];
return iTemp;                 // rather than “return iTable[k];”
```

3. For certain corner case input values (close to zero or infinity), the following functions found in *math.h* are known to return incorrect results: sinh(), cosh(), tanh(), atan2().
4. In the Small Memory Model, internal references prevent the code compressor from removing certain API functions that ought to be removed.

C Compiler/Assembler/Build System Notes

1. Long path lengths (more that 94 characters) cause a *mkdepend.exe* error on systems running Windows 98 or Windows Me. If you receive a “cannot open mkdep” error, you will need to reboot your computer for the make system to function properly. The problem is remedied by copying the project to a shorter path.
2. The “TOP” area is reserved for the boot code (*boot.asm*) and has special linker implications. Do not create code within a “TOP” area declared in another source file, other than *boot.asm*.
3. In C, the total size of arrays and structures is limited to 255 bytes, even in the large memory model.
4. Use of the code compressor makes debugging very difficult when two or more blocks of code are combined into a single "subroutine." The problem is that the debugger does not know which chunk of associated source code to display. This can be partially mitigated by using step assembly as necessary or, when possible, by turning code compression off.

User Module Errata

1. ADCINCVR iGetData API can result in data skewing if interrupt occurs in between LSB and MSB handling. The work around is to set the flag to check for mismatched data in between LSB and MSB.
2. The new ADCINC User Module will be changed slightly with the first 4.2 Service Pack expected to be released within two months of the PSoC Designer 4.2 release. The GetSample(n) API function, which currently accepts a parameter specifying the number of samples to be gathered, will be changed so that it ignores this parameter and will simply start continuous sampling. A new function called StartADC will perform the same function and become the recommended method of enabling this functionality.

For assistance go to http://www.cypress.com or contact our Application Support Team at 425.787.4814.

Silicon Errata CY8C25xxx/CY8C26xxx or CY8C22/24/27/29xxx

The most up-to-date versions of the silicon errata are available on the web site by following the link and navigating to Software & Drivers >> Errata Update (tab) >> Embedded Processors and Controllers >> PSoC Mixed-Signal Array at http://www.cypress.com.

Cypress MicroSystems, Inc.
2700 162nd Street SW, Building D
Lynnwood, WA 98037
Phone: 425.787.4400
Fax: 425.787.4641
Application Support Hotline: 425.787.4814
http://www.cypress.com/ / http://www.cypress.com/support/mysupport.cfm
Copyright © 2004 Cypress MicroSystems, Inc. All rights reserved.
PSoC™, Programmable System-on-Chip™, and PSoC Designer™ are trademarks of Cypress MicroSystems, Inc.
All other trademarks or registered trademarks referenced herein are the property of their respective owners.
The information contained herein is subject to change without notice. Made in the U.S.A.