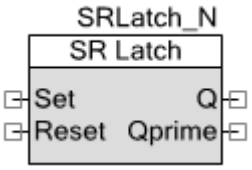
Set-Reset Latch

PA_SRLatch v1.0 **porcine_aviator**

Features



- Implemented with NOR gates
- Asynchronous implementation

General Description

This component is implemented using cross coupled NOR gates present in the PLD logic of the UDB. That results in circuit that changes its output based on a change to either input (S or R) without the use of a clock.

Note: The PSoC architecture is designed to work in a clocked synchronous manner. The architecture can implement an asynchronous component, but this methodology should be avoided and special care must be taken using these outputs. The Static Timing Analysis tool cannot evaluate an asynchronous circuit and will generate a warning when this component is used:

```
Warning: sta.M0019: SR Latch Example.rpt: Warning-1361: The design contains a
combinational loop. Check the design for unintentional latches. Breaking the loop at
Net_14/q --> Net_14/main_0
```

Pin Description

Pin	Type	Function
Set	Input	Set
Reset	Input	Reset
Q	Output	Latch state
Qprime	Output	Inverted latch state

Function Table

Inputs		State		Output	
Set	Reset	Q	Next Q	Q	Qprime
0	0	0	0	0	1
0	0	1	1	1	0
1	0	X	1	1	0
0	1	X	0	0	1
1	1	0	X*	0	1

* This is an invalid condition with an indeterminate next state.

Support

PSoC Creator Community Components are developed and supported by the Cypress Developer Community. Go to www.cypress.com/CommunityComponents to discuss this and other Community Components.