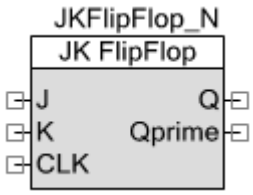
JK Flip Flop (Master-Slave Latch Implementation)

PA_JKFlipFlop v1.0 **porcine_aviator**

Features



- Master-Slave NAND gate latch implementation
- Inputs active while the clock is high
- Outputs change on the falling edge of the clock

General Description

This component is implemented using cross coupled NAND gates present in the PLD logic of the UDB. The master / slave implementation changes the master state while the clock is high. That state is transferred to the slave on the falling edge of the clock and the results then propagated to the outputs. The JK inputs must be held stable at the falling edge of the clock.

Note: Dedicated flip flops should normally be used instead of this component. The PSoC architecture is designed to work in a clocked synchronous manner. The clock for this component is used as a data signal to the NAND gates instead of using the clock tree fed to the dedicated flip flops. The architecture can implement this component, but this methodology should be avoided and special care must be taken using these outputs and the routed clock input. The Static Timing Analysis tool cannot evaluate an asynchronous circuit and will generate a warning when this component is used:

```
Warning: sta.M0019: JK Flip Flip Example.rpt: Warning-1361: The design contains a
combinational loop. Check the design for unintentional latches. Breaking the loop at
\JKFlipFlop_1:b1\/main_2 --> \JKFlipFlop_1:b1\/q
```

Pin Description

Pin	Type	Function
J	Input	J (Set)
K	Input	K (Reset)
CLK	Input	Clock
Q	Output	Latch state
Qprime	Output	Inverted latch state

Function Table

Inputs			Output	
J	**K**	**CLK**	**Q**	**Qprime**
X	X	0	Q_0	$\sim Q_0$
0	0	▼	Q_0	$\sim Q_0$
1	0	▼	1	0
0	1	▼	0	1
1	1	▼	$\sim Q_0$	Q_0

Support

PSoC Creator Community Components are developed and supported by the Cypress Developer Community. Go to www.cypress.com/CommunityComponents to discuss this and other Community Components.