AN76474

PSoC® 3 Power Supervisor

Author: Jason Konstas
Associated Project: Yes (*.hex)
Associated Part Family: PSoC® 3
Software Version: N/A

AN76474 demonstrates how you can quickly implement and customize a full-featured power supervisor that supports up to 13 power supply rails with Cypress's PSoC® 3.

Contents

1 Introduction

Power supervision plays a critical role in modern communications systems such as routers, switches, storage systems, servers and base stations. These systems require multiple power supply rails for their various components including ASICs, PHY devices, FPGAs, CPUs, memory modules, and peripheral I/O devices. Cypress's PSoC® 3 Power Supervisor controls and monitors all of these rails and provides critical system functions:

- Voltage sequencing
- Over-voltage (OV) and under-voltage (UV) fault detection using a high-speed window comparator
- ADC-based power converter output voltage and load current measurements
- Trimming
- Margining
- Data reporting over the Power Management Bus (PMBus™) host interface

Voltage sequencing with tightly controlled timing ensures that costly ASICs and high-density FPGAs safely and reliably come out of reset and have time to be configured and initialized before subsequent devices are powered up.

OV and UV faults can result in partial or full system shutdown. The power supervisor can automatically attempt to bring a failed system back up to operational mode in case the failure was due to a transient event, minimizing system down-time.

Real time power converter output voltage and load current measurements provide power consumption data down to the individual power converter level. This enables system designers to optimize the power ratings for each power converter in order to minimize cost and size. It also enables designers to minimize power consumption through carefully orchestrated power management algorithms. The end result is more energy-efficient system.

Trimming the output voltage of each power converter ensures that high-performance ASICs get the optimal power supply voltage for their current task. Trimming also gives designers the flexibility to change converter output voltages at any time during the life of the product without redesigning the power circuits. This is useful when removable components such as memory modules are upgraded and require lower operating voltages.

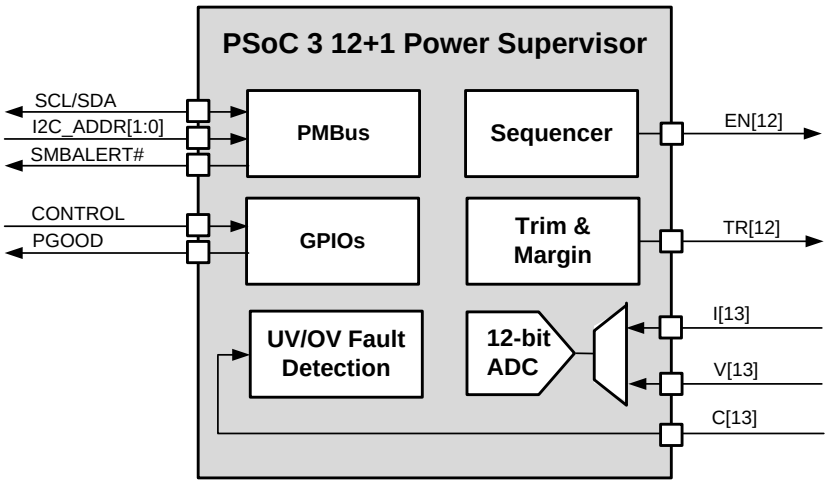
Margining sets the power converter's output to its maximum rating followed by its minimum rating to ensure that the system functions properly across the entire specified voltage range. Margining is used for system qualification and manufacturing test and is not part of normal system operation.

Cypress's PSoC 3 Power Supervisor reports data to the system supervisor and management software stack over the industry standard PMBus host interface. The same interface enables maintenance personnel or system software designers to change the operational parameters of the power supervisor in real-time.

Non-volatile EEPROM fault/event logging records system data such as the total number of operational hours, maximum temperature and its duration, maximum voltage/current recorded on each rail and the nature of a failure (OV, UV or OC). The power supervisor logs the location and type for all faults. This information provides a record of the events leading up to a system shutdown for failure analysis purposes similar to that of a black-box, or flight-recorder. The PSoC 3 Power Supervisor solution does not currently include EEPROM fault logging capability, but this will be added in a future release. If you require this feature for your system, please contact your local Cypress sales representative for support.

This application note describes how Cypress's PSoC 3 can be configured to meet your most demanding power supervisor needs. Throughout this document you will find exercises on real hardware designed to help you gain a better understanding of the fundamental concepts of power supervisor design. Figure 1 shows the PSoC 3 when configured as a full-featured power supervisor.

Figure 1: PSoC 3 Power Supervisor Block Diagram



2 PSoC 3 Power Supervisor Solutions

Two versions of the PSoC 3 Power Supervisor solution are provided with this application note:

1. Evaluation version
2. Production version

You can configure and interact with the prototype solution without having to write any firmware or become familiar with the PSoC Creator™ integrated design environment. This means that you can quickly evaluate Cypress's Power Supervisor solution with near-zero learning curve. Designers who want to develop a fully customized power supervisor or add their own intellectual property should contact their local Cypress sales representative for support.

Note In power supervisor terminology: an "N+1" power supervisor solution includes "N" power converters and one, "+1", primary power source. The power supervisor can monitor and control the power converters; however, it can only monitor the primary power source. The solutions in this application note include a 4+1 power supervisor and a 12+1 power supervisor.

2.1 Evaluation Version

To evaluate Cypress's Power Supervisor solution you will need one of the following sets of hardware and software:

2.1.1 Option 1

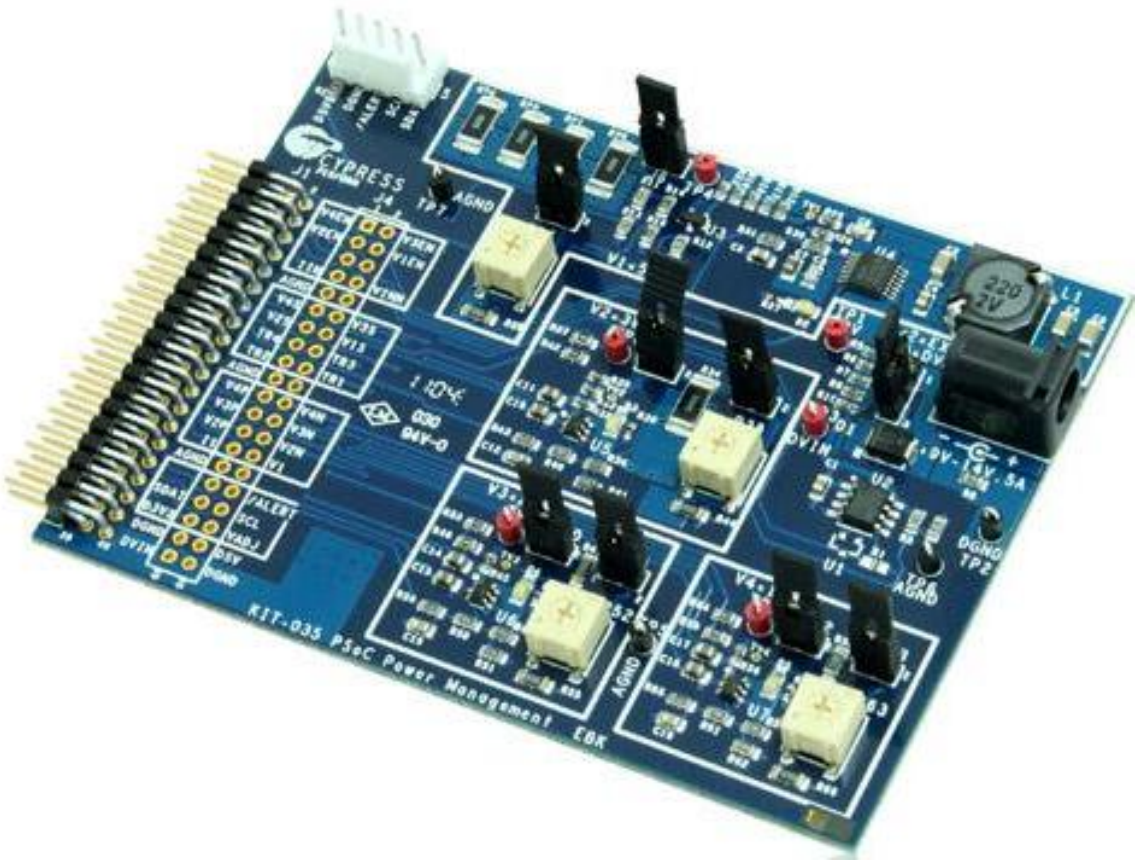
1. PSoC Power Management EBK (CY8CKIT-035)
2. PSoC Development Kit (CY8CKIT-001)
3. MiniProg3 Programming Software

2.1.2 Option 2

1. PSoC Power Management EBK (CY8CKIT-035)
2. PSoC 3 Development Kit (CY8CKIT-030)
3. MiniProg3 Programmer (CY8CKIT-002)
4. MiniProg3 Programming Software

The *PwrSpvr035_001.hex* and *PwrSpvr035_030.hex* programming files are targeted to the CY8C3866AXI-040 PSoC 3 device in the 100 pin TQFP package and are intended for use with the CY8CKIT-035 PSoC Power Management Expansion Board Kit (EBK) shown in Figure 2.

Figure 2: CY8CKIT-035 PSoC Power Management Expansion Board Kit (EBK)



The Power Management EBK includes four DC-DC power converters so you can quickly prototype a complete power supervisor system. It is important to know that the EBK does not have a PSoC device on it. It is designed to be plugged into either the CY8CKIT-001 PSoC Development Kit (DVK) or the CY8CKIT-030 PSoC 3 Development Kit (DVK).

Whichever DVK you use, please make sure it is set to V_{DD} = 5 V operation. The power supervisor can run from a 3.3 V power source, however, the exercises in this application note are designed for 5 V.

2.2 Production Version

The *PwrSpvr.hex* file is targeted to the CY8C3666AXI-036 PSoC 3 device in the 100-pin TQFP package and is intended for designers who are ready to include the PSoC 3 Power Supervisor solution in their custom PCB design. Appendix A includes the PSoC pin out, schematic recommendations, and the performance parameters for the power supervisor solution.

3 Setting-Up the Equipment

The PSoC Power Management EBK Quick Start Guide explains how to configure and prepare it for first use. Please follow the instructions in that guide to set up the Power Management EBK with the particular PSoC DVK you are using.

If you don't have the Power Management EBK, you can build your own power converter system using the prototyping area on one of the PSoC DVKs or by making your own expansion board. However, it will be much easier to follow along with the hands-on exercises if you use the Power Management EBK.

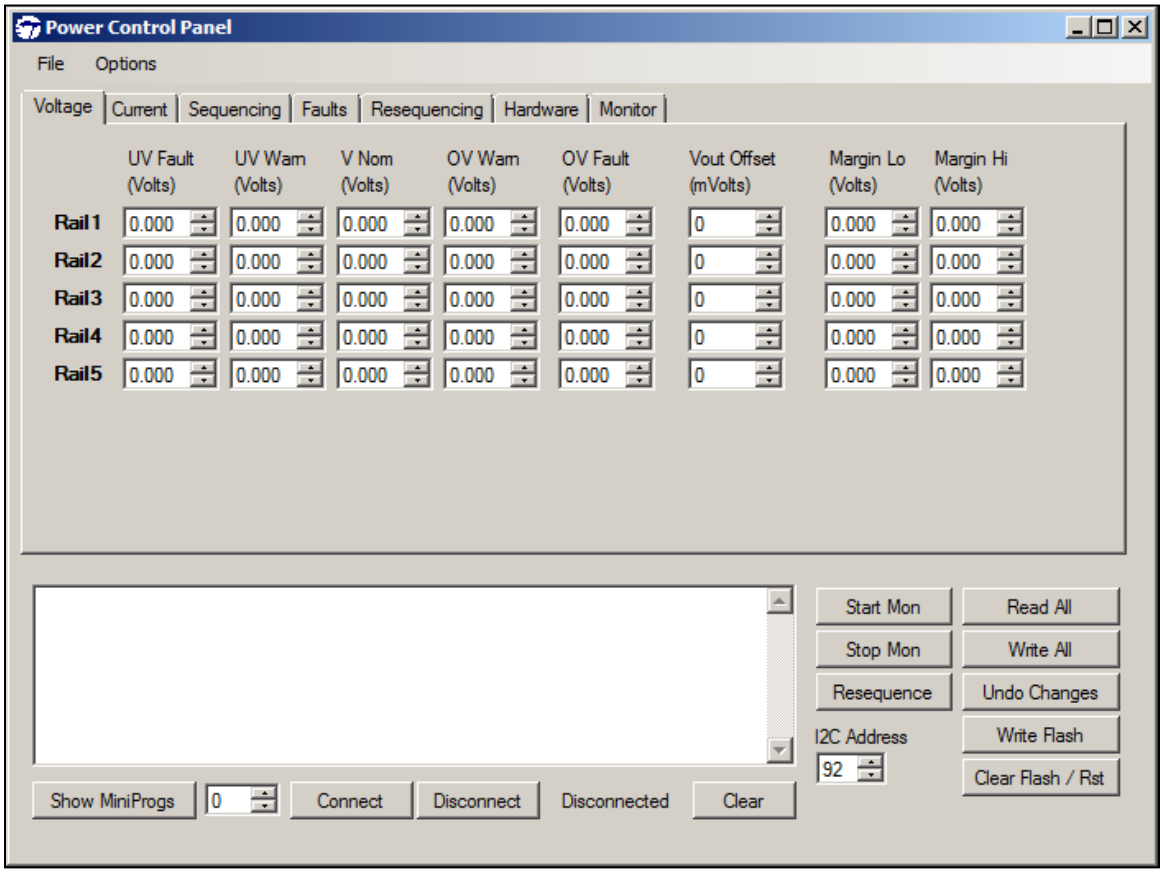
To prepare the hardware for use with this application note, program your PSoC DVK with one of the provided programming hex files:

- *PwrSpvr035_001.hex* is for CY8CKIT-001
- *PwrSpvr035_030.hex* is for CY8CKIT-030

The next step is to run the PMBus **Power Control Panel** software that is provided with this application note. Copy the two files to a convenient location on your hard drive. Run *PowerControlPanel.exe* or create a shortcut to it for future use. Figure 3 shows what the **Power Control Panel** should look like when first launched.

Note The purpose of the **Power Control Panel** software is to enable readers of this application note to gain hands-on experience with the PSoC 3 Power Supervisor solutions provided. It is provided as-is and has not been exhaustively tested on all operating systems. If you experience any problems getting it to run properly on your computer, please contact your local Cypress sales representative for assistance. A production quality PMBus configuration and debug GUI is planned for the 2H-2012.

Figure 3: PMBus Power Control Panel



The **Power Control Panel** can be configured to support either the 4+1 solution or the 12+1 solution. This can be selected through the pull-down menu at the top: **Options → Select Rail Count** and then choosing the appropriate option. For the hands-on exercises presented in this application note, select **4+1 Rails**.

The **Power Control Panel** communicates with the PSoC hardware over I^2C using the MiniProg3 programmer:

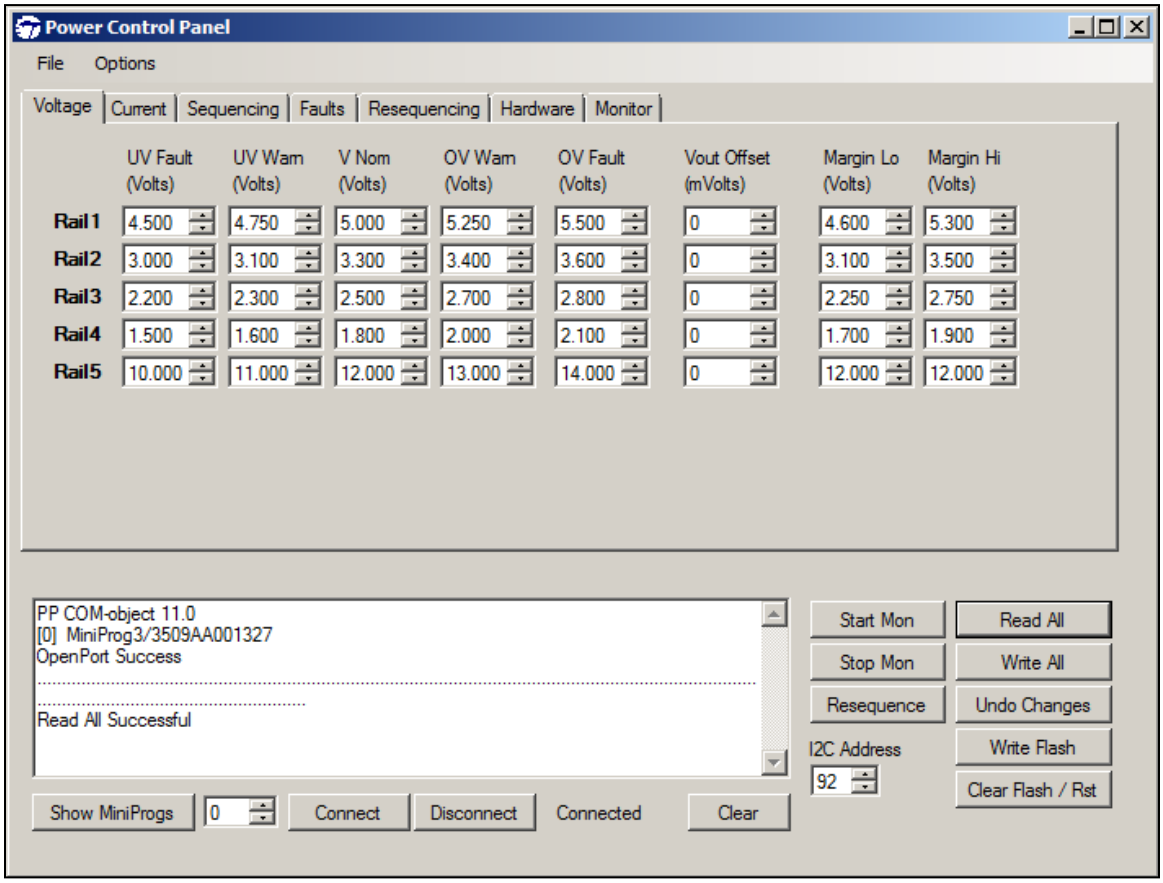
1. Connect the MiniProg3 to your computer's USB port and ensure that the MiniProg3 has been properly recognized by your computer. If it has, the green LED inside the MiniProg3 should be turned on.
2. Attach the 5-pin white connector of the MiniProg3 to the 5-pin white header mounted on the PSoC Power Management EBK.
3. Click on the **Find MiniProgs** button in the bottom left corner of the **Power Control Panel** GUI. If this is successful, the MiniProg3 and its serial number will be displayed in the status window.

4. If you have multiple MiniProg3 programmers connected to your computer, use the numeric selector right next to the **Find MiniProgs** button to select the instance you would like the **Power Control Panel** to use.
5. Click on the **Connect** button and you should see the message **OpenPort Success** displayed if the connection has been properly made.

Troubleshooting Since the MiniProg3 is also used for programming PSoC, make sure that you have closed the PSoC Programmer software tool to release the MiniProg3 device driver for use by the **Power Control Panel**.

When you have established a connection to the MiniProg3, click on the **Read All** button to load the default configuration parameters stored in the 4+1 PSoC 3 Power Supervisor solution. This will save you a significant amount of time as the solution has already been configured to work with the hardware components on PSoC Power Management EBK. The **Power Control Panel** should now look like Figure 4.

Figure 4: Successful Read of PSoC Parameters



Troubleshooting If you are unable to successfully read from the PSoC, check the I^2C address. The Power Management EBK can be set to one of four I^2C slave address using the two I^2C Address select pins (Table 1).

Table 1: I^2C Slave Base Address Settings

I2C ADDR 1	I2C ADDR 0	7-bit I^2C Address	
		Hexadecimal	Decimal
High	High	0x5C	92
High	Low	0x5D	93
Low	High	0x5E	94
Low	Low	0x5F	95

The address select pins are internally pulled high. Leaving the pins open will set the 7-bit I^2C base address to 0x5C (hexadecimal) or 92 (decimal). If you connect the address select pins to one of the non-default options, you must set the corresponding address in the **Power Control Panel** using the **I2C Address** parameter found on the bottom of the status window on the right-side (see Figure 3). Enter the base address in decimal.

The nominal voltages for the power converters on the PSoC Power Management EBK are as follows:

Rail 1: V1 = 5 V

Rail 2: V2 = 3.3 V

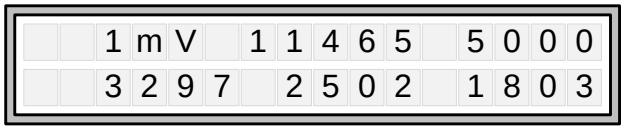
Rail 3: V3 = 2.5 V

Rail 4: V4 = 1.8 V

Rail 5: V5 = 12 V

The LCD on the PSoC DVK should be displaying the five power converter output voltages as measured by the ADC in units of mV. An example of what you should be seeing is shown in Figure 5

Figure 5: Debug LCD Display on the PSoC DVK



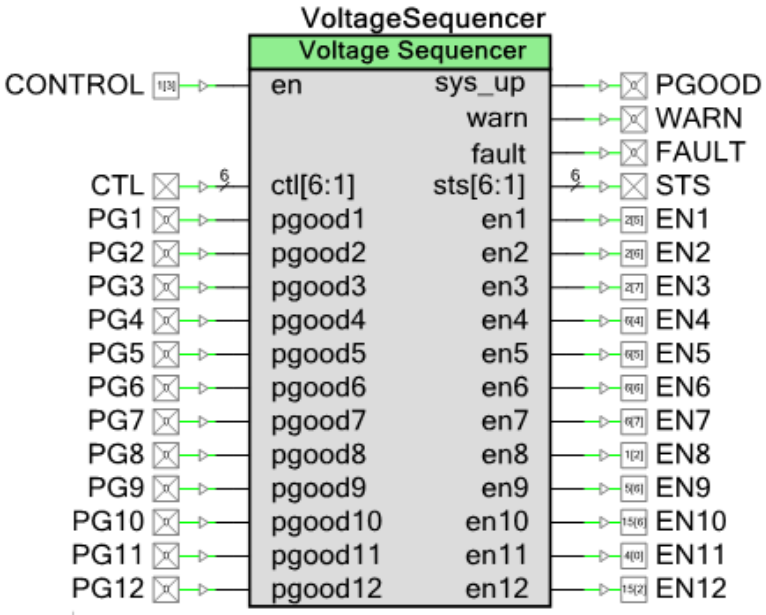
The LCD displays the measured voltage of the AC-DC adaptor powering your hardware (the “+1” primary input power source), followed by the voltages measured from each of the power converters on the Power Management EBK.

Now that you have the system properly set up and running, we can begin the hands-on exercises.

4 Section 1 – Voltage Sequencing

The first task for the PSoC 3 Power Supervisor is to turn the power converters on. You can specify the order in which the rails come up, including the ability to bring up multiple rails in parallel. The timing of turning the rails on can be specified in relative or absolute terms, depending on your requirements.

Figure 6: Voltage Sequencer Block Diagram



The voltage sequencer block inside PSoC, shown in Figure 9, is responsible for generating the power converter enable (EN) signals and for monitoring the health of the power converter voltage rails through power good (PG) inputs. How the PSoC generates the PG signals will be explained in a later section, for the discussions in this section, just think of the PG inputs as logic level signals, where a logic high level means that the associated rail is good.

Three voltage sequencer status flags are available. The active-high WARN and FAULT output pins are used to signal that a warning or fault condition has occurred. Potential sources for these conditions will be presented as we go through the hands-on exercises. The PGOOD output reflects the overall health of the power system in its entirety. If all of the rails are good PGOOD is high.

The voltage sequencer also provides some general purpose I/Os that are not related to the power converter circuits. The CONTROL pin is an optional PMBus feature and can be used as the global enable control input for the voltage sequencer. This gives the PMBus system host a hardware mechanism to start and stop the voltage sequencer. This is extremely useful if the PMBus communication link goes down.

In most systems, voltage sequencing should not begin until other key components of the system are operational. Some examples include waiting for the system fans to spin up to nominal speed or waiting for the primary system power supply to ramp up and become stable. The Sequencer Control (CTL) inputs allow you to control when voltage sequencing begins. The Sequencer Status (STS) outputs track the progress of the voltage sequencer as each rail, or group of rails, comes up. An example of how to use the STS outputs would be to release the reset on an ASIC or FPGA once its power system is up and running. In the power supervisor solutions provided with this application note, the CTL inputs and STS outputs are not routed to external PSoC pins and the STS outputs are not used. However, you will use the **Power Control Panel** to drive the CTL inputs. This can be very useful for single-stepping through your sequencer design during development and debug.

Before we begin exploring the sequencing capabilities of the PSoC 3 Power Supervisor, let's get familiar with the power converters that are on the PSoC Power Management EBK.

Figure 7: PSoC Power Management EBK Power Converter Hierarchy

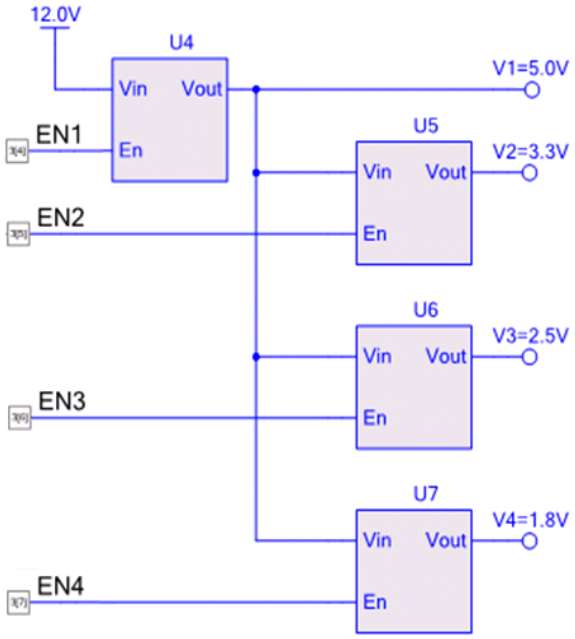


Figure 7 shows the power converter hierarchy that exists on that board. The four enable signals (EN1—EN4**)** are outputs from the voltage sequencer block inside PSoC and are used to turn each power converter on or off. The 12 V primary input power source (the "+1" rail) powers U4 which in turn generates the V1 = 5 V power rail. The remaining power rails, V2—V4, are powered from the output of U4.

Keep in mind that turning off V1 will turn off all the other rails. For example, if you attempt to configure the voltage sequencer to turn on V2 before V1, it will not be possible.

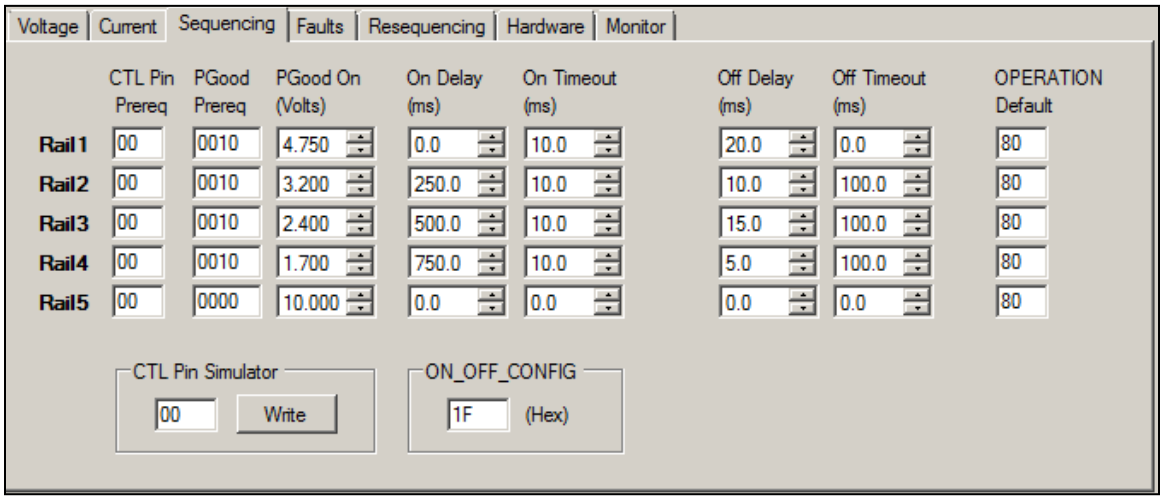
Let's start with a very simple power-on sequence to become familiar with the voltage sequencer control parameters.

4.1 Exercise 1 – Absolute Time Based Power Up Sequencing

Let's begin by simply turning on all four rails one at a time in forward order (Rail 1 → Rail 2 → Rail 3 → Rail 4) with a 250 ms delay between them.

Click on the **Sequencing** tab of the **Power Control Panel** to gain access to the sequencer controls. This tab enables you to specify how the sequencer should power up and power down the rails under normal circumstances (no faults detected). How to respond to fault conditions will be discussed later. Figure 8 shows the parameters.

Figure 8: PMBus Power Control Panel – Sequencing Tab



At first glance, there appears to be an overwhelming amount of data shown on this screen, however, every row is independent from the others. The voltage sequencer is implemented using independent state machines for each rail. Let's discuss each of the parameters as you look across a single row in the **Sequencing** tab:

4.1.1 Ctl Pin Prereq

This parameter defines which control pins (CTL1—CTL6) must be set before sequencing starts on the rail. It is a 2-digit hexadecimal number shown in Table 2.

Table 2: Ctl Pin Prereq Parameter Format

Bits 7—6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
–	CTL6	CTL5	CTL4	CTL3	CTL2	CTL1

Setting a bit in the parameter field configures the associated CTL pin as a pre-requisite to sequencing for the associated rail. Multiple bits can be set simultaneously. In that case, all selected CTL input pins need to be true (active high) before sequencing can begin.

The **Ctrl Pin Simulator** parameter on the **Sequencing** tab enables you to set or clear any of the CTL pins that are internally wired to the voltage sequencer. To take advantage of this feature, add a CTL pin pre-requisite to any of the rails. Sequencing will not begin on that rail until you manually assert the CTL bit through the **Power Control Panel**. The **Ctl Pin Simulator** parameter is a 6-bit field with the same format as **Ctl Pin Prereq**.

4.1.2 PGood Prereq

Since the state machine that drives the EN pin for each power converter is independent, there needs to be a mechanism to synchronize them. This is particularly important when you want a rail to turn on only when a previously enabled rail has reached nominal voltage and is stable, indicated by a logic high level on its PG pin. This is function of the **PGood Prereq** parameter.

This parameter is a 4-digit hexadecimal number in order to support up to 16 rails. For the 4+1 solution only five of the bits are used. The format is shown in Table 3.

Note PG5 represents the status of the +12 V primary input power source (the "+1" rail).

Table 3: PGood Prereq Parameter Format

Bits 15—5	Bit4	Bit3	Bit2	Bit1	Bit0
–	PG5	PG4	PG3	PG2	PG1

Just like CTL pin pre-requisites, setting a bit in the parameter field will configure the associated PG pin as a pre-requisite to sequencing for the associated rail. Multiple pins can be set simultaneously. In that case, all selected PG pins must be true.

4.1.3 PGood Volts

This parameter enables you to define the minimum threshold (in Volts) that the rail needs to reach before it is good. This threshold applies only when the power converter is powering up and should be set higher than the UV fault threshold used for normal operation. This provides some hysteresis in the PG qualification circuit which is useful for power converters that have a slow rise time due to heavy loading. This is particularly important when glitch filtering is disabled in the window comparator circuit that determines PG. We will cover this in more detail in a later section.

4.1.4 On Delay and On Timeout

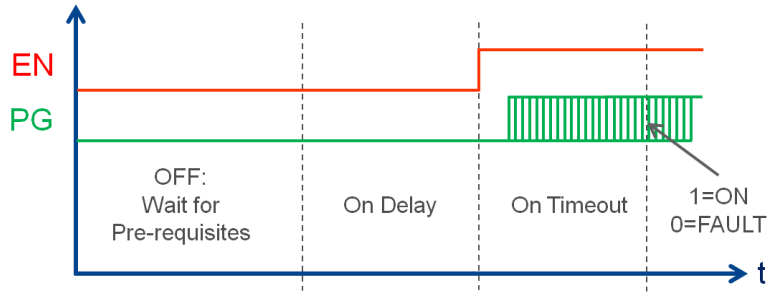
Every rail has two timing parameters associated with powering up.

The **On Delay** parameter specifies how much time to wait after the rail's pre-requisite conditions (CTL and PG) become true before enabling the power converter by asserting its EN signal. Using different **On Delay** settings for different rails makes user-defined sequencing possible.

The **On Timeout** parameter specifies the acceptable time limit for the power converter to ramp up to nominal voltage after it is enabled. The ramp up time is defined as the time between EN being asserted and PG becoming true. If the ramp up time exceeds the **On Timeout** parameter, a fault occurs. The user can specify what should happen in response to the fault. We will cover fault response handling in one of the later exercises in this section.

Figure 9 shows the relationship of the power up sequencing delay parameters to the EN and PG signals for a single rail.

Figure 9: Power Up Sequencing Delay Parameters



OPERATION Default and **ON_OFF Config** are discussed in Exercise 5.

Now that we've discussed the parameters on the **Sequencing** tab, let's set the parameters necessary to turn on all four rails one at a time in forward order (Rail 1 → Rail 2 → Rail 3 → Rail 4) with a 250 ms delay between them.

For the first hands-on exercise:

1. Clear all bits of the **Ctl Pin Prereq** parameters
2. Make sure that the +12 V primary power source, Rail 5, is good before turning on any other rails by setting the **PGood Prereq** to 0x0010 for all rails
3. Leave the default **PGood Volts** and **On Timeout** settings since they have been selected to be compatible with the Power Management EBK

To get the desired time delay between the rails, set the **On Delay** parameters as shown in Table 4.

Table 4: On Delay Parameter Settings for Exercise 1

Rail #	On Delay	Comment
1	0	Turn on as soon as Rail 5 is good
2	250 ms	Turn on 250 ms after Rail 5 is good
3	500 ms	Turn on 500 ms after Rail 5 is good
4	750 ms	Turn on 750 ms after Rail 5 is good
5	0	Cannot be sequenced

When you make any parameter changes in the **Power Control Panel**, you will notice that the cells turn green. This indicates that the parameter changes have not yet been sent to the PSoC. Clicking on the **Write All** button will send the new parameters to the PSoC's volatile memory and take immediate effect, but the changes will be lost when power is removed. To make the parameter changes permanent, click on the **Write All** button first and then click on the **Write Flash** button. If you have entered all the parameters correctly, the sequencing tab parameters should be the same as those shown Figure 8.

To try out this configuration, click on the **Resequence** button. This will power all the rails down. Click on it again to power all the rails back up. The green LEDs on the Power Management EBK are connected to the power converters' EN signals allowing you to see the sequencing in action. You can also attach logic analyzer or oscilloscope probes to the test point array (J4) on the Power Management EBK to measure the actual delays between the EN signals. The relevant signals are labeled V1EN—V4EN on the EBK. You can repeat this as many times as necessary until you confirm the power up sequence is operating properly.

You can power up Rails 2—4 in any order by changing the **On Delay** parameters. Feel free to do your own experiments. A quick reminder that Rail 1 provides power to Rails 2—4, so be sure it always turns on first.

4.2 Exercise 2 – Relative Time Based Power Up Sequencing

In Exercise 1 we did not take into account the possibility that one of the rails might not come up properly during the sequence. To do this, you need to add PG prerequisites for Rails 2—4 using the **PGood Prereq** parameter as shown in Table 5.

Table 5: PGood Prereq Parameter Settings for Exercise 2

Rail #	PGood Prereq	Comment
1	0010	Wait for Rail 5 to be good
2	0011	Wait for Rail 1 and Rail 5 to be good
3	0013	Wait for Rail 1, Rail 2, and Rail 5 to be good
4	0017	Wait for Rail 1, Rail 2, Rail 3, and Rail 5 to be good
5	0000	Cannot be sequenced

Now that each rail waits for the previous rail to be good, the **On Delay** parameters are no longer absolute time delays referenced to Rail 5's PG being asserted. Instead, the **On Delay** parameters are relative to the previous rail powering on. Therefore, the **On Delay** parameters for Rails 2—4 should all be set to 250 ms.

When you're ready, try out these new settings by clicking on the **Write All** button and then on the **Resequence** button twice to bring the system back up. If everything worked as expected, the sequencing behavior should look similar to Exercise 1. The timing will be a little different due to small additional delays introduced by waiting for each rail to ramp up and become good.

Using these voltage sequence settings, if any of the rails fail to come up, subsequent rails will not be turned on. This is an important feature designed to protect ICs. Many ICs have strict requirements for the order in which power supplies come up in order to ensure they come out of reset properly and are not damaged.

You can use a combination of the methods demonstrated in Exercises 1 and 2 depending of the specific requirements and design objectives of your application. For example, using the following settings would achieve the same sequencing result as the two previous exercises provided all rails come up successfully:

- Rail 3 and Rail 4 **PGood Prereq** set to wait for Rail 2 to be good
- Rail 3 **On Delay** set to 250 ms
- Rail 4 **On Delay** set to 500 ms

4.3 Exercise 3 – Power Down Sequencing

In the previous exercises we used the **Resequence** button to force all rails to power down. While it may appear that all of the rails power down at the same time, the power down sequencing time delays are so short that it is difficult to perceive them. For this exercise we will extend the delays so they are easily visible on the green LEDs on the Power Management EBK.

For this exercise, change the **Off Delay** parameters such that the rails turn off in the reverse order that they were turned on (Rail 4 → Rail 3 → Rail 2 → Rail 1) with a 250 ms delay between them. This can be achieved by entering different delays in the **Off Delay** parameters for each rail as shown in Table 6.

Table 6: Off Delay Parameter Settings for Exercise 3

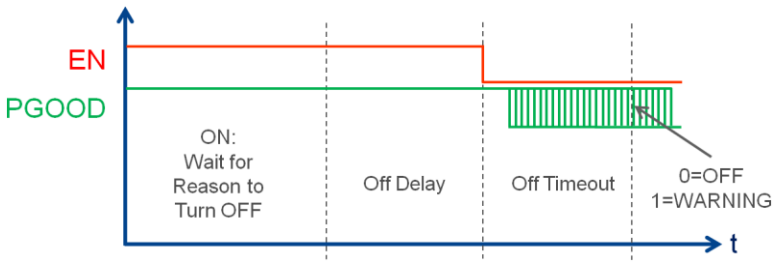
Rail #	Off Delay	Comment
1	750 ms	Turn off last, 750 ms after Rail 4
2	500 ms	Turn off 500 ms after Rail 4
3	250 ms	Turn off 250 ms after Rail 4
4	0	Turn off first
5	0	Cannot be sequenced

Try it out and make sure it works the way you expect it to. Once again, feel free to experiment with the Off Delay settings, but remember to turn Rail 1 off last since it provides power to Rails 2—4.

The **Off Timeout** parameter specifies the acceptable time limit for the power converter to ramp down after it is disabled. This is useful for applications that need to ensure that the rail powers down before taking further action. The ramp down time is defined as the time between EN being de-asserted and the rail voltage decaying to 12.5% of its nominal value. If the ramp down time exceeds the **Off Timeout** parameter, a warning (not a fault) condition occurs that can be signaled to the host through the PMBus Status Registers.

Figure 10 shows the relationship of the power down sequencing delay parameters to the EN and PG signals for a single rail.

Figure 10: Power Down Sequencing Delay Parameters



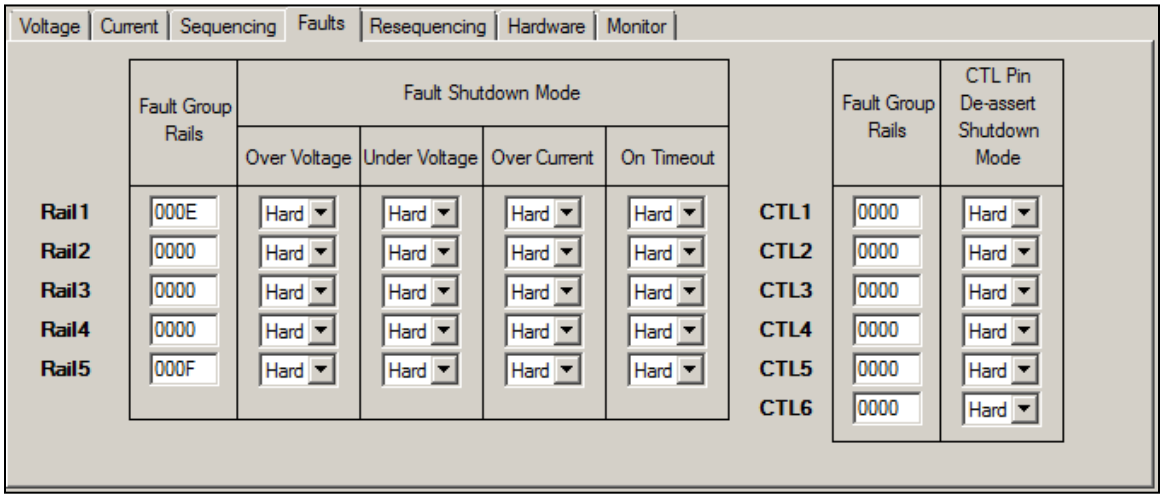
Sequencing down like this is fine when the shutdown is intentional. When a fault condition is detected on one of the rails, taking a long time to shutdown is dangerous because the power converter could be experiencing a short circuit condition on its output due to an IC failure. If the converter is capable of sourcing a large amount of current, this could cause permanent damage to the board and in an extreme case, result in fire. In the next exercise, we'll take a look at how to configure the voltage sequencer to respond appropriately to fault conditions.

4.4 Exercise 4 – Fault Responses

For the safety reasons mentioned in Exercise 3, the voltage sequencer in the PSoC 3 Power Supervisor always immediately turns off a rail when a fault condition is detected on it. This is implemented entirely in hardware inside PSoC (no firmware intervention required) with a worst case response time of 25 ns. The three possible fault sources are over-voltage (OV), under-voltage (UV) and over-current (OC).

Although shutting down of the faulty rail is done by the hardware, the voltage sequencer allows you to take additional actions in response to the fault. Go to the **Faults** tab to configure those additional actions.

Figure 11: PMBus Power Control Panel – Faults Tab



Before we discuss the details of each parameter, the concept of a **Fault Group** needs to be introduced. In many designs multiple rails power a single IC or a sub-system of ICs. Therefore, if one rail powers down due to a fault, some or all of the other rails should also be powered down. To achieve this, the rails can be defined as a group. On the **Faults** tab, the parameter called **Fault Group** allows you to specify which good rails belong to the same group as the faulty rail and should also be powered down.

The **Fault Group** parameter is a 4-digit hexadecimal number that supports up to 16 rails shown in Table 7.

Table 7: Fault Group Parameter Format

Bits 15—5	Bit4	Bit3	Bit2	Bit1	Bit0
–	Rail 5	Rail 4	Rail 3	Rail 2	Rail 1

Setting a bit in this parameter means that the corresponding rail is in the same group as the rail labeled to the left of the current row and will be shut down when a fault is detected on that rail.

For this exercise, let's configure the voltage sequencer such that any fault on any rail, will shut down all the other rails in same the group. To make that happen, set the **Fault Group** parameters as shown in Table 8.

Table 8: Fault Group Parameter Settings for Exercise 4

Rail #	Fault Group	Comment
1	000E	Shutdown Rail 2, Rail 3, and Rail 4 if Rail 1 faults Note This will occur no matter what value we enter since Rail 1 powers Rails 2— 4
2	000D	Shutdown Rail 1, Rail 3, and Rail 4 if Rail 2 faults
3	000B	Shutdown Rail1, Rail 2, and Rail 4 if Rail 3 faults
4	0007	Shutdown Rail 1, Rail 2, and Rail 3 if Rail 4 faults
5	0	Cannot be sequenced

The **Fault Shutdown Mode** parameters define how to shut down the rail groups for each fault type using pull-down menus. The options are:

- **Soft** – turn the good rails in this group off after the delay specified by the **Off Delay** parameter entered on the **Sequencing** tab
- **Hard** – turn the good rails in this group off immediately

The **Soft** option enables you to set a controlled power down sequence (through different **Off Delay** settings on each rail), whereas the **Hard** option just shuts down all rails in the group at the same time.

We already discussed the use of CTL1—CTL6 to gate the start of sequencing on any rail. Once a rail has successfully powered-up and is running, it can be configured to shut down if one or more CTL pins is de-asserted. A de-asserted CTL pin is treated as a fault condition with user-specified response handling.

The **CTL Fault Group** parameter is a 4-digit hexadecimal number that supports up to 16 rails shown in Table 9.

Table 9: CTL Fault Group Parameter Format

Bits 7—5	Bit4	Bit3	Bit2	Bit1	Bit0
–	Rail 5	Rail 4	Rail 3	Rail 2	Rail 1

Setting a bit in the parameter field will configure the CTL input pin as a fault source for the selected rail. Multiple bits can be set simultaneously. In that case, the de-assertion of the CTL pin will generate a fault condition on the selected rails. The **CTL Pin De-Assert Shutdown Mode** parameters define whether to use the **Soft** or **Hard** shutdown modes, as described earlier. Remember that the CTL pins are not routed to external PSoC pins in the PSoC 3 Power Supervisor hex files. However, users can still use this feature to manually force a voltage sequencer shutdown by using the **Ctrl Pin Simulator** on the **Sequencing** tab.

To test the voltage sequencer's fault response capability, we need a way to generate faults on the rails. For this exercise, you have two options:

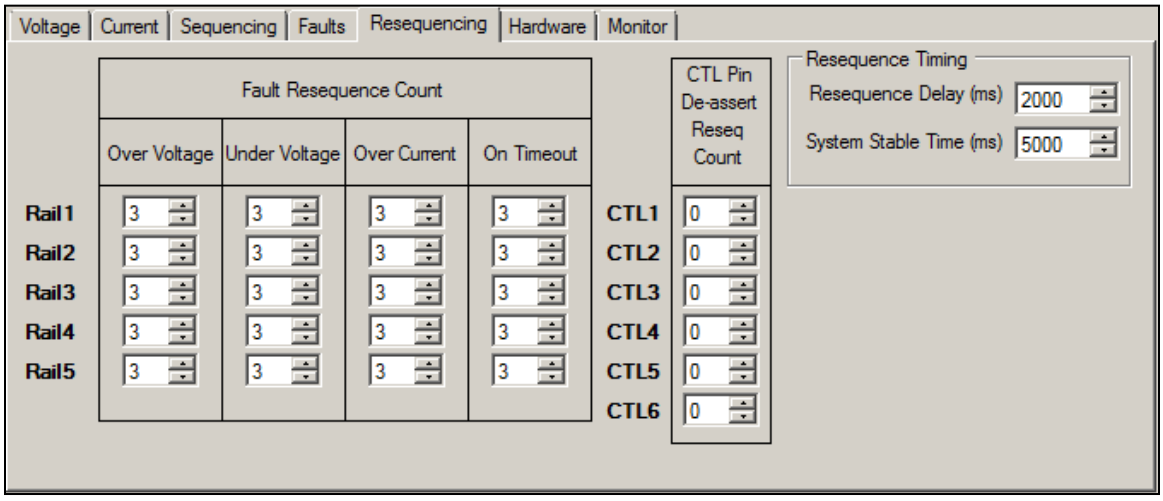
1. You can configure one or more of the CTL pins as fault sources and use the **Ctrl Pin Simulator** to generate faults
2. You can grab a wire and physically short one of the rail outputs to ground on the Power Management EBK. The rail outputs are available on the red colored test points. Connect one end of the wire to one of these test points and the other end to one of the ground test points.

As with the previous exercises, you will learn more about how these features work by experimenting with them. If the rail turns off and stays off, you can bring it back by clicking on the **Resequence** button twice.

4.5 Exercise 5 – Automatic Re-sequencing

In the previous example, you probably noticed that after the rail shuts down, it powers up again automatically. However, if you generate a fault multiple times, the voltage sequencer will eventually give up attempting to retry. Go to the **Resequencing** tab to configure the voltage sequencer's automatic re-sequencing behavior.

Figure 12: PMBus Power Control Panel – Resequencing Tab



The **Fault Resequence Count** defines how the individual rails should respond to each type of fault. The values for automatic re-sequencing are described in Table 10.

Table 10: Re-sequence Count Parameter Format

Value	Comment
0	No automatic re-sequencing. When a fault occurs the rail is shut down and remains off
1—30	Specifies the maximum number of re-sequencing attempts
31	Attempt re-sequencing indefinitely (infinite retries)

If automatic re-sequencing is enabled, the **Resequence Delay** parameter specifies how long to wait before attempting the next power up sequence. This parameter is a global setting and is applied to re-sequencing attempts on any rail.

The **System Stable Time** parameter provides a mechanism to reset the re-sequence counter once the entire power system has been up and running for an extended period of time. The thinking behind this implementation is that when a rail faults, you want to try to bring it back up as specified by the **Reseq Count** parameter. Once the rail is back up and running normally, the history of the previous retries should be cleared in preparation for a future fault. For example, suppose you set the **Reseq Count** to 3 on a rail. The rail faults, but comes back up after the third retry, and resumes normal operation for an extended period of time. If the rail faults again later, it makes sense to give it another chance to recover by giving it three more re-sequence attempts. In other words, the **Reseq Count** should be applied to isolated fault incidents and reset for future faults. The **System Stable Time** parameter allows you to set the definition of "running normally for an extended period of time". The upper limit for this parameter is 262 seconds.

For this exercise, experiment with different settings for **Reseq Count**, **Resequence Delay** and **System Stable Time** until you are confident that you understand the way the parameters work. Remember, if you cause a fault on a rail so many times that you exceed the **Reseq Count** parameter setting, the rail will turn off and stay off. When that happens, click on **Resequence** button twice to bring the system back up.

4.6 PMBus Specific Parameters

Back on the **Sequencing** tab shown in Figure 8, there are two parameters that work together to influence the power on behavior of the voltage sequencer and how it responds to the PMBus **CONTROL** pin and the PMBus **OPERATION** command, **OPERATION Default** and **ON_OFF_CONFIG.**

These two parameters enable you to define when the voltage sequencer begins sequencing. You can specify that sequencing:

- Begin immediately after power on
- Wait for either the PMBus **CONTROL** pin to be asserted or for the PMBus **OPERATION** command.

You can apply these settings globally or independently to each rail for maximum flexibility.

4.6.1 ON_OFF_CONFIG Parameter

You change the global **ON_OFF_CONFIG** default setting by entering the desired 8-bit hexadecimal number in the **ON_OFF_CONFIG** field found on the **Sequencing** tab of the **Power Control Panel**. The default setting for this parameter is 0x1F which means that the voltage sequencer must to wait for either the PMBus **CONTROL** pin to be asserted or for the PMBus **OPERATION** command to begin sequencing. The default setting also specifies that de-asserting the PMBus CONTROL pin will force the voltage sequencer to shutdown all rails. De-asserting the PMBus CONTROL pin is not considered a fault condition, but rather an intentional shutdown. If none of these control methods is required, you should change the **ON_OFF_CONFIG** parameter to 0.

Note The PMBus CONTROL pin on PSoC is connected to an internal pull-up resistor, so if you leave this pin open, the default behavior of the voltage sequencer will be to begin executing the power up sequence immediately after power is applied to PSoC.

Refer to section 12.1 of the PMBus Power System Management Protocol Specification Part II for full details on the functionality and the bit-field format of **ON_OFF_CONFIG**.

IMPORTANT NOTE: If you are planning to use the PSoC 3 Power Supervisor solution on your own board, it is recommended that you set the CONTROL pin low the first time you power-up your board so that the voltage sequencer will stay off until you have a chance to configure the sequencing parameters to match your own power design.

4.6.2 OPERATION Default Parameter

The **OPERATION Default** parameter can be specified for each rail. A setting of 0x80 on all rails means that the rails will be turned on and set to nominal voltage output. Refer to section 12.2 of the PMBus Power System Management Protocol Specification Part II for full details on the functionality and the bit-field format of the **OPERATION** command.

4.7 Voltage Sequencer Summary

The voltage sequencer allows power designers to implement complex sequencing and highly customizable fault response with automatic re-sequencing. To support such a high-level of configurability, the sequencing implementation is firmware based. The one important exception is the high-speed, low-latency rail shutdown in response to a fault condition. Since this is critical for safety, that function is implemented in hardware to guarantee a fixed response time (< 25 ns) under all circumstances.

If the voltage sequencer does not meet your requirements or if you are interested in building your own voltage sequencer, using either firmware or digital logic based on your own custom state machine, please contact your local Cypress sales representative for support.

5 Section 2 – Voltage and Current Measurements

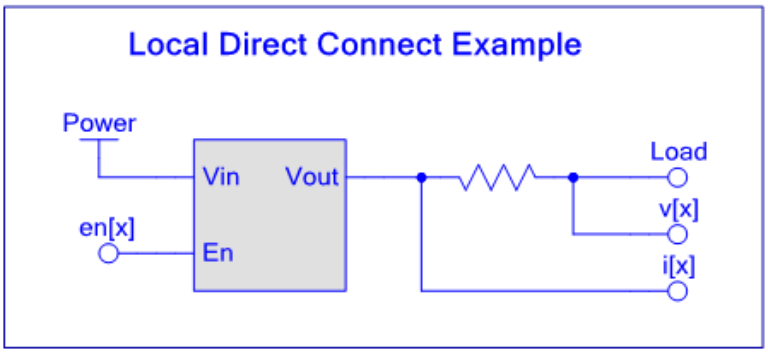
An important function of any power supervisor solution is the ability to measure the output voltage and load current of all the power converters in real-time. This information can be used by the power supervisor locally to generate warnings when the power converters perform outside of their expected nominal range, or the information can be relayed over the PMBus communications interface, to an external management processor that has visibility into the behavior of the broader system.

This section covers system design issues you may encounter when measuring power converter voltages and load currents.

5.1 Measurement Topologies

The PSoC 3 Power Supervisor solutions are capable of performing both voltage and load current measurements on all rails. Voltage measurements are performed using a 12-bit resolution Delta-Sigma ADC configured for a single-ended input voltage range of 0—4.096 V. Load current measurements are performed by measuring the voltage drop across a small series shunt resistor on the power converter output side. The same 12-bit Delta-Sigma ADC is used, but it is re-configured in real-time to support a differential input voltage range of ±64 mV (for the 12+1 solution) or ±128 mV (for the 4+1 solution). For rails that are below 4.096 V, both sides of the series shunt resistor can connect directly to PSoC analog pins as shown in Figure 13.

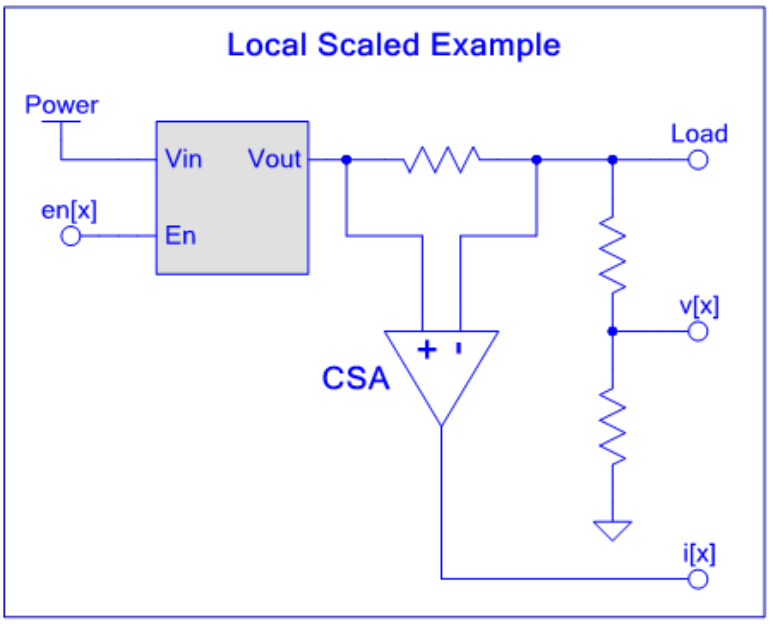
Figure 13: Voltage and Load Current Measurement –Direct Connect Topology



For power rails that are above 4.096 V, scaling is required for the voltage measurements and an external current sense amplifier (CSA) is required for converting the high common mode differential voltage across the sense resistor to a single ended voltage that can be connected to PSoC's analog input pins. This is shown in Figure 14.

Note In Figures 13 and 14, the terminal labeled i[x] represents a voltage. It is labeled i[x] to indicate that the voltage measurement will be translated into a current.

Figure 14: Voltage and Load Current Measurement –Scaled Topology



Both of these measurement topologies are supported by both the 4+1 and 12+1 PSoC 3 Power Supervisor solutions. The first and last rails are configured to support the scaled topology and assume that an external CSA is present for current sensing. All other rails are configured to support the direct connect topology.

PSoC can be configured to support several other measurement topologies including differential voltage measurement (Figure 15 and Figure 16) and power converter input side current measurement (Figure 17 and Figure 18).

Figure 15: Differential Voltage Measurement – Direct Connect Topology

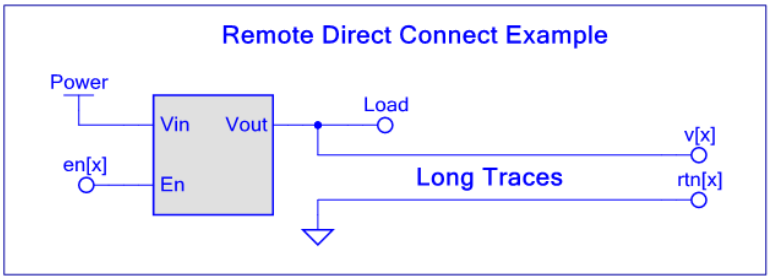


Figure 16: Differential Voltage Measurement – Scaled Topology

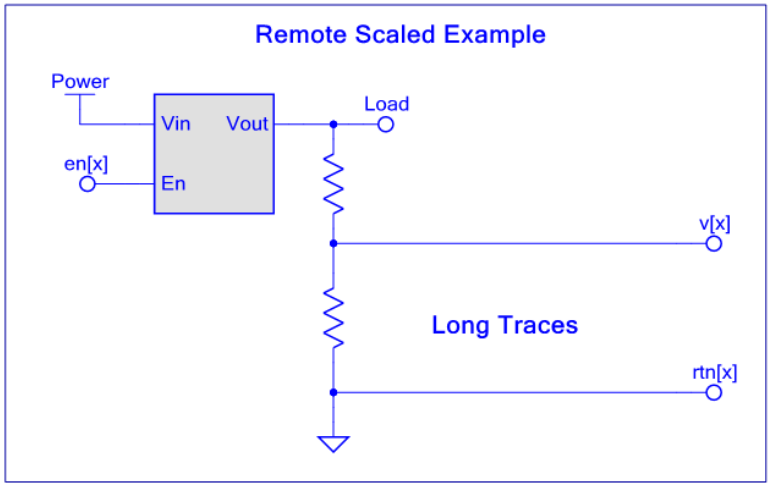


Figure 17: Output Voltage and Input Current Measurement – Direct Connect Topology

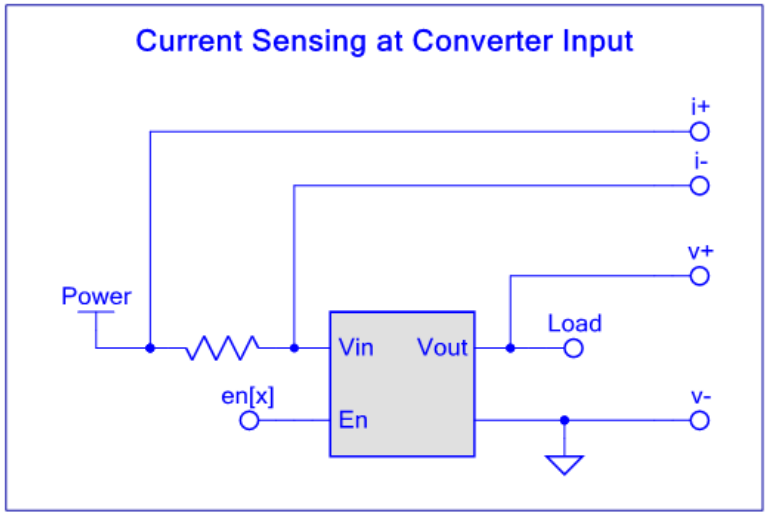
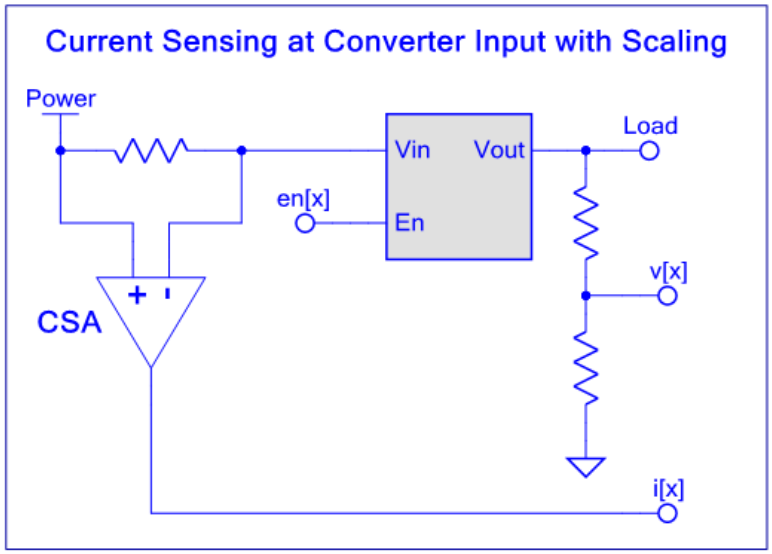


Figure 18: Output Voltage and Input Current Measurement – Scaled Topology



If you are interested in using PSoC to measure power converter voltages and/or currents in any of these alternate configurations, please contact your local Cypress sales representative for more information.

5.2 External Component Selection

The resistors used to scale down higher voltages should have a maximum tolerance of ±0.1% to minimize their impact on voltage measurement accuracy. The ADC is configured for a single ended voltage range of 0—4.096 V. The scaling factor should be designed to attenuate the actual converter output to well within this range during maximum expected over-voltage conditions. The magnitude of the resistors should be in the 10—100 kΩ range. This is high enough to minimize quiescent current draw but low enough such that the input impedance of the ADC input buffer does not impact the measurement.

The series shunt resistor used for current measurements should also have a maximum tolerance of ±0.1% to minimize its impact on current measurement accuracy. The upper bound for the value of the resistor depends entirely on the maximum expected converter load current. Remember that in differential measurement mode, the ADC has a range of ±64 mV (12+1 solution) or ±128 mV (4+1 solution). The maximum load current multiplied by the shunt resistor value cannot exceed the ADC's range. To minimize the power dissipated through the sense resistor, the smallest possible value should be chosen that will generate a voltage of sufficient magnitude to be measured with adequate accuracy. A general rule-of-thumb is to select a resistor that generates a differential voltage (at maximum load current) of around 85% of full-scale ADC range.

There are many low-cost CSAs available on the market. The device that best meets your needs will depend on common mode voltage, accuracy, package size and cost. Some CSA solutions have a built-in calibration capability; some have an embedded ADC dedicated to measuring the current and reporting the result via a digital interface (typically I^2C). This is particularly useful when the power converter is located far from the power supervisor. While this is not supported in the PSoC 3 Power Supervisor solutions provided in this application note, PSoC does have the capability to interface to digital CSAs with an I^2C interface. Please contact your local Cypress sales representative for more information.

5.3 Number of ADC Inputs

The vast majority of PSoC's I/O pins can be configured as analog pins. For example, the 100-pin TQFP package can support up to 64 analog pins. All of these can be routed to the ADC. Therefore, you can measure 64 power converter output voltages, 32 differential voltages or currents, or any combination in a single PSoC. If your application requires ADC measurement of a large number of power converter voltages, please contact your local Cypress sales representative for more information.

5.4 Post-Processing of ADC Measurements

The PSoC 3 Power Supervisor solution performs a minimal amount of post-processing on every voltage and current measurement. Even though the Delta Sigma ADC converter inherently filters the analog signal during the measurement process, additional firmware filtering suppresses AC noise and rejects transients or glitches. This is accomplished using an 8-sample box-car filter on all measurements. Once the filtered data is available, voltage measurements are compared to the user-defined OV/UV warning thresholds. The power supervisor can then alert the host processor over the PMBus interface if a power converter is beginning to deviate too far from the expected nominal range and may be approaching a fault condition. Similarly, current measurements are compared to the user-defined OC threshold and if the limit is exceeded the converter can be powered down.

5.5 ADC Resolution

Many engineers confuse resolution with accuracy. While increasing ADC resolution usually has a positive impact on accuracy, the two terms are not interchangeable. This will be explored further in the ADC Accuracy section.

While some devices in the PSoC 3 family can support ADC resolutions up to 20-bits, the PSoC 3 Power Supervisor solutions are targeted to PSoC 3 devices that have an ADC a resolution of up to 12-bits. This resolution was selected as an optimal trade-off between device cost, sample rate, and accuracy (in that order).

5.6 ADC Sample Rate

Conversion time, sample rate, update rate or scan time; whatever you choose to call it, what matters is how often you get a new measurement from each ADC input. The three factors that dictate this number are shown in Table 11.

Table 11: ADC Measurement Timing

ADC Configuration	Measurement Type	Conversion Time	Processing Time
0—4.096 V, Single-ended	Voltages and CSA currents	38 µs	15 µs
±64 mV, Differential	Sense Resistor Currents	87 µs	23 µs
Change ADC Configurations	N/A	N/A	320 µs

The overall ADC scan time for the two PSoC 3 Power Supervisor solutions can be calculated using these values. They are shown in Table 12.

Table 12: ADC Measurement Timing

Solution	# V	# CSA	# I	# ADC Re- configs	Total
4+1	5	2	3	1	1.021 ms
12+1	13	2	11	1	2.325 ms

These calculations are based on a 40 MHz MCU core running with no interruptions. Factoring in interrupts from other tasks, such as servicing PMBus transactions, could extend the samples rates by up to 10%.

5.7 ADC Accuracy

The purpose of an ADC converter is to convert an analog voltage to a digital code using a transfer function. Ideally, that transfer function would be linear and would intersect the origin (that is zero volts would produce a digital code of zero).

Imperfections in an ADC's transfer function can be characterized using three parameters that are typically combined to determine the ADC's overall absolute accuracy:

1. Input Offset Voltage Error
2. Gain Error
3. Integral Non-Linearity Error

5.7.1 Input Offset Voltage Error

This error term specifies the offset (in volts) that the actual ADC transfer function deviates from intersecting the origin. Its significance is dependent on the range of the ADC or the full-scale voltage level of the signal being measured. In the PSoC 3 Power Supervisor solution, the input offset voltage is periodically measured by internally shorting the differential ADC inputs together and taking an ADC reading. The reading is stored as a calibration data point and is either added or subtracted to subsequent power converter voltage and current readings depending on the polarity of the error. This automatic self-calibration works toward improving measurement accuracy without any effort or intervention from the user.

5.7.2 Gain Error

This error term describes by how much the slope of the ADC's actual transfer function deviates from the ideal case and is generally expressed as a percentage. The gain error can be calibrated out by connecting two known voltage sources to the ADC and comparing the measured results with the expected results. This calibration method can be difficult to achieve and costly to implement using traditional solutions. However, thanks to the flexibility and real-time re-configurability of PSoC, this error is also calibrated out by connecting PSoC's internal precision 1.024 V voltage reference to the ADC and taking a reading. The reading is stored as a calibration data point and subsequent power converter voltage and current readings are corrected based on the measured gain error. The second voltage source used for determining the gain error is zero volts. That measurement is taken and set to zero ADC counts during input offset voltage calibration.

5.7.3 Integral Non-Linearity Error (INL)

This error term describes the extent to which the ADC's actual transfer function deviates from a straight line and is expressed in units of converter LSBs. Its significance is dependent on the resolution of the ADC. INL error can only be calibrated out by measuring the full ADC transfer function across the entire voltage range, making it impractical to implement in a production system. The worst case INL Error for the PSoC 3 Power Supervisor solution is specified in Appendix A.

5.8 Voltage Reference Accuracy

Even when all ADC error sources are known and measured, additional error sources need to be considered to understand the true system-level accuracy of voltage and current measurements.

All ADC converters compare the voltage to be measured to a known reference voltage in order to produce the digital code. Therefore, the accuracy of the voltage reference also impacts the accuracy of the ADC measurement.

The PSoC 3 Power Supervisor solutions make use of PSoC 3's internal precision voltage reference. Its voltage reference is factory trimmed and known to have an accuracy of ±0.1% at 25 ºC.

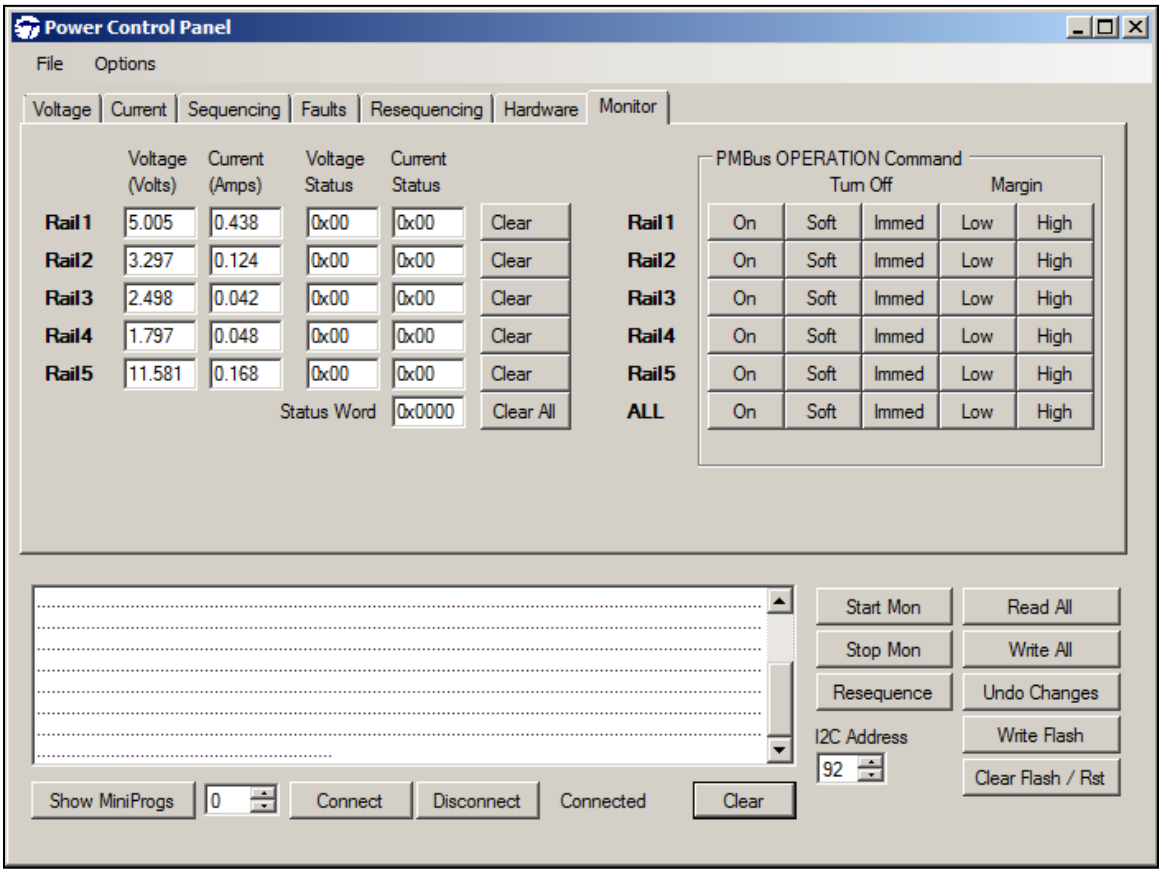
5.9 Drift, Stability, and Aging

Many of the error sources discussed so far are exacerbated by environmental stresses such as high temperature operation (drift) and cold→hot→cold thermal cycling (stability) and can worsen over time (aging). Appendix A provides several specifications that describe how the ADC and voltage reference parameters are impacted by these effects. The built-in automatic self-calibration can compensate for these errors with the exception of those that impact the voltage reference accuracy.

5.10 Exercise 6 – Voltage Measurement

In the **Power Control Panel**, go to the **Monitor** tab to see the ADC post-processed voltage and current measurements. When you initially view this tab, the first two columns that display the voltage and current measurements should be blank. Click on the **Start Mon** button to begin reading them over the PMBus. The measurements displayed here should match the measurements displayed on the LCD on the PSoC DVK shown previously in Figure 5. The **Monitor** tab is shown in Figure 19.

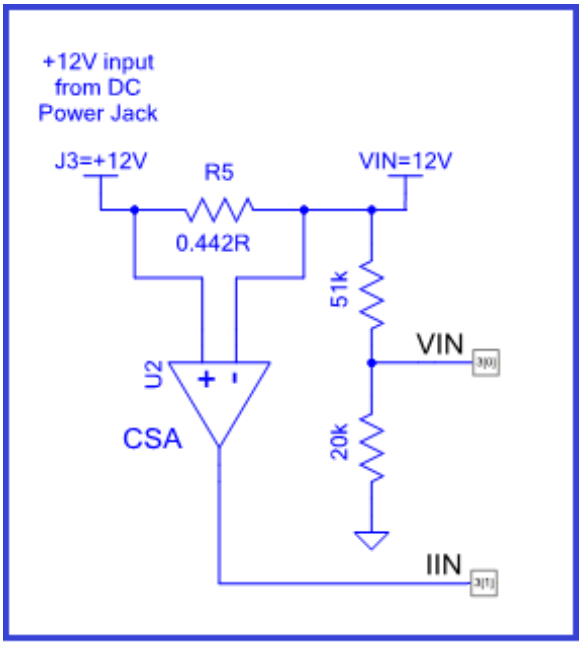
Figure 19: PMBus Power Control Panel – Monitor Tab



If you are interested, compare the voltages reported by PSoC with a digital multi-meter (DMM) if you have one available. All five power rails are accessible through the red colored test points on the PSoC Power Management EBK.

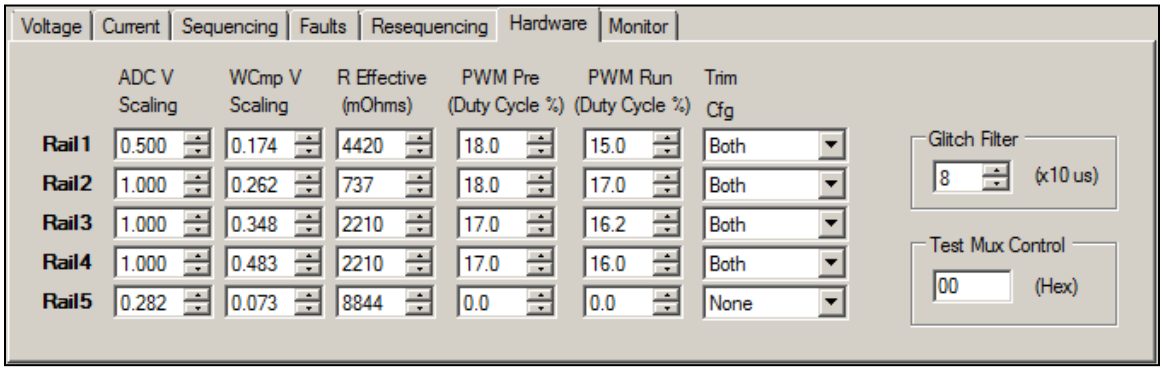
We discussed various measurement topologies earlier in this section. Figure 20 shows the topology implemented on the PSoC Power Management EBK for the +12 V primary input power source (the "+1" rail). The voltage is scaled down to around 3.8 V by the combination of the 20 kΩ and 51 kΩ resistor divider to suit the ADC range of 0—4.096 V. An external CSA is used with a gain of 20, presenting PSoC with a single-ended voltage which is 20x the differential voltage measured across the 442 mΩ sense resistor. Because the regulators on this board have very light loads (not more than a few hundred mA), the current sense resistors are much larger than those used in a real-world applications.

Figure 20: PSoC Power Management EBK – Primary Input Voltage Measurement Topology



For the PSoC 3 Power Supervisor solution to correctly convert scaled measurements back into actual voltages, it needs to know the external hardware components. Hardware parameters can be entered in the **Hardware** tab of the **Power Control Panel** as shown in Figure 21.

Figure 21: PMBus Power Control Panel – Hardware Tab



The two relevant parameters for this discussion are ADC V Scaling and R Effective.

5.10.1 ADC V Scaling

This parameter represents the scaling factor applied to the measured voltage. For the +12 V primary input shown in Figure 20, the scaling factor is 20 kΩ/ 71 kΩ = 0.282. You can see this value has been entered for Rail 5.

5.10.2 R Effective

This parameter allows you to specify the relationship between the voltage measurement made by PSoC and the actual load current. For the direct connect topology shown in Figure 13, **R Effective** is the value in mΩ of the series shunt resistor, since the voltage measured by PSoC is simply the load current multiplied by the sense resistor value.

For rails that use a CSA for current measurement as shown in Figure 14, **R Effective** is the product of the series shunt resistor value and the voltage gain provided by the CSA circuit. For CSAs that provide a voltage output, such as the MAX4080T from Maxim (used on Rail 5 of the Power Management EBK), this gain value can be obtained from the device's datasheet and is fixed at 20. Other CSAs provide a current output, such as the ZXCT1009 from Zetex (used on Rail 1 of the Power Management EBK). For that type of CSA, an external shunt resistor sets the effective voltage gain. From the device's datasheet, the gain of the CSA can be calculated using Equation 1.

Equation 1

$$Gain = \frac{V_{OUT}}{V_{IN}} = 0.01 \times R_{OUT}$$

On the PSoC Power Management EBK, a value of R_{OUT} = 1k Ω was chosen for a gain of 10. Therefore, to match the hardware configuration of the PSoC Power Management EBK, the **R Effective** parameter to be entered into the **Power Control Panel** for Rail 1 can be calculated using Equation 2:

Equation 2

$$R\ Effective = R_{SENSE} \times 0.01 \times R_{OUT}$$

Where:

$$R_{SENSE} = 5\ parallel\ 2.21\Omega = 442\ m\Omega$$

$$R_{OUT} = 1k\ \Omega$$

Solving:

$$R\ Effective = 4420\ m\Omega$$

Figure 22 through Figure 25 show the measurement topologies implemented for each of the four power converters on the PSoC Power Management EBK. Study these for a moment and observe how the hardware components relate to the parameters entered into **Hardware** tab of the **Power Control Panel.**

Figure 22: PSoC Power Management EBK – Rail 1 Voltage Measurement Topology

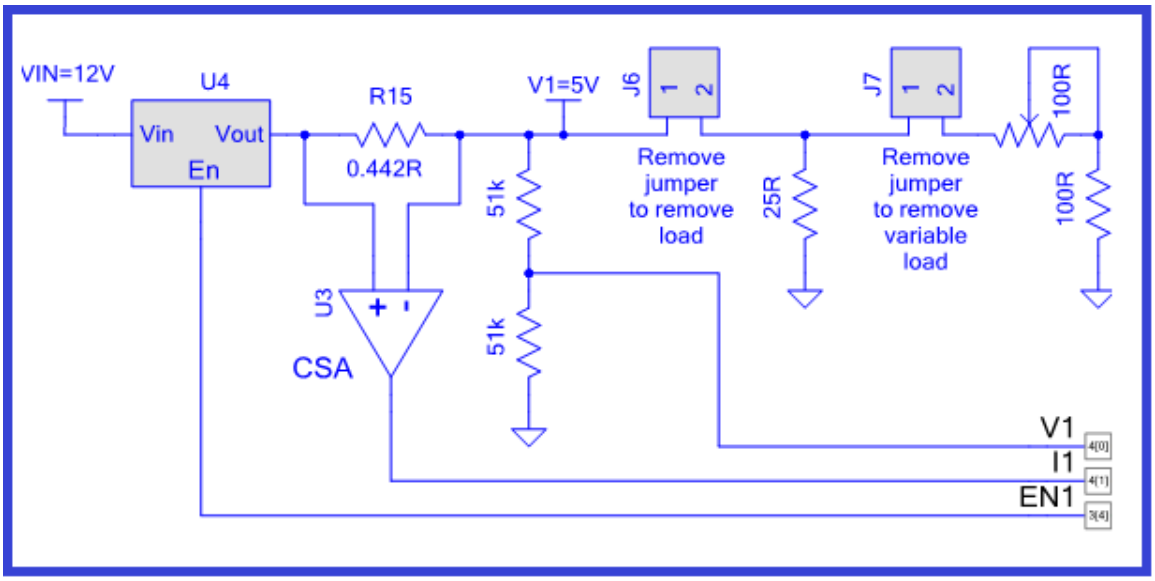


Figure 23: PSoC Power Management EBK – Rail 2 Voltage Measurement Topology

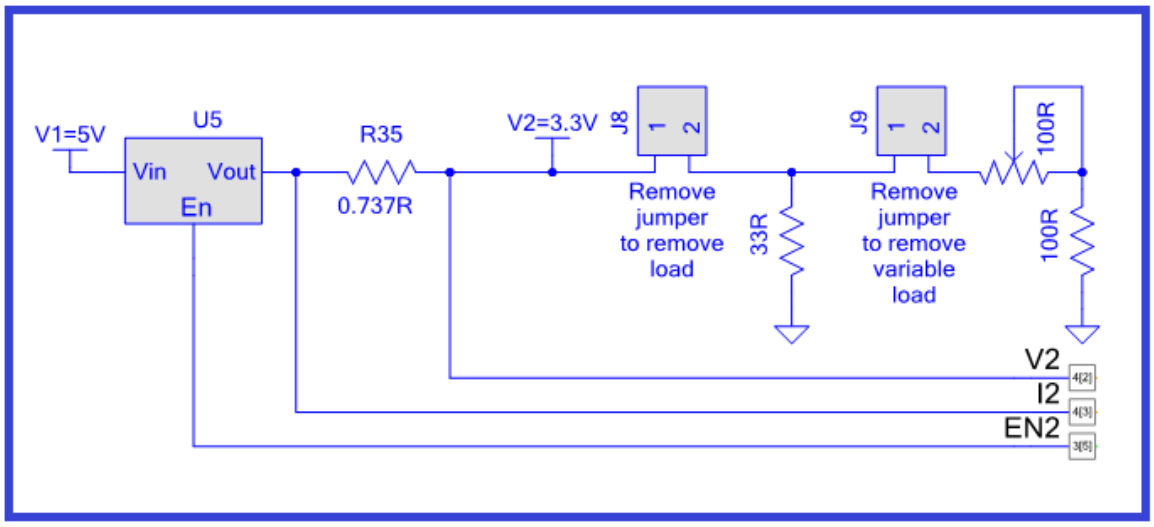


Figure 24: PSoC Power Management EBK – Rail 3 Voltage Measurement Topology

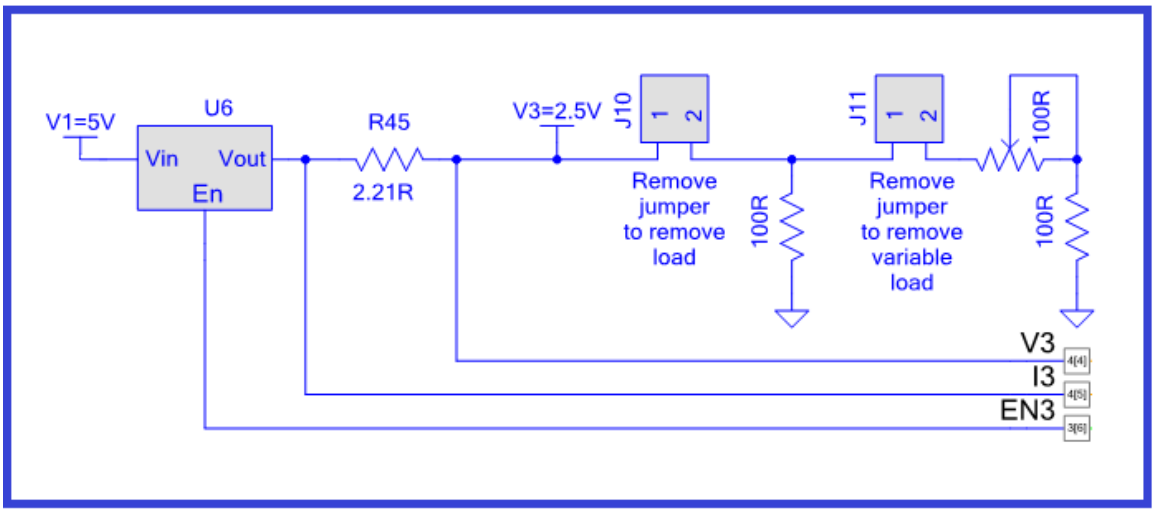
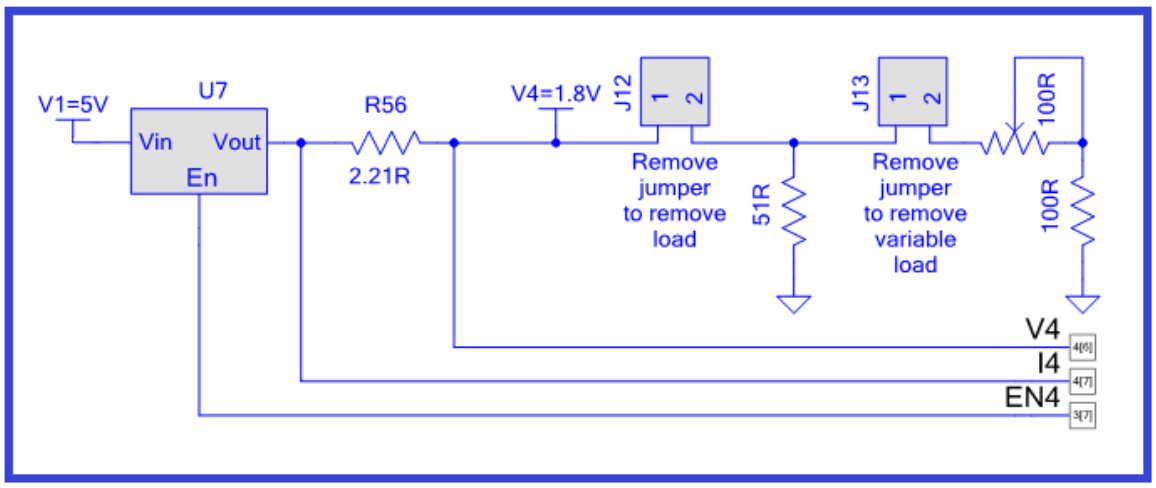


Figure 25: PSoC Power Management EBK – Rail 4 Voltage Measurement Topology



The **Power Control Panel** enables you to add or remove a fixed offset from the voltage measurements using the **Vout Offset** parameter on the **Voltage** tab. This feature was added to support the PMBus **VOUT_CAL_OFFSET** command which is intended primarily for manual system calibration. Since PSoC automatically self-calibrates, it is unlikely that you will need to use this feature; however, it is available if your application could take advantage of it.

5.11 Exercise 7 – Current Measurement

Now that we have entered the parameters that describe the hardware on the Power Management EBK, let's start reading the measured load currents.

The PSoC Power Management EBK provides some hardware hooks for you to simulate various load conditions. With reference to Figure 22 through Figure 25, you will see that each regulator has both a fixed load and a variable load that can be added using jumpers. The jumpers are also a convenient place to connect a DMM in series with the simulated loads to compare PSoC's current measurements against the DMM readings.

For the first part of this exercise, remove the variable loads by removing the jumpers labeled J7, J9, J11, and J13. In this condition, we can calculate the expected loads on each regulator as shown in Table 13.

Table 13: Expected Currents with Fixed Loads

Rail #	Nominal Voltage (V)	Fixed Load Resistance (Ω)	Expected Current (A)
1	5.0	25	0.2
2	3.3	33	0.1
3	2.5	100	0.025
4	1.8	51	0.035

In the **Power Control Panel**, go to the **Monitor** tab to see the ADC post-processed voltage and current measurements. Click on the **Start Mon** button to see the actual current readings displayed in amps.

What do you observe? The current measurements should be close to what we expected for Rails 2—4. However, Rail 1 is likely way off from the calculated value. Why is this so? Look back at Figure 7 for a clue. Rail 1 provides power to Rails 2—4, so the current reading from PSoC includes not only the fixed load resistance but also the power draw from the regulators that generate power for the other rails. We can virtually eliminate the current draw from those converters by removing the loads from Rails 2—4. Do this by removing jumpers J8, J10 and J12 from the Power Management EBK. When you have done this, you should notice two changes in the actual current readings displayed in the **Power Control Panel**:

1. The measured load current for Rail 1 now matches our expectation based on the fixed 25 Ω load resistor
2. The measured load currents for Rails 2—4 are now almost zero. The currents for these rails aren't truly zero since there are still some passive components connected to the rails for other purposes that you will see in the next section on fault detection

Feel free to put PSoC to the test by attaching a DMM across the terminals that are exposed when you remove a jumper such as J8, J10 or J12. Re-attach jumpers J7, J9, J11 and J13 to connect the potentiometers that enable you to simulate variable loads. When you're done with this exercise, remember to replace all the jumpers in preparation for subsequent exercises.

The **Power Control Panel** enables you to add or remove a fixed offset from the current measurements using the **Iout Offset** parameter on the **Current** tab. This feature was added to support the PMBus **IOUT_CAL_OFFSET** command which is intended primarily for manual system calibration. Since PSoC automatically self-calibrates, it is unlikely that you will need to use this feature; however, it is available if your application could take advantage of it.

5.12 Exercise 8 – OV/UV Warnings

In the **Power Control Panel**, go to the **Voltage** tab to see the **Margin Lo** and **Margin Hi** parameter settings. You will notice that the default voltage settings have been chosen to be between the OV/UV fault and warning thresholds. All of these values are shown in Figure 4. In this exercise we will take advantage of the margining capability of the PSoC 3 Power Supervisor solutions and demonstrate their ability to detect when the measured ADC readings are outside the warning threshold windows.

Go back to the **Monitor** tab and click on the **Start Mon** button to start displaying the voltage readings from PSoC. Click on either the **Low** or **High** buttons associated with Rails 1—4 in the control section labeled **PMBus OPERATION Command**. This invokes the margining operation, and you will see the voltage reading change from nominal to the user-specified **Margin Lo** voltage that was entered on the **Voltage** tab.

For example, Rail 1's **Margin Lo** voltage has been set to 4.6 V. Its **Margin Hi** voltage has been set to 5.3 V. When you click on Rail 1's **Low** button, the converter output should ramp down close to the 4.6 V target. At the same time, you should see Rail 1's **Voltage Status** field turn yellow and display 0x40 indicating UV warning. This value is based on the PMBus **STATUS_VOUT** reporting format. Click on Rail 1's **On** button to return it to its nominal voltage. The UV warning is still present in the **Voltage Status** display. The "sticky" warning reporting behavior is done to be compliant with the PMBus protocol specification. To clear the reported warning, click on Rail 1's **Clear** button.

The PMBus **OPERATION** command enables you to turn individual rails on and off. On the **Power Control Panel** go to the **Monitor** tab. Click on the **Soft** button to turn a rail off after the delay specified by the **Off Delay** parameter entered in the **Sequencing** tab or click on the **Immed** button to turn it off immediately. When you do this, you generate a fault condition as indicated by the **Voltage Status** field turning red for the associated rail. Click on the **On** button to bring the rail back up. After the rail returns to nominal output voltage, you will need to click on the rail's **Clear** button as described above to clear the sticky fault and warning conditions.

Experiment further with this, generating OV and UV warnings and UV faults on Rails 1—4. Remember that turning off Rail 1 will turn off Rails 2—4. Also, Rail 5, the primary power source, cannot be margined away from nominal voltage since no circuitry exists to adjust that voltage. Clicking on Rail 5's **Low**, **High** or **On** buttons has no effect.

5.13 Voltage and Current Measurements Summary

The 12-bit Delta-Sigma ADC inside PSoC is a high-accuracy (0.3%) converter that can be configured for single-ended and differential measurements. The PSoC 3 Power Supervisor solutions can be easily configured to match the power converter voltage and current measurement circuits including specific component values on your board.

PSoC's automatic self-calibration ensures that the measured values are as accurate as possible under any environmental conditions. This feature prevents you from having to add expensive, external calibration circuitry or spending time developing custom calibration solutions.

6 Section 3 – OV and UV Fault Detection

6.1 OV/UV Fault Detector Block Overview

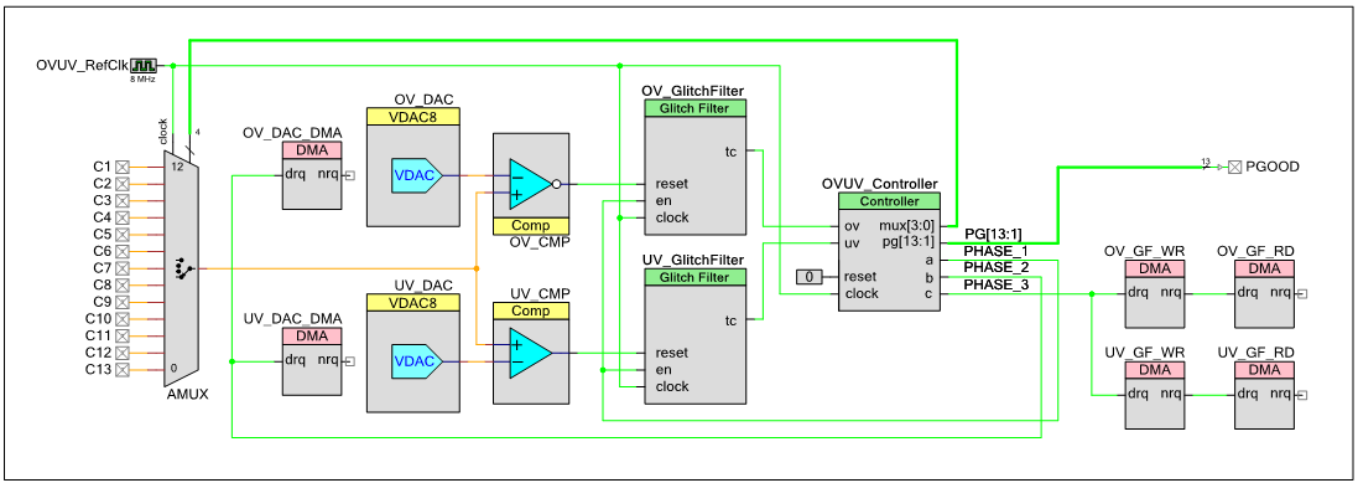
The OV/UV fault detector is arguably the most critical component of any power supervisor solution. It must respond as quickly as possible to OV or UV faults on a rail and shut it down before any damage occurs to the system.

In the PSoC 3 Power Supervisor solutions, the OV/UV fault detector is implemented entirely in hardware. It shuts down faulty rails within a guaranteed response time and does not require any intervention from PSoC's MCU core. At the heart of the fault detector is an analog window comparator with OV and UV fault thresholds set by two independent 8-bit DACs. System designers can set the OV and UV fault thresholds independently for every rail in the system. To monitor 13 rails (for the 12+1 solution), 26 independent thresholds are required. To support this requirement, and to make the solution scalable up to a maximum of 32 rails in a single chip (64 independent thresholds), the PSoC implementation is a little unique. Figure 26 shows the detail of the OV/UV fault detector. The inputs labeled C1—C13 are the power converter output voltages. Those voltages come into PSoC on different pins from the V1—V13 that we saw connected to the ADC. This is done for two reasons:

1. The input multiplexing rate of the ADC and the OV/UV fault detector are very different and not synchronized. The power converter voltage inputs are brought in on different pins to enable the ADC and the OV/UV fault detector block to operate truly independently
2. Voltage inputs to the OV/UV fault detector need to be scaled. The reason for this will be explained later in this section

Let's walk through the fault detector circuit block diagram to fully appreciate what's going on inside.

Figure 26: OV/UV Fault Detection Circuit Block Diagram



The central controller is labeled OVUV_Controller. It is a custom Verilog state machine responsible for coordinating the operation and timing of the hardware. The first step in the process is to select which power converter rail to monitor. This is done by generating a 4-bit control code that is connected to the select lines of the analog multiplexer shown on the left side of the block diagram. The selected rail is connected to the window comparator for 2 µs to allow the DACs to settle to the OV/UV thresholds for that rail. At the end of the 2 µs period, the central controller generates three timing strobes (PHASE_1, PHASE_2 and PHASE_3) to store the current result from the window comparator and prepare the circuit for the next rail to be monitored. PHASE_1 is generated first and is responsible for latching the window comparator results into the pair of programmable length glitch filters. PHASE_2 is generated next and triggers the DMA controllers that update the DACs with the OV/UV thresholds that are required for the *next* rail to be monitored. PHASE_3 is generated last and triggers two pairs of DMA controllers. The first DMA controller in each chain transfers the glitch filter result for the rail that was just monitored to SRAM for re-use during the next scan cycle. The second DMA controller in each chain retrieves the glitch filter result from SRAM for the rail that will be monitored *next* and puts it back into the glitch filter components. You can think of this as a context switch of the glitch filters. Once PHASE_3 is complete, the system disconnects the rail that was just monitored and then connects the *next* rail to monitor to the analog bus that feeds the comparators. The multiplexer has a guaranteed break-before-make switching mechanism to ensure that it is not possible to short two power converter rails together.

The central controller also generates the power good signals for all 13 rails, PG[13:1], that are connected to the voltage sequencer component. The voltage sequencer contains the hardware that immediately turns off a rail off if the OV/UV fault detector indicates that it has gone outside either the OV or UV fault threshold range signaled by de-asserting the rail's PG output.

The central controller repeats this process, stepping through each power converter rail input one-by-one in a round-robin fashion. It takes 2 µs per rail to complete the OV/UV threshold comparison. For the 12+1 solution, the worst case fault detection time is 13 x 2 µs = 26 µs. Once a fault is detected and PG is de-asserted, the worst case response time for de-asserting the EN to the faulty power converter is 25 ns. Once again, fault detection and converter shutdown is performed entirely in hardware and does not rely on the MCU in any way. This guarantees predictable timing and flawless operation no matter what other tasks are being performed by the MCU.

6.2 Hardware Settings for the OV/UV Fault Detector

To achieve maximum performance from the OV/UV fault detector, the DACs are set to the 1 V range. The maximum DAC update rate is 1 Msps. To directly compare the DAC-based OV/UV thresholds to the power converter voltages (C1—C13), the power converter voltages need to be scaled down. This is done on the PSoC Power Management EBK with a resistor divider network using resistors with ±0.1% tolerance. The values for these resistors should be kept low (2 kΩ or less) to minimize the analog settling time when the scaled input voltage is connected internally to the window comparator. Figure 27—Figure 30 show the resistor values used for scaling Rails 1—4. For Rail 1, the voltage scaling resistors for the ADC are also shown.

Figure 27: PSoC Power Management EBK – Rail 1 Voltage Scaling for the OV/UV Fault Detector

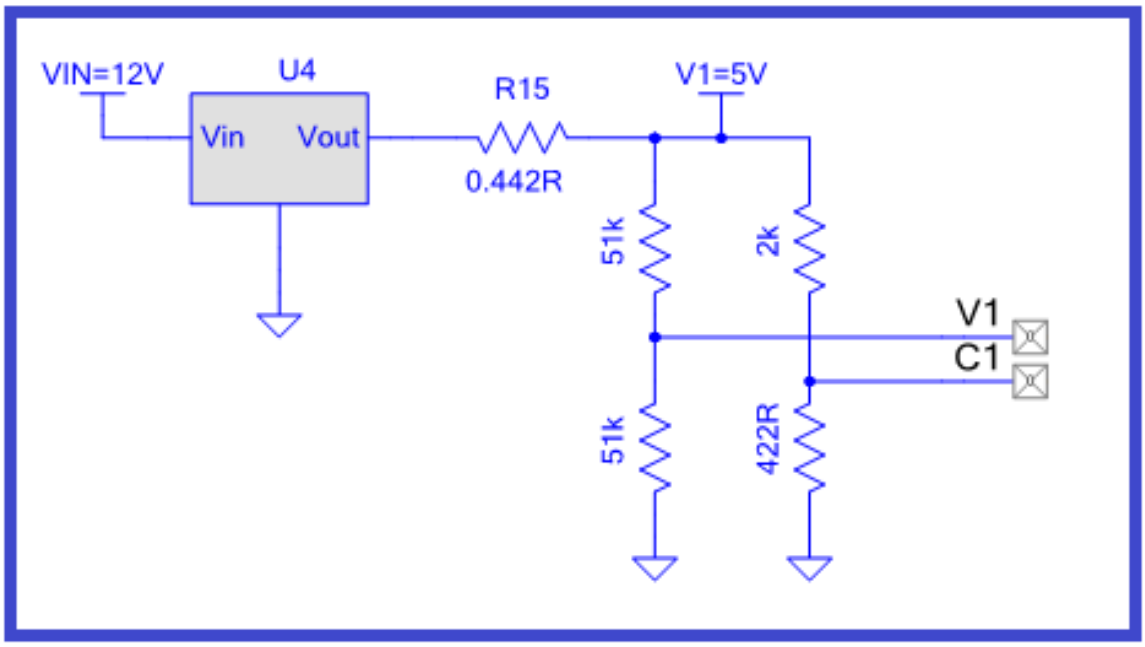


Figure 28: PSoC Power Management EBK – Rail 2 Voltage Scaling for the OV/UV Fault Detector

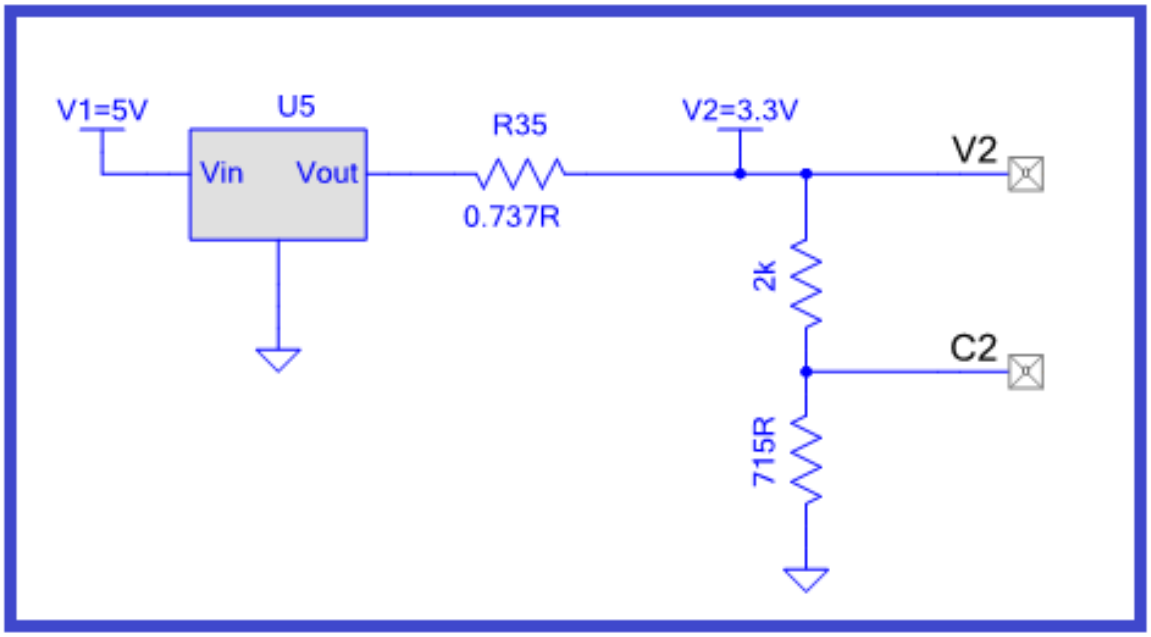


Figure 29: PSoC Power Management EBK – Rail 3 Voltage Scaling for the OV/UV Fault Detector

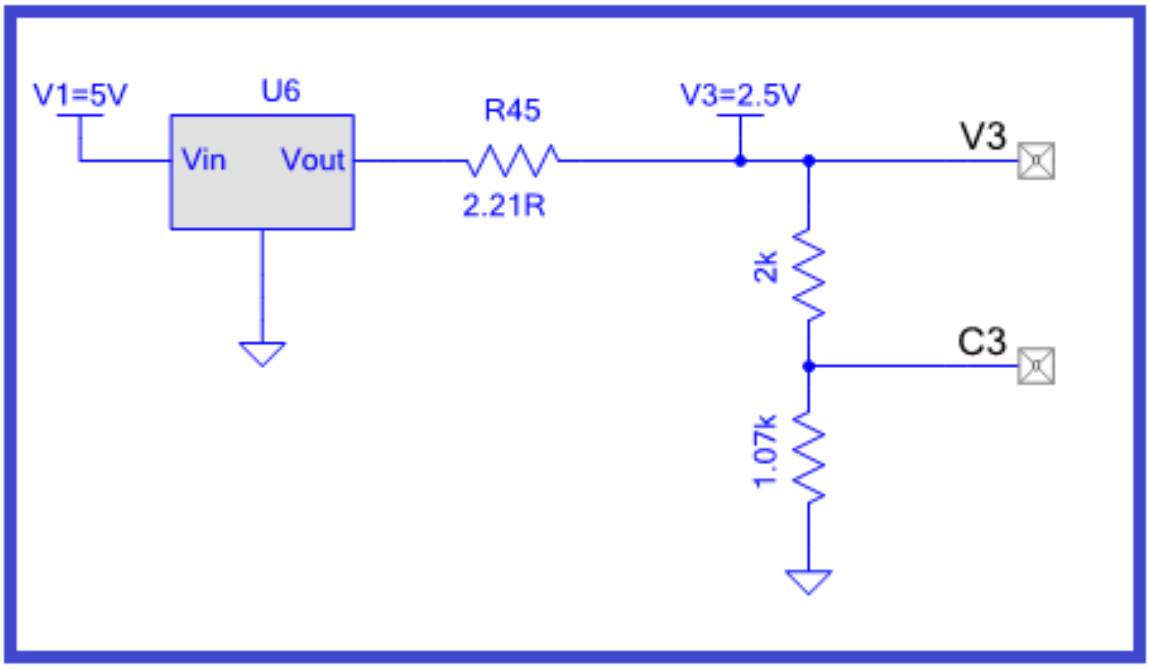
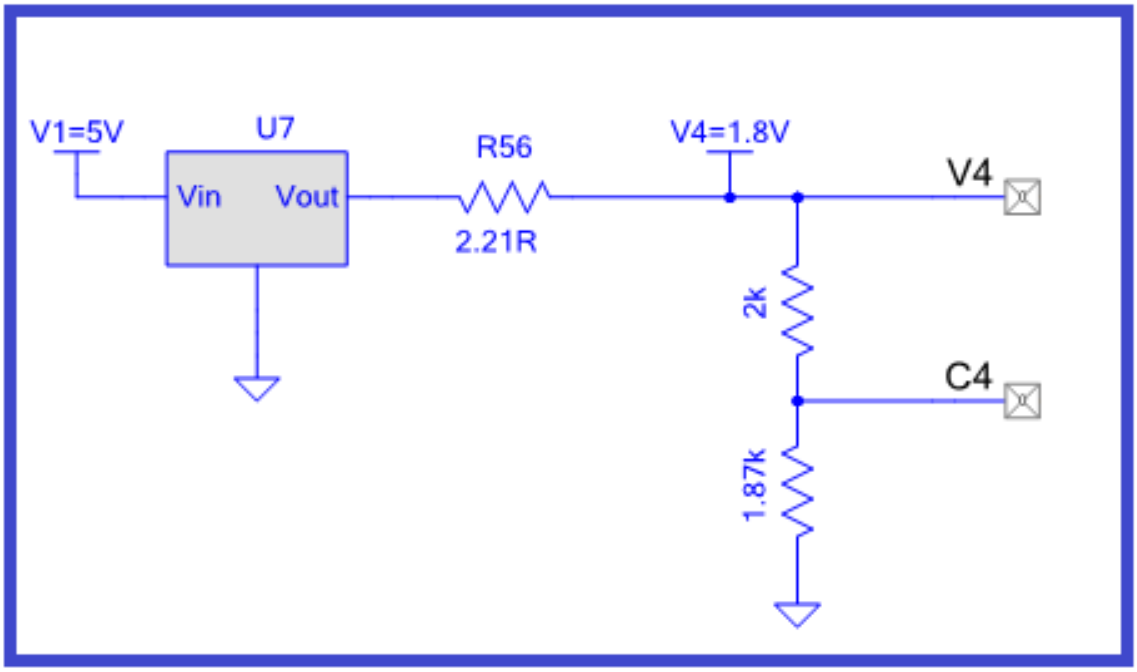


Figure 30: PSoC Power Management EBK – Rail 4 Voltage Scaling for the OV/UV Fault Detector



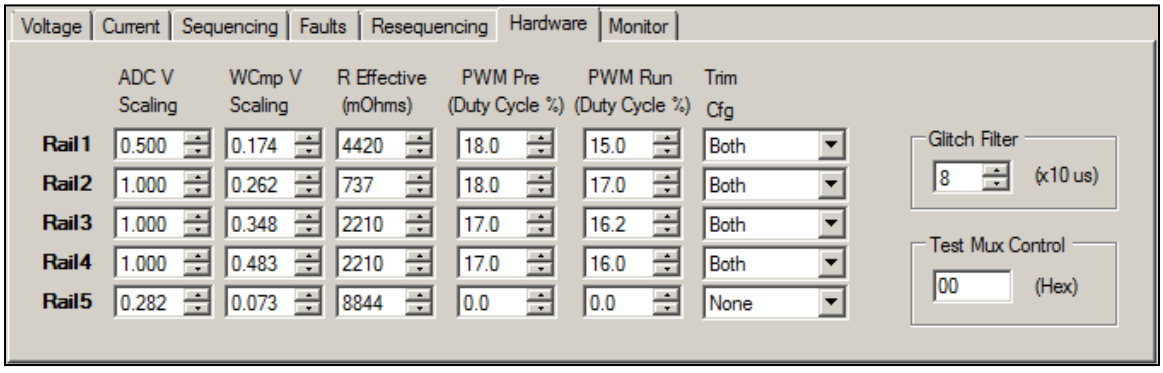
You can use these resistor values to calculate the scaling factors shown in Table 14.

Table 14: OV/UV Fault Detector Voltage Scaling Factors

Rail #	Nominal Voltage (V)	RA (Ω)	RB (Ω)	Scaling Factor
1	5.0	2k	422R	0.174
2	3.3	2k	715R	0.263
3	2.5	2k	1.07k	0.348
4	1.8	2k	1.87k	0.483

In the **Power Control Panel** go to the Hardware tab to enter the scaling factors in the **WCmp V Scaling** field shown in Figure 31.

Figure 31: PMBus Power Control Panel – Hardware Tab



Note On the PSoC Power Management EBK, the primary +12 V power supply input does not connect to the window comparator and faults on that rail can only be detected using the ADC. The worst case fault detection time for the 4+1 solution is therefore 4 x 2 µs = 8 µs. For the 12+1 Power Supervisor solution, the primary rail is scaled along with the other rails for fast fault detection using the OV/UV fault detector.

The other parameter that affects the operation of the fault detector is the glitch filter length. The length can be set between 0 and 255 time steps. The resolution of the time steps depends on the number of rails in the system. For the 12+1 solution, the step size is 26 µs. For the 4+1 solution, the step size is 8 µs. The glitch filter length can be entered on the **Hardware** tab using the **Glitch Filter** parameter. This is a global setting that impacts all rails for both OV and UV glitch filtering.

Finally, the OV and UV fault thresholds that were entered into the **Voltage** tab are the values that will be scaled down and applied to the DACs responsible for setting the thresholds. The PSoC 3 Power Management solutions will take care of the scaling issues for you, you just need to enter your desired OV and UV thresholds in Volts.

The **Vout Offset** parameter on the **Voltage** tab also comes into play here. Entering a non-zero value into this parameter will cause the same magnitude of adjustment to occur in the OV/UV threshold settings for the DACs.

6.3 Exercise 9 – Detecting OV/UV Faults

Let's use the solution's margining capability to generate faults that will test the OV/UV fault detector. In the **Power Control Panel**, go to the **Voltage** tab to see the **Margin Lo** and **Margin Hi** parameter settings. Change them both so that the voltages are outside the OV/UV fault thresholds. Alternatively, you could change the OV/UV fault thresholds. Either way, configure the system so that clicking on the **Margin Lo** or **Margin Hi** buttons will generate a fault.

Go back to the **Monitor** tab and click on the **Start Mon** button to start displaying the voltage readings from PSoC. Click on either the **Low** or **High** buttons associated with any of the Rails 1—4 in the control section labeled **PMBus OPERATION Command**. Doing so will invoke the margining operation. When the power converter output voltage crosses one of the fault thresholds, you should see the voltage sequencer shut down the rails as you have specified in the **Faults** tab. The fault condition will also be indicated by the red color background of the faulty rail's **Voltage Status** field. Click on the **On** button to bring the rail back up. When the rail recovers and returns to nominal output voltage, you will need to click on the **Clear** button as described earlier to clear the sticky fault condition flags.

More adventurous experimenters can try shorting one or more of the rails to ground with a wire as described in Exercise 4 – Fault Responses. However you choose to generate faults, keep experimenting with the setup and play with the configuration parameters until you are comfortable with how the OV/UV fault detector works.

OV and UV Fault Detection Summary

The flexibility of PSoC's programmable analog blocks, digital blocks and interconnect make it possible to implement complex mixed-signal functions like the OV/UV fault detector. Even though all rails share a single window comparator block, the fault detection response times are still very competitive with other solutions available in the market. You can instantiate two OV/UV fault detection blocks inside a single PSoC to cut the fault response time in half. Please contact your local Cypress sales representative for more information.

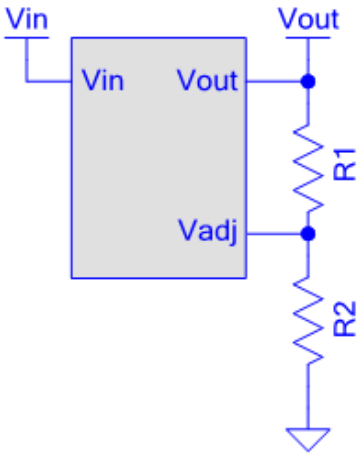
7 Section 4 – Trimming and Margining

In this section we will explore how to dynamically adjust the power converter output voltages in real time through the trimming capability of the PSoC 3 Power Supervisor solution. Trimming power rails provides several system-level benefits:

- High-performance ASICs and multi-core processors get the optimal power supply voltage to tradeoff power vs. performance.
- Designers can change converter output voltages at any time during the life of the product without redesigning the power circuits. This is useful when removable components such as memory modules are upgraded and require lower operating voltages.
- Setting the power converters to their maximum or minimum rated output voltage during system testing ensures that the system functions properly across the entire specified voltage range.

Figure 32 shows the typical schematic for an adjustable output power converter. The converter employs a negative feedback control loop that adjusts the output voltage (V_{OUT}) based on the sensed voltage that is presented to the feedback or adjust terminal (V_{ADJ}). The sensed voltage is compared to an internal reference voltage and the error voltage term is used to increase or decrease the output voltage (V_{OUT}) in order to maintain proper regulation. The manufacturer's datasheet will specify what voltage is required or will be present on the V_{ADJ} terminal to achieve stable regulation.

Figure 32: Typical Adjustable Power Converter Circuit



The voltage at the V_{ADJ} terminal is divided down from the V_{OUT} terminal as follows:

Equation 3

$$V_{ADJ} = V_{OUT} \times \left(\frac{R2}{R1 + R2}\right)$$

The converter will be in regulation when V_{ADJ} is equal to its internal reference voltage (V_{REF}). Re-arranging this equation:

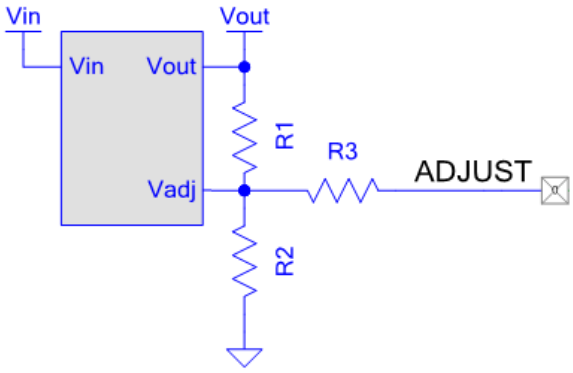
Equation 4

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

Using the V_{REF} value from the manufacturer's datasheet, designers can select the ratio of R1 and R2 to produce the desired nominal output voltage.

There are several ways to accomplish real-time dynamic trimming or margining. It should be clear from Equation 4 that changing R1 or R2 will change the output voltage. We could achieve this goal using a digitally controlled potentiometer, but this is a costly solution especially when trimming is required on a large number of rails. The simplest method, commonly used for margining, is to add a third resistor, R3, to the circuit as shown in Figure 33.

Figure 33: Simple Margining Control

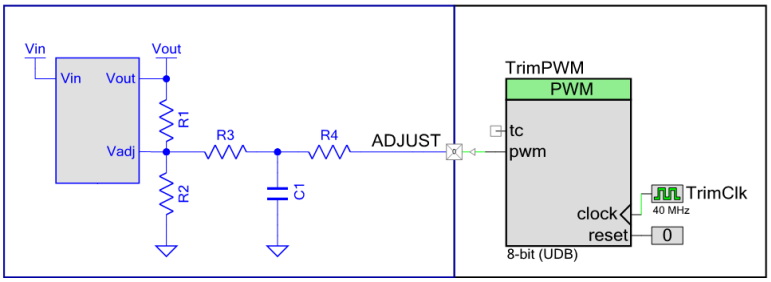


R3 is pulled to ground to raise the converter output voltage, pulled high to lower the converter output voltage or tri-stated to have no impact. The benefit of this approach is that a low-cost microcontroller or programmable logic device can adjust the output voltage of the power converter using a single logic-level control pin (labeled ADJUST in Figure 33). The extent to which the converter output voltage can change is set by selecting the appropriate resistor value for R3. When the ADJUST terminal is pulled low, R2 and R3 are in parallel, which will result in a reduced voltage seen at the V_{ADJ} terminal of the regulator, resulting in an increased output voltage, V_{OUT}. When the ADJUST terminal is pulled high, the current flowing through R3 will be added to the current flowing through R1 and flow into R2. That will result in an increased voltage seen at the V_{ADJ} terminal and the converter will respond by reducing V_{OUT}.

This approach works well for margining applications where the designer wants to change the converter output voltage in discrete steps, but it does not provide the capability to adjust the output voltage across a continuous range of voltages. One common method for achieving that goal is to drive R3 with a DAC. This allows the user to control the direction and magnitude of the current that flows through R3, and therefore, the voltage seen at the V_{ADJ} terminal. Using this method, the level of trimming control is dictated not just by the value of R3 but also by the resolution and voltage range of the DAC.

In the PSoC 3 Power Supervisor solutions, DACs are emulated using PWMs with an external RC filter as shown in Figure 34.

Figure 34: PWM Based Trimming/Margining Control



This implementation was chosen in order to support designs that require trimming/margining on many rails. The black colored box on the right represents the circuitry inside PSoC. The blue colored box on the left represents circuitry external to PSoC. R3 provides the mechanism to change the current flow into R2, while R4 and C1 provide the filtering mechanism to convert the AC PWM signal into a DC control voltage for R3.

Let's walk through the component value selection process for this implementation based on a real example. Rail 4 on the PSoC Power Management EBK is a 1.8 V rail generated by an ADP3331 LDO regulator. The manufacturer's datasheet recommends:

- The parallel resistance of R1 and R2 should be as close as possible to 230 kΩ
- For 1.8 V nominal output, the suggested values are R1 = 340 kΩ and R2 = 698 kΩ
- V_{ADJ} = 1.2104 V with those resistor values

This power converter has a unique design. The internal reference for this converter (V_{REF}) is not equal to the voltage present on the V_{ADJ} pin.

Rail 4 on the Power Management EBK was designed to support a trimming range of ±25% around nominal (1.35—2.25 V). The high end of the trimming range (V_{MAX} = 2.25 V) is achieved when the PWM duty cycle is at 0% or when the PWM output is held at a low level. In that case, the sum of resistances R3 and R4 are pulled to ground in parallel with R2. Working through the math, this results in:

Equation 5

$$R3 + R4 = \frac{V_{ADJ} \times R1 \times R2}{V_{MAX} \times R2 - V_{ADJ} \times (R1+R2)}$$

Substituting results in:

$$R3 + R4 = 914\ k\Omega$$

The recommended rule of thumb is to make R3 ten times larger than R4. Using 1% tolerance standard values:

$$R3 = 825\ k\Omega$$

$R4 = 82.5\ k\Omega$

The final step is calculating the C1 filter capacitor value. This choice is driven by four factors:

1. The frequency of the PWM signal (F_{PWMOUT})
2. The resolution of the PWM (PWM_{RES})
3. The voltage swing of the PWM signal (V_{PWM})
4. How much ripple is acceptable at the output of the filter formed by R4 and C1 (V_{RIPPLE}) since that ripple ultimately couples into the V_{ADJ} pin

For the PSoC 3 Power Supervisor solutions, the PWMs have an internal clock source of 40 MHz. The PWMs are all configured for 8-bit resolution. The frequency of the PWM output signal that connects to R4 and C1 is therefore:

Equation 6

$$F_{PWMOUT} = \frac{40\ MHz}{256} = 156.25\ kHz$$

For the 12+1 solution, the voltage swing of the PWM outputs is different depending on the trim output pin number. Trim PWM outputs 1—6 have a logic high level of 5 V, while outputs 7—12 have a logic high level of 1.8 V (internally regulated). For the 4+1 solution, all PWM outputs have a logic high level of 5 V. There are three benefits to using the lower voltage output PWMs:

1. It improves the trimming resolution ($TRIM_{RES}$). That is, the minimum possible change in regulator output voltage is lower, enabling finer control.
2. The lower amplitude signal is easier to filter resulting in less ripple at the V_{ADJ} pin.
3. Most regulators regulate their V_{ADJ} pin to around 800 mV. Since that is near the midpoint of the 1.8 V PWM voltage swing, you get nearly symmetrical trim control around the nominal voltage point. When using the 5 V swing PWMs, the duty cycle to achieve the 800 mV nominal is around 16%. That means the PWM can trim the power converter down much lower than the nominal voltage, but it does not have the ability to trim up to the same extent.

Designers should use trim PWM outputs 7—12 for the power converters that require the finest possible control. Based on this information, the equation for calculating C1 is:

Equation 7

$$C1 = \frac{V_{PWM}}{(2 \times \pi \times R4 \times F_{PWMOUT} \times V_{RIPPLE})}$$

If we set a design goal that **V_{RIPPLE}** must be < 500 µV, and use the 5 V voltage PWM outputs, **C1** becomes:

$$C1 = \frac{5000\ mV}{(2 \times \pi \times 82.5k\Omega \times 156.25\ kHz \times 0.5\ mV}$$

$$C1 = 0.12\ \mu F$$

This example shows that when you use PWMs for trim/margin control, a very low amount of ripple is generated even when using modest values for the passive filter components. Both filter component values are readily available in very small surface mount packages.

Now that we've designed the trim circuit, let's evaluate its performance to confirm it will meet our needs. We selected the appropriate values of R3 and R4 to ensure that we will meet the maximum required power converter output voltage V_{MAX} = 2.5 V when the PWM duty cycle is 0%. Let's start by calculating the PWM duty cycle high-time counts required to achieve the nominal converter output voltage:

Equation 8

$$COUNTS_{NOM} = (2^{PWM_{RES}} - 1) \times \frac{V_{ADJ}}{V_{PWM}}$$

Substituting yields:

$$COUNTS_{NOM} = 61\ (24\%\ Duty\ Cycle)$$

The minimum resolution of the trimming circuit is the smallest change in the power converter's output voltage based on a duty cycle high-time change of one count. It can be calculated from using Equation 9:

Equation 9

$$\text{TRIM}_{\text{RES}} = \frac{V_{MAX} - V_{NOM}}{COUNTS_{NOM}} = 7.4\ mV\ (0.4\%)$$

This equates to 0.4% of the 1.8 V nominal output per step change of PWM duty cycle high-time count. The minimum power converter output voltage we can achieve when the duty cycle is 100% is:

Equation 10

$$V_{MIN} = V_{NOM} - TRIM_{RES} \times ((2^{PWM_{Res}} - 1) - COUNTS_{NOM})$$

$$\rightarrow V_{MIN} = 0.36\ V$$

In summary, our design goal for the trim circuit was to trim the nominal converter output voltage of 1.8 V up or down symmetrically by ±25% (1.35—2.25 V). Our actual performance is 0.36—2.25 V or -80% to +25%. The reason for this asymmetry is the high voltage swing of the PWM (V_{PWM} = 5 V).

Let's work through the math again using one of the low voltage (1.8 V) PWM outputs available on the 12+1 solution. Re-calculating equations 8, 9, and 10:

$$COUNTS_{NOM} = 171\ (PWM_{NOM} = 67\%)$$

$$\text{Min.}\,\Delta V_{OUT} = 2.6\ mV\ (0.14\%)$$

$$V_{MIN} = 1.58\ V$$

The trimming symmetry and resolution have both improved, but we have failed to meet the minimum trim voltage output goal of 1.35 V. The right way to ensure we meet the trim dynamic range goal is to calculate the TRIM_{RES} needed:

Equation 11

$$\text{TRIM}_{\text{RES}} = \frac{V_{NOM} - V_{MIN}}{((2^{PWM_{Res}} - 1) - COUNTS_{NOM})} = 5.3\ mV$$

$$V_{MAX} = V_{NOM} + (COUNTS_{NOM} \times \text{TRIM}_{\text{RES}})$$

$$\rightarrow V_{MAX} = 2.72\ V$$

Now our solution has a trim range of 1.35—2.72 V (-25% to +50%) with a trim resolution of 5.3 mV (0.3%). If we elect to change to the lower voltage PWM, we need to go back and re-calculate R3, R4 and C1 based on the new V_{MAX} and V_{PWM} parameters.

It may appear that the trim circuit design flow is based on trial and error, however, it was presented that way intentionally as a learning process. The right way to design the trim circuit is based on the nominal output voltage.

If $V_{PWM}/2 > V_{ADJ}$

- The trim circuit has plenty of head room to reduce the output voltage, but limited range to increase it
- Use the target VMAX to select R3,
- Go through the rest of the math and you're done

If $V_{PWM}/2 < V_{ADJ}$

- The trim circuit has plenty of head room to increase the output voltage, but limited range to decrease it
- You may not be able to achieve your desired V_{MIN}
- Calculate TRIM_{RES} based on your V_{MIN} requirement
- Use TRIM_{RES} to dictate V_{MAX} and calculate R3
- Go through the rest of the math and you're done

This exercise has shown that using lower voltage PWMs improves the trimming circuit resolution and the symmetry of the trim range around nominal. The trim symmetry issues we saw are not unique to a PWM based trimming architecture. DAC based trimming architectures suffer from the same issue. If the voltage output from the DAC does not equal V_{ADJ} at nominal output voltage when the DAC digital code is half of full-scale, then a DAC based solution will have symmetry issues as well. In a PWM-based architecture, our equivalent of the DAC digital code is the PWM duty cycle. For this discussion, they can be considered to be the same thing.

To further improve the resolution of the trimming circuit, you could consider increasing the PWM resolution to 9 or 10-bits. This will improve (reduce) the resolution by 2x or 4x respectively. However, this will also reduce the PWM output frequency by the same amount which will require larger filtering components. Designers can trade off resolution vs. PWM frequency and ripple to meet the system level needs of their application. The PSoC 3 Power Supervisor solutions are fixed at 8-bit PWM resolution. However, if you are interested in developing trimming circuits using higher resolution PWMs with PSoC, please contact your local Cypress sales representative for more information.

7.1 Active Trimming

The PSoC 3 Power Supervisor solutions employ active trimming. This means that the power converter output voltage is constantly monitored by the ADC and compared to the desired trim output voltage. Any error will be compensated for with a change in the PWM duty cycle. This feedback control loop ensures continuous regulation to the desired trim output voltage under varying load conditions. This control loop also operates in margining modes.

7.2 Power Converter Start-Up Considerations

Active trimming is enabled by default in the PSoC 3 Power Supervisor solutions provided. You can change this default behavior by changing the **Trim Cfg** parameters on the **Hardware** tab of the **Power Control Panel** shown in Figure 31. Table 15 explains the selections that are available on the **Trim Cfg** pull down menus.

Table 15: Trim Cfg Parameter Options

Trim Cfg Option	Description	Comment
None	PWM outputs are tri-stated	Trim/margin is disabled
Margin Only	PWMs are driven only when margin commands are sent	Active trimming control loop runs to regulate to the desired margin levels
Both	PWMs are always driven	Active trimming control loop is always running
Fixed	PWMs are always driven	User specifies the PWM duty cycles

If trimming is disabled (**Trim Cfg** = None), the PWM outputs are tri-stated and do not influence the power converter's self-regulation loop. There are no special start up considerations.

If trimming is enabled, some care must be taken to set the initial duty cycles for the PWMs. If the PWM that drives the trim circuit is enabled at the same time that the voltage sequencer enables the power converter, capacitor C1 will not yet be charged. This will initially result in a lower than desired control voltage at the V_{ADJ} pin of the converter, causing the converter to overshoot the desired nominal voltage. This overshoot could trip the OV/UV fault detection circuit, which is clearly undesirable. To avoid this problem, the PWM trimming circuit should be turned on before the voltage sequencer enables the converter. In that condition, the converter output voltage is close to ground potential. Therefore, R1 will be acting as an additional pull down resistor in parallel with R2 (refer back to Figure 34 with V_{OUT} = 0 V). To compensate for this, a PWM pre-run duty cycle (PWM_{PRE}) is calculated to ensure that the desired voltage is present on the V_{ADJ} pin at the time the voltage sequencer enables the regulator. The pre-run duty cycle is calculated as follows:

Equation 12

$$COUNTS_{PRE} = COUNTS_{NOM} \times \left[\left(\frac{R4}{R3 + (R2 \,//\, R1)}\right) + 1\right]$$

Substituting $COUNTS_{NOM}$ = 61 for 5 V PWM voltage swing and R1—R4 as calculated earlier under the same conditions:

$$COUNTS_{PRE} = 66 \; or \; PWM_{PRE} = 26\%$$

This duty cycle will be used as the starting point for the active trimming control loop. As the power converter ramps up, the duty cycle will be adjusted to achieve the desired power converter output.

When you have completed your trimming circuit design, the only parameters you need to enter into the **Power Control Panel** are the PWM duty cycle required to achieve nominal output and the PWM pre-run duty cycle for each converter. These values can be entered into **Hardware** tab through the **PWM Run** and **PWM Pre** parameters respectively. When you make changes to these parameters, they will not take effect immediately since active trimming is in progress. To see the impact of the changes, you should send a new PMBus **OPERATION** command. You can do this by going to the **Monitor** tab and click on the **On** button for the associated rail. Alternatively, you can commit your new parameters to flash and reset PSoC by pressing the reset switch on your PSoC DVK.

The default target voltage for each rail is the nominal voltage specified on the **Voltage** tab. If you need a power converter to always startup and run at a different voltage than what was designed on your board when you selected the initial values for R1 and R2, all you need to do is:

1. Configure the new nominal voltage and OV/UV warning and fault thresholds on the **Voltages** tab
2. Re-calculate the $COUNTS_{NOM}$ and $COUNTS_{PRE}$ to set the initial data points for the active trimming algorithm. These values are entered into the **Power Control Panel** on the **Hardware** tab using the **PWM Run** and **PWM Pre** parameters respectively

The active trimming circuit will do the rest automatically, and the OV/UV fault detector will monitor the rail based on the new OV/UV warning and fault thresholds.

7.3 Turning Active Trim On and Off

You can turn active trim on and off at any time by changing the **Trim Cfg** parameter (located on the **Hardware** tab) and sending a new PMBus **OPERATION** command as described above. When turning active trim off, the V_{ADJ} voltage will go back to the nominal setting dictated by R1 and R2 on your board. If you are trimming above nominal voltage, be sure to trim back to nominal before turning active trim off to avoid a sudden change in power converter output voltage. Also be sure to change the OV/UV thresholds appropriately to avoid triggering unintentional fault conditions.

When turning active trim back on, you do not need to be concerned about setting the PWM duty cycle to the pre-charge PWM_{PRE} value. The power converter is on and R1 is connected to the nominal output voltage and is scaling that voltage appropriately to generate V_{ADJ}. PWM_{NOM} will be used as the starting point for the active trim algorithm.

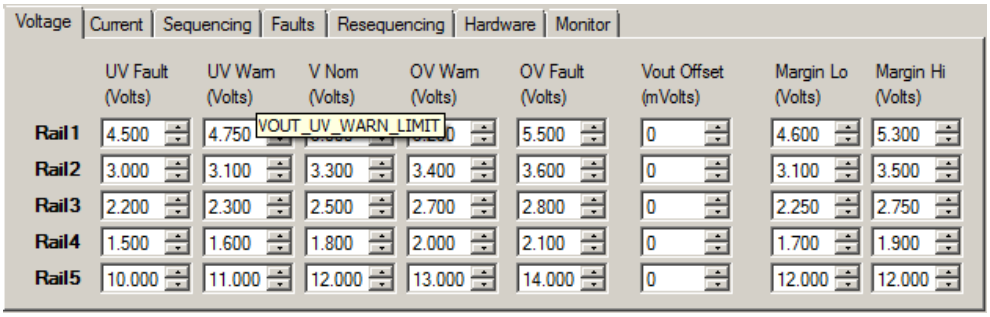
There are no hands-on exercises for this section since we already experimented with active trimming when we did low and high margining to generate faults for the OV/UV fault detector. If you're longing for some hands-on exercises after such a long section on trimming theory, why not connect an oscilloscope to one of the rail outputs on the Power Management EBK and observe the dynamic behavior of the converters under the control of the active trim algorithm in response to margin low and high commands? You can also monitor the PWM signals before they are filtered by R4 and C1 on the matrix of exposed pads next to the Power Management EBK expansion connector. The PWM outputs are labeled TR1—TR4.

8 Section 5 – PMBus Interface

All of the interactions we've had with the PSoC 3 Power Supervisor solution in the hands-on exercises have been through PMBus commands. Many of the parameters in the **Power Control Panel** are defined by the PMBus specification. The PMBus protocol was chosen as the host interface for these solutions because it has been widely adopted in the industry for power applications and software developed for other PMBus components can be leveraged when developing software support for the PSoC 3 Power Supervisor solution. To support features and functions that are specific to the PSoC implementation, PMBus manufacturer specific commands have been defined. The full list of PMBus protocols and commands supported by the PSoC 3 Power Supervisor solutions are described in Appendix A.

The **Power Control Panel** has tooltips incorporated to help you relate each specific parameter to the associated PMBus command. Figure 35 shows an example of how tooltips pop up when you hover your cursor over a parameter name.

Figure 35: PMBus Power Control Panel – PMBus Command Tooltips



The PMBus interface in the PSoC 3 Power Supervisor solutions is configured to run at 100 kbps and does not support packet error checking (PEC). If you require PEC, need to run at 400 kbps, would like to use a simple I^2C register-based access model, or prefer an alternative PHY interface such as SPI, UART, or USB, PSoC can be re-configured to meet your needs. Please contact your local Cypress sales representative for support.

Two optional PMBus pins are also supported by the PSoC 3 Power Supervisor solutions, CONTROL and SMBALERT#.

The PMBus CONTROL pin was described in Section 1 – Voltage Sequencing. This pin provides the system supervisor a hardware means of turning the power converters on or off.

The SMBALERT# pin enables the PSoC 3 Power Supervisor solutions to alert the PMBus host that a warning or a fault condition has occurred. While this pin is supported, the PSoC 3 Power Supervisor solutions do not respond to the I^2C Alert Response Address (ARA) defined in the SMBus specification. Instead, the PMBus host should clear alerts reported by PSoC through the PMBus **CLEAR_FAULTS** command. This is described in more detail in Appendix A.

9 Building Your Own Custom Solution

The PSoC 3 Power Supervisor solutions presented in this application note are intended to provide designers with a highly configurable power supervisor solution that is ready to run right out-of-the-box. These solutions are very easy to configure using the simple PMBus **Power Control Panel** GUI without having to develop any custom firmware and are intended to facilitate rapid time-to-market.

For designers who want to take full advantage of PSoC's mixed-signal programmable architecture and develop more custom solutions, the PSoC Creator™ Integrated Design Environment (IDE) provides full support for mixed-signal hardware design and firmware development using PSoC. Throughout this application note, various modifications and extensions to the power supervisor solution were suggested. In addition to those ideas, PSoC can:

- Manage analog and digital power converters together from a single power supervisor device
- Integrate other functions such as I^2C multiplexers, expanders etc.
- Support EEPROM fault and event logging
- Integrate thermal management (temperature sensing and fan control)

To explore these or any other ideas, contact your local Cypress sales representative to discuss options.

10 Conclusion

By working through all of the hand-on exercises in this application note, you will have gained a good understanding of the PSoC 3 Power Supervisor solutions.

The unique ability of the PSoC architecture to combine custom digital logic, analog signal chains and an MCU in a single device enables power system designers to develop high-performance, high-reliability power supervisor solutions.

This architecture also enables you to integrate many external fixed-function ASSPs such as I^2C multiplexers, reset supervisors, EEPROMs, and analog comparators. This powerful integration capability not only reduces BOM cost, but also results in PCB board layouts that are less congested and more reliable.

A Appendix A: PSoC® 3 12+1 Power Supervisor Solution User Guide

A.1 Functional Description

The PSoC® 3 12+1 Power Supervisor is a highly configurable solution capable of controlling and monitoring up to 12 secondary power rails and monitoring one (referred to as “+1”) primary input power source. This 12+1 power supervisor solution features voltage sequencing, fault detection, trimming, and margining, and measures voltages and load currents using a highly accurate 12-bit, differential Delta-Sigma ADC. It includes fast hardware window comparators with user-programmable over-voltage (OV) and under-voltage (UV) thresholds, PWM-based control voltage generation for high precision active trimming and four-corner margin testing during system development and manufacturing. The solution can interface to an external supervisor or host controller using the industry standard PMBus™ protocol.

The PSoC 3 12+1 Power Supervisor solution is built on Cypress’s PSoC programmable, mixed-signal system-on-chip architecture that combines a microcontroller unit, flash, SRAM and EEPROM memories, as well as analog and digital peripherals. Due its programmable architecture, this pre-configured solution enables system architects and engineers the unique capability to develop a fully-customized power supervisor solution in a matter of days. Fault logging EEPROM, integrated I^2C multiplexers, field upgradability, temperature sensing and fan control are just a few examples of functions and features that can be added to this solution. Please contact your local Cypress sales representative for more information.

This solution is designed to run on the CY8C3666AXI-036 PSoC 3 device.

A.2 Features

- Complete power supervisor solution supporting up to 12 secondary power rails and one primary input power source
- Programmable power supply sequencing engine
  - Complex time and event based sequencing for up to 12 secondary power rails
  - Sequencing time delays programmable from 250 µs—16.384 s
  - High-speed (< 25 ns) faulty rail shutdown
  - Automatic re-sequencing capability on any or all rails
  - User-definable rail groups
- Voltage and current measurement of all 13 rails
  - 12-bit Delta-Sigma ADC
  - 0.3% voltage and current measurement accuracy
  - Programmable early warning under-voltage, over-voltage and over-current thresholds for all rails
  - All rail voltages and currents sampled every 2.5 ms
  - Built-in automatic self-calibration
- High-speed hardware window comparator over-/under-voltage fault detection
  - 26 µs fault response time
  - Programmable under-voltage and over-voltage fault thresholds for each rail
  - Programmable glitch filtering up to 6.6 ms in 26 µs steps
- High-precision active trimming for all 12 secondary rails
  - Built-in auto-trim algorithm
  - Real-time power supply feedback adjustment
  - 0.6% trim accuracy

- Run-time re-configurable to support manufacturing test and margining

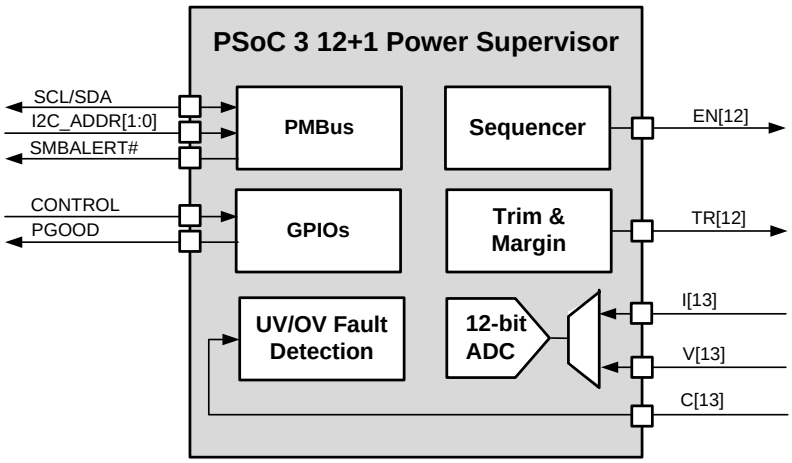
- Configurable analog and digital I/O architecture
  - 1.8—5.5 V I/O interface voltages
  - Up to four independent domains
- User-configurable warning and fault interrupts through SMBALERT# pin
- PMBus Communications interface with graphical configuration tool
- -40°C to +85°C industrial temperature
- 100-pin TQFP package

A.3 Applications

- Telecommunications and Networking Equipment
- Servers and Storage Systems
- Industrial / ATE
- Embedded Computing

A.4 Block Diagram

Figure 36. PSoC 3 12+1 Power Supervisor Solution Block Diagram



A.5 Configurable Parameters

- Hardware configurable I2C base address
- Nominal power converter rail voltages
- Over-voltage (OV) and under-voltage (UV) warning and fault thresholds
- Margin high and margin low voltages
- Over-current (OC) fault thresholds
- Voltage and current offset control
- Power up sequencing pre-requisites, sequence delays, power good thresholds, and rail timeouts

- Power down sequencing delays, timeouts, and power rail groups
- Automatic re-sequencing re-try counts, and re-try delay
- Manual or automatic active trim/margin with individual enable and disable

A.6 Electrical Specifications

A.6.1 Absolute Maximum Ratings

Table 16. Absolute Maximum Ratings DC Specifications

Parameter	Description	Conditions	Min	Max	Units
T_{STG}	Storage temperature	Higher storage temperatures reduce NVL data retention time. Recommended storage temperature is +25°C ±25°C. Extended duration storage temperatures above 85°C degrade reliability	-55	100	°C
V_{DDA}	Analog supply voltage relative to V_{SSA}		-0.5	6	V
V_{DDD}	Digital supply voltage relative to V_{SSD}		-0.5	6	V
V_{DDIO}	I/O supply voltage relative to V_{SSD}		-0.5	6	V
V_{SSA}	Analog ground voltage		V_{SSD}-0.5	V_{SSD}+0.5	V
V_{GPIO}	DC input voltage on GPIO[a]	Includes signals sourced by V_{DDA} and routed internal to the pin	V_{SSD}-0.5	V_{DDIO}+0.5	V
V_{GPIO}	DC input voltage on SIO	Output disabled	V_{SSD}-0.5	7	V
		Output enabled	V_{SSD}-0.5	6	V
V_{SSA}	Analog ground voltage		V_{SSD}-0.5	V_{SSD}+0.5	V
I_{VDDIO}	Current per V_{DDIO} supply pin		-	100	mA
I_{diode}	Current through protection diode to V_{DDIO} and V_{SSIO}		-	100	µA
LU	Latch up current[b]		-140	140	mA
ESD_{HBM}	Electrostatic discharge voltage	Human body model	750	-	V
ESD_{CDM}	Electrostatic discharge voltage	Charge device model	500	-	V

Note:

Usage above the absolute maximum conditions listed in Table 16 may cause permanent damage to the device. Exposure to maximum conditions for extended periods of time may affect device reliability. When used below maximum conditions but above normal operating conditions the device may not operate to specification.

[a] The V_{DDIO} supply voltage must be greater than the maximum analog voltage on the associated GPIO pins. Maximum analog voltage on GPIO pin ≤ V_{DDIO} ≤
[b] Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch-up Test

A.7 Device Level Specifications

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted, where T_A and T_J are ambient and junction temperature respectively. Specifications are valid for V_{DDA} = 4.5—5.5 V, except where noted.

A.7.1 AC/DC Specifications

Table 17. DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDD}, V_{DDA}, V_{DDIOx}	Digital, analog, and I/O supply voltages[a]		3.0	-	5.5	V
I_{DDD} + I_{DDA}	Digital and analog supply current[b]	V_{DDD} = V_{DDA} = 5 V T = 25 °C.	-	30	38	mA

Table 18. AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
S_{VDD}	V_{DD} ramp rate		-	-	1	V/ns
T_{IO_INIT}	Time from V_{DDD}/V_{DDA}/V_{CCD}/V_{CCA} ≥ 1.8V to I/O ports set to their reset states		-	-	10	µs
$T_{STARTUP}$	Time from V_{DDD}/V_{DDA} ≥ 4.5 V until sequencing is possible		-	110	-	ms

A.7.2 Inputs and Outputs

Specifications are valid for –40°C ≤ TA ≤ 85°C and TJ ≤ 100°C, except where noted. Specifications are valid for V_{DDA} 4.5—5.5 V, except where noted.

Table 19. Digital Input/Output DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input voltage high threshold	CMOS Input	0.7xV_{DDIO}	-	-	V
V_{IL}	Input voltage low threshold	CMOS Input	.	-	0.3xV_{DDIO}	V
V_{OH}	Output voltage high	I_{OH} = 4 mA at 3.3 V_{DDIO}	V_{DDIO}-0.6	-	-	V
		I_{OH} = 1 mA at 1.8 V_{DDIO}	V_{DDIO}-0.5	-	-	V
V_{OL}	Output voltage low	I_{OL} = 8 mA at 3.3 V_{DDIO}	-	-	0.6	V
		I_{OL} = 4 mA at 1.8 V_{DDIO}	-	-	0.6	V
R_{pullup}	Pull-up resistor[c]		3.5	5.6	8.5	kΩ
$R_{pulldown}$	Pull-down resistor[c]		3.5	5.6	8.5	kΩ
I_L	Input leakage current (absolute value)[d]	25°C V_{DDIO} = 3.0V	-	-	2	nA
C_{IN}	Input capacitance[d]		-	4	7	pF
I_{diode}	Current through protection diode to V_{DDIO} and V_{SSIO}		-	-	100	µA

[a] When operating with power supplies below 5 V, the ADC range is limited to approximately V_{DDA}-0.7 V. Scale power converter voltage inputs accordingly to measure them with the ADC
[b] Note that I_{DDIO} currents vary by application and are therefore excluded here
[c] Optional internal resistors are available on each output pin
[d] Based on device characterization (not production tested)

Figure 37. Digital Output High Voltage and Current

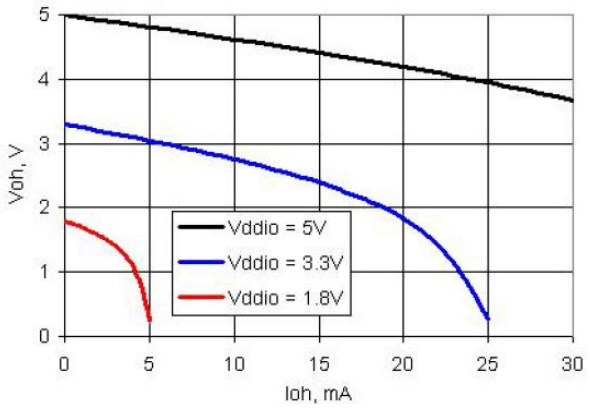


Figure 38. Digital Output Low Voltage and Current

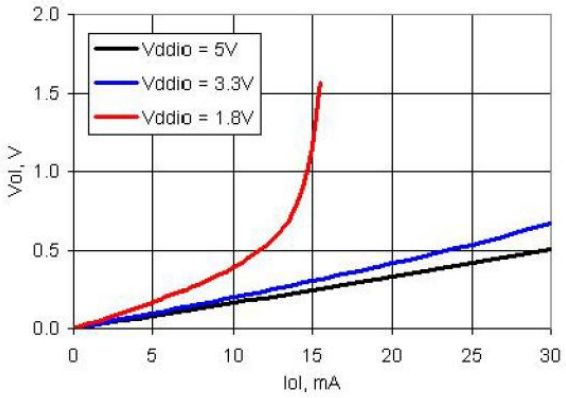
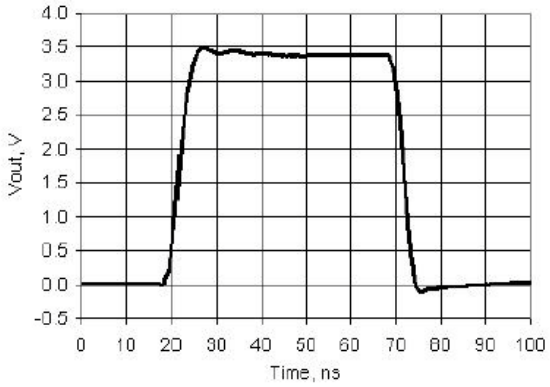


Table 20. I/O AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RISE}	Rise time, Fast Strong Drive[a]	3.3V V_{DDIO} C_{LOAD}=25 pF	.	-	12	ns
T_{FALL}	Fall time, Fast Strong Drive[a]	3.3V V_{DDIO} C_{LOAD}=25 pF	.	-	12	ns

Figure 39. Output Rise and Fall Times, Fast Strong Mode, VDDIO = 3.3 V, 25 pF Load



A.8 Analog to Digital Converter System Level Specifications

Table 21. ADC System Level Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		-	12	-	bits
	Monotonic	Yes	-	-	-	-
R_{IN_BUF}	ADC input resistance	Input buffer enabled	10	-	-	MΩ
	General input voltage range		V_{SSA}	-	V_{DDA}	V
	High ADC range	Single-ended input	0	-	4	V
	Low ADC range	Differential input	-128	-	+128	mV
	Low ADC range	Differential input	-64	-	+64	mV
INL12	Integral non linearity[a]	Range = ±1.024 V	-	-	±1	LSB
DNL12	Differential non linearity	Range = ±1.024 V	-	-	±1	LSB
	ADC voltage conversion time[b]	2.048 V ± 2.048 V scale	-	54	-	µs
	ADC current conversion time	± 64 mV scale	-	110	-	µs
	ADC reconfiguration time[b]	Switching between voltage and current measurement	-	135	-	µs
	ADC scan time	12+1 voltage and current measurements	-	2500	-	µs
	Signal to noise ratio, 12-bit, internal reference	Range = ±1.024 V, un-buffered	66	-	-	dB
G_E	ADC Gain Error	uncompensated, 25°C	-	-	±0.2	%
G_D	ADC Gain Drift	uncompensated	-	-	50	ppm/°C
V_{OS}	ADC Input Offset	uncompensated, 25°C	-	-	±0.1	mV
TCV_{OS}	Temperature coefficient, input offset voltage		-	-	55	µV/°C
	V_{REF} total variation[c]	-40°C to +85°C	-	-	±0.39	%
	Calibrated ADC system error[d]	-40°C to +85°C, Vin 1.0V	-	0.3	-	%

[a] Based on device characterization (not production tested)
[b] All ADC times assume the ADC ISR is not pre-empted by a higher priority ISR and CPUCLK = 40 MHz
[c] After 1000 hours of operation, based on device characterization (not production tested)
[d] Includes V_{REF}, input buffer, and ADC errors remaining after periodic run-time calibration; excludes error from optional external components

A.9 Window Comparator OV/UV Fault Detect System Level Specifications

Table 22. Window Comparator OV/UV Fault Detect Specifications[a]

Parameter	Description	Conditions	Min	Typ	Max	Units
	DAC resolution for thresholds		-	8	-	bits
	DAC output voltage, code = 255		-	1.02	-	V
	DAC settling time to 0.1%, step 25% to 75%	C_{LOAD} = 15 pF	-	0.45	1	µs
INL1	DAC INL (un-calibrated)	2.5 bits for 8-bit VDAC	-	-	1	%
E_G	DAC Gain error (un-calibrated)	25ºC	-	-	±2.5	%
TC_E_G	Un-calibrated DAC gain temperature coefficient		-	-	0.03	%FSR/°C
	Comparator offset		-	-	10	mV
	Absolute accuracy[b]	+25 ºC ±60ºC, no calibration	-	-	6.3	%
	Cumulative error	Run-time calibration	-	1.5	-	%
	Power Good detect time		-	13	26	µs
	Power Fail detect time, 12+1 rails	glitch filter = 0 samples	-	31	45	µs
		glitch filter = 8 samples	-	237	252	µs
	Power Fail glitch filter	26 µs / count	0	-	255	counts
	Window Comparator update rate		-	500	-	ksps

A.10 Voltage Sequencer Specifications

Table 23. Voltage Sequencer Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Adjustable timer resolution	Unless otherwise noted	-	250	-	µs
$VS_{TOnDelay}$	TON_Delay accuracy	Configured for 10 ms	-0	-	+300	µs
VS_{TOnMax}	TON_Max accuracy	Configured for 50 ms	-0	-	+30	µs
VS_{TOffHw}	Delay between PGood loss and Enable de-assertion of faulty rail		-	13	25	ns
$VS_{TOffFaultImmed}$	Accuracy in the delay between PGood loss and Enable de-assertion of a non-faulty rail in the same rail group	Group rails set to immediate (hard) shutdown	-	-	25	µs[c]
$VS_{TOffSoft}$	Accuracy in the delay between PGood loss and Enable de-assertion of a non-faulty rail in the same rail group	Group rails set to 10 ms soft shutdown	-	-	300	µs
$VS_{ToffMax}$	TOFF_MAX_WARN_LIMIT accuracy	Rail decays to ≤ 12.5% of nominal voltage	-	10	-	ms
$VS_{ReseqDelay}$	Accuracy in delay between fault shutdown complete and re-sequencing begins (if enabled)	Configured for 100 ms Adjustment units: 8 ms	+8	-	+20	ms
$VS_{ReseqRange}$	Range for re-sequence delay		0.008	-	524	sec
	Number of Restart Attempts		0	-	30[d]	

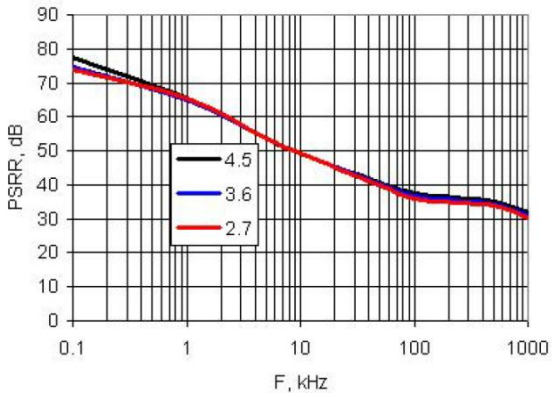
[a] Rail voltages are normalized below 1 V as necessary with an external resistor-divider circuit
[b] When measuring a 1 V scaled signal
[c] Assumes no higher priority interrupt intervenes
[d] A setting of 31 is a special case and gives ∞ attempts

A.11 Trim and Margin Specifications

Table 24. Voltage Trim and Margin Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Number of PWM outputs		-	-	12	-
PWM_{PSRR}	PSRR PWM DAC	Using internal regulated V_{CCD}	See Figure 40			dB
	Trim update rate[a]	User adjustable	0.1	-	10	sec
	Margin update rate[b]	User adjustable	10	-	500	ms
	Trim and Margin Accuracy		-	0.6	-	%

Figure 40. VCCD Digital Regulator PSSR vs. Frequency and VDDD



[a] Trim update rate refers to the rate (in seconds) that the PWM duty cycle is adjusted by 1 count
[b] Margin update rate refers to the rate (in seconds) that the PWM duty cycle is adjusted by 1 count

A.12 PMBus Interface Specifications

The I^2C slave interface runs at 100 kbps. It will reset and release the SDA and SCL lines if it detects the SCL clock held low for > 25 ms (SMBus $T_{TIMEOUT}$ parameter). The optional PMBus CONTROL pin is supported. Details are described in Standard PMBus Commands.

I^2C data transfers follow the format shown in Figure 41. After the START condition, a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) – 0 indicates a transmission (WRITE), and 1 indicates a request for data (READ). A data transfer is always terminated by a STOP condition generated by the master. However, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such a transfer.

Figure 41. I²C Complete Transfer Timing

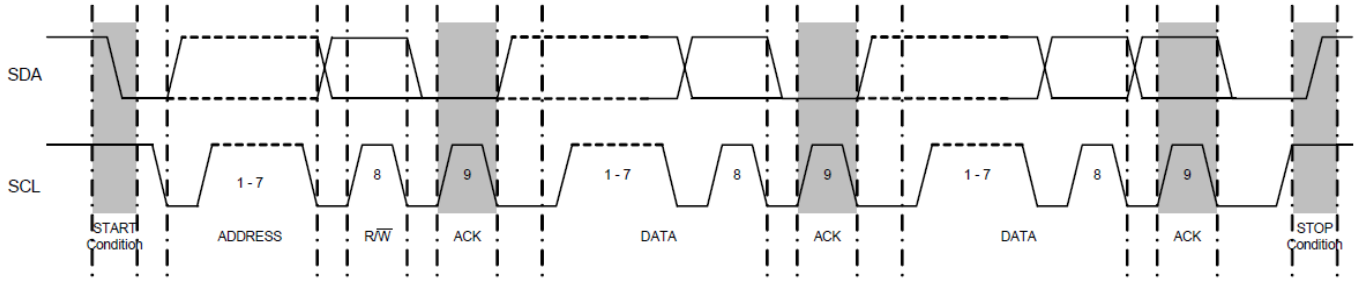


Table 25: I²C Selectable Base Address Settings

I2C ADDR1	I2C ADDR0	7-bit I²C Base Address	
		Hexadecimal	Decimal
High	High	0x5C	92
High	Low	0x5D	93
Low	High	0x5E	94
Low	Low	0x5F	95

A.13 PMBus Data Formats

The PMBus Specification defines two formats for command parameters that must be expressed as floating point numbers. The two formats are LINEAR and DIRECT. All of the PSoC 3 12+1 Power Supervisor solution's floating point parameters are stored in the LINEAR format. Depending on the command, there are two different variants of the LINEAR format, LINEAR11 and LINEAR16. In Standard PMBus Commands, the summary for each command indicates which of the two formats is used.

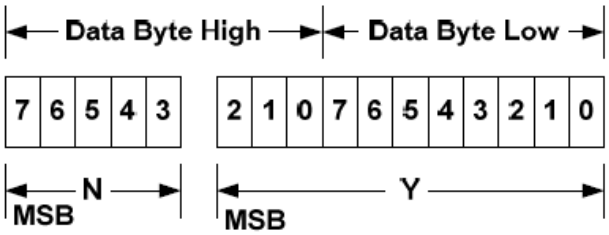
A.13.1 LINEAR11 Format

In the PMBus Specification, LINEAR11 is referred to as "Linear Data Format". The "11" comes from the fact that the mantissa portion of the LINEAR11 format is 11-bits long.

The LINEAR11 data format shown in Figure 42 is a 2-byte value:

- An 11-bit, two's complement mantissa
- A 5-bit, two's complement exponent (scaling factor)

Figure 42. LINEAR11 Format Exponent and Mantissa



The relation between Y, N and the "real world" Value is:

$$Value = Y \times 2^{N}$$

Where:

Value is the “real world” value
Y is an 11-bit, two’s complement integer
N is a 5-bit, two’s complement integer

A.13.2 LINEAR16 Format

In the PMBus Specification LINEAR16 is referred to as “LINEAR Format for Output Voltage and Voltage Related Parameters”. The “16” comes from the fact that the mantissa portion is 16-bits long.

LINEAR16 encode/decode uses values from two different PMBus commands. The 16-bit mantissa comes from the actual command, for example, READ_VOUT to read a rail voltage. The exponent comes from the VOUT_MODE command. See *VOUT_MODE (0x20), R/W Byte, Paged* for more details.

A.14 Standard PMBus Commands

This section describes the supported PMBus commands. Each description includes the PMBus command code, the protocol type, and the scope (paged or common). Commands take effect immediately except where noted otherwise. When a command takes effect at the next reset event, the description includes the reset type: power-on reset, hardware reset using the XRES# pin, or software reset as a result of a watchdog timeout.

A.14.1 PAGE (0x00), R/W Byte, Common

The PAGE command provides the ability to configure, control, and monitor multiple logical units using one physical I^2C address. In the case of the PSoC 3 12+1 Power Supervisor, the page is a zero-based rail index. This means that all parameters related to Rail 1 are located on page 0, Rail 2 on page 1, and so on. Once the PMBus host sets the desired page, all subsequent PMBus commands apply to the parameter set associated with that page. The page setting remains in effect until changed via a subsequent PAGE command. PMBus commands that are not page specific are known as common commands.

Setting PAGE to 0xFF specifies “All Rails” mode. This is a standard PMBus value and indicates that the following commands should apply to all rails. The only valid command for All Rails mode in the PSoC Power Supervisor solution is OPERATION (0x01). Valid values for PAGE are 0—12 and 255. If PAGE is set to an invalid value, the PSoC 3 12+1 Power Supervisor will NAK any subsequent commands until PAGE is set to a valid value.

A.14.2 OPERATION (0x01), R/W Byte, Paged

The OPERATION command is used to turn the unit on and off in conjunction with the CONTROL pin. It is also used to cause the unit to set the output voltage to the upper or lower MARGIN VOLTAGEs. The unit stays in the commanded operating mode until a subsequent OPERATION command or change in the state of the CONTROL pin instructs the device to change to another mode. The ON_OFF_CONFIG setting determines whether the OPERATION command is capable of turning a rail On and Off.

Table 26. OPERATION Command Bit Definitions

Bits [7:6]	Bits [5:4]	Bits [3:2]	Bits [1:0]	Unit On Or Off	Margin State
0	XX	XX	XX	Immediate	N/A
1	XX	XX	XX	Soft Off	N/A
10	0	XX	XX	On	Off
10	1	1	XX	On	Margin Low (Ignore Fault)
10	1	10	XX	On	Margin Low (Act On Fault)
10	10	1	XX	On	Margin High (Ignore Fault)
10	10	10	XX	On	Margin High (Act On Fault)

Note The PSoC 3 Power does not support the Ignore Fault Margin Low/High OPERATION commands. The user must ensure that the fault and warning limits for the margined rail are outside of the margin voltage while margining.

Table 27. OPERATION Command Values Supported

OPERATION Mode	Value	Description
OPERATION_OFF_IMED	0x00	Turn the rail OFF with no delay
OPERATION_OFF_SOFT	0x40	Turn the rail OFF after TOFF_DELAY
OPERATION_ON	0x80	Turn the rail ON and return to nominal voltage from margined voltage.
OPERATION_MARG_LO	0x94	Set the rail voltage to VOUT_MARGIN_LOW
OPERATION_MARG_HI	0xA4	Set the rail voltage to VOUT_MARGIN_HIGH
ALL Others	Invalid	Invalid - Ignore

The PMBus ON_OFF_CONFIG command affects the behavior of the OPERATION command. OPERATION On/Off support must be enabled in the ON_OFF_CONFIG setting, otherwise OPERATION On and Off commands will have no effect. The exception to this is the OPERATION_ON command which is used to return from MARGIN mode to normal operation regardless of the ON_OFF_CONFIG setting.

OPERATION is a command and not a state. OPERATION retains the last value written to it and may not reflect the actual state of the associated rail. For example, reading the OPERATION command for a rail that has faulted may report OPERATION_ON even though the rail is physically in the OFF state due to the fault.

The manufacturer specific command OPERATION_DEFAULT (described in OPERATION_DEFAULT (0xD7), R/W Byte, Paged) determines the value of OPERATION command at Power Supervisor reset. This default is used once at start-up to set the initial On/Off state of each rail (assuming the OPERATION_ON command is enabled by ON_OFF_CONFIG).

A.14.3 ON_OFF_CONFIG (0x02), R/W Byte, Common

The ON_OFF_CONFIG command defines how the CONTROL pin input and serial bus commands (specifically OPERATION) work together to turn the unit on and off. This includes how the unit responds when power is applied.

Table 28 shows the ON_OFF_CONFIG command bit definitions from the PMBus Specification:

Table 28. ON_OFF_CONFIG Command Bit Definitions

Bit	Purpose	Value	Meaning
[7:5]	Reserved	0	Reserved For Future Use
4	Sets the default to either operate any time power is present or for the on/off to be controlled by CONTROL pin and serial bus commands	0	Unit powers up any time power is present regardless of state of the CONTROL pin
		1	Unit does not power up until commanded by the CONTROL pin and OPERATION command (as programmed in bits [3:0]).
3	Controls how the unit responds to commands received via the serial bus	0	Unit ignores the on/off portion of the OPERATION command from serial bus
		1	To start, the unit requires that that the on/off portion of the OPERATION command is instructing the unit to run. Depending on bit [2], the unit may also require the CONTROL pin to be asserted for the unit to start and energize the output.
2	Controls how the unit responds to the CONTROL pin	0	Unit ignores the CONTROL pin (on/off controlled only the OPERATION command)
		1	Unit requires the CONTROL pin to be asserted to start the unit. Depending on bit [3], the OPERATION command may also be required to instruct the device to start before the output is energized.
1	Polarity of the CONTROL pin	0	Active low (Pull pin low to start the unit)
		1	Active high (Pull high to start the unit)
0	CONTROL pin action when commanding the unit to turn off	0	Use the programmed turn off delay (Section 16.5) and fall time (Section 16.6)
		1	Turn off the output and stop transferring energy to the output as fast as possible. The device's product literature shall specify whether or not the device sinks current to decrease the output voltage fall time.

Table 29 describes the ON_OFF_CONFIG command in simpler terms.

Table 29. ON_OFF_CONFIG Command Summary

Bit	Description	Description
4	Auto Mode	0: Auto On Mode – Power Supervisor powers up all rails (rail pre-requisites still apply) at system reset. The CONTROL pin and OPERATION On/Off commands are disabled. All other bits ignored 1: Controlled On Mode – On/Off is controlled by the CONTROL pin and/or OPERATION command (As determined by the other bits)
3	OPERATION Command Enable	0: Power Supervisor ignores the OPERATION On/Off commands 1: Power Supervisor responds to the OPERATION On/Off commands
2	CONTROL Pin Enable	0: Power Supervisor ignores the CONTROL pin for turning rails On/Off (bits 1:0 do not matter) 1: CONTROL pin turns rails On/Off (configured by bits 1:0)
1	CONTROL Pin Polarity	0: CONTROL pin is active high 1: CONTROL pin is active low
0	CONTROL Pin Off Mode	0: CONTROL Off triggers Soft Off (sequenced/TOFF_DELAY) 1: CONTROL Off triggers Immediate Off

Note If Auto On Mode is enabled (ON_OFF_CONFIG bit 4 = 0) on the PSoC 3 12+1 Power Supervisor there is no way to turn ON a rail that has transitioned to the OFF state. For example, if a faulty rail has been automatically re-sequenced the maximum number of times without success, Auto On Mode will disable both the CONTROL pin and OPERATION command. To avoid this situation, enable the OPERATION command (ON_OFF_CONFIG bit 4=1, bit 3=1) and set the OPERATION_DEFAULT command to OPERATION_ON for all rails instead of enabling Auto On Mode.

A.14.4 CLEAR_FAULTS (0x03), Write Only, Common

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously and causes the PSoC 3 12+1 Power Supervisor to de-assert its SMBALERT# signal. The CLEAR_FAULTS command does not have any effect on rails that may have been turned OFF in response to faults being cleared.

If a fault is still present when the associated bit is cleared, the fault bit will immediately be set again. For example, if the UV warning bit in the STATUS_VOUT register for Rail 1 is set, CLEAR_FAULTS will clear it and de-assert SMBALERT#. However, if the UV condition persists on Rail 1, the PSoC 3 12+1 Power Supervisor will immediately set the UV warning bit in the STATUS_VOUT register.

Asserting CLEAR_FAULTS clears the following:

- STATUS_BYTE
- STATUS_WORD
- STATUS_VOUT
- STATUS_IOUT
- STATUS_CML

A.14.5 STORE_DEFAULT_ALL (0x11), Send Byte (Dataless), Common

The STORE_DEFAULT_ALL command instructs the PSoC 3 12+1 Power Supervisor to copy the entire contents of the PMBus Register Store from RAM to non-volatile memory. The Register Store contains all of the PMBus register values. After being stored in non-volatile memory via the STORE_DEFAULT_ALL command, this new Register Store becomes the default initialization source for the PMBus registers at subsequent power-up. In this way, the PSoC 3 12+1 Power Supervisor can be configured with user-defined PMBus default settings. This command is write-only.

The host should not send any additional PMBus commands to the PSoC 3 12+1 Power Supervisor for at least 250 ms after sending the STORE_DEFAULT_ALL command. During the write to non-volatile memory, the PSoC 3 12+1 Power Supervisor may not meet SMBus I^2C timing requirements. This is allowed by the PMBus Specification.

A.14.6 RESTORE_DEFAULT_ALL (0x12), Send Byte (Dataless), Common

The RESTORE_DEFAULT_ALL command instructs the PSoC 3 12+1 Power Supervisor to restore the original factory default PMBus register settings. It replaces the register settings in the non-volatile Register Store (created by STORE_DEFAULT_ALL) and performs a software reset. This command should be used to replace any user-defined custom register settings and return to the original factory default settings. This command is write-only.

Note This command's behavior differs from the PMBus Specification. The PMBus Specification version restores the Operating Memory Register Store from the non-volatile Register Store (created by STORE_DEFAULT_ALL). The PSoC 3 12+1 Power Supervisor version **deletes** the non-volatile version of the Register Store and resets the part.

The host should not send any additional PMBus commands to the PSoC 3 12+1 Power Supervisor for at least 350 ms after sending the RESTORE_DEFAULT_ALL command. This delay is necessary to allow for the non-volatile memory update and the software reset. This is allowed by the PMBus Specification.

A.14.7 CAPABILITY (0x19), Read-Only Byte, Common

The CAPABILITY command provides a way for the host system to determine key capabilities of the PSoC 3 12+1 Power Supervisor. This is a Read-Only command. The PSoC 3 12+1 Power Supervisor's response to this command is always 0x10, as described in Table 30:

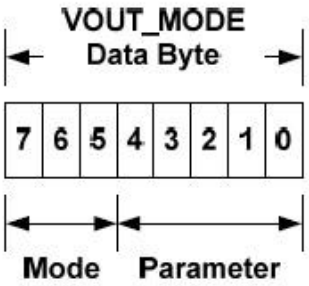
Table 30. CAPABILITY Response

Bit	Description	PSoC 3 12+1 Power Supervisor Value
7	Packet Error Checking	0 = Packet Error Checking Not Supported
6:5	Maximum Bus Speed	00 = Maximum Bus Speed is 100 kHz
4	SMBALERT#	1 = SMBALERT# Pin Supported
3:0	Reserved	000

A.14.8 VOUT_MODE (0x20), R/W Byte, Paged

The VOUT_MODE command is used to set the data format for PMBus commands that express rail voltages. Its format is shown in Figure 43.

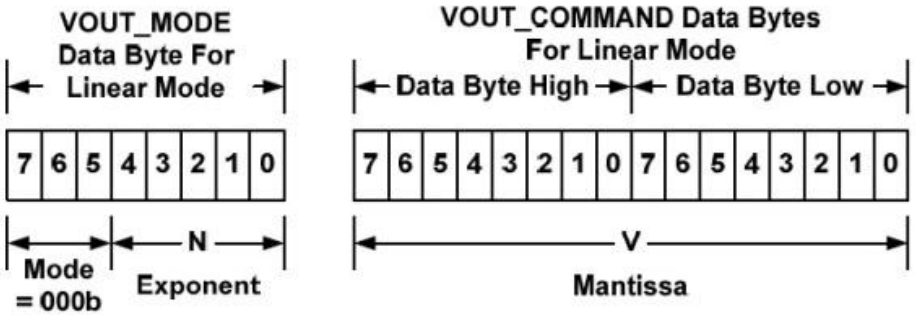
Figure 43. VOUT_MODE Encoding



PMBus supports several different data formats, which are specified in the Mode bits of the VOUT_MODE command. All rail voltages are expressed in the LINEAR16 format which has a Mode value of 000b. Any values written to the Mode bits are assumed to be 000b. This means that these bits are treated as "don't care" by the PSoC 3 Power Supervisor.

The Parameter portion of the VOUT_MODE command contains a 5-bit two's complement integer. This value becomes the exponent used to convert all 16-bit voltage commands/registers to fractional volts. The VOUT_COMMAND is an example of a voltage command. The VOUT_COMMAND is stored as an unsigned 16-bit mantissa as shown in Figure 44.

Figure 44. VOUT_MODE Exponent and Mantissa



To convert the VOUT_COMMAND value to actual fractional volts, the mantissa is combined with the value stored in VOUT_MODE as shown in Equation 13.

Equation 13

$$Voltage = V \times 2^{N}$$

All voltage commands for a single rail share a single VOUT_MODE value. Typically, the PMBus host determines the ideal exponent value based on the range of the voltage and sets VOUT_MODE to this value. All commands that are dependent on VOUT_MODE must be updated to reflect the new exponent value whenever VOUT_MODE is updated.

The following PSoC 3 12+1 Power Supervisor PMBus commands are stored in LINEAR16 format:

- VOUT_COMMAND
- VOUT_MARGIN_HIGH
- VOUT_MARGIN_LOW
- VOUT_OV_FAULT_LIMIT
- VOUT_OV_WARN_LIMIT
- VOUT_UV_WARN_LIMIT
- VOUT_UV_FAULT_LIMIT
- POWER_GOOD_ON

A.14.9 VOUT_COMMAND (0x21), R/W Word (LINEAR16 Volts), Paged

VOUT_COMMAND is used to set the nominal output voltage of a rail. The nominal voltage serves as the target voltage when trimming is enabled. The nominal voltage is also used to calculate the Power-Off threshold (12.5% of nominal voltage) when powering down rails.

This command does not take effect immediately. If it is stored in non-volatile memory it will take effect at the next reset event.

A.14.10 VOUT_CAL_OFFSET (0x23), R/W Word (INT16 mV), Paged

The VOUT_CAL_OFFSET command is used to nullify any known, fixed offsets in the voltage measurements. The offset is applied to internal voltage measurements, so not only is the offset reflected in the reported voltage readings, but the adjusted voltage is also used in warning and fault detection.

VOUT_CAL_OFFSET is a signed, 16-bit integer in mV.

This command has an immediate effect on voltage measurements read through the READ_VOUT command. It will not take effect on warning or fault thresholds until either new VOUT_UV_WARN_LIMIT, VOUT_OV_WARN_LIMIT, VOUT_UV_FAULT_LIMIT or VOUT_OV_FAULT_LIMIT commands are received or the next reset event (provided the settings were stored in non-volatile Register Store using STORE_DEFAULT_ALL).

A.14.11 VOUT_MARGIN_HIGH (0x25), R/W Word (LINEAR16 Volts), Paged

The VOUT_MARGIN_HIGH command defines the output voltage when the OPERATION command is set to Margin High. This command only stores the value. The OPERATION command is required to initiate margining.

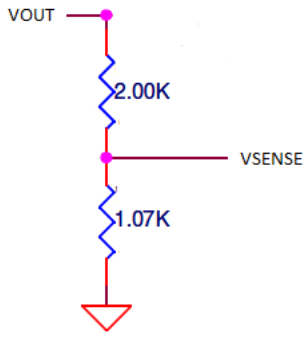
A.14.12 VOUT_MARGIN_LOW (0x26), R/W Word (LINEAR16 Volts), Paged

The VOUT_MARGIN_LOW command defines the output voltage when the OPERATION command is set to Margin Low. This command only stores the value. The OPERATION command is required to initiate margining.

A.14.13 VOUT_SCALE_MONITOR (0x2A), R/W Word (LINEAR11), Paged

The VOUT_SCALE_MONITOR command is used to specify the external scaling applied to the voltage rail that is being monitored. Any voltage that exceeds either the ADC range or the power supply of the PSoC 3 12+1 Power Supervisor is sensed through a resistive voltage divider. Figure 45 shows an example of a resistive voltage divider where VOUT is the voltage to be monitored, and VSENSE is the scaled measurement voltage that is connected to the analog input pin of PSoC.

Figure 45. VOUT_SCALE_MONITOR Example



In this example, the correct value for VOUT_SCALE_MONITOR would be:

$$\text{VOUT\_SCALE\_MONITOR} = \frac{1.07\ k\Omega}{(2.00\ k\Omega + 1.07\ k\Omega)} = 0.349$$

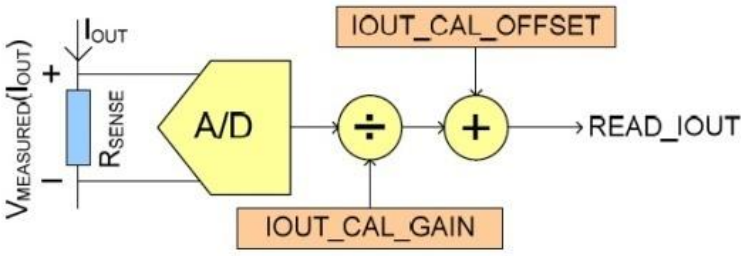
VOUT_SCALE_MONITOR applies to the ADC voltage inputs of the PSoC 3 12+1 Power Supervisor. The OV/UV fault detection block typically uses different scaling factors for voltage inputs, so there is a separate manufacturer specific PMBus command (VOUT_SCALE_MONITOR_FAULT) to specify the scaling factor for the OV/UV fault detection block voltage inputs.

This command has an immediate effect on voltage measurements read through the READ_VOUT command. It will not take effect on warning thresholds until either new VOUT_UV_WARN_LIMIT or VOUT_OV_WARN_LIMIT commands are received or the next reset event (provided the settings were stored in non-volatile Register Store using STORE_DEFAULT_ALL).

A.14.14 IOUT_CAL_GAIN (0x38), R/W Word (LINEAR11 mΩ), Paged

The IOUT_CAL_GAIN command is used to set the ratio of the voltage measured by PSoC at the current sense input pins to the sensed current. When sensing current directly across a series shunt resistor, IOUT_CAL_GAIN is simply the value of the sense resistor. When sensing current with a current sense amplifier (CSA), IOUT_CAL_GAIN should be set to the value of the sense resistor multiplied by the CSA voltage gain. Figure 46 shows how the IOUT_CAL_GAIN value is applied when converting measured voltage to current.

Figure 46. IOUT_CAL_GAIN Parameter



This command has an immediate effect on current measurements read through the READ_IOUT command. It will not take effect on the over-current fault threshold until either a new IOUT_OC_FAULT_LIMIT command is received or the next reset event (provided the settings were stored in non-volatile Register Store using STORE_DEFAULT_ALL).

A.14.15 IOUT_CAL_OFFSET (0x39), R/W Word (LINEAR11 Amps), Paged

The IOUT_CAL_OFFSET is used to nullify any known, fixed offsets in the output current sensing circuit. This command is used in conjunction with the IOUT_CAL_GAIN command to minimize the error of the current sensing circuit.

This command has an immediate effect on current measurements read through the READ_IOUT command. It will not take effect on the over-current fault threshold until either a new IOUT_OC_FAULT_LIMIT command is received or the next reset event (provided the settings were stored in non-volatile Register Store using STORE_DEFAULT_ALL).

A.14.16 VOUT_OV_FAULT_LIMIT (0x40), R/W Word (LINEAR16 Volts), Paged

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage for a rail that causes an OV fault. In response to an OV fault, the PSoC 3 12+1 Power Supervisor will:

- Set the VOUT_OV_FAULT bit in the STATUS_BYTE
- Set the VOUT bit in the STATUS_WORD
- Set the VOUT_OV_FAULT bit in the STATUS_VOUT register
- Assert the SMBALERT# pin
- Disable the output
- Perform group shutdown and re-sequencing as configured

A.14.17 VOUT_OV_WARN_LIMIT (0x42), R/W Word (LINEAR16 Volts), Paged

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage for a rail that causes an OV warning. This value is typically less than the OV threshold. In response to an OV warning, the PSoC 3 12+1 Power Supervisor will:

- Set the NONE OF THE ABOVE bit in the STATUS_BYTE
- Set the VOUT bit in the STATUS_WORD
- Set the VOUT_OV_WARNING bit in the STATUS_VOUT register
- Assert the SMBALERT# pin

A.14.18 VOUT_UV_WARN_LIMIT (0x43), R/W Word (LINEAR16 Volts), Paged

The VOUT_UV_WARN_LIMIT command sets the value of the output voltage for a rail that causes a UV warning. This value is typically greater than the output UV fault threshold. In response to a UV warning, the PSoC 3 12+1 Power Supervisor will:

- Set the NONE OF THE ABOVE bit in the STATUS_BYTE
- Set the VOUT bit in the STATUS_WORD
- Set the VOUT_UV_WARNING bit in the STATUS_VOUT register
- Assert the SMBALERT# pin

A.14.19 VOUT_UV_FAULT_LIMIT (0x44), R/W Word (LINEAR16 Volts), Paged

The VOUT_UV_FAULT_LIMIT command sets the value of the output voltage for a rail that causes a UV fault. This fault is masked until the unit reaches the programmed output voltage (POWER_GOOD_ON). This fault is also masked when the rail is disabled. In response to a UV fault, the PSoC 3 12+1 Power Supervisor will:

- Set the VOUT bit in the STATUS_WORD
- Set the VOUT_UV_FAULT bit in the STATUS_VOUT register
- Assert the SMBALERT# pin
- Disable the output
- Perform group shutdown and re-sequencing as configured

A.14.20 IOUT_OC_FAULT_LIMIT (0x46), R/W Word (LINEAR11 Amps), Paged

The IOUT_OC_FAULT_LIMIT command sets the value of the output current that causes the over-current detector to indicate an over-current fault condition. In response to an over-current fault, the PSoC 3 12+1 Power Supervisor will:

- Set the IOUT_OC_FAULT bit in the STATUS_BYTE
- Set the IOUT bit in the STATUS_WORD
- Set the IOUT_OC_FAULT bit in the STATUS_IOUT register
- Assert the SMBALERT# pin
- Disable the output
- Perform group shutdown and re-sequencing as configured

A.14.21 POWER_GOOD_ON (0x5E), R/W Word (LINEAR16 Volts), Paged

The POWER_GOOD_ON command sets the voltage at which a rail is determined to be “good” during power-up sequencing. POWER_GOOD_ON should be set to less than the nominal voltage (the VOUT_COMMAND voltage) because some rails function as expected without ever reaching the nominal voltage. POWER_GOOD_ON should be set to a value greater than the UV warning and fault thresholds to guarantee that the power-on voltage has ramped beyond those thresholds. If the POWER_GOOD_ON value is equal to VOUT_UV_WARN_LIMIT, a warning may be triggered just as the rail transitioned to operational mode.

POWER_GOOD_ON is only used during sequencing to define when a rail transitions from power-up ramp to operational mode.

Note This is a different usage than the one defined by the PMBus Specification.

This command does not take effect immediately. It will not take effect on until either a new SEQUENCE_DBG command is received or the next reset event (provided the settings were stored in non-volatile Register Store using STORE_DEFAULT_ALL).

A.14.22 TON_DELAY (0x60), R/W Word (LINEAR11 ms), Paged

The TON_DELAY command sets the time, in ms, between when a start condition is received and when the rail voltage output is enabled by the sequencer. A start condition occurs when a rail is in the pending ON state and all of the rail's pre-requisites (rail and CTL signal pre-requisites) are satisfied.

Valid values are 0—16383. The maximum ON delay is approximately 16 seconds.

This command does not take effect immediately. It will not take effect on until either a new SEQUENCE_DBG command is received or the next reset event (provided the settings were stored in non-volatile Register Store using STORE_DEFAULT_ALL).

A.14.23 TON_MAX_FAULT_LIMIT (0x62), R/W Word (LINEAR11 ms), Paged

The TON_MAX_FAULT_LIMIT command sets the upper limit, in ms, for how long the PSoC 3 12+1 Power Supervisor can attempt to power up a rail without reaching the voltage specified by the POWER_GOOD_ON command.

Valid values are 0—16383. Setting the value to 0 means that there is no limit, and the PSoC 3 12+1 Power Supervisor can attempt to bring up the rail indefinitely. The maximum ON timeout is approximately 16 seconds.

Note This is a slightly different usage than the one defined by the PMBus Specification which uses VOUT_UV_FAULT_LIMIT as the target voltage rather than POWER_GOOD_ON.

This command does not take effect immediately. It will not take effect on until either a new SEQUENCE_DBG command is received or the next reset event (provided the settings were stored in non-volatile Register Store using STORE_DEFAULT_ALL).

A.14.24 TOFF_DELAY (0x64), R/W Word (LINEAR11 ms), Paged

The TOFF_DELAY sets the time, in ms, between when a stop condition is received and when the PSoC 3 12+1 Power Supervisor disables the rail voltage output. A stop condition could be the result of an OPERATION OFF command, the CONTROL pin, or a fault on another rail.

TOFF_DELAY is only used for Soft m shutdown. During a Hard Off shutdown the rail output voltage is disabled as soon as a stop condition is received. Whether a shutdown is Soft Off or Hard Off depends on the source of the stop condition. There are different versions of the OPERATION command to specify Hard/Soft Off. When using the CONTROL pin, Hard/Soft Off is selected via a bit in the ON_OFF_CONFIG command. For the various fault response shutdowns the selection of Hard/Soft Off is determined by the associated manufacturer specific xxx_FAULT_RESEQ_CFG command.

Valid values are 0—16383. The maximum OFF Delay time is approximately 16 seconds.

This command does not take effect immediately. It will not take effect on until either a new SEQUENCE_DBG command is received or the next reset event (provided the settings were stored in non-volatile Register Store using STORE_DEFAULT_ALL).

A.14.25 TOFF_MAX_WARN_LIMIT (0x66), R/W Word (LINEAR11 ms), Paged

The TON_MAX_WARN_LIMIT command sets an upper limit, in ms, for how long the PSoC 3 12+1 Power Supervisor can attempt to power down a rail without reaching 12.5% of the output voltage programmed at the time the rail is turned off (the current value of VOUT_COMMAND).

Valid values are 0—16383. Setting the value to 0 means that there is no limit, and the PSoC 3 12+1 Power Supervisor waits indefinitely for the output voltage to decay. The maximum power down timeout is approximately 16 seconds.

Failure to power down within the timeout period is considered a warning condition. In response to the TOFF_MAX_WARN_LIMIT being exceeded, the PSoC 3 12+1 Power Supervisor will:

- Set the NONE OF THE ABOVE bit in the STATUS_BYTE
- Set the VOUT bit is the upper byte of the STATUS_WORD
- Set the TOFF_MAX Warning bit in the STATUS_VOUT register
- Assert the SMBALERT# pin

This command does not take effect immediately. It will not take effect on until either a new SEQUENCE_DBG command is received or the next reset event (provided the settings were stored in non-volatile Register Store using STORE_DEFAULT_ALL).

A.14.26 STATUS_BYTE (0x78), R/W Byte, Common

The STATUS_BYTE command returns one byte of information that summarize the most critical faults. See the individual FAULT and WARN commands to see which events set bits in this register.

Table 31. STATUS_BYTE Format

Bit	Status Bit Name	Meaning
7	BUSY	Not Supported
6	OFF	Not Supported
5	VOUT_OV_FAULT	An output over-voltage fault has occurred
4	IOUT_OC_FAULT	An output over-current fault has occurred
3	VIN_UV_FAULT	Not Supported
2	TEMPERATURE	Not Supported
1	CML	A communications, memory or logic fault has occurred
0	NONE OF THE ABOVE	A fault or warning not listed in bits [7:1] has occurred

Even though STATUS_BYTE is writeable, it is effectively read-only since its value is constantly updated as a logical OR of the bits in the lower level status registers. Any value written will be quickly replaced.

A.14.27 STATUS_WORD (0x79), R/W Word, Common

The STATUS_WORD command returns two bytes of information that summarize the PSoC 3 12+1 Power Supervisor's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. See the individual FAULT and WARN commands to see which events set bits in this register.

The low byte of the STATUS_WORD is the same register as the STATUS_BYTE command shown in Table 31. The high byte of the STATUS_WORD is shown in Table 32.

Table 32. STATUS_WORD Format

Byte	Bit	Status Bit Name	Meaning
High	7	VOUT	An output voltage fault or warning has occurred
	6	IOUT/POUT	An output current or output power fault or warning has occurred
	5	INPUT	Not Supported
	4	MFR_SPECIFIC	Used to indicate that a CTL pin de-assert has caused a fault
	3	POWER_ GOOD#	Not Supported
	2	FANS	Not Supported
	1	OTHER	Not Supported
	0	UNKNOWN	Not Supported

Even though STATUS_WORD is writeable, it is effectively Read-only since its value is constantly updated as a logical OR of the bits in the lower level status registers. Any value written will be quickly replaced.

A.15 STATUS_xxx Commands

The following behaviors apply to all of the STATUS_xxx commands:

- Status bits are sticky. Status bits will remain set until cleared even after the condition that caused the bit-set has passed. For example, after an OV warning, the VOUT_OV_WARNING bit for the associated rail will remain set even after the rail voltage has returned to nominal.
- Individual status bits are cleared by writing a 1 to the corresponding bit of the STATUS_xxx command. For example, to clear the lower 4-bits of a status register, write 0x0F. Writing 0xFF will clear all bits.
- If the fault or warning condition that caused the status bit to be set is still present, the status bit will remain set after any clear.
- STATUS_VOUT and STATUS_IOUT are Paged allowing detailed status tracking for each rail in the system.

A.15.1 STATUS_VOUT (0x7A), R/W Byte, Paged

The STATUS_VOUT command returns output voltage status information for a single rail.

Table 33. STATUS_VOUT Format

Bit	Meaning
7	VOUT_OV_FAULT (Output Over-voltage Fault)
6	VOUT_OV_WARNING (Output Over-voltage Warning)
5	VOUT_UV_WARNING (Output Under-voltage Warning)
4	VOUT_UV_FAULT (Output Under-voltage Fault)
3	VOUT_MAX Warning – Not Supported
2	TON_MAX_FAULT (Power on timeout)
1	TOFF_MAX_WARNING (Power off timeout)

Bit	Meaning
0	VOUT Tracking Error – Not Supported

A.15.2 STATUS_IOUT (0x7B), R/W Byte, Paged

The STATUS_IOUT command returns output current status information for a single rail.

Table 34. STATUS_IOUT Format

Bit	Meaning
7	IOUT_OC_FAULT (Output Over-current Fault)
6	IOUT_OC_LV_FAULT – Not Supported
5	IOUT_OC_WARNING – Not Supported
4	IOUT_UC_FAULT – Not Supported
3	Current Share Fault – Not Supported
2	In Power Limiting Mode – Not Supported
1	POUT_OP_FAULT – Not Supported
0	POUT_OP_WARNING – Not Supported

A.15.3 STATUS_CML (0x7E), R/W Byte, Common

The STATUS_CML (Communications, Memory, and Logic) command returns status information related to the communications interface and protocol.

Table 35. STATUS_CML Format

Bit	Meaning
7	Invalid Or Unsupported Command Received
6	Invalid Or Unsupported Data Received
5	Packet Error Check Failed – Not Supported
4	Memory Fault Detected – Not Supported
3	Processor Fault Detected – Not Supported
2	Reserved
1	Fault other – Used to report a general communication/protocol error
0	Other Memory Or Logic Fault has occurred – Not supported

A.15.4 READ_VOUT (0x8B), R/W Word (LINEAR16 Volts), Paged

The READ_VOUT command returns the measured output voltage of the selected rail. The returned voltage is the actual voltage, taking into account the external resistor divider (VOUT_SCALE_MONITOR) and any user-defined offset (VOUT_CAL_OFFSET).

READ_VOUT returns the 16-bit mantissa portion of the voltage. This must be combined with the exponent returned by the associated VOUT_MODE command to calculate the actual voltage. Although READ_VOUT is writeable, any value written to this command will be overwritten by actual measurements.

A.15.5 READ_IOUT (0x8C), R/W Word (LINEAR11 Amps), Paged

The READ_IOUT command returns the measured output current. The returned current is the actual current, taking into account the external sense resistor circuit (IOUT_CAL_GAIN) and any user–defined offset (IOUT_CAL_OFFSET).

Although READ_IOUT is writeable, any value written to this command will be overwritten by actual measurements.

A.15.6 PMBUS_REVISION (0x98), Read-Only Byte, Common

The PMBUS_REVISION command returns the revision of the PMBus to which the PSoC 3 12+1 Power Supervisor is compliant. The command has one data byte.

- Bits [7:4] indicate the revision of PMBus specification Part I to which the device is compliant.
- Bits [3:0] indicate the revision of PMBus specification Part II to which the device is compliant.

The PSoC 3 12+1 Power Supervisor returns 0x22 for the PMBUS_REVISION, indicating compliance with Revision 1.2 of Parts I and II of the PMBus Specification.

A.16 Inventory Information (MFR_xxx Commands)

The PMBus protocol provides commands for the storage and retrieval of the device manufacturer's inventory information. This information is stored as strings. SMBus block write and block read commands (SMBus specification, Version 2.0 [A03], Section 7.5.7) are used to write and retrieve inventory information. The block write and read commands require that the first data byte be the number of bytes to follow (Byte Count). All power supervisor manufacturer inventory information commands are fixed at 15-bytes in length. All Reads will return a Byte Count of 15 followed by 15-bytes of data. All Writes should have a Byte Count 15, followed by 15-bytes of data. The user must pad short strings to the fill the full 15-bytes.

Manufacturer's inventory information is always loaded using one byte text (ISO/IEC 8859-1 [A05]) characters.

A.16.1 MFR_ID (0x99), R/W Block[15+1], Common

The MFR_ID command is used to either set or read the manufacturer's ID (name, abbreviation or symbol that identifies the unit's manufacturer). Each manufacturer chooses their identifier. The PSoC 3 12+1 Power Supervisor returns the string: "Cypress Semicon".

A.16.2 MFR_MODEL (0x9A), R/W Block[15+1], Common

The MFR_MODEL command is used to either set or read the manufacturer's model number. The PSoC 3 12+1 Power Supervisor returns the string: "12+1 Power Spvr".

A.16.3 MFR_REVISION (0x9B), R/W Block[15+1], Common

The MFR_REVISION command is used to either set or read the manufacturer's revision number. Each manufacturer uses the format of their choice for the revision number. The PSoC 3 12+1 Power Supervisor returns a string with the current revision such as: "039 v1.0".

A.16.4 MFR_LOCATION (0x9C), R/W Block[15+1], Common

The MFR_REVISION command is used to either set or read the manufacturing location of the device. Each manufacturer uses the format of their choice for the location information. The PSoC 3 12+1 Power Supervisor returns the string: "San Diego, CA".

A.16.5 MFR_DATE (0x9D), R/W Block[15+1], Common

The MFR_DATE command is used to either set `or read the date the device was manufactured. While each manufacturer uses the format of their choice for the revision number, the recommended MFR_DATE format is YYMMDD (padded) where Y, M and D are integer values from 0 to 9, inclusive. MFR_DATE is typically only set once, at the time of manufacture. The PSoC 3 12+1 Power Supervisor returns the string: "120701".

A.16.6 MFR_SERIAL (0x9E), R/W Block[15+1], Common

The MFR_SERIAL command is used to either set or read the manufacturer's serial number of the device. Each manufacturer uses the format of their choice for the serial number. The PSoC 3 12+1 Power Supervisor returns the string: "No Serial Num".

A.17 Manufacturer Specific PMBus Commands

A.17.1 Fault Re-sequence Configuration Commands

When the PSoC 3 12+1 Power Supervisor powers down a rail because of a fault, it can be configured to automatically re-sequence that rail after a programmable delay according to the rail's power on pre-requisites and timing parameters. When re-sequencing is enabled, the faulty rail and all of the rails in the same group assume the same re-sequence settings as the faulty rail. Re-sequencing is configured on a per-rail and per-fault-type basis. For example, Rail 1 can be set to re-sequence after an OV fault while Rail 2 can be set to turn off and not re-sequence after an OV fault.

Fault re-sequence configuration is done with the xxx_RESEQ_CFG commands. There is a command for each type of fault, and the command is paged so it can be set for each rail. The xxx_RESEQ_CFG commands also determine if the non-faulty rails in the group will power down in Hard (immediately) or Soft (after their individual TOFF_DELAYs) mode.

All of the xxx_RESEQ_CFG commands are R/W Bytes with the format shown in Table 36.

Table 36. RESEQ_CFG Format

Bit	Name	Description	
7:6	Reserved	Set to zero	
5	Soft Shutdown	0	Non-faulty rails in the group use Soft shutdown as defined by their individual TOFF_DELAY time settings
		1	Non-faulty rails in the group use Hard shutdown (immediately)
4:0	Re-sequence Count	0	Do not re-sequence
		1—30	Re-sequence count. Attempt to re-sequence up to this many times
		31	Infinite re-sequencing

The re-sequence configuration interacts closely with two other commands discussed in this guide: TRESEQ_DELAY and TSYS_STABLE. TRESEQ_DELAY sets the time to delay after powering down a faulted rail (and its slaves) before re-sequencing. TSYS_STABLE sets the system stable time. Once re-sequencing occurs the system is assumed to be “stable” if TSYS_STABLE time elapses without any faults. When this occurs, the PSoC 3 12+1 Power Supervisor will reset the re-sequence “allowance” for all rails.

The following are the re-sequence configuration commands for the various fault types:

A.17.2 VOUT_OV_FAULT_RESEQ_CFG (0xD0), R/W Byte, Paged

The VOUT_OV_FAULT_RESEQ_CFG command sets the re-sequence configuration for OV faults.

A.17.3 VOUT_UV_FAULT_RESEQ_CFG (0xD1), R/W Byte, Paged

The VOUT_UV_FAULT_RESEQ_CFG command sets the re-sequence configuration for UV faults.

A.17.4 IOUT_OC_FAULT_RESEQ_CFG (0xD2), R/W Byte, Paged

The IOUT_OC_FAULT_RESEQ_CFG command sets the re-sequence configuration for OC faults.

A.17.5 TON_MAX_FAULT_RESEQ_CFG (0xD3), R/W Byte, Paged

The TON_MAX_FAULT_RESEQ_CFG command sets the re-sequence configuration for power on timeout faults. This fault occurs when a rail does not reach POWER_GOOD_ON voltage within TON_MAX_FAULT_LIMIT.

A.17.6 CTRL_PIN_FAULT_RESEQ_CFG (0xD4), R/W Byte, Paged

The CTRL_PIN_FAULT_RESEQ_CFG command sets the re-sequence configuration for CTL pin faults. A CTRL pin fault occurs when a CTL pin de-asserts. This command is Paged, however, this command can only be accessed on the first six pages, since there are only six CTL pins.

A.17.7 TSYS_STABLE (0xD5), R/W Unsigned Word (ms), Common

The TSYS_STABLE command sets the amount of time, in ms, which all rails must remain powered up before the system is considered “stable”. This time is used to reset the rail re-sequence allowance.

Valid values are 0—262000. The maximum system stable time is approximately 262 seconds.

This command does not take effect immediately. It will not take effect on until either a new SEQUENCE_DBG command is received or the next reset event (provided the settings were stored in non-volatile Register Store using STORE_DEFAULT_ALL).

A.17.8 TRESEQ_DELAY (0xD6), R/W Unsigned Word (ms), Common

The TRESEQ_DELAY command sets the amount of time, in ms, that the sequencer will wait before attempting to re-sequence a rail or set of rails.

Valid values are 0—262000. The maximum re-sequence delay is approximately 262 seconds.

This command does not take effect immediately. It will not take effect on until either a new SEQUENCE_DBG command is received or the next reset event (provided the settings were stored in non-volatile Register Store using STORE_DEFAULT_ALL).

A.17.9 OPERATION_DEFAULT (0xD7), R/W Byte, Paged

The OPERATION_DEFAULT command sets a default value for the standard PMBus OPERATION command. The value in OPERATION_DEFAULT is only used once at power up, so it must be committed to non-volatile memory to have any effect.

In addition to setting the default OPERATION value, The PSoC 3 12+1 Power Supervisor will also set the initial rail state based on the OPERATION_DEFAULT value. In other words, during initialization, the PSoC 3 12+1 Power Supervisor treats the OPERATION_DEFAULT value as though it were an OPERATION command sent from the PMBus host.

The only valid OPERATION_DEFAULT values are On and Off. OPERATION margining commands are invalid and will be treated as Off. The allowed OPERATION_DEFAULT values are shown in Table 37.

Table 37. OPERATION_DEFAULT Format

OPERATION Mode	Value	Description
OPERATION_OFF_IMMED	0x00	Initial Rail State is OFF
OPERATION_ON	0x80	Initial Rail State is ON

A.17.10 STATUS_CTL_FAULT (0xDA), R/W Byte, Common

The STATUS_CTL_FAULT returns the status of faults caused by CTL pin de-asserts. This is a manufacturer specific command similar to the PMBus standard STATUS_xxx commands, and has all of the same properties discussed in the STATUS_xxx commands section (sticky, Write '1' to clear, etc).

Table 38. STS_CTL_FAULT Format

Bit	Description
7:6	Reserved
5	CTL6 has caused a fault
4	CTL5 has caused a fault
3	CTL4 has caused a fault
2	CTL3 has caused a fault
1	CTL2 has caused a fault
0	CTL1 has caused a fault

A.17.11 READ_CTL (0xDB), R/W Byte, Common

The READ_CTL command returns the current state of the six CTL inputs. The CTL states are returned as a bitmap:

Table 39. STS_CTL_FAULT Format

Bit	Description
7:6	Reserved
5	CTL 6 - 1: High, 0: Low
4	CTL 5 - 1: High, 0: Low
3	CTL 4 - 1: High, 0: Low
2	CTL 3 - 1: High, 0: Low
1	CTL 2 - 1: High, 0: Low
0	CTL 1 - 1: High, 0: Low

A.17.12 VOUT_SCALE_MONITOR_FAULT (0xE0), R/W Word (LINEAR11), Paged

The VOUT_SCALE_MONITOR_FAULT command is used to specify any external scaling applied to a voltage rail that is being monitored by the OV/UV fault detector. Otherwise, this parameter is identical to the VOUT_SCALE_MONITOR. A separate command is required because the PSoC 3 12+1 Power Supervisor has separate voltage inputs for voltage measurement (ADC) and OV/UV fault detection. Even if the scaling is identical for both inputs, the scaling value must be entered using both commands. See VOUT_SCALE_MONITOR (0x2A), R/W Word (LINEAR11), Paged for more details on this command.

This command does not take effect immediately. It will not take effect on fault thresholds until either new VOUT_UV_FAULT_LIMIT or VOUT_OV_FAULT_LIMIT commands are received or the next reset event (provided the settings were stored in non-volatile Register Store using STORE_DEFAULT_ALL).

A.17.13 TRIM_PWM_PRERUN (0xE1), R/W Word (LINEAR11), Paged

The TRIM_PWM_PRERUN command is used to specify the duty cycle to be applied to the trim/margin PWM when the rail is turned off. This pre-run duty cycle charges the filter capacitor so that when the power converter is turned on by the sequencer, the output voltage does not over shoot.

This command does not take effect immediately. It will not take effect on until either a new SEQUENCE_DBG command is received or the next reset event (provided the settings were stored in non-volatile Register Store using STORE_DEFAULT_ALL).

A.17.14 TRIM_PWM_RUN (0xE2), R/W Word (LINEAR11), Paged

The TRIM_PWM_RUN command is used to specify the duty cycle to be applied to the trim/margin PWM when the rail is turned on and set for nominal output voltage. It is used as the starting point for the active trim algorithm.

This command does not take effect immediately. It will not take effect on until either a new SEQUENCE_DBG command is received or the next reset event (provided the settings were stored in non-volatile Register Store using STORE_DEFAULT_ALL).

A.17.15 CY_TEST_REG (0xE3), R/W Byte, Common

The CY_TEST_REG command enables users to access internal digital signals for debug, validation, and characterization purposes. The selected signal is routed to the SMBALERT# pin. The default value for this command is 0x00, which correctly routes the SMBALERT# signal to the SMBALERT# pin.

Table 40. CY_TEST_REG Multiplexer Options

Bit	Encoding	Description
7:5	All zeros	Reserved. Write with all zeroes
4:0	0	SMBALERT#
	1	Rail 1 Power Good as determined by the ADC
	2	Rail 2 Power Good as determined by the ADC
	3	Rail 3 Power Good as determined by the ADC
	4	Rail 4 Power Good as determined by the ADC
	5	Rail 5 Power Good as determined by the ADC
	6	Rail 6 Power Good as determined by the ADC
	7	Rail 7 Power Good as determined by the ADC
	8	Rail 8 Power Good as determined by the ADC
	9	Rail 9 Power Good as determined by the ADC
	10	Rail 10 Power Good as determined by the ADC
	11	Rail 11 Power Good as determined by the ADC
	12	OV/UV Fault Detector input mux enable for Rail 12
	13	OV/UV Fault Detector input mux enable for Rail 13
	14	Sequencer Control Pin 0

Bit	Encoding	Description
	15	Sequencer Control Pin 1
	16	Heartbeat signal. Gets pulsed at a regular rate to indicate firmware is running properly
	17	Rail 1 Power Good as determined by the OV/UV Fault Detector
	18	Rail 2 Power Good as determined by the OV/UV Fault Detector
	19	Rail 3 Power Good as determined by the OV/UV Fault Detector
	20	Rail 4 Power Good as determined by the OV/UV Fault Detector
	21	Rail 5 Power Good as determined by the OV/UV Fault Detector
	22	Rail 6 Power Good as determined by the OV/UV Fault Detector
	23	Rail 7 Power Good as determined by the OV/UV Fault Detector
	24	Rail 8 Power Good as determined by the OV/UV Fault Detector
	25	Rail 9 Power Good as determined by the OV/UV Fault Detector
	26	Rail 10 Power Good as determined by the OV/UV Fault Detector
	27	Rail 11 Power Good as determined by the OV/UV Fault Detector
	28	Rail 12 Power Good as determined by the OV/UV Fault Detector
	29	Rail 13 Power Good as determined by the OV/UV Fault Detector
	30	Reserved
	31	ADC end-of-conversion signal. Indicates ADC sample rate

A.17.16 GLITCH_FILTER (0xE4), R/W Byte, Common

The GLITCH_FILTER command sets the number of steps of the OV/UV fault detector glitch filter.

Valid values are 0—255. Each step is 26 µs.

A.17.17 SEQ_RAIL_PREREQ (0xE5), R/W Word (Rail Bitmask), Paged

The SEQ_RAIL_PREREQ command sets the PGood pre-requisites required for the selected rail to power up. The SEQ_RAIL_PREREQ value is a bitmask where bit 0 = Rail 1, bit 1 = Rail 2, etc. Setting a bit to 1 indicates that the associated rail must be in the PGood State before the rail selected by the Page number can power up.

Valid values are 0x0000—0x1FFF. Some examples are shown below.

- SEQ_RAIL_PREREQ[0] = 0x0000 Rail 1 has no pre-requisites
- SEQ_RAIL_PREREQ[1] = 0x0001 Rail 2's pre-requisite is Rail 1
- SEQ_RAIL_PREREQ[2] = 0x0003 Rail 3's pre-requisites are Rail 1 and Rail 2
- SEQ_RAIL_PREREQ[3] = 0x0007 Rail 4's pre-requisites are Rail 1,Rail 2,and Rail 3
- SEQ_RAIL_PREREQ[4] = 0x000F Rail 5's pre-requisites are Rail 1, Rail 2, Rail 3, and Rail 4

A rail may not have itself as a pre-requisite (e.g.. SEQ_RAIL_PREREQ[0] = 0x0001) otherwise the rail will never power up. Also, rails may not have each other as pre-requisites as this would result in deadlock.

This command does not take effect immediately. It will not take effect on until either a new SEQUENCE_DBG command is received or the next reset event (provided the settings were stored in non-volatile Register Store using STORE_DEFAULT_ALL).

A.17.18 SEQ_CTRL_PREREQ (0xE7), R/W Word (Control Bitmask), Paged

The SEQ_CTRL_PREREQ command sets the CTL pin pre-requisites required for the selected Rail to power up. The SEQ_CTRL_PREREQ mask that specifies which CTL pins must be asserted before the rail can power up.

Valid values are 0x00—0x3F. Some examples are shown below.

- SEQ_CTRL_PREREQ[0] = 0x01 Rail 1's pre-requisite is CTL1
- SEQ_CTRL_PREREQ[1] = 0x02 Rail 2's pre-requisite is CTL2
- SEQ_CTRL_PREREQ[2] = 0x03 Rail 3's pre-requisites are CTL1 and CTL2
- SEQ_CTRL_PREREQ[3] = 0x00 Rail 4 has no CTL pin pre-requisites

This command does not take effect immediately. It will not take effect on until either a new SEQUENCE_DBG command is received or the next reset event (provided the settings were stored in non-volatile Register Store using STORE_DEFAULT_ALL).

A.17.19 FAULT_GROUP_RAILS (0xE9), R/W Word (Rail Bitmask), Paged

The FAULT_GROUP_RAILS command defines which operational rails will be shut down when a fault is detected on the rail indicated by the Page number. The rail set is specified as a bitmask where bit 0 = Rail 1, bit 1 = Rail 2, etc. Setting a bit to 1 indicates that the rail is in the fault group.

Whether to use Soft of Hard shutdown is determined by the xxx_FAULT_RESEQ_CFG command for the associated fault (OV, UV, OC, and power on timeout).

A.17.20 CTRL_GROUP_RAILS (0xEA), R/W Word (Rail Bitmask), Paged

The CTRL_GROUP_RAILS command defines which operational rails will be shut down when the CTL input indicated by the Page number is de-asserted. The rail set is specified as a bitmask where bit 0 = Rail 1, bit 1 = Rail 2, etc. Setting a bit to 1 indicates that the rail is in the fault group. Since there are only six CTL pins, this command only appears on Pages 0—5.

Whether to use Soft or Hard shutdown is determined by the CTRL_PIN_FAULT_RESEQ_CFG command.

A.17.21 MARGIN_TRIM_CFG (0xEB), R/W Byte, Paged

The MARGIN_TRIM_CFG command configures how the PSoC 3 12+1 Power Supervisor supports trimming and margining. Table 41 shows the valid values for this command:

Table 41. MARGIN_TRIM_CFG Format

Mode	Value	Description
MODE_NONE	0x00	PWM output is tri-stated. There is no trim or margin capability
MODE_MARGIN_ONLY	0x01	In normal operating mode (i.e. PMBus OPERATION mode is not Margin) the PWM pin is tri-stated. When margining is enabled, the PWM duty-cycle is driven and adjusted to reach the margin voltage.
MODE_BOTH	0x02	In normal operating mode (i.e. PMBus OPERATION mode is not Margin) active trimming is enabled to achieve the specified nominal voltage output. When margining is selected, active trimming change the voltage output to achieve the desired margin voltage target
MODE_FIXED_PWM	0x03	In normal operating mode (i.e. PMBus OPERATION mode is not Margin) the PWM duty cycle is fixed at the PWM_RUN duty cycle. When margining is enabled, the duty-cycle is adjusted to reach the margin voltage.
	Other	Reserved

This command does not take effect immediately. It will not take effect on until either a new SEQUENCE_DBG command is received or the next reset event (provided the settings were stored in non-volatile Register Store using STORE_DEFAULT_ALL).

A.17.22 SEQUENCER_STATUS (0xED), Read-Only Byte, Paged

The SEQUENCER_STATUS command is a debug command that returns the current internal sequencer state for the selected rail. Each rail is controlled by an independent state machine.

Table 42. SEQUENCER_STATUS Format

Value	State
0	SEQUENCER_STATE_OFF
1	SEQUENCER_STATE_TRESEQ_DELAY
2	SEQUENCER_STATE_PEND_ON
3	SEQUENCER_STATE_TON_DELAY
4	SEQUENCER_STATE_TOFF_MAX
5	SEQUENCER_STATE_PEND_RESEQ
6	SEQUENCER_STATE_TON_MAX
7	SEQUENCER_STATE_ON
8	SEQUENCER_STATE_TOFF_DELAY

A.17.23 SEQ_DBG_SEQ_CTL (0xF0), R/W Byte, Common

The SEQ_DBG_SEQ_CTL command is a debug command that allows the PMBus host to drive the internal CTL inputs.

Table 43. SEQ_DBG_SEQ_CTL Format

Bit	Description
7:6	Reserved
5	CTL6 (1: High, 0: Low)
4	CTL5 (1: High, 0: Low)
3	CTL4 (1: High, 0: Low)
2	CTL3 (1: High, 0: Low)
1	CTL2 (1: High, 0: Low)
0	CTL1 (1: High, 0: Low)

A.17.24 SEQUENCE_DBG (0xF3), Write-Only Byte, Common

The SEQUENCE_DBG is a debug command that will force all rails to toggle between power-up or power-down. If any rail is powered-up, this command will force all rails to power-down. If all rails are powered down, this command will force all rails to power-up. This is a useful command to use when developing complex sequencing. The one-byte payload is not used. Writing any value will cause this command to execute.

A.18 PMBus Command Summary

Table 44. Standard Supported PMBus Commands

Code	Command Name	Transaction Type	Format / Units	Scope	Description	Run-Time	Flash	GUI
0x00	PAGE	R/W Byte	Byte	Common	Output Rail Selection	Y		Y
0x01	OPERATION	R/W Byte	Byte	Page	Runtime Rail Control (Margin High/Low, etc.)	Y		Y
0x02	ON_OFF_CONFIG	R/W Byte	Byte	Common	Determines how the device responds to the CONTROL pin and OPERATION command	Y	Y	Y

Code	Command Name	Transaction Type	Format / Units	Scope	Description	Run-Time	Flash	GUI
0x03	CLEAR_FAULTS	Send Byte	n/a	Common	No Data - Clear all faults/status registers	Y		
0x11	STORE_DEFAULT_ALL	Send Byte	n/a	Common	No Data - Commit current configuration to flash	Y		Y
0x12	RESTORE_DEFAULT_ALL	Send Byte	n/a	Common	No Data - Replace current configuration with flash configuration	Y		
0x19	CAPABILITY	RO Byte	Byte	Common	PMBus CAPABILITY - Read Only	Y	Y	
0x20	VOUT_MODE	R/W Byte	Byte	Page	Numeric Format of VOUT commands	Y	Y	Y
0x21	VOUT_COMMAND	R/W Word	LINEAR 16 (V)	Page	Secondary side output voltage value	Y	Y	Y
0x23	VOUT_CAL_OFFSET	R/W Word	Signed Int16	Page	Voltage measurement fixed offset	Y	Y	Y
0x25	VOUT_MARGIN_HIGH	R/W Word	LINEAR 16 (V)	Page	Secondary side output voltage margin high value (enabled via OPERATION command)	Y	Y	Y
0x26	VOUT_MARGIN_LOW	R/W Word	LINEAR 16 (V)	Page	Secondary side output voltage margin low value (enabled via OPERATION command)	Y	Y	Y
0x2A	VOUT_SCALE_MONITOR	R/W Word	LINEAR 11 (V/V)	Page	External secondary side voltage divider ratio (ADC input - Warn/Voltage Measurements)	Y	Y	Y
0x38	IOUT_CAL_GAIN	R/W Word	LINEAR 11 (mΩ)	Page	V/I gain used for current measurements	Y	Y	
0x39	IOUT_CAL_OFFSET	R/W Word	LINEAR 11 (A)	Page	Current measurement fixed offset	Y	Y	Y
0x40	VOUT_OV_FAULT_LIMIT	R/W Word	LINEAR 16 (V)	Page	Secondary side over voltage fault limit	Y	Y	Y
0x42	VOUT_OV_WARN_LIMIT	R/W Word	LINEAR 16 (V)	Page	Secondary side over voltage warn limit	Y	Y	Y
0x43	VOUT_UV_WARN_LIMIT	R/W Word	LINEAR 16 (V)	Page	Secondary side under voltage warn limit	Y	Y	Y
0x44	VOUT_UV_FAULT_LIMIT	R/W Word	LINEAR 16 (V)	Page	Secondary side under voltage fault limit	Y	Y	Y
0x46	IOUT_OC_FAULT_LIMIT	R/W Word	LINEAR 11 (A)	Page	Secondary side over current fault limit	Y	Y	Y
0x5E	POWER_GOOD_ON	R/W Word	LINEAR 16 (V)	Page	Voltage level where a rail is determined to be good. Used only during power on sequencing	Y	Y	Y
0x60	TON_DELAY	R/W Word	LINEAR 11 (ms)	Page	Power on sequencing delay		Y	Y
0x62	TON_MAX_FAULT_LIMIT	R/W Word	LINEAR 11 (ms)	Page	Rail power up timeout		Y	Y
0x64	TOFF_DELAY	R/W Word	LINEAR 11 (ms)	Page	Power down sequencing delay		Y	Y
0x66	TOFF_MAX_WARN_LIMIT	R/W Word	LINEAR 11 (ms)	Page	Rail power down timeout		Y	Y
0x78	STATUS_BYTE	R/W Byte	Byte	Common	PMBus Status - per spec - Status summary	Y		

Code	Command Name	Transaction Type	Format / Units	Scope	Description	Run-Time	Flash	GUI
0x79	STATUS_WORD	R/W Word	Word	Common	PMBus Status - per spec - Status summary	Y		
0x7A	STATUS_VOUT	R/W Byte	Byte	Page	PMBus Status - per spec - Secondary side voltage warn/fault	Y		Y
0x7B	STATUS_IOUT	R/W Byte	Byte	Page	PMBus Status - per spec - Secondary side current warn/fault	Y		Y
0x7E	STATUS_CML	R/W Byte	Byte	Common	PMBus Status - per spec - PMBus protocol errors	Y		
0x8B	READ_VOUT	R/W Word	LINEAR 16 (V)	Page	Returns the measured Secondary Side Voltage	Y		Y
0x8C	READ_IOUT	R/W Word	LINEAR 11 (A)	Page	Returns the measured Secondary Side Current	Y		Y
0x98	PMBUS_REVISION	RO Byte	Byte	Common	PMBus revision		Y	
0x99	MFR_ID	R/W Block	String	Common	Manufacturer ID		Y	
0x9A	MFR_MODEL	R/W Block	String	Common	Manufacturer Model		Y	
0x9B	MFR_REVISION	R/W Block	String	Common	Manufacturer Revision		Y	
0x9C	MFR_LOCATION	R/W Block	String	Common	Manufacturer Location		Y	
0x9D	MFR_DATE	R/W Block	String	Common	Manufacturer Date		Y	
0x9E	MFR_SERIAL	R/W Block	String	Common	Manufacturer Serial No.		Y	

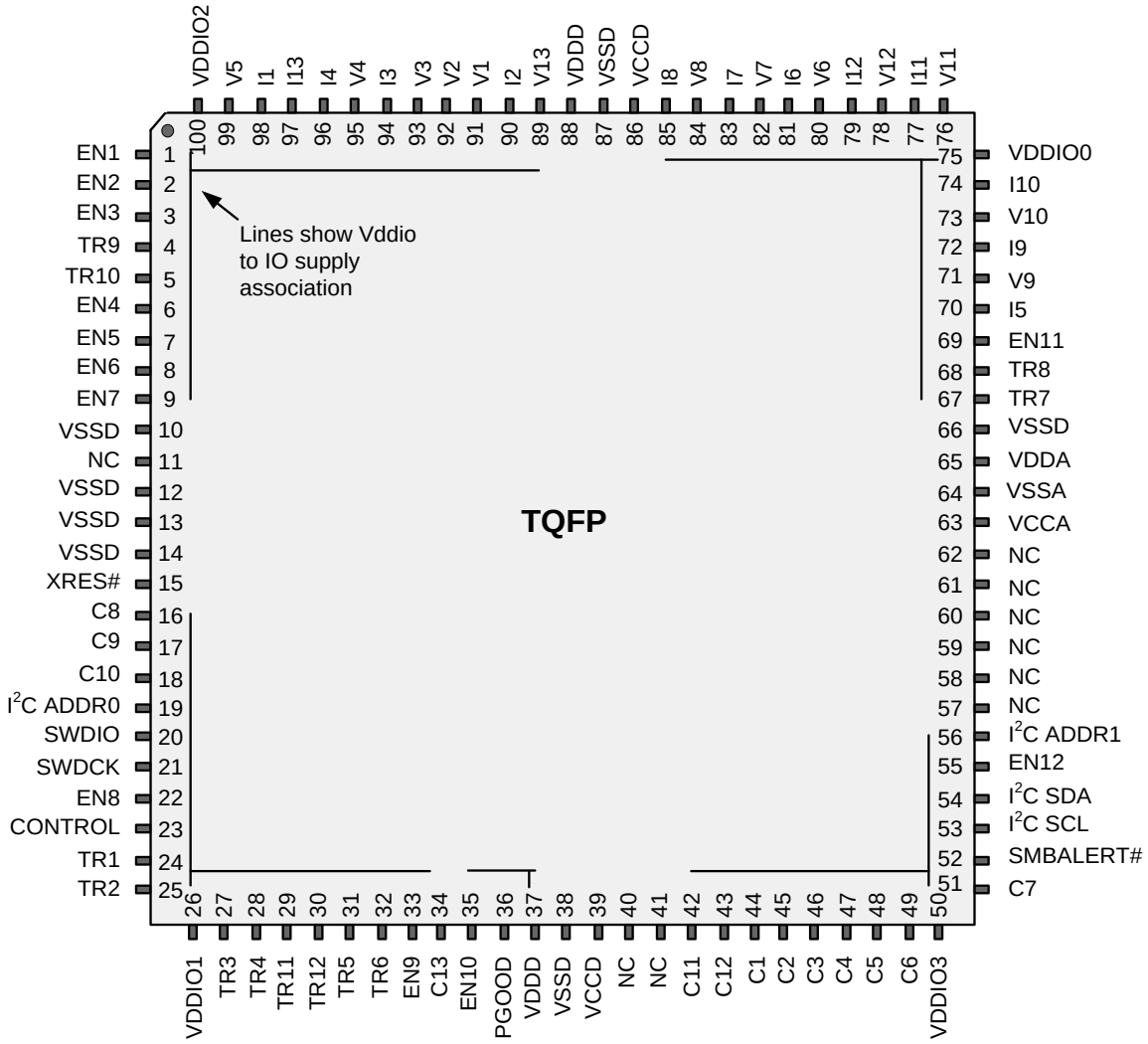
Table 45. Manufacturer Specific (Cypress Defined) PMBus Commands Supported

Code	Command Name	Transaction Type	Format / Units	Scope	Description	Runtime	Flash	GUI
0xD0	VOUT_OV_FAULT_RESEQ_CFG	R/W Byte	Byte (bitmask)	Page	Re-sequence count and shutdown type for OV faults	Y	Y	Y
0xD1	VOUT_UV_FAULT_RESEQ_CFG	R/W Byte	Byte (bitmask)	Page	Re-sequence count and shutdown type for UV faults	Y	Y	Y
0xD2	IOUT_OC_FAULT_RESEQ_CFG	R/W Byte	Byte (bitmask)	Page	Re-sequence count and shutdown type for OC faults	Y	Y	Y
0xD3	TON_MAX_FAULT_RESEQ_CFG	R/W Byte	Byte (bitmask)	Page	Re-sequence count and shutdown type for TON_MAX faults	Y	Y	Y
0xD4	CTL_PIN_FAULT_RESEQ_CFG	R/W Byte	Byte (bitmask)	Page	Re-sequence count and shutdown type for CTL pin de-assert	Y	Y	Y
0xD5	TSYS_STABLE	R/W Word	LINEAR11 (ms)	Common	System stable time	Y	Y	Y
0xD6	TRESEQ_DELAY	R/W Word	LINEAR11 (ms)	Common	Global re-sequence delay	Y	Y	Y

Code	Command Name	Transaction Type	Format / Units	Scope	Description	Runtime	Flash	GUI
0xD7	OPERATION_DEFAULT	R/W Byte	Byte	Page	Sets the default PMBus OPERATION state for each rail at Power On Reset		Y	Y
0xE0	VOUT_SCALE_MONITOR_FAULT	R/W Word	LINEAR11 (V/V)	Page	OV/UV fault detector input voltage scaling	Y	Y	Y
0xE1	TRIM_PWM_PRERUN	R/W Word	LINEAR11 (%)	Page	PWM duty cycle applied when rail is OFF		Y	
0xE2	TRIM_PWM_RUN	R/W Word	LINEAR11 (%)	Page	Initial PWM duty cycle used by the active trim algorithm once the regulator is enabled		Y	
0xE3	CY_TEST_REG	R/W Byte	Byte	Common	Test mux control	Y	Y	Y
0xE4	GLITCH_FILTER	R/W Byte	Byte	Common	Glitch filter setting for the OV/UV fault detect window comparator	Y	Y	
0xE5	SEQ_RAIL_PREREQ	R/W Word	Word (bitmask)	Page	Power up rail pre-requisites		Y	Y
0xE7	SEQ_CTRL_PREREQ	R/W Byte	Byte (bitmask)	Page	Power up CTL pre-requisites		Y	Y
0xE9	FAULT_GROUP_RAILS	R/W Word	Word (bitmask)	Page	Rails assigned to a power good failure fault group		Y	Y
0xEA	CTRL_GROUP_RAILS	R/W Byte	Byte (bitmask)	Page	Rails assigned to a CTL pin de-assert fault group		Y	Y
0xEB	MARGIN_TRIM_CFG	R/W Byte	Byte	Page	Trim/Margin mode	Y	Y	Y
0xF0	SEQ_DBG_SEQ_CTL	R/W Byte	Byte (bitmask)	Common	Drive internal CTL signals	Y		Y
0xF3	SEQUENCE_DBG	R/W Byte	Byte (bitmask)	Common	Force power-up/power-down	Y		Y

A.19 Pin Descriptions

Figure 47. 100-TQFP Package Pinout



Notes:
Any unused analog inputs should be connected to ground on the PCB

Table 46. Pin Descriptions

Pin	Name	Description
91	V1	Rail 1 voltage sense to ADC, scaled to below 4 Volts
92	V2	Rail 2 voltage sense to ADC, scaled to below 4 Volts
93	V3	Rail 3 voltage sense to ADC, scaled to below 4 Volts
95	V4	Rail 4 voltage sense to ADC, scaled to below 4 Volts
99	V5	Rail 5 voltage sense to ADC, scaled to below 4 Volts
80	V6	Rail 6 voltage sense to ADC, scaled to below 4 Volts
82	V7	Rail 7voltage sense to ADC, scaled to below 4 Volts
84	V8	Rail 8 voltage sense to ADC, scaled to below 4 Volts
71	V9	Rail 9 voltage sense to ADC, scaled to below 4 Volts
73	V10	Rail 10 voltage sense to ADC, scaled to below 4 Volts
76	V11	Rail 11 voltage sense to ADC, scaled to below 4 Volts
78	V12	Rail 12 voltage sense to ADC, scaled to below 4 Volts
89	V13	Rail 13 (primary power) voltage sense to ADC, scaled to below 4 Volts
98	I1	Input from Current Sense Amplifier (CSA) on Rail 1
90	I2	Rail 2, high-side of shunt resistor
94	I3	Rail 3, high-side of shunt resistor
96	I4	Rail 4, high-side of shunt resistor
70	I5	Rail 5, high-side of shunt resistor
81	I6	Rail 6, high-side of shunt resistor
83	I7	Rail 7, high-side of shunt resistor
85	I8	Rail 8, high-side of shunt resistor
72	I9	Rail 9, high-side of shunt resistor
74	I10	Rail 10, high-side of shunt resistor
77	I11	Rail 11, high-side of shunt resistor
79	I12	Rail 12, high-side of shunt resistor
97	I13	Input from Current Sense Amplifier (CSA) on Rail #13 (primary power)
44	C1	Rail 1 window comparator input, scaled to around 800 mV
45	C2	Rail 2 window comparator input, scaled to around 800 mV
46	C3	Rail 3 window comparator input, scaled to around 800 mV
47	C4	Rail 4 window comparator input, scaled to around 800 mV
48	C5	Rail 5 window comparator input, scaled to around 800 mV
49	C6	Rail 6 window comparator input, scaled to around 800 mV
51	C7	Rail 7 window comparator input, scaled to around 800 mV
16	C8	Rail 8 window comparator input, scaled to around 800 mV
17	C9	Rail 9 window comparator input, scaled to around 800 mV
18	C10	Rail 10 window comparator input, scaled to around 800 mV
42	C11	Rail 11 window comparator input, scaled to around 800 mV
43	C12	Rail 12 window comparator input, scaled to around 800 mV

Pin	Name	Description
34	C13	Rail 13 (primary power) window comparator input, scaled to around 800 mV
24	TR1	Rail 1 PWM Trim output
25	TR2	Rail 2 PWM Trim output
27	TR3	Rail 3 PWM Trim output
28	TR4	Rail 4 PWM Trim output
31	TR5	Rail 5 PWM Trim output
32	TR6	Rail 6 PWM Trim output
67	TR7	Rail 7 PWM Trim output
68	TR8	Rail 8 PWM Trim output
4	TR9	Rail 9 PWM Trim output
5	TR10	Rail 10 PWM Trim output
29	TR11	Rail 11 PWM Trim output
30	TR12	Rail 12 PWM Trim output
1	EN1	Rail 1 Enable output signal
2	EN2	Rail 2 Enable output signal
3	EN3	Rail 3 Enable output signal
6	EN4	Rail 4 Enable output signal
7	EN5	Rail 5 Enable output signal
8	EN6	Rail 6 Enable output signal
9	EN7	Rail 7 Enable output signal
22	EN8	Rail 8 Enable output signal
33	EN9	Rail 9 Enable output signal
35	EN10	Rail 10 Enable output signal
69	EN11	Rail 11 Enable output signal
55	EN12	Rail 12 Enable output signal
54	I^2C SDA	PMBus data, bidirectional
53	I^2C SCL	PMBus clock
52	SMBALERT#	Open drain, active LOW output for PMBus interface
19	I^2C ADDR0	I^2C address bit 0 select, ground = 0, float or high = 1
56	I^2C ADDR1	I^2C address bit 1 select, ground = 0, float or high = 1
23	CONTROL	PMBus Control input
36	PGOOD	Power Good output
20	SWDIO	In-circuit programming pin
21	SWDCK	In-circuit programming pin
10	VSSD	Digital ground
11	NC	No-connect
12	VSSD	Digital ground
13	VSSD	Digital ground
14	VSSD	Digital ground

Pin	Name	Description
15	#XRES	Active low reset
26	VDDIO1	Connect to VDDD
37	VDDD	Supply for all digital peripherals and digital core regulator. VDDD must be ≤ VDDA
38	VSSD	Digital ground
39	VCCD	Digital core voltage
40	NC	No-connect
41	NC	No-connect
50	VDDIO3	Connect to VDDD
57	NC	No-connect
58	NC	No-connect
59	NC	No-connect
60	NC	No-connect
61	NC	No-connect
62	NC	No-connect
63	VCCA	Analog core voltage
64	VSSA	Analog core ground
65	VDDA	Analog supply
66	VSSD	Digital ground
75	VDDIO0	Connect to VDDD
86	VCCD	Digital core voltage
87	VSSD	Digital ground
88	VDDD	Digital supply
100	VDDIO2	Connect to VDDD

A.20 Power System

The power system consists of separate analog, digital, and I/O supply pins, labeled VDDA, VDDD, and VDDIOx, respectively. It also includes two internal 1.8 V regulators that provide the digital (VCCD) and analog (VCCA) supplies for the internal core logic. The output pins of the regulators (VCCD and VCCA) and the VDDIOx pins must have capacitors connected as shown in Figure 48. The two VCCD pins must be shorted together with as short a trace as possible (a trace beneath the device is recommended), and connected to a 1 µF ±10% X5R capacitor.

Figure 48. Example Schematic with Power Connections

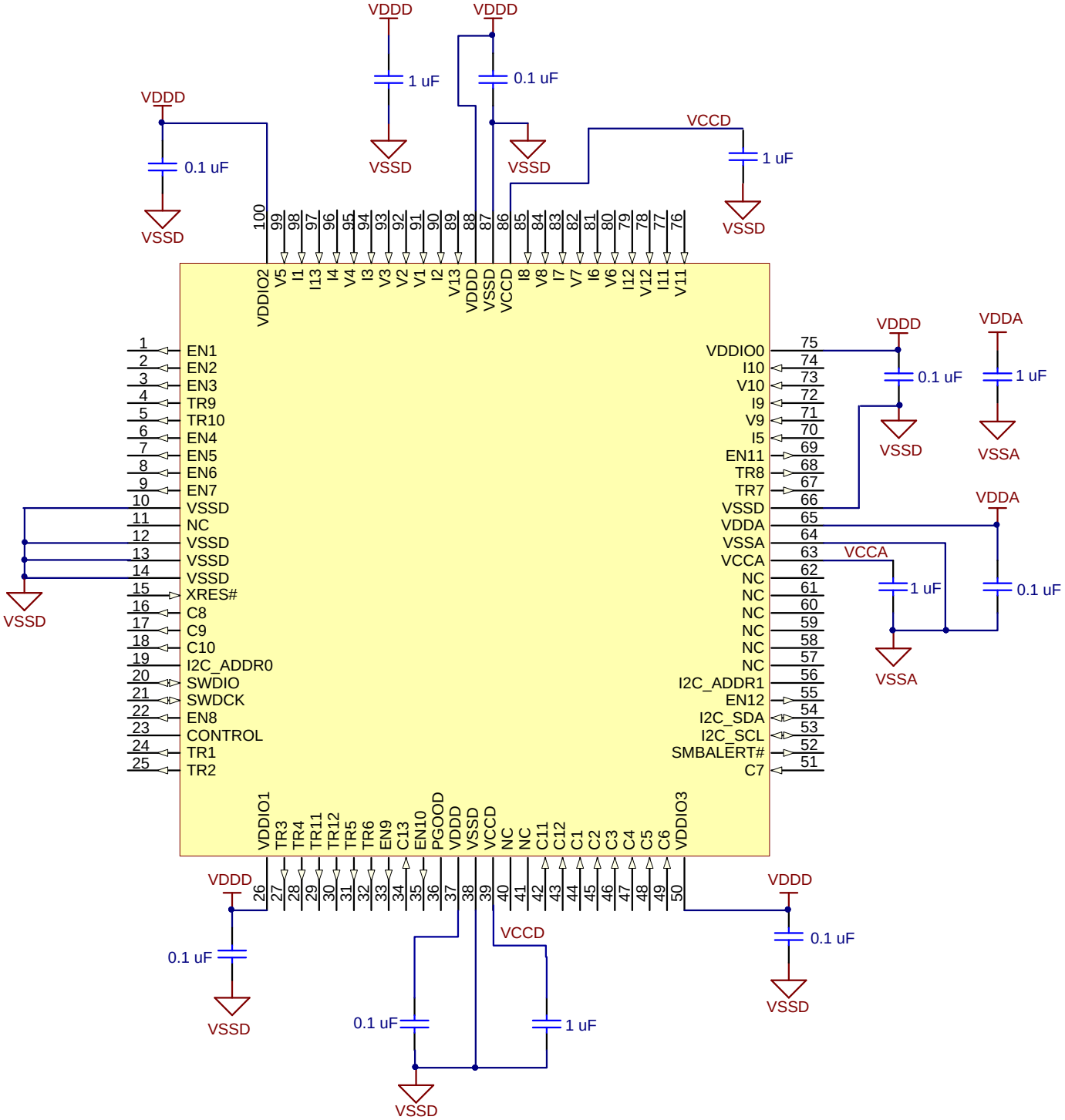
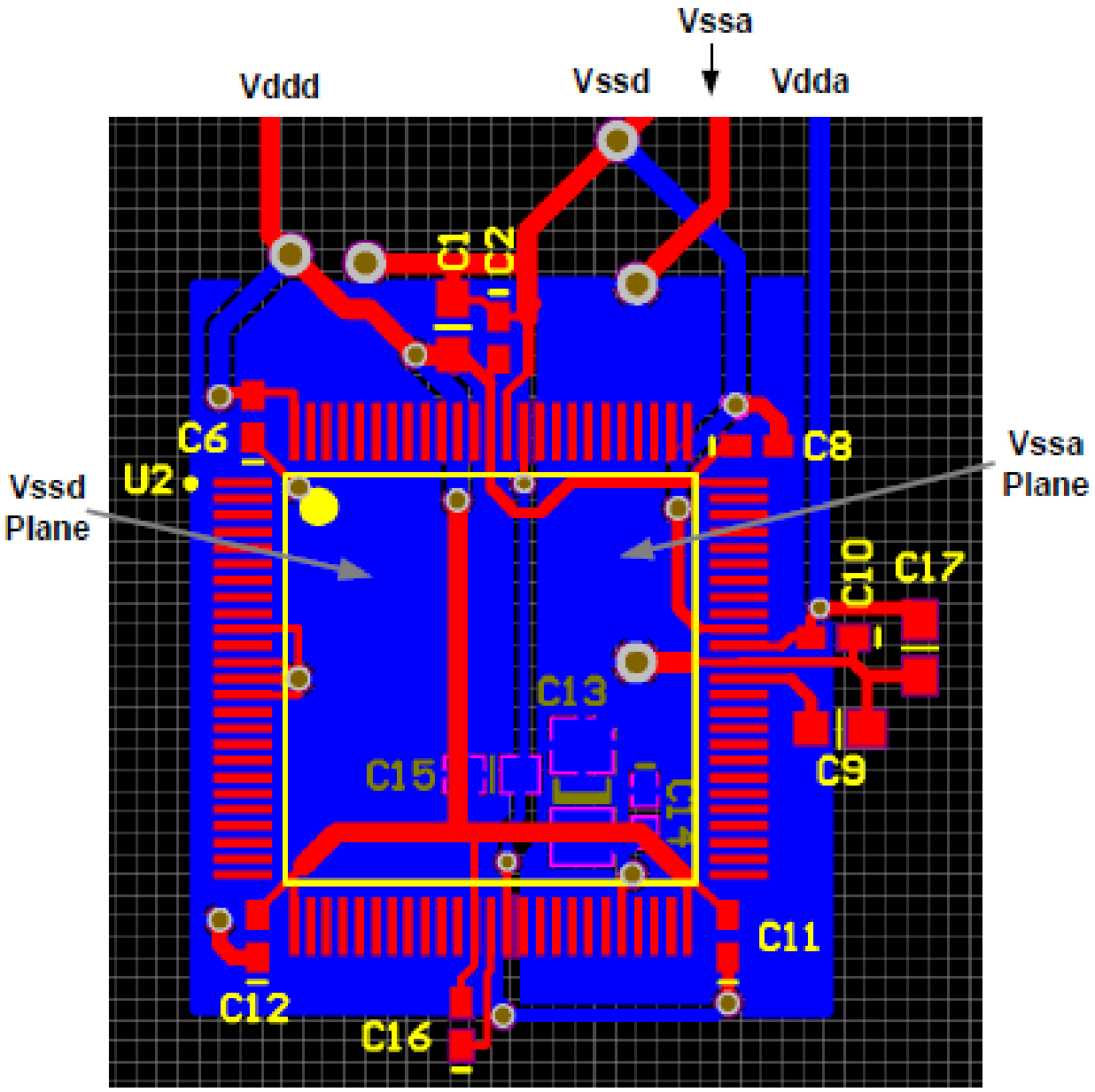
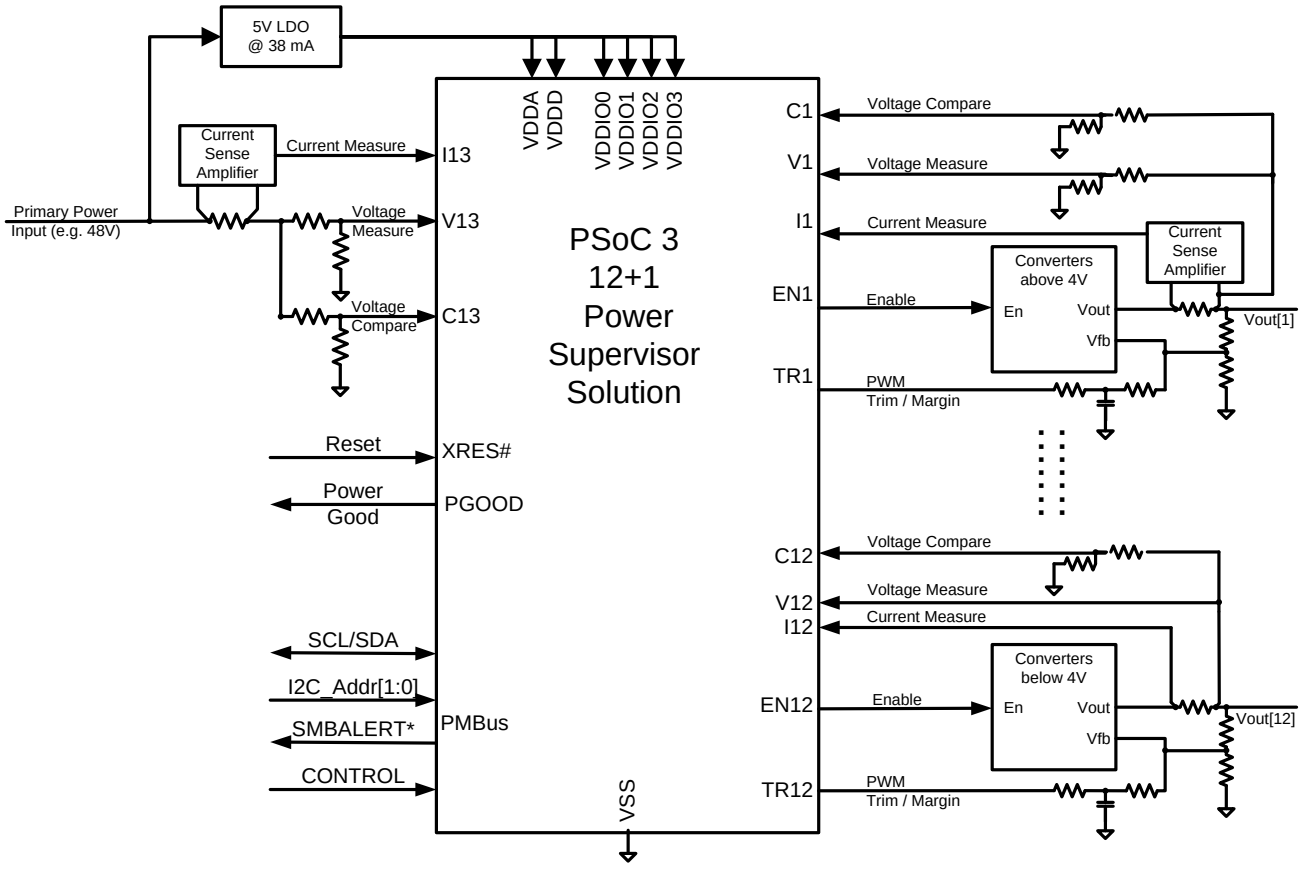


Figure 49. Example PCB Layout for Power Routes



A.21 Typical Application

Figure 50. Typical Application Circuit Diagram



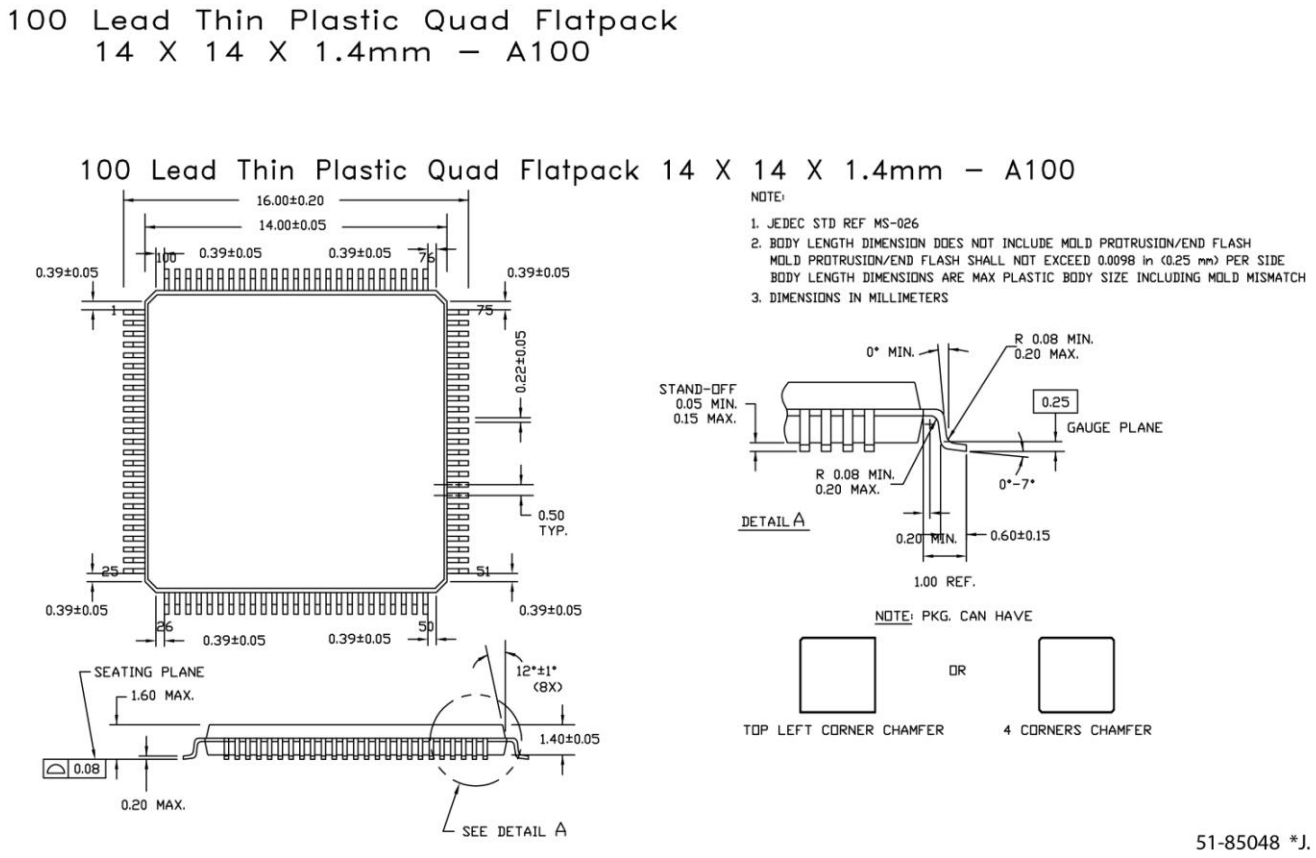
Notes:
1. All Vx voltages should be scaled below 4 V using external 0.1% resistors
2. All Cx voltages should be scaled with an external resistor divider such that the maximum expected OV fault trigger voltage is below 1020 mV (1020 mV is the highest configurable threshold value)
3. All Cx scaling resistors should have no more than 2 KΩ resistance to minimize delays when being multiplexed within the PSoC 3 12+1 Power Supervisor

A.22 Packaging

Table 47. Package Characteristics

Parameter	Description	Min	Typ	Max	Units
T_A	Operating ambient temperature	-40	25	85	ºC
T_J	Operating junction temperature	-40	-	100	ºC
T_{JA}	Package θ_{JA}	-	34	-	ºC/Watt
T_{JC}	Package θ_{JC}	-	10	-	ºC/Watt
	Solder reflow peak temperature	-	-	260	ºC
	Solder reflow max time at peak temperature	-	-	30	s
	Package moisture sensitivity level Per IPC/JEDEC J-STD-2	MSL 3			-

Figure 51. 100-pin TQFP (14 x 14 x 1.4 mm) Package Outline



Document History

Document Title: AN76474 - PSoC® 3 Power Supervisor

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3689904	RADH	07/23/2012	New Spec.
*A	3700931	RADH	08/01/2012	1. Updated incorrect description of the CTL Fault Parameter and Table 9 2. Table 19 in the User Guide updated to reflect operating on power supplies below 5 V 3. Typographical error fixes
*B	4245050	KJV	01/13/2014	Updated and restructured the document to introduce the new 17-rail Power Supervision solution (previously 12-rail) along with its User Guide (Appendix A). The new PSoC Power Supervision Tool is also introduced along with hands-on exercises. Updated copyright date.
*C	4456345	RLRM	07/24/2014	Reverted application note back to the *A revision content. Updated Figure 51 to *I.
*D	4862509	RLRM	07/28/2015	Updated template
*E	5715411	AESATMP9	05/18/2017	POD 51-85048 Rev *J is updated on page 78 and Updated logo and copyright

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