AN72362

Reducing Radiated Emissions In Automotive Capsense® Applications

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Associated Part Family: CY8C21x34, CY8C21x45, CY8C22x45, CY8C24x94

Related Application Notes: None

AN72362 describes various hardware and firmware techniques that reduce radiated electromagnetic emissions in order to pass automotive and general electromagnetic compatibility (EMC) tests for capacitive touch based applications.

Contents

1 Introduction

Every automobile manufacturer is trying to improve the aesthetics and usability of their dashboard with intuitive human-machine interfaces (HMI). Capacitive based touch switches for infotainment is one of the latest offering by all carmakers worldwide. CapSense® (Cypress's Capacitive Touch Technology based on PSoC) provides a flexible and cost effective solution to implement capacitive sensing, proximity detection, and capacitive touch screens.

While CapSense offers an intuitive and robust interface that increases product reliability by eliminating mechanical parts, it can also contribute to electromagnetic compatibility (EMC) issues in the form of radiated emissions (RE). Proper care must be taken by system engineers during hardware design. Electromagnetic immunity (EMI) or EMC is a complex problem and even after following all guidelines you may not be able to limit the emissions. In that case the flexibility of PSoC devices allows the adjustment of firmware parameters to further reduce RE.

This document describes best layout practices and firmware techniques that could be helpful in reducing emissions and enable the system to meet various emission standards. The application note also shows some test results of a typical CapSense based application. It is assumed that the reader has some basic understanding of CapSense operation. If not we strongly recommend to go through Getting Started with CapSense®.

This application note provides the following

- Brief introduction to CapSense
- Main factors contributing to RE for CapSense
- Firmware techniques to reduce emissions
- Hardware best practices to reduce emissions

This application note also briefly describes some of the key Automotive EMC standards followed in the industry.

1.1 Automotive EMC Standards

EMI or EMC testing for automotive applications follows standards from two main organizations:

1. International Organization for Standardization (ISO).
2. Special International Committee for Radio Interference (CISPR), which is part of the International Electrotechnical Commission (IEC) that is responsible for emission for all products.

All significant automotive EMC test methods have international versions of one of the tests within the ISO and IEC.

Listed below are some of the major standards for automobiles:

- Radiated emissions (RE)
  - CISPR 25
  - SAE J1113-41

These Standards contain limits and procedures for the measurement of radio disturbances in the frequency range of 150 kHz to 2500 MHz. The standards applies to any electronic or electrical component intended for use in vehicles, trailers, and electronic devices

- Radiated immunity (ALSE)
  - ISO 11452-2
  - SAE J1113-21

These standards specify an absorber-lined shielded enclosure (ALSE) method for testing the immunity of electronic components for a passenger's car and commercial vehicles. The device under test together with the wiring harness is subjected to electromagnetic disturbance generated inside an ALSE.

- Bulk current injection (BCI)
  - ISO 11452-4
  - SAE J1113-4 Conducted Immunity
- Electrostatic discharge (ESD)
  - ISO 10605
  - SAE J1113-13

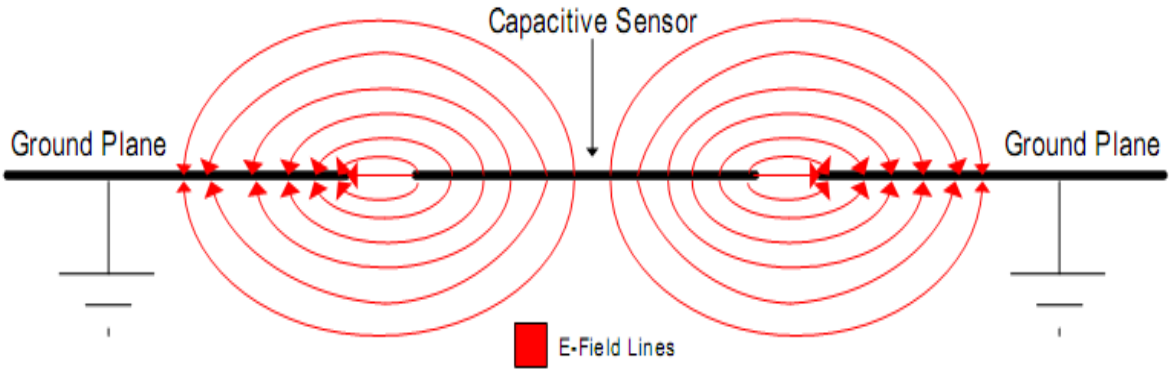
Besides these standards, automobile manufactures typically develop and enforce proprietary standards, tests and limits. For example, GM5097, 3100 DC 10614, Ford AB/AC, BMW GS 95002/3 and so on.

2 How does CapSense work?

A capacitive sensor is composed of a pair of adjacent electrodes and when a conductive object comes in proximity or in contact it adds an additional capacitance, which can be used to measure the object's presence.

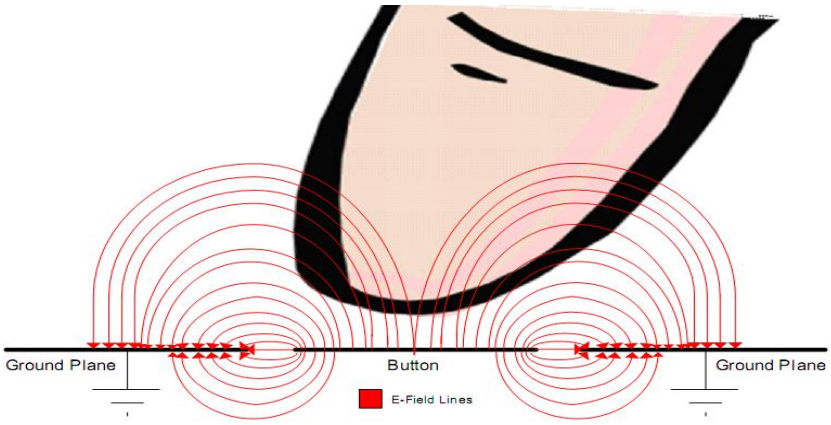
In order to understand capacitive sensing, it is first important to understand some basics about electric fields (E fields). It is a fundamental fact that E field take the path of least resistance to ground. Figure 1 shows a general form of E field in a capacitive sensing design.

Figure 1. Electric Field on Capacitive Sensor



Electric field lines propagate from a higher potential to a lower potential that is from the capacitive sensor to ground as shown in the following figure.

Figure 2. Increase in Electric Field Concentration due to Presence of Finger

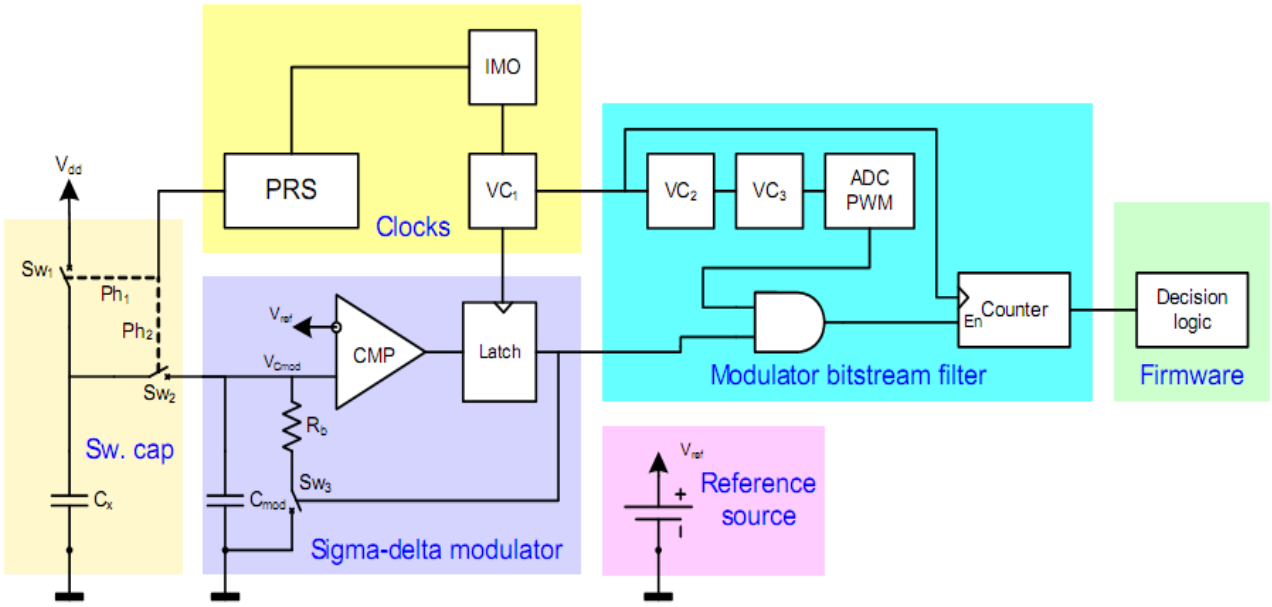


The presence of a conductive object (finger) allows an increased number of electric field lines to travel between the button and the ground plane as higher permittivity of a conductor allows more electric field lines to pass through. This greater concentration of E field results in greater capacitance to be measured at the sensor.

CapSense® technology is based on CSD algorithm. The architecture of CSD is briefly described as follows.

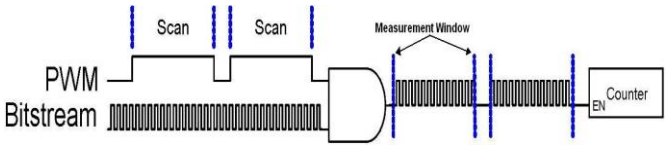
2.1 CSD Architecture

Figure 3. CSD Architecture for 21x34



The CSD algorithm uses the switched capacitor circuitry to convert the capacitance into voltage, which is compared to a reference voltage. The sensor keeps on transferring charge to C_{MOD} capacitor and when the capacitor voltage reaches the reference voltage the comparator triggers a bleed resistor, which discharges the capacitor (C_{MOD}). When the capacitor voltage declines below the reference voltage, the bleed resistor (R_B) is left floating to allow the capacitor to continue charging. The comparator output, which continually toggles the bleed resistor, is a bit stream which fluctuates as the sensor capacitance changes. The bit stream is ANDed with a PWM to provide consistent framing of the stream. The number of counts in each frame (raw count) is then analyzed to determine if the capacitive sensor is being triggered.

Figure 4. Raw Count Calculation



For more details about CapSense UM refer Getting Started with CapSense.

Figure 3 shows CSD architecture of 21x34 devices. But the CSD architecture of 24x94 and 22x45 are different from what is shown in Figure 3.

3 Factors Affecting Radiated Emission for CapSense UM

As far as CapSense UM is concerned the main parameters that contribute to RE are:

- Device operation frequency (IMO)
- Electrode modulation frequency
- Shield electrode

These parameters contribute to the bulk of electromagnetic radiated emission caused when using CapSense.

Increasing the device operation frequency will increase the emission as all the switching that happens is driven by the internal main oscillator (IMO) as shown in Figure 3.

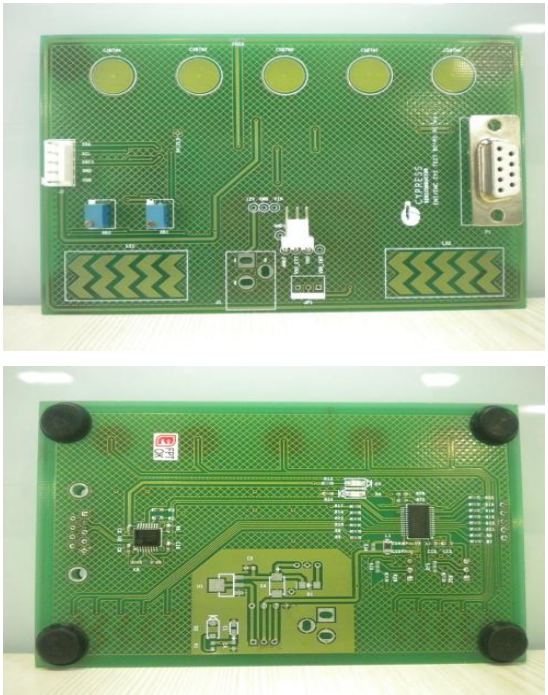
Electrode Modulation Frequency: CapSense electrode is being charged and discharged continuously during the scanning. Electrode modulation frequency refers to the rate at which the electrode is being charged and discharged. So reducing modulation frequency will reduce RE.

CapSense measures the sensor capacitance by using a switched capacitor circuitry where the electrode is modulated using an AC signal. Through this mechanism the charge is transferred from the sensor electrode to the C_{MOD} capacitor, which is then converted into voltage and is compared with a reference. The capacitor is charged and discharged at a frequency determined by the pseudo random sequence (PRS) or prescaler output. Therefore, the overall RE will be reduced by decreasing the charging and discharging frequency of the capacitor (electrode modulation frequency). The section Reducing Frequency discusses how to reduce IMO frequency and electrode modulation frequency.

Enabling shield will increase the emissions significantly as high frequency switching signals are being routed across the board. More details about the shield are discussed in section Shield Output.

To understand the effect of different parameters on emissions from CSD, RE test were performed according to the CISPR 25 on a non-optimized test board. The results are reported in the following sections describing firmware and hardware options to reduce RE. This test board was designed for test purpose to study the impact of different parameters in emission and emission levels can be made better than in the graphs shown in this application note.

Figure 5. Test Boards

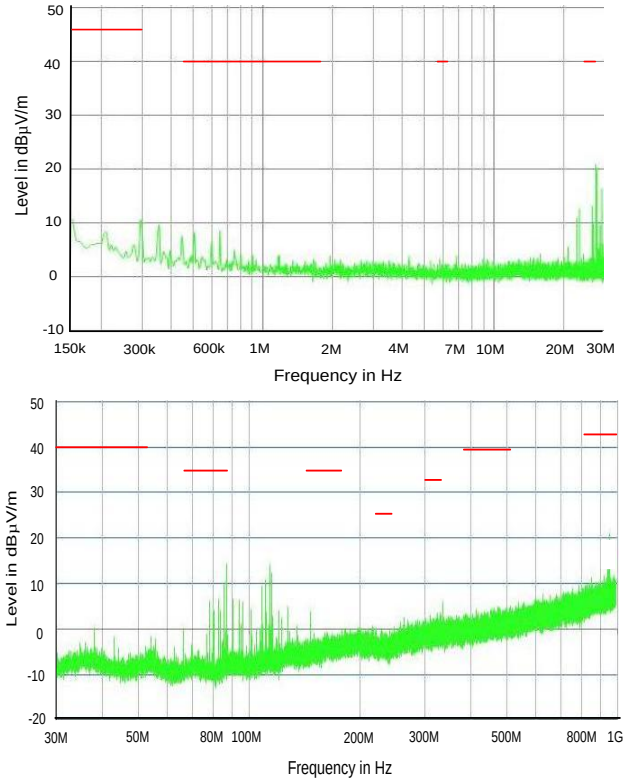


It is a known fact that emissions increase with switching frequency and voltage. For high performance the operating frequency has to be high. If we go for lower operational frequency it will affect scanning or process time, which reduces the overall system performance. So the challenge here is to get the maximum performance and at the same time be EMC compliant.

Different methods to reduce emissions are discussed in the following sections.

4 Best Case Result

Below graph shows best case results. Emissions in this configuration falls within class 5 limits as per CISPR25 standards.



Settings	
V_{DD}	3.3 V
Series resistor	2.2 kΩ
Shield	Disabled
Sensor modulation frequency	375 kHz
Sensor modulation signal	PRS
Dithering (frequency hopping)	ON

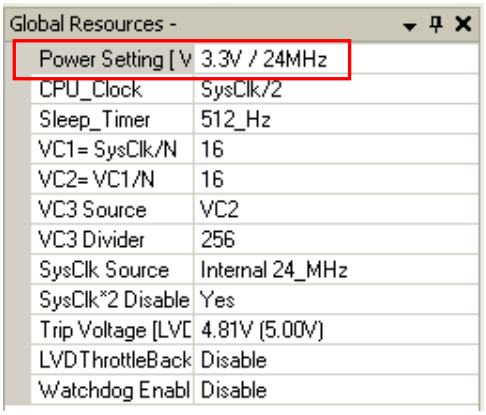
5 Options to Reduce RE

5.1 Firmware Options

5.1.1 Operating Voltage

As the emissions is directly proportional to voltage levels at which switching happens. Reducing the operating voltage will help to reduce emissions to a great extent as the amplitude of switching signal at any pin is dependent on the operating voltage of the device. Operating voltage can be reduced by changing the Power Setting parameter in the global resources window of the PSoC Designer project as shown in Figure 6.

Figure 6. Power Setting and Sysclk Settings in Global Resources Window



PSoC allows you to operate at lower operating voltages thereby reducing the emissions. At lower operating voltages the maximum CPU frequency possible is 12 MHz and with a 5 V operating voltage CPU frequency can be up to 24 MHz. So select your operating voltage depending upon your system requirements.

Disable **SysClk*2** if it is not used as shown in Figure 6. For CapSense only application it is advised to disable this in global resources window.

The Figure 7(a) and 7(b) show the impact of operating voltage on the radiated emissions. In this case there is not much improvement because for CY8C22x45 devices switching on sensor pins happens between Vref (Reference voltage) and ground. But for CY8C21X34 and CY8C24X94 devices V_{DD} setting can affect emissions more significantly as the sensor switching here happens between V_{DD} and Vref. Vref can be set in CSD parameter window.

Figure 7(a). Effect of V_{DD}

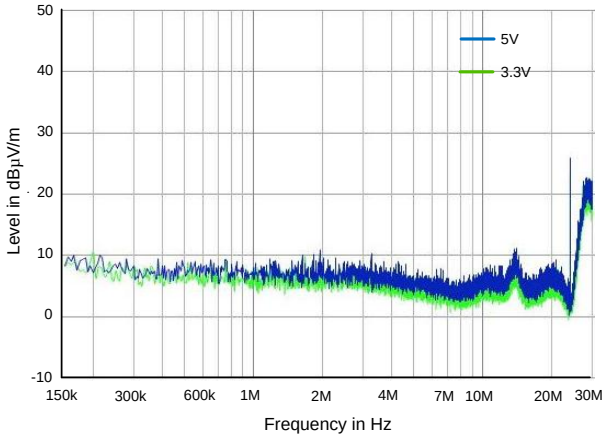
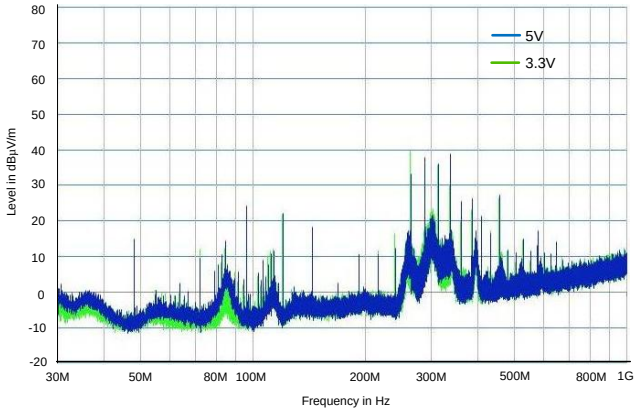


Figure 7(b). Effect of V_{DD}



5.1.2 Reducing Frequency

System Oscillator Frequency

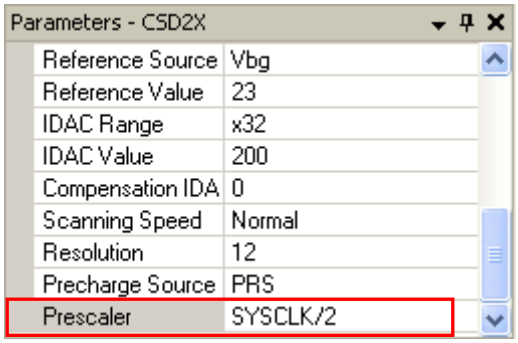
Lowering system clock will lower RE by a good amount. But lowering the system clock will impact the performance of your system, as IMO is low, it can take more time to scan the sensors and do the processing. So suitably lower the system frequency depending on your application.

Electrode Switching Frequency

Reducing the electrode switching or sensor modulation frequency by increasing the prescaler will also help to improve your emission results, as the capacitive sensors are scanned at a lower frequency.

Figure 8 and Figure 9 show how to reduce electrode switching frequency by adjusting prescaler for CSD2X UM and CSD UM respectively.

Figure 8. Prescaler Setting for CSD2X UM



Here the average scanning frequency will be $F_{PRESCALER}/4$ and maximum is $F_{PRESCALER}/2$ as pseudo random sequence (PRS) source is used. With the prescaler setting as shown in Figure 8 scanning frequencies will be as shown as follows.

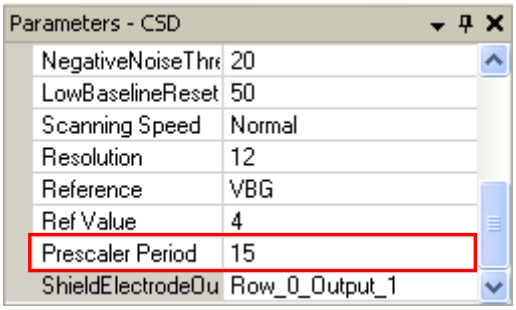
$F_{PRESCALER} = F_{SYSCLK}/2$

$F_{SCAN\ AVERAGE} = F_{PRESCALER}/4 = F_{SYSCLK}/8$

$F_{SCAN\ MAX} = F_{PRESCALER}/2 = F_{SYSCLK}/4$

If using CSD user module with PRS16 configuration prescaler option is not available. Prescaler period is automatically set here. But prescaler option is available if you are using CSD user module with PRS8 configuration.

Figure 9. Prescaler Setting for CSD UM



Here the average scanning frequency will be $F_{PRESCALER}/4$ and maximum is $F_{PRESCALER}/2$.

Where $F_{PRESCALER} = F_{SYSCLK}/(\text{Prescaler Period} + 1)$

5.1.3 Shield Output

Cypress CapSense best practice recommends usage of hatched pattern around CapSense buttons. Hatched pattern can be connected to:

1. Ground
2. Shield

Hatched pattern connected to ground:

Advantage:

1. Reduced emissions

Disadvantage:

1. Increased parasitic capacitance
2. Lower sensitivity
3. Water proofing is not possible

Hatched pattern connected to shield:

Advantage:

1. Reduced parasitic capacitance
2. Higher sensitivity
3. Water proofing is possible

Disadvantage:

1. Higher emissions

Working of Shield:

Shield signal is a series of square waves that are generated in synchronization with CapSense switching signals as shown in Figure 10. The only difference being the amplitude of the signals. Shield is switched between ground and V_{DD} while CSD scanning signal will be toggling between Vref and V_{DD} for CSD UM and between Vref and ground for CSD2X UM.

Figure 10. Shield Signal Output

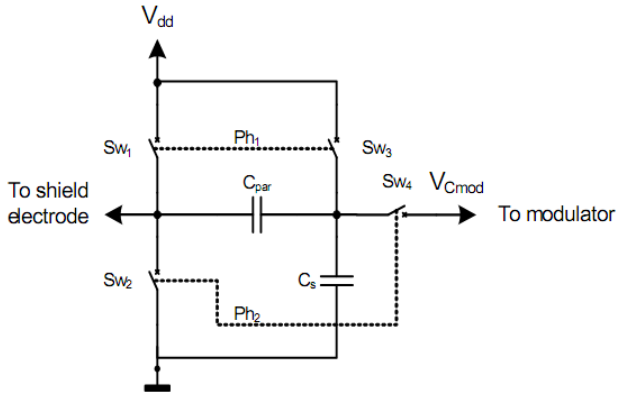
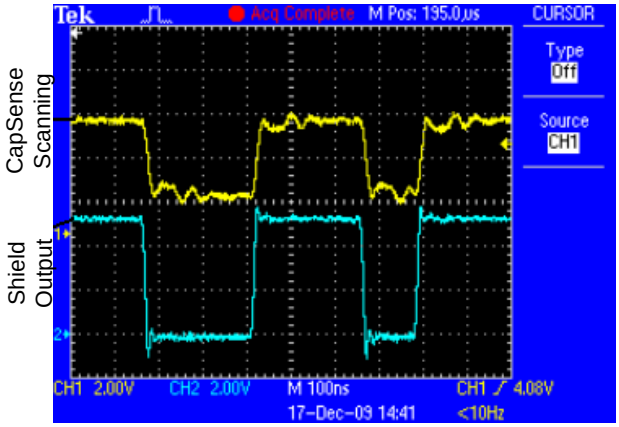


Figure 11. Shield Signal



Shielding electrode also reduces the influence of parasitic capacitance by lowering sigma delta modulator input current, as the potential difference between the sensor button and the surrounding hatched pattern, which is driven by shield, is less than that without shield. Shield output is important in designs that require reliable operation in the presence of water films or droplets. Particularly in Automotive application where it is very critical that the capacitive sensors do not give false triggering because of water, ice, and humidity changes. For example CapSense buttons in key fob should not false trigger in under any circumstances. In those cases shield signal is essential. Shield signal can be routed along shield electrode helps to reduce overall parasitic capacitance.

As mentioned earlier main disadvantage of using shield signal is that it will increase the emissions. But emissions can be reduced by adding a passive low-pass filter (LPF) to the shield output by putting a series resistor to the shield pin. An inherent LPF is formed by the resistance of electrode material and the parasitic capacitance of the electrode. So adding a series resistor increases the RC of the filter and help to improve emissions to a great extend as the RC filter formed will eliminate higher order frequencies.

Note Filtering the shield too much can cause phase difference between shield and CapSense nodes. Phase difference more than 90° is not recommended as it can break the shield operation.

Figure 12(a). Effect of Shield

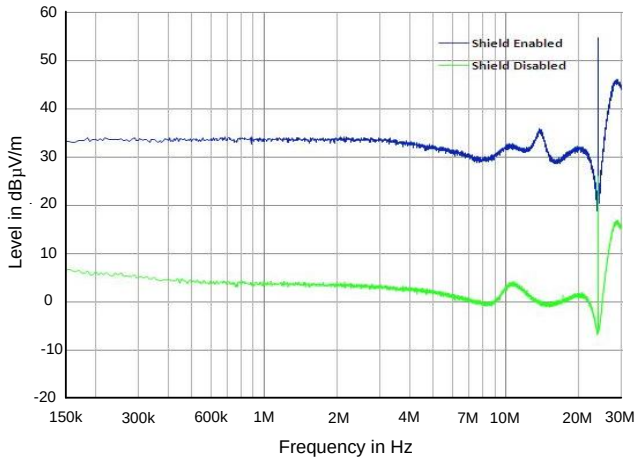
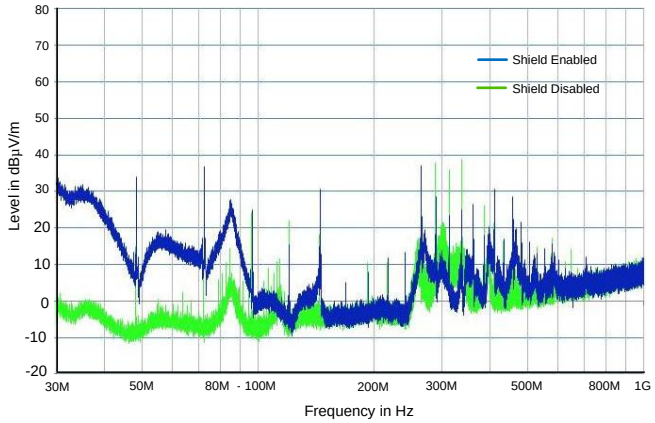


Figure 12(b). Effect of Shield



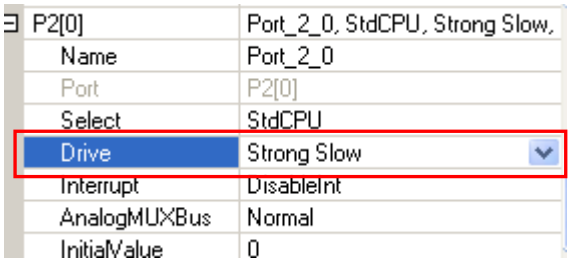
5.1.4 Slew Rate of Shield Output

We can reduce the emissions if we decrease the slew rate, that is, by increasing the rise time of the signal we are reducing overall bandwidth of the signal by eliminating higher order frequency components in the signal.

Bandwidth α 1/τ
Where τ → rise time of the signal.

In PSoC you can do it by changing the drive mode from **Strong to Strong Slow** as shown in Figure 13.

Figure 13. Changing Drive Mode

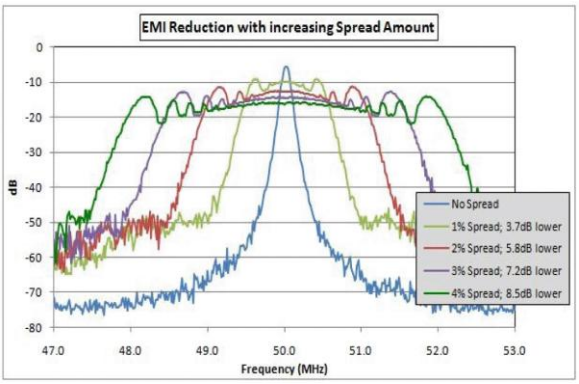


If you make drive mode of shield pin from strong to strong-slow, a LPF is added to the shield pin (internal to PSoC) there by reducing emissions.

5.1.5 Frequency Hopping

Frequency hopping is the method of spreading the input or operating frequency over a narrow band of frequencies. This method will help to reduce the peaks and spread out the emissions over a range of frequencies as shown in Figure 14. The various methods to do frequency hopping in PSoC are IMO trimming/dithering or using a Spread Spectrum (SS) clock.

Figure 14. Frequency Hopping



IMO dithering – PSoC 1 does not require an external crystal to work as it has an internal oscillator, which can run at a maximum frequency of 24 MHz. One can change the frequency of internal oscillator and sweep across a range of frequencies; this will cause emissions to spread across a band of frequency as shown in Figure 14. This can be achieved by modifying the value of IMO_TR register in PSoC 1. For example we can sweep the internal oscillator speed over a range from 24 to 22 MHz.

When doing IMO dithering try to scan a sensor always with same frequency. And scan different sensors at different frequencies.

Code snippet to do IMO dithering is shown below.

```
initial_IMO = find_IMO();
temp_IMO = initial_IMO; /* Initial IMO hold the initial IMO value */
while(1)
{
for(i = 0; i < CSD_TotalSensorCount; i++)
 {
   CSD_ScanSensor(i);
   CSD_UpdateSensorBaseline ( i );
   if( i <=  CSD_TotalSensorCount/2 )
      temp_IMO--;
   else
      temp_IMO++;
   IMO_TR = temp_IMO;
 }
IMO_TR = initial_IMO; /* Restore initial IMO */
/*
Do other operations/processing
*/
}
```

This code goes on decreasing the IMO frequency in steps until half of the sensors are scanned, and then goes on increasing the IMO frequency and restore the original frequency once all the sensors are being scanned. This method will ensure that we sweep the IMO in steps and there is not a huge/sudden jump in IMO frequency. When you are changing the IMO_TR register value by one you are changing the IMO frequency almost by 60 kHz.

So inorder to achieve dithering we have to change the value in **IMO_TR** during run time. For this you require initial IMO trim value. In order to get the initial trim value you have to do supervisory system call (SSC).

Code snippet to get the initial IMO value is shown below. Make a new *.asm* file copy this code into that asm file

```
include "m8c.inc"
include "m8ssc.inc"
include "psocapi.inc"
include "memory.inc"
include ".\lib\GlobalParams.inc"

  SROM_TABLE_1:           equ 01h
  SROM_TABLE_2:           equ 02h
  POWER_SET_5V0_24MHZ:    equ 10h
  POWER_SET_5V0_6MHZ:     equ 11h
  POWER_SET_3V3_24MHZ:    equ 08h
  POWER_SET_3V3_6MHZ:     equ 09h
;AREA bss
Initial_IMO:
        BLK 1

export _find_IMO
; Fastcall16 inputs (none)
;     A - none
; Fastcall16 return value (single byte)
;     A - read data
_find_IMO:
; To set the page pointers correctly before doing SSC operations
  mov   A, reg[MVW_PP]
  push  A
  mov   A, reg[CUR_PP]
  push  A
  mov   reg[MVW_PP], 0
  mov   reg[CUR_PP], 0

  mov A, POWER_SETTING
  cmp A, POWER_SET_3V3
  jz .Read24m3v3TrimValue
  cmp A, POWER_SET_5V0
  jz .Read24m5v0TrimValue
  cmp A, POWER_SET_5V0_6MHZ
  jz .Read6m5v0TrimValue
  cmp A, POWER_SET_3V3_6MHZ
  jz .Read6m3v3TrimValue
  jmp .Exit


.Read24m5v0TrimValue:
; Get 5V, 24MHz IMO trim value
  mov [bSSC_TABLE_TableId], SROM_TABLE_1
       SSC_Action(TABLE_READ)
  nop
  mov A, [SSCTBL1_TRIM_IMO_5V_24MHZ]
  mov [Initial_IMO], A
  jmp .Exit

.Read24m3v3TrimValue:
; Get 3.3V, 24MHz IMO trim value
  mov [bSSC_TABLE_TableId], SROM_TABLE_1
  SSC_Action(TABLE_READ)
  nop
  mov A, [SSCTBL1_TRIM_IMO_3V_24MHZ]
  mov [Initial_IMO], A
  jmp .Exit
```

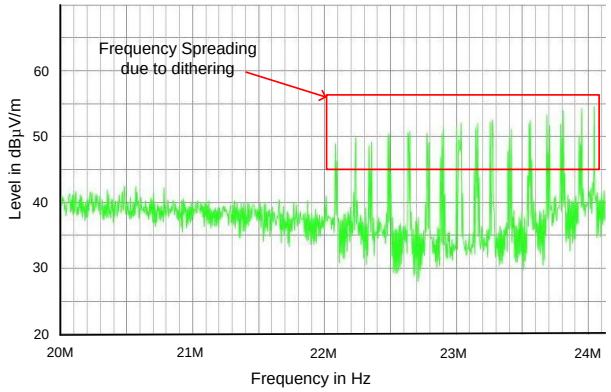
```
.Read6m5v0TrimValue:
; Get 5V, 6MHz IMO trim value
  mov [bSSC_TABLE_TableId], SROM_TABLE_2
  SSC_Action(TABLE_READ)
  nop
  mov A, [SSCTBL2_TRIM_IMO_5V_6MHZ]
  mov [Initial_IMO], A
  jmp .Exit

.Read6m3v3TrimValue:
; Get 3.3V, 6MHz IMO trim value
  mov [bSSC_TABLE_TableId], SROM_TABLE_2
  SSC_Action(TABLE_READ)
  nop
  mov A, [SSCTBL2_TRIM_IMO_3V_6MHZ]
  M8C_SetBank0
  mov [Initial_IMO], A
  jmp .Exit

.Exit:
  pop   A
  mov   reg[CUR_PP], A
  pop   A
  mov   reg[MVW_PP], A
  mov A, [Initial_IMO]
  ret
```

Following code should be included in *main.c* to access the function which finds the IMO trim values.

```
#include <m8c.h>        /* part specific constants and macros */
#include "PSoCAPI.h"    /* PSoC API definitions for all User Modules */

#pragma fastcall16 find_IMO
char find_IMO(void);

void main()
{
BYTE initial_IMO;
initial_IMO = find_IMO();  /* find_IMO returns the IMO trim value */
/* Do further processing*/

}
```

Once we get the initial IMO value we can modify it according to our need. In dithering algorithm it is advisable that the frequency should be always be dithered down from the base frequency. If it is dithered up from the base frequency it might get too fast and exceed device limitations. Also take care not to trim the IMO register too high or too low so that an overflow or underflow occurs.

Figure 15. Effect of Dithering

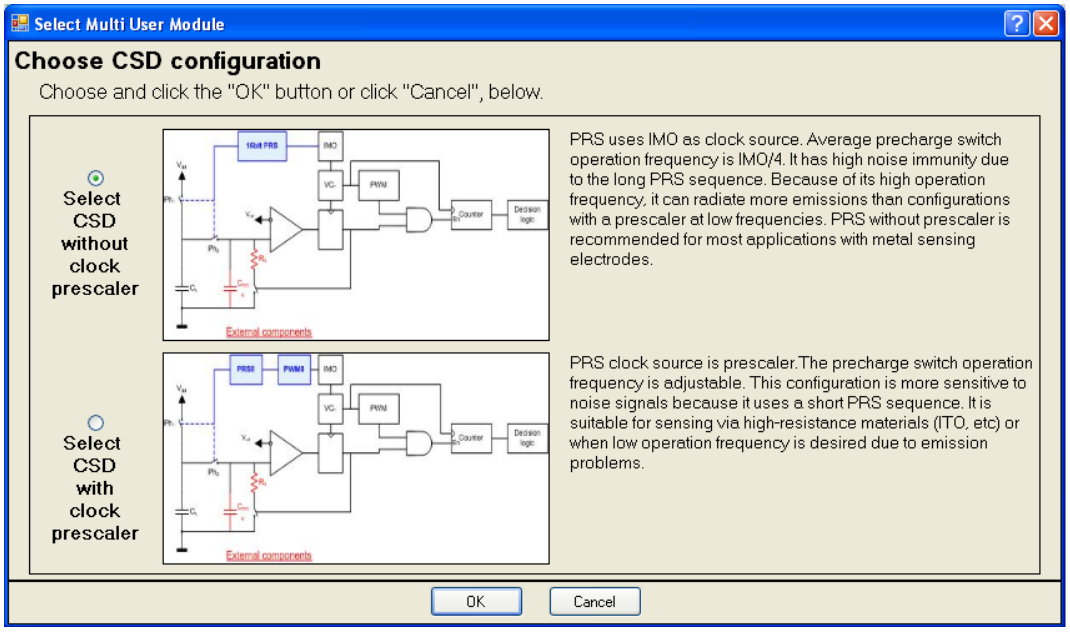


As you can see the emissions are spread across a band of frequencies and the maximum peak reduces as shown in Figure 15. Here the IMO is dithered down from 24 MHz to 22 MHz. Peaks can be observed at frequencies at which scanning occurs and peak emission at 24 MHz is reduced due to dithering.

Spread Spectrum clock – PSoC can also work using external clock. If we use a spread spectrum clock this will help in spreading out the emissions over a wider range of frequency similar to IMO dithering. PSoC allows only port **P1[4]** to be used to supply the external clock. In this case, pin P1[4] **drive mode must be set to HI-Z digital**.

Pseudo random sequencer (PRS) - A PRS is used instead of fixed clock source in order to attenuate emitted noise on CapSense pins by reducing the amount of EMI created by a fixed frequency source and to increase EMI immunity from other sources and their harmonics.

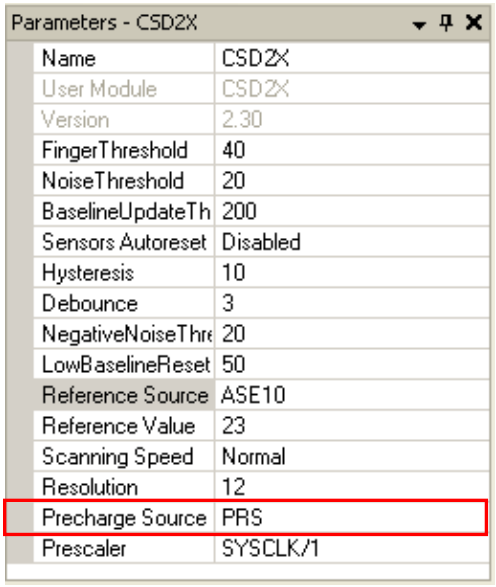
Figure 16. CSD Prescaler Configuration



When using CSD UM it is better to select CSD without clock prescaler as shown in Figure 16. This uses a 16-bit PRS to generate scanning signals which will spread around the scanning signal frequency and provide much better EMI or EMC performance with respect to using a fixed frequency clock source.

If you are using CSD2X UM select precharge source as PRS instead of timer for better EMC results.

Figure 17. Selecting PRS Source in CSD2X UM



5.2 Board Design Considerations / Best Practices

Capacitive sensing is based on measurement of capacitance and significant amount of high frequency switching happens in the process. This can result in significant amount of emissions if proper care is not taken in board design. Getting started with CapSense presents best practices for designing CapSense™ systems and gives details about best layout practices for CapSense. Following are some hardware guidelines which will help to reduce emissions for a system involving CapSense.

5.2.1 Adding Series Resistors

Placing series resistance in each sensor line will reduce emissions significantly as this is equivalent to adding an LPF (LPF formed by series combination of resistor and parasitic capacitance due to sensor electrode). This will help in eliminating higher order harmonics and attenuate the emissions. However it has an impact on sensitivity. With higher series resistor values the SNR decreases, so selection of series resistor should be done properly. ITO panel already provides high resistance; one may not have too much flexibility in value selection (Range 100 Ω – 1 kΩ). For general copper PCBs this value can go up 4.7 kΩ and even more. Series resistors are generally used between 560 Ω – 4.7 kΩ.

Figure 18(a). Effect of Series Resistors

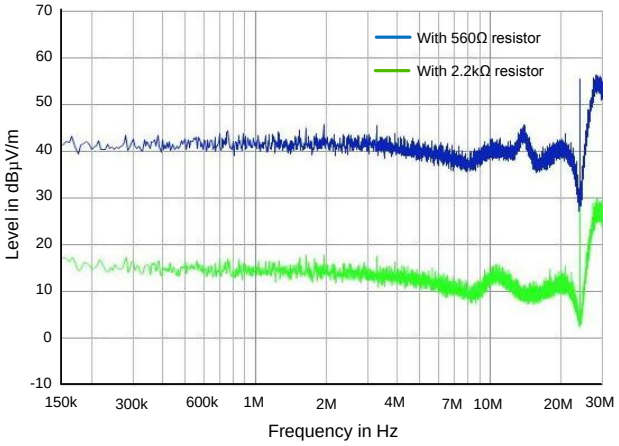
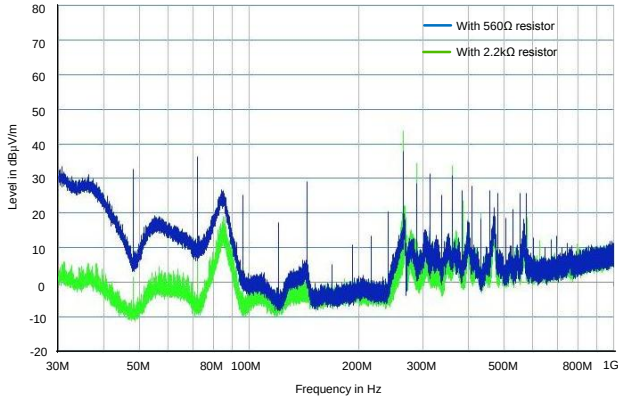


Figure 18(b). Effect of Series Resistors



It is better that the series resistor aligns with the direction of the trace routing, as this reduces the trace length. For CapSense applications it is essential that the length of traces is kept to a minimum and is equal for all sensors as much as possible. This will minimize the parasitic capacitance added due to sensor traces and also minimize the variation of such capacitance across sensors.

5.2.2 Providing Proper Ground

A ground plane can lower the overall ground impedance, thus reducing high frequency ground bounce. Hence ensure good GND return paths for each sensor line. This is important as current flows in loops. Unless there is a proper return path for high speed signals, the return current will flow through a longer return path forming a larger loop and this can cause signal issues on the signal and also other signals due to the mutual inductance caused. Use a solid GND plane under the IC's and a hatched ground pattern where CapSense buttons/traces are present. Typical hatching for the ground fill is 25 percent on the top layer (7 mil line, 45 mil spacing) and 17 percent on the bottom layer (7 mil line, 70 mil spacing). Multiple layer board should be the preferred choice. If you are using a board with four layers or more, you can provide a complete layer for ground that will further help to reduce emissions as it reduces ground debounce significantly.

When a device package contains high-frequency current loops, energy can also be coupled out of the device through a magnetic field. It is possible for the magnetic flux to form a current loop in the device to link to circuit loops outside the device. This mutual inductance can produce an unwanted voltage in the external loop. Likewise, an external magnetic flux can induce an unwanted voltage across an interior circuit loop. Magnetic field coupling can be minimized by keeping power and signal loop areas as small as possible. Stitch all the grounds with as many vias as possible. This will reduce the overall ground impedance.

High-frequency traces, such as those used for clock and oscillator circuits, should be contained by two ground lines. This will ensure that there is no coupling, which results in crosstalk. Use separate ground plane and power planes where ever possible.

5.2.3 Proper Filters to V_{DD}

A LPF can be useful for reducing most of the high-frequency EMC problems. For V_{DD}, generally pi-filter is recommended as it will effectively isolate noise from power supply to IC and back, as multiple ICs may share a common power supply.

Proper use of decoupling capacitors as recommended by the device datasheet can limit the problem with conducted emissions. For further protection, a passive filter can be used. This filter effectively limits not just the conducted noise emitted but also the noise entering the system. Thus it improves the conducted noise immunity of the system. A pi filter is a simple bidirectional LPF. The bidirectional nature of the filter is very important. Not only it prevents the supply noise from affecting sensitive parts, it can also prevent the switching noise of the part itself from coupling back onto the power planes.

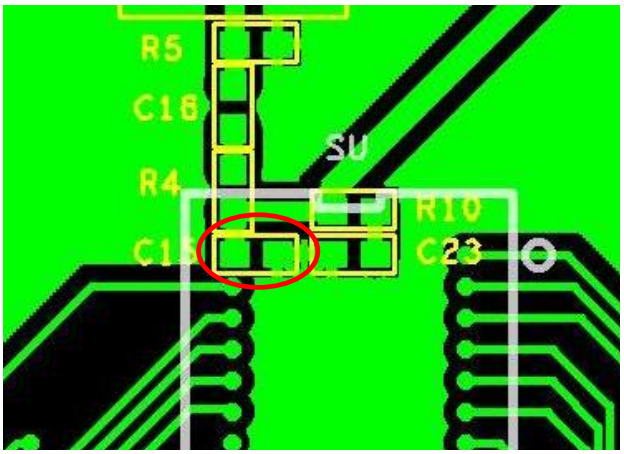
5.2.4 Decoupling Caps

Use decoupling capacitors to stabilize the power rail voltage. Place the decoupling capacitors as close as possible to their intended device, and that the current flows through them. Connect decoupling capacitor directly to device ground. Figure 19 shows an example for good decoupling capacitor placement. Decoupling capacitor should be selected such that frequencies up to one half the fastest signal transitions must be bypassed.

Key aspects of proper decoupling are given below:

- A large electrolytic capacitor (typically 10 µF –100 µF) no more than 1 inch away from the chip
  - The purpose of this capacitor is to be a reservoir of charge to supply the instantaneous charge requirements of the circuits locally so the charge need not come through the inductance of the power trace.
- A smaller cap (typ. 0.01 µF –0.1 µF) as physically close to the power pins of the chip as possible
  - The purpose of this capacitor is to short the high frequency noise away from the chip.
- All decoupling capacitors should connect to a large area low impedance ground plane through a vias or short trace to minimize inductance.
- Optionally a small ferrite bead in series with the supply pin.
  - Localizes the noise in the system.
  - Keeps external high frequency noise away from the IC.
  - Keeps internally generated noise from propagating to the rest of the system

Figure 19. Decoupling Capacitor Placement



6 Summary

The practices presented in this application note will help engineers to design their system and configure their application in such a way that it helps to improve emission levels of their system. Although emissions may be caused by more than one of the parameters discussed above. So making the right combination will help to overcome the stringent emission levels in automotive domain.

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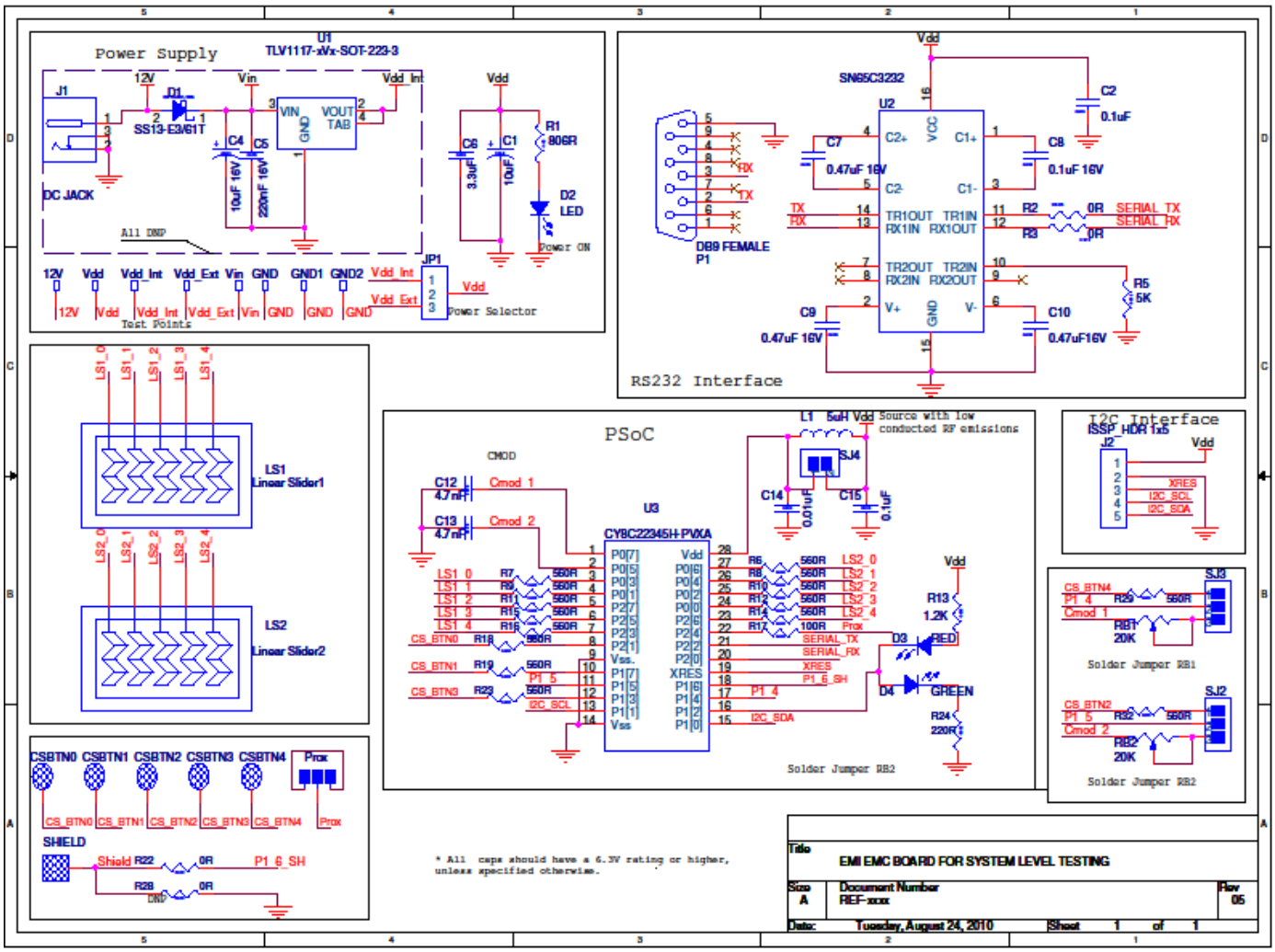
7 Appendix A

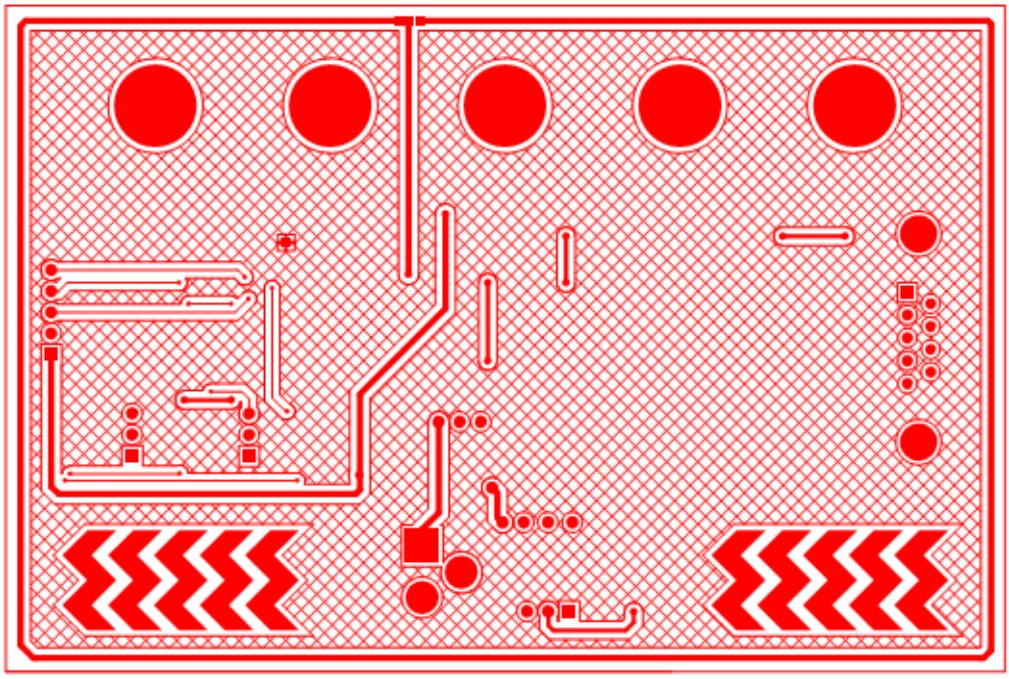
7.1 Schematics of the Test Board



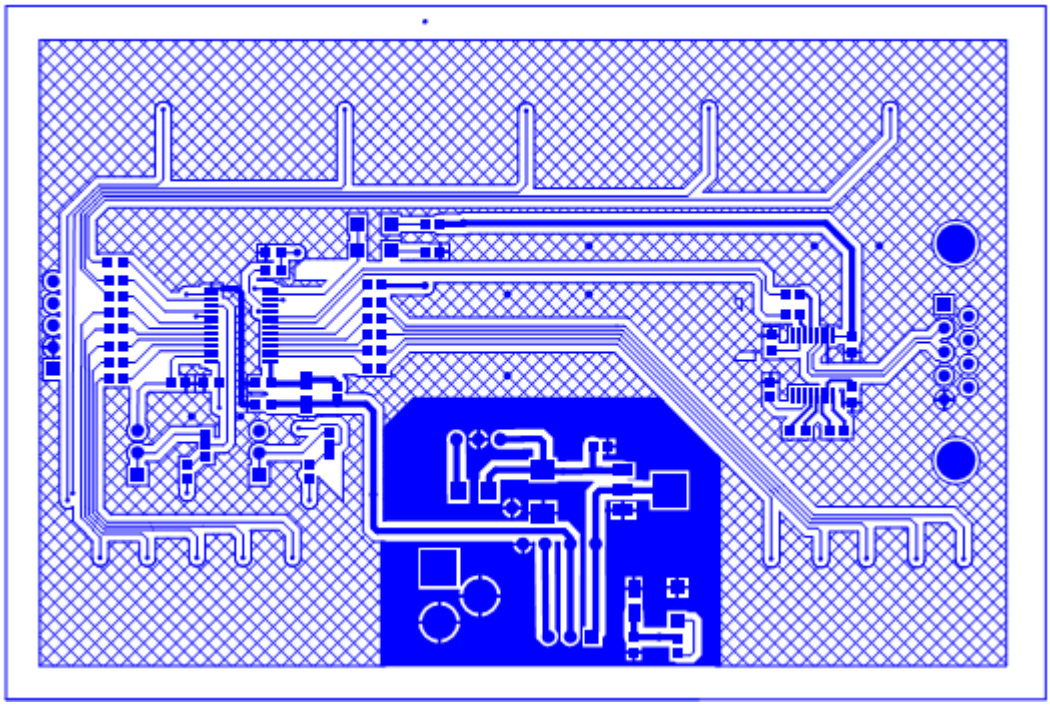
Appendix B

7.2 PCB Layout

7.2.1 Top Layer



7.2.2 Bottom Layer



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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3587521	JICG	04/16/2012	New application note.
*A	4786982	JICG	07/13/2015	Formatted the document as per new template.
*B	5713707	AESATMP9	04/26/2017	Updated logo and copyright.

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