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AN67391

PSoC® 1 - Low Distortion FSK Generator

Author: Dennis Seguine

Associated Project: No

Associated Part Family: CY8C24xxx, CY8C27xxx, CY8C28xxx, CY8C29xxx

Software Version: PSoC Designer™ 5.1

Related Application Notes: AN2336

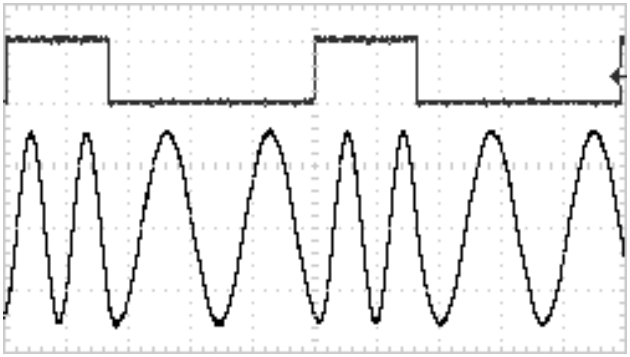
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AN67391 demonstrates means to generate Frequency Shift Keying (FSK) modulation with very low distortion and zero run-time software using PSoC® digital and analog block features.

Introduction

FSK encodes digital data to be transmitted in an analog fashion by assigning one frequency to a logical 0 and another frequency to a logical 1. Transmitting data in this manner is a simple, robust and standard method for communicating over telephone lines and a variety of other transmission media. A typical example is shown in Figure 1 with one bit at logic 1 followed by a single bit a logic 0 in a repeating sequence.

Figure 1. FSK Waveforms

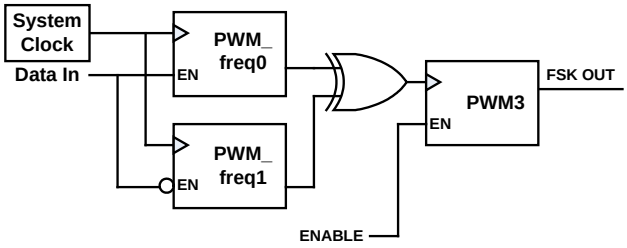


The design is demonstrated at 1200 Hz and 2200 Hz, Bell 202 standard 1200 baud modem frequencies. Common applications for these operating frequencies include telephone caller ID and Highway Addressable Receiver Transmitter (HART) modems. HART modems are used for transmission over DC power lines, often shared with 4-20 mA current loop data. The HART standard waveform, while not enforcing a specific requirement, has a relatively low distortion level. A simple square wave will not do.

Digital FSK Generation

The basic FSK generation structure uses three pulse width modulators (PWMs), as shown in Figure 2.

Figure 2. FSK Digital Block Diagram



PWM_freq1 divides the clock source to provide a fixed multiple of the output frequency at the logical 1 frequency, 160*2200 Hz. or 352 kHz

PWM_freq0 divides the clock source to provide a fixed multiple of the output frequency at the logical 0 frequency, 160*1200 Hz or 192 kHz.

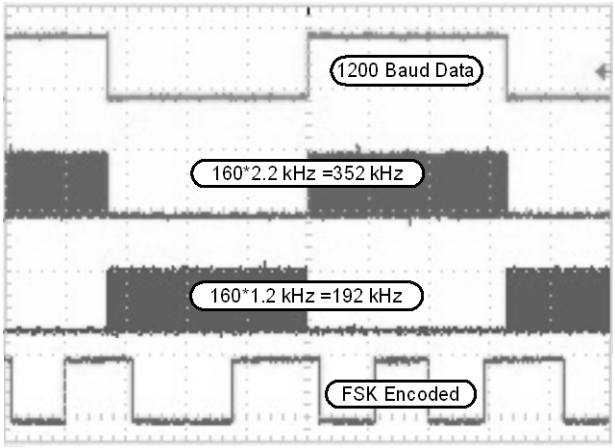
PWM3 divides the summed output of PWM1 and PWM2 by 160 to provide a square wave at one of the signaling frequencies.

The remaining trick comes in picking which frequency is transmitted. The enable inputs of PWM_freq1 and PWM_freq0 are driven by the common data signal. Typically this comes from a UART clocked at the baud rate. PWM_freq1 is enabled when the data input is high. PWM_freq0 has its enable input inverted, so that it runs when the data input is low and stops when the enable input is high.

With one of the PWM enables inverted, when the output one PWM is toggling, the other is static. The outputs are added together with an exclusive-OR gate. When one input is low and static, the output follows the other toggling input. When one input is high and static, the output is inverted from the toggling input. Thus, when one of PWM_freq1 or PWM_freq0 is static, the output follows the toggling input of the other PWM. The result is a square wave output PWM . . . . with no interrupts. The XOR is implemented in the LUT that combines two adjacent digital row outputs.

For an initial evaluation, a separate PWM with 1200 baud alternating 1s and 0s is used to provide the digital data. The input data, the two 160 times multiples of the output frequencies, and the FSK encoded signal are shown in Figure 3.

Figure 3. FSK Waveforms



The HART modem spec allows up to 20 degrees phase error in the transition from one bit to the next. Since the output frequency is derived from a 160x clock, the phase error will be between 0 and 2.25 degrees. This exceptionally clean phase transition limits the inter-symbol error and enables easier detection of the FSK data at the receiving end. What remains is turning that square wave into a respectable sine wave, or something with low enough harmonics to meet the intent of the spec.

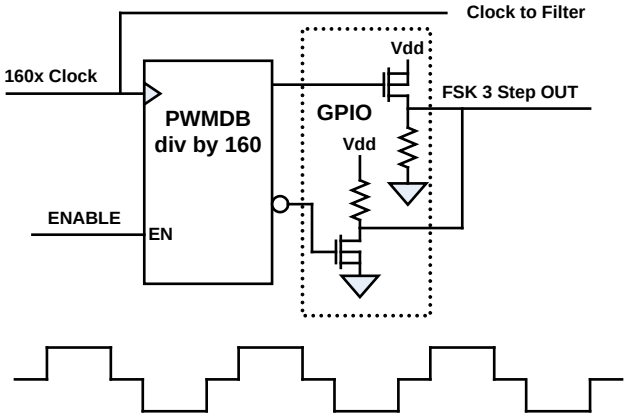
Digital Harmonic Reduction

The square wave output of PWM3 has harmonics (all ODD) that fall off as 1/n. Thus the third harmonic is down 10 dB, the fifth down 14 dB, the seventh down 17 dB, the ninth down 19 dB, and so on.

The higher harmonics are easily filtered, but it is difficult to attenuate the third harmonic because it is very close to the useful band. There are several approaches: lots of filter sections, elliptical filters with strategically placed notches, or digital waveform modifications to reduce near-band harmonics before they are filtered.

Modifying the PWM to be a PWMDB (with a dead band), a three step waveform can be generated as shown in Figure 4. The dead band is set to be one third of each half of the waveform, or 67% duty cycle.

Figure 4. PWM Deadband with Summed Waveform



One of the PWMDB's outputs is inverted and the two PWMDB outputs are added together. This is not done logically, but rather arithmetically using resistors. One way is to connect a resistor (10 k ohms is sufficient) from each PWMDB output to a common point. Easier yet is using the resistive pull-up and pull-down outputs of the PWMDB GPIO. When both outputs are high, the strong drive of one drives the output to the positive rail (V_{DD}). When both outputs are low, the strong drive of the other output drives the summing point to the negative rail (V_{ss}). When the first PWMDB output is low (pulled down) and the second PWMDB output is high (pulled up), the combined output is resistively divided at a point at $V_{DD}/2$, resulting in the three step waveform of Figure 4. The two outputs are connected externally, then also to a switched capacitor filter on one of the analog inputs.

But why does the three step waveform work so well? This waveform has a Fourier series:

$$f(t) = \sum_{n-1}^{\infty} \sin\left(\frac{n\pi}{2}\right) \frac{\sin\left(\frac{n\pi d}{2}\right)}{\left(\frac{n\pi d}{2}\right)} \sin\left(2\pi f_{SIG} t\right)$$

Where d is the duty cycle of the half wave pulse.

Parsing the equation will help understanding:

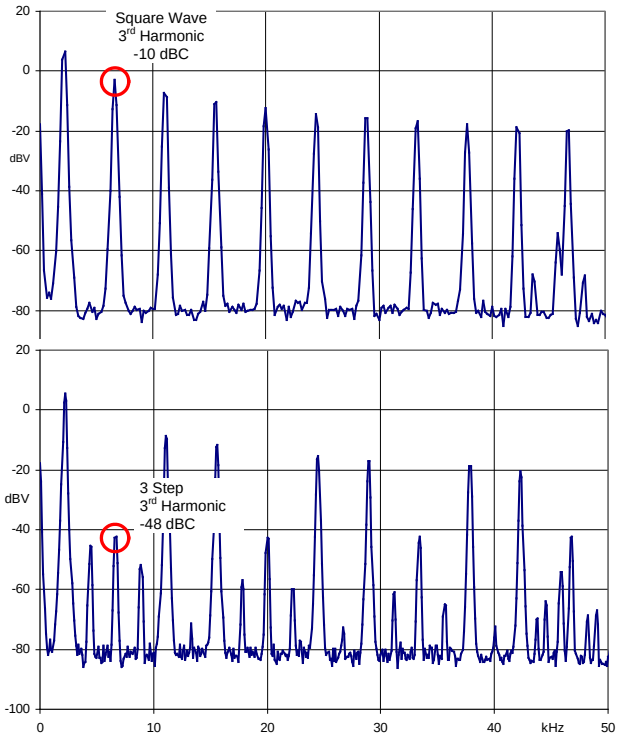
f_{SIG} is the FSK output frequency (either 1200 or 2200 Hz).

sin(nπ/2) yields zero when n is even, guaranteeing that the waveform has only odd harmonics.

sin(nπd/2) is zero when n*d is an even integer, so for d = 2/3, sin(nπd/2) when n = 3, 9, 15 . . . .

The resultant spectrum is shown in Figure 5. "dBC" refers to dB below Carrier.

Figure 5. Waveform Spectrum Comparison



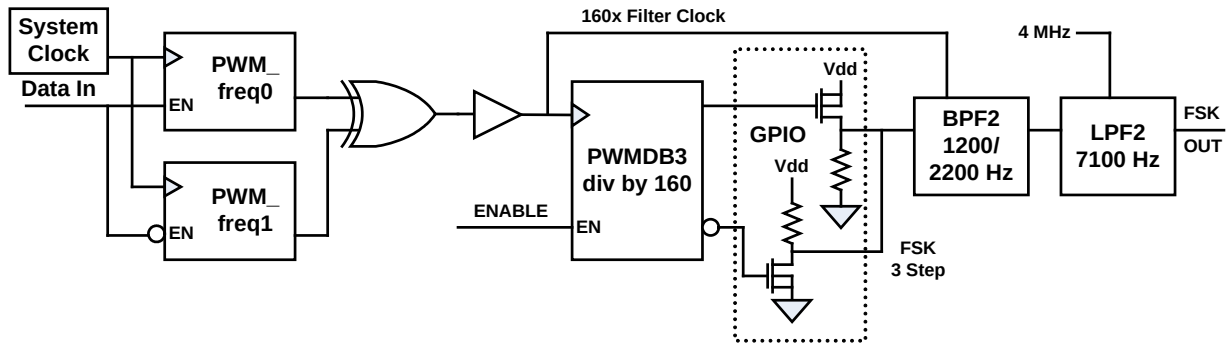
When d=0.67, the third, ninth, and other harmonics are reduced to near zero. A similar result for d = 0.8 results in suppression of harmonics 5, 15, 25 . . . . The best result is attained when the lowest harmonics are eliminated. The limit of the harmonic suppression is the matching of the resistors used in summing the signals, in this case the matching of the pull-up and pull-down resistors in the GPIOs. When d=0.75, harmonics 3 and 5 are partially attenuated; the design tradeoff is based on ease of suppression other harmonics.

Filtering Out Harmonics

The 3rd harmonic content of the waveform is less than 0.5%, a good start, but the total is not up to the standard of the HART modem. The output of the three-step generator is filtered with a switched capacitor band pass filter. The switched capacitor low pass filter is clocked at four times the sample rate. With the clock at 160 times the output frequency, the waveform is sample at 40 times per sample. The three step waveform uses the combined outputs (XORd) of two blocks, but the clock to the filter can only come from a single block selected by the analog clock multiplexer. This signal is derived by connecting the composite clock output to a DigBuf, then using this buffer output as the clock source for the analog column.

The completed digital block connection with digital signal generation and filters is shown in Figure 6.

Figure 6. Complete Block Diagram

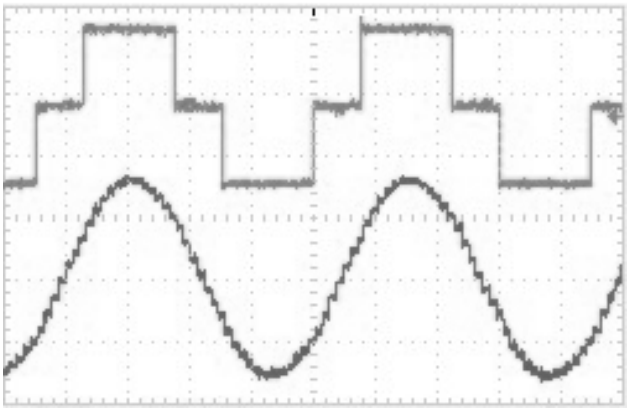


Design of the band pass filter is enabled by using either the filter wizard in PSoC Designer™ or the design spreadsheet in PSoC Designer→Help→Documentation. The input to the filter is a 5.0 Vpp signal, which is large enough to saturate the filter output unless the filter is designed to attenuate the signal. Narrow band PSoC filters have high gain, this is a mathematical limitation based on the range of capacitor values available.

While a filter bandwidth of 50 Hz would be "nice" in order to reduce harmonics, it is not achievable. At 2.2 kHz, a bandwidth of 800 Hz is achievable. This results in attenuation of the 5th harmonic by more than 20 dB (the 3rd harmonic is already attenuated by the three step waveform). Of course the filter characteristic on the 1.2 kHz signal is the same as the 2.2 kHz signal because the filter performance is determined by the synchronized over-sample clock.

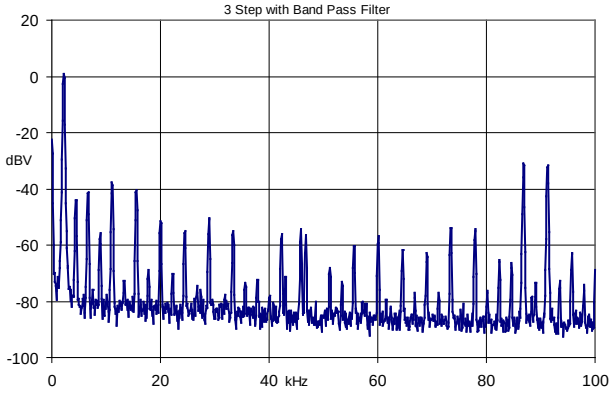
The filter output waveform is shown at 2.2 kHz in the time domain in Figure 7 and frequency domain in Figure 8.

Figure 7. Band Pass Filter Waveform



That's a nice clean sine wave although the 40 samples per cycle transitions can be clearly seen.

Figure 8. Band Pass Filter Spectrum

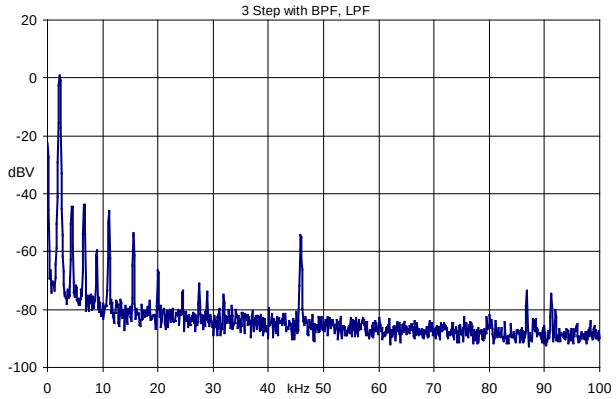


The harmonics of Figure 8 are considerably reduced from the levels shown in Figure 5. The highest harmonic is the fifth at 38.5 dB below carrier, or 1.1% of distortion. All others are lower except the lines at 87.8 and 90.2 kHz; these are the sampling aliases of the filter with a level 32 dB below carrier. The sum of the low-order harmonics and the first pair of aliases results in a signal to noise ratio of 29 dB or 3.3% distortion.

For further reduction, the band pass filter is followed by a 7.1 kHz low pass filter with a 1.0 MHz sample rate. The waveform looks even cleaner because the first filter's sampling alias is significantly attenuated, but it is hard to evaluate distortion less than 1% with an oscilloscope.

The second filter, sampled at 1.0 MHz has aliases at 1.0 MHz - 2.2 kHz and 1.0 MHz + 2.2 kHz. Sampling aliases follow a sin(x)/x pattern. As the ratio of the over-sample increases, the aliases are closer to the null points of sin(x)/x and their levels drop. The dominant signal is still the FSK, which is now over-sampled by a factor of 450, significantly reducing the alias. The low pass filter reduced the aliases from the band pass filter. The spectrum scan from 0 to 100 kHz in Figure 9 shows that the first filter's alias components are reduced to a negligible level. The line at 46 kHz is an interference from the RS232 level translator on the development board where this prototype was constructed.

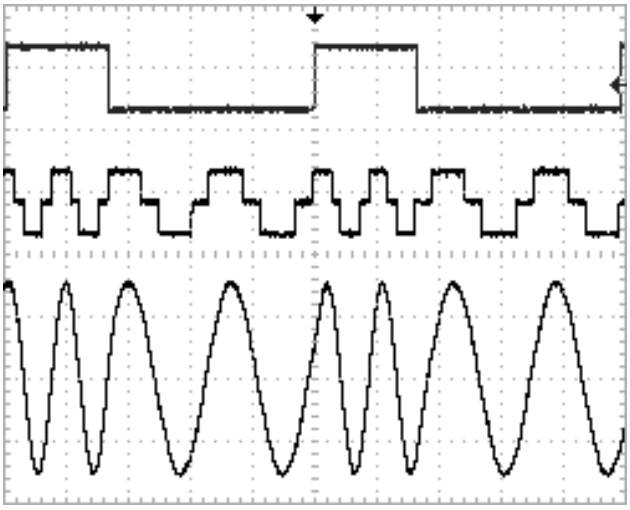
Figure 9. Second Filter (Low Pass) Spectrum



The highest harmonic is the third at -44 dB, the total distortion is less than 0.8; the highest alias is at 998 kHz at -52 dB; this is a very clean, easily generated waveform.

The final output waveform is shown in Figure 10. The steps in the waveform are from the resolution of the digital scope, not the sampling in the FSK generator.

Figure 10. FSK Output Waveform



Construction Options

The FSK generator can be a limited to a simple modulator driven by externally supplied data or it can be a part of a larger system built in the PSoC.

Digital only versions with square wave output can be constructed with only three digital blocks. A three step analog output version takes another digital block, replacing the PWM with a PWMDB. If a very clean waveform is needed, the three step waveform and both filters are used. This takes a total of 5 digital blocks and 4 analog blocks. This fits best into a 28-pin or larger part CY8C27443 or CY8C29866. If a PGA is used for waveform input to the filter instead of Port 2.1, the design will fit into the 8-pin CY8C27143 or the 20-pin CY8C27243.

If all that is required is the FSK modulator, with modest allowed harmonics and no on-chip data generation, the design can fit easily into an 8-pin CY8C24123 which has 4 digital blocks and 6 analog blocks. This version uses a PGA is to feed the digital FSK data to the filter because the 8-pin part does not have Port 2 inputs available. The filter can be either the single band pass, which will also help limit power requirements, or the combined band pass and low pass. In either case, the pin requirements are 1 for digital data input, 1 for square wave FSK data (instead of the three step waveform) to feed the filter and 1 for FSK sine wave output.

The PSoC internal main oscillator is accurate to +/- 2.5% over the full range of voltage and temperature. While this is good enough for UART communications, the HART standard requires 1% frequency accuracy. This requirement is easily met using the PSoC's 32.768 kHz external crystal oscillator with phase-locked internal main oscillator.

Resource utilization boils down to how much distortion reduction do you need, summarized in Table1.

Table 1. Resource/Performance Comparison

	# Digital Blocks	# Analog Blocks	Current mA	% Distortion
Square Wave	3	0	0.1	46.7
Square Wave 1 Filter	3	2	1.3	5.1
3 Step	4	0	0.1	39.5
3 Step 1 Filter	5	2	1.3	4.0
3 Step 2 Filter	5	4	2.5	1.0

The distortion includes harmonic distortion from the digital waveform generation plus the aliasing products from the switched capacitor filtering. Distortion can be further reduced using active RC filters (such as Sallen and Key) with the PSoC PGA as the active element.

Software

The entire code to operate the FSK modulator is listed below in C.

```
PWM_freq0_Start();
PWM_freq1_Start();
PWMDB8_1_Start();
BPF2_1_Start(MEDPOWER);
LPF2_1_Start(MEDPOWER);
```

Starting and stopping the modulator output is done by controlling the PWMDB8 Enable or Kill inputs. This design has a significant advantage over direct digital synthesis techniques using a DAC in that zero run-time code execution is required. When implemented as part of a complete system, this leaves the processor available to do what processors do best, calculate and control.

Associated Project

The associated project is built in a CY8C27443. Data is simulated by a PWM16. This can be replaced by a UART and clock generator or the modulator can be fed digital data through a global input.

Summary

This signal generation technique is useful in many applications, not just FSK transmission. The idea is to reduce as much of the harmonic content as possible prior to analog filtering, then in the filtering process take as much advantage as possible of PSoC switched capacitor signal processing.

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