Please note that Cypress is an Infineon Technologies Company.
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

AN64475

PSoC® 1 - Optimizing Cascaded Switched Capacitor Filters

Author: Dennis Seguine
Associated Project: Yes
Associated Part Family: NA
Software Version: PSoC® Designer™ 5.1
Related Application Notes: AN67391

If you have a question, or need help with this application note, contact the author at seg@cypress.com.

AN64475 demonstrates how PSoC® 1 switched capacitor band pass filters (BPF2, BPF4) and elliptical low pass filters (ELPF2 and ELPF4) can be combined to provide excellent near out-of-band rejection for communications applications. The included project demonstrates a filter system tuned to the requirements of a 60 kHz Binary phase shift keyed (BPSK) modem receiver. The design technique can be extended to other requirements using the filter design wizards in the user modules in PSoC Designer.

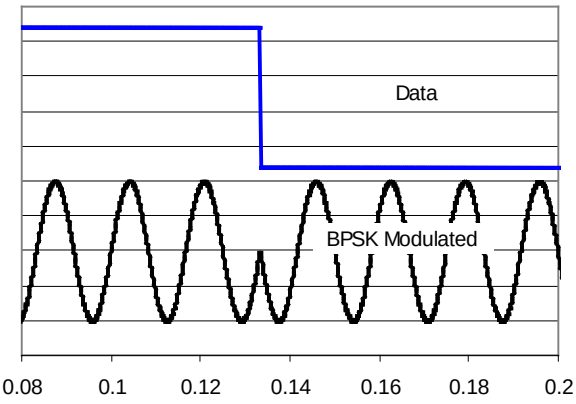
Introduction

Sometimes you need more near-out-of-band attenuation than you can get with a simple band pass filter. The design example chosen here is a key component in a BPSK modem. It filters 60 kHz BPSK data and rejects VERY LARGE 120 kHz noise. In some applications, the offending 120 kHz tone may be as much as 70 dB greater than the 60 kHz BPSK signal. The filter must push this tone down AND supply an adequate SNR (10 dB is sufficient) at its output to drive a separate BPSK demodulator.

BPSK Basics

The first problem is figuring out the nature of the signal. BPSK (binary phase shift keying) is at a constant frequency, but the phase is inverted at the bit transition. The 60 kHz BPSK waveform is modeled below:

Figure 1. BPSK Waveform



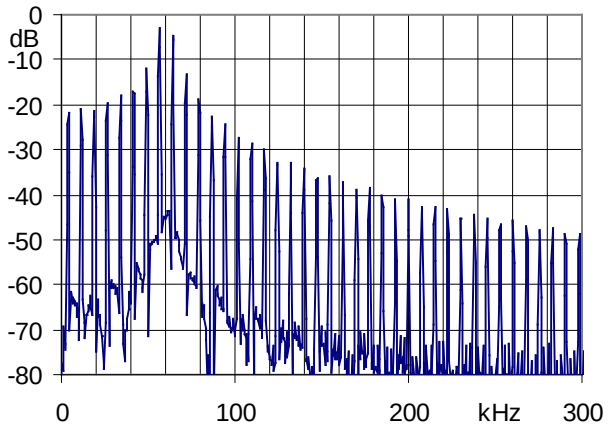
The data is carried in the phase, not the frequency, in spite of the fact that the signal shifts in frequency with the data as per

$$V\,\mathrm{mod}(t) = V * \sin\left[2\pi ft + D\pi\right]$$

Where f = 60 kHz
D = data, 0 or 1

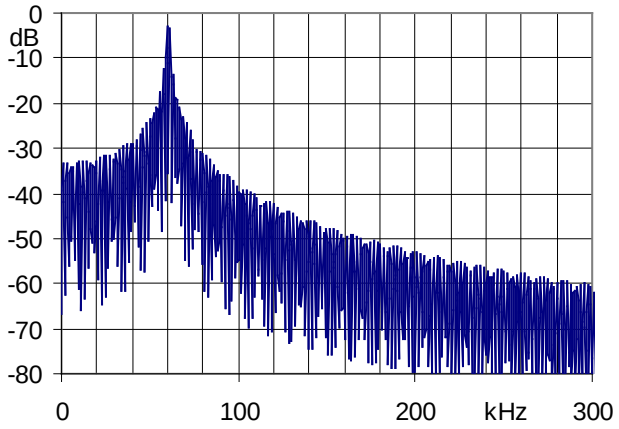
Data changes are synchronous with the clock, switching at a maximum of every 8 cycles of the 60 kHz waveform. This results in the spectrum:

Figure 2. FFT: BPSK at Maximum Baud Rate



When the data is unchanging, the carrier is at 60 kHz with no phase modulation, so the spectrum shows a single line frequency. At slower data rates, the frequency excursion of the waveform is not as large as that of maximum baud rate. The spectrum for data changes at half of the maximum rate is:

Figure 3 FFT: BPSK at Maximum Baud Rate/4



The maximum frequency excursion from the nominal carrier is 60 kHz/(2*n) where n is the number of cycles per bit. Typical modulated data looks essentially random in frequency, so the spectrum varies between the spectra of Figure 2 and Figure 3. There are a lot of harmonic tones in these plots. These harmonics are modulation products based on a pure sine wave; they are not "distortion."

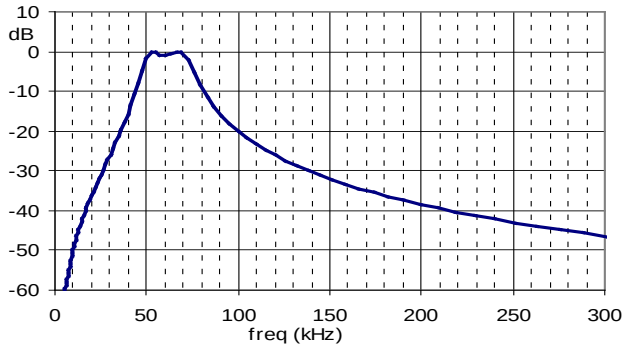
Filter Requirement Definition

The bandwidth of the filter must be sufficient to allow settling of the waveform at the phase transition of the data. At least several cycles should be allowed at each bit value for the phase detector in the BPSK demodulator to work properly. A bandwidth of 22 kHz was selected. A Chebyshev band pass filter has attenuation of the form

$$H(f) = -10\log\left[1+\varepsilon^2\left(2\left(\frac{f_S - f_C{}^2/f_S}{BW}\right)^2 - 1\right)^2\right]$$

where f_S = signal frequency,
f_C = filter center frequency,
ε = ripple parameter
=0.156 for 1.0 dB ripple), and
BW = filter bandwidth = f_C/Q

Figure 4. 1.0 dB Two Pole-Pair Chebyshev Band Pass Nominal Filter Response.

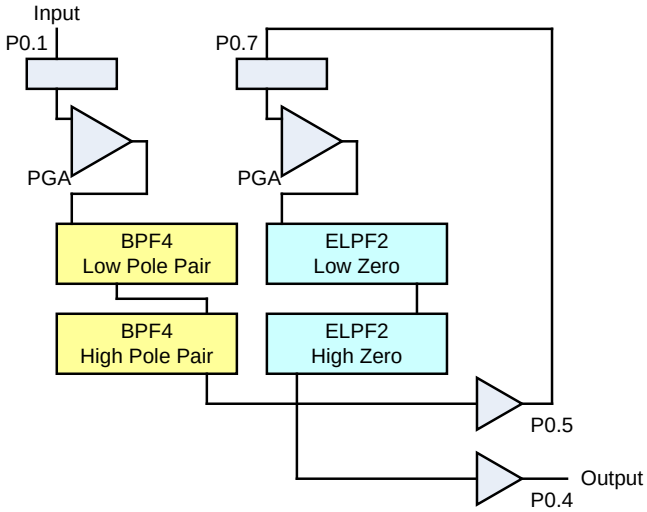


This filter has an attenuation of 24 dB at 120 kHz. This reduces the offending out-of-band signal by only a factor of only 20. The solution to greater attenuation is a notch filter. The elliptical low pass filter (ELPF2) user module provides a low pass filter with an adjustable notch. An ELPF4 user module provides a flatter response in the band and a pair of adjustable notches. The band pass filter is still needed to eliminate noise from the low frequency side.

Filter Realization

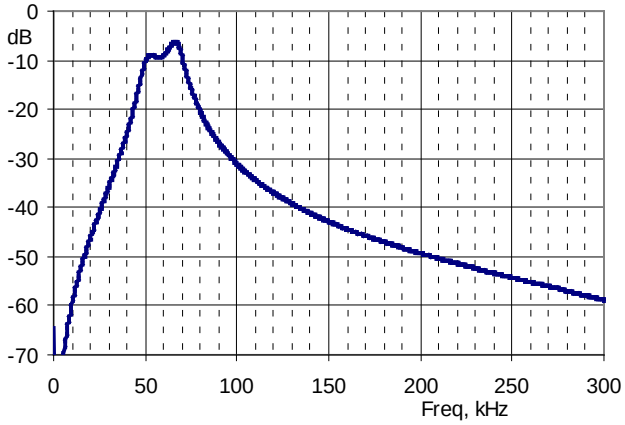
The filter design consists of a 60 kHz 4 pole band pass filter followed by two sequential two pole elliptical low pass filters. PGAs are required to couple the signals to the appropriate block inputs. Elliptical low pass filters (and notch filters) require the same signal to be fed to both switched-capacitor blocks. This limits placement to horizontal locations.

Figure 5 . Filter Block Diagram



The notches of the elliptical low pass filters are set to attenuate the 120 kHz interfering signal. The sample frequency, common to all filter sections, should be selected to be as high as possible to eliminate the possibility of aliasing. The band pass filter was designed using the filter design wizard built into PSoC Designer. The BPF4 response was measured using a spectrum analyzer and matched the design requirement, albeit with larger ripple.

Figure 6 Measured Band Pass Filter Response



The ELPF2's notch characteristic causes some frequency-dependent attenuation in the signal band, so the band pass filter's components are slightly "tweaked" to pick up the higher frequency signal. This can be more easily observed using the excel spreadsheet in the "help/documentation/filter design" folder in PSoC Designer. Filter plots are normally done using logarithmic frequency axis, but in this case, the linear frequency does a better job of showing the increments and response at 60 kHz, the edges of the modulated frequency range and the level of the 120 kHz interference.

The ELPF4 filter was initially designed at 70 kHz, but the high order pole pair required a very low damping ratio, which could not be achieved at this frequency because of the available cap values and ratios at the 1.5 MHz sample rate. Accordingly, the ELPF4 user module was placed but the values were calculated from two separate ELPF2s.

Ideally, sequential identical notch filters at 120 kHz would be expected to give the best performance (that is deepest notch). There is, however, some cross-talk caused by capacitive leakage from the output of one SC block opamp into the input of the adjacent opamp. This is a known issue and limits the performance of multi-block user modules including both filters and DACs. As a result, the notches are not as deep as planned. The spreadsheet implies that each section is capable of 45 dB attenuation at the center of the notch. In fact, even with adjustments to realign one of the notches for the greatest TOTAL depth, the best found for this design is about 36 dB. Identical notches at 120 kHz were actually worse by 6 dB at 120 kHz. The "nominal" design and the adjusted design are shown in Figure 7, with the non-equal filter section performance indicated by the RED line being preferable.

Figure 7 Notch Location Comparison

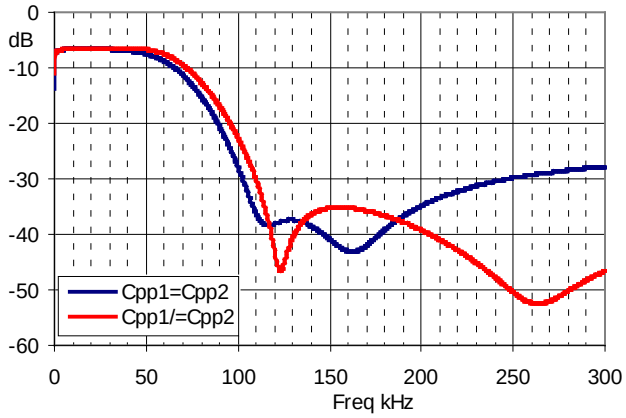
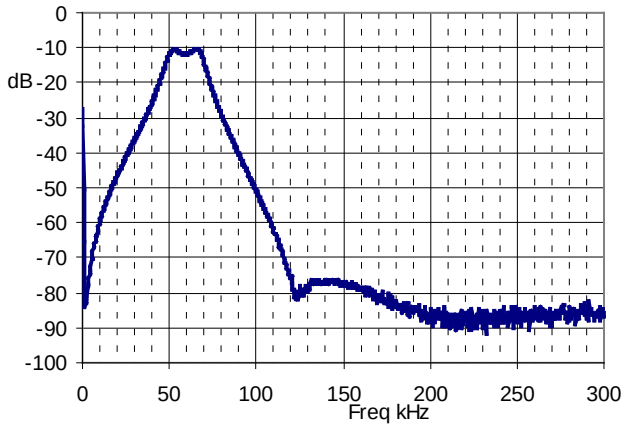


Figure 8 shows the measured composite of the two filters. A single pole RC filter was added from the output of the BPF4 to the input of the first ELPF2 (P0.5 to P0.7) to yield another 5 dB for a total of 68 dB attenuation at 120 kHz.

Figure 8 Composite BPF4 +2 * ELPF2 Response

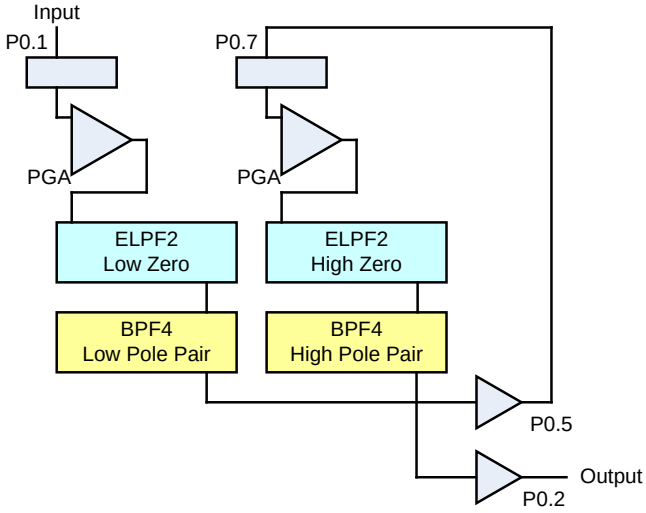


This is not quite to the -81 dB required. The problem is cross-talk between the two halves of the ELPF4. The output of the block in the upper row "leaks" into the inverting input of the lower filter's input block.

Topology Optimization

A re-ordering of the blocks separates the notch filters. The development models for the elliptical filters are not exact; it takes a little tuning to find the correct Cpp value to precisely tune the notch to the desired frequency.

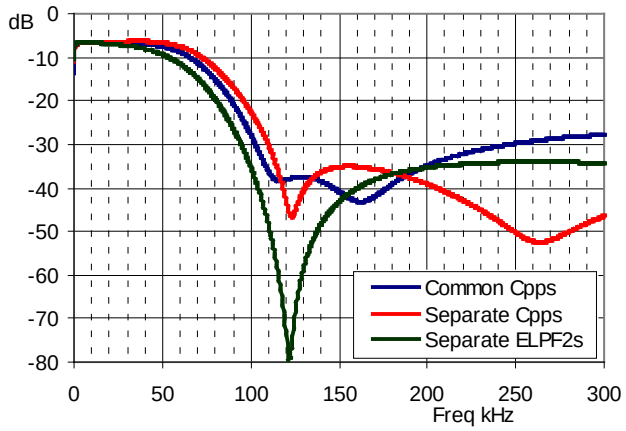
Figure 9 Adjusted Block Placement to Reduce Cross-Talk



The output of the first two filter sections on P0.5 is routed to P0.7 for input to the second set of filters, but it can be connected to P0.5 to save a pin with no cost to performance.

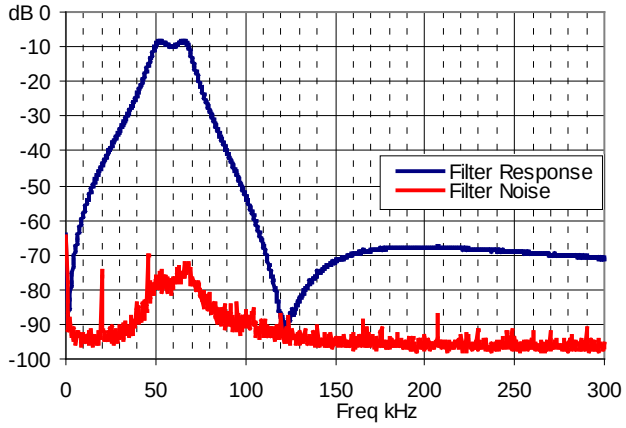
A test of the ELPFs without the band pass connected, Figure 10, shows that the isolation works. The attenuation at the notch frequency is >30 dB better than either of the earlier attempts at aligning the notches to fit signal requirements.

Figure 10 2*ELPF2 Topology Selection Measured Response



The composite filter now meets the required 81 dB attenuation spec at 120 kHz. The notch may in fact be a little bit better, but the limit in the measurement is the noise of the circuit. The attenuation above 200 kHz is not as low and not as deep as the earlier structure, but this performance at 120 kHz is more critical than the high-out-of-band response in this application. The self noise of the filter was measured with a bandwidth of 100 Hz and plotted with the frequency response.

Figure 11 Complete Filter Transfer Function and Output Noise



Firmware

The PSoC in this project is emulating a fixed-function filter. The total code is limited to a few lines of start commands; there is zero run-time code and no interrupts:

```
PGA_1_Start(PGA_1_HIGHPOWER);
PGA_2_Start(PGA_2_HIGHPOWER);
BPF2_1_Start(BPF2_1_HIGHPOWER);
BPF2_2_Start(BPF2_2_HIGHPOWER);
ELPF2_1_Start(ELPF2_1_HIGHPOWER);
ELPF2_2_Start(ELPF2_2_HIGHPOWER);
```

Filter Performance Testing

The performance of this filter system was tested using an HP3585A spectrum analyzer, which uses a tracking sine wave generator. Care should be taken in determining drive levels so the filters do not saturate. Evaluation of narrow frequency notch filters should be done with the minimum possible bandwidth in order to accurately display the location and depth of the notch.

Design Extensions

This filter system was designed for unity gain at 60 kHz. The maximum input is 1.5 Vrms to maintain adequate headroom on the 5.0 V supply. The input PGA and first ELPF2 stage of the filter must operate at unity gain to avoid saturation. Gain can be added to the both stages of the band pass filter. A gain of 28 dB can be easily added to the PGA between the first band pass filter and second elliptical low pass filter. Gain cannot be added in the elliptical low pass filter because the C1 value that normally sets gain interacts with the zero location.

The expected load for this filter is a demodulator which utilizes a nominal square wave. This is realized by connecting the comparator output of the second band pass filter to the comparator bus; a DigBuf connects the comparator bus to the pin of the user's choice. The demodulator is another interesting PSoC problem, but this one is out of resources. Gain control and BPSK demodulation of the filter output will be done in a separate PSoC.

Summary

Band pass filters with out-of-band notch depth greater than 75 dB are demonstrated in PSoC 1. The 60 kHz BPSK filter can fit into any CY8C27xxx, 28xxx, or 29xxx part using only two resistors for biasing and an input capacitor of nominal value. The design techniques can be extended to any PSoC switch capacitor filter operating range from 100 Hz to 150 kHz using the design wizards built into PSoC Designer.

About the Author

Name:	Dennis Seguine
Title:	Member of Technical Staff Cypress Semiconductor
Contact:	seg@cypress.com

Document History

Document Title: AN64475 - PSoC® 1 - Optimizing Cascaded Switched Capacitor Filters

Document Number: 001- 64475

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3048156	SEG	10/07/2010	New Application Note
*A	3180401	SEG	02/23/2011	Update title, abstract, convert project to PSC 5.1 SP1
*B	4169370	SEG	10/23/2013	Updated in new template. Completing Sunset Review.

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/usb
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support

PSoC is a registered trademark of Cypress Semiconductor Corporation. "Programmable System-on-Chip," PSoC Designer is trademarks of Cypress Semiconductor Corporation. All other trademarks or registered trademarks referenced herein are the property of their respective owners.

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

Phone : 408-943-2600
Fax : 408-943-4730
Website : www.cypress.com

© Cypress Semiconductor Corporation, 2010-2013. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.
This Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.
Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.
Use may be limited by and subject to the applicable Cypress software license agreement.