AN60321

Peak Detection with PSoC® 3 and PSoC 5

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Associated Part Family: CY8C3xxx, CY8C5xxx

Software Version: PSoC® Creator™ 2.0

Related Application Notes: None

If you have a question, or need help with this application note, contact the author at drsw@cypress.com

Abstract

Techniques for implementing a peak detector in PSoC® 3 and PSoC 5 is explained in this Application Note. Some of the peak detector designs have been encapsulated as PSoC Creator™ components for easy reuse.

Introduction

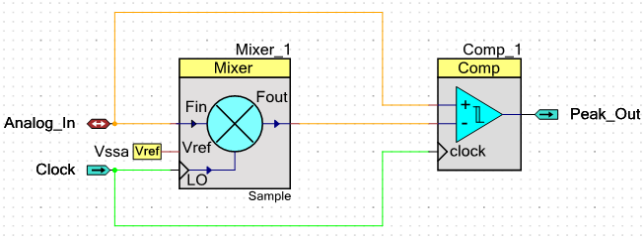
A peak detector detects the peaks of an input waveform and produces an output based on the detected peaks. The output of the peak detector depends on the type of peak detector used. Some peak detectors produce a digital output consisting of information about when positive and negative peaks of a waveform occur. In this case, the digital information can also be used to determine the direction of the slope of the input waveform. Other peak detectors produce an analog output with a magnitude equal to the last detected peak, or the magnitude of the maximum peak encountered.

Accurately detecting the peaks in an input waveform can be useful in a variety of different applications. This application note describes how these three peak detection methods are implemented in PSoC 3 and PSoC 5.

Peak Detector Using Sample and Hold

One method for constructing a peak detector uses a comparator and a down-mixer acting as a sample and hold. When the slope of the input is positive, the output of the peak detector will be high. When the slope of the input is negative, the output of the peak detector will be low. Positive peaks are represented with a falling edge on the output, and negative peaks are represented with a rising edge. Figure 1 shows a schematic for this method.

Figure 1. Peak Detector with Sample and Hold

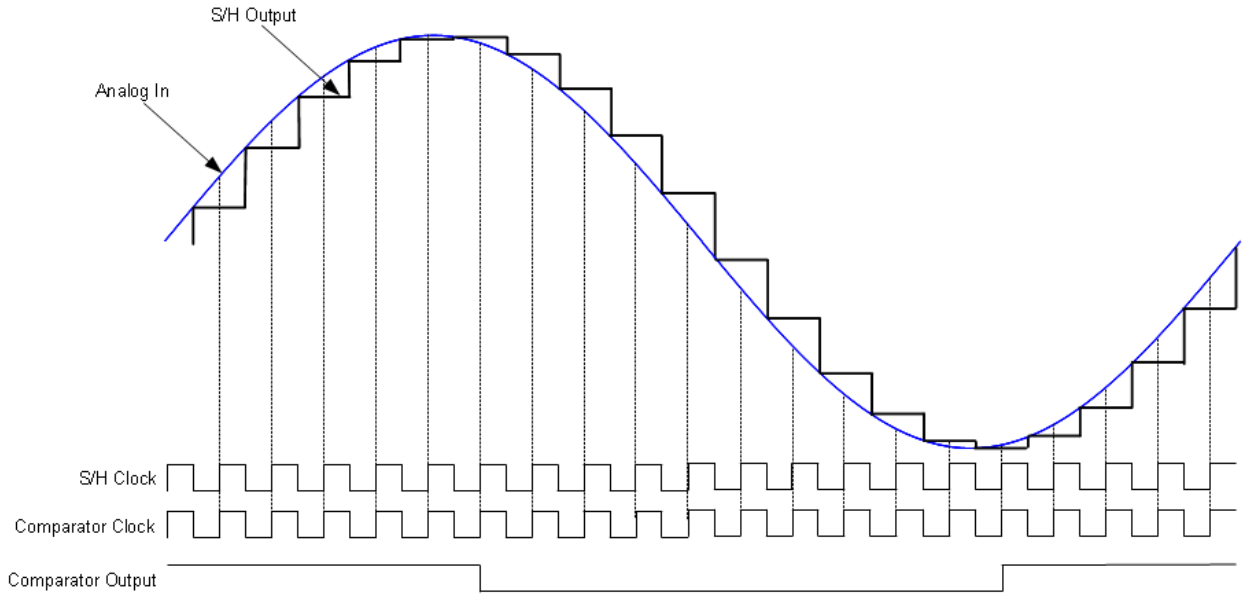


A down mixer is used as a sample and hold. The sample and hold creates a time delay on the input signal, which is fed to a comparator and compared to the original input signal. The output of the sample and hold is held on the falling edge of the sample (LO) clock. The comparator is clocked on the rising edge of the sample clock to ensure the sampled signal is stable and appropriately delayed from the input signal.

There is approximately 10 mV of hysteresis built into the comparator. This helps ensure that slowly moving voltages or slightly noisy voltages will not cause the output of the comparator to oscillate. Enabling hysteresis in the comparator is recommended for most input signals to reduce false peak detections.

Figure 2 shows a sinusoidal input waveform. When the slope of the input waveform is positive, the sample and hold output is less than the input waveform at each rising edge of the comparator clock, so the output of the comparator is high. When the slope of the input waveform is negative, the sample and hold output is greater than the input waveform at each rising edge of the comparator clock, so the comparator output is low.

Figure 2. Sample and Hold Peak Detection Waveform



To accurately detect each peak, the sample clock frequency must be adjusted to meet the frequency and noise characteristics of the input signal. As the input sample clock frequency increases, the delay between the peak of the input waveform and the output of the comparator decreases. However, the increased frequency also makes the circuit more susceptible to false peak detections because of noise. This is because there is less difference between the input waveform and the sample and hold output at higher frequencies. Decreasing the input sample clock frequency will increase the delay between the peak of the input waveform and the output of the comparator, but will also be less susceptible to erroneous peak detections due to noise.

Figure 3 shows the effect when the clock speed is set too high. The output of the comparator triggers very close to the peaks of the waveform, but the output triggers multiple times because of noise and a slowly changing input signal. In this case, the clock rate is 200x the frequency of the 1 V peak-to-peak input sine wave.

Figure 3. Clock too Fast

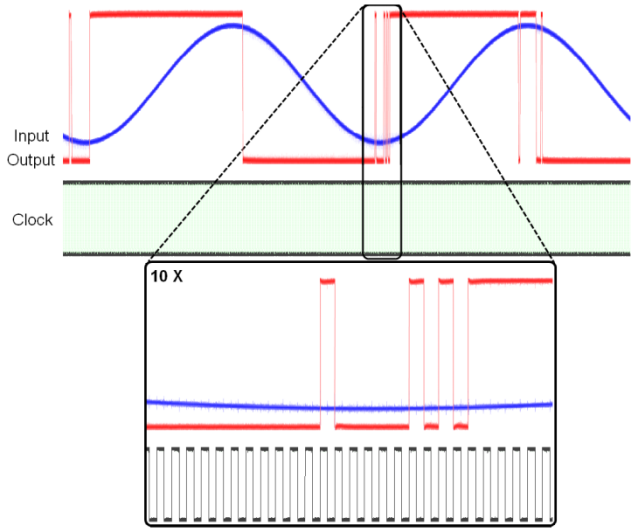


Figure 4 shows the effect when the clock speed is set too low. Notice that the output should be high during the positive slope; the output is severely delayed from the input waveform. Some peaks may be missed altogether. In this case, the clock rate is 2.5x the frequency of the 1 V peak-to-peak input sine waves; the input is sampled only two or three times per cycle.

Figure 4. Clock Too Slow

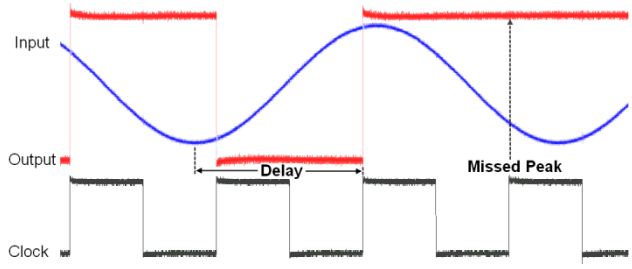
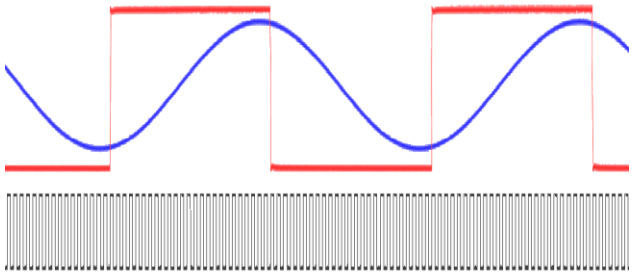


Figure 5 shows the output when the correct clock is selected. There is very little delay between the input peaks and the output; there are no erroneous triggers or missed peaks. In this case, the clock rate is 50x the frequency of the 1 V peak-to-peak input sine wave.

Figure 5. Correct Clock Selection

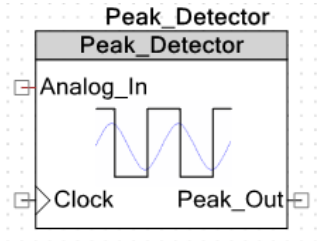


The appropriate clock speed differs for each application, depending on the frequency and noise characteristics of the input waveform.

Note The LO Frequency parameter for the sample and hold component must be set to match the input clock. This parameter is used to determine the appropriate values for the input and feedback resistance of the mixer opamp circuit. The maximum LO input frequency supported by the mixer block is 4 MHz.

For easy reuse, the hardware-based design for this peak detector is encapsulated as a component in a PSoC Creator library project. Figure 6 shows the component symbol.

Figure 6. Sample and Hold Peak Detection Component



Peak Detector Using an SIO Pin

An alternative peak detecting method to the sample and hold technique can be created using a special I/O (SIO) pin in PSoC 3 and PSoC 5. SIO pins provide a programmable input threshold, which allows the SIO pin to function as an analog comparator. When a signal is supplied as an input threshold, it passes through a reference generator block. The reference generator block introduces a time delay of approximately 200 ns into the threshold signal. This time delay, similar to the delay introduced by the sample and hold component used in the last example, enables the SIO to be used as a peak detector.

Figure 7 shows the block diagram for an SIO peak detector, which requires 2 pins: one SIO input pin and one analog input pin. The input signal is tied to both the SIO input and to the SIO threshold input through an analog pin. The threshold input signal is delayed and compared to the original input signal using the differential input buffer of the SIO.

Figure 7. SIO Peak Detector Block Diagram

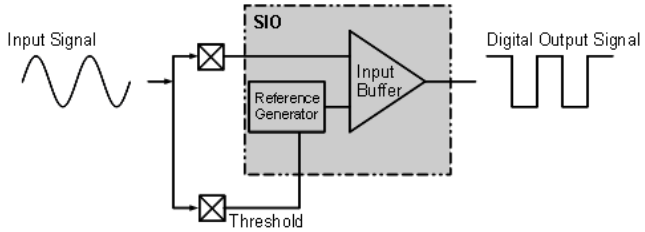
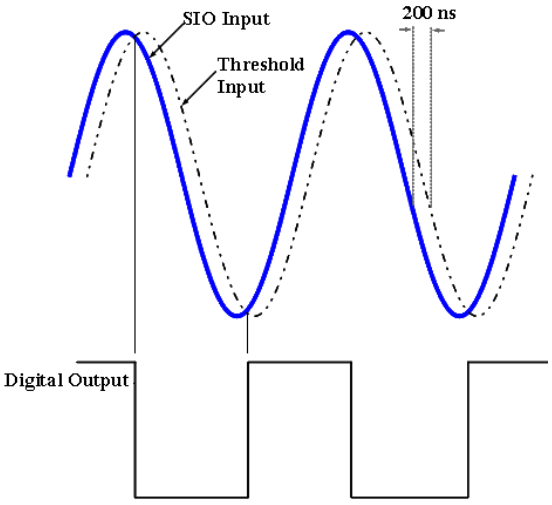


Figure 8 shows the expected waveforms for the SIO peak detector circuit. The threshold input is delayed by approximately 200 ns, which allows the differential input buffer (acting as a comparator) to detect the peaks in the input waveform.

Figure 8. SIO Peak Detector Waveform



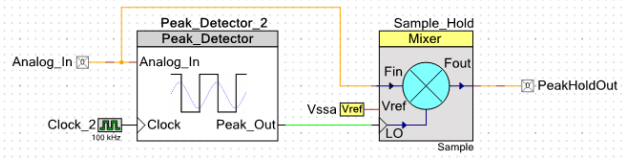
The SIO has approximately 50 mV of hysteresis. This, combined with the 200-ns delay induced by the reference generator, limits the frequency range of this peak detector. With a 1 V peak-to-peak sine wave input, the frequency is limited to a range of approximately 250 kHz to 1.25 MHz. However, the frequency range also depends on the amplitude of the input signal and the amount of noise in the system. An additional RC delay circuit can be added to the threshold analog input to induce additional delay. This will enable the peak detector to work with lower frequency signals.

Peak and Hold

Another useful form of a peak detector is a peak and hold. The peak detectors presented earlier in this application note detect the peak locations of the input waveform, but they do not detect the magnitude of the peaks. A peak and hold detector is useful in applications where the ADC is not fast enough to accurately measure the peaks of a waveform.

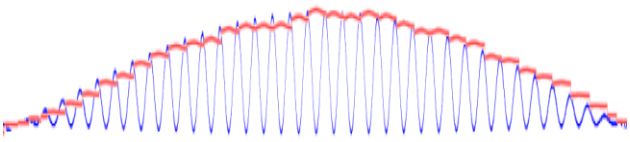
A peak and hold circuit can be created using a peak detector and an additional sample and hold component. The schematic for a peak and hold is shown in Figure 9.

Figure 9. Peak and Hold Schematic



At every peak from the peak detector component, the original input waveform is sampled by another sample and hold component. Because the output of the sample and hold is held on the falling edge of the input clock, each peak is held at the output until the next peak is detected. To create a negative peak and hold, simply invert the output polarity of the peak detector component. The output of the peak and hold circuit is shown in Figure 10.

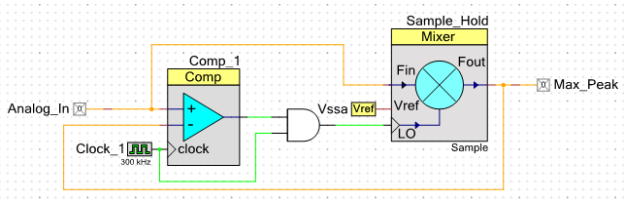
Figure 10. Peak and Hold Waveform



Maximum Peak Detector

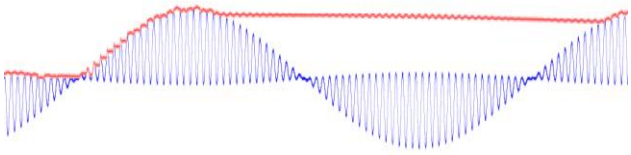
Certain applications require a peak detector that holds the maximum peak of a given input waveform. This can also be created with a comparator and a sample and hold component. The schematic for a maximum peak detector is shown in Figure 11.

Figure 11. Maximum Peak Detector Schematic



With this configuration, the sample and hold component is clocked only if the analog input is greater than the last maximum value held at the output. When the analog input is greater than the last held value, the sample and hold is clocked to update the output to a new maximum value. Comparator hysteresis is not needed for this configuration. Figure 12 shows the output waveform for this peak detector.

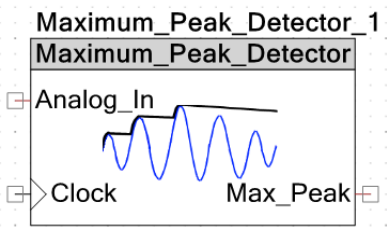
Figure 12. Maximum Peak and Hold Waveform



The output of the sample and hold will decay over time. Refer to the Mixer datasheet for specifications on this droop voltage. The output of the sample and hold will droop towards the supplied reference voltage for the sample and hold component. By changing your reference to Vdda and inverting the comparator polarity, a minimum peak detector can be created.

For easy reuse, the hardware-based design for the maximum peak detector is encapsulated as a component in a PSoC Creator library project. This component supports both maximum and minimum peak detection. The component symbol is shown in Figure 13.

Figure 13. Maximum Peak Detector Component Symbol



Summary

This Application Note presents three unique methods of peak detection with PSoC 3 and PSoC 5. Solutions have been provided to extract the peak timing, slope direction, peak amplitude, and maximum peak amplitude from an input waveform. Peak detection can be useful in a variety of different applications including magnetic card readers, ECG's, detecting the amplitude or timing of analog sensor output signals, and many more useful and interesting applications.

Attached Project Summary:

Library Project Peak_Detector_Component.cywrk:

This library project contains the implementation of two components for easy reuse in other designs.

- Peak_Detector: Sample and hold-based peak detection component with digital output.
- Maximum_Peak_Detector: Component to detect and hold the maximum peaks of a given waveform.

AN60321-Proj.cywrk:

This workspace contains four example projects to demonstrate the techniques from this application note.

- *A_SH_Peak_Detector:* Demonstrates use of the Peak_Detector component.
- *B_SIO_Peak_Detector:* Demonstrates peak detection using an SIO pin.
- *C_Peak_Hold_Detector:* Demonstrates peak and hold implementation using the Peak_Detector along with a sample and hold component.
- *D_Maximum_Peak_Detector:* Demonstrates a maximum peak detector using the Maximum_Peak_Detector component.

Note that in PSoC Creator 1.0 this workspace will generate a total of three warnings about entering the correct LO clock frequency into the mixer components. This is simply a reminder to enter in a frequency, which has already been completed in these sample projects. These warnings can be ignored. If PSoC Creator 2.0 or later is used these warning should not appear.

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2899480	DRSW	03/25/2010	New application note
*A	2991597	SRIH	07/22/2010	Fixed branding discrepancies
*B	3154800	DRSW	01/13/2010	Updated for PSoC Creator 1.0. Added note about temporary project warnings.
*C	3451277	DRSW	11/30/2011	Template update Updated projects and components for PSoC Creator 2.0. Fixed typo in About the Author section Updated section covering warnings to inform users the warning will only occur in Creator 1.0, not in 2.0.
*D	3562896	DRSW	03/26/2012	Updated header with author email contact information Added a few common peak detection applications to the summary

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