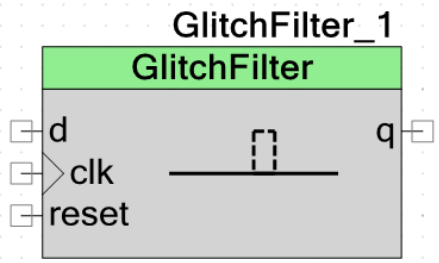
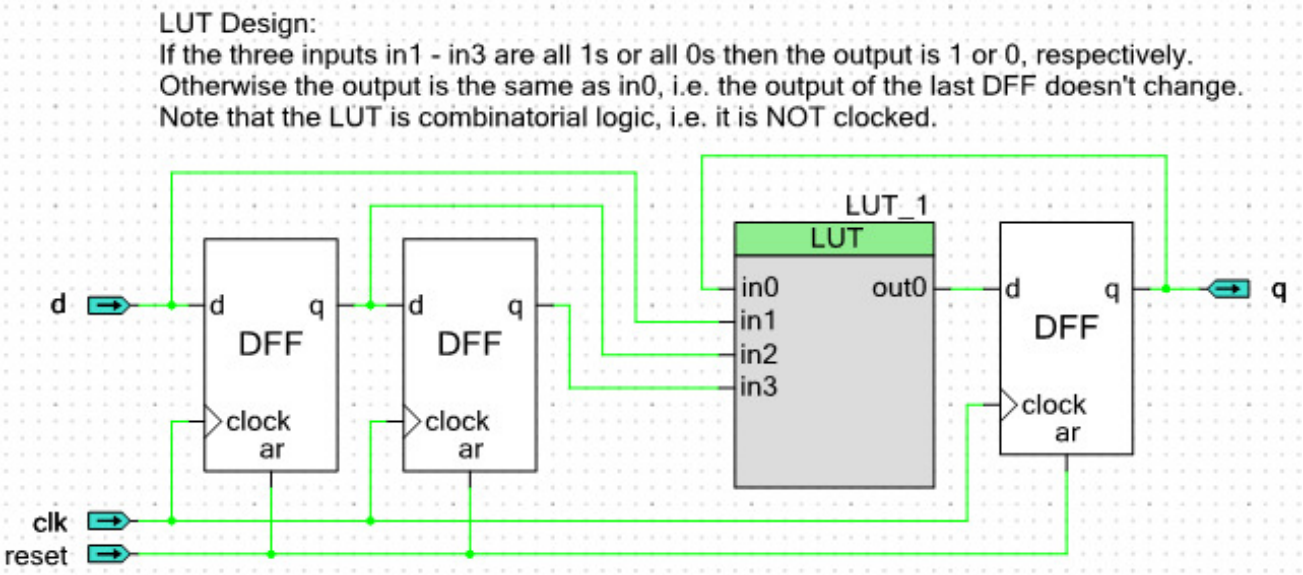
GlitchFilter
1.40

Features

- Eliminates unwanted “glitch” pulses on digital input lines



Schematic



General Description

Glitch filtering is the process of removing unwanted pulses from a digital input signal that is usually high or low. Glitches frequently occur on lines carrying signals from sources such as RF receivers. Electrical or in some cases even mechanical interference can trigger an unwanted glitch pulse from the receiver.

This design outputs a ‘1’ only when the current and previous N samples are ‘1’, and a ‘0’ only when the current and previous N samples are ‘0’. Otherwise the output is unchanged from its current value.

Both the clock frequency and an appropriate value for N depend on (a) anticipated glitch pulse width relative to sample period, (b) delay through the filter, and (c) resource usage – the number

of DFFs required is equal to N and the number of LUT inputs is equal to N + 2. In this component N is set to 2, which is an adequate value for most applications.

For more details on glitch filtering please see application note AN60024.

When to use a GlitchFilter

A GlitchFilter concept component can be used with any digital input, however it is typically associated with noise interference on a line that is connected to an input pin. Since it does a function that could otherwise be done by firmware, it can be used when a firmware-based glitch filter solution is not practical.

Input/Output Connections

This section describes the various input and output connections for the Debouncer. An asterisk (*) in the list of I/Os states that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.

d – Input

The input that is sampled. It is usually connected to an input Pin component.

clk – Input

Clock used to sample the ‘d’ input. Its frequency depends on anticipated glitch pulse width and delay through the filter.

reset – Input

Resets all of the component DFFs to a ‘0’ output. Note that a DFF is reset to ‘0’ output at device reset. If this input is not needed, it can be connected to a Logic Low ‘0’ component.

q – Output

This output is set to logic ‘1’ when the current and previous N samples are logic ‘1’, and logic ‘0’ when the current and previous N samples are ‘0’. Otherwise the output is unchanged from its current value.

Parameters

The GlitchFilter concept component has no configuration parameters.

Placement

The GlitchFilter concept component is placed in the PLD portion of one or more of the UDBs in PSoC 3/5.

Resources

The GlitchFilter uses the following device resources:

- Three UDB macrocells and four UDB product terms.

DC and AC Electrical Characteristics

The following values are indicative of expected performance and based on initial characterization data.

GlitchFilter AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	-	67.01	MHz

Concept Component Changes

This section lists the major changes in the component from the previous version.

Version	Description of Changes
1.0	Initial design.
1.1	Updated for compatibility with PSoC Creator beta5. Updated data sheet format.
1.2	Updated for compatibility with PSoC Creator v1.0.
1.30	Updated for compatibility with PSoC Creator v2.0, to be used as a concept component included in PSoC Creator.
1.40	Simplified the design by removing the unnecessary reset input.

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