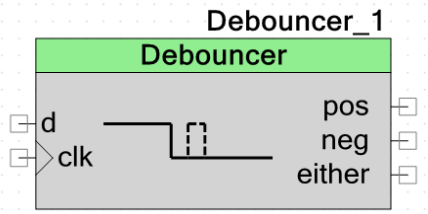
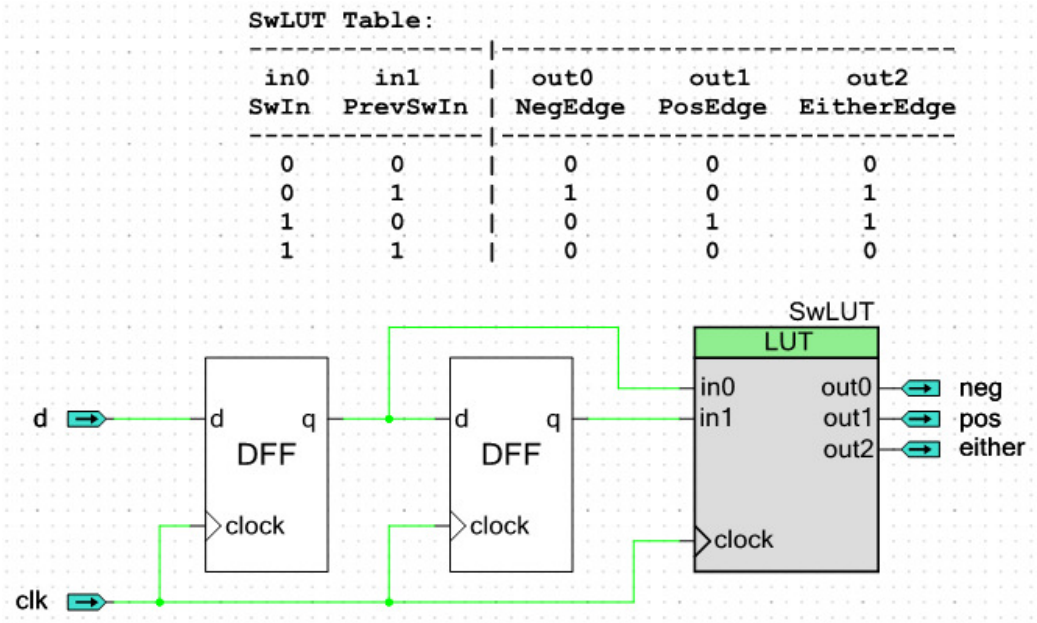
Debouncer
1.40



Features

- Eliminates unwanted “bounce” pulses associated with a switch transition
- Detects and captures positive and negative edges
- Separate resets for edge detection and output

Schematic



General Description

When a mechanical switch or button is pressed or released the output of the switch can oscillate rapidly for a brief period. These oscillations can cause other parts of the system to falsely detect multiple press and release events, possibly leading to erratic and unexpected system behavior. It is possible to filter out these oscillations; the process of doing so is known as switch debouncing.

There are many ways to do switch debouncing, in hardware or software; this component encapsulates a hardware-based design. In the component, the clk input is used to sample the switch input ‘d’. The clock frequency should be much less than the expected bounce frequency, but should also be fast enough that the system appears to be responsive when the switch is opened or closed. 10 to 100 samples per second is usually appropriate.

In the design, the first DFF is used to sample the switch input. The second DFF stores the previous sample, and the LUT does edge detection by comparing the two samples. Note that the delay from an input transition to an edge detect at one or more of the LUT outputs is one period of clk.

For more details on switch debouncing please see application note AN60024.

When to use a Debouncer

A Debouncer concept component can be used with any digital input, however it is usually associated with a mechanical button or switch that is connected to an input pin. Since it does a function that could otherwise be done by firmware, it can be used when a firmware-based debounce solution is not practical.

Input/Output Connections

This section describes the various input and output connections for the Debouncer. An asterisk (*) in the list of I/Os states that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.

d – Input

The switch input that is sampled. It is usually connected to an input Pin component; the pin is usually connected to a mechanical switch or button.

clk – Input

Used to sample the ‘d’ input. Its frequency is typically 10 – 100 Hz.

pos – Output

This output is set to logic ‘1’ whenever the current sample is ‘1’ and the previous sample is ‘0’.

neg – Output

This output is set to logic ‘1’ whenever the current sample is ‘0’ and the previous sample is ‘1’.

either – Output

This output is set to logic ‘1’ whenever the current sample and the previous sample are different.

Parameters

The Debouncer concept component has no configuration parameters.

Placement

The Debouncer concept component is placed in the PLD portion of one or more of the UDBs in PSoC 3 or PSoC 5.

Resources

The Debouncer uses the following device resources:

- Two UDB macrocells and three UDB product terms.

Registers

The Debouncer concept component has no registers.

DC and AC Electrical Characteristics

The following values are indicative of expected performance and based on initial characterization data.

Debouncer AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	-	67.01	MHz

Concept Component Changes

This section lists the major changes in the component from the previous version.

Version	Description of Changes
1.0	Initial design.
1.1	Updated for compatibility with PSoC Creator beta5. Updated data sheet format.
1.2	Updated for compatibility with PSoC Creator v1.0.
1.30	Updated for compatibility with PSoC Creator v2.0, to be used as a concept component included in PSoC Creator.
1.40	Corrected a defect by simplifying the design. The status register and reset input have been removed.

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