PSoC 3 and PSoC 5LP External Crystal Oscillators

Associated Part Family

All PSoC® 3 and PSoC 5LP Parts

Software Version

PSoC Creator™ 3.0

About this document

Scope and purpose

AN54439 describes how to use an external crystal or ceramic resonator at 32.768 kHz or in the 4-25 MHz range with PSoC® 3 or PSoC 5LP. External crystal oscillators provide more accurate clock signals than the oscillators built into the PSoC 3 and 5LP devices. These devices also include a wide range of clock dividers, PLLs, and a clock distribution network that is covered in the **AN60631 PSoC 3 or PSoC 5LP Clocking Resources** application note.

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1 Introduction

AN54439 describes how to configure hardware and firmware for PSoC 3 or PSoC 5LP using the integrated oscillator subsystems and external crystal or ceramic resonators. The PSoC 3 and PSoC 5LP microcontrollers can use a variety of clock sources. Among these, there are two oscillators that can be used with external passive components to generate clock signals with more frequency accuracy than the Internal Main Oscillator (IMO) and Internal Low-speed Oscillator (ILO). The MHz and kHz External Crystal Oscillators (ECOs) can be used with external parallel resonant crystals and ceramic resonators. The MHz ECO can be used to generate clock signals in the 4-25 MHz range, and the kHz ECO can be used to generate a clock signal at 32.768 kHz.

2 PSoC 3 and PSoC 5LP Clocking Overview

PSoC 3 and PSoC 5LP have a number of clocking resources. They are summarized in **Figure 1**. Clock sources are shown at the top of the figure. The muxes and PLLs that use an input clock to create an output clock are shown in the middle of the figure. The resultant clocks that are routed throughout the part are shown at the bottom of the figure.

The two clock sources in PSoC 3 and PSoC 5LP that can be replaced by the ECOs are the 3-62 MHz (3-74 MHz on some PSoC 5LP devices) IMO and the 1/33/100 kHz ILO. These two clock sources operate without external components, with a lower accuracy than achievable by the ECOs (+/-1% error for the IMO and -50%, +100% for the ILO). The ECO clock outputs can be substituted for the IMO and ILO clocks in all of the relevant resources in the part.

Clock routing and substitution is discussed further in the **ECOs and the Clock Tree** section.

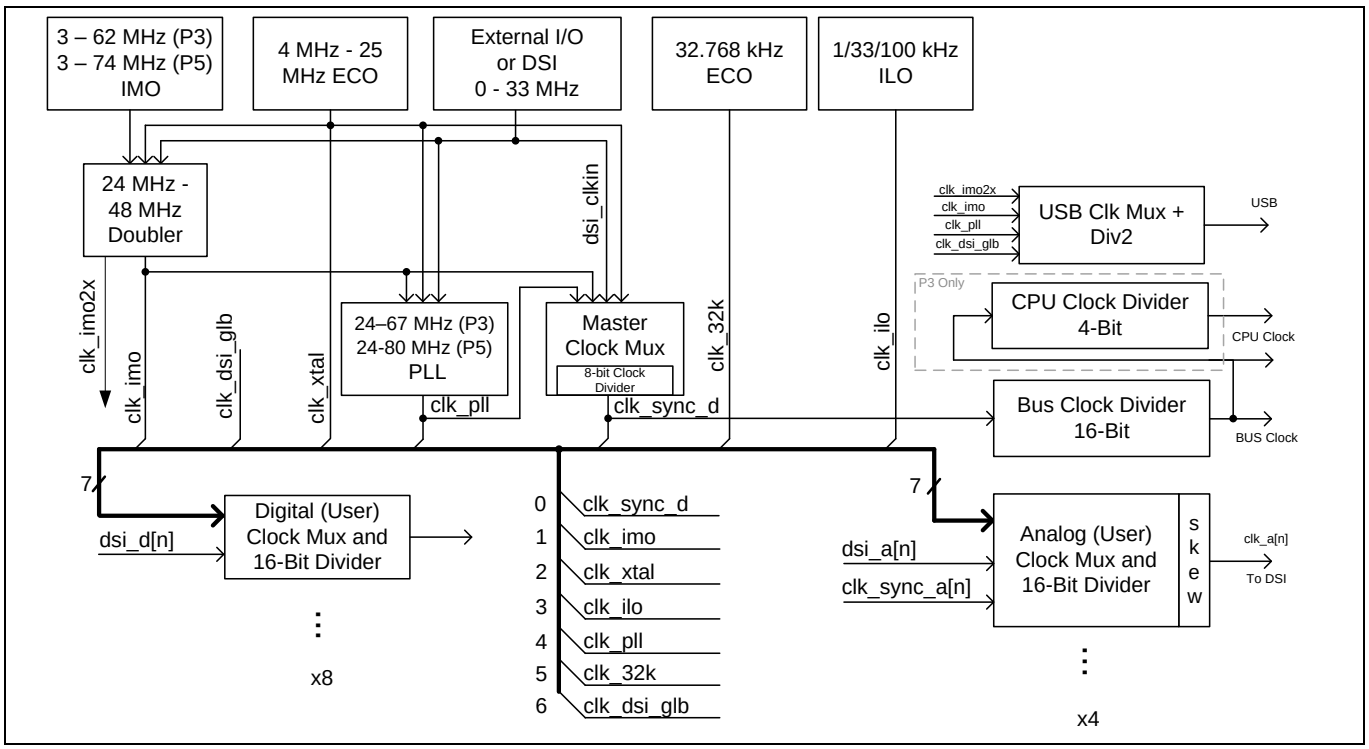

Figure 1 PSoC 3 and PSoC 5LP Clock Overview Diagram

3 External Crystal Oscillator Theory

The kHz and MHz external oscillators in PSoC 3 and PSoC 5LP are Pierce oscillators, meaning an inverting amplifier provides feedback across a crystal in parallel with it. A circuit diagram of a Pierce oscillator is shown in **Figure 2**. The gray region indicates that the inverting amplifier is internal to the PSoC 3 and PSoC 5LP devices, and all other components are external. The crystal input and output (Xi and Xo) pins are also labeled in the diagram. In this scheme, there are three distinct parts. The crystal or resonator (X1) in the pi-network is physically designed to oscillate at the desired frequency. The load capacitors (CL1, CL2) in the pi-network "load" the crystal or resonator to ensure proper operation. The inverting amplifier amplifies the output of the pi-network and drives the input terminal with the inverse signal.

The pi-network made up of a crystal or resonator and capacitors exists to provide 180 degrees of phase shift at the resonant frequency. When combined with the inverting amplifier, 360 degrees of phase shift exist in the circuit, leading to resonant oscillation at the desired frequency.

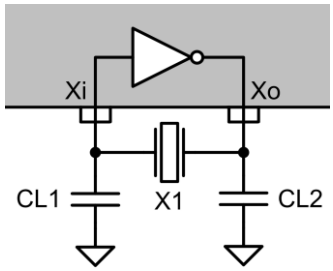

Figure 2 Pierce Oscillator Topology

*Note: Some ECO designs will require additional passive components to decrease drive level or improve startup. For more details, see the **Series and Feedback Resistors** section.*

4 ECO Hardware Implementation

4.1 Overall ECO Hardware Topology

In most microcontrollers with ECO capabilities, the Pierce oscillator's inverting amplifier is internal to the part, and two pins are provided for crystal input and output signals. To implement an ECO with PSoC 3 or PSoC 5LP, a crystal or resonator, and load capacitors must be added to the Printed Circuit Board (PCB).

Depending on resonator selection, the load capacitors may not be required. Ceramic resonators often have built-in load capacitors.

4.2 ECO PCB Layout

ECOs are very sensitive to stray capacitance, board noise, and electromagnetic interference. For these reasons, ECO circuitry requires special attention during PCB layout.

To minimize stray capacitance, the crystal and bypass capacitors are placed as close to the PSoC 3 or PSoC 5LP as possible. Optimally, they are on the same side of the PCB as the PSoC 3 or PSoC 5LP, with no unnecessary vias on the XTALin and XTALout traces. Care should also be taken to ensure that there are no floating islands of conductor neighboring the ECO components, as these can introduce stray capacitance. Trace capacitance to ground must be carefully managed to correctly load the resonator, but the capacitance between crystal traces should also be monitored. For this reason, resonator input and output traces should not be routed over one another on different layers. The series resistance of the traces will be negligible if these guidelines are followed.

Note: *After the circuit board is fabricated, the capacitance of the crystal input and output traces must be measured so that they are accounted for in pi-network capacitor selection. Typical trace capacitances range from 0.1 to 10 pF.*

To ensure that electromagnetic interference does not interfere with ECO operation, the ECO components should be surrounded by a ground fill. If possible, the pins neighboring the XTALin and XTALout pins should be set to high impedance, and tied to ground. If this is not possible, they should be used for slowly changing, low current signals. Fast changing, high current traces and pins such as LED or motor drive signals should be kept away from the ECO circuitry.

Figure 3 demonstrates these guidelines.

Note: *Most resonators are non-polar. Their input and output pin nets may be swapped to ease layout.*

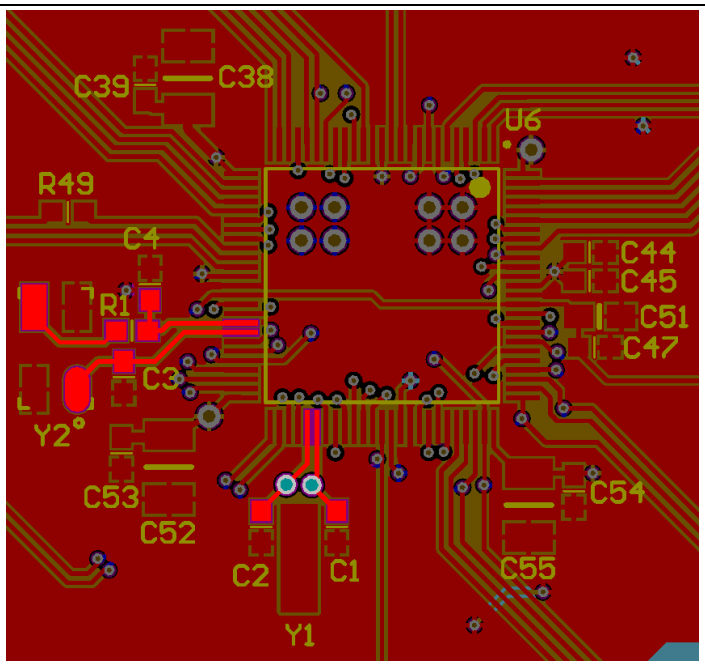

Figure 3 ECO PCB Layout Example

4.3 MHz Resonator

There are two types of resonators that can be used with the MHz ECO: crystal resonators and ceramic resonators. Crystals have tighter initial frequency tolerances and a higher cost. Ceramic resonators are usually found in smaller packages, often with integrated pi-network capacitors.

Crystal resonators offer initial frequency tolerances as low as tens of parts per million (PPM), or thousandths of a percent. Ceramic resonators offer initial frequency tolerances as low as thousands of PPM, or tenths of a percent. PSoC 3 and PSoC 5LP's Internal Main Oscillator (IMO) is rated between 1% and 7% accurate depending on the clock frequency generated. Lower frequency IMO outputs are more accurate.

4.3.1 MHz Resonator Selection

Resonator selection should begin with the choice of desired frequency accuracy. Frequency accuracy requirements are determined based upon the end application. If the frequency accuracy requirement is 1000 PPM or better, a crystal resonator should be selected. If only 50000 PPM or less frequency accuracy is required, a ceramic resonator may be used.

Frequency selection is another important resonator selection factor. The MHz ECO clock may be used as an input to the PSoC 3 and PSoC 5LP phase-locked loop (PLL). This means that the resonator does not need to be the same frequency required for clocking a design with. Lower frequency ECOs have more design tolerance, consume less current, and start up faster. PSoC 3 and PSoC 5LP's MHz ECO can operate with resonators in the range of 4 to 25 MHz.

Other important selection factors include resonator packaging, load capacitance, and drive level. A lower load capacitance makes ECO circuit design easier. Resonators in larger packages typically have lower load capacitances, so larger packages are beneficial. Finally, crystals with a high drive level rating are more likely to be compatible with PSoC 3 and PSoC 5LP's MHz ECOs.

Ceramic resonators are different from crystal resonators in that they have extremely high drive level specifications, and sometimes have integrated load capacitors. When ordering ceramic resonators with

integrated load capacitors, the built-in capacitance values may be specified. Load capacitor selection is described in-depth in the **Pi-network Capacitors** section.

4.4 kHz Crystal

PSoC 3 and PSoC 5LP's kHz ECO circuitry works with 32.768 kHz parallel resonant crystals. This frequency is used because it is 2^{15} Hz, and a 15-bit counter can generate a 1 Hz signal that is useful for Real Time Clocks (RTCs).

Note: The kHz ECO is sometimes described as a "32kHz ECO" to save space, but it operates at 32.768 kHz.

The kHz crystal oscillators typically have initial frequency tolerances of tens of PPM, or thousandths of a percent. In real-time clocks, 11.5 PPM of error will lead to a clock drift of one second per day.

4.4.1 kHz Crystal Selection

PSoC 3 and PSoC 5LP's kHz ECO can operate with parallel resonant 32.768 kHz crystals with a load capacitance of 6 pF or 12.5 pF. Acceptable crystals must meet these guidelines, and also have frequency accuracy and packaging acceptable in the application. Frequency accuracy is specified as initial, across temperature, and across time.

4.5 Pi-network Capacitors

Both crystal and ceramic resonators must be loaded with the proper capacitance in order to oscillate at the correct frequency. The pi-network capacitors should be chosen based on the resonator's load capacitance specification, as well as parasitic capacitances.

Parasitic capacitances include PCB trace capacitance and microcontroller pin capacitance. These parasitic capacitances are shown in **Figure 4** as CP1, CP2 for pin capacitance and CB1, CB2 for PCB trace capacitance. PCB trace capacitance can be measured after manufacturing with an LCR meter, or calculated before manufacturing using the physical properties of the traces and PCB. Pin capacitance can be determined through measurement or by checking the "GPIO DC Specifications" table in the device datasheet. Both traces should have the same capacitance if proper PCB layout practices are followed. Pin and trace capacitances can range from 0.1 to 10 pF.

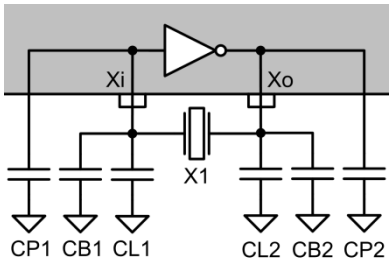

Figure 4 ECO Circuit with Parasitic Capacitances Shown

After pin and trace capacitances are determined, pi-network capacitor values are chosen. The ultimate goal of pi-network capacitor selection is to set the equivalent series combination of input and output capacitances to be the same as the resonator's rated load capacitance. This relationship is expressed in **Equation 1**. In most designs, the load capacitance is "balanced", and both load capacitors are of equal value. In some designs it is advantageous to use "unbalanced" capacitors. For more details on this arrangement, see the **Unbalanced ECO Load Capacitors** section.

ECO Hardware Implementation

In the equations shown here, CL represents rated crystal load capacitance, CP1 and CP2 represent microcontroller input pin capacitances, CB1 and CB2 represent PCB trace capacitances and crystal package capacitance, and CL1 and CL2 represent discrete capacitor values. In most cases, these parasitic capacitances are symmetrical, so CP1=CP2 and CB1=CB2.

Ideal Load Capacitance Criterion

$$CL = \frac{1}{\frac{1}{CL1+CB1+CP1} + \frac{1}{CL2+CB2+CP2}}$$ **Equation 1**

If pin and trace capacitances are assumed to be equal, balanced load capacitor values may be determined using **Equation 2**.

Balanced Pi-network Capacitance Criterion

$$CL1 = CL2 = 2 * CL - (CP + CB)$$ **Equation 2**

Capacitor initial and temperature variation should also be considered when selecting parts. Variations in load capacitor values will cause frequency error. This is described in detail in the **Load Capacitance Trim Sensitivity** section.

4.5.1 Balanced Load Capacitor Example

To determine appropriate load capacitor values for a 12.5-pF kHz crystal, we apply **Equation 2**. If we assume PSoC 3 and PSoC 5LP pin input capacitance(CP) of 5 pF and a board trace capacitance (CB) of 1 pF, then the result is 2*12.5-(5+1) = 19 pF, or a standard 18-pF value. Thus, we would place one 18-pF load capacitor on each side of the crystal.

5 ECO Firmware Implementation

After hardware design is complete, the next step is PSoC 3 or PSoC 5LP firmware. PSoC Creator automatically generates firmware to set up the ECOs based on the project's configuration. The PSoC Creator project is configured using the Design Wide Resources interface.

5.1 ECOs and the Clock Tree

The kHz and MHz ECOs can be used in various ways throughout PSoC 3 and PSoC 5LP. The kHz and MHz ECOs are highlighted in the clock tree diagram shown in **Figure 5**. Both clocks are routed to the clock bus, allowing them to be used as the clock sources for components throughout the digital and analog resources.

The MHz ECO is the more versatile of the two clock signals, as it is routed to the IMO doubler, PLL, and the Master Clock Mux. The IMO doubler should only be used for the USB clock and should not be used to double the MHz ECO clock, because it introduces significant jitter. The PLL may be used to multiply and divide the MHz ECO clock to create a 24 to 67 MHz signal and up to 80 MHz for some PSoC 5LP parts. The MHz ECO may also be used as the master clock.

The kHz ECO has more limited uses. It is routed to the clock bus, but not the IMO doubler, PLL, or Master Clock Mux. Both the IMO doubler and PLL have minimum frequency limitations that invalidate their use with the 32-kHz ECO. See **AN60631** for more information on the clock tree.

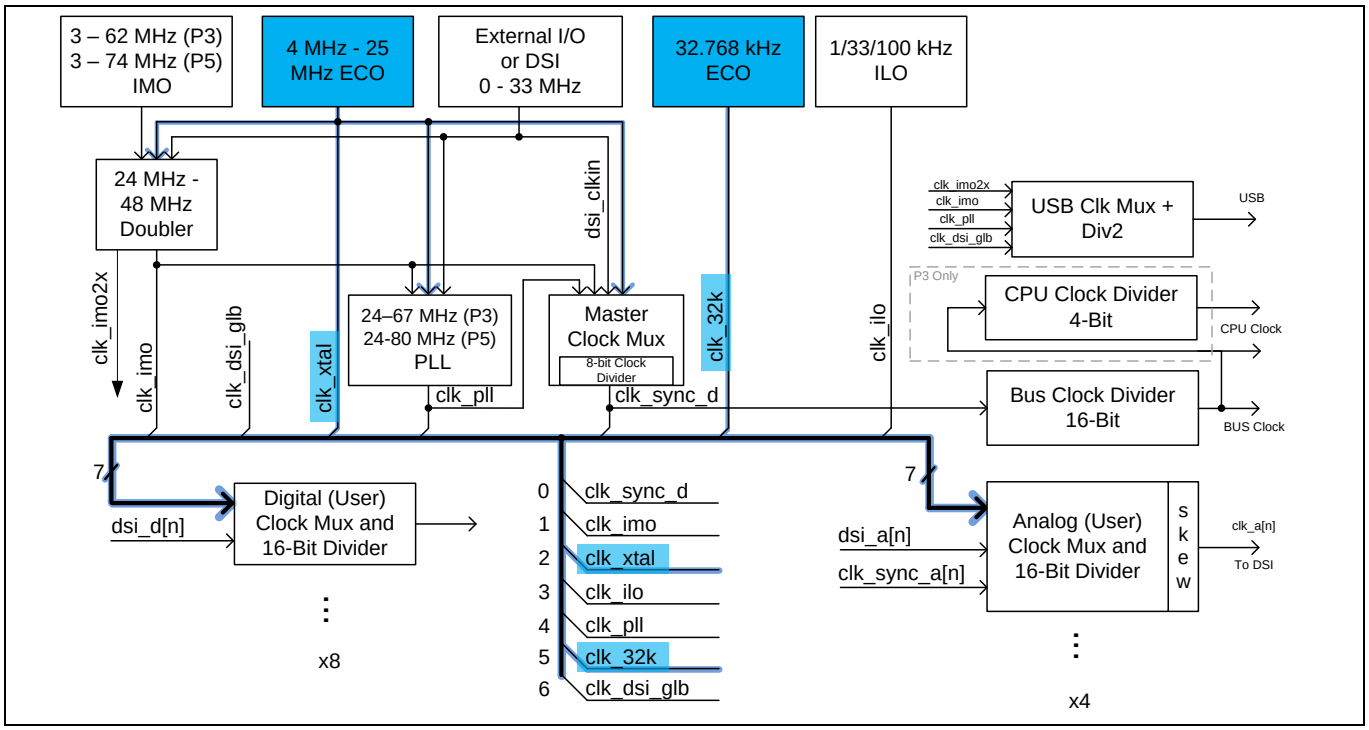

Figure 5 PSoC 3 and PSoC 5LP Clocking Tree with ECOs Highlighted

5.2 Design Wide Resources Settings

The Design Wide Resources interface is used to configure the ECOs in a PSoC Creator project. Within the design wide resources, clocks are configured in the “Clocks” tab. The clock tree may be configured using the “configure system clocks” dialog, which is accessed by double-clicking on any of the system clocks.

*Note: More information on clock tree configuration may be found in **AN60631**.*

Figure 6 shows an example Configure System Clocks dialog, using an 8-MHz crystal and a 32.768-kHz crystal as clock sources. In this system, an 8-MHz ECO is used as the source for both the IMO and the PLL, and the PLL is used as the source for the Master Clock.

Figure 7 shows the more advanced MHz ECO Configuration dialog. The MHz ECO Configuration dialog can be used to configure a number of MHz ECO options, including setting the frequency, configuring amplitude detection and control, and other parameters. These options are discussed in detail in the following sections.

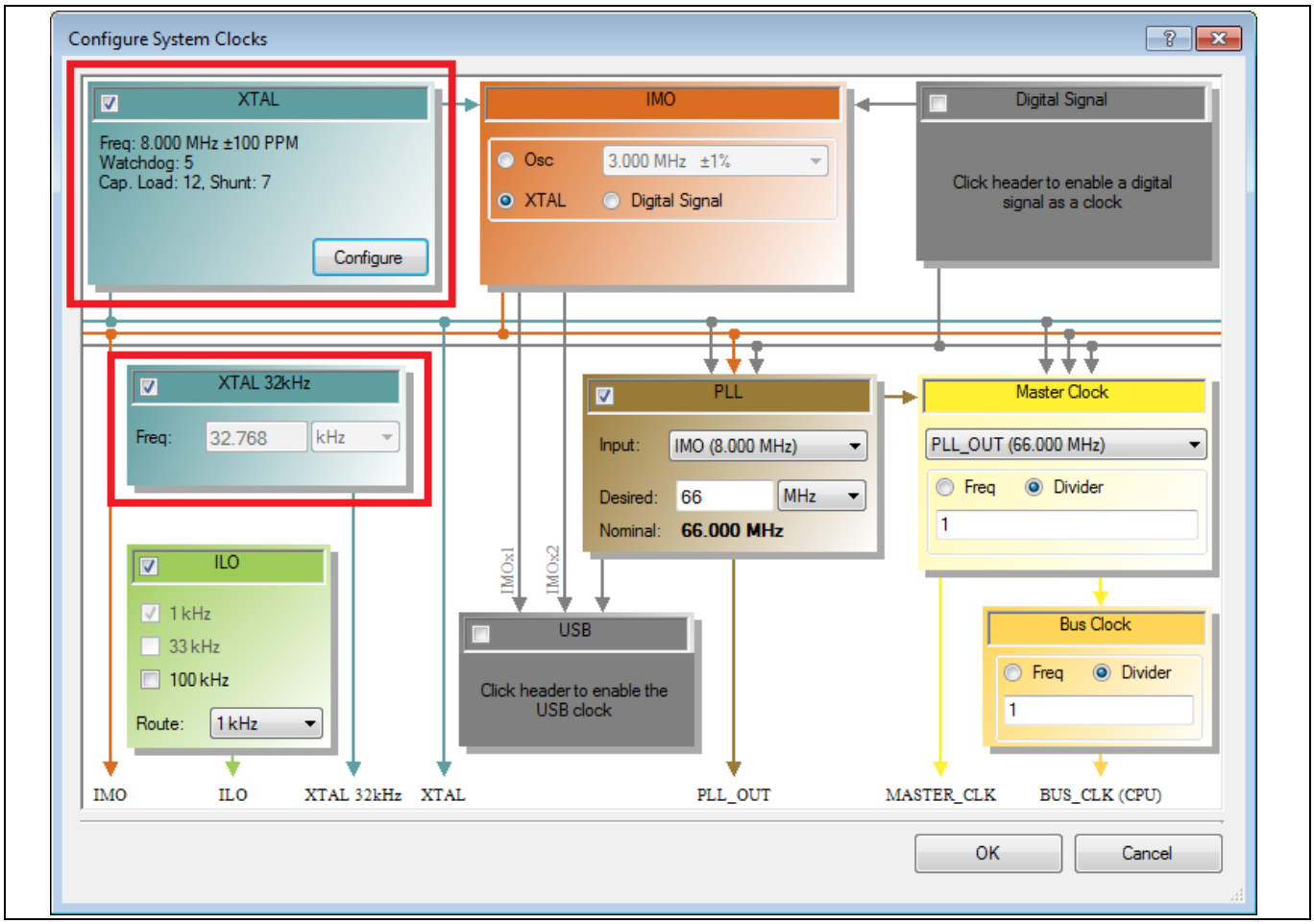

Figure 6 Example PSoC Creator Configure System Clocks Dialog with ECOs Highlighted

To configure the clock tree for a specific ECO configuration, a number of settings must be configured. Both XTAL sources, kHz and MHz, may be enabled using their checkboxes. The MHz ECO configuration dialog has a number of configuration options, as shown in **Figure 7**. These options are explained in detail in the following sections.

ECO Firmware Implementation

Once the MHz ECO is configured, the IMO, PLL, and Master Clock may be configured to use the MHz crystal as their clock source. Local clocks may also be derived from the oscillators or other sources in the Clocks tab of the design wide resources.

Note: *The kHz crystal clock frequency is not configurable, because PSoC 3 and PSoC 5LP support only 32.768-kHz crystals.*

Some design decisions must be made when choosing how to use the ECO clocks. Both MHz and kHz ECO clocks may be used as sources for digital and analog clocks, so no special configuration is required to create an externally based local clock. However, there are clocks in the tree that can only be derived from certain other clocks. The IMO may be sourced from the MHz XTAL clock. This can be useful if the IMO doubler is used to generate a clock at twice the frequency of the ECO. The PLL may be sourced from the MHz XTAL, allowing division and multiplication of the MHz XTAL frequency, and the creation of a desired MHz range clock. The Master Clock may be derived from the MHz XTAL, or MHz XTAL sourced PLL, which allows clocking the 8051 and Cortex M3 cores with a MHz XTAL derived bus clock.

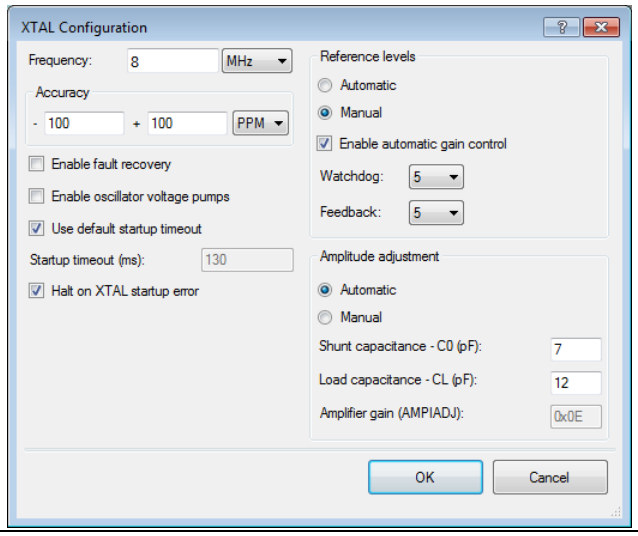

Figure 7 Example PSoC Creator MHz ECO Configuration Dialog

5.2.1 MHz ECO Automatic Gain Control

The Automatic Gain Control (AGC), allows the MHz ECO to increase or reduce the inverting amplifier gain to increase or decrease oscillation amplitude. This can increase or decrease the drive level.

The AGC monitors the amplitude of the crystal input waveform and compares it to a reference value. If the amplitude is higher or lower than desired, the inverting amplifier gain is modified in hardware. The reference value is generated based on the vref_sel_fb bits of the FASTCLK_XMHZ_CFG1 register. A lookup for these bits is available in the PSoC 3 and PSoC 5LP Registers Technical Reference Manual (book 2).

The AGC may be enabled or disabled in PSoC Creator using the MHz ECO Configuration dialog, shown in **Figure 7**. The “Enable automatic gain control” checkbox controls this feature. The AGC feedback register value may be selected using the “Feedback” dropdown, which only appears when the AGC is enabled. The AGC should be left disabled in most designs. It should only be enabled if the ECO circuit is not meeting drive level requirements, as described in the **Drive Level** section. Lower “feedback” values will correspond to lower drive level results. The feedback value can be automatically set by PSoC Creator based on the ECO’s operating frequency, if the “Automatic” radio button is selected.

5.2.2 MHz ECO Error Detection “Watchdog”

The error detection, or “watchdog” circuitry allows the ECOs to detect when each resonator is oscillating properly. This result is used to determine when the ECO has completed startup and can be used to clock the system. It may also be used to change configurations if the ECO stops working properly. The current value of the MHz ECO error bit is stored in the xerr bit of the FASTCLK_XMHZ_CSR register. The kHz ECO error bit is stored in the ana_stat bit of the SLOWCLK_X32_CR register.

The kHz and MHz ECO error status bits may also be polled using the `CyXTAL_32KHZ_ReadStatus()` and `CyXTAL_ReadStatus()` APIs described in the System Reference Guide.

The MHz ECO error detection circuitry works similarly to the AGC, monitoring the amplitude of the crystal input waveform and comparing it to a reference value. If the amplitude is lower than desired, the ECO error bit is asserted. The reference value is generated based on the vref_sel_wd bits of the FASTCLK_XMHZ_CFG1 register. This value may be configured in PSoC Creator using the Design Wide Resources interface, in the MHz ECO Configuration dialog, shown in **Figure 7**. The ECO error detection threshold is set using the “Watchdog” dropdown. This value should only be changed if the ECO is found to have greater than expected noise susceptibility, or if crystal failures are not being detected. It can be automatically set by PSoC Creator based on the ECO’s operating frequency, if the “Automatic” radio button is selected, by default.

The kHz ECO error detection does not require configuration, unlike the MHz ECO.

The fault recovery setting allows the designer to choose what behavior to carry out when the ECO fails to oscillate. If fault recovery is enabled, then the device automatically enables and switches to the IMO clock in case of ECO failure. Fault recovery may be enabled using the “Enable fault recovery” checkbox in the MHz ECO Configuration dialog, shown in **Figure 7**.

The “Halt on XTAL startup error” checkbox controls the behavior of the PSoC firmware during MHz ECO startup. If this box is checked, the firmware will automatically halt device startup if the MHz ECO does not stabilize within the specified startup timeout. The device will instead go into a special error function, whose contents can be edited. This function is called “`CyClockStartupError()`”, and is located in the *cyfitter_cfg.c* source file.

5.2.3 Amplitude Adjustment

Amplitude adjustment allows modification of the gain of the inverting amplifier in the Pierce oscillator circuit shown in **Figure 2**. Modifying the gain of the inverting amplifier has multiple effects on the performance of the MHz ECO, including the metrics of negative resistance, drive level, and startup time that are explained in the **ECO Performance Testing and Improvement** section.

Amplitude adjustment configuration can be performed manually or automatically in PSoC Creator, as shown in **Figure 7**. The automatic selection will choose an inverting amplifier gain based on the frequency, shunt capacitance, and load capacitances entered in the tool. Manual selection allows the user to choose their own amplifier gain value (AMPIADJ). It is recommended that this setting be left automatic for most applications. Details on setting the gain can be found in the Register section of the Technical Reference Manual (summarized in **Table 1**). Although the gain setting is referred to as “AMPIADJ” in PSoC Creator, it is referred to as “xcfg” in the Technical Reference Manual.

ECO Firmware Implementation

Table 1 Manual AMPIADJ Settings

	FASTCLK_XMHZ_CF0 (xcfg)
Load Capacitance $C_L \geq 15$ pF Shunt Capacitance $C_O < 3.5$ pF	Freq ≤ 6.9 MHz (xcfg= 0x13) Freq > 6.9 MHz (xcfg= 0x17)
Load Capacitance $C_L \geq 15$ pF Shunt Capacitance $C_O \geq 3.5$ pF	Freq ≤ 7.3 MHz (xcfg= 0x0E) 7.3 MHz < Freq ≤ 13.2 MHz (xcfg= x13) Freq > 13.2 MHz (xcfg= 0x19)
Load Capacitance $C_L < 15$ pF	Freq ≤ 7.3 MHz (xcfg= 0x0A) 7.3 MHz < Freq ≤ 12.9 MHz (xcf= 0x0E) Freq > 12.9 MHz (xcfg= 0x13)

5.3 Real-Time Clock

The kHz ECO can be used to source a real-time clock for applications that must accurately keep track of time. PSoC Creator provides the RTC component, which allows the designer to quickly implement a real-time clock in PSoC 3 and PSoC 5LP using a kHz ECO. For more information about how to implement a Real-Time Clock, refer to the “RTC” Component datasheet in PSoC Creator under the Component Catalog.

6 ECO Performance Testing and Improvement

When designing microcontroller based systems, reliability is a critical concern. The best way to improve reliability is to test systems over a range of critical variables, slightly exceeding required performance specifications. There are design modifications that can be made to improve this performance based upon feedback.

6.1 ECO Performance Metrics

There are four key measurements that give information about MHz and kHz ECO performance. They are described in the following sections.

6.1.1 Negative Resistance

Negative resistance is a measurement of the amount of series resistance that can be added to the effective series resistance of the resonator without stopping the ECO from starting up properly. It is a measurement of reliability of the ECO, higher being better. Negative resistance is also known as “-R” or “oscillation allowance”.

The final metric of reliability relating to negative resistance is usually a ratio of negative resistance to the effective series resistance of the resonator used. This ratio of -R/ESR is then compared to some arbitrary value, usually 3 or 5, to determine if it is high enough.

Negative resistance should be measured by inserting a resistor in series with the resonator, and observing the ECO clock output. The circuit arrangement is shown in **Figure 8**. A fixed value resistor should be used, as potentiometers have non-ideal characteristics that can lead to an incorrectly low measurement. The series resistance should be increased and the part reset until a resistance is found with which the ECO no longer starts up. The highest value that allows startup should be added to the ESR specification of the resonator, and this should be considered the negative resistance of the ECO. This relationship is shown in **Equation 3**.

Negative Resistance Formula

$$-R = R1_{MAX} + ESR \qquad \textbf{Equation 3}$$

Negative resistance is lowest at high temperature and low VCCA and VCCD, so this corner should be tested.

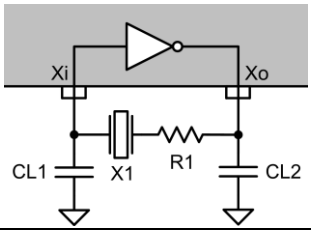

Figure 8 ECO Circuit for Negative Resistance Tests

Negative resistance may also be measured using a network analyzer. This method usually gives higher -R values. For more details, see the technical article **Crystal Oscillator Design and Negative Resistance**.

6.1.2 Drive Level

Drive level is a measurement of the power applied to the resonator by the inverting amplifier in the ECO circuit. It is a measurement of how much power is being dissipated by the resonator, and implies whether the resonator will be damaged during operation. Crystal vendors specify a maximum drive level that may be

ECO Performance Testing and Improvement

applied to their resonator without negatively affecting performance. Ceramic resonators usually do not have a drive level specification, as their construction is more tolerant of high energy dissipation.

Crystals have rated drive levels that typically range from 0.1 µW to 1.0 mW. Drive level may be calculated using **Equation 4**. In this equation, DL represents the drive level, I_{RMS} represents the RMS current flowing through the resonator, and ESR represents the resonator's effective series resistance.

Resonator Drive Level Calculation

$$DL = I_{RMS}^{2} * ESR \qquad \textbf{Equation 4}$$

Drive level may be measured by using a current probe measuring the current entering or exiting the resonator. This may require modification of a circuit for testing, for example by adding a small wire that can be passed through the current probe. The ECO should be tested in the intended final configuration, without any resistance used for testing –R. The current measurement should be taken after ECO startup has completed and the automatic gain control has had time to stabilize at the steady state drive level of the circuit. This takes less than 100 ms in most designs. The RMS current measurement may be used in conjunction with **Equation 3** to calculate drive level.

Drive level relatively constant across operating temperatures and voltages, so no specific corner needs to be tested. Drive level does vary with load capacitance.

Drive level may also be measured by using the differential voltage across a series resistance to determine series current. This would be implemented using the same circuit as used for negative resistance tests, as shown in **Figure 8**. The series resistor should be as low as possible to avoid altering the behavior of the ECO circuit. This method may be employed if a current probe with an appropriate frequency response is not available.

If the measured drive level is higher than the rated drive level, there are three methods to reduce it. The automatic gain control may be used to reduce drive level. For more details, see the **MHz ECO Automatic Gain Control** section. The inverting amplifier gain may also be manually reduced to reduce drive level. A series resistance may also be used to reduce the drive level. For more details, see the **Series and Feedback Resistors** section.

As crystals rapidly shrink to fit into smaller devices, it is important to know the power dissipation of the crystal to avoid damaging them. The following equation is used to calculate the power dissipation of the crystal. This equation assumes that the load capacitors CL1 and CL2 are the same value "C". V_{PP} is the peak to peak voltage across the crystal.

Crystal Power Dissipation

$$P_{xtal} = 2R(\pi f C V_{pp})^2 \qquad \textbf{Equation 5}$$

6.1.3 Startup Time

Startup time is a measurement of the time it takes for the ECO to stabilize at the desired frequency after it is enabled. This value will vary with both hardware and firmware configuration. Maximum values for these specs are shown in the PSoC 3 and 5LP device datasheets. Example startup times for MHz resonators with PSoC 3 are shown in **Figure 9**. It is worth noting that lower frequency crystals tend to start up faster, and ceramic resonators tend to startup faster than crystals.

Startup time may be measured by adding firmware pin toggles to the clock startup function "`ClockSetup()`" in the *cyfitter_cfg.c* source file that is automatically generated by PSoC Creator. Within that function, a pin

toggle should be added before the register CYREG_FASTCLK_XMHZ_CSR is set, and another should be added after the following `for()` loop, which should be just a few lines of code below it.

Startup time is longest at high temperature, low VCCA and VCCD, and high load capacitance, so this corner should be tested. Startup time is slightly higher with the automatic gain control on.

6.1.4 Frequency Accuracy

Frequency accuracy is a measurement of how closely the ECO's clock matches the desired frequency. The initial tolerance specification of the resonator will have the largest impact on frequency accuracy, but other factors will also have an impact. These factors include trim sensitivity, aging, and temperature variation. These topics are discussed in the **ECO Frequency Accuracy** section.

To measure ECO frequency accuracy, simply route the ECO clock output to a GPIO, and observe it with a frequency counter. Frequency accuracy should be measured across temperature and component variation.

Note: *When routing clock signals to GPIOs for frequency measurement, the designer should consider the pins' rated operational frequencies. It is often easier to measure a clock that has been divided by 10 internally.*

6.2 ECO Test conditions

The physical operating conditions of the whole ECO circuit have an effect on its performance. There are two key variables that drastically affect ECO performance. They are humidity variation and temperature variation.

Humidity variation implies increased conductivity across the surface of the PCB, introducing megaohms or even high kilohms of resistance in parallel with components. In the case of ECOs, this parallel resistance has negative effects upon performance. In situations where performance across humidity is a large concern, the designer should consider a conformal coating or potting to protect the PCB and components from humidity, and use a forced humidity chamber to test performance.

Temperature variation causes changes in performance in many components in the system. Most notably, temperature variation causes a drift in the resonant frequency of crystal and ceramic resonators. This drift is always specified by the manufacturer, and should be considered when selecting parts. For more details, see the **Frequency Temperature Variation** section.

Temperature drift also causes variations in the capacitance of the discrete pi-network capacitors. Variation in this capacitance causes "pulling" of the resonator's natural frequency. For more details, see the **Load Capacitance Trim Sensitivity** section.

Note: *Initial component value variation should also be considered when testing for reliability.*

Startup condition also has an effect on ECO operation. Variations in the amount of time a part is off before being turned back on increases the amount of time that is required for the ECO to stabilize. The type of part reset, whether a voltage rail toggle or XRES pulse also cause variations. Variations in operating conditions, such as low power operating mode, have similar effects. Behavior under these circumstances should also be examined when testing for reliability.

Supply voltage, both input (VDDA and VDDD) and regulated (VCCA and VCCD) can have an effect on ECO performance. The worst case voltage corners for various performance metrics have been described in the previous sections of this application note.

7 Recommended PSoC 3 MHz ECO Configurations

Figure 9 shows a small selection of resonators that have been tested with PSoC 3. Their most important specifications are shown, and a recommended configuration is given. **Figure 9** also shows typical performance values, tested as described in the **ECO Performance Metrics** section for the performance parameters described in **Figure 9**. Resonators were tested across operating temperature and supply voltage.

The two 24 MHz ECS crystals shown are the same parts used on the PSoC 3 and PSoC 5LP DVKs. The KIT-030 and KIT-050 have the ECS-240-20-5PX-TR, and the KIT-009A and KIT-010 have the ECS-240-12-5PX-TR.

Note: *These resonators were tested with a single unit of PSoC 3 silicon, so these results should be considered "typical", and should be re-measured in each design. PSoC 5LP performance may differ slightly.*

Resonator Specifications						Recommended Configuration				Typical Performance		
Manufacturer	Part Number	Resonator Type	Frequency (MHz)	Initial Tolerance	Drive Level Maximum (µW)	Discrete load capacitors CL1 = CL2 =	AGC enabled?	Amplifier Gain (AMPlADJ)	Feedback Value	Max Expected Drive Level (µW)	Minimum -R/ESR Ratio	Maximum Startup Time (µs)
ECS	ECS-245.7-18-5PXEN-TR	Crystal	24.576	30 PPM	500	28 pF	Yes	0x19	3	95	11	340
ECS	ECS-240-12-5PX-TR	Crystal	24	30 PPM	500	16 pF	Yes	0x17	3	425	11	300
ECS	ECS-240-20-5PX-TR	Crystal	24	30 PPM	500	32 pF	Yes	0x19	3	105	11	310
ECS	ECS-80-20-5PVX	Crystal	8	30 PPM	500	32 pF	No	0x13	5	180	12	700
ECS	ECS-40-20-5PX-TR	Crystal	4	30 PPM	500	32 pF	No	0x0E	5	105	14	2250
Murata	CSTCW24M0X53-R0	Ceramic	24	0.50%	N/A	N/A	No	0x19	3	1700	5.5	200
Murata	CSTLS8M00G53-A0	Ceramic	8	0.50%	N/A	N/A	No	0x13	5	20	60	73
Murata	CSTCR4M00G53-R0	Ceramic	4	0.50%	N/A	N/A	No	0x0E	5	40	160	75

Figure 9 PSoC 3 MHz Resonator Recommendations and Typical Performance

7.1 Resonator Equivalent Circuit

Crystal and ceramic resonators can be modeled as a combination of basic passive components. The equivalent model is shown in **Figure 10**. The series combination of R1, C1, and L1 is known as the "motional arm". R1 is known as the "motional resistance" or "effective series resistance" (ESR). C1 is known as the "motional capacitance". L1 is known as the "motional inductance". C0 is known as the "shunt capacitance". Some or all of these characteristics may be specified by the crystal manufacturer.

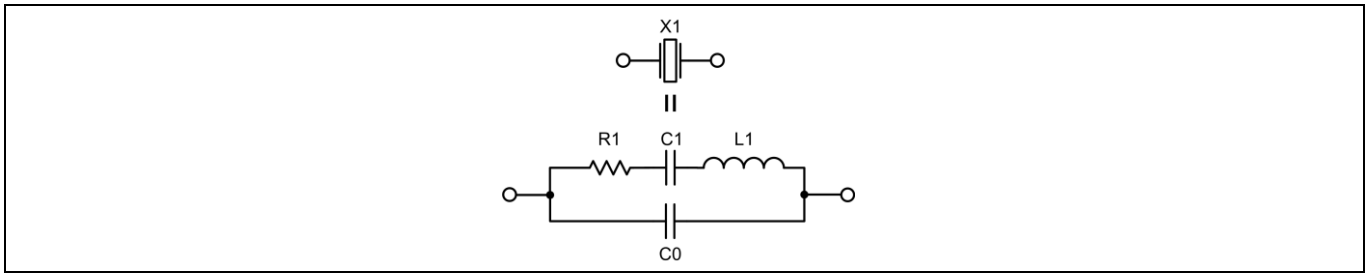

Figure 10 Resonator Equivalent Circuit

7.2 ECO Frequency Accuracy

The frequency of the clock generated by the ECO will always deviate from the desired frequency by some amount. It is important to understand how much it will deviate, and how to improve it. This section describes the various factors that impact frequency performance.

Frequency accuracy is a measurement of the maximum expected deviation from expected frequency. This maximum will be a sum of the individual causes of frequency inaccuracy. Each of the individual causes is listed below. In designs, all of these factors should be calculated and summed to determine overall system maximum frequency deviation, and thus frequency accuracy.

7.2.1 Initial Frequency Tolerance

Initial frequency tolerance, sometimes called simply “frequency tolerance”, describes the maximum expected deviation in resonant frequency of a resonator at room temperature when the proper load capacitance is in place. This contributor of frequency error is the “base” to which all other contributors should be added. It is usually the largest contributor of frequency error.

7.2.2 Frequency Temperature Variation

Frequency temperature variation, sometimes called “frequency stability” or “temperature stability”, describes the increase in maximum expected deviation of resonant frequency of a resonator across its operating temperature range.

7.2.3 Resonator Aging

Resonator aging describes an increase in frequency deviation that occurs over the operating life of the resonator. This spec is usually given in units of PPM/year. The resonator frequency deviation at a given age can be easily calculated by multiplying the aging value times age in years.

The term “aging” is also sometimes used to describe the damage that can occur to a crystal if its drive level specification is exceeded. This type of aging is usually not specified by crystal vendors, as it implies that the ECO circuit is not operating within specifications.

7.2.4 Load Capacitance Trim Sensitivity

Variation of actual load capacitance tends to “pull” the resonant frequency of the resonator. This effect is known as “trim sensitivity”, or sometimes “pullability”. This effect can be both good and bad. On the good side, the designer may tune the resonant frequency of an oscillator by slightly modifying capacitor values. However, on the bad side, capacitance variation across parts and across temperature can cause the generated frequency to differ from the desired value.

Trim sensitivity is measured in PPM of added clock error per pF of variation in total actual load capacitance. It can be determined using resonator parameters described in the **Resonator Equivalent Circuit** section. Trim sensitivity is a function of the resonator’s rated load capacitance (CL), shunt capacitance (C0), and motional capacitance (C1). The relationship is shown in **Equation 6**.

ECO Trim Sensitivity

$$Trim\ Sensitivity = S = \frac{C1 * 1{,}000{,}000}{2*(C0+CL)^2}\frac{(PPM)}{(pF)} \qquad \textbf{Equation 6}$$

Recommended PSoC 3 MHz ECO Configurations

Note: *This formula is a linearization of a second order function. For more details, inquire with crystal vendors.*

Here is an example of calculation of trim sensitivity for an Abracon AB38T-32.768KHZ crystal. This 32.768 kHz crystal has a typical C1 of 0.0035 pF, typical C0 of 1.6 pF, and rated CL of 12.5 pF. Thus, the trim sensitivity is determined as shown in **Equation 7**. This calculation shows that for 1 pF in error in the actual applied load capacitance, the frequency will err by 8.8 PPM, or 0.29 Hz.

Note: *1 pF in discrete capacitor error will cause less than 1 pF of total load capacitance error, because of the relationship shown in **Equation 1**.*

Trim Sensitivity Calculation Example

$$S = \frac{C1 * 1{,}000{,}000}{2*(C0+CL)^2} = \frac{0.0035 * 1{,}000{,}000}{2*(1.6+12.5)^2} = 8.8\frac{PPM}{pF}$$ **Equation 7**

Trim sensitivity implies requirements for load capacitor values and temperature coefficients. It should be considered along with resonator frequency accuracy and system performance requirements to determine what load capacitors to use.

7.3 Series and Feedback Resistors

The resistors Rs and Rf shown in **Figure 11** can be used to improve MHz oscillator behavior under certain circumstances. The series resistor Rs reduces the power dissipated by the resonator to meet drive level specifications. The feedback resistor Rf allows noise feedback across the resonator at startup, decreasing startup time.

Drive level, described in the **Drive Level** section, describes the amount of power dissipated by the resonator. If the actual drive level of the ECO circuit is above the resonator's specifications, it can cause the resonator to age, reducing frequency accuracy. To reduce drive level, a series resistor Rs may be added. The series resistance will create a power divider with the ESR of the crystal. Typical Rs values are near ESR specifications of resonators they are used with, in tens or hundreds of ohms.

Ceramic resonators, unlike crystal resonators, do not typically have drive-level specifications. Thus, series resistors are not needed in their ECO circuits.

ECO circuits start up by amplifying ambient thermal noise and electromagnetic interference. The pi-network acts as a filter for this noise, resonating at the proper frequency, with the inverting amplifier increasing the amplitude of the signal. Initial startup can be hampered in low noise environments, requiring the addition of a feedback resistor Rf. If added, this feedback resistor should be on the order of 5-15 MΩ.

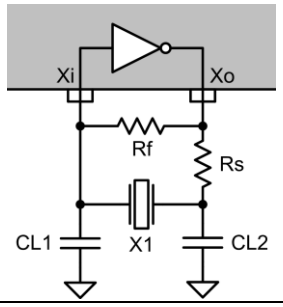

Figure 11 Pierce Oscillator Topology with Series and Feedback Resistors

7.4 Unbalanced ECO Load Capacitors

There are two load capacitor configuration options: balanced and unbalanced. In a balanced configuration, both capacitor values are equal. In an unbalanced configuration, one capacitor is larger than the other capacitor. The imbalance can be in either direction. If the output capacitor is larger than the input capacitor, the oscillator will be more stable, but consume more current. If the input capacitor is larger than the output capacitor, the oscillator will consume less current but be less stable.

Regardless of whether the configuration is balanced or unbalanced, the combination of capacitances should still load the resonator according to its specifications. In the unbalanced configuration, the ratio of capacitances should be about three to one. This criterion should be used in conjunction with the basic criterion expressed in **Equation 1** to determine the capacitor values.

A typical pair of unbalanced values for a 12.5 pF, 32.768 kHz crystal are Cin = CL1 = 15 pF and Cout = CL2 = 47 pF.

7.5 Reducing Clock Power Consumption with ECOs

Use of an ECO eliminates the need for internal clock sources. Disabling these clock sources offers power savings. The IMO may be disabled using the `CyIMO_Stop()` API. Disabling the IMO saves hundreds or thousands of µA depending on the IMO's configuration.

The power consumption of the ECOs themselves can also be optimized. Decreasing the drive level of the MHz ECO using the AGC reduces its current consumption. See the **MHz ECO Automatic Gain Control** section for more details.

The kHz ECO has multiple power modes that may be selected using the SLOWCLK_X32_CR register, or using the `CyXTAL_32KHZ_SetPowerMode()` API provided by PSoC Creator. See the Clocking section of the System Reference Guide for more details on these APIs.

Note: *ECO power consumption can be further reduced using unbalanced pi-network capacitors. See the **Unbalanced ECO Load Capacitors** section for details.*

7.6 ECO Startup Behavior

An example 32 kHz ECO startup output waveform is shown in **Figure 12**. Initially, when the part is held in reset, the crystal output is pulled low. During startup, the pin is pulled to logic high, and then when crystal startup commences, the output goes to the bias voltage. Crystal startup can range in length depending upon system configuration. Over the course of crystal startup, the amplitude of oscillations increases until it reaches its steady state amplitude.

The MHz ECO configuration firmware can cause startup code execution to halt depending on the project settings. See the **MHz ECO Error Detection "Watchdog"** section for more details.

Note: *When observing oscillator input or output waveforms, a high impedance probe or a buffer such as an op-amp follower should be used. Otherwise, the probe will load the oscillator, and change ECO behavior or cause it to stop oscillating.*

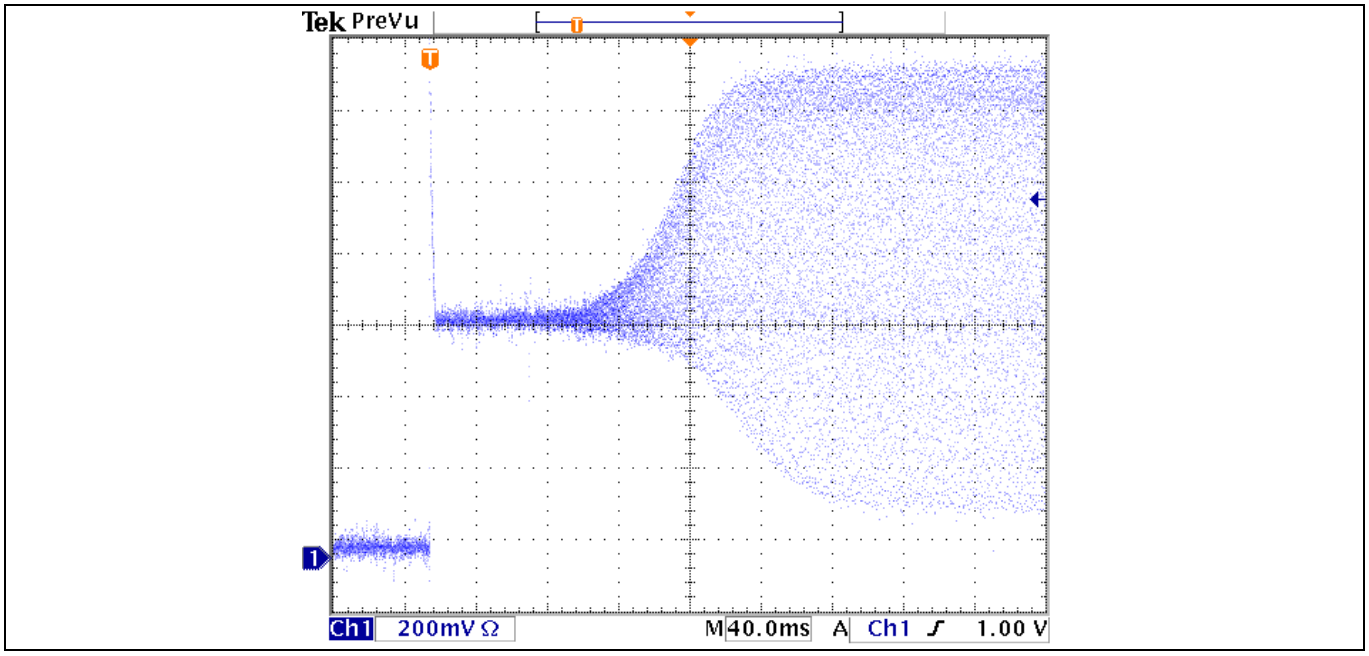

Figure 12 32-kHz ECO Startup Behavior

7.7 Using an External Clock Signal on the ECO Pins

If the MHz or kHz ECO is not being used, an external clock signal may be routed onto the ECO clock nets using the kHz or MHz crystal input pins. This allows the use of these clock nets in place of the usual DSI clock net in the clock tree.

External clocks can be routed into the part through the kHz and MHz XtalIn pins. The XtalOut pins should be allowed to float. Ideally, the external signals should be rail-to-rail sine or square waves. If the amplitude of the signals is too low, they may not be properly translated into digital signals. These signals must be within the frequency ratings of the ECOs, either at 32.768 kHz or 4-25 MHz. No additional firmware is required. Just set up the oscillator, as if using a crystal, in the Clocks section of the Design Wide Resources in PSoC Creator.

External clocks can also be routed into the part using the GPIOs. For more details, see **AN60631** - PSoC® 3 and PSoC 5LP Clocking Resources.

7.8 Using Clock Resources in PSoC Creator

This application note has discussed how to configure external oscillators, but once that is done, the use of the clocks generated by these oscillators is abstracted to a simple Clock Component in PSoC Creator. The user may place one or more Clock Components onto the schematic and connect it to various components or logic. **Figure 13** shows a clock connected to a PWM.

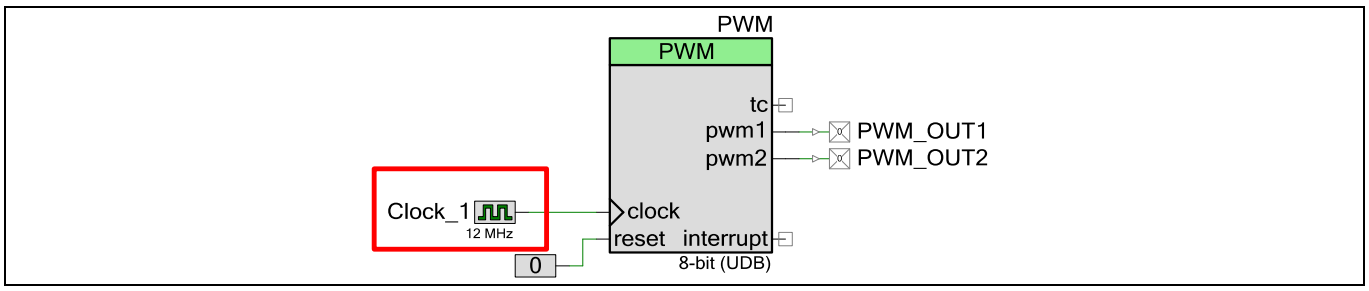

Figure 13 Using Clocks in PSoC Creator

Recommended PSoC 3 MHz ECO Configurations

To configure the Clock Component's frequency and source, double click on the Clock Component to open the configuration dialog. To learn more about configuring the Clock Component, refer to the component datasheet by right-clicking on the Clock Component and selecting "Open Datasheet…" in PSoC Creator.

Related Application Notes

[1] **AN60616** - PSoC 3 and PSoC 5LP Startup Procedure

[2] **AN60631** - PSoC 3 and PSoC 5LP Clocking Resources

[3] **AN2027** - PSoC 1 32.768-kHz External Crystal Oscillator

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Revision history

Document version	Date of release	Description of changes
**	2009-07-02	New Application Note
*A	2009-09-03	Updated project Clarified diagrams
*B	2010-08-20	Updated code Added PSoC 5.
*C	2011-01-04	Added and updated information (low power, startup, R selection, etc.).
*D	2011-06-29	Added trim sensitivity information Added clock tree information Added resonator selection sections Updated unbalanced capacitor information Removed associated project
*E	2011-12-16	Updated load capacitor nomenclature to CL1 and CL2 Corrected trim sensitivity equation typo Added trim sensitivity example Added external clock information Updated template
*F	2012-06-27	Changed title to “PSoC® 3 and PSoC 5 External Crystal Oscillators” Added recommended resonators table Added performance testing metrics Updated Layout Example Updated for PSoC Creator 2.1 Rearranged contents and added “Advanced Topics” section
*G	2012-11-12	Updated for PSoC 5LP Added clocking overview
*H	2015-03-19	Updated for the new interface in PSoC Creator 3.0 Added AMPIADJ modification and selection details Updated Figure 1, 5, 6, 7 and added Table 1 Several minor changes Added section Using Clock Resource in PSoC Creator Updated abstract Updated template
*I	2015-07-31	Updated template Sunset review
*J	2017-04-20	Updated logo and copyright.
*K	2017-07-18	Stated that no extra firmware is required when connecting an external clock to the xtal input, in section 7.7.
*L	2019-08-21	Added crystal power equation in section 6.1.2
*M	2020-03-17	Updated to Infineon Template

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