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Spec No: 001-32399

Spec Title: USER INTERFACE - LCD DRIVING METHODS USING PSOC(R) - AN2228

Sunset Owner: Rajiv Vasanth Badiger (RJVB)

Replaced By: 001-56384

User Interface – LCD Driving Methods using PSoC®

AN32399

Author: Svyatoslav Paliy
Associated Project: Yes
Associated Part Family: All
Software Version: PSoC® Designer™ 5.0
Associated Application Notes: None

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Application Note Abstract

This Application Note provides a basic introduction to LCD construction, working principles, and driving methods. The attached project demonstrates how to drive the multiplexed LCD.

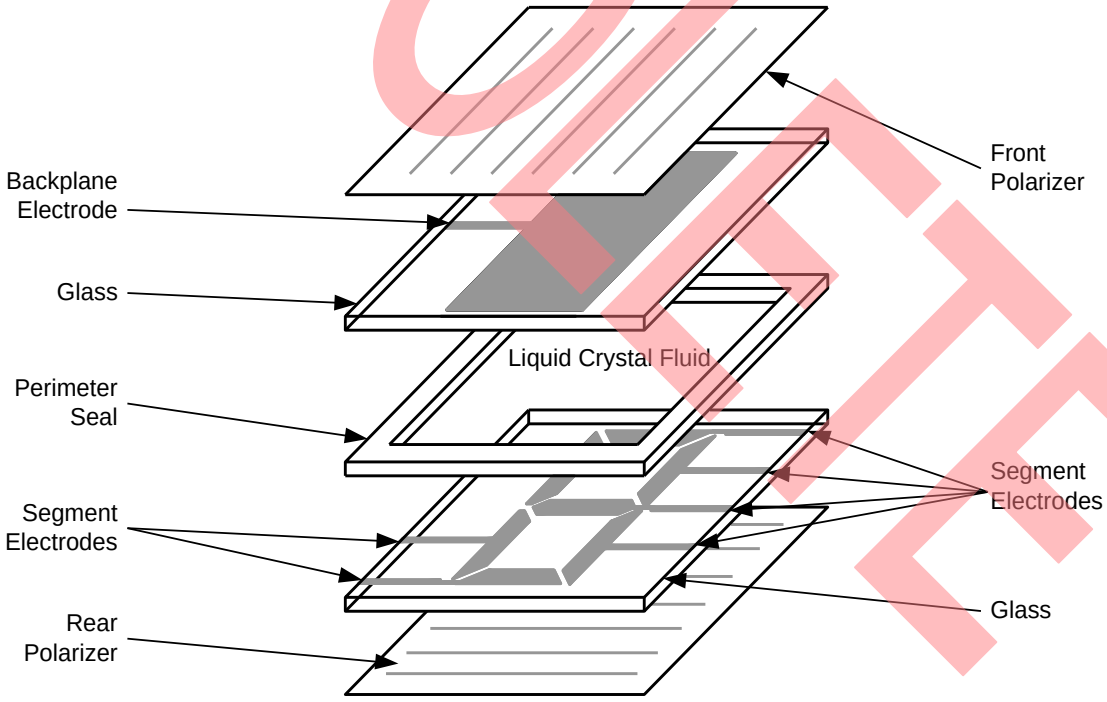
Introduction

Liquid crystal displays (LCDs) are widely used in various applications. They provide good graphic displays, consume minimal energy, and are easy to use.

LCD Basics

An LCD panel is constructed of many layers. Figure 1 shows the typical construction of an LCD panel. The first layer is called a Front Polarizer.

Figure 1. Basic LCD Construction



Polarization is the process in which rays of light exhibit different properties in different directions, especially the state in which all vibrations take place in one plane (see Figure 2). Essentially, a polarizer passes light only in one plane.

The second layer is the glass that provides structural support for the LCD panel. A transparent conductive coating (usually Indium-Tin Oxide) is applied on the bottom plane of the glass and forms the backplane (also called common) electrode. Then a polyimide coating is applied to the conductive coating. The polyimide is rubbed in the same direction as the polarization direction of the front polarizer.

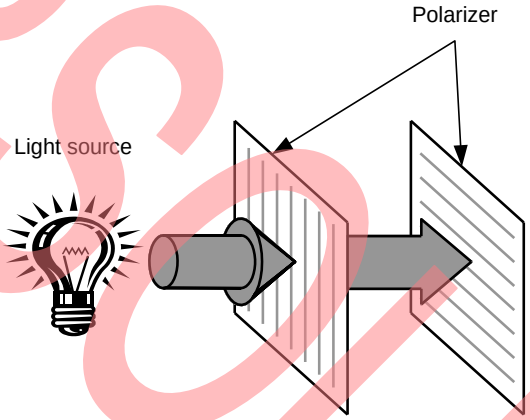
The action of rubbing the polyimide causes the liquid crystal molecules in the outermost plane to be aligned in the same direction.

The third layer is the reservoir of liquid crystals.

The fourth layer is similar to the second layer, which is a glass that provides structural support for the LCD. On the top plane of the fourth layer, a conductive coating is applied. Then a polyimide coating is applied to the conductive coating. The direction of the polyimide is perpendicular to the polyimide direction on the top glass. This orientation prompts the liquid crystal fluid to rotate. The pattern of the conductive coating creates the segments of numbers, letters, symbols, and icons or pixels.

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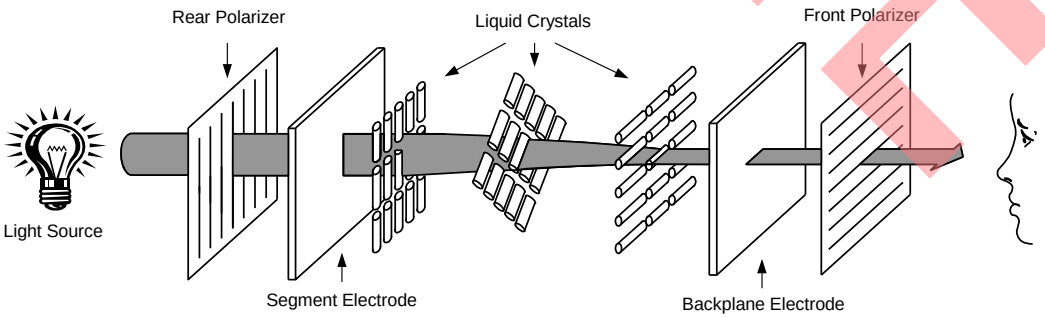
Figure 2. How Polarization Works



The rotation of the liquid crystal fluid is the basis of how the LCD operates. Figure 3 and Figure 4 show how the LCD creates an OFF and ON picture element. In the case of OFF, the liquid crystal fluid is not energized and the potential between the backplane and the segment electrodes equals 0 V_{RMS}.

The light enters through the rear polarizer and is vertically polarized as it goes through all the other elements. Then the light goes unobstructed through the segment electrode to the liquid crystal fluid. The liquid crystal fluid rotates the light polarization direction and causes the light to leave the liquid crystal fluid horizontally polarized. Then the light passes unobstructed through the transparent backplane electrode and the front (horizontal) polarizer.

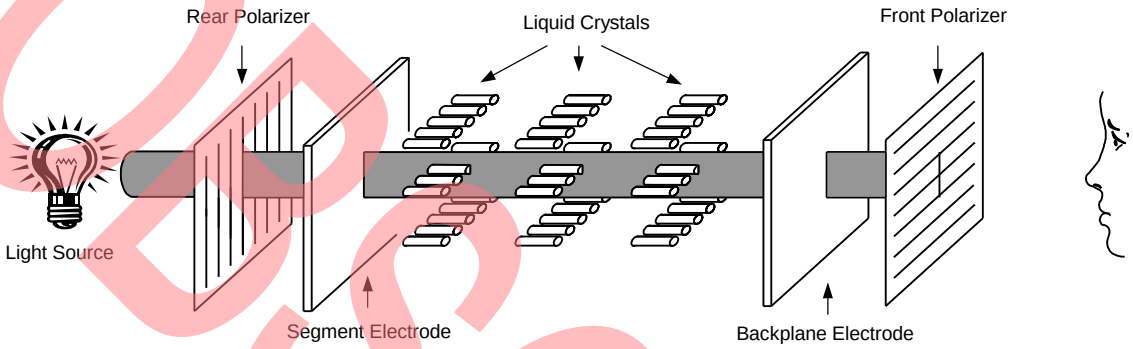
Figure 3. Light Path for OFF Pixel



After applying light source between the segment and the backplane electrode, the liquid crystal fluid becomes energized. The molecules of liquid crystal now align themselves such that they are parallel to the electrical field generated by the potential differences. This removes the effect of light polarization rotation direction (see Figure 4).

In this case, the light enters the LCD trough the rear polarizer and becomes polarized vertically such as in the OFF pixel case. The polarized light passes unobstructed through the segment electrode, the liquid crystal fluid, and the backplane electrode. Because the light is still polarized on the vertical plane, it is obstructed by the front polarizer, which has horizontal polarization. Because the light is obstructed, it creates dark regions on the display and the observer detects that the pixel is ON.

Figure 4. Light Path for ON Pixel



There are essentially three types of viewing modes for an LCD:

- Transmissive
- Reflective
- Transflective

The transmissive LCD uses the light source placed on the back of the LCD panel (figures 1 through 4 show transmissive LCDs).

A reflective LCD has a light reflector instead of a light source on the back of the panel.

The third type of display is called transflective, which is a combination of transmissive and reflective. A white or silver translucent material plane is applied to the rear of the display. It reflects some of the ambient light back to the observer while also enabling backlighting. However, a transflective LCD has a lower contrast ratio than the other types of LCDs due to some reflected light passing through the reflector while some of the backlight is obstructed by the reflector.

Temperature Effects

Temperature has a large impact on the performance of the LCD panel. All liquid crystal fluids have well defined temperature operation limits.

If an LCD operates above its fluid limit, the liquid crystal molecules begin to assume random orientation instead of rotated-plane orientation. In this case, all segments of the LCD become ON. Also, temperatures that exceed 110° C cause the Indium-Tin Oxide and polyimide coatings to deteriorate.

Low temperatures slow the LCD response time due to increased viscosity of the liquid crystal fluid. At very low temperatures, such as -60° C, the fluid turns into a crystalline state.

Driving Voltages

The LCD must only be driven with AC voltages. A DC voltage deteriorates the liquid crystal fluid and hence cannot be energized. Therefore, DC voltage applied to LCD electrodes may harm and destroy the LCD. The LCD driver waveforms are designed to create 0-V_{dd} potential across all LCD segments.

Static LCD

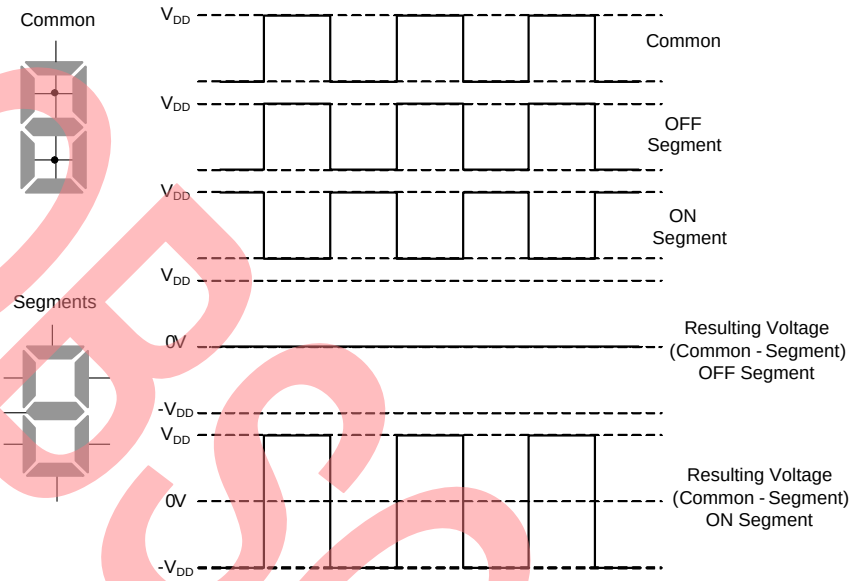
Static LCD has one pin for each segment and one pin for the backplane. Static LCD has a high contrast ratio but requires a great number of pins, (e.g., an 80-segment LCD requires 81 pins). Typical examples of static LCDs are clocks, phone displays, and similar LCDs dedicated to show numbers and or status icons with minimal segment counts.

With static LCDs, each segment pin drives one segment. Figure 5 on page 4 shows a waveform example of a static LCD.

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As you see, if the segment waveform equals a common waveform, then the segment is in OFF state. If the segment waveform equals an inverted common waveform, then the segment is in ON state.

Figure 5. Common and Inverted-Common Static LCD Waveforms



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Driving the Static LCD with PSoC

Currently, there are no production PSoC devices with internal LCD controller hardware to drive the static and multiplexed LCD without software influence. But, PSoC has unique flexibility in output drive port modes and internal signal routing to enable driving LCD types (both static and multiplexed) with minimum external components and software load.

Driving a static LCD is negligible. The hardware timer is used as a 50 to 60 Hz interrupt source. The interrupt handler performs all the necessary functions for the LCD driving routine.

Code 1. Driving the Static LCD

```
#pragma interrupt_handler Timer_Interrupt

void Timer_Interrupt()

{

  static BYTE common = 0xFF;

  // invert base to get the common waveform //

  common = ~common;

  // If bit in the "data" is set, the corresponding bit in PRTxDR is set "not data". Therefore, corresponding segment in LCD is ON //

  PRT0DR = common ^ data0;

  PRT1DR = common ^ data1;

}
```

`data0` and `data1` are global variables where each bit corresponds to one segment on the display. The port bits that correspond to ON LCD segments are inverted in anti-phase to the common backplane. The bits that are related to the OFF LCD segments are inverted in phase to the common electrode.

Driving the Multiplexed LCD with PSoC

LCD segments are often multiplexed to reduce pin count. This means that individual LCD segments are arranged in a matrix of segments and common pins, such that each LCD segment is a unique combination of a segment pin and a common pin, which are used for activation. But each segment pin and common pin may be used for more than one segment. Due to the multiplexing of different segments with the same segment pins, the required drive signals for the segment pins and common pins could be complicated. Each segment and common pin of a multiplexed LCD requires a time-division-multiplexed signal to turn on only the desired segments and to avoid having a DC voltage on any segment at the same time.

Multiplexed LCDs can be driven by two types of waveforms, which are called Type A and Type B in LCD specifications and data sheets. Prior to the definition of the driving types, the term frame frequency must be defined.

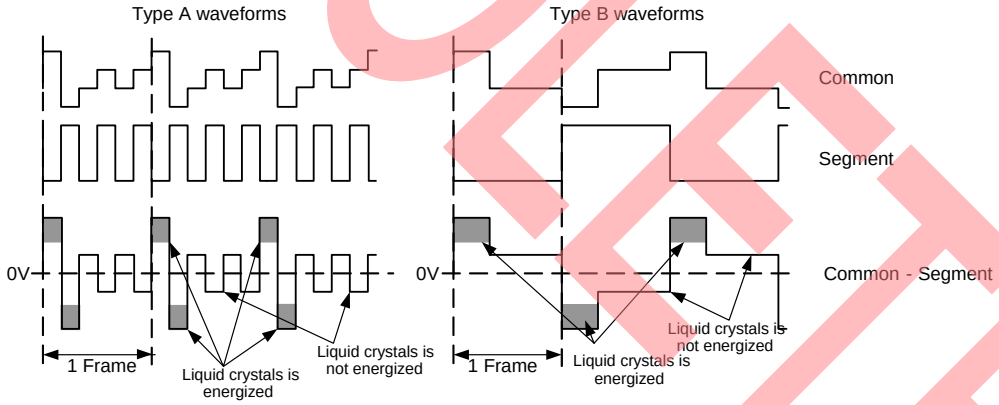
The LCD frame frequency is the rate at which the backplane and segment outputs change. The typical range of the frame frequencies is between 50 and 150 Hz. Higher frequencies result in higher power consumption and lower frequencies cause image flickering on the LCD.

As previously mentioned, the LCD must maintain zero DC potential on every segment.

Type A waveforms take single frames to maintain 0 V_{dd} whereas Type B waveforms take two frames to maintain 0 V_{dd}. Figure 6 shows Type A and Type B waveforms.

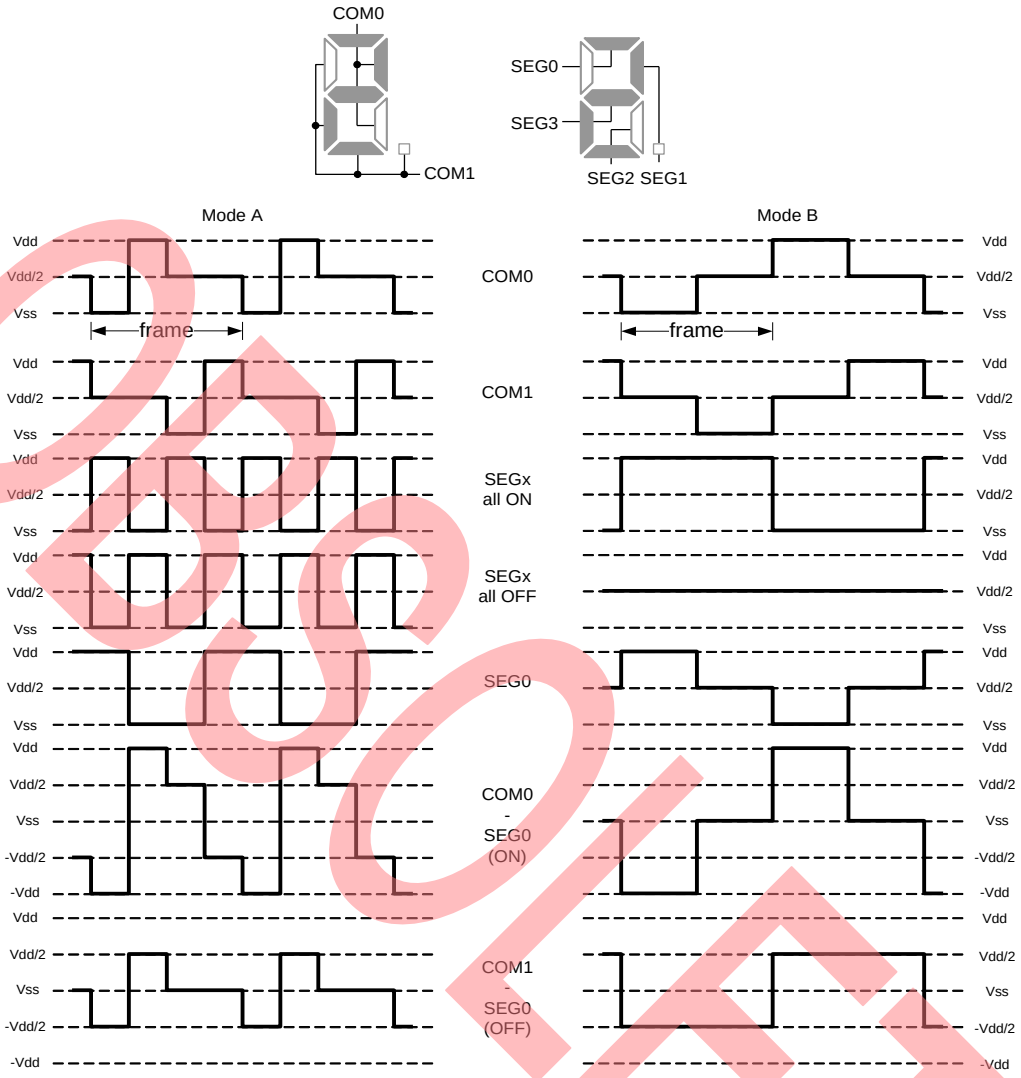
Each multiplexed LCD is characterized by the bias and duty ratio, which are defined by LCD type, its construction, and materials used. Bias is the number of voltage steps to be applied to the LCD. Therefore, the voltage level amount used to power the LCD display is equal to voltage steps + 1. Duty cycle ratio or duty cycle indicates the number of commons; each common line is driven by each individual output. Figures 7 to 15 show examples of waveforms for different bias and duty cycle ratio LCDs.

Figure 6. Type A and Type B Waveforms



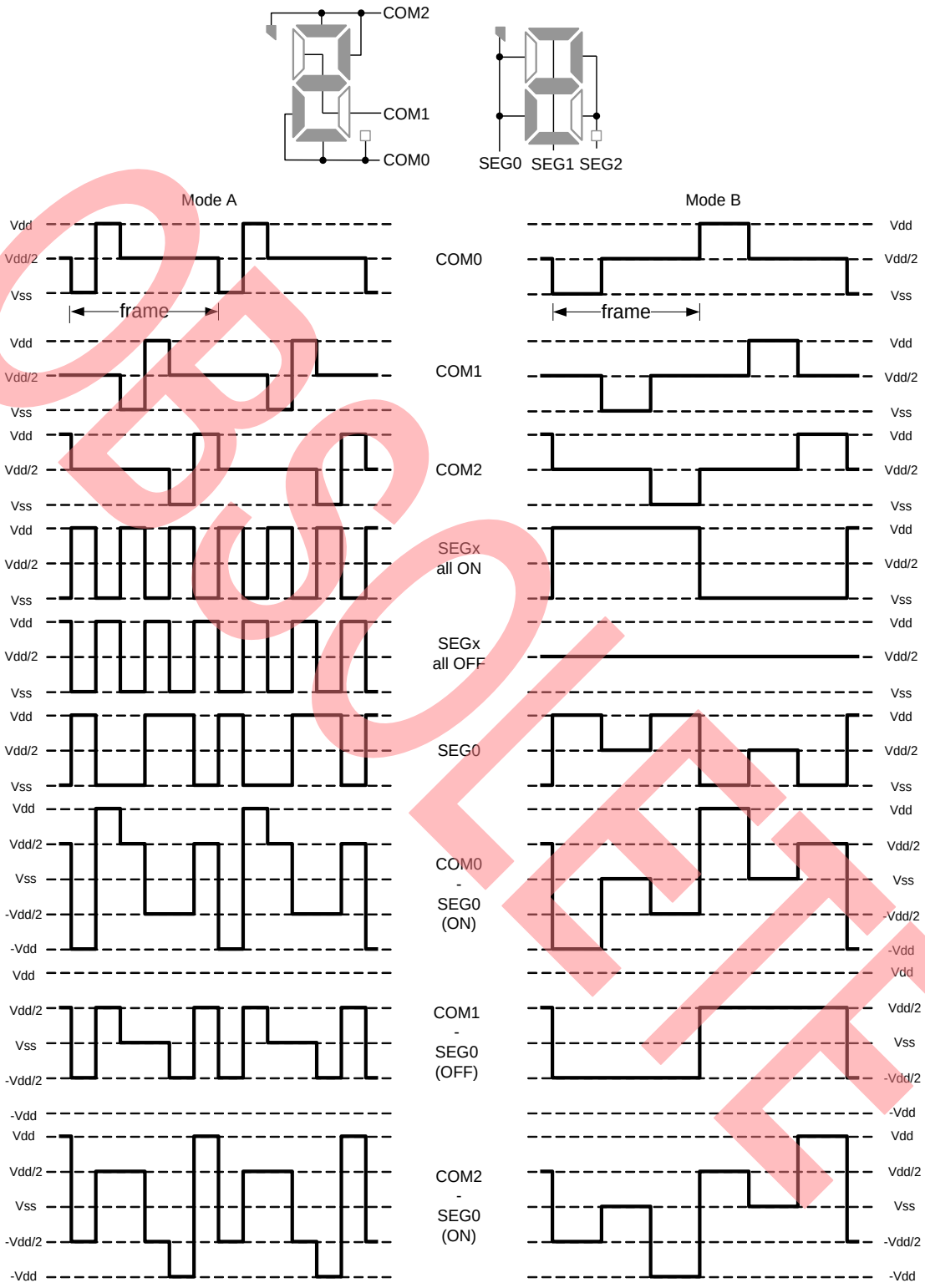
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Figure 7. 1/2 Bias and 1/2 Duty Ratio Waveforms



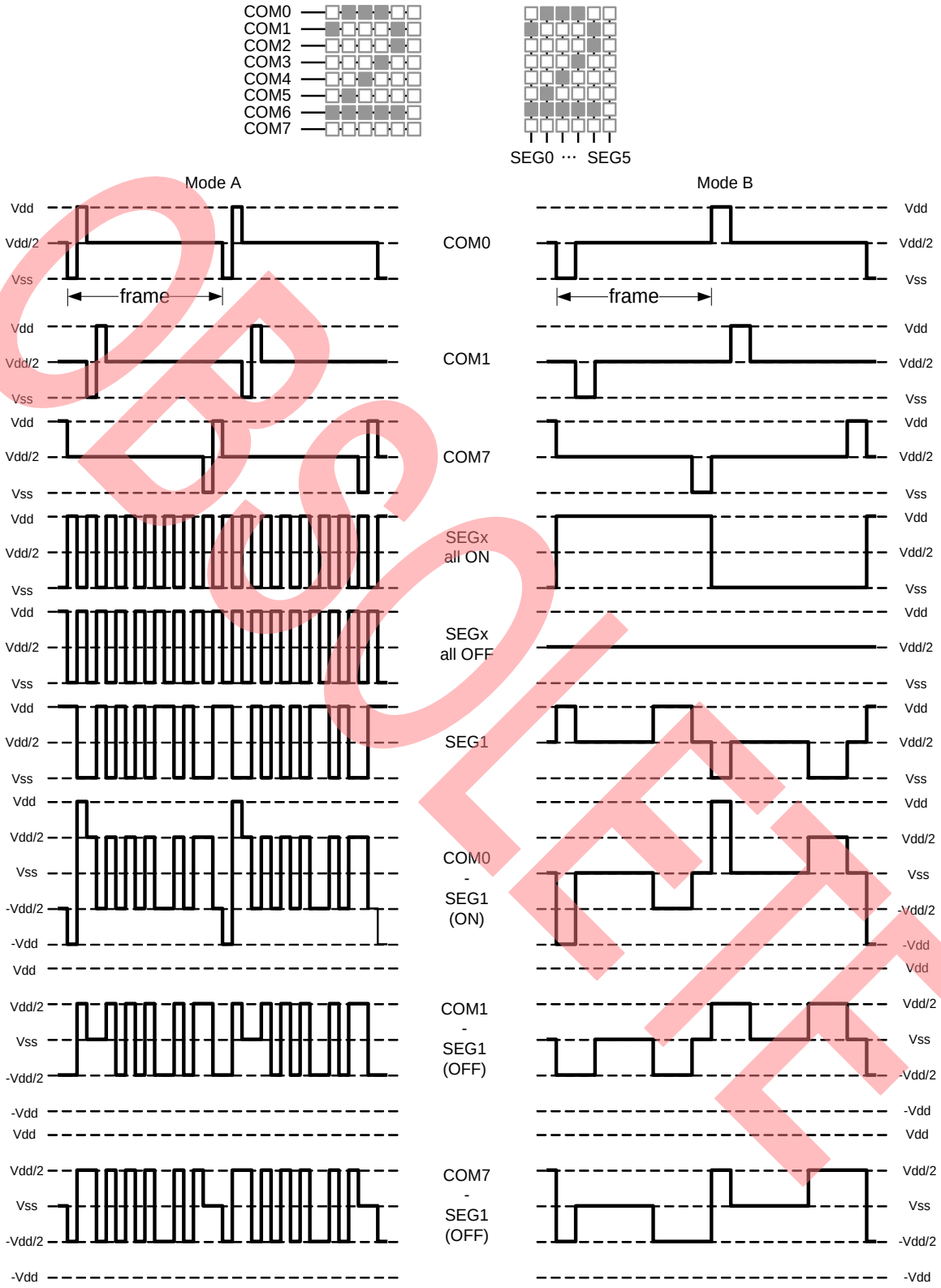
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Figure 8. 1/2 Bias and 1/3 Duty Ratio Waveforms



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Figure 9. 1/2 Bias and 1/8 Duty Ratio Waveforms



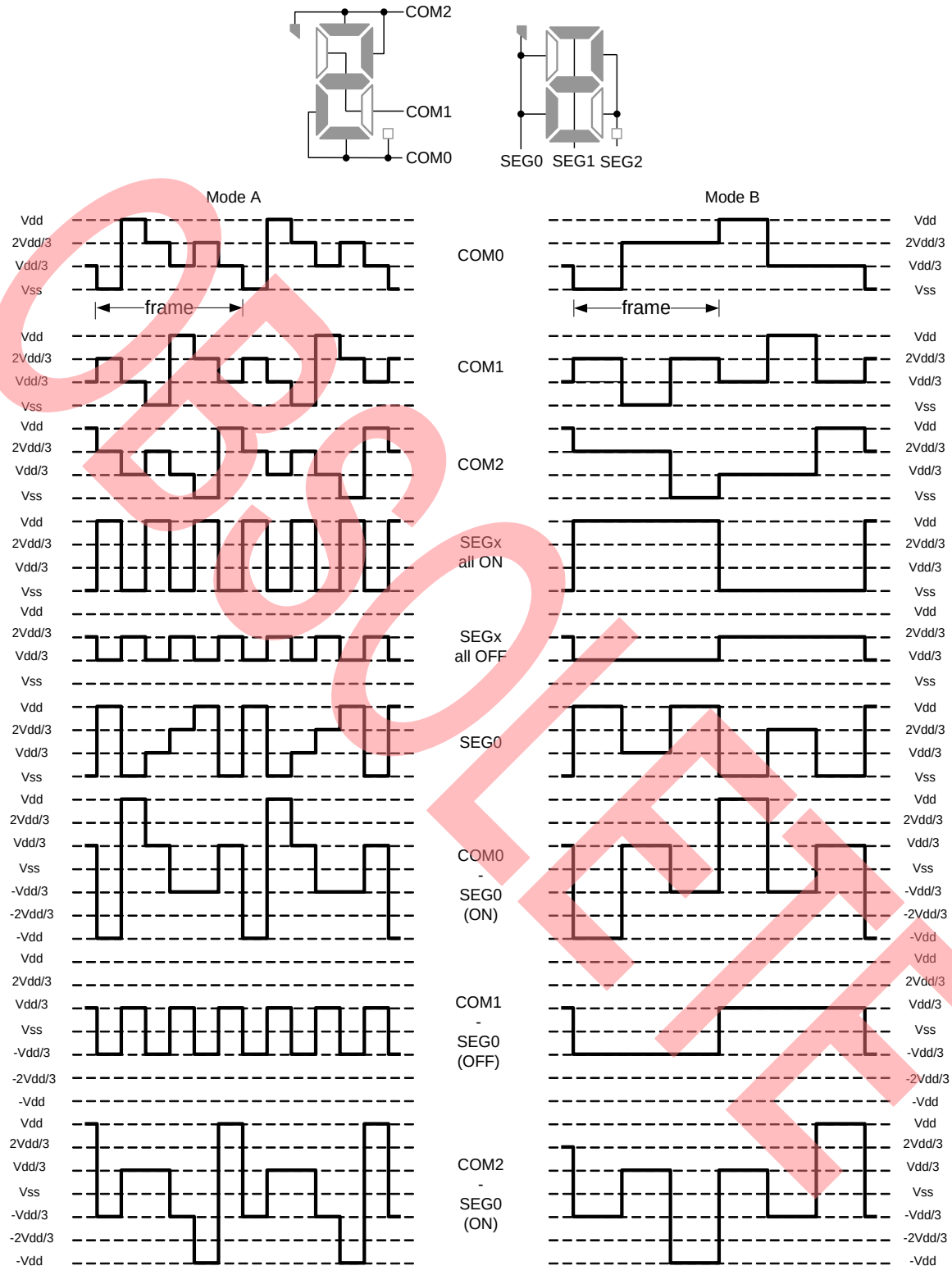
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Figure 10. 1/3 Bias and 1/2 Duty Ratio Waveforms



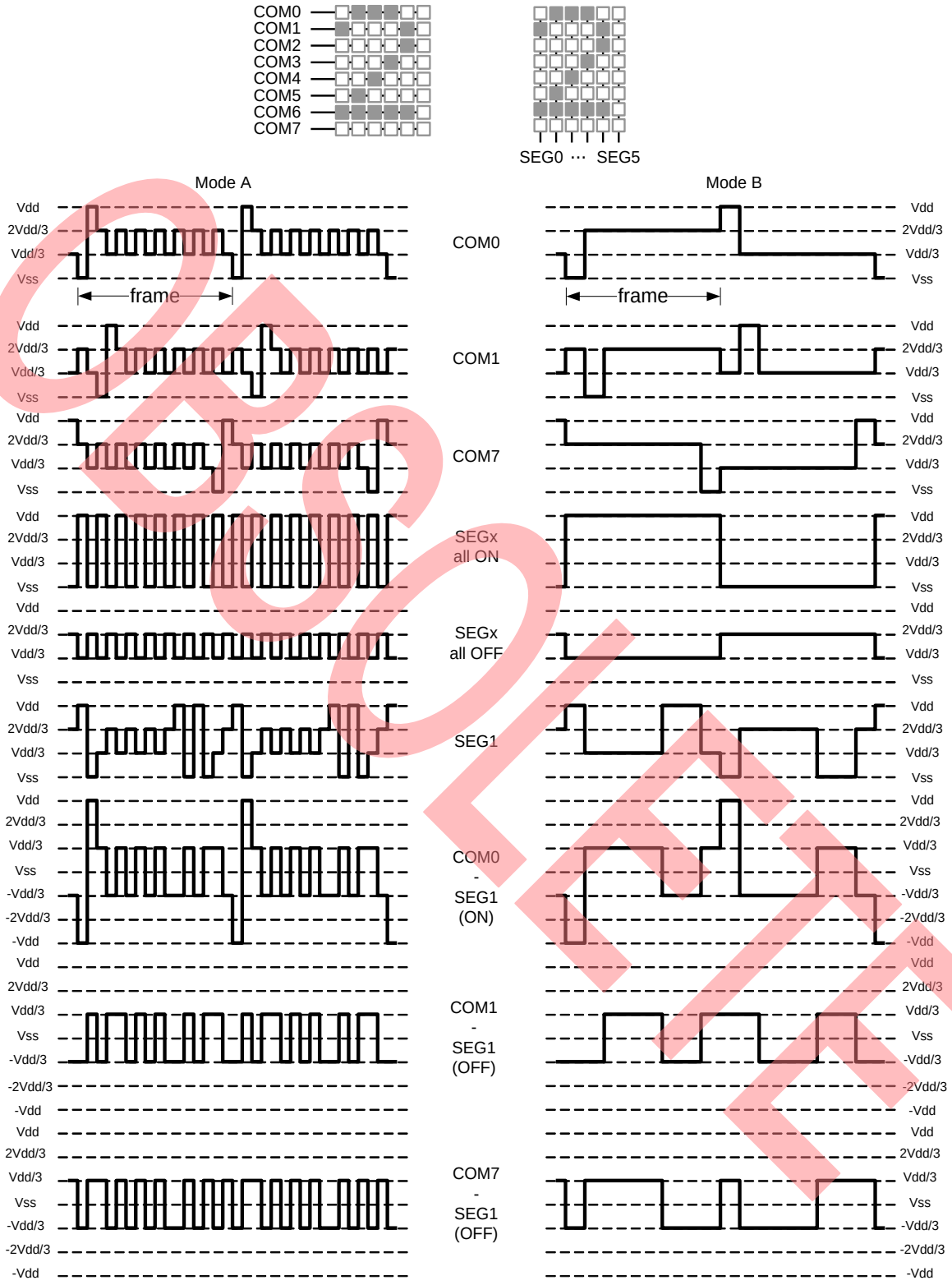
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Figure 11. 1/3 Bias and 1/3 Duty Ratio Waveforms



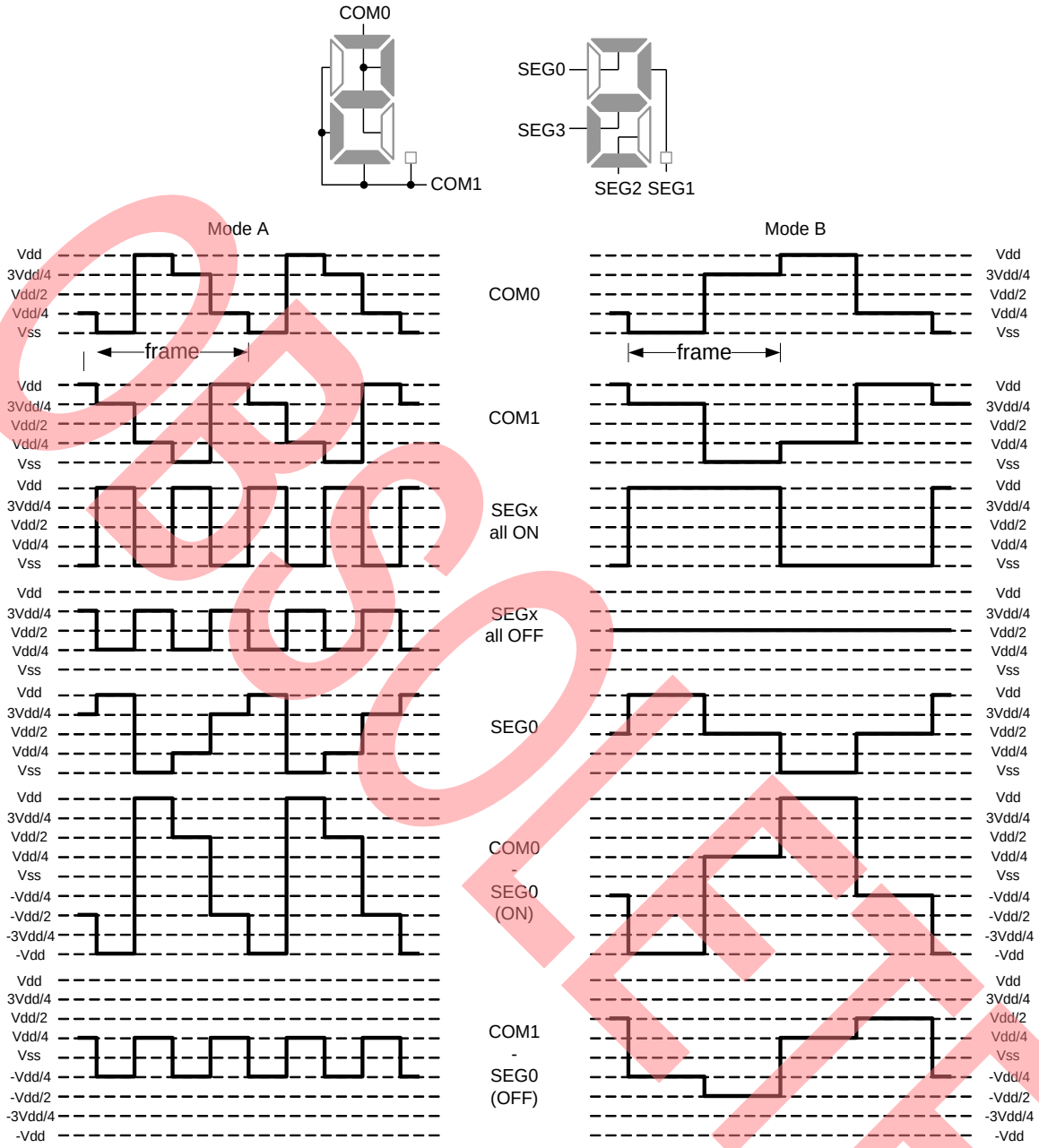
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Figure 12. 1/3 Bias and 1/8 Duty Ratio Waveforms



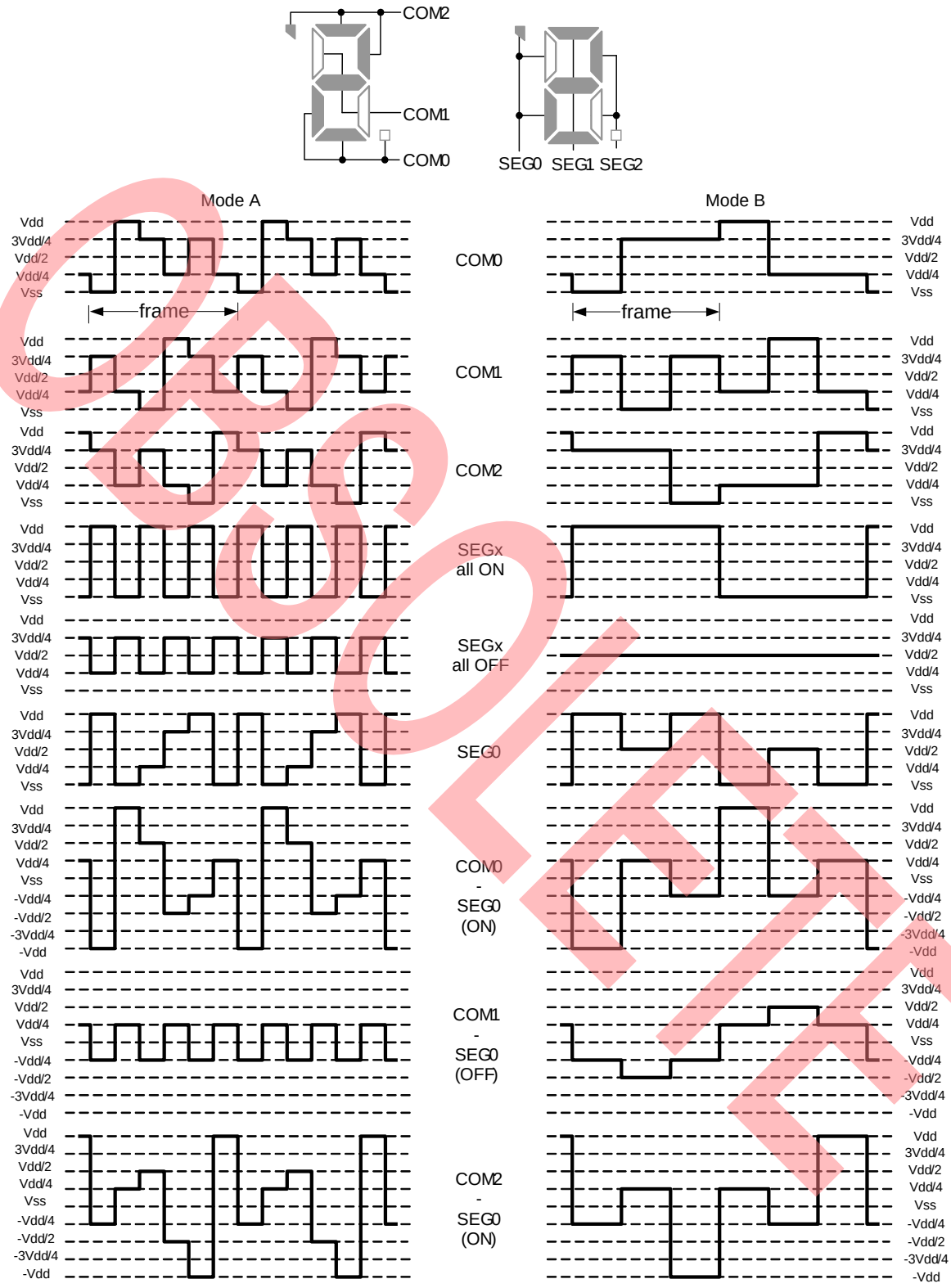
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Figure 13. 1/4 Bias and 1/2 Duty Ratio Waveforms



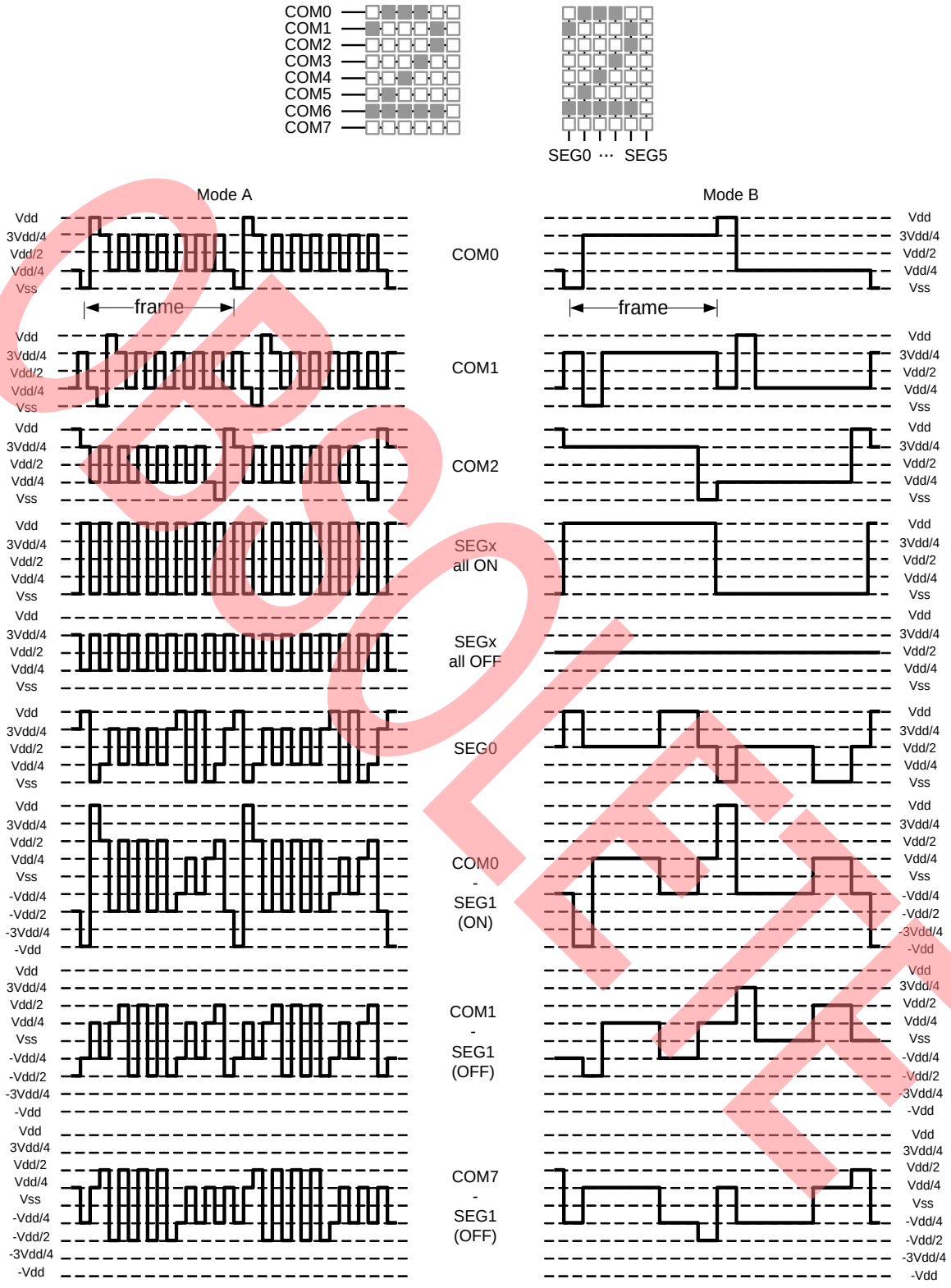
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Figure 14. 1/4 Bias and 1/3 Duty Ratio Waveforms



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Figure 15. 1/4 Bias and 1/8 Duty Ratio Waveforms



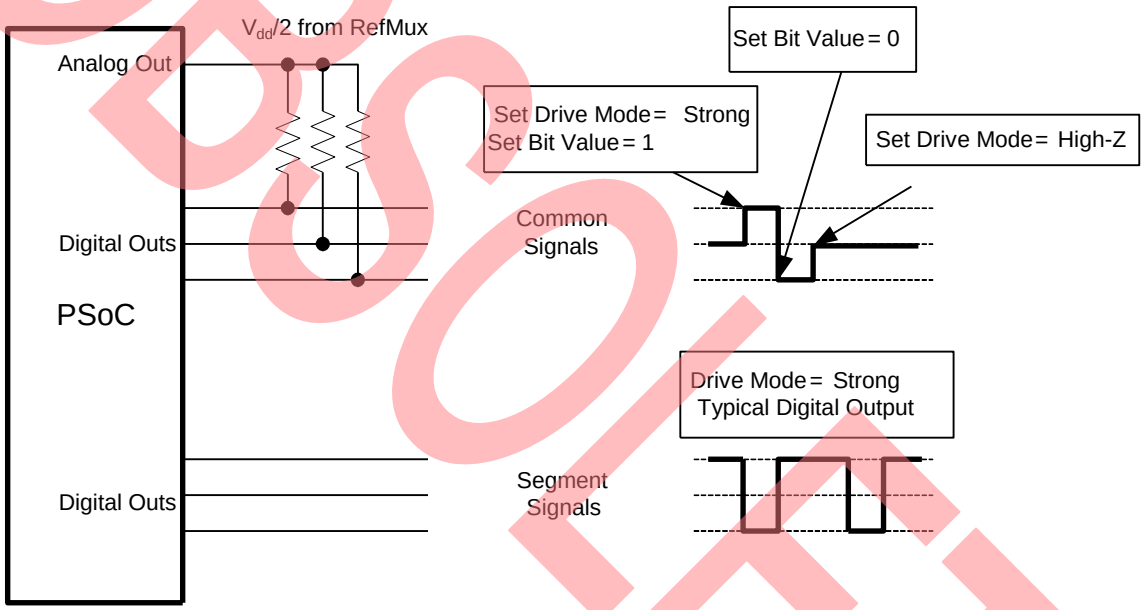
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Principles of using PSoC as LCD Driver

As shown in the previous waveform figures, the multilevel signal is required from the driver. PSoC has a limited number of analog output pins. Therefore, digital output pins should be used with some external biasing and on-the-fly drive mode changes in order to obtain intermediate voltage levels.

The first case concerns the voltage levels for 1/2 bias mode (see Figure 16). For Type A waveforms, three voltage levels (V_{ss}, $V_{dd}/2$ and V_{dd}) are needed for the common signal and only two levels (V_{ss} and V_{dd}) are needed for the segment signals. For Type B waveforms, three voltage levels are needed for both the common and segment signals. To form V_{ss} and V_{dd} levels, strong drive mode '0' and '1' were used in the port data register. To form the external $V_{dd}/2$ voltage level, which sets the pin level, the combination of the port mode and bit value must enable high impedance of the pin (for example open drain low and '1' and so forth). The resistance between $V_{dd}/2$ output and common output must be about 5 to 20 kΩ.

Figure 16. 1/2 Bias Signal Generation



In the case of 1/3 bias mode, four voltage levels (V_{ss}, $1/3V_{dd}$, $2/3V_{dd}$ and V_{dd}) are required. To form V_{ss} and V_{dd} levels, strong high and low drive modes may be used. To obtain two additional levels, the resistive pulldown or pullup drive modes may be used. The internal pulldown or pullup drive modes, with external resistors, create a resistive divider that generates the desired four different voltage levels (see Figure 17). Generation of 1/3 bias signals is shown in Figure 18. The external resistance value must approximately equal one half of the internal pulldown or pullup drive mode resistance. Unlike the 1/2 bias mode, the high impedance drive mode is not used.

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Figure 17. Generating Four Voltage Levels

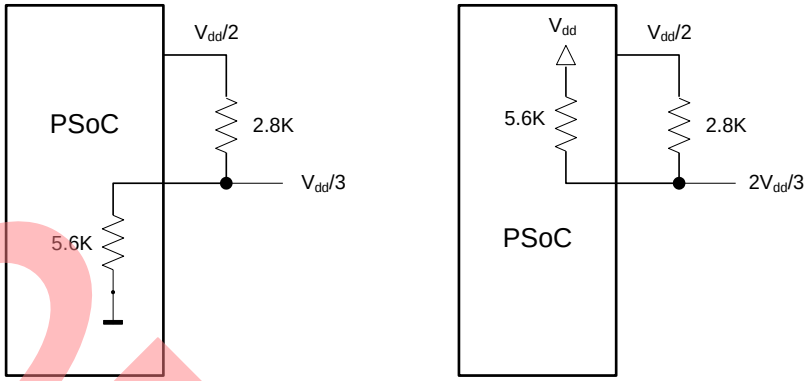
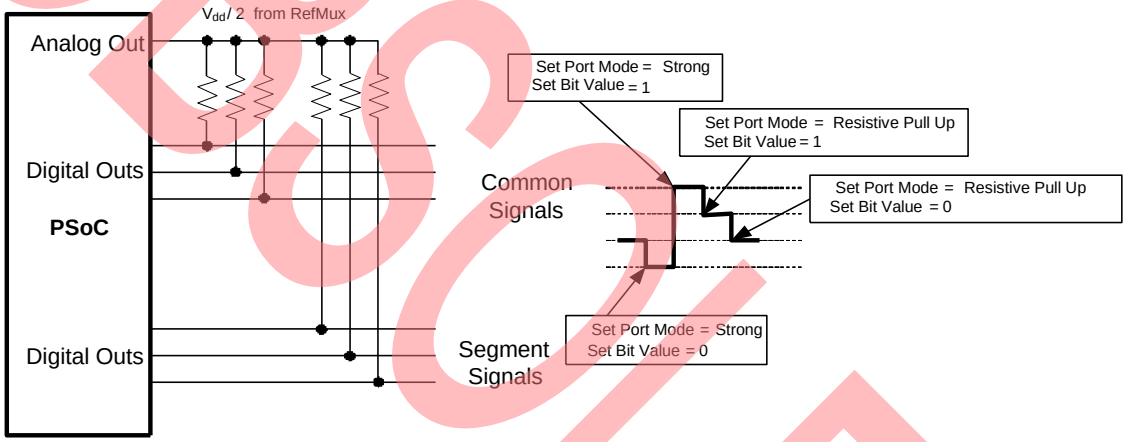


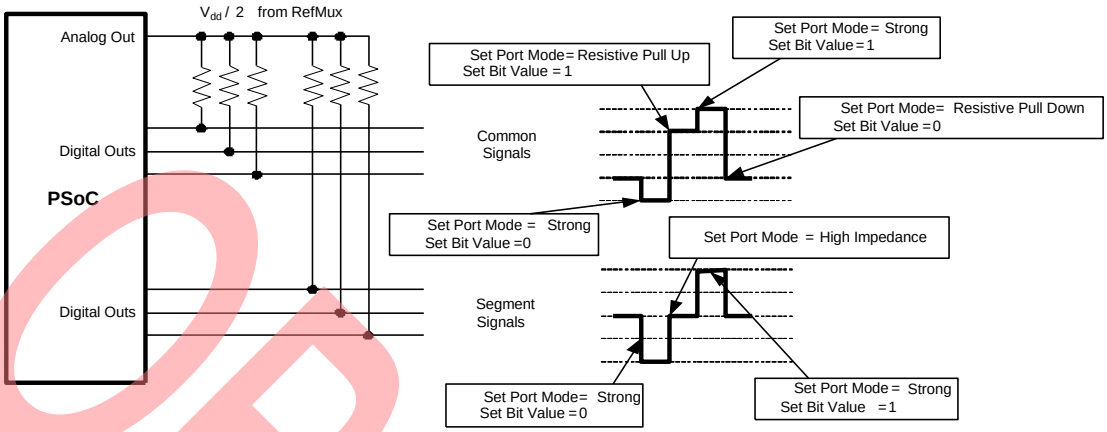
Figure 18. 1/3 Bias Signal Generation



The 1/4 bias signal generation is similar to 1/2 and 1/3 bias signal generation, but both the high impedance and the resistive pulldown or pullup drive modes were used to obtain the five voltage levels. Figure 19 illustrates 1/4 bias signal generation. In this case, the external resistance value is equal to the nominal internal pulldown or pullupdrive mode resistance, which equals 5.6 kΩ. Note that the internal pulldown or pullup resistor may vary in the 4-8 kΩ range (see PSoC specifications) but the pull-down resistor value always equals the pullup resistor value due to their location on the die. This is not critical because variation of these resistance values causes only symmetrical charges to intermediate levels, not V_{dd}, $V_{dd}/2$, V_{ss} levels. Therefore, this situation does not cause DC presence. The internal resistor tolerances can change the LCD contrast. Contrast may easily be adjusted using the PWM driving method, which is discussed ahead.

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Figure 19. 1/4 Bias Signal Generation



LCD Driving Method with Contrast Adjustment

In many situations, the contrast adjustment is an important feature for end applications. For example, contrast adjustment is mandatory for devices that are used in wide temperature ranges, because the liquid crystal molecule re-orientation threshold varies depending on temperature. A normally well-contrasted display may be unreadable under high or low temperatures. Typically, LCD contrast is adjusted by increasing and decreasing the driving voltage value. The dedicated LCD drivers enable the connection of the external potentiometer to manipulate driving voltage. The contrast can also be adjusted in the PSoC-based driver implementation by varying the supply voltage. However, this method is not a very good solution because a supply voltage change in the PSoC device may create unfavorable conditions elsewhere.

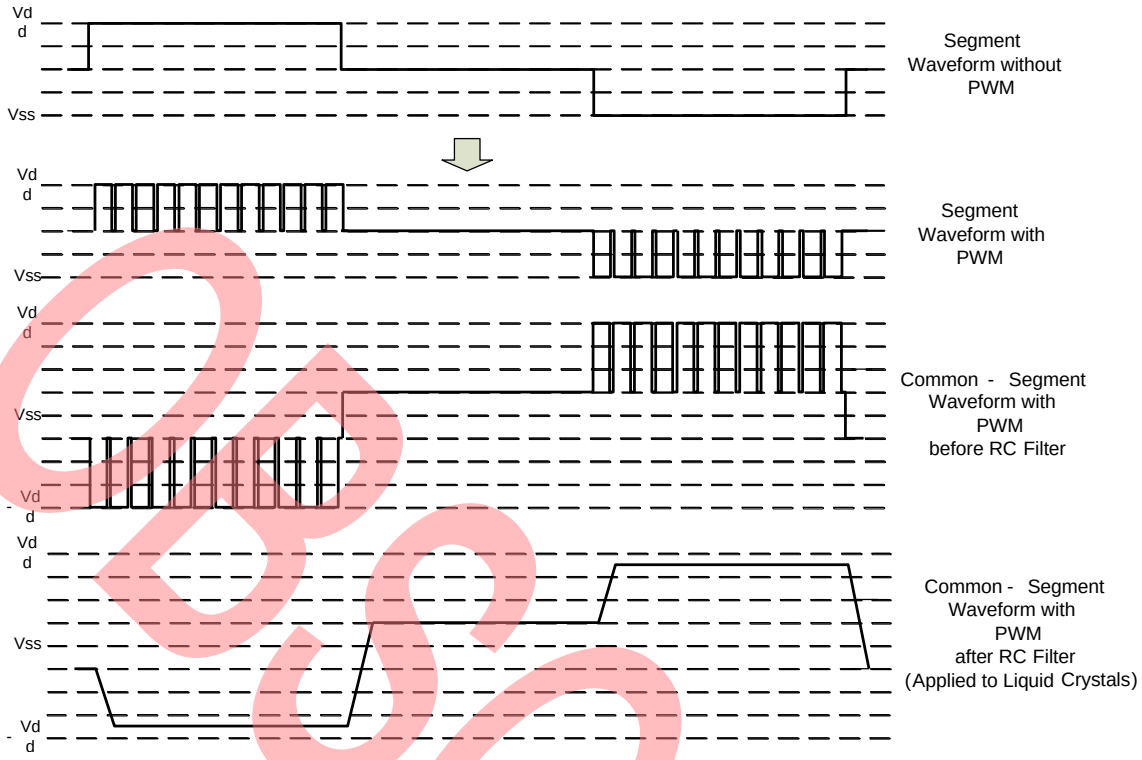
An alternative method is to gradually adjust the LCD contrast ratio. This reduces the tolerance influence of the internal pulldown or pullup resistors. This method is based on the use of the internal LCD capacitance that together with applying a variable duty cycle PWM signal, enables manipulation of the LCD driving voltage.

The common and segment electrodes of the LCD create a capacitor with the approximate value of 3-20 nF, depending on the LCD electrode's square and the liquid dielectric constant value. In this method, the common signals are supplied as shown in Figure 19. But segment signal driving becomes more complicated. Instead of using fixed V_{ss}, $V_{dd}/4$, $3V_{dd}/4$ and V_{dd} values, variable duty cycle PWM signals are used. Only the $V_{dd}/2$ voltage is left constant and is formed by using the RefMux.

Figure 20 on page 18 shows the PWM usage for contrast adjustment. It also shows that the actual PWM frequency is much greater than the LCD frame frequency.

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Figure 20. PWM Usage for Contrast Adjustment (Schematic)

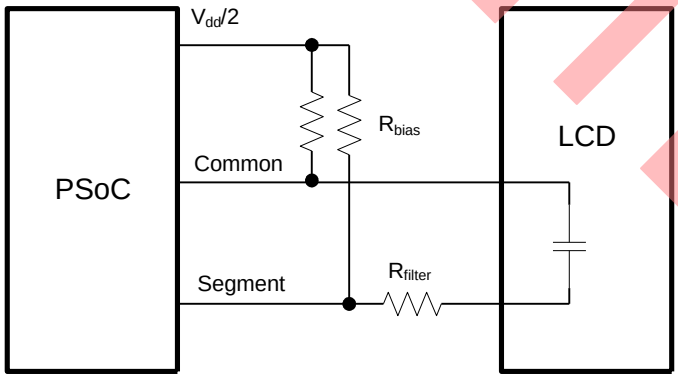


The Resistance R_{filter} and the segment capacitance together create a low-pass filter, which filters the PWM signal and produces clear DC voltage to the applicable segment. Resistance is added sequentially with a segment wire and calculated using Equation (1) in such a way that the filter time is constant and greater than the drive PWM signal period.

- R is the resistor value
- T is the PWM period
- C is the LCD electrode internal capacitance

$$R \approx \frac{10T}{C} \qquad \text{Equation 1}$$

Figure 21. PWM Used for Contrast Adjustment



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Practical Implementation of an LCD Driver

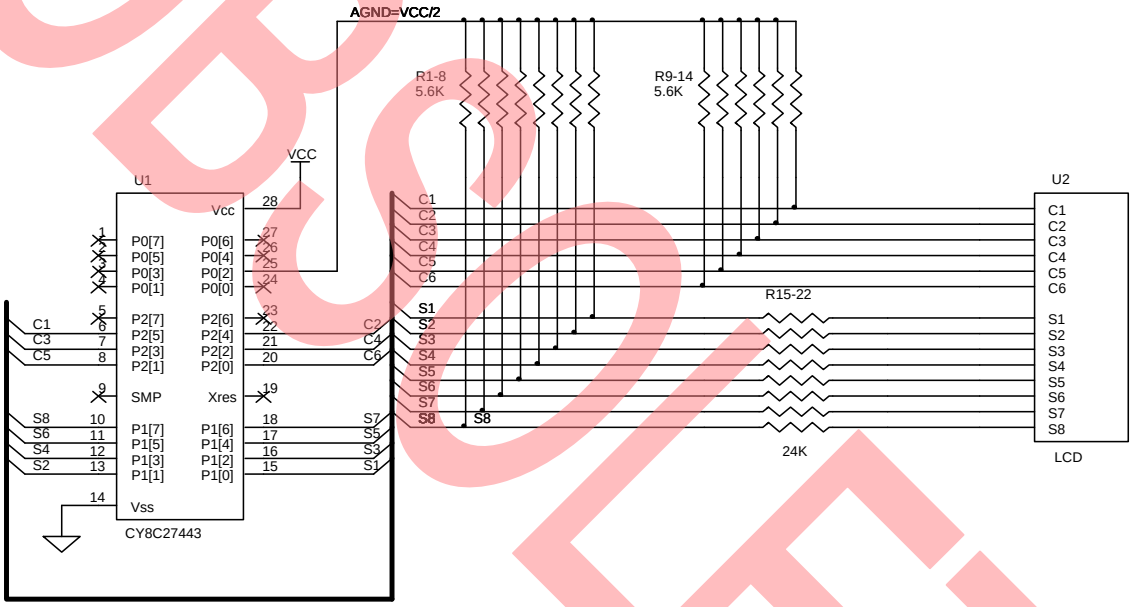
Associated to this project is a 1/4 bias mode, 1/6 duty cycle ratio, and Type B LCD driving example with implemented contrast adjustment. This project uses an LCD that has six common signal pins and eight segment signal pins. Nominal operating voltage is 5V and internal capacitance is 5 to 9 nF. The frame frequency for this LCD is equal to 64 Hz.

The schematic for this project is shown in Figure 22. Resistors R1-R14 are dedicated to $V_{dd}/2$ level biasing. Resistors R15-R21 use internal LCD capacitance that forms the segment RC filters previously mentioned.

The internal structure of the PSoC is very simple and consists of a 16-bit timer (Timer16) dedicated to generate periodic interrupts with a frequency of 64*6 Hz = 384 Hz. The PWM8 generates a PWM signal with an output frequency of 93.75 kHz (T = 10.6 µs). The DigBuf User Module sends the PWM signal to all of the global output wires. One analog user module, RefMux, is used to supply $V_{dd}/2$ reference voltage to port pin, P0[2].

All driver functionality is implemented in the interrupt handler that serves interrupts from Timer16. The main() routine only contains initialization of the internal user modules.

Figure 22. Project Schematic



The resistive pull-down drive mode is used to form common electrode levels during the first frame. The value 00100000b is written to the port and shifted to the right during each new interrupt within the first frame. If '1' is written to the port, it produces the V_{dd} level on the LCD pin. If '0' is written to the port, it produces the $V_{dd}/4$ level on the LCD. The second frame is similar to the first, but 11011111b is written to the output port and the port drive mode is changed to a resistive pull up. A '0' written to the port initiates the V_{ss} voltage level and a '1' initiates the $3V_{dd}/4$ level.

To form the segment signals, the open drain low drive mode is used and '1' is written to all port bits during the first frame. For the second frame, the port is configured as an open drain high and '0' is written to all of the port bits. Therefore, port output stays in High-Z during both frames. To turn ON the LCD, the segment pin is connected to the global output bus by directly writing to the PRTxGS register. To turn OFF the LCD, the segment port should be disconnected from the global output bus and the $V_{dd}/2$ level should be obtained from the external bias.

The proposed method enables the LCD segments to turn ON or OFF by modifying only one PRTxGS register and a minimal number of drive modes or port data registers. Note that each bit of PRTxGS corresponds to one LCD segment.

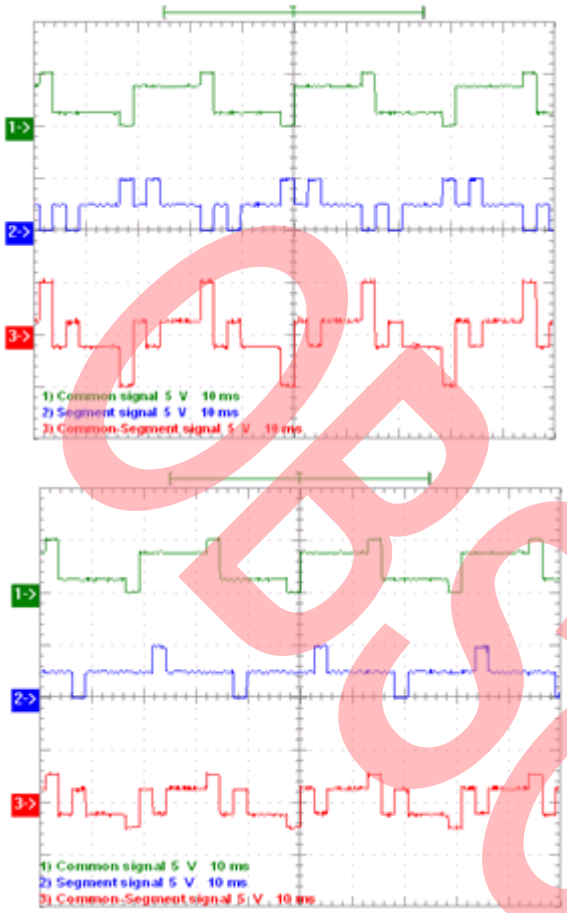
The PWM output is connected to all internal global buses. Row LUTs are configured as inverters to pass the PWM signal to the global output buses during the first frame and non-inverted during the second.

This trick enables symmetrical $V_{dd}/2$ output levels without changing the compare value of the single PWM generator. Modifying the PWM duty cycle causes the LCD contrast ratio and segment driving voltage amplitude to change.

The measured waveforms of the common signal, the segment signal, and resulting waveforms applied to the liquid crystal are shown in Figure 23 on page 20.

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Figure 23. Real LCD Waveforms Obtained from a Scope



Summary

This Application Note demonstrates how to drive various LCD contrasts using the PSoC device without any dedicated LCD controllers. The proposed project can easily be modified to support other LCD types with different bias, duty cycle ratio, and segment numbers.

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Document Number: 001-32399

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1491203	SWU	09/20/07	New Application note.
*A	2912109	SVYP	05/19/10	Project is updated to use new project structure introduced in the PD5.0 that cause some issues during open old project. Refer to PSoC Designer version 5.0 on the first page. Fixed ON Segment and OFF Segment labels on the Figure 5. Fixed frame arrows on the Figure 6. Updated author contact on the last page. Added document history.
*B	4036244	RJVB	06/21/2013	Obsolete spec

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