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Spec No: 001-32909

Spec Title: PROGRAMMABLE ANALOG HIGH CURRENT SOURCE, PSOC(R) 1 STYLE - AN2203

Sunset Owner: Rajiv Vasanth Badiger (RJVB)

Replaced By: 001-40440

# Programmable Analog High Current Source, PSoC® 1 Style

# AN2203

**Author**: Dave Van Ess
**Associated Project**: Yes
**Associated Part Family**: CY8C24xxxA, CY8C27xxx, CY29xxx
**Software Version**: PSoC Designer™ 5.1 SP1
**Associated Application Notes**: AN2089

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## Application Notes Abstract

The unique configuration of the PSoC®1 switched capacitor blocks allows, with the addition of an external pass transistor and current setting resistor, the construction of a programmable current source. A detailed explanation of this function is provided, demonstrating how to build a programmable current source using a single switched capacitor block.

## Introduction

One of the first functions required by users was a programmable current source. The first response to this need was a bipolar current source capable of sourcing or sinking 40 mA, documented in application note, AN2089: *Programmable Bipolar Analog Current Source, PSoC Style*.

Of course, the natural user was to ask for more; “More current please!”

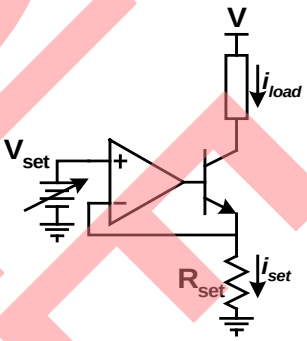
This application note provides:

- A brief explanation of opamp based current sources.
- An explanation of how a switched capacitor integrator can be substituted to simulate an opamp.
- An example of analog current source implemented with a single PSoC analog switched capacitor block.

## Current Source

Figure 1 shows a classic design of a current source built with an opamp and a bipolar pass transistor.

Figure 1. Opamp and Pass Transistor Current Source




This circuit has an opamp configured with negative feedback. The opamp attempts to do whatever is necessary to make a voltage difference between its inputs zero. This condition is met when the opamp’s output is a base emitter junction greater than $V_{set}$ as shown in Equation 1.

$$V_{out} = V_{be} + V_{set} \quad \text{Equation 1}$$

The voltage across the reference resistor is one base emitter junction lower than the opamp output or $V_{set}$. Equation 2 defines the current generated by the resistor.

$$i_{set} = \frac{V_{set}}{R_{set}} \quad \text{Equation 2}$$

The load current is approximately equal to the set current. It differs by the beta value of the transistor. The actual load current is shown in Equation 3.

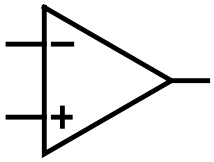
$$i_{load} = \frac{\beta}{\beta + 1} \cdot i_{set} \quad \text{Equation 3}$$

This circuit is easily constructed given an unencumbered opamp. This set of connections is possible using continuous time PSoC blocks, but due to routing phase shift, this topology is unstable. What is needed is an equivalent PSoC topology that is stable.

## Faux Opamp S'il Vous Plait

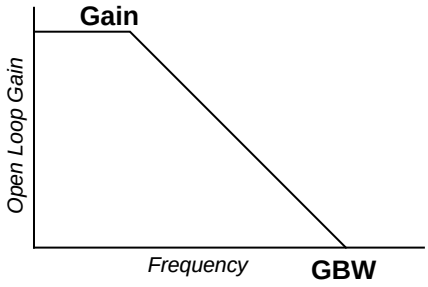
A generic compensated opamp is shown in Figure 2.

Figure 2. Generic Compensated Opamp



Its Bode plot is shown in Figure 3.

Figure 3. Typical Opamp Bode Plot




The opamp has an open loop DC **Gain** and rolls off at the roll-off frequency **Gain/GBW**. The frequency where the gain is equal to one is known as the gain bandwidth (**GBW**). The transfer function is shown in Equation 4.

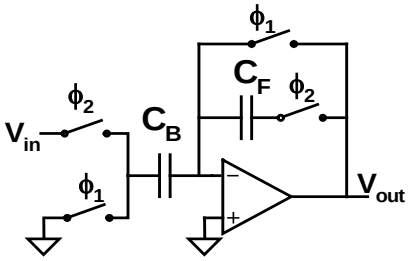
$$H(s) = \frac{-Gain}{1 + \frac{s}{2\pi GBW/Gain}} \approx \frac{1}{\frac{s}{2\pi GBW}} \quad \text{Equation 4}$$

For frequencies greater than the roll-off point, this transfer function approximates an integrator.

For close loop control circuits, an integrator can be used in lieu of an opamp.

A switched capacitor integrator is shown in Figure 4.

Figure 4. Switched Capacitor Integrator




The transfer function is shown in Equation 5.

$$H(s) = \frac{-\left(1 + \frac{s}{2f_s}\right)}{\left(\frac{s}{f_s C_B/C_F}\right)} \approx \frac{-1}{\left(\frac{s}{f_s C_B/C_F}\right)} \quad \text{Equation 4}$$

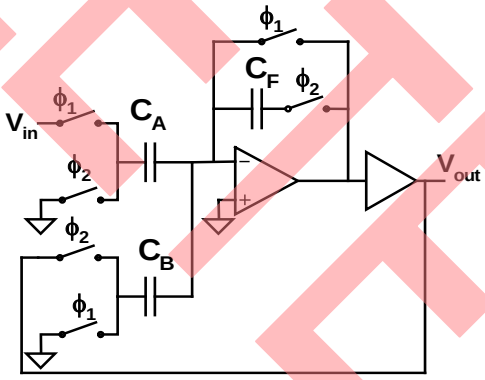
Combining Equations 4 and 5 produce the gain bandwidth value for a switched capacitor integrator, shown in Equation 6.

$$GBW = \frac{f_s}{2\pi}\frac{C_B}{C_F} \quad \text{Equation 5}$$

Changing the values of $C_B$, $C_F$, or $f_s$ alters the gain bandwidth. Flexible control of **GBW** allows the user to design a stable, closed loop feedback system.

A differential input integrator is shown in Figure 5.

Figure 5. Differential Input Integrator

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The output of the integrator is connected to an analog buffer and brought out to a pin. This analog output is fed back to a pin having a negative (**$C_B$**) input to the integrator. The transfer function is shown in Equation 7.

$$H(s) = \cdot \frac{\frac{C_A}{C_B}\left(1+\frac{s}{2f_s}\right)}{\frac{s}{f_s}\left(\frac{C_F}{C_B}+\frac{1}{2}\right)+1} \approx \frac{\frac{C_A}{C_B}}{\frac{s}{f_s}\left(\frac{C_F}{C_B}+\frac{1}{2}\right)+1}$$ Equation 6

This transfer equation is that of a single pole low pass filter with gain. The general form is shown in Equation 8.

$$H(s) = \cdot \frac{Gain}{\frac{s}{2\pi f_0}+1}$$ Equation 7

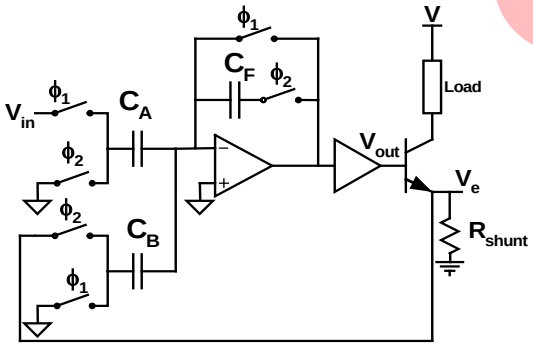
Combining these two equations result in the gain (Equation 9) and the roll-off frequency (Equation 10).

$$Gain = \cdot \frac{C_A}{C_B}$$ Equation 8

$$f_0 = \frac{f_s}{2\pi\left(\frac{C_F}{C_B}+\frac{1}{2}\right)}$$ Equation 9

To make a current source, a bipolar transistor is added to the output of a differential integrator. The transistor's emitter is fed back to the negative input. The schematic is shown in Figure 6.

Figure 6. Faux Opamp Current Source




Its operation is defined in Equations 11 and 12.

$$V_{out} = V_{in}\frac{C_A}{C_F}\frac{1+\frac{s}{f_s}}{\frac{s}{f_s}} - V_e\frac{C_B}{C_F}\frac{1+\frac{s}{f_s}}{\frac{s}{f_s}}$$ Equation 10

$$V_e = V_{out} - v_{be}$$ Equation 11

Combining these two equations to solve for **$V_e$**, results in Equation 13.

$$V_e = V_{in}\frac{\frac{C_A}{C_B}\left(1+\frac{s}{2f_s}\right)}{\frac{s}{f_s}\left(\frac{C_F}{C_B}+\frac{1}{2}\right)+1} - v_{be}\frac{\frac{s}{f_s}\frac{C_F}{C_B}}{\frac{s}{f_s}\left(\frac{C_F}{C_B}+\frac{1}{2}\right)+1}$$ Equation 12

The output voltage at the emitter is a function of **$V_{in}$** and the base emitter voltage drop **$v_{be}$**. Note that the transfer function for contribution **$v_{be}$** provides a high pass filter. Because **$v_{be}$** is a DC value, nothing is contributed. This leads to a more simplified Equation 14.

$$\frac{V_e}{V_{in}} = \frac{\frac{C_A}{C_B}\left(1+\frac{s}{2f_s}\right)}{\frac{s}{f_s}\left(\frac{C_F}{C_B}+\frac{1}{2}\right)+1} \approx \frac{\frac{C_A}{C_F}}{\frac{s}{f_s}\left(\frac{C_F}{C_B}+\frac{1}{2}\right)+1}$$ Equation 13

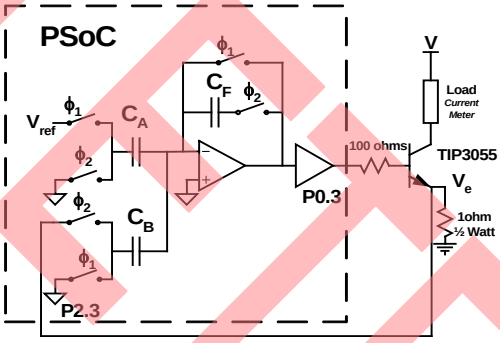
Again, this transfer function is a single pole low pass filter with gain. Its gain and roll-off values are the same as those defined in Equations 9 and 10.

The resistor at the emitter converts this voltage to a current. This current flows through the collector to the load.

## So Build Something Already

This example is a 500 mA current source. Its schematic is shown in Figure 7.

Figure 7. 500 mA PSoC Current Source Implementation




A 100 ohm resistor is in series with the base of the transistor. This isolates the analog buffer from the input capacitance of the power transistor's base emitter junction to guarantee stable operation of the output buffer. Figure 8 shows the user module placement for this example.

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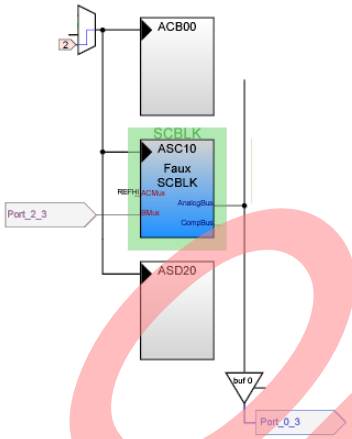
Figure 8. Current Source User Module Placement




Several system parameters must be set. They are:

- **Set AGND to $V_{bg}$ (1.3V)**. This sets the analog ground 1.3 volts above $V_{SS}$.
- **Set Vref to $V_{bg}$.**
- **Set VC2 to 1 MHz**. This value is selected as the column clock frequency.

$$f_s = \frac{f_{cc}}{4} = \frac{1.0MHz}{4} = 250kHz \qquad \text{Equation 14}$$

This is a good sample frequency for an autozeroed integrator.

The global resources are shown in Figure 9.

Figure 9. Global Resources for 500 mA Current Source

| Global Resources | |
|---|---|
| CPU_Clock | 3_MHz (SysClk/8) |
| 32K_Select | Internal |
| PLL_Mode | Disable |
| Sleep_Timer | 512_Hz |
| VC1= SysClk/N | 6 |
| VC2= VC1/N | 4 |
| VC3 Source | SysClk*2 |
| VC3 Divider | 256 |
| SysClk Source | Internal 24_MHz |
| SysClk*2 Disable | Yes |
| Analog Power | SC On/Ref High |
| Ref Mux | BandGap+/-BandGap |
| AGndBypass | Disable |
| Op-Amp Bias | Low |
| A_Buff_Power | Low |
| SwitchModePump | OFF |
| Trip Voltage [LVD (SMP)] | 4.64V (5.00V) |
| LVDThrottleBack | Disable |
| Supply Voltage | 5.0V |
| Watchdog Enable | Disable |

To generate 500 mA, a 1 ohm resistor is used. $V_e$ must be set to be ½ volt above $V_{SS}$. This resistor dissipates ¼ watt of power. A ½ watt resistor was selected. With **$V_{ss}$** selected to be 1.3V below ground, Equation 16 defines the required value of **$V_e$**.

$$V_e = V_{ss} + .5v = -1.3v + .5v = -.8v \qquad \text{Equation 15}$$

Using the gain equation (Equation 9), Equation 17 gives the value of $V_e$ as a function of **$V_{ref}$**, **$A_{sign}$**, **$C_A$**, and **$C_B$**, the gain equation.

$$V_e = A_{sign} \cdot V_{ref} \cdot \frac{C_A}{C_B} \qquad \text{Equation 16}$$

Equation 17 is rearranged and shown in Equation 18.

$$A_{sign} \frac{C_A}{C_B} = \frac{V_e}{V_{ref}} = \frac{-.8v}{1.3v} \qquad \text{Equation 17}$$

One solution for Equation 18 is given in Equation 19.

$$\begin{aligned} C_A &= 16 \\ C_B &= 26 \\ A_{sign} &= Neg \end{aligned} \qquad \text{Equation 18}$$

With these values for **$C_A$**, **$C_B$**, and **$A_{sign}$** and setting the other parameters to configure a differential autozeroed integrator, the SCBlock is fully parameterized. The parameter selection is shown in Figure 10.

Figure 10. Parameter Selection for Faux SCBlock

Faux

| User Module Parameters | |
|---|---|
| FCap | 32 |
| ClockPhase | Norm |
| ASign | Neg |
| ACap | 16 |
| ACMux | REFHI |
| BCap | 26 |
| AnalogBus | AnalogOutBus_0 |
| CompBus | Disable |
| AutoZero | On |
| CCap | 0 |
| ARefMux | AGND |
| FSW1 | On |
| FSW0 | Off |
| BMux | Port_2_3 |
| Power | High |

Adapted from the equation, the roll-off frequency is calculated as shown in Equation 20.

$$f_0 = \frac{f_s}{2\pi\left(\frac{C_F}{C_B} + \frac{1}{2}\right)} = \frac{250kHz_s}{2\pi\left(\frac{32}{26} + \frac{1}{2}\right)} = 23.0kHz \qquad \text{Equation 19}$$

For a DC current source, a roll-off frequency of 23 kHz, allows for fast response to load changes.

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## Now for the Software

There isn't any! The SCBlock is configured at start up and immediately starts functioning as a current source. Most users choose not to have to write any 'C' code. Those uncomfortable or inexperienced with 'C' may choose not to write any assembly code.

## But I Don't Have a Port 2

The previous solution had $V_e$ coming in on one of the port 2 switched capacitor inputs. This allows it a range that includes the supply rails. It also requires the use of a port 2 switched capacitor input. If you don't have a port 2, you are not out of luck. There are two solutions.

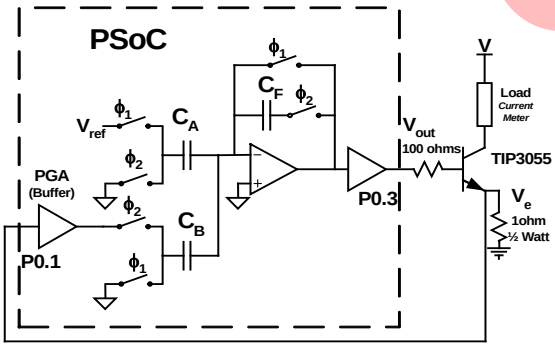
### The Marketing Solution

Have you considered getting a part that includes port 2? Think of it as "super sizing" your order. For a few more pennies per pin you can get at least eight more general-purpose I/O pins, some with switched capacitor inputs. How many times at a project's conclusion have you wished you had fewer resources?

### The Technical Solution

Figure 11 looks like the implementation in Figure 2 except that $V_e$ now feeds a Programmable Gain Amplifier **(PGA)** configured as a unity gain **Buffer**. The PGA input is on Port 0[2]; its output is fed directly into the B input of the differential integrator.

Figure 11. 500 mA PSoC Current Source Buffer Input Implementation

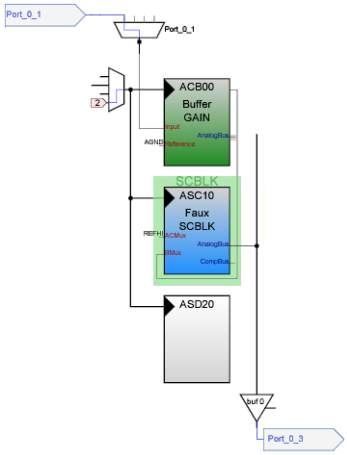



Whenever a component is added to a feedback loop, the question of stability arises. Will this circuit be stable? Applying the defined parameters to Equation 6, results gain bandwidth value. It is shown in Equation 21.

$$GBW = \frac{f_s}{2\pi}\frac{C_B}{C_F} = \frac{250kHz}{2\pi}\frac{26}{32} = 32.3kHz \qquad \text{Equation 20}$$

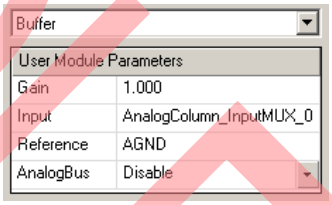
A PGA (unity gain, high power) has a 3 dB roll-off point of about 6 MHz. At 32 kHz, this buffer adds no significant phase shift to the signal. This implementation is unconditionally stable. The block placement is shown in Figure 12.

Figure 12. Current Source with Buffered Feedback User Module Placement




The parameter selection for the PGA buffer is shown in Figure 13.

Figure 13. Analog Buffer Parameters




The only change to the SCBlock parameters is to connect the input to $C_B$ from port 2[3] to the output of the buffer (**ACB00**) as shown in Figure 14.

Figure 14. SCBlock B Input Parameter Selection

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## Software?

An API call is required to power on the PGA **Buffer**. Code 1 shows how it is done in 'C'.

Code 1.

```
Buffer_Start(Buffer_HIGHPOWER);
```

Code 2 shows the assembly implementation.

Code 2.

```
mov  A,Buffer_HIGHPOWER
call Buffer_Start
jmp _main
```

## About the Author


**Name**: Dave Van Ess

**Title**: Staff Applications Engineer

**Background**: BSEE from University of California, Berkeley.

More than 27 years experience in circuit, signal processing, digital, software, analog, and system design.

Holder of five U.S. patents (plus three pending) for medical systems and signal processing. Holder of one U.S. patent (plus one pending) for PSoC enhancements. Author of numerous application notes and technical articles.

Joined Cypress in 2000.

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## Summary

Switched capacitor blocks are easily configured to be integrators. When configured as an integrator, a switch capacitor block can function as an op-amp. Parameterization of the capacitor values and sample frequency allow precise control of its gain bandwidth, insuring closed loop stability. The addition of an external pass transistor and current setting resistor, allows easy construction of a current.

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# Document History

**Document Title: Programmable Analog High Current Source, PSoC® 1 Style – AN2203**

**Document Number: 001-32909**

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 1494923 | DWV | 09/21/07 | Recataloged application note. |
| *A | 2577399 | YJI | 10/03/08 | Added part CY29xxx to associated parts. |
| *B | 3223406 | YJI | 04/12/11 | Application note updated for PSoC Designer 5.1 SP1 |
| *C | 4345951 | RJVB | 04/14/2014 | Obsolete document.<br>Completing Sunset Review. |

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In March of 2007, Cypress recataloged all of its Application Notes using a new documentation number and revision code. This new documentation number and revision code (001-xxxxx, beginning with rev. **), located in the footer of the document, will be used in all subsequent revisions.

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