AN206426

FR Family, All series, Setting initialization reset and Operation Initialization reset

The reset operations of the FR family are classified into two levels, each of which has different causes and initialization operations.

Contents

1 Reset Level....1
1.1 Settings Initialization Reset (INIT)....1
1.2 Operation Initialization Reset (RST)....1
2 The difference of register value after each reset....2
2.1 RSRR: reset source register....2
2.2 STCR: Standby control register....2
2.3 TBCR: Time base counter control register....2
2.4 CLKR: Clock source control register....2
2.5 DIVR0: Base clock division setting register 0....3
2.6 DIVR1: Base clock division setting register 1....3
2.7 OSCCR: Oscillation control register....3
2.8 OSCR: Main oscillator stabilization time control register....3
Document History....4
Worldwide Sales and Design Support....5

1 Reset Level

The reset operations of the FR family are classified into two levels, each of which has different causes and initialization operations.

1.1 Settings Initialization Reset (INIT)

The highest-level reset, which initializes all settings, is called a settings initialization reset (INIT).

1.2 Operation Initialization Reset (RST)

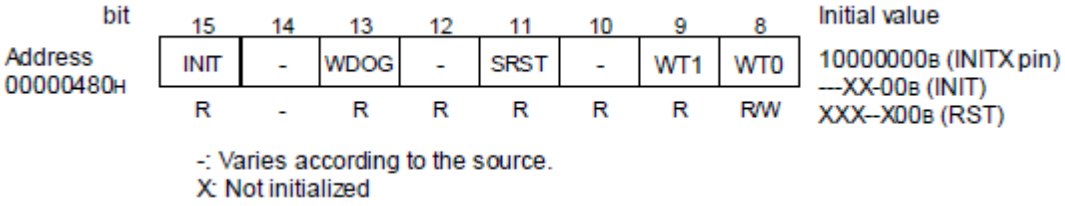
A normal-level reset that initializes the operation of a program is called an operation initialization reset (RST). If a settings initialization reset (INIT) occurs, an operation initialization reset (RST) also occurs.

But after RST, the initial value at some registers are different after INIT such as internal clock settings, PLL settings, divided gear settings, and clock stabilization time settings.

2 The difference of register value after each reset

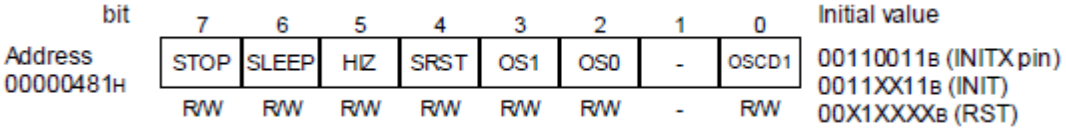
2.1 RSRR: reset source register

Figure 1. RSRR



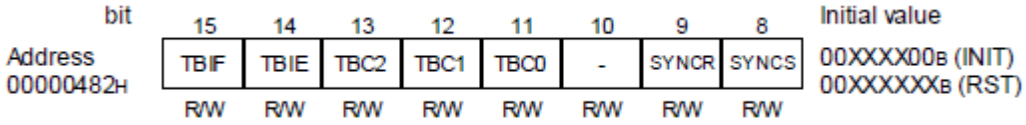
2.2 STCR: Standby control register

Figure 2. STCR



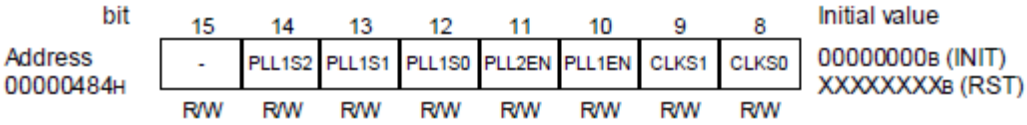
2.3 TBCR: Time base counter control register

Figure 3. TBCR



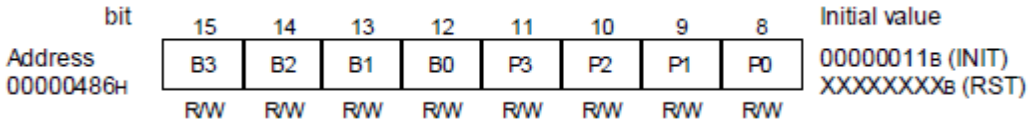
2.4 CLKR: Clock source control register

Figure 4. CLKR



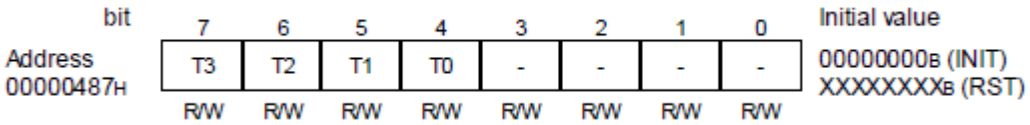
2.5 DIVR0: Base clock division setting register 0

Figure 5. DIVR0



2.6 DIVR1: Base clock division setting register 1

Figure 6. DIVR1



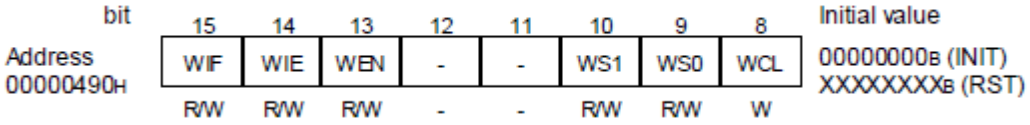
2.7 OSCCR: Oscillation control register

Figure 7. OSCCR

Bit	7	6	5	4	3	2	1	0
Address : 0000048Ah	—	—	—	RTCSRC	—	—	—	OSCDS1
	—	R/W	R/W	R/W	—	—	—	R/W
INIT	×	0	0	0	×	×	×	0
RST	×	×	×	×	×	×	×	0

2.8 OSCR: Main oscillator stabilization time control register

Figure 8. OSCR



Document History

Document Title: AN206426 - FR Family, All series, Setting initialization reset and Operation Initialization reset

Document Number: 002-06426

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	YUIS	03/21/2008	First Edition
*A	5294865	YUIS	06/02/2016	Migrated Spansion Application Note “AN07-00162-1E” to Cypress format.
*B	5876213	AESATMP9	09/07/2017	Updated logo and copyright.

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Videos | Blogs | Training | Components

Technical Support

cypress.com/support

All other trademarks or registered trademarks referenced herein are the property of their respective owners.

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

© Cypress Semiconductor Corporation, 2008-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.